Implementation of a Doped Pocket Region in Order to Enhance the Device Performance of MOSFET

Prasenjit Saha and Bijoy Goswami

Abstract The majority carrier concentration in the channel of an n-MOSFET is increased by inserting a moderately doped pocket region at the bottom of the substrate which is partially below the source and gate. Base of the substrate is insulated by SiO_2, so that there is least possibility of leakage through it. The device designed is of 20 nm channel length, and a simulation-based study has been carried out. In order to perform analysis and comparison, the same is designed with 30–40 nm channel length and conventional MOSFET of 30–40 nm is designed. Device characteristics obtained from the simulation shows that it follows characteristics of the conventional MOSFET. On comparing the drain current of the modified MOSFET with the conventional one, the modified structure performs better. On performing leakage current analysis, it is found that the modified MOSFET has a smaller value than the conventional MOSFET.

Keywords Conventional MOSFET · Modified MOSFET · Leakage current · Channel length

1 Introduction

The demand for faster cheaper and smaller devices has led to the downscaling of MOSFETs to well below 30 nm for VLSI application, and has successfully been fabricated and characterized [1, 2]. However, with a decrease in the channel length, the device performance is found to be continuously degrading, because many physical barriers arise like short-channel effects, drain-induced barrier lowering, punch through, etc. [3, 4]. One of the main technological roadblocks when we scale these devices beyond some limit is that the high mechanical leakage current penetrates through the gate oxide and it increases the power dissipation [5]. The direct tunneling current increases exponentially with the decrease in oxide thickness which is of

P. Saha (✉) · B. Goswami
Department of ETCE, Jadavpur University, Kolkata, India
e-mail: prasenj1ps@gmail.com

R. Bera et al. (eds.), *Advances in Communication, Devices and Networking*,
Lecture Notes in Electrical Engineering 537,
https://doi.org/10.1007/978-981-13-3450-4_4

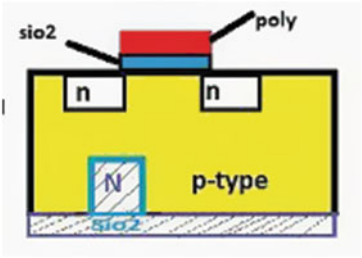

Fig. 1 Modified MOSFET structure of 22 nm × 60 nm

primary concern of MOS scaling [6, 7]. From research of recent years, it is seen that the modified structures like double gate, triple structure, and gate around structures are found to be more promising than the conventional model. The structure is shown in Fig. 1.

2 Device Structure and Simulation Setup

In the n-MOSFET, the majority carriers in the channel are electrons. The drain current at a corresponding gate and drain voltage can be increased if the electron density in the channel increases, correspondingly the hole concentration decreases. In order to enhance the electron concentration in the channel, an n-type moderately doped region is inserted in the substrate [8]. The doped region in the substrate is positioned in such a way that it is below the half of source and the channel. The holes in the channel are attracted by the introduced moderately doped region in the substrate, thereby increasing the electron concentration in the channel. Since the doped region introduced is layering in the substrate, there may be some leakage. Therefore, the base of the substrate is insulated by SiO_2, which is of 1 nm thickness, so that there is no possibility of leakage through the substrate [9, 10]. Figure 2 shows the structure formation.

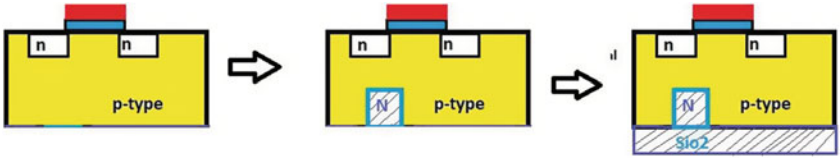

Fig. 2 Structure formation

2.1 Fabrication Steps

A moderately doped region is inserted in a p-type silicon substrate using N-well process. After the formation of the SiO_2 layer using oxygen ion implantation technology [11], the structure is first rotated 180° vertically [12] and horizontally. Now using the fabrication of conventional n-MOSFET, the complete structure can be developed. Figure 3 shows the fabrication steps.

2.2 Simulation Setup

A 20 nm n-MOSFET with the doped region in the substrate is designed using the ATLAS simulator of the Silvaco TCAD, and then the same device has been also designed for the channel length of 30–40 nm to a make comparison with varying channel length. 30–40 nm conventional MOSFET is designed to find the comparison with the new doping of MOSFET. Figures 4 and 5 show the structure designed.

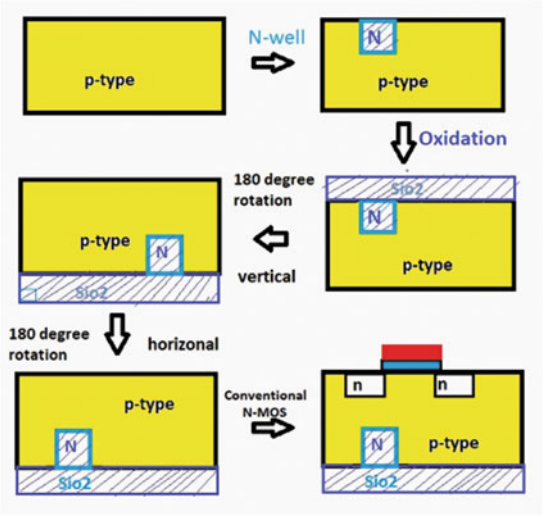

Fig. 3 Fabrication steps

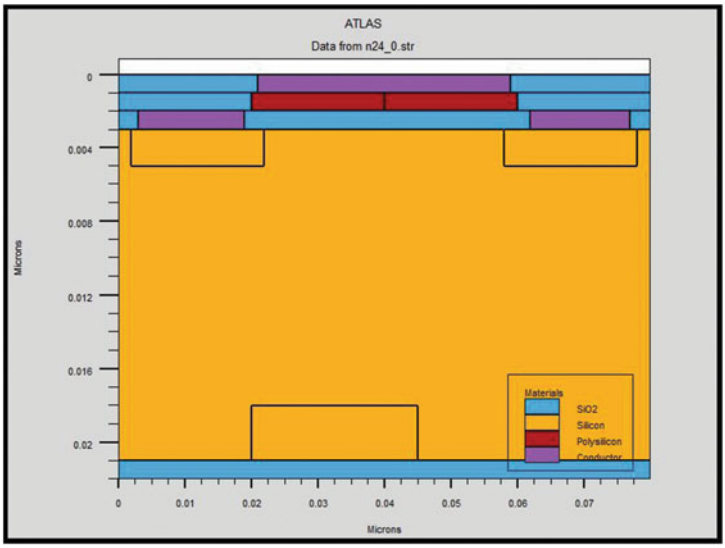

Fig. 4 40 nm modified MOSFET

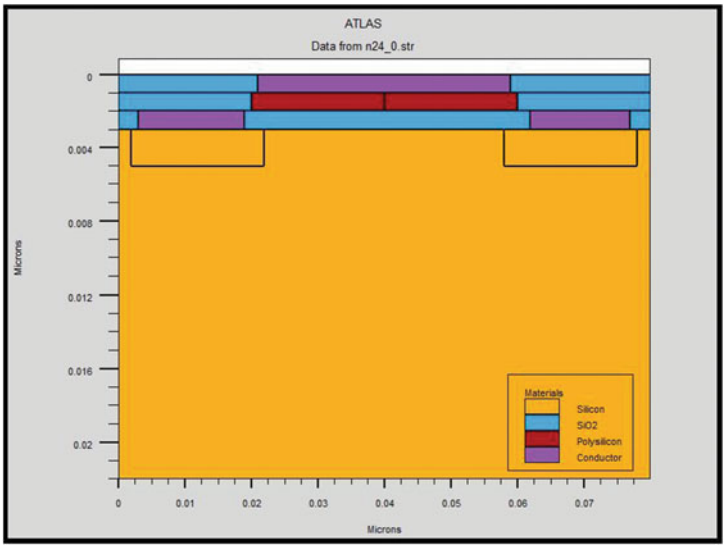

Fig. 5 40 nm conventional MOSFET

3 Results and Discussions

3.1 Drain Biasing

The drain is biased with $V_d = 0.1$ V and the gate voltage is varied with 0–3 V to obtain the I_d versus V_g characteristics for 20, 30, and 40 nm modified n-MOSFET. Figure 6 shows the I_d–V_g characteristics.

The graphs show the I_d–V_g characteristics of the modified n-MOSFET for 40, 30, and 20 nm channel length. On comparing them, we can observe that as channel length decreases the slope of the curve increases which follows the characteristics of the conventional MOSFET.

3.2 Gate Biasing

The gate is biased with $V_g = 1.1$, 2.2, and 3.3 V, and the drain voltage is varied from 0 to 3 V to obtain the I_d versus V_{ds} curve. And a comparison is done among 20, 30, and 40 nm.

The graphs showing the I_d–V_d characteristics of the modified n-MOSFET for 20 nm channel length is shown in Fig. 7. On comparing them, we can observe that

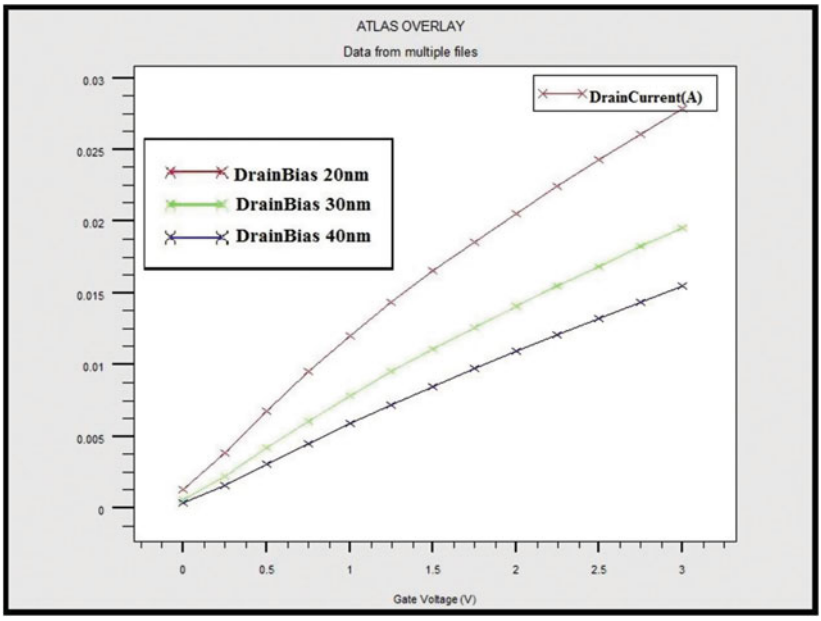

Fig. 6 Drain current obtained at $V_g = 3$ V

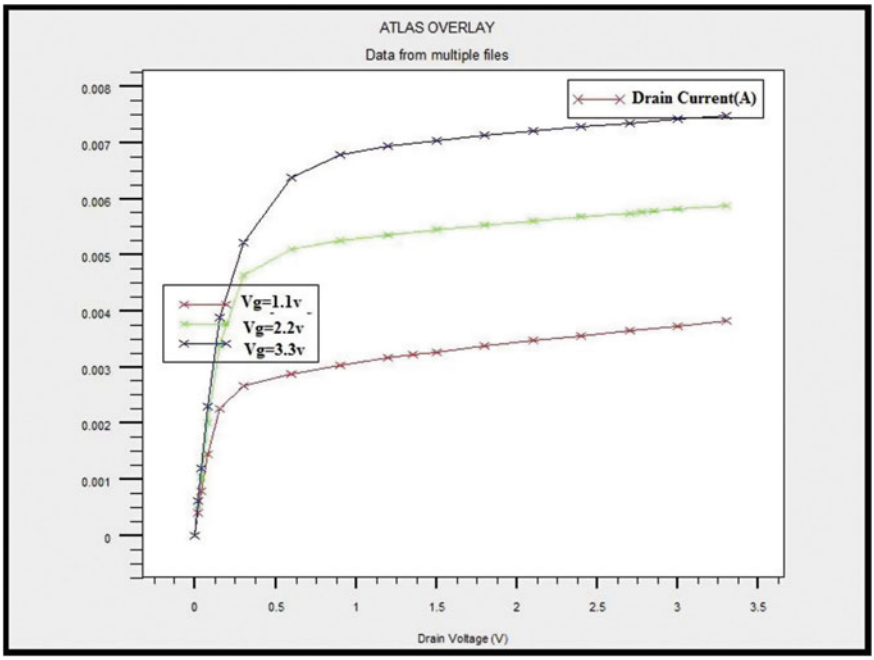

Fig. 7 I_d–V_d characteristics for 20 nm channel length

as channel length decreases the slope of the curve increases, thus yielding a higher drain current and it follows the characteristics of the conventional MOSFET.

3.3 Comparison of Conventional MOSFET and Proposed MOSFET

Drain Biasing: Drain biasing is performed on both the structures and a comparison is made for 40 nm channel length. Figure 8 shows the results obtained for the comparison on the drain biasing.

The slope of the characteristics is equal to 1/Ron. If we compare both, we can see that the new MOSFET has a greater slope than the conventional MOSFET; hence, it has a greater drain current than the conventional one.

Gate Biasing: The gate is biased with $V_g = 1.1$, 2.2, and 3.3 V, and the drain voltage is varied from 0 to 3 V to obtain the I_d versus V_{ds} curve. And a comparison is done among 40 nm. Both have a 40 nm channel length, which follows the characteristics of the conventional MOSFET. On comparing the characteristics of both the devices, we can see that the new MOSFET has a greater slope than the conventional

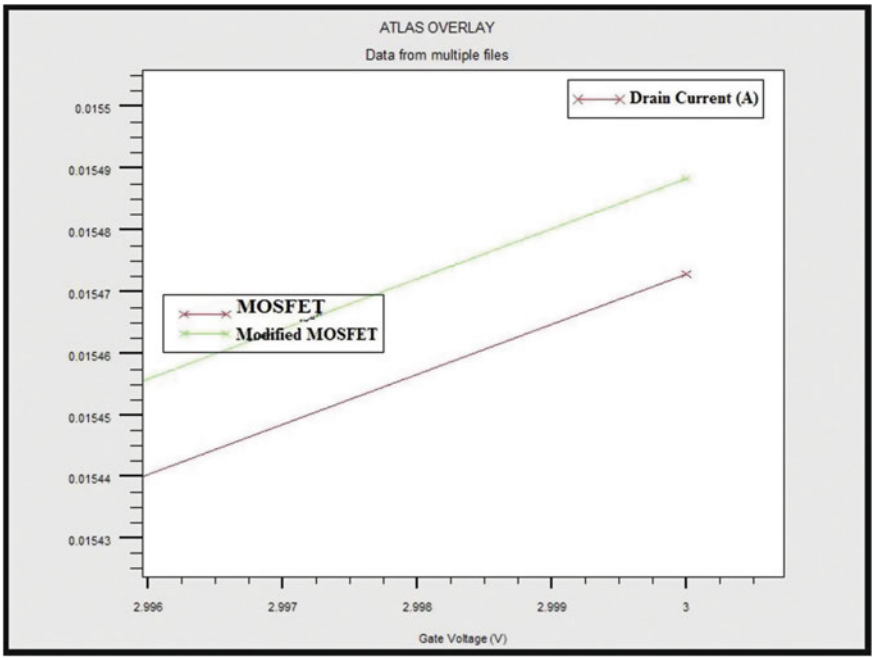

Fig. 8 I_d versus V_g curve for 40 nm

MOSFET in all gate voltages of 1.1, 2.2, and 3.3 V; hence, it yields a greater drain current than the conventional one.

Leakage Current Analysis: Leakage current analysis is performed on the MOSFETS with channel length of 30 nm and 40 nm and a comparison is done between the devices at respective channel lengths. The results obtained for 30 nm are shown in Fig. 9.

It is observed that the leakage current is minimized; in case of 30 nm it is 1.154 mA less, and in case of 40 nm it is 5 uA less than the conventional MOSFET.

4 Conclusion

The results obtained from the drain and gate biasing signify that the MOSFET with the newly introduced doped region obeys the characteristics of the conventional MOSFET. On comparing the drain current of modified MOSFET with the conventional MOSFET at different conditions of gate voltage, drain voltage, and channel length, the modified MOSFET has a higher value, and thus the gain will be higher. The leakage current of the modified MOSFET is found to be less than the conventional MOSFET, and hence the power consumption will be minimized.

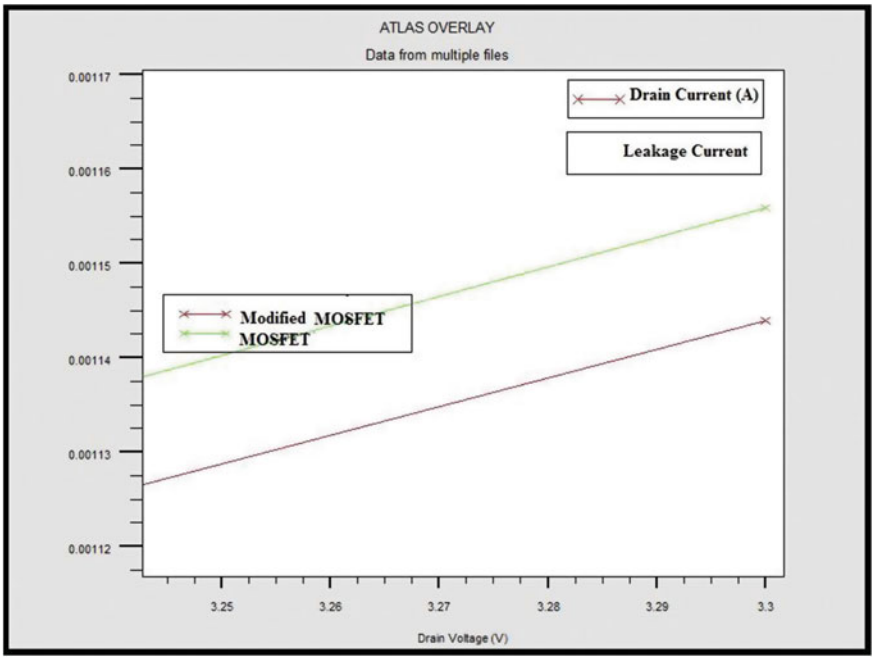

Fig. 9 Leakage current comparison at 30 nm channel length

References

1. Emerging research devices, International technological roadmap semiconductors (2009)
2. Packan P (1999) Pushing the limits. Science 285(5436):2079–2081
3. Banerjee P, Sarkar SK (2017) 3-D analytical modelling of dual-material triple gate silicon-on-nothing MOSFET. IEEE Trans Electron Devices 64(2)
4. Shrivastava A, Tripathi N, Agarwal E, Singh A (2015) Comparative study of double gate soi MOSFET and single gate soi MOSFET through simulation. IJEEE 07(01). ISSN: 2321-2055 (E)
5. Sacconi F, Carlo AD, Lugli P, Stadile M (1980) Full band approach to tunneling in MOS structures. IEEE Trans Electron Devices 22(11)
6. Chang L, Yeo YC, Polishchuk I, King TJ, Hu C (2002) Direct-tunneling gate leakage current in double-gate and ultrathin body MOSFETs. IEEE Trans Electron Devices 49(12)
7. Choi CH, Yu Z, Dutton RW (2001) Impact of gate tunneling current in scaled MOS on circuit performance: a simulation study. IEEE Trans Electron Devices 48(12)
8. Sze SM, Ng KK (2014) Physics of semiconductor devices (Chapter 7), 3 ed, p 376. ISBN: 978-8126517022
9. Sano E, Kasai R, Ohwada K, Ariyoshi H (1980) A two dimensional analysis for MOSFET's fabricated on buried SiO_2 layer. IEEE Trans Electron Devices 22(11)
10. Duan, B, Yang Y (2011) REBULF super junction MOSFET with N+ buried layer. Micro Nano Lett
11. Ohwada K, Omura Y, Sano E (1981) A high-speed buried channel MOSFET isolated by an implanted silicon dioxide layer. IEEE Trans Electron Devices 28(9)
12. Gandhi SK (2013) VLSI Fabrication and principles: silicon and gallium arsenide (Chapter 11), 2nd ed, pp 710–711. ISBN: 978-8126517909