# Comparative Analysis of Standard 9T SRAM with the Proposed Low-Power 9T SRAM

**Balraj Singh, Mukesh Kumar and Jagpal Singh Ubhi**

**Abstract**   This paper presents a novel 9T SRAM (static random-access memory) cell design with reduced leakage power and high performance. The design makes use of a sleep transistor so as to curtail the leakage power by eliminating the formation of a direct connection between the supply voltage ($V_{DD}$) and ground. The results are compared with existing 9T SRAM cell with the same transistor sizing and parameter variations. The designed SRAM cell has decoupled read and write operations and is simulated using Cadence at 45 nm CMOS technology. At 0.8 V, the proposed cell has an improvement of 31.78% and 73.66% respectively in dynamic and static powers when compared with the reported 9T SRAM cell. Also, nearly 36% improvement in power delay product (PDP) is achieved with the proposed design.

**Keywords**   SRAM · Leakage power dissipation · Dynamic power · Static power
Transistor sizing · PDP

## 1   Introduction

In earlier times, the major challenges for the VLSI designer were area, performance, cost, and power consumption. In recent years, however, power consumption is being given comparable weight to area and speed considerations. With the technological developments, Moore's law has led to a much smaller integrated circuit technology. Amid the shrinking of the technology, the performance of the integrated circuits is enhanced but this improved performance comes with the cost of increases in leakage power, process variation, and power density. Today, most of the power systems

B. Singh · M. Kumar (✉) · J. Singh Ubhi
Department of ECE, SLIET, Longowal, India
e-mail: mukeshkumar@sliet.ac.in

B. Singh
e-mail: balraj@gmail.com

J. Singh Ubhi
e-mail: js_uhbi@yahoo.com

require high performance when in active state while a very low leakage when in idle/hold state [1]. It is important to note that the power dissipation parameters and some other parameters like propagation delay and PDP (Power Delay Product), all are interrelated. An improvement in one parameter leads to the degradation of other parameters [2]. The motivations for reducing power consumption differ from application to application and circuit to circuit. Downscaling and lower voltage activity are the most critical and supportive approaches to accomplish the low power and superior CMOS logic. Despite the way that the pattern of contracting gate length is exceptionally forceful nowadays and there are a few difficulties associated with having low power activity with gadgets having small dimensions.

An attempt with CMOS technology is used to observe the performance of NAND and NOR gate and conclude NAND gate has more advantages over NOR gate. Static power dissipation is 55.73% less, also having less area and less access time for NAND gate [3]. SRAM is primary memory block implemented in high-performance processors because of its compatibility with the logic. In fact, the biggest area in modern silicon on the chip is possessed with SRAM [4, 5]. SRAM has a vital role in ADC, cache memory, camera, electronic toys, mobile phone, etc. The main advantage of SRAM is that it need not refresh data periodically [6]. The outline of low-power SRAM is itself a monstrous test to manage. Further, scaling and the process variations are huge snags to low power SRAM outline. As the supply voltage diminishes, SRAM must be consistent with the working conditions. However, with low-voltage task in SRAM, designers need to confront a few difficulties like process variations, bit cell stability, detecting and dependability of the entire memory. The upside of SRAM is the low power utilization, yet to configuration low power, planner needs to deal with the area and performance trade-off. For enhancing these areas and execution metrics, additionally makes a challenge to manage leakage current.

A Novel 9T SRAM cell is proposed with less leakage power and high performance. The measurement results of this cell are compared with the standard 9T SRAM cell and concluded it is 31.78% and 73.66% efficient for static power and dynamic power dissipation, respectively.

This paper is sorted out into following segments: Segment I enrolls a short presentation of past work done. Segment II has a talk on the activity of existing 9T SRAM cell. Segment III has centered around the operation of proposed 9T SRAM cell. In segment IV, simulated results are discussed along with graphs. Segment V has the comparison of results of novel 9TSRAM with existing. Segment VI has the conclusion of the paper.

## 2   Existing 9T SRAM Cell

First, the schematic of 9T SRAM cell with transistors sized for 45 nm CMOS technology is shown in Fig. 1. The SRAM can be thought as consisting of two parts namely upper subsystem and lower subsystem [7].
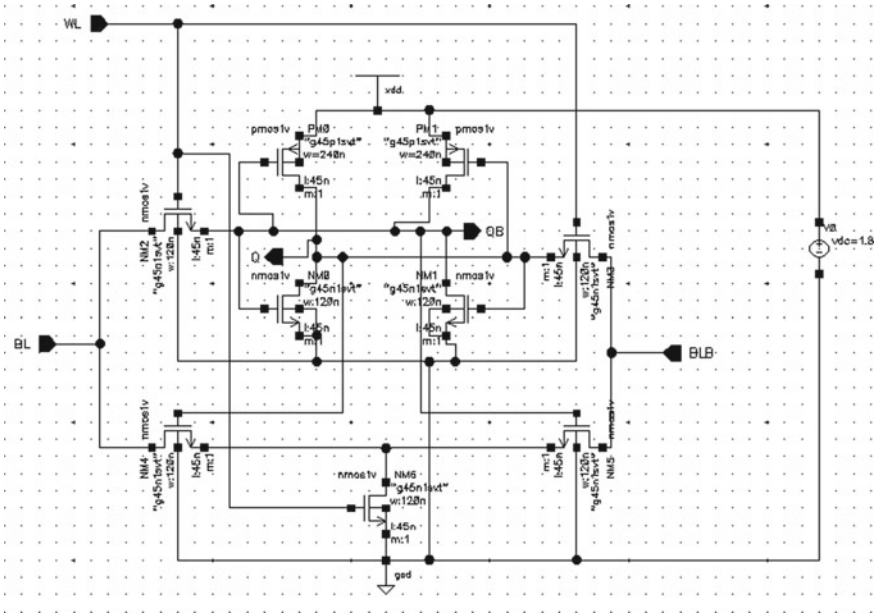
**Fig. 1** Schematic of the standard 9T SRAM cell [8]

The upper subsystem is basically a six transistor (6T) conventional SRAM cell consisting of four NMOS transistors from NM0 through NM3 and two PMOS transistors shown as PM0 and PM1 in Figure. The access transistors, named as NM2 and NM3, are controlled by the same word line (WL). The lower subsystem of the 9T SRAM cell consists of transistors NM4 through NM6, in which, NM4 and NM5 transistors act as access transistors for bit lines while transistor NM6 act as the read access transistor. The data stored in the cell control the operations of NM4 and NM5 transistors and a separate read line (RL) signal controls the transistor NM6. The gate of this NM6 transistor can also be connected to the WL instead of connecting a separate RL signal.

**Operations of the Cell**:

When write operation is performed, WL signal transitions are made HIGH while RL is kept LOW making NM6 OFF, the two access transistors NM2 and NM3 are turned ON. If one wishes to write bit '0' to node Q, then BL is discharged while BLB is charged. Bit '0' is stored in the SRAM cell through NM2. To write '1' at Q, the operations at BL and BLB are reversed, i.e., BL is charged and BLB is discharged.

While performing Read operation, RL is made to go HIGH and maintaining WL at LOW causing NM6 ON and NM2 and NM3 transistors OFF. If stores a '1' then BL is discharged through NM4 and NM6 and if QB stores a '1' then BLB is discharged through NM5 and NM6. Since during the Read it is seen from the operation that accesses transistors NM2 and NM3 are in cut off, the storage nodes Q and QB are
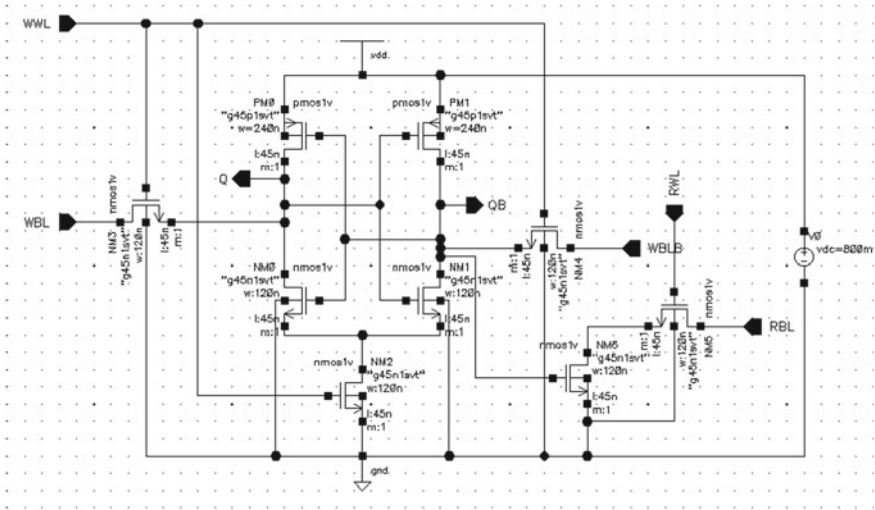
**Fig. 2** Schematic of proposed 9T SRAM cell

totally segregated from the bit lines. The read stability of this conventional 9T SRAM cell is improved compared to that of standard 6T SRAM cell as the voltage of the node which stores '0' is stringently kept at the ground during a read operation which is not so in case of standard 6T SRAM cell [7].

## 3 Proposed 9T SRAM Cell

The schematic of the proposed SRAM cell is shown in Fig. 2 which is supposed to be split into two parts: left sub-circuit of the SRAM cell consists of a traditional 6T SRAM cell with a sleep transistor at the bottom through which the cell is grounded. The right sub-circuit of the proposed cell consisting of two transistors used for Read operation.

In this 9T SRAM cell, read and write are controlled by separate devices within the cell as the two operations are entirely decoupled [9]. The transitions of the read word line (RWL) decide the read operation of the proposed cell. NM3 and NM4 act as the write access transistors which are guarded by the column based write word line (WWL) whose transitions control the write process of the SRAM cell. The bottom transistor NM2 is sized uniformly to that of cross-coupled inverters [10]. This is done as such as to coordinate their current conveying limit. Thus, by employing the extra transistor in the read stable 8T SRAM cell [9], the leakage or static power dissipation can be reduced.

**Operations of the Cell**:

For read operation, the row-based high going read word line and row-based gnd enable the two-stacked read port, and if QB = '1' the RBL would be discharged and sensing of Q = '0' will be done by the sense amplifier. When '1' is to be read reverse operation is performed. Generally, during read operation, RBL is pre-charged to VDD and WWL is kept LOW or at '0' volt. When WWL, WBL and WBLB are maintained LOW, the cross-coupled inverter get separated from the external interconnect and there is no intrusion effect in the latch [11]. Depending on the data associated in the cross-coupled inverters, RBL discharges or remain at VDD. If RBL discharges, it can be treated as the stored bit is supposed to be '1', otherwise, it is '0'. Therefore, it can be interpreted here that the read stack works indirectly to read the data from the latch.

To execute the write operation, read circuitry is disabled by keeping RWL at LOW level while WWL is asserted. But before asserting the write word line, the data is loaded onto the write bit lines (WBL and WBLB), i.e., write operation is initialized by pre-charging the WBL and WBLB signals. After pre-charging of write bit lines is done the asserting of the WWL signal makes the access transistors NM3 and NM4 to switch ON so as to access or pass the data from word bit line to the cell. Thus, data is placed into the cell at the respective nodes.

## 4 Simulation Results

The existing as well as the proposed SRAM cell has the width for the NMOS transistor as 120 nm while it is 240 nm for PMOS transistors. The length of each transistor used in the cell is taken as 45 nm. The simulation results for both the SRAMs are obtained for the same transistor sizing and other parameter variations.

A. **Transient and DC Responses for Existing 9T SRAM Cell**

The combined transient and DC responses are shown in the Fig. 3. The transient response is obtained for a period of 100 ns. The output Q varies with respect to BLB signal and gives the same value as BLB when WL is enabled. The case when WL is disabled/LOW, the output Q holds the previous value. DC response is obtained against the DC voltage applied.

B. **Transient and DC Responses for Proposed 9T SRAM Cell**

The transient and DC responses obtained for 45 nm node for the proposed 9T SRAM cell are combined together in Fig. 4. A 100 ns period is taken for the transient response. Owing to separate circuitries for write as well as read operation, timing control is an important aspect to obtain a response in this case.

The output Q in transient response follows WBLB and if WWL is HIGH Q changes accordingly as WBLB while it holds the previous state in case the WWL is LOW. The different plots in DC response are with respect to applied voltage.
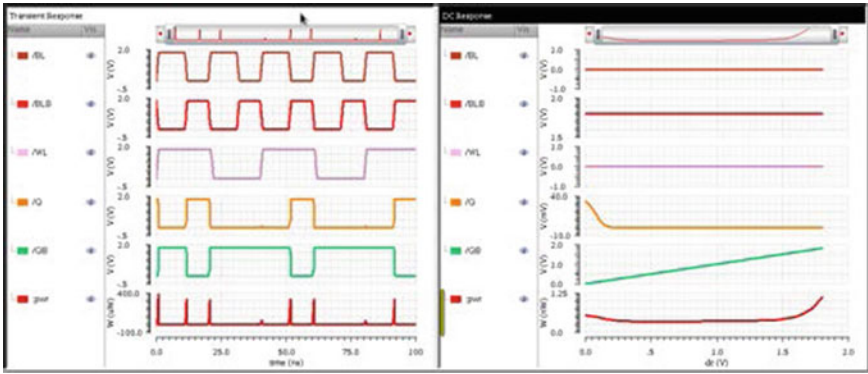
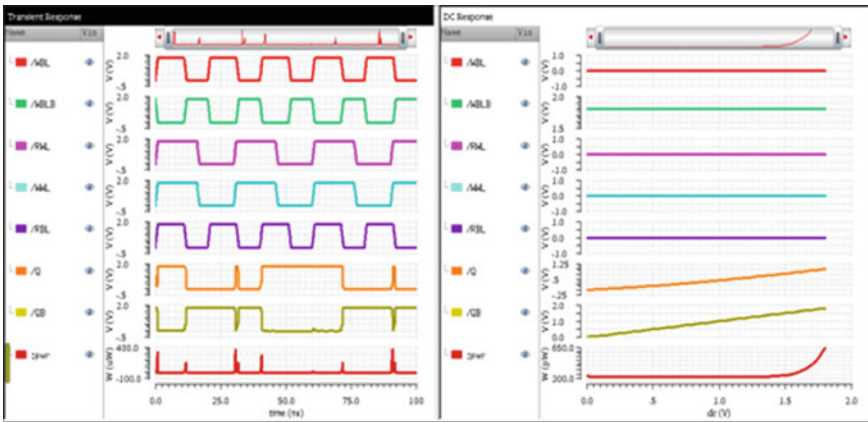**Fig. 3** Transient and DC responses for existing 9T SRAM cell



**Fig. 4** Transient and DC responses for the proposed 9T SRAM cell

## 5 Comparison Between the Existing and the Proposed 9T SRAM Cells

Nine transistor SRAM cells are compared with the same transistor features and other parameter variations. The results for both the SRAM cells are obtained at a temperature of 27 °C and with the same technology node of 45 nm.

**Dynamic and Static Power Against Applied Supply Voltage**

The comparison graph for the reported 9T SRAM cell and proposed 9T SRAM cell are shown in the Figs. 5 and 6.
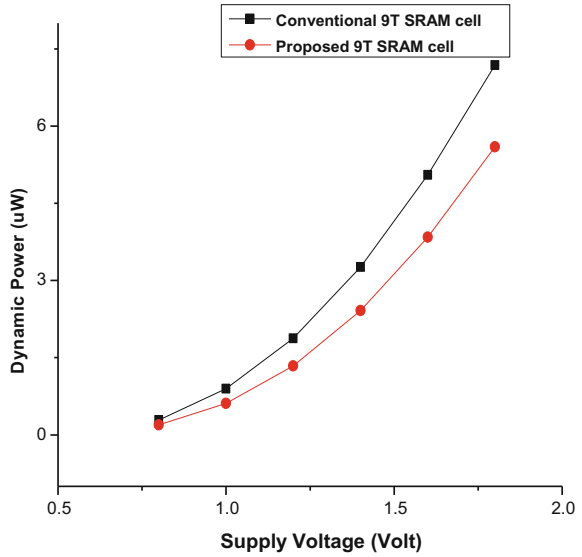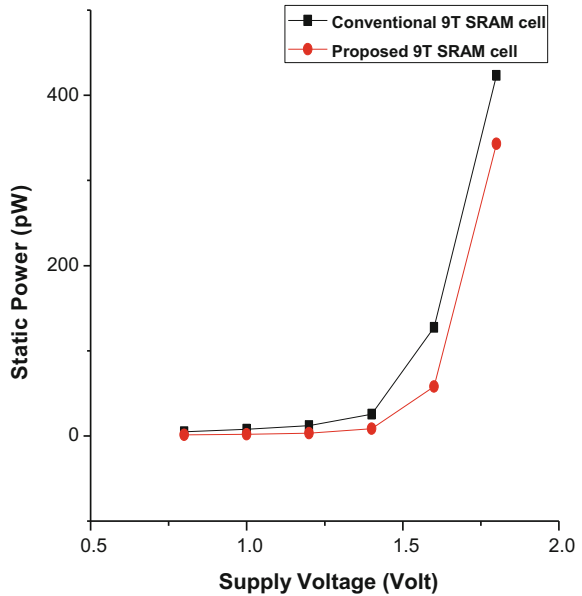
**Fig. 5** Dynamic power versus supply voltage



**Fig. 6** Static power versus supply voltage



## Various Timing Parameters with Voltage

The various timing parameters obtained through simulation results are the rise time, fall time, and delay. From the graphs plotted in Fig. 7, it can be interpreted that the rise time for the signal is higher in the case of proposed SRAM cell to that of

**Fig. 7** Time versus voltage
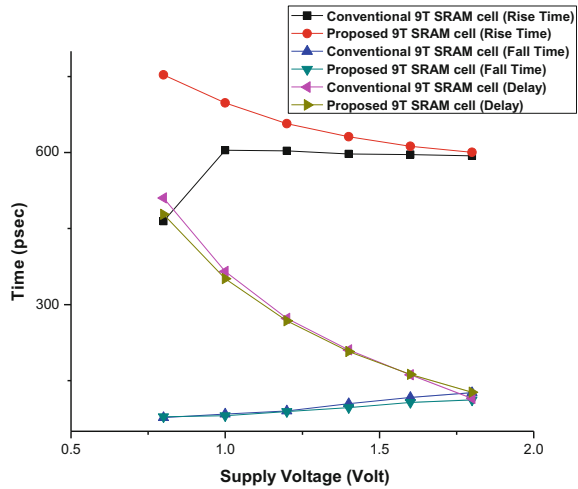


conventional SRAM cell. In other cases, i.e., fall time and delay, the results are better for the proposed 9T SRAM cell when compared with the existing SRAM cell.

**Different Parameter Variation with Temperature**

The dynamic power for both the SRAM cells is improved with the temperature while the static power and the delay parameters are degraded in case of existing as well as the proposed nine transistor SRAM cells.

From Fig. 8, it can be seen that the dynamic power varies nearly the same for two SRAM cells against the temperature. However, from Fig. 9, it can be observed that leakage power dissipation in reported 9T SRAM cell increases exponentially with the temperature while there is nearly a linear increase in case of proposed SRAM cell making it better in temperature varying environments.

It can be reported from the Fig. 10 that the variation in delay for the proposed cell with respect to temperature is nearly linear. At temperatures above 100 °C, the delay in the case of existing SRAM increases more while this increase for the proposed bit cell is very low.

**Comparison Between Power Delay Product (PDP)**

The power delay product for the two cells is shown separately in Table 1.

**Table 1** PDP comparison at different voltages

| Voltage (volt) | | 1.2 | 1.0 | 0.8 |
|---|---|---|---|---|
| PDP (Watt-femtosecond) | Existing 9T SRAM cell | 0.511 | 0.327 | 0.146 |
| | Proposed 9T SRAM cell | 0.359 | 0.214 | 0.093 |

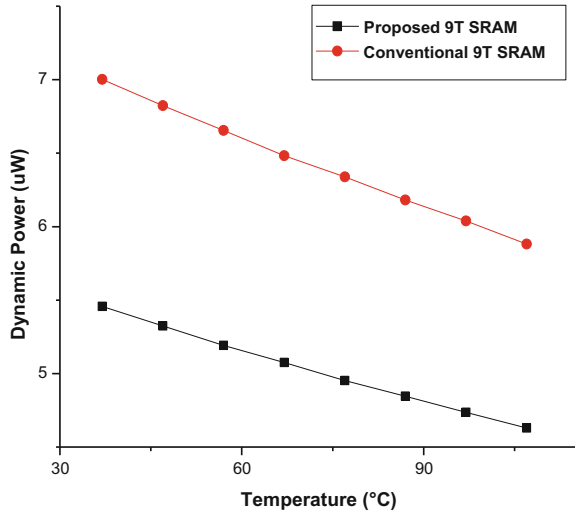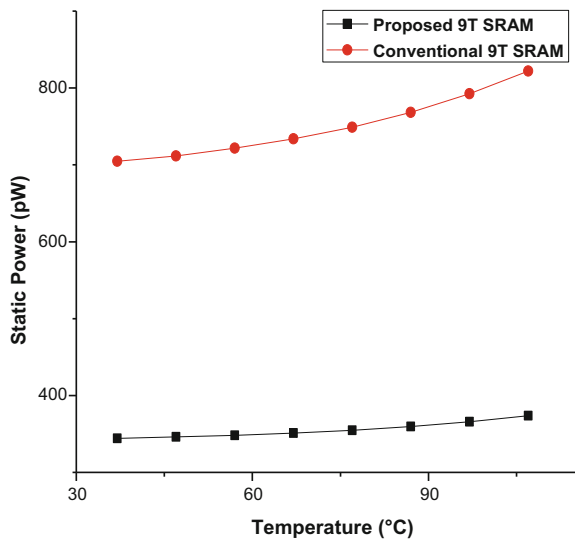**Fig. 8** Dynamic power versus temperature



**Fig. 9** Static power versus temperature



The power delay product for both the SRAM cells decreases as the voltage decreases. The variation with the voltage can be clearly observed from the combined graphs of power delay product with the voltage as shown in Fig. 11.

From the above Fig. 11, it can be clearly depicted that PDP value against the voltage is higher in case conventional 9T SRAM cell which is further degraded at lower voltages. The simulation results show that at 1.8 V, there is an increase of 13.73% in PDP for the conventional SRAM cell which increases to 36.30% when the applied voltage is reduced to 0.8 V. Therefore, from this, it can be interpreted that
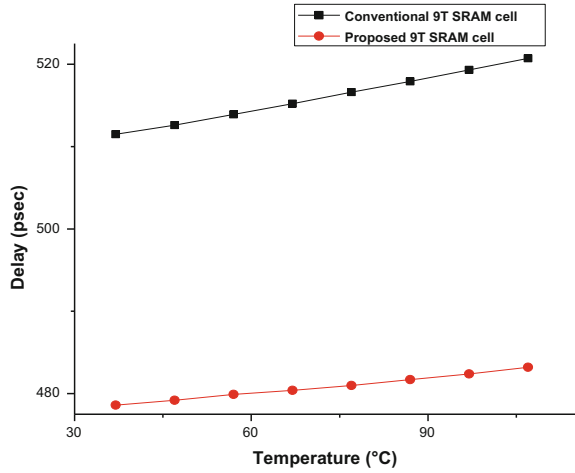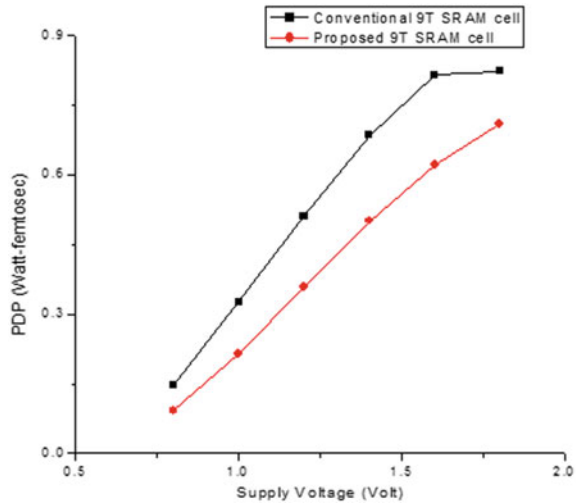
**Fig. 10** Delay versus
temperature



**Fig. 11** PDP versus supply
voltage



the PDP value increases in case of existing SRAM cell when the voltage is scaled
down. This makes the proposed SRAM cell a favorable choice for use over existing
SRAM cell.

## 6  Conclusion

The proposed SRAM cell shows better results at a higher temperature in contrast to
the reported bit cell in which the increase in leakage power with the temperature is
much higher than the former. The simulation results using Cadence Spectre show that

at 0.8 V the proposed cell has an improvement of 31.78% and 73.66% respectively in dynamic and static power when compared with the reported nine transistor SRAM cell. There is a little degradation of nearly 10.7% in propagation delay which makes the PDP to be improved by 13.73% at 1.8 V for the proposed cell. At a scaled voltage of 0.8 V, it exhibits an improvement of about 36.30% in PDP due to a step up of about 6% in propagation delay. Therefore, with the voltage getting scaled down, this improvement in PDP increases making the proposed SRAM cell better than the reported one at the same technology node.

# References

1. Weste, N.H.E., Harris, D., Banerjee, A.: CMOS VLSI Design, 3rd edn. Pearson Education
2. Rabaey, J.M., Kasan, A.C., Nikolic, B.: Digital Integrated circuits: A Design Perspective, 2nd edn
3. Singh, B., Kumar, M., Ubhi, J.S.: Analysis of CMOS based NAND and NOR gates at 45 nm technology. IJEECS **6**(4), 224–227 (2017)
4. Sinangil, M.E., Chandrakasan, A.P.: Application-specific SRAM design using output prediction to reduce bit-line switching activity and statistically gated sense amplifiers for up to 1.9 lower energy/access. IEEE J. Solid-State Circuits **49**(1), 107–117 (2014)
5. Rusu, S., et al.: A 65-nm dual-core multithreaded xeon processor with 16-MB L3 cache. IEEE J. Solid-State Circuits **42**(1), 17–25 (2007)
6. Kumar, M., Ubhi, J.S.: Performance evaluation of 6T, 7T & 8T SRAM at 180 nm technology. In: Presented in IEEE Conference held at IIT Delhi, July 2017
7. Liu, Z., Kursun, V.: Characterization of novel nine transistor SRAM cell. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **16**, 488–492 (2008)
8. Kao, J.T., Chandrakasan, A.: Dual-threshold voltage techniques for low-power digital circuits. IEEE J. Solid State Circuits, **35**(7), 1009–1018 (2000)
9. Chang, Leland, Montoye, Robert K., Nakamura, Yutaka, Batson, Kevin A., Eickemeyer, Richard J., Dennard, Robert H., Haensch, Wilfried, Jamsek, Damir: An 8T SRAM for variability tolerance and low voltage operation in high-performance caches. IEEE J. Solid-State Circuits **43**(4), 956–963 (2008)
10. Hentrich, D., Oruklu, E., Saniie, J.: Performance evaluation of SRAM cell in 22 nm predictive CMOS technology. In: IEEE International Conference on Electron/Information Technology, pp. 470–475 (2009)
11. Rahman, M.I., Bashar, T., Biswas, S.: Performance evaluation and read stability enhancement of SRAM bit-cell in 16 nm CMOS. In: 5th International Conference on Informatics, Electronics and Vision (ICIEV), pp. 713–718 (2016)