A 6-Bit Low Power SAR ADC

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Abstract. The design of a 6-bit, 100 MHz successive approximation register (SAR) analog to digital converter (ADC) is presented in this paper. The implemented SAR ADC is realized by using SAR logic, a 6-bit DAC, a sample and hold circuit and a comparator circuit. The fully realized system is measured under different input frequencies with a sampling rate of 100 MHz and it consumes 36.7 μW from a 1.8 V power supply. The ADC implemented in 130 nm CMOS technology exhibits signal-to-noise plus distortion ration SNDR of 64.2 dB and occupies a die area of 0.14 mm^2.

Keywords: Data converter · High linearity · Low power · Time-interleaving Comparator · Amplifier

1 Introduction

Physically most data in the real world is described by analog signals. In order to control/process the data using a microprocessor or microcontroller, a data converter circuit is very much indispensable. A data converter is a microelectronic circuit that is used to transform analog signal to digital signal or a digital signal to analog signal. Currently, there has been rapid progress in the design of electronic systems for various applications. The prominence of data converter circuits in the implementation of digital computers and signal processing in communications, image processing, instrumentation and industrial control systems is increasing by leaps and bounds. Hence data converter circuits are extensively used as interface between analog and digital circuits. In general there are two different types of data converter circuits. They are (i) Analog to Digital Converter (ADC) and (ii) Digital to Analog Converter (DAC). Analog to Digital Converter converts an analog signal (continuous time and continuous magnitude) into digital signals (discrete time and discrete magnitude).

ADCs are used in various applications such as Wireless Telecommunication circuits, Medical Imaging technologies, Audio and Video Processing Systems, Software radio and Instrumentation. Broadly there are numerous ADC architectures available to be used for these applications. But selection of an ADC is determined by the application and its specifications. However no single ADC architecture is found to be appropriate for all these applications. At present the major advances in consumer electronics are reflected in smart phones, notebook computers, camcorders, tablets and portable storage devices. All these devices employ various wireless technologies. Also

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wireless infrastructural systems such as satellite communication systems, cellular base stations, and various electronic warfare systems require the direct digitization of analog signal in the giga-hertz range. High resolution, High speed and low power consumption are the essential requirements in many wireless portable applications.

Different ADC architectures such as Flash type, Two-step flash type, Integrating type, Sigma-Delta, Pipeline and Interleaving are being used to deliver these requirements for various applications. The performance of an ADC is often affected by the nature of the input signal they process. Because the input analog signal is continuous in nature, ADCs suffer numerous problems such as clock jitter, nonlinear input impedance, number of bits, signal and clock skew, number of components, chip size, power dissipation etc. These problems limit the use of ADC architectures for various applications. Flash ADCs are very fastest converters and are well suitable for large bandwidth applications. But the main problem is that they consume lot of power as the resolution of the converter increases which in turn reflects in the increase in the size of the chip. Also as the chip size increases, more problems associated with signal and clock routing becomes noticeable.

Two step ADCs also well known as subranging converters is a cross between a flash ADC and pipeline ADC can be used to realize higher resolution and small power. Pipelined ADC architecture is a more specialized application of the two-step architecture and has been developed to be the most popular architecture for sampling rates from a few mega samples per second (MS/s) to 500 MS/s, with resolutions ranging from 8 bits to 12 bits.

Sigma-Delta ($\sum$-Δ) ADC architecture are used in low speed applications with resolution ranging from (12–24) bits. Integrating ADCs provide increased resolution and can offer good line frequency and noise rejection. Time interleaved ADCs uses several identical analog to digital converters to process regular sampled data series at a faster rate than the operating rate of each individual ADC. Time inter leaving technique will relax the power-speed tradeoffs of ADC and minimizes metastability error rate while increasing the input capacitance.

Presently Successive Approximation Register (SAR) ADCs are being used in many applications, due to the innovations in architectural design and process scaling techniques of the transistors, which in turn lead to the improvements in low power consumption and high speed operation. SAR analog to digital converters are highly power efficient. Also in recent years, time interleaving of SAR ADCs have led to operate in the giga hertz range. One of the reasons SAR ADCs are doing better is because they use simple logic circuitry (both analog and digital) that tend to scale well and benefit from the evolving newer technologies day by day.

Lai *et al.* [1] presented a SAR analog-to-digital converter implemented in TSMC 0.18-um CMOS process which can be used as a part of the biological signal acquisition system. It employs single-sided switching method that reduces DAC switching energy, thereby achieves low power consumption. Yan *et al.* [2] proposes a two channel interleaved 6-bit 2GS/s SAR ADC design, that employs different comparators using small sized capacitor for each stage, which eliminates digital control delay. Zhu *et al.* [3] presents a high-speed and low-power SAR ADC, that uses a common-mode based charge recovery switching method. Kull *et al.* [4] presents a single-channel SAR ADC which operates at high-speed by converting each sample with two alternate

comparators clocked asynchronously and a redundant capacitive DAC with constant common mode to improve the accuracy of the comparator. Kuo *et al.* [5] propose a new structure namely the charge redistribution DAC to reduce the area cost and power consumption and to enhance the bandwidth. Yang *et al.* [6] proposed an asynchronous ADC realized by time interleaving two ADCs based on the binary successive approximation (SA) algorithm using a series capacitive ladder circuit. Lee *et al.* [7] implemented an ultra-low power SAR ADC for biosignal acquisition systems which utilized a passive sample-and-hold circuit, and an op-amp free, capacitor-based DAC. Compared to the previous related works, a 6-bit low power and medium resolution successive approximation register ADC is designed and simulated in this work.

The outline of the work is as follows. Section 2 discusses the theoretical background of successive approximation register ADC architecture and various parameters associated with the proposed work. Section 3 describes the implementation of the proposed SAR ADC. The simulation results are presented in Sect. 4. Finally conclusions are provided in Sect. 5.

2 Successive Approximation Register ADC Architecture

An SAR analog to digital converter works on the principle of binary search algorithm. This algorithm requires exactly N steps for converting the analog input voltage to an N-bit digital output. Figure 1 shows the block diagram of 6-bit SAR analog to digital converter. It includes a SAR control logic block which is realized using D-flip flop with set and reset controls, a sample and hold circuit, 6-bit digital to analog converter and a comparator circuit [8]. Initially the most significant bit of 6-bit control logic block has been set to 100000. The output of the SAR logic block is connected to 6-bit DAC. This in turn produces equivalent analog output voltage. The output of the 6-bit DAC is compared with the output of the Sample and Hold (S/H) circuit. If the DAC output is higher than the sample and hold output, then the comparator produces a logic zero output, else the comparator produces logic high.

Based on the output of comparator circuit, the SAR control logic will remains the same or reset the control logic block [9]. Recently the design of SAR ADCs has been enhanced considerably in terms of speed, power, resolution, signal to noise ratio and dynamic performance. The important specifications considered in this design are resolution = 6 bits, power supply voltage = 1.8 V, input bandwidth = upto 1 GHz, sampling rate = 100 MHz, power dissipation less than 2 mW and fabricated in 130 nm CMOS technology.

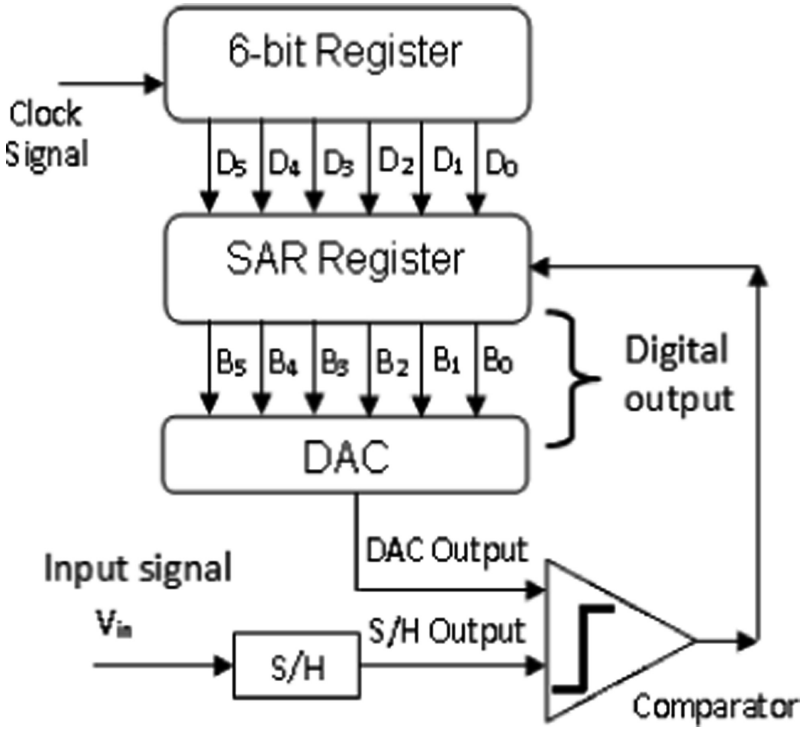

Fig. 1. Block diagram of 6-bit SAR analog to digital converter

3 System Implementation

This section discusses the design of the individual building blocks of the SAR ADC. The performance of these blocks will govern the performance of each stage and then finally the performance of the 6-bit converter. All these blocks are implemented on the HSPICE and Cadence schematic editor.

3.1 Sample and Hold Circuit

The S/H circuit is a key analog building block in many applications. The purpose of the sample and hold circuit is to sample an input analog signal and hold the analog input value over a certain interval of time for sub sequent processing. Here input signal is sampled based on the clock frequency. Figure 2 shows the schematic diagram of sample and hold circuit. It consists of a transmission gate circuit and a sampling capacitor. As long as the clock signal is high i.e. V_{DD} output voltage is same as the input voltage. When the clock signal becomes low, the input signal is sampled and the output voltage is same as the voltage across the sampling capacitor. The input to the sample and hold circuit is a sine wave having amplitude of 1.2 $V_{p\text{-}p}$, power supply is ± 1.8 V, and clock frequency is 100 MS/s. A voltage follower circuit is connected at the output side, in order to avoid the loading effect.

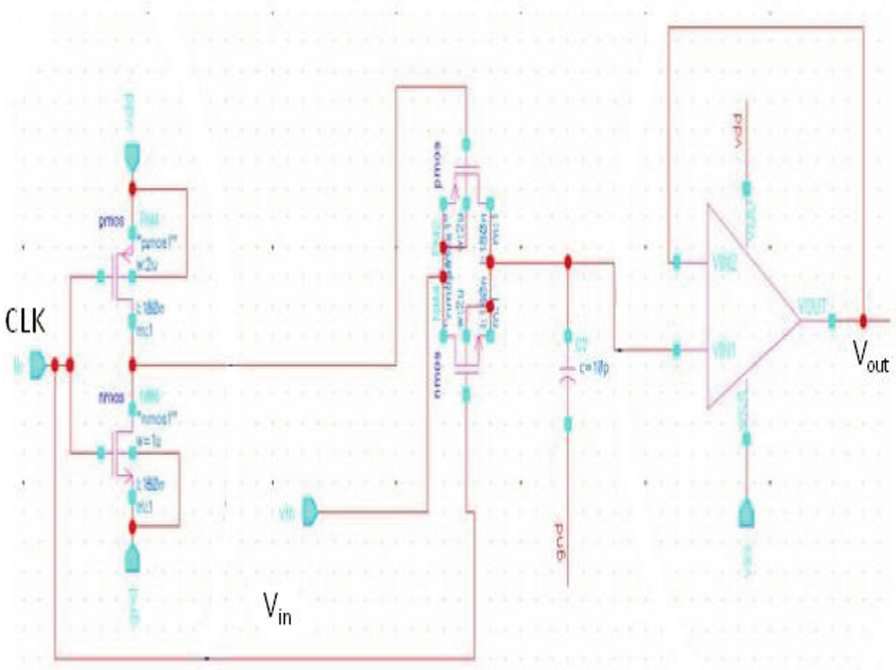

Fig. 2. Sample and hold circuit schematic diagram

3.2 Comparator Circuit

A CMOS Comparator circuit is used for comparing the input voltage with a known reference voltage. If the input voltage is greater than reference voltage the comparator output is one, else if the input voltage is less than reference voltage the comparator output is zero. Here transistors M_1 and M_2 act as a differential pair. The source of transistors M_1 and M_2 are connected with the current sink for biasing. The transistors M_3 and M_4 are PMOS based current mirror, used to realize the load. The transistor M_8 is connected in common source configuration which helps to improve the gain of the complete stage. The comparator schematic is shown in Fig. 3.

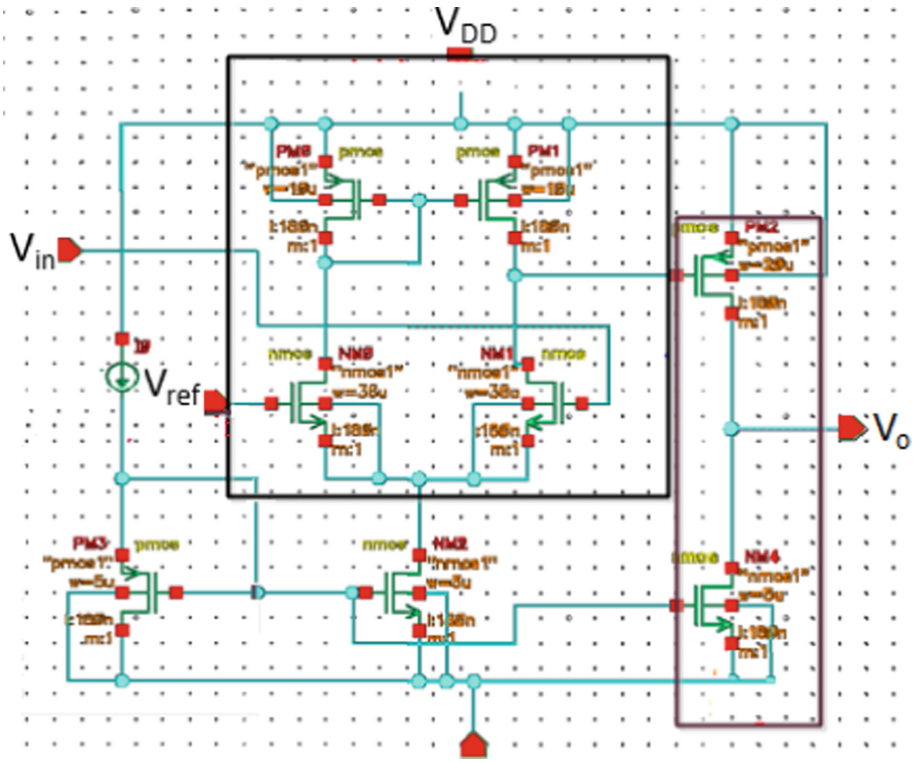

Fig. 3. Comparator schematic

3.3 6-Bit Digital to Analog Converter Circuit Using Transmission Gates

The Fig. 4 shows the 6-bit DAC circuit implemented using resistive ladder network and transmission gates. The resistive ladder network consists of 64 resistors. Based on the values of SAR registers, the distributed voltage is compared with the sample and hold circuit output by comparator.

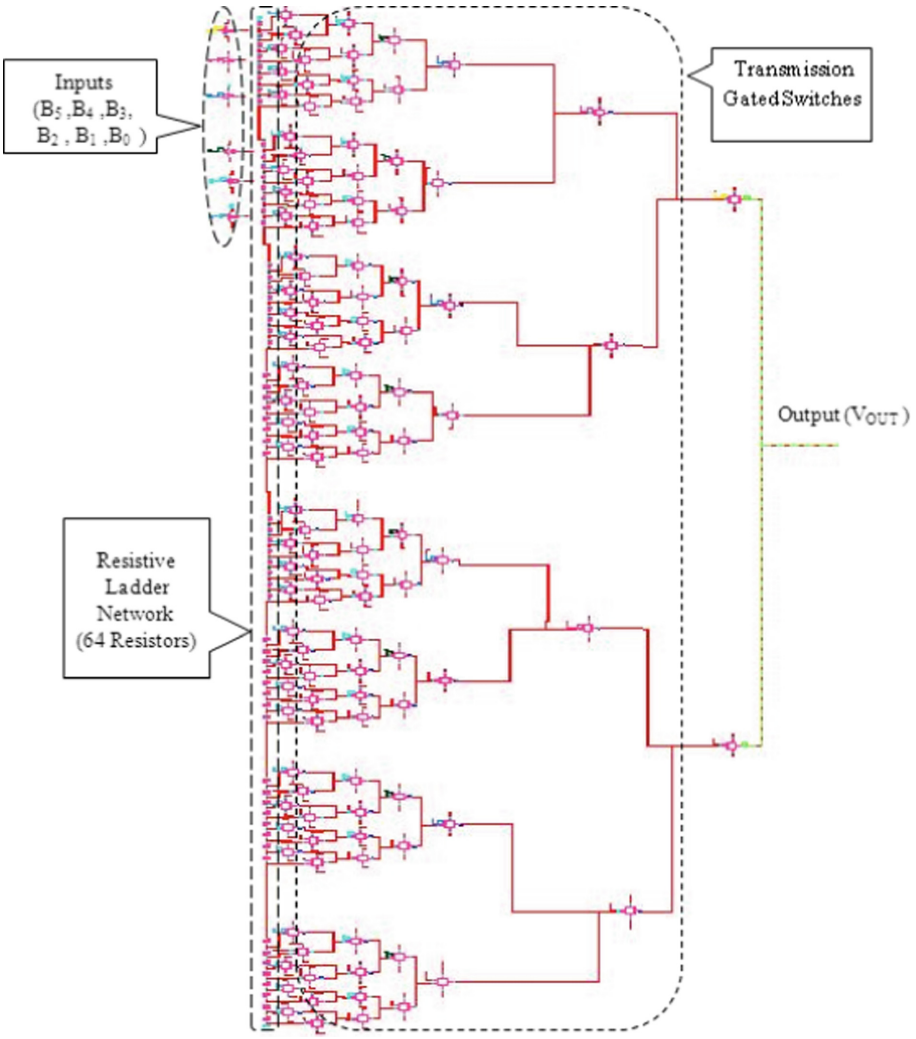

Fig. 4. Schematic of 6-bit DAC

4 Simulation Results

The performance of the proposed 6-bit SAR ADC was simulated using Cadence spectre. The entire SAR ADC is designed in 130 nm CMOS technology. The simulation results of sample and hold circuit is shown in Fig. 5. The input to the sample and hold circuit is a sine wave having amplitude of 1.0 Vp-p, power supply is ±1.8 V, and clock frequency is 800 MHz. The input signal is sampled based on the clock signal frequency.

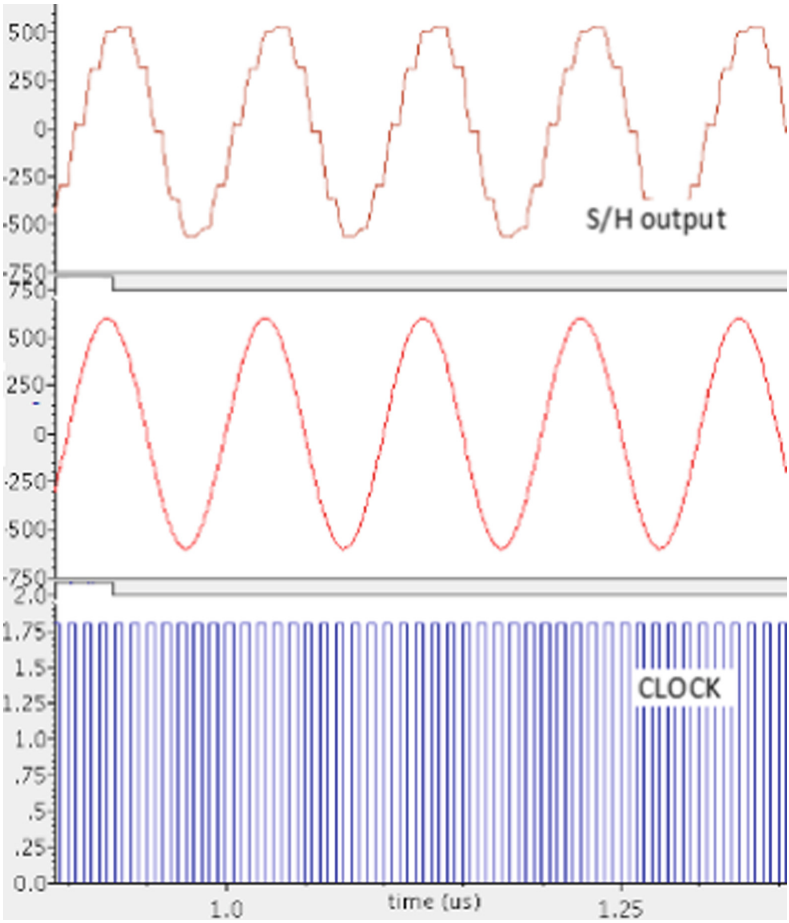

Fig. 5. Simulation results of sample and hold circuit

The final simulation results of 6-bit SAR ADC are shown in Fig. 6. The entire design of the SAR ADC is carried out using 130 nm CMOS technology.

The results obtained are summarized in Table 1.

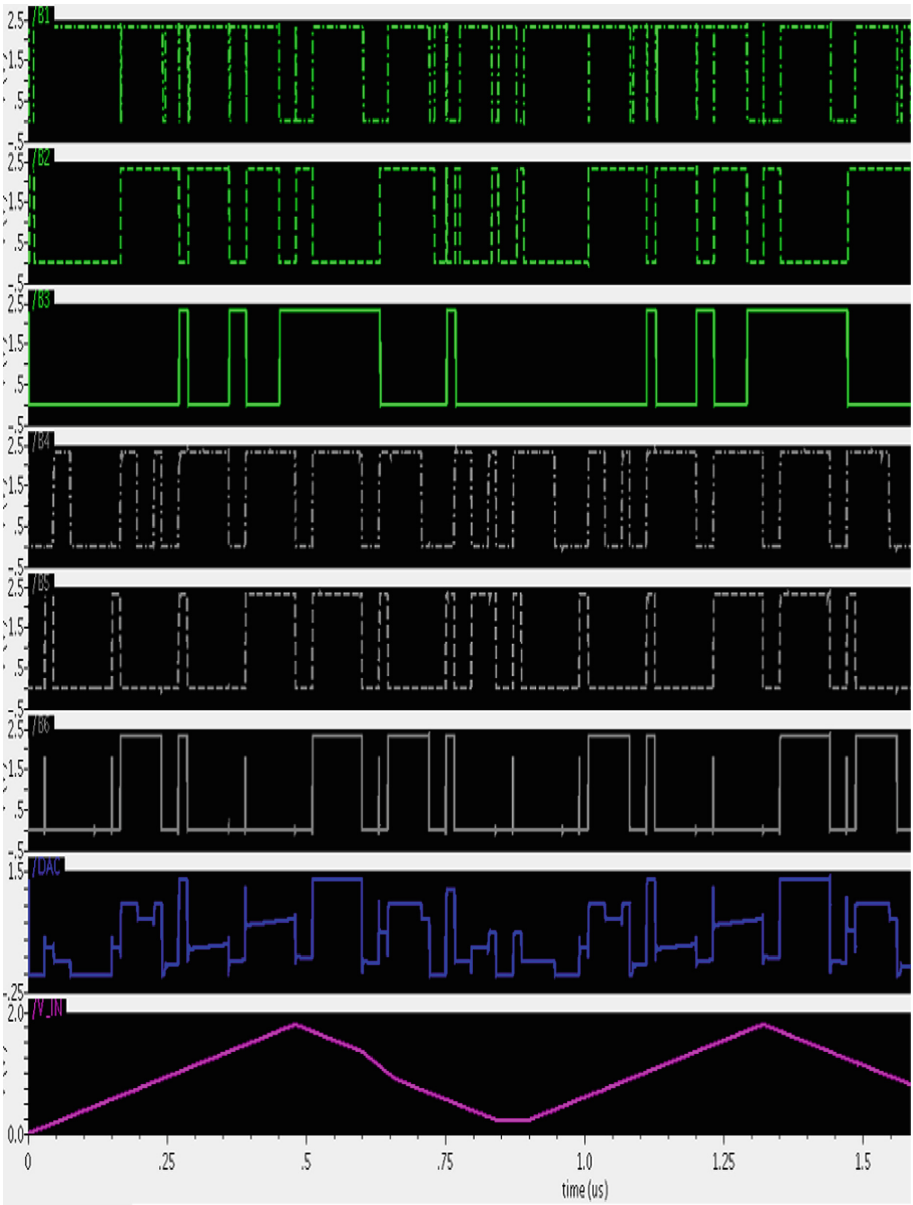

Fig. 6. Simulation results of 6-bit SAR ADC

Table 1. Summary of the 6-bit SAR ADC

Resolution	6 bits
Technology	CMOS 130 nm
Power supply	+1.8 V
Sampling rate	100 MHz
Input signal frequency	upto 1 GHz
Input voltage range	1.0 V_{P-P}
Power dissipation	36.7 μW
Area	0.14 mm^2
SNDR	64.2 dB

5 Conclusion

In this paper, a 6-bit 100 MHz successive approximation register ADC is designed and implemented in a 130 nm CMOS process technology. The ADC is operated at a power supply of 1.8 V and the simulated power consumption is only 36.7 μW. The sampling rate of the proposed ADC is 100 MHz. The ADC with an active die area of 0.14 mm^2 shows a maximum signal to noise distortion ratio (SNDR) of 64.2 dB. The designed SAR ADC can be used in applications requiring lower power dissipation, resolution requirement is medium and speed required is also not high which is MHz to KHz range such as in ultrasonic medical imaging and wireless transmission sensor networks.

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