



# Upgrade of the ATLAS Tile Calorimeter for the High Luminosity LHC

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on behalf of the ATLAS Tile Calorimeter System

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**Abstract.** The ATLAS hadronic Tile Calorimeter (TileCal) covers the central angular region of the detector. The TileCal will undergo a major replacement of its on- and off-detector electronics in 2024 for the high luminosity program of the LHC. The TileCal signals will be digitized and sent directly to the off-detector electronics, which will store them in fixed-latency buffers and digitally construct and transmit trigger sums for the Level-1 trigger at a rate of 40 MHz. The improved signal resolution and precision will allow more complex and effective algorithms to be implemented in the Level-1 trigger hardware. Three different front-end options are currently being investigated for the TileCal upgrade with extensive test beam studies to determine which option will be selected. The off-detector electronics are based on the Advanced Telecommunications Computing Architecture (ATCA) standard and are equipped with large, modern FPGAs and high-performance optical links. The on-detector electronics are designed to operate in a high radiation environment and has a high level of redundancy. The large scale, high performance FPGAs are also extensively used for the logic functions and data links in data acquisition for on-detector electronics. A hybrid Demonstrator prototype with the new calorimeter module electronics, but still compatible with the present system, is planned to be inserted in ATLAS in one of the next winter shutdowns.

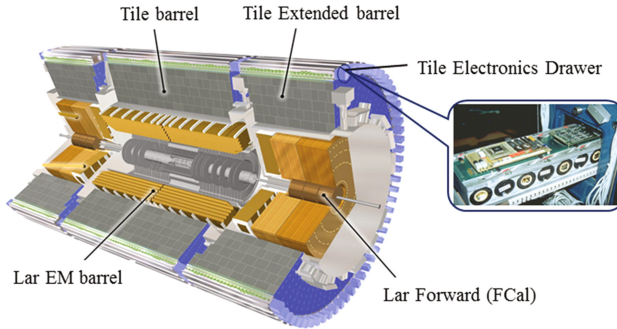
We present the components of the Tile Calorimeter upgrade for the high luminosity LHC, the production and performance of the readout electronics prototypes, the results of the beam tests at CERN and the plans for the next years.

**Keywords:** LHC · HL-LHC · Tile calorimeter · Analog front-end readout ATCA

## 1 Introduction

The High Luminosity Large Hadron Collider (HL-LHC, also known as Phase-2) is expected to start in 2026, with upgrade of the luminosity of up to  $5\text{--}7 \times 10^{34} \text{ cm}^{-2} \text{ s}^{-1}$  [1], allowing us to explore physics beyond the Standard Model, to study the electroweak symmetry breaking mechanism, and to measure the Higgs boson in detail. Here we describe the ATLAS TileCal upgrade program for the HL-LHC. The ATLAS TileCal is a cylindrical hadronic sampling detector with steel absorbers and scintillating plastic tiles, surrounding the EM calorimeter cryostat. It is divided into one long central

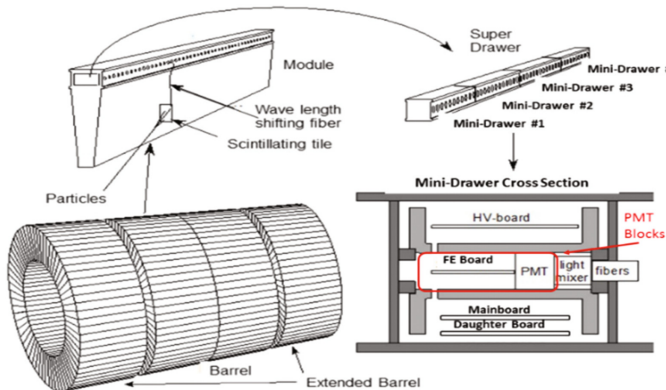
barrel (LB) of 5.56 m in length, covering a total pseudorapidity range  $|\eta| < 1.0$ , and two extended barrel (EB) cylinders of 2.91 m in length, covering in total a pseudorapidity range of  $0.8 < |\eta| < 1.7$ . Each cylinder is composed of 64 detector modules, each module covers the azimuthal  $\varphi$  in an angle of  $2\pi/64$ . The TileCal and its readout electronics contained in the Tile Electronics Drawers are depicted in Fig. 1.



**Fig. 1.** TileCal architecture with the readout system in the Tile Electronics Drawers Copyright 2017 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license

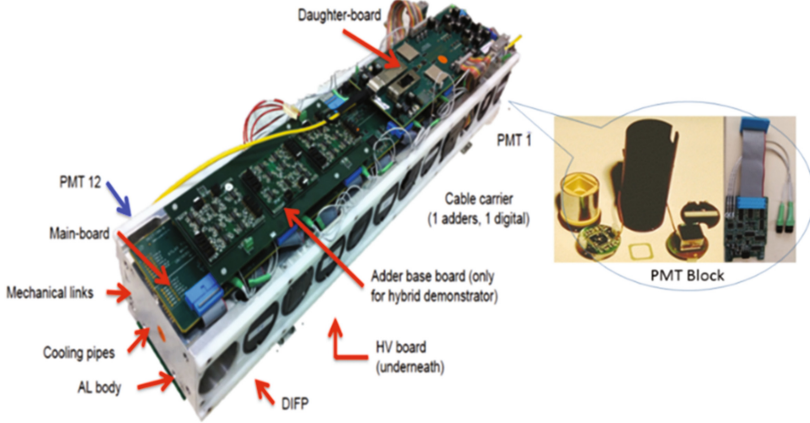
## 2 On-detector Electronics

The TileCal on-detector electronics read out a total of  $\sim 10,000$  photomultiplier tubes (PMT), housed in 256 Tile Electronics Drawers; the system structure is shown in Fig. 2. A Tile Electronics Drawer will consist of up to 4 identical Mini-drawers supporting up to 12 PMT blocks each, with front-end readout electronics and a Main Board (MB) to handle the data digitization and data concentration, and a Daughter Board (DB) to serve as a hub for the communication between on- and off-detector electronics.



**Fig. 2.** TileCal on-electronics system structure Copyright 2017 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license

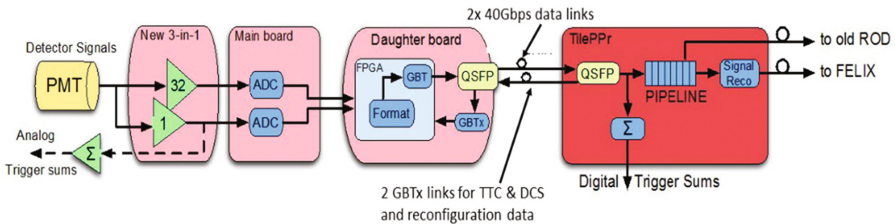
The assembly of a Mini-drawer with PMT blocks and electronics is shown in Fig. 3. Three different front-end electronics alternatives have been developed by three institutions in the TileCal collaboration. The “3-in-1” front-end electronics developed by The University of Chicago, USA, the QIE front-end electronics developed by Argonne National Laboratory, USA, and the FATALIC front-end electronics developed by Laboratoire de Physique Clermont-Ferrand, France. One of these will eventually be chosen for the upgrade production. The three alternatives are described in the following subsections.



**Fig. 3.** PMT blocks and readout electronics in a Mini-drawer Copyright 2017 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license

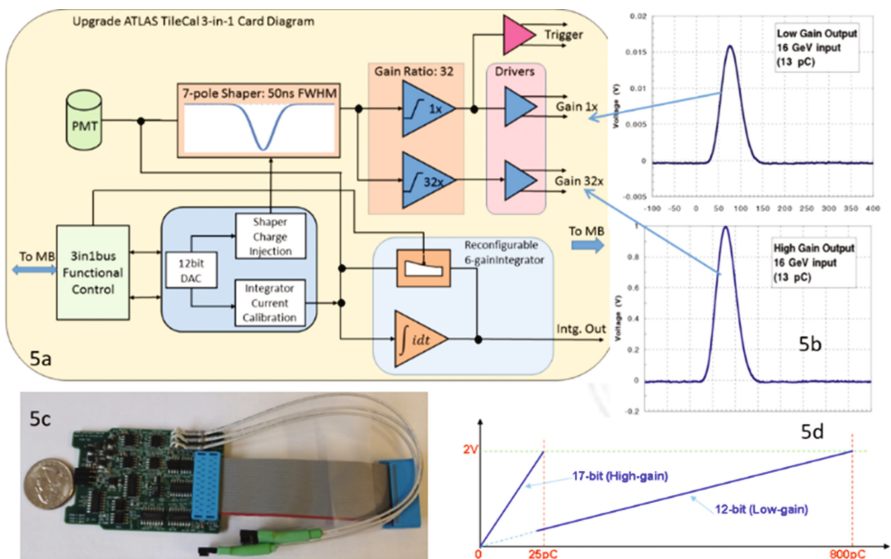
**2.1 The 3-in-1 Front-End Readout Electronics**

The upgrade of the 3-in-1 front-end electronics and associated MB is based on the present system used at the LHC [2]. It utilizes commercial off-the-shelf components. The active devices used in the design are selected from the advanced CMOS or BiCMOS technologies, most of them in 130 nm CMOS. A schematic for the hybrid Demonstrator prototype system aimed at the Phase 2 upgrade, equipped with the 3-in-1 front-end readout electronics is shown in Fig. 4.



**Fig. 4.** The TileCal readout structural diagram using the 3-in-1 front-end electronics Copyright 2017 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license

In order to be compatible with the current readout system at the LHC, an analog trigger sum is still retained on the new 3-in-1 card. This is necessary for the hybrid Demonstrator, which is aimed for the planned insertion of a few prototype modules in the present ATLAS detector system. A functional diagram of the 3-in-1 card is shown in Fig. 5a. It processes a PMT output signal in two paths: the fast signal processing path and the slow signal processing path. The fast signal processing path receives the PMT signals with a 7-pole passive LC shaper. The shaper output is sent to the high gain and low gain channel in parallel. The high gain and low gain amplifiers have a gain ratio of 32. Both low and high gain amplifiers send the analog signals to the MB for digitization. For compatibility with the current Level-1 trigger, an analog trigger sum is still included on the 3-in-1 card. In Phase 2, the level-1 trigger will transition to fully digital inputs. The latency of the readout electronics is required to meet the fully digital Phase 2 trigger requirements.



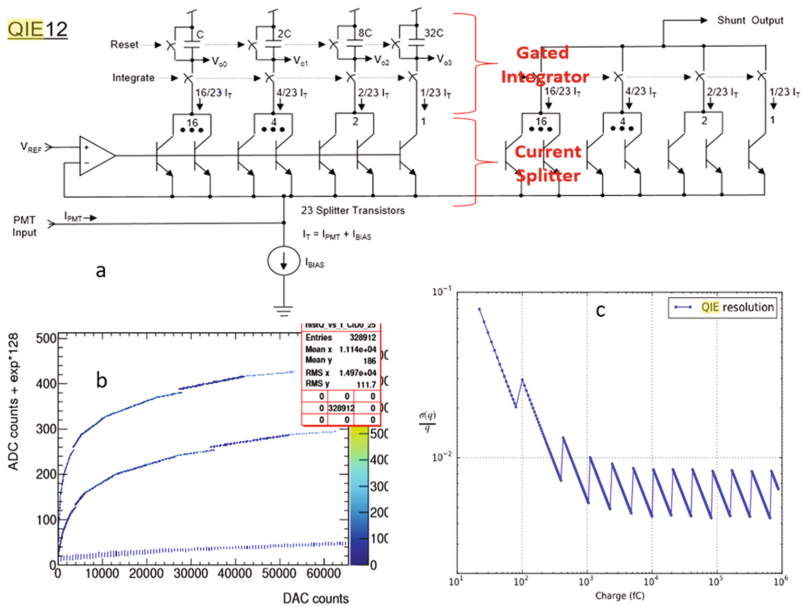
**Fig. 5.** (a) Diagram of the 3-in-1 card, (b) Waveforms of bi-gain channel outputs, (c) Photo of a 3-in-1 card, (d) Dynamic range of the bi-gain system Copyright 2017 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license

The 7-pole passive LC shaper gives an output bandwidth of 1 kHz–12.5 MHz, with effective bandwidth roll-off  $-140$  dB/Dec. The fast PMT output pulse in a rise time of 7–9 ns and a fall time of 17–20 ns is shaped to a waveform like a Gaussian function. The shaper output waveform has a rise time of 25 ns and a fall time of  $\sim 26$  ns and a pulse width of 50 ns FWHM as shown in Fig. 5b. The high-gain channel covers an input dynamic range of 0–25 pC to process the low energy particle signals, such as muons and electrons. The low gain channel covers an input dynamic range of 25–800 pC to process signals generated by large energy hadrons. With 12-bit 40 Mbps ADCs in digitization, the combined bi-gain system achieves input dynamic range of 17 bits as shown in Fig. 5d.

The TileCal detector cells and PMT gains are calibrated using a Cesium source hydraulically driven through a system of steel tubes traversing all cells of the entire TileCal detector. The slow signal processing path measures PMT responses during the Cesium calibration and monitors the minimum bias current during the proton-proton collisions. The slow signals are measured by a slow integrator with 6 programmable gains having variable time constant of 10–20 ms. A prototype 3-in-1 card is shown in Fig. 5c. The dynamic range of the slow integrator is 0–10  $\mu\text{A}$  with a resolution of 12 bits.

### 2.2 The QIE Front-End and Readout Electronics

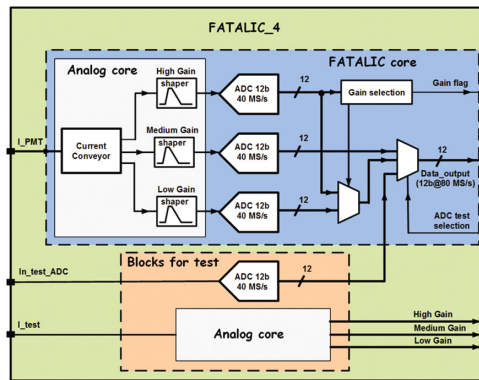
The QIE front-end readout card [4] was developed in a BiCMOS technology. A block diagram of the QIE12 ASIC is shown in Fig. 6a. In principle, it is a 4 range current splitter in ratios of 1/23, 2/23, 4/23 and 16/32. Each range has a gated current integrator. The outputs of 4 integrators are sequentially digitized by a flash ADC (FADC) in multiplexed 4 clock phases from a 40 MHz clock source. A final encoder will sort and encode the 4 FADC outputs to a final digital value for the total charge of a PMT pulse. A time to digital converter (TDC) of 5-bits is also implemented in QIE 12 and read out together with the digitized charge value. The readout data is streamed out word-by-word at a rate of 80 MHz. The data word format consists of 7-bit digitized charge, 2-bit range, 2-bit clock-phase control ID and 5-bit TDC data. The dynamic range of QIE 12 is comprised of 4 ranges having non-linear transfer function shown in Fig. 6b. It presents 18-bit linear dynamic range after calibration with a look-up-table. The resolution and digitization uncertainty varying range by range is shown in Fig. 6c.



**Fig. 6.** (a) Principle of QIE 12 ASIC, (b) QIE 12 transfer function, (c) QIE 12 resolution and digitization uncertainty Copyright 2017 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license

### 2.3 The FATALIC Front-End and Readout Electronics

The FATALIC front-end readout is being developed with IBM 130 nm CMOS Technology [5]. The front-end analog block is a current conveyor that gives 3-outputs with a gain ratio of 64:32:1. The conveyor output pulses are shaped with an RC single pole integrator to a lower bandwidth pulse to meet the Nyquist criterion in 40 MHz sampling ADCs. A functional diagram of FATALIC 4 chip that currently in test is shown in Fig. 7. The on-chip 3 channels of 12-bit ADC cores convert the analog signal to digital data. The auto-range selection allows only 2 channels of data to be read out together for every event, e.g. read out data either from both medium-gain and low-gain channels or from both medium-gain and high-gain channels. The auto-range readout will help reduce the readout data bandwidth. The FATALIC 4 outputs are readout in 12-bit at 80 MHz.



**Fig. 7.** A functional diagram of the FATALIC 4 ASIC Copyright 2017 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license

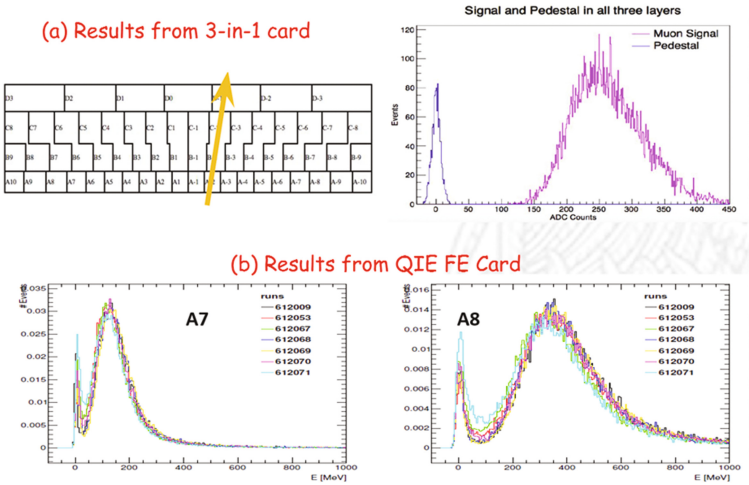
The FATALIC 4 front-end electronics can handle a combined dynamic range of 0–1.2 nC (18-bit). The output electric noise is 7.5 fC and has a non-linearity less than 2% for high and medium gain outputs. An on-chip dedicated electronics block is implemented for the purpose of the die testing. The FATALIC 4 chip operates in +1.6 V single power supply and consumes 205 mW. A new design of FATALIC 5 is planned to eliminate the need for data concentration by the FPGAs on the MB.

### 2.4 Front-End Electronics Performance and Test-Beam Results

In terms of electronics performance, the systems work well over a large dynamic range and with very low electric noise. All 3 front-end electronics candidates meet the TileCal design requirements in the lab tests. Both prototypes of the 3-in-1 and QIE systems gave very good results in test-beam experiments. The smallest interested low energy muon signals are clearly separated from the background noise in the beam testing for 3-in-1 shown in Fig. 8a and QIE readout systems shown in Fig. 8b.



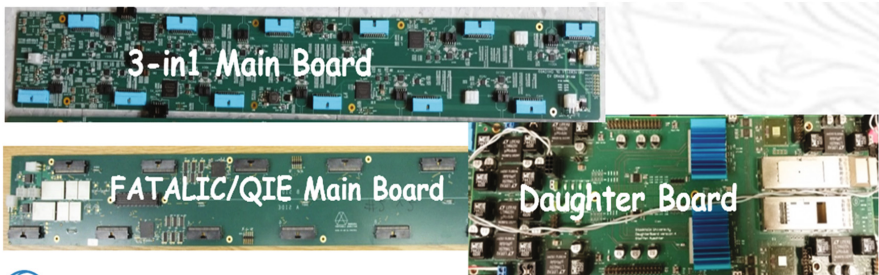
However, the test beam testing of FATALIC system is scheduled on the second half of 2017, the results can be reported in the near future.



**Fig. 8.** (a) 3-in-1 test-beam result, (b) QIE test-beam results Copyright 2017 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license

### 2.5 The Main Board and Daughter Board

As shown in Fig. 9, two different Main Board designs with different functionalities have been built to accommodate the different front-end options, one for the 3-in-1 front-end electronics and a second which is compatible with both the FATALIC and QIE front-end readout electronics [6].



**Fig. 9.** Two types of Main Boards and the Daughter Board Copyright 2017 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license

The MB for the 3-in-1 front-end electronics has 24 channels of 12-bit 40 Mbps digitizers (LTC2264-12) supporting 12 PMTs in bi-gain channel readout. In order to avoid single point failures in a single centralized system, the MB divides the 12 PMTs to be read out in 4 groups; each group employs a low cost Altera Cyclone IV FPGA

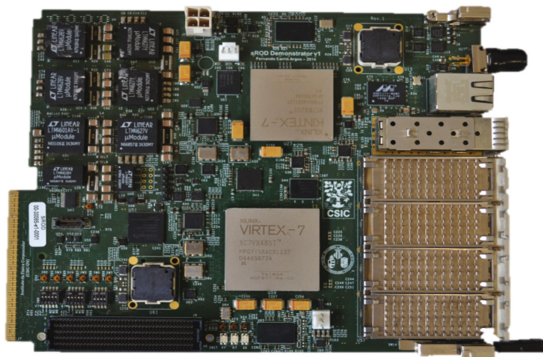
that serves three 3-in-1 cards for configuration controls via a dedicated SPI bus. Each ADC provides 1-bit serial output at a rate of 560 Mbps sending directly to the DB without routing through the FPGAs.

The FATLIC and QIE systems use same MB. FATALIC system uses two FPGAs to convert the 80 MHz, 12-bit ADC parallel data from each PMT to 2-bit serial data stream at a rate of 560 Mbps, which are then transmitted to the DB. By the contrast, the QIE electronics send the parallel data at a rate of 80 MHz directly to the DB. The DB is electronically compatible with all three readout interfaces, but requires different FPGA firmware for each front-end solution.

The DB is a data hub responsible for the multi gigabit data communication between the on-detector and off-detector electronics. It receives detector control system (DCS) commands via 4.8 Gbps optical links in GBTX protocol from the off-detector TileProcessor (Tile PPr) module, which in turn collects data from the front-end electronics via the MB and send read out data and DCS monitoring data to the Tile PPrs. Both down-stream and up-stream optical links use redundancy to eliminate single point failures in the system, a failed link can be overcome by switching links at a patch panel in the counting room. This design will not require the duplication of Tile PPr modules.

### 3 Back-end Electronics

The TileCal back-end electronics, Tile PPr will be housed in ATCA chassis, although they will not fully complying with ATCA backplane specifications [7]. A prototype Tile PPr module is shown Fig. 10. It sends trigger, clocks and slow control commands to the DB for the on-detector electronics using the GBTX protocol (4.8 Gbps) and receives the readout data from 4 identical Mini-drawers. The prototype Tile PPr has been designed to allow the testing of all the Phase 2 readout and trigger functionalities and provide backward capability with the current Readout-out Driver (ROD) system for data evaluations. In the Phase 2 runs, the Tile PPr receives data from the on-detector electronics at 40 MHz and transmits the data to a FELIX module for further data acquisition and trigger electronics. The Tile PPr is capable of preprocessing data based on the ATLAS physics requirements.



**Fig. 10.** Tile PPr Board Copyright 2017 CERN for the benefit of the ATLAS Collaboration. CC-BY-4.0 license



## 4 Conclusion

The Tile Calorimeter Phase 2 Upgrade design has been successfully tested in the lab and test-beam runs in 2016 with the Demonstrator prototype. All 3 candidates for the front-end analog readout electronics are expected to meet the requirements for implementation in ATLAS. Compared to the current system, the new system is improved in terms of reliability, mechanical assembly, and system installation. In a future winter shutdown, a hybrid Demonstrator prototype with the upgraded calorimeter module and the new calorimeter electronics compatible with the present system, is planned to be inserted in the ATLAS detector for data taking. This will permit all functionality and performance to be fully evaluated.

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