John H. Lau

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Preface

The first fan-out wafer-level packaging (FOWLP) U.S. patent was filed by Infineon on October 31, 2001, and the first technical papers were also published (2006) by Infineon and their industry partners: Nagase, Nitto Denko, and Yamada. At that time, they called it embedded wafer-level ball (eWLB) grid array. Since 2009 Infineon and since 2011 Intel and STATS ChipPAC have been in volume production of packaging semiconductor devices with the FOWLP technology. Unfortunately, because of the small sizes and low performance of the packaged devices, the FOWLP did not get too much tractions. Until September 2016, after TSMC used their InFO (integrated fan-out) technology to package the Apple application processor (A10), then the whole semiconductor packaging community is excited about the FOWLP technology. This is because the chip size of A10 is $> 125\ mm^2$ and A10 is a very high-performance SoC (system-on-chip).

The advantages of FOWLP over the popular PBGA (plastic ball grid array) packages with solder-bumped flip chip are (1) lower cost, (2) lower profile, (3) eliminating the substrate, (4) eliminating the wafer bumping, (5) eliminating the flip chip reflow, (6) eliminating the flux cleaning, (7) eliminating the underfill, (8) better electrical performance, (9) better thermal performance, and (10) easier to go for system-in-package (SiP) and 3D IC packaging. The advantages of FOWLP over the popular WLCSP (wafer-level chip scale package) are (1) the use of known good die (KGD), (2) better wafer-level yield, (3) using the best of silicon, (4) multi-chip, (5) embedded integrated passive devices, (6) more than one RDL, (7) higher pin counts, (8) better thermal performance, (9) easier to go for SiP and 3D IC packaging, and (10) higher PCB-level reliability.

Unfortunately, for most of the practicing engineers and managers, as well as scientists and researchers, temporary bonding and debonding of carriers, reconstituted wafer or panel, pick and place, EMC (epoxy molding compound), compression molding, PMC (post mold cure), copper revealing, organic RDLs (redistribution layers), inorganic RDLs, hybrid RDLs, warpage, chip-first and die face-up, chip-first and die face-down, and chip-last or RDL-first are not well understood. Thus, there is an urgent need, both in industry and research institute, to create a comprehensive book on the current state of knowledge of these key

enabling technologies. This book is written so that readers can quickly learn the basics of problem-solving methods and understand the trade-offs inherent in making system-level decisions.

There are 11 chapters in this book, namely (1) Patent Issues of Fan-out Wafer-Level Packaging, (2) Flip Chip Technology versus FOWLP, (3) Fan-In Wafer-Level Packaging versus FOWLP, (4) Embedded Chip Packaging, (5) FOWLP: Chip-First and Die Face-Down, (6) FOWLP: Chip-First and Die Face-Up, (7) FOWLP: Chip-Last or RDL-First, (8) FOWLP: PoP (package-on-package), (9) Fan-Out Panel-Level Packaging (FOPLP), (10) 3D Integration, and (11) 3D IC Heterogeneous Integration by FOWLP.

Chapter 1 briefly discusses the patent issues of FOWLP and FOPLP. The patents impacting the semiconductor packaging will also be mentioned.

Chapter 2 presents the wafer-level flip chip technology. Emphasis is placed on wafer bumping, various substrate technologies, flip chip assembly, underfill, and reliability. Cu–Cu direct hybrid bonding is also briefly mentioned. Finally, the flip chip technology versus FOWLP is presented.

Chapter 3 details the fan-in wafer-level packaging. Emphasis is placed on WLCSP, PCB assembly of WLCSP, and solder joint reliability of WLCSP. TSMC's UFI (UBM-free integration) WLCSP will also be briefly mentioned. Finally, WLCSP versus FOWLP will be presented.

Chapter 4 presents the embedded chip packaging. Emphasis is placed on chips embedded in laminated/polyimide substrate, Si wafer, and glass panel.

Chapter 5 discusses the chip-first and die face-down FOWLP. Emphasis is placed on the demonstration of the feasibility of a SiP (system-in-package), which consists of four chips and four capacitors. The test chips, test package, temporary carrier, thermal release tape, EMC, compression molding, RDLs, solder ball mounting, and dicing will be presented.

Chapter 6 provides the chip-first and die face-up FOWLP. Emphasis is placed on the demonstration of the feasibility of a large package with three RDLs for a very larger chip. The test chip, test package, temporary glass carrier, Cu revealing, RDLs, debonding, and dicing will be discussed. The packages are then assembled on PCB and then go through thermal-cycling test and drop test.

Chapter 7 presents the chip-last (or RDL-first) FOWLP. Emphasis is placed on the reasons for chip-last FOWLP. Various methods in making the organic RDLs, inorganic RDLs, and hybrid RDLs will be examined.

Chapter 8 discusses the PoP with FOWLP. Emphasis is placed on the application of the FOWLP method to house the application processors for smartphones in the bottom package. STATS ChipPac's and TSMC's PoP with FOWLP technology will be presented.

Chapter 9 provides the fan-out panel-level packaging (FOPLP). Emphasis is placed on various methods in using PCB technology and LDI (laser direct imaging) to make the fan-out packages. The panel versus wafer and the issues of FOPLP will be discussed.

Chapter 10 presents the most recent developments in 3D integrations. Emphasis is placed on 3D IC packaging, 3D IC integration, and 3D silicon integration. Who should be making the TSV (through silicon via) will also be discussed.

Chapter 11 discusses the heterogeneous integration by FOWLP. Emphasis is placed on heterogeneous integration on organic substrates, silicon substrates, and RDL substrates. The 3D IC heterogeneous integration by FOWLP is also provided.

For whom is this book intended? Undoubtedly, it will be of great interest to three groups of specialists: (1) those who are active or intend to become active in research and development of the key enabling technologies of FOWLP and FOPLP such as temporary bonding and debonding of carriers, reconstituted wafer or panel, EMC, compression molding, PMC, copper revealing, RDLs fabricated by polymer and copper plating/etching, PECVD (plasma enhanced chemical vapor deposition) and copper damascene and CMP (chemical mechanical polishing), and PCB and LDI, warpage, chip-first and die face-up, chip-first and die face-down, and chip-last or RDL-first; (2) those who have encountered practical FOWLP and FOPLP problems and wish to understand and learn more methods for solving such problems; and (3) those who have to choose a reliable, creative, high performance, high density, low power consumption, and cost-effective FOWLP and FOPLP technique for their products. This book can also be used as a text for college and graduate students who have the potential to become our future leaders, scientists, and engineers in the electronics and optoelectronics industry.

I hope that this book will serve as a valuable reference source for all those faced with the challenging problems created by the ever-increasing interest in FOWLP and FOPLP. I also hope that it will aid in stimulating further research and development on key enabling technologies and more sound applications to FOWLP and FOPLP products. The organizations that learn how to design and manufacture temporary bonding and debonding carrier, molding, and RDLs in their semiconductor packaging systems have the potential to make major advances in the electronics and optoelectronics industry, and to gain great benefits in performance, functionality, density, power, bandwidth, quality, size, and weight. It is my hope that the information presented in this book may assist in removing roadblocks, avoiding unnecessary false starts, and accelerating design, materials, process, and manufacturing development of key enabling technologies of FOWLP and FOPLP.

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John H. Lau, Ph.D., P.E. has been a Senior Technical Advisor at ASM Pacific Technology in Hong Kong since July 2014. Prior to that, he was a fellow of the Industrial Technology Research Institute in Taiwan for 4½ years; a Visiting Professor at Hong Kong University of Science and Technology for 1 year; the Director of the Microsystems, Modules, and Components Laboratory at the Institute of Microelectronics in Singapore for 2 years; and a Senior Scientist/MTS at Hewlett-Packard Laboratory/Agilent in California for more than 25 years.

His professional competences are design, analysis, materials, process, manufacturing, qualification, reliability, testing, and thermal management of electronic, optoelectronic, LED, CIS, and MEMS components and systems, with emphases on solder mechanics and manufacturing, RoHS-compliant products, SMT, flip chip, fan-in and fan-out WLP, SiP, heterogeneous integration, and TSV and other enabling technologies for 3D IC integration.

With more than 39 years of R&D and manufacturing experience, he has authored or coauthored more than 460 peer-reviewed technical publications, invented more than 30 issued or pending US patents, and given more than 290 lectures/workshops/keynotes worldwide. He has authored or coauthored 20 textbooks on 3D IC integration and packaging, TSV for 3D integration, advanced MEMS packaging, reliability of 2D and 3D IC interconnects, flip chip, WLP, MCM, area-array packages, WLCSP, high-density PCB, SMT, DCA, TAB, lead-free materials, soldering, manufacturing, and solder joint reliability.

He earned a Ph.D. degree in theoretical and applied mechanics from the University of Illinois at Urbana–Champaign, an M.A.Sc. degree in structural engineering from the University of British Columbia, a second M.S. degree in engineering mechanics from the University of Wisconsin at Madison, and a third M.S. degree in management science from Fairleigh Dickinson University. He also has a B.E. degree in civil engineering from National Taiwan University.

He has received many awards from the American Society of Mechanical Engineers (ASME), the Institute of Electrical and Electronics Engineers (IEEE), the Society of Manufacturing Engineers (SME) and other societies, including for the best IEEE/ECTC proceedings paper (1989), outstanding IEEE/EPTC paper (2009),

best ASME transactions paper (*Journal of Electronic Packaging*, 2000), and best IEEE transactions paper (*CPMT*, 2010), and the ASME/EEP Outstanding Technical Achievement Award (1998), IEEE/CPMT Manufacturing Award (1994), IEEE/CPMT Outstanding Contribution Award (2000), IEEE/CPMT Outstanding Sustained Technical Contribution Award (2010), SME Total Excellence in Electronics Manufacturing Award (2001), Pan Wen Yuan Distinguished Research Award (2011), IEEE Meritorious Achievement in Continuing Education Award (2000), IEEE Components, Packaging, and Manufacturing Technology Field Award (2013), and ASME Worcester Reed Warner Medal (2015). He is an elected ASME fellow, IEEE fellow, and IMAPS fellow, and has been heavily involved in many of ASME's, IEEE's, and IMAPS' technical activities.

Chapter 1
Patent Issues of Fan-Out Wafer-Level Packaging

1.1 Introduction

In the industry, research institute, and university, there are many engineers, researchers, students, and professors working on fan-out wafer-level packaging. In order to avoid the granted patents in this area, they are trying various methods such as die-up, die-down, die-first, die-last, RDL (redistribution layer)-first, RDL-last, mold-first, mold-last, round temporary carrier, and rectangular temporary carrier. In this chapter, the patent issues of fan-out wafer/panel-level packaging will be investigated. Emphasis will be placed on the claims of the granted patents and the range of things which might be covered under the patents. Depending on the RDL line width/spacing, the material, process, equipment, and application of fan-out wafer/panel-level packaging are examined and some recommendations are made. The patents which impacting the semiconductor packaging the most, so far, will be briefly mentioned first.

1.2 Functions of Semiconductor Packaging

Figure 1.1 shows the inside of a typical electronic product. It consists of printed circuit boards (PCBs) with some semiconductor integrated circuit (IC) chip components. IC chip is not an isolated island. It must communicate with other IC chips in a circuit through an input/output (I/O) system of interconnects. Furthermore, the IC chip and its embedded circuitry are delicate, requiring the package to both carry and protect it. Consequently, the major functions of the semiconductor packaging are, for example [1]: (1) to provide a path for the electrical current that powers the circuits on the IC chip; (2) to distribute the signals onto and off the IC chip; (3) to remove the heat generated by the circuits on the IC chip; and (4) to support and protect the IC chip from hostile environments.

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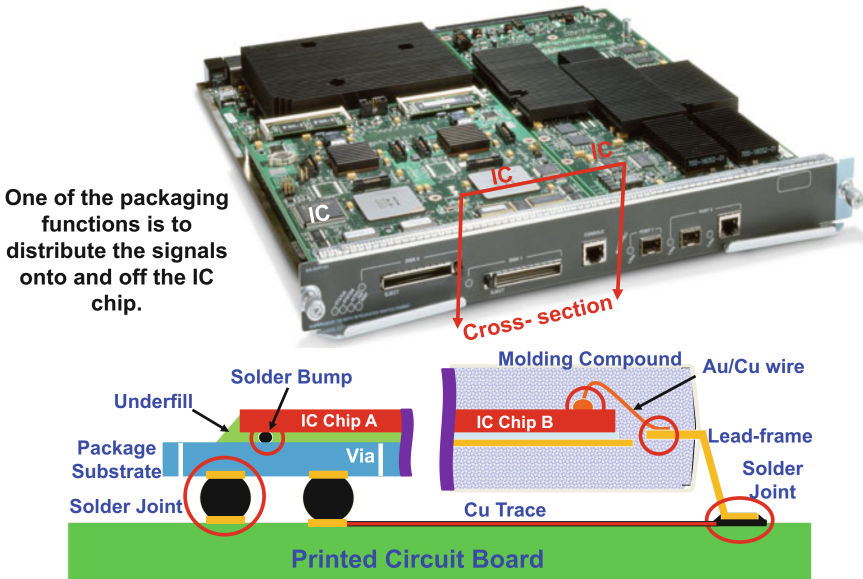


Fig. 1.1 Inside an electronic product and schematic of the cross section of a typical PCB

1.3 Level of Semiconductor Packaging

Semiconductor packaging is an art (engineering) based on the science of establishing interconnections ranging from [1] zero-level packages (i.e., chip-level connections, wire bonding, solder bump flip chip, and tape automated bonding), first-level packages (e.g., leadframe, substrate, molding, and single/multichip module), and second-level packages, i.e., board-level interconnect or PCB. Figure 1.1 schematically shows the cross section of a simple semiconductor packaging. It can be seen that Chip A is solder bumped flip chip on an organic substrate with solder balls. The circuitry of Chip A is fanned out through the substrate with vias, solder joints, and then to the PCB. By going through the Cu trace on the PCB, the circuitry is moving up the solder joint, leadframe, wire bond, and reaching to Chip B. This is how an electronic product works.

1.4 Patents Impacting the Semiconductor Packaging

There are many significant patents such as the solder bumped flip chip and through-silicon vias that impact semiconductor packaging. However, based on the author's opinion, the leadframe, organic substrate with area-array solder balls,

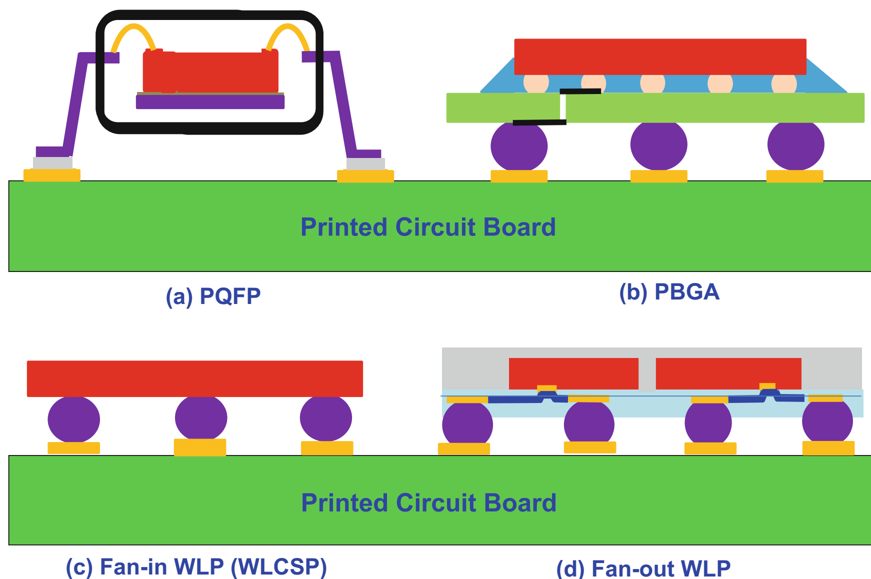


Fig. 1.2 Schematically showing the patents impacting the semiconductor packaging. **a** Leadframe. **b** Substrate and area-array solder balls. **c** Fan-in WLP. **d** Fan-out WLP

fan-in wafer-level packaging, and fan-out wafer-level packaging (schematically shown Fig. 1.2) are the most important so far [2].

1.4.1 Leadframe

On July 17, 1967, Kauffman of The Jade Corporation [3] proposed the use of a leadframe (see items #**14**, **16** in Fig. 1.3) having terminal ends (item #**18**) to fan-out the circuitry from a chip (item #**20**) as shown in Fig. 1.3, to a PCB. Today, just about all electronic products use leadframes such as the gull-wing lead (e.g., plastic quad flat pack (PQFP)), J-lead (e.g., plastic leaded chip carrier (PLCC)), and/or dual inline package (DIP) to fan-out the circuitry from a chip to a PCB (Fig. 1.4). The pitch of gull-wing leadframe for PQFP is usually 0.4 or 0.5 mm, J-lead leadframe for PLCC is 1.27 mm, and through-hole leadframe for DIP is 2.54 mm. In the past almost 50 years, the leadframe patent has had the most impact on semiconductor packaging.

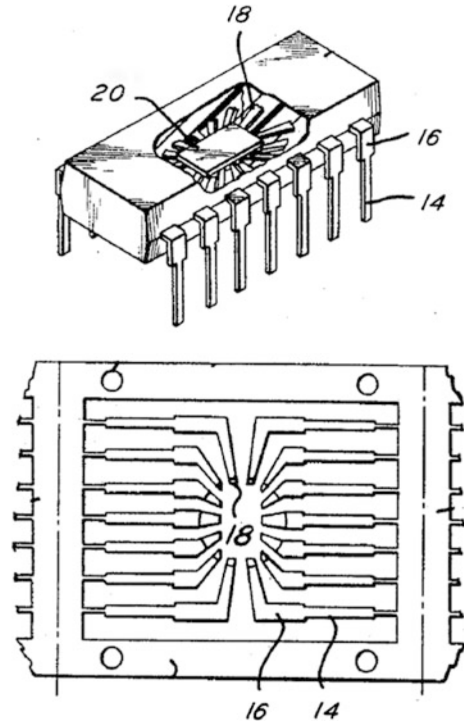


Fig. 1.3 Leadframe patent proposed by Jade Corporation

1.4.2 Organic Substrate with Solder Balls

On March 2, 1992, Paul Lin, Mike McShane, and Howard Wilson of Motorola proposed [4] the use of an organic carrier or substrate (item #**12** in Fig. 1.5) with area-array solder balls (item #**26**) (instead of leadframes) to fan-out the circuitry (items #**22**, **30**, **33**) from a chip (item #**18**) (Fig. 1.5) to a PCB, which is called a plastic ball grid array (PBGA) package. Also referring to Fig. 1.5, item #**22** is a wire bond and item #**32** is a via in the substrate connecting the upper wiring layer (item #**30**) to the bottom wiring layer (item #**33**). It should be pointed out that in 1989, Motorola and Citizen Watch announced the over molded pad array carrier (OMPAC) package [1, 5], which is the first PBGA.

Amkor (1993) led the OSATs (outsourced semiconductor assembly and test providers) to license this packaging technology from Motorola—and the BGA era began. Since then, hundreds of patents such as solder bumped flip chip on organic substrate as shown in Fig. 1.6 have been granted in the related area. However, they are incremental patents and Motorola's [4] is the fundamental patent.

The advantages of PBGA packages with organic substrate and area-array solder balls over the gull-wing leadframe PQFP and J-lead PLCC packages are (1) less package area for the same package pin count and thus less PCB real estate, (2) higher pin counts, (3) lower profile, (4) better in handling (no-bend leads),

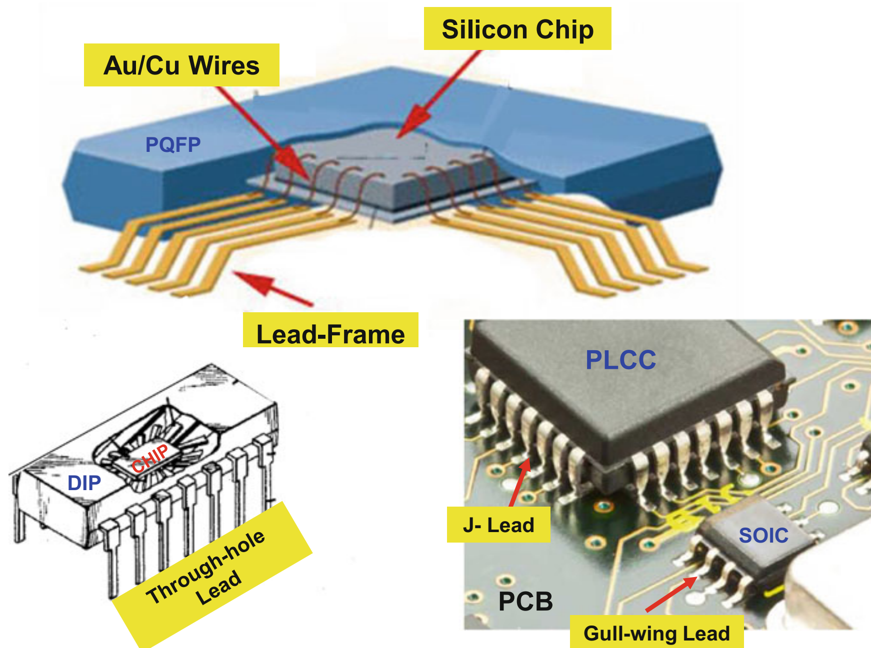


Fig. 1.4 Through-hole lead (DIP), gull-wing lead (PQFP), and J-lead (PLCC)

(5) better coplanarity, (6) better assembly yield because the forgiving of self-aligning characteristic of the surface tension of molten solder ball during reflow, (7) better in rework, (8) smaller inductance because of the short runs between the chip and the solder balls on the bottom of the substrate, (9) smaller reflections and noise levels, respectively, by matching the trace length with the output impedance, and (10) better heat dissipation with copper power and ground planes.

Today, PBGA packages have been used for housing just about any (low-end to high-end) semiconductor ICs (from 4 to 625 mm^2) with area-array solder balls ranging from 10 to 1000 s and their pitch ranges from 1.27, 1, 0.8, 0.65, 0.5, to 0.4 mm. The sizes of the PBGA packages range from 10 mm × 10 mm, to as large as 55 mm × 55 mm. The organic substrate with solder ball patent ranks second in terms of impact on semiconductor packaging, so far.

1.4.3 Fan-In Wafer-Level Packaging

On July 13, 1998, Peter Elenius and Harry Hollack of flip chip technologies proposed [6] the use of redistribution layer (RDL) (item #**30** in Fig. 1.7) to fan-in the circuitry from the original peripheral bond pads (items #**18**, **20**) of a chip (item #**10**)

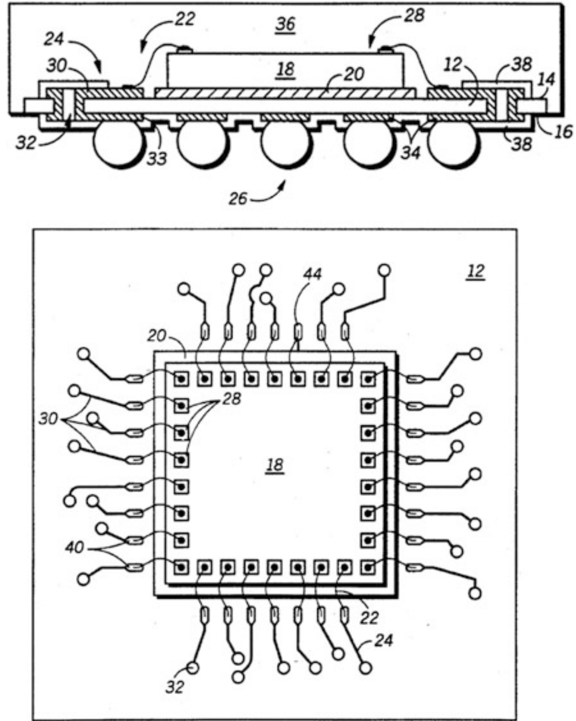


Fig. 1.5 Organic substrate with area-array solder balls patent proposed by Motorola

on a wafer (item #**14**) and of solder balls (item #**28**) (Fig. 1.7) to connect to a PCB without underfill. The RDL (item #**30**) is connecting the electrical contact (item #**32**) on the peripheral bond pad (items #**18**, **20**) to the solder bump pad (item #**26**). Large solder balls (item #**28**) can be fabricated within the chip (item #**10**) on the wafer (item #**14**). Leadframe, substrate, and underfill are eliminated as shown in Fig. 1.8.

It should be pointed out that the concept of fan-in wafer-level packaging (WLP) was first proposed by flip chip technologies [6, 7, and 8]. However, the knowledge in this area has been mentioned/demonstrated by many others such as Mitsubishi [9, 10], Marcoux [11], Sandia [12], ShellCase [13], Fraunhofer IZM [14, 15], DiStefano [16], and EPIC [17]. The packages made by the fan-in WLP are called wafer-level chip scale package (WLCSP) and one of the most famous is UltraCSP [18] developed and patented by flip chip technologies [6]. In 2001, again Amkor led the OSATs and foundries to license the UltraCSP, and the WLP era began.

In the past 16 years, WLCSP has been used mainly for low pin counts (≤ 200) with redistributed pad pitch ranges from 0.5, 0.4, 0.35, and 0.3 mm, small die size (≤ 6 mm $\times$ 6 mm), low-cost, low-end, low-profile, and high-volume applications. Semiconductor ICs such as the electrostatic discharge/electromagnetic interference protection, radio frequency (RF) filtering, power management, power amplifiers,

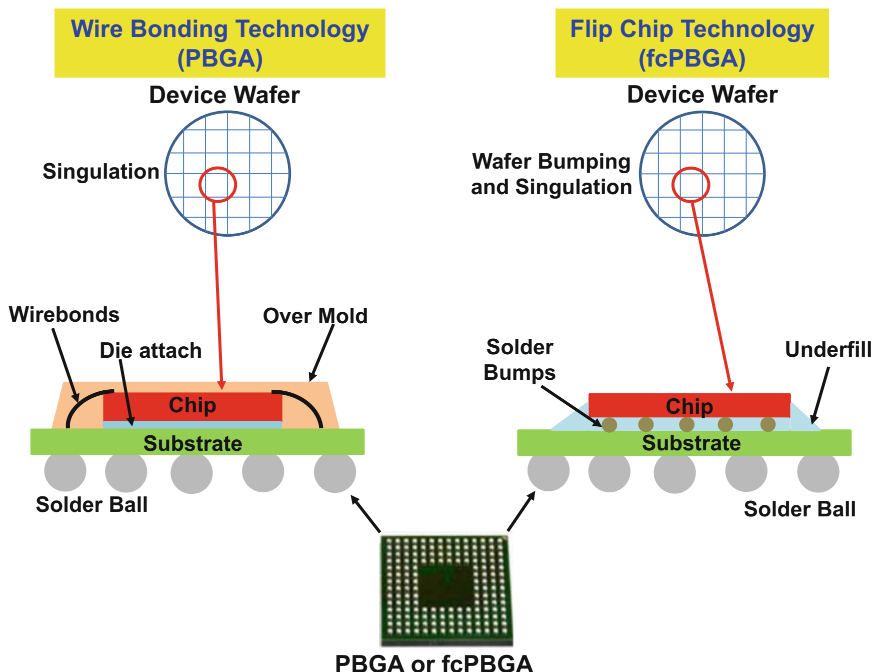


Fig. 1.6 PBGA and fcPBGA

surface acoustic wave/bulk acoustic wave filters, DC/DC converters, light-emitting diodes, battery and display driver, audio/video codes and amplifiers, logic gates, electrically erasable programmable read-only memory (EEPROM), microcontrollers, Bluetooth + frequency modulation (FM) + Wi-Fi combos, global positioning system (GPS), baseband, and radio frequency transceivers have been packaged with various WLCSPs for various electronic products such as cellphones, smartphones and tablets, and wearables. For internet of things (IoTs) [19], the CMOS image sensors and MEMS sensors will also be packaged with WLCSPs.

The advantages of WLCSPs over PBGA packages are (1) lower cost, (2) lover profile, (3) small form factor, (4) simpler structure, (5) lighter, (6) less assembly steps, (7) better electrical performance, and (8) eliminate the substrate, underfill, and one level of wafer bumping. The fan-in WLP patent is the third most impactful one in semiconductor packaging, so far.

1.4.4 Fan-Out Wafer-Level Packaging

On October 31, 2001, Harry Hedler, Thorsten Meyer, and Barbara Vasquez of Infineon proposed [20] the use of RDLs (items #**34a–f** in Fig. 1.9) to fan-out the

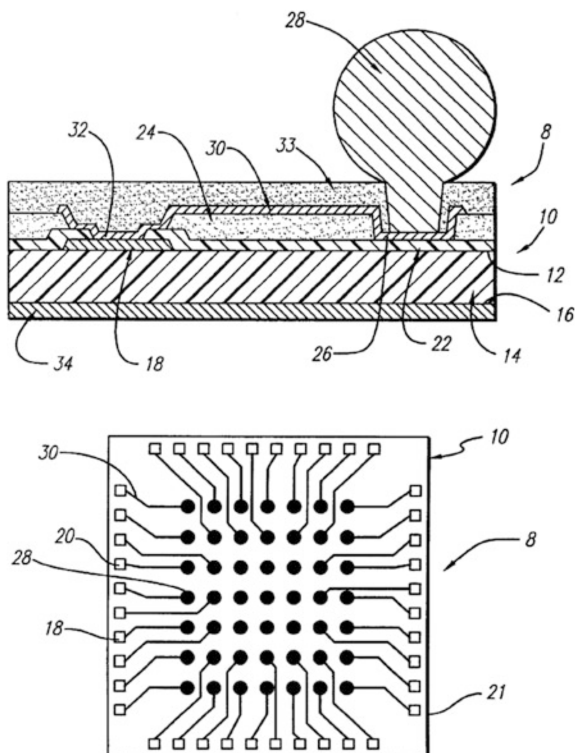


Fig. 1.7 Fan-in WLP patent proposed by flip chip technologies

circuitry from the metal pad (item #**22**) of the chip (item #**16a**) on a wafer and solder ball (items **40a–f**) to the metal pads (items #**52b–g**) on a PCB (item #**50**) without underfill (Fig. 1.9). Some of the RDLs (items #**34a**, **34f**) having a portion that extends beyond (fan-out) the edges (item #**36a**) of the chip (item #**16a**). Item #**26a** is the encapsulant (molding compound). Items #**14a–b** are the dielectric layer.

It should be pointed out that the concept of fan-out WLP was first proposed by Infineon [20]. Even though some of the knowledge of this technology has been patented by General Electric [21, 22] and EPIC [23], however, Infineon's patent [20] specifically pointed out the use of RDLs to fan-out the circuitry from the metal pad of the chip on a wafer and solder ball to the metal pads on a PCB (Fig. 1.10). Infineon also specifically pointed out that some of the RDLs have a portion that extends beyond (fan-out) the edges of the chip. These are the major claimed in [20], which were not claimed by GE and EPIC.

Infineon first commercialized the fan-out WLP for their wireless baseband SoC (system-on-chip) with multiple integrated functions (GPS, FM radio …) for LG's cellphone in 2009. The same SoC has also been used in Nokia's handsets since 2010. Since then, LG (wireless baseband), Samsung (baseband modem), and Nokia (baseband modem and RF transceiver) have used Infineon's fan-out WLP in their cellphones and smartphones. Infineon's fan-out WLP technology was licensed by ASE, STATSChipPAC, STMicroelectronics, and NANIUM (now Amkor).

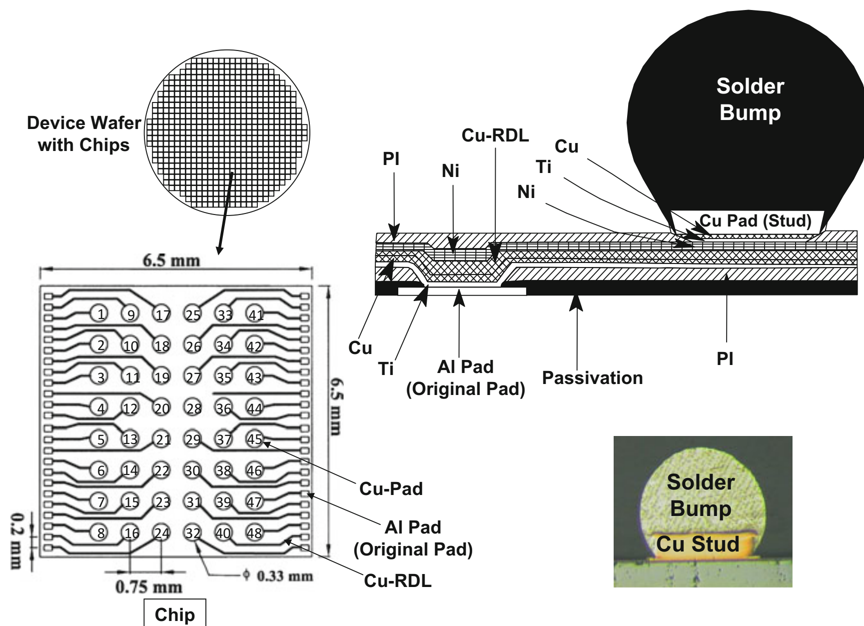


Fig. 1.8 WLCSP made by fan-in WLP technology

In 2011, Intel acquired Infineon's wireless operation, which includes the fan-out WLP patents. Intel used the fan-out WLP technology to package their RF IC (5 mm × 5 mm × 0.67 mm) with 139 solder balls on 0.4 mm pitch.

The advantages of fan-out WLP over fcPBGA packages with solder bumped flip chip are (Fig. 1.11) (1) lower cost, (2) lower profile, (3) eliminating the substrate, (4) eliminating the wafer bumping, (5) eliminating the flip chip reflow, (6) eliminating the flux cleaning, (7) eliminating the underfill, (8) better electrical performance, (9) better thermal performance, and (10) easier to go for system-in-package (SiP) and 3D IC packaging [24].

The advantages of fan-out WLP over fan-in WLP are (Fig. 1.12) (1) the use of known good die (KGD), (2) better wafer-level yield, (3) using the best of silicon, (4) single or multichip, (5) embedded integrated passive devices, (6) more layer of RDLs, (7) higher pin counts, (8) better thermal performance, (9) easier to go for SiP and 3D IC packaging, and (10) higher PCB level reliability.

Fan-out WLP can do the same things fan-in WLP can, such as for low-cost, low-end, low-profile, low pin count, small form factor, and high-volume applications. In addition, fan-out WLP can do most of the things PBGA can, such as for middle-end to high-end microprocessor, ASIC, and memory applications. Even fan-out WLP is not in very high-volume manufacturing yet, however, because of

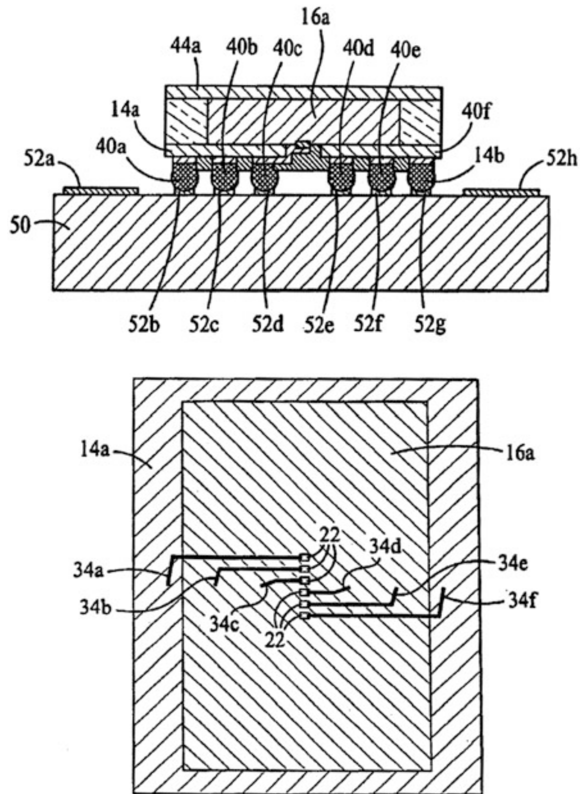


Fig. 1.9 Fan-out WLP patent proposed by Infineon

the important advantages over the fan-in WLP and PBGA; it has the potential for substantial growth. Thus, this author considers fan-out WLP as the four most impactful for semiconductor packaging in the near future.

1.5 Major Claims of Infineon's Patent

The major claims of Infineon's patent [20] are the use of RDLs to fan-out the circuitry from the metal pad of the chip and solder ball to the metal pads on a PCB, Figs. 1.9 and 1.10. The company [20] also claimed that some of the RDLs have a portion that extends beyond the edges of the chip. As a matter of fact, Infineon [20] did not claim anything such as die-first or last, die-up or down, RDL-first or last, mold-first or last, and reconfigured wafer or panel at all. It is a "structure" patent.

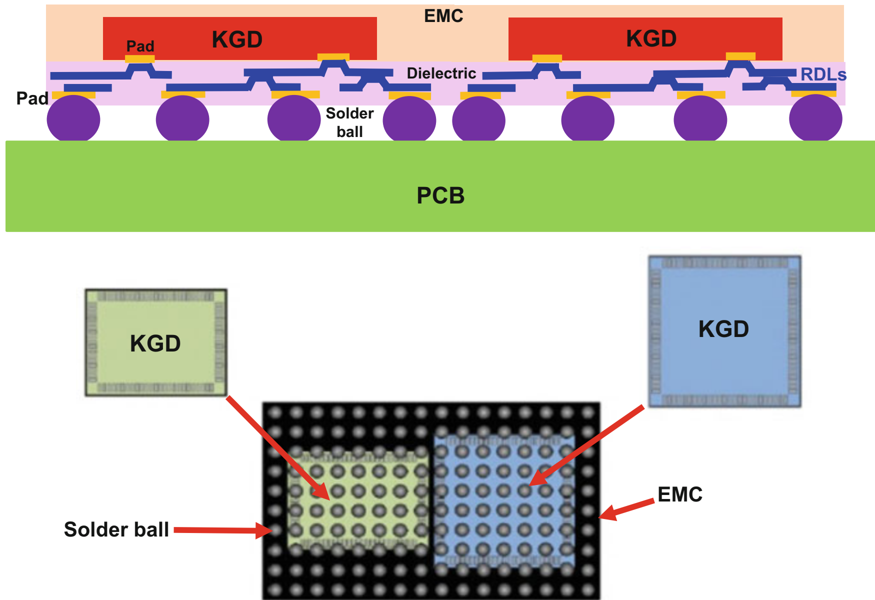
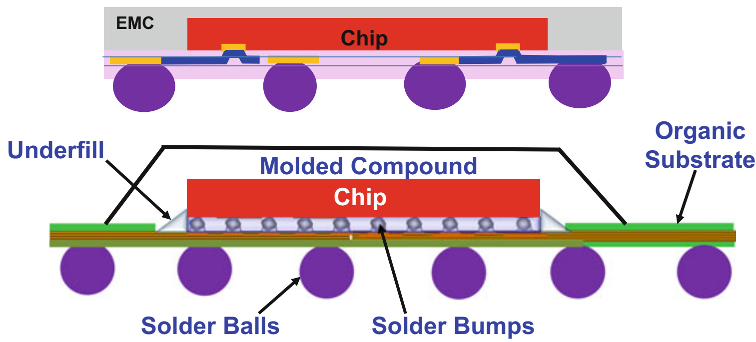


Fig. 1.10 Fan-out WLP—multiple chips



(1) lower cost
(2) lower profile
(3) eliminating the substrate
(4) eliminating the wafer bumping
(5) eliminating the flip chip reflow
(6) eliminating the flux cleaning
(7) eliminating the underfill
(8) better electrical performance
(9) better thermal performance
(10) easier to go for system-in-package (SiP) and 3D IC packaging

Fig. 1.11 Advantages of fan-out WLP over fcPBGA

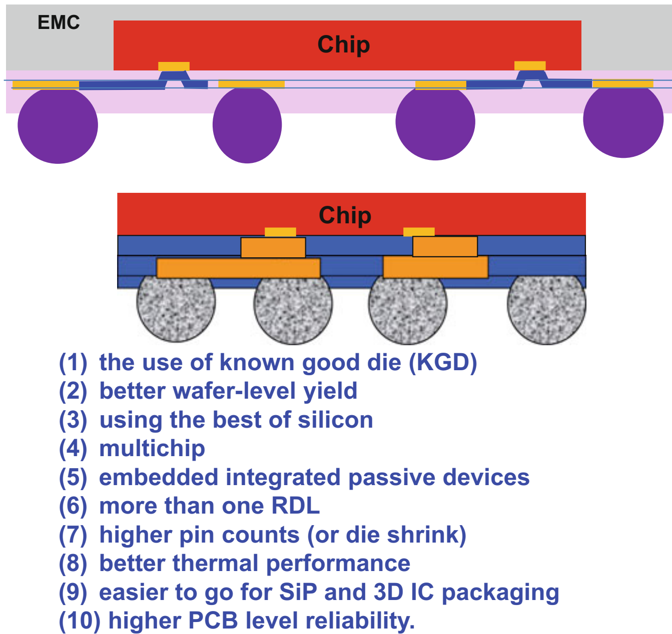


Fig. 1.12 Advantages of fan-out WLP over fan-in WLP

1.6 TSMC InFO-WLP

One of the most famous fan-out WLPs is TSMC' integrated fan-out wafer-level packaging (InFO-WLP). Figure 1.13 schematically shows a typical process of the InFO-WLP technology [25–28]. It starts off by KGD testing of a device wafer. Then, under bump metallization (UBM) is performed by sputtering (e.g., Ti/Cu) with physical vapor deposition (PVD), and the Cu contact pad (or post) accomplished using electroplating. These steps are followed by spin coating a polymer [e.g., polyimide (PI), benzocyclobutene (BCB), or polybenzobisoxazole (PBO)] on top of the whole device wafer and laminating a die-attach film (DAF) on the bottom of the whole device wafer. Then, singulating the device wafer into individual dies, Fig. 1.13a. The individual KGD is placed (face-up) on a temporary round carrier (wafer) with a light-to-heat conversation (LTHC) layer as shown in Fig. 1.13b, and then EMC (epoxy molding compound) dispensing, compression molding, and post-mold curing of EMC are done on the whole temporary wafer with KGDs to form the molded reconstituted wafer (Fig. 1.13c). It is followed by backgrinding the EMC of the reconstituted wafer to expose the Cu contact pad (Fig. 1.13d), building up the RDLs (Fig. 1.13e) with conventional processes [29], and mounting the solder ball, Fig. 1.13e. Finally, remove the temporary wafer (Fig. 1.13f) and singulate the reconfigured wafer into individual units, and then we have the fan-out package by InFO-WLP technology. Comparing the cross section of Fig. 1.13f with

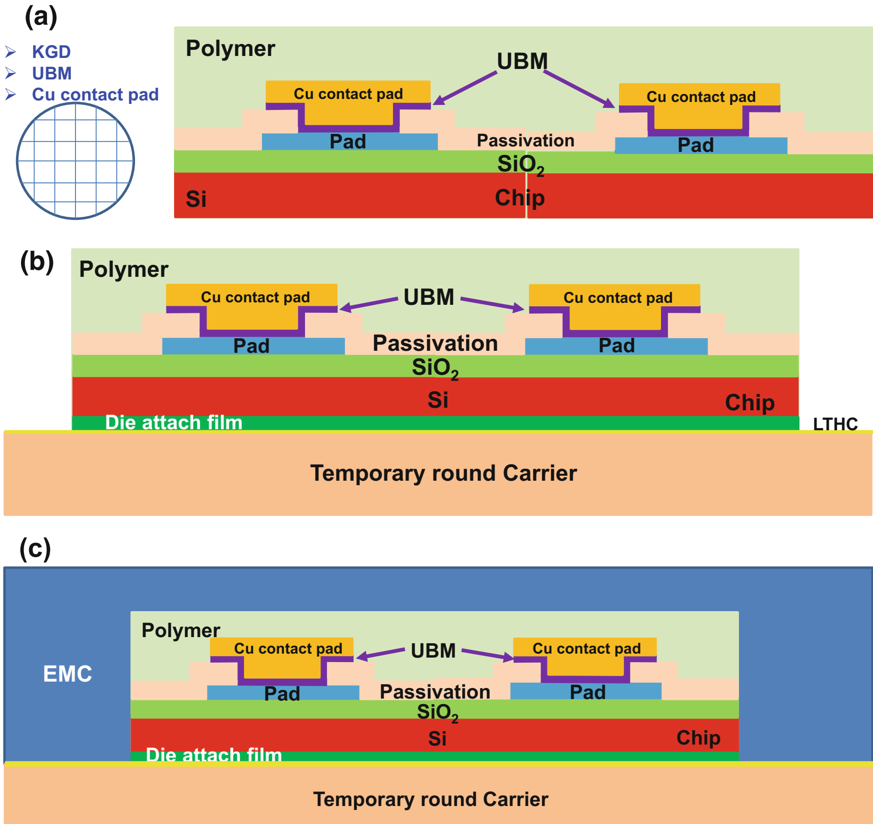


Fig. 1.13 Integrated fan-out (InFO)-WLP patent proposed by TSMC. **a** UBM and Cu contact pad on the Al-pad and polymer over the whole wafer. **b** Laminate a DAF on the backside of the device wafer and attach to a glass carrier with LTHC layer. **c** Compression mold and PMC. **d** Backgrind the EMC to expose the Cu contact pad. **e** Build the RDLs and solder balls. **f** Debond the glass carrier by a laser, then dicing

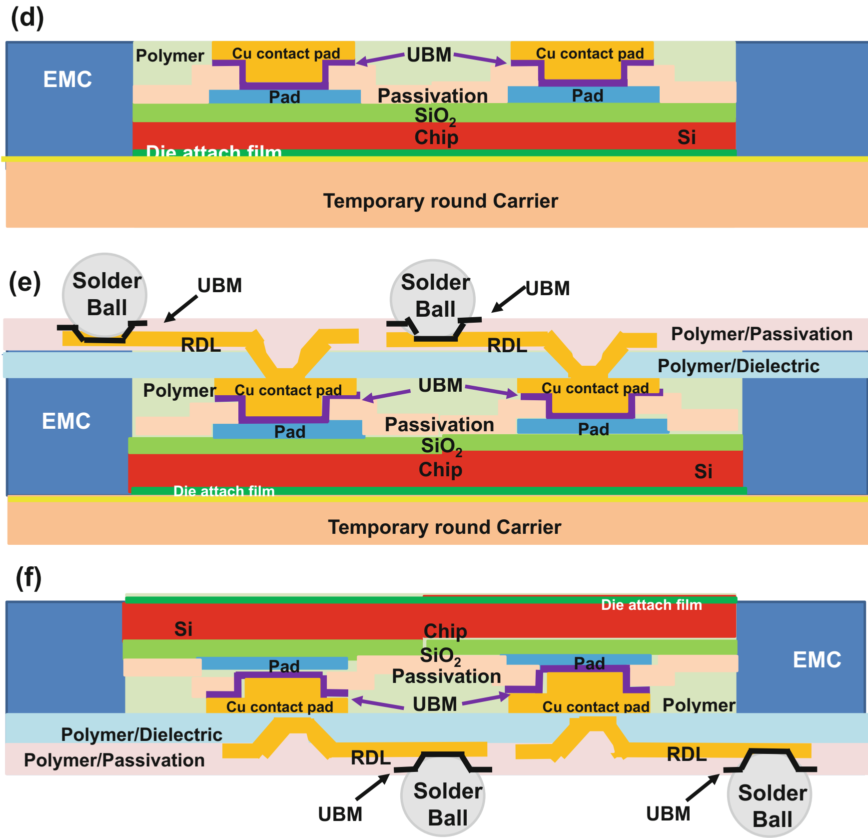


Fig. 1.13 (continued)

that of Figs. 1.9 and 1.10, it can be seen that they are similar, i.e., the RDLs fan-out the circuitry beyond the chip edge.

TSMC have been working on a new package-on-package (PoP) called InFO-PoP for the application processor (AP) chipset (mobile DRAM + AP SoC). Just like TSMC' CoWoS (chip-on-wafer on substrate) technology, they called this PoW (package-on-wafer) technology [30–32]. PoW means the mobile DRAM package is stacked on the AP InFO reconfigured wafer, and the connection between the memory package and the AP InFO package is by through-InFO-via (TIV).

TSMC put the PoP of AP with FOWLP technology into high-volume manufacturing on September 15, 2016. This is very significant, since this means that FOWLP is not just only for packaging baseband, power management IC, RF (radio frequency) switch/transceiver, RF radar, audio codec, microcontroller unit, connectivity ICs, etc., it can also be used for packaging high-performance and large (>120 mm^2) SoC (system-on-chip) such as APs. More information on TSMC's PoP will be presented in Chap. 8.

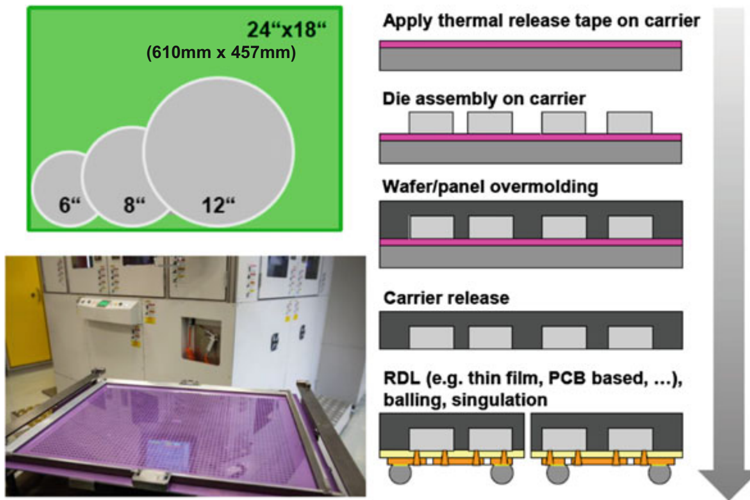


Fig. 1.14 Fraunhofer IZM's fan-out panel-level packaging (FOPLP) process flow

1.7 Fraunhofer IZM FOPLP

During 2015 IEEE/ECTC, Fraunhofer IZM presented a paper [33] that summarized its 3-year development on fan-out panel-level packaging (FOPLP). They showed that with surface mount technology (SMT) equipment for picking and placing the dies and integrated passive devices (IPD) and PCB technology for making the RDLs, they are able to fabricate FOPLP at a very low-cost (with a large panel instead of a wafer) for low-end, low pin count, small chip sizes, and high-volume applications. A typical Fraunhofer IZM FOPLP process flow is shown in Fig. 1.14 and a complete Fraunhofer IZM FOPLP integration line is shown in Fig. 1.15. It can be seen that there is not any semiconductor foundry equipment. Their test vehicle is a standard PCB size (610 mm × 457 mm) rectangular panel as shown in Fig. 1.14. Comparing the cross section of Fig. 1.14 with that of Figs. 1.9 and 1.10, it can be seen that they are almost the same, i.e., the RDLs fan-out the circuitry beyond the chip edge. More Fraunhofer's FOPLP will be presented in Chap. 9.

1.8 Ball/Bump Pitch/Size of PBGA, fcPBGA, WLCSP, and FOWLP

Figure 1.16 shows the solder ball/bump pitch/size of PBGA, fcPBGA, WLCSP, and FOWLP. It can be seen that the solder ball pitches of the wirebonding PBGA are 1.27, 1, 0.8, and 0.65 mm. The solder ball pitches of the fcPBGA are 1.27, 1, 0.8, 0.65, 0.5, and 0.4 mm. The solder ball sizes of the wirebonding PBGA and

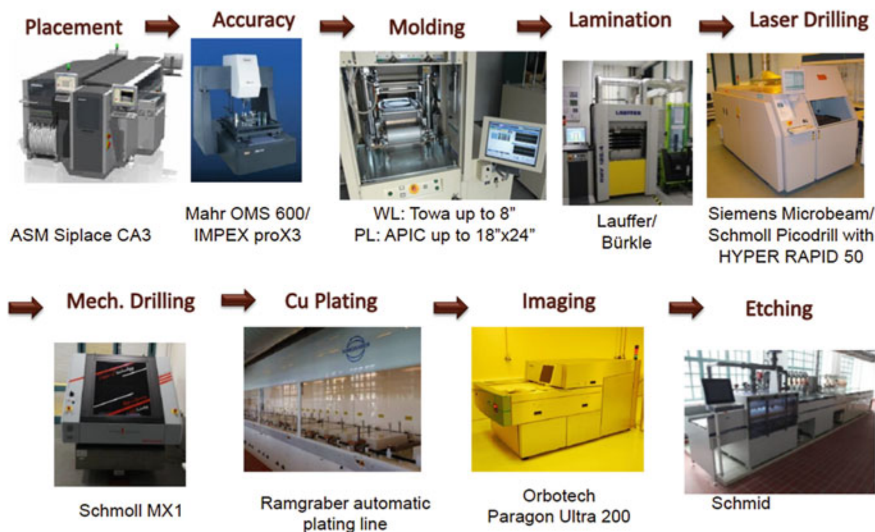


Fig. 1.15 Fraunhofer IZM's fan-out panel-level packaging (FOPLP) integration line

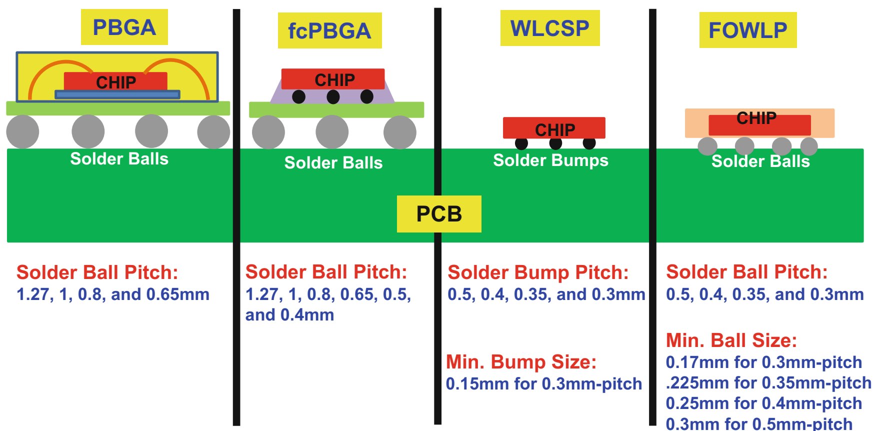


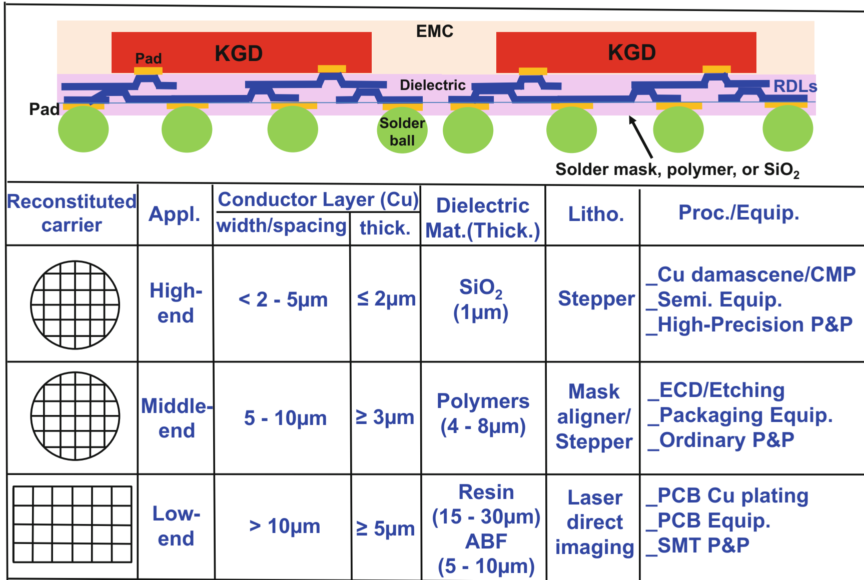
Fig. 1.16 Ball/Bump Pitch/Size of PBGA, fcPBGA, WLCSP, and FOWLP

fcPBGA vary. The solder bump pitch of WLCSP is 0.5, 0.4, 0.35, and 0.3 mm and the solder bump size of WLCSP is 0.15 mm for 0.3 mm pitch. The solder ball pitch and size for FOWLP do not have a standard yet. However, it is recommended that the solder ball pitches of FOWLP are 0.5, 0.4, 0.35, and 0.3 mm. The solder ball sizes of FOWLP are 0.17 mm for 0.3 mm pitch, 0.225 mm for 0.35 mm pitch, 0.25 mm for 0.4 mm pitch, and 0.3 mm for 0.5 mm pitch.

1.9 Summary and Recommendations

The patent issues of embedded fan-out wafer-level packaging have been investigated. Some important results and recommendations are as follows:

- As of today, the patents impacting the semiconductor packaging industry the most are (1) leadframe [3], (2) organic substrate with area-array solder balls [4], (3) fan-in WLP [6], and (4) fan-out WLP [20].
- Fan-out WLP can do the same things fan-in WLP can such as for low-cost, low-end, low-profile, low pin count, small form factor, and high-volume applications.
- Fan-out WLP can do most of the things PBGA can such as for middle-end to high-end microprocessor, ASIC, and memory applications. However, some of the things PBGA can do but fan-out WLP cannot are (1) large die size (≥ 12 mm × 12 mm) and (2) large fan-out package size (≥ 25 mm × 25 mm). These are due to the thermal expansion mismatch and warpage limitations of the fan-out WLP.
- Infineon's patent [20] is a "structure" patent. The major claims are the use of RDLs to fan-out the circuitry from the metal pad of the chip and solder ball to the metal pads on a PCB; some of the RDLs have a portion that extends beyond the edges of the chip.
- If the cross section of an individual fan-out package (no matter if it is made from die-first or last, die-up or down, RDL-first or last, mold-first or last, and reconstituted wafer or panel) looks like the one in Figs. 1.9 and 1.10 (RDLs fan-out the circuitry beyond the chip edge), then it is subjected to Infineon's patent [20].
- Instead of trying to avoid Infineon's fan-out WLP patent [20], the focus should be on the development of new and innovative applications such as TSMC' low-profile and low-cost InFO-PoP and Fraunhofer IZM's low-cost and high-volume FOPLP with SMT and PCB/LDI technology.
- The geometry, material, process, equipment, and application of fan-out wafer/panel-level packaging are recommended as follows (Fig. 1.17).
  - For high-end applications (e.g., high-end APs), the reconstituted carrier is a wafer, and the RDL line width/spacing and thickness are, respectively, ≤ 5 and 2 µm right now. But very soon the RDLs are going down to ≤ 2 and 1 µm, and the lithography process is accomplished using a stepper. They are fabricated by the Cu damascene method. The dielectric layer (SiO_2) is ~ 1 µm thick and fabricated by the plasma-enhanced chemical vapor deposition (PECVD) method. A high-precision pick-and-place (P&P) bonder is needed for die placement.
  - For middle-end applications (e.g., low-end APs, ASIC and memory), the reconstituted carrier is a wafer, and the RDL line width/spacing and thickness are, respectively, 5–10 and 3 µm, and the lithography is accomplished using a mask aligner or stepper for better yield. They are fabricated by the



Reconstituted carrier	Appl.	Conductor Layer (Cu) width/spacing	Conductor Layer (Cu) thick.	Dielectric Mat.(Thick.)	Litho.	Proc./Equip.
	High-end	< 2 - 5µm	≤ 2µm	SiO_2 (1µm)	Stepper	_Cu damascene/CMP _Semi. Equip. _High-Precision P&P
	Middle-end	5 - 10µm	≥ 3µm	Polymers (4 - 8µm)	Mask aligner/ Stepper	_ECD/Etching _Packaging Equip. _Ordinary P&P
	Low-end	> 10µm	≥ 5µm	Resin (15 - 30µm) ABF (5 - 10µm)	Laser direct imaging	_PCB Cu plating _PCB Equip. _SMT P&P

Fig. 1.17 Geometry, material, process, and equipment for fan-out wafer/panel WLP

electrochemical deposition method. The dielectric layer comprises polymers (e.g., PI, PBO, or BCB) and is 4–8 µm thick. An ordinary P&P bonder should be able to perform the die placement.

- For low-end applications (e.g., Wi-Fi/Bluetooth, FM module, RF transceivers, PMIC, baseband, and the power management unit), the reconstituted carrier can be a panel, and the RDL line width/spacing and thickness are, respectively, 10–20 and 5 µm. They can be fabricated using PCB/LDI technology. A resin-coated copper (RCC) sheet or Ajinomoto build-up film (ABF) is laminated on the reconstituted panel. Microvias are drilled through the RCC or ABF layer to the die pads and electrically connected by Cu plating. RDL formation is done by laser direct imaging (LDI) in combination with a dry film resist and copper etching. The dielectric layer (resin or film) ranges from 5 to 30 µm. In general, an SMT P&P is adequate for die and IPD placement.
- There is a small overlapping area between the high-end and middle-end, and the middle-end and low-end.

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Chapter 2
Flip Chip Technology Versus FOWLP

2.1 Introduction

In this chapter, a flip chip is defined [1–4] as a chip attached to the pads of a substrate or another chip with various interconnect materials (e.g., Sn–Pb, Cu, Au, Ag, Ni, In, and isotropic or anisotropic conductive adhesives) and methods [e.g., mass reflow and thermocompression bonding (TCB)], as long as the chip surface (active area or I/O side) is facing the substrate or another chip as shown in Fig. 2.1.

The flip chip technology was introduced by IBM in the early 1960s for their solid logic technology, which became the logical foundation of the IBM System/360 computer line [5]. Figure 2.2a shows the first IBM flip chip with three terminal transistors, which are Ni/Au-plated Cu balls embedded in an Sn–Pb solder bump on the three I/O pads of transistor. A Cr–Cu–Au adhesion/seed layer is deposited between the Al–Si contact pads on the Si chip and the solder bump. Figure 2.2b shows the first IBM flip chip assembly (three chips) on a ceramic substrate.

As the I/Os increase, the Cu ball is replaced by solder bump. The so-called C4 (controlled collapse chip connection) technology [6] utilizes high-lead solder bumps deposited on wettable metal terminals on the chip and a matching footprint of solder wettable terminals on the substrate. The solder-bumped flip chip is aligned to the substrate, and all solder joints are made simultaneously by reflowing the solder.

Today, the applications of flip chip technology have been extended to [7–12] chip-to-chip, face-to-face, and face-to-back. Figure 2.3 shows Amkor's Double-POSSUM package [12]. It can be seen that the package is actually defined by two levels of nesting die. The three daughter dies are flip chip attached to the larger mother die which is then attached to the largest grandma die. The grandma die is then flip chip attached to the package substrate. The bumps between the daughter dies and the mother dies are microbumps (Cu pillar with solder cap). C4 bumps are used between the mother die and grandma die, and between the grandma die and package substrate.

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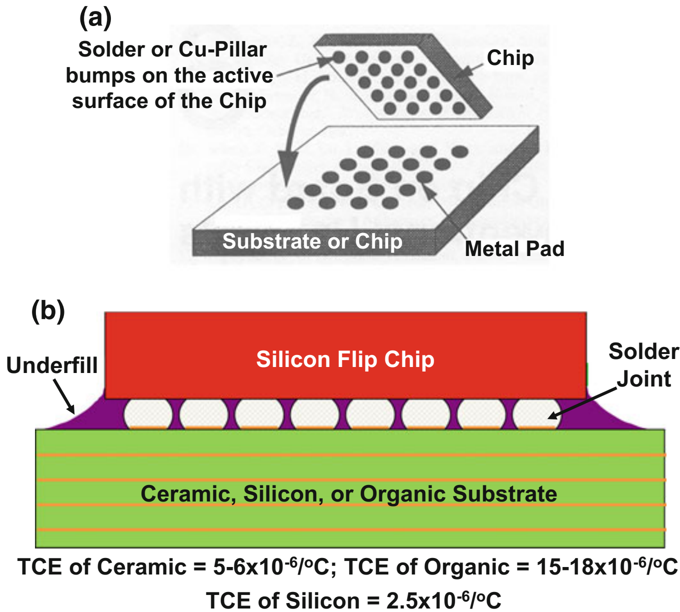


Fig. 2.1 **a** Definition of flip chip assembly. **b** Flip chip assembly on various substrates

Flip chip technologies have been used extensively for the processors of mainframe computers, servers, personal computers, notebooks, smartphones, tablets, games, etc., the application-specific integrated circuits (ASICs) of networking, telecommunications, etc., and the memories of data storage devices, etc. Most of the flip chip assemblies are mass reflowed.

Recently, because of the requirements of higher functionalities of the chips and shrinking the chips' area, the number of pin-outs of the processors, ASICs, and memories increases and their pitch (or the spacing between the pin-out pads) decreases. Also, because of the trends of smaller form factors for mobile (e.g., smartphones and tablets) and portable (e.g., notebooks) products, the thickness of the chips and package substrates must be as thin as possible. Higher pin counts, tighter pitches, thinner chips, and thinner package substrates lead to the necessity of the TCB method for flip chip assemblies. In this study, besides mass reflow, various TCB techniques are mentioned.

Recent advances in high-density and low-cost package substrates have promoted more flip chip applications. In this study, the organic build-up substrate, organic build-up substrate with thin-film layers, coreless substrate, bump-on-lead (BOL), and embedded trace substrate (ETS) will be discussed.

In order to enhance the solder joint reliability of flip chip assemblies, underfill is a must, especially for organic package substrate. In this study, the preassembly underfill such as the no-flow underfill (NUF), nonconductive paste (NCP), and nonconductive film (NCF) will be discussed. Also, the post-assembly underfill such

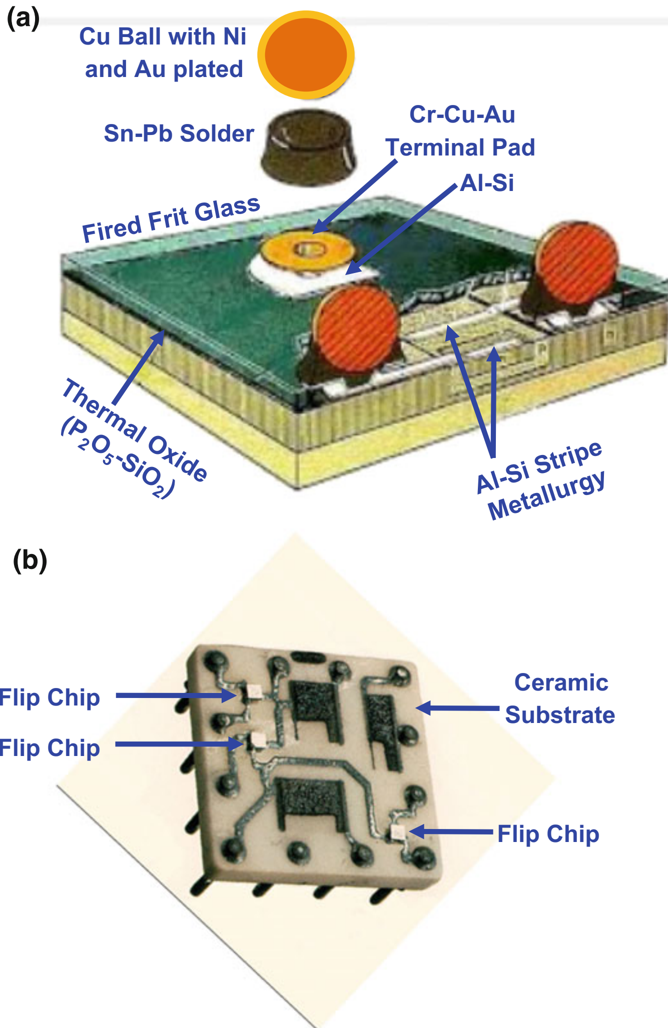


Fig. 2.2 **a** IBM's first flip chip component with three-terminal transistors. **b** IBM's first flip chip assembly (3 chips) on a ceramic substrate

as the capillary underfill (CUF) and molded underfill (MUF) will be examined. Since wafer bumping is the mother of flip chip technology, it will be briefly mentioned first.

Flip chip technology is facing stiff competition from fan-out wafer-level packaging (FOWLP) [13, 14], which will be discussed in Chaps. 4, 5, 6, 7, 8, 9, 10, and 11. Fan-in wafer-level packaging (WLCSP) [15–17] will be discussed in Chap. 3.

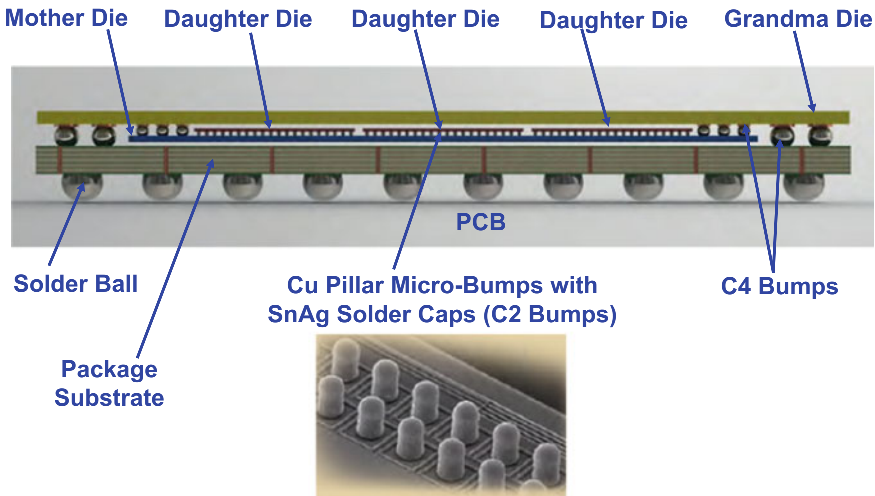


Fig. 2.3 3D IC packaging (Amkor's multiple chip-to-chip interconnects)

2.2 Wafer Bumping

There are many ways to perform the wafer bumping (at least 12 are shown in [2]), and the most common method is by electrochemical deposition (ECD) or electroplating [18]. Stencil printing method [19–25] is also used for wafer bumping but it will not be presented herein.

2.2.1 C4 Bumps

Usually, the pad size is equal to 100 μm and the target bump height is equal to 100 μm. After redefining the passivation opening (usually, it is not required), either Ti or TiW (0.1–0.2 μm) are sputtered over the entire surface of the wafer first, followed by 0.3–0.8 μm of Cu. Ti–Cu and TiW–Cu are called under bump metallurgy (UBM). In order to obtain 100 μm bump height, a 40 μm layer of resist is then overlaid on the Ti–Cu or TiW–Cu and a solder bump mask is used to define (ultraviolet exposure) the bump pattern as shown in steps #1–4 in Fig. 2.4. The opening in the resist is 7–10 μm wider than the pad opening in the passivation layer. A 5 μm layer of Cu is then plated over the UBM, followed by electroplating the solder. This is done by applying a static or pulsed current through the plating bath with the wafer as the cathode. In order to plate enough solder to achieve the target (100 μm), the solder is plated over the resist coating by about 15 μm to form a mushroom shape. The resist is then stripped off and the Ti–Cu or TiW–Cu is removed with a hydrogen peroxide or plasma etching. The wafer is then reflowed

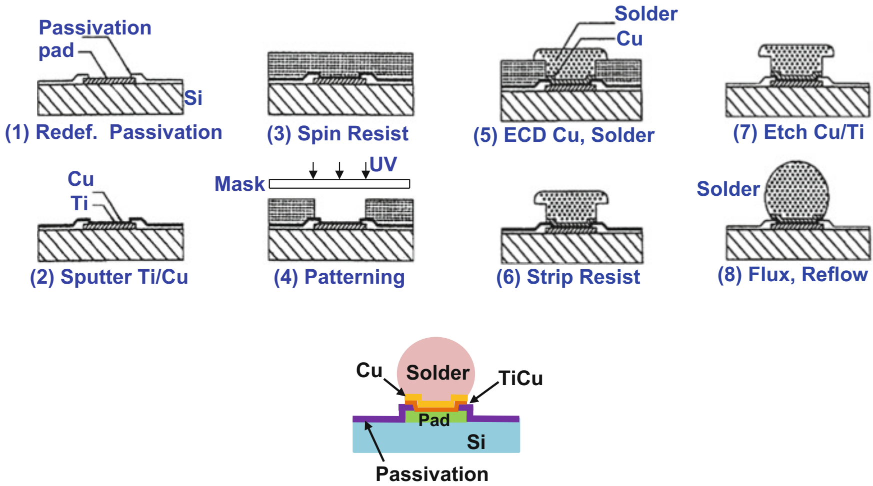
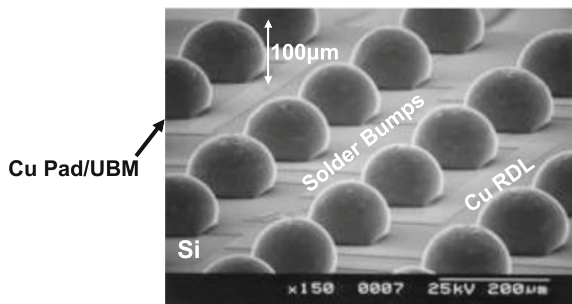


Fig. 2.4 Wafer bumping by ECD or electroplating method for C4 bumps

Fig. 2.5 SEM image of C4 bumps



with flux, which creates smooth truncated spherical solder C4 bumps, Figs. 2.4 and 2.5, due to surface tension as shown in steps #5–8 on the right-hand side of Fig. 2.4 [18].

2.2.2 C2 (Cu Pillar with Solder Cap) Bumps

Because of higher pin count and tighter pitch (smaller spacing between pads), there is a possibility of shorting the adjacent solder C4 bumps. Wire interconnects [26] and Cu pillar with solder cap [27, 28] can be a solution. The fabrication process is basically the same as that of the C4 bumps except electroplating the Cu instead of solder as shown in step #5 of Fig. 2.6. It is followed by electroplating the solder cap and then reflowing the solder with flux (Fig. 2.7a shows the Cu pillar with solder

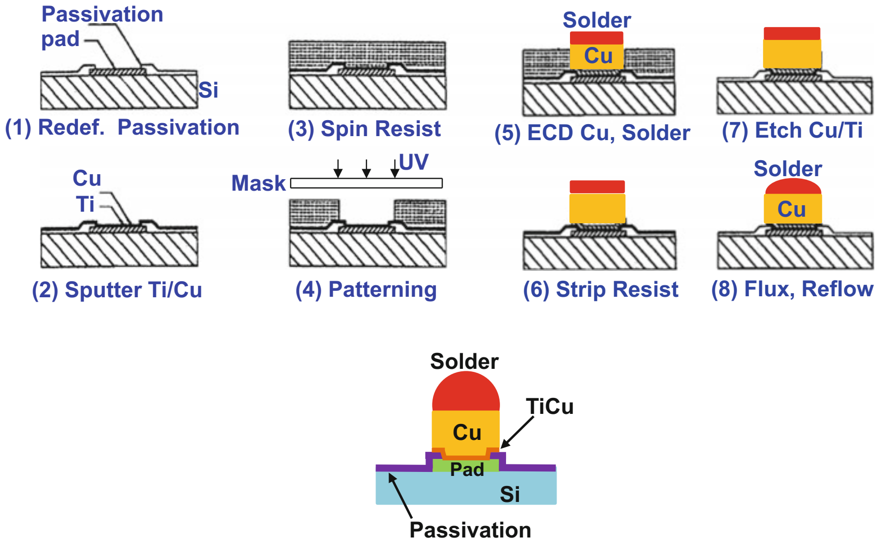


Fig. 2.6 Wafer bumping by ECD or electroplating method for C2 bumps

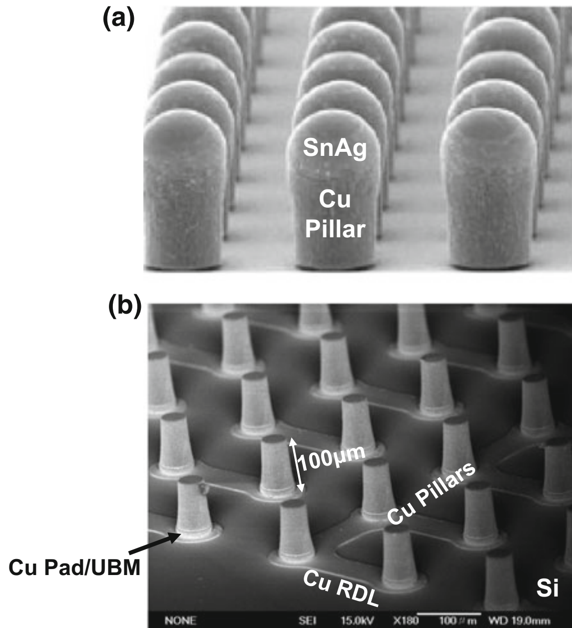


Fig. 2.7 **a** SEM image of C2 bumps with solder cap. **b** SEM image of C2 bumps without solder cap

Table 2.1 C4 bumps versus C2 bumps

Structure	Major material	Thermal conductivity (W/m K)	Electrical resistivity (μΩm)	Pad pitch	Self-alignment
C2 bump	Cu	400	0.0172	Smaller	Smaller
C4 bump	Solder	55–60	0.12–0.14	Larger	Larger

cap and Fig. 2.7b shows the very tall Cu pillar without solder cap). Because the solder volume is very small compared with the C4 bump, the surface tension is not enough to perform the self-alignment of the Cu pillar with the solder cap bump and therefore, it is sometimes called a C2 (chip connection) bump. Besides being able to handle finer pitch, C2 bumps also provide better thermal and electrical performances than C4 bumps. This is because the thermal conductivity (W/m K) and electrical resistivity (μΩm) of Cu (400 and 0.0172) are superior to those (55–60 and 0.12–0.14) of solder as shown in Table 2.1.

2.3 Flip Chip Package Substrates

In the past few years, tremendous efforts have been devoted to enhance/advance the capabilities of the conventional low-cost build-up organic package substrates by increasing the number of build-up layers, fabricating thin-film layers on top of the build-up layer, shrinking the dimensions of the metal line width and spacing, reducing the pad size and pitch, eliminating the core, making the BOL, and laminating the ETS. For silicon substrates, first come with the TSV interposer and the future trend is for TSV-less interposer, which will be discussed in Chap. 10. Ceramic substrate [29–34] will not be discussed in this book.

2.3.1 Surface Laminar Circuit (SLC) Technology

Almost 25 years ago, IBM in Japan at Yasu invented the SLC technology, Fig. 2.8 [35–38], which formed the basis of today's very popular low-cost organic package substrates with build-up layers vertically connected through microvias [39–59] to support flip chips. There are two parts of the SLC technology: one is the core substrate and the other is the SLC for the signal wiring. The core substrate is made by the ordinary glass epoxy panel. However, the SLC layers are sequentially built up with the dielectric layers made of photo-sensitive epoxy and the conductor plane of copper plating (semi-additive technique). In general, a package substrate with twelve layers [e.g., two core layers and ten build-up layers (5-2-5)] and 10 μm line width and spacing are more than adequate to support most of the chips.

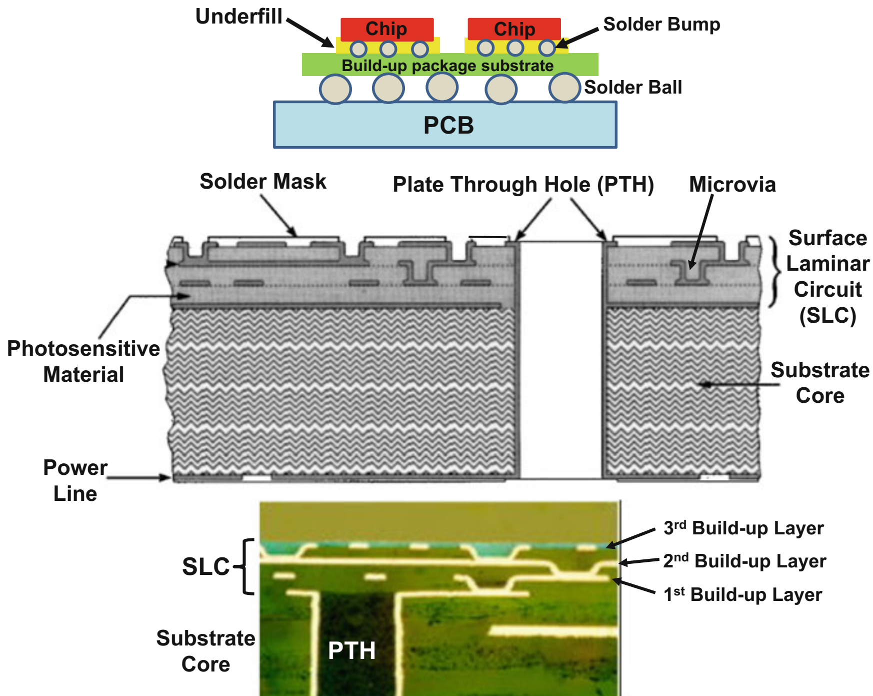


Fig. 2.8 IBM's SLC for flip chip organic build-up package substrate

2.3.2 Integrated Thin-Film High-Density Organic Package (i-THOP)

In 2013, Shinko proposed to make thin-film layers on top of the build-up layer of a package substrate. Figure 2.9 shows Shinko's i-THOP substrate [60, 61] for high-performance applications. It is a 4 + (2-2-3) test vehicle, which means there is a two-layer metalcore, three build-up metal layers at the bottom (PCB) side, two build-up metal layers on the top (chip) side, and the first number "4" represents that there are four thin-film Cu wiring layers (RDLs) on the surface of the top build-up layer. The thickness, line width, and spacing of the thin-film Cu RDLs can be as small as 2 μm. The thin-film Cu RDLs are vertically connected through a 10 μm via, as shown in Fig. 2.9. The surface Cu pad pitch is 40 μm, and the Cu pad diameter is 25 μm with a height of 10–12 μm. The i-THOP substrate passed the warpage and reliability tests and there was no via delamination observed [60].

In 2014, Shinko demonstrated that [61] ultrafine pitch flip chips can be successfully assembled on the i-THOP substrate. Figure 2.10 schematically shows the two chips' lateral communications by the 2 μm line width/spacing RDLs of the two thin-film layers, which are built on top of the 1-2-2 build-up organic substrate,

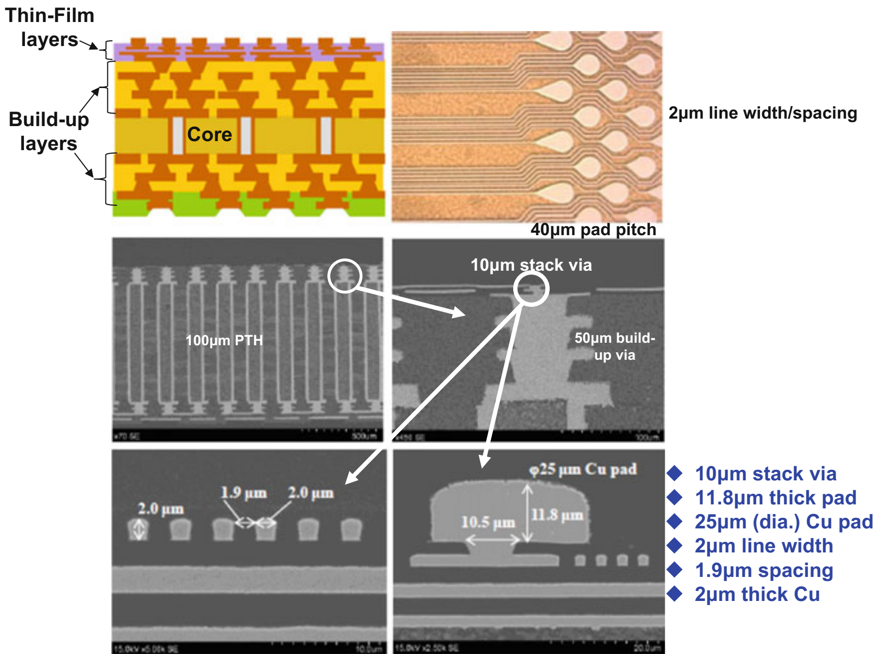


Fig. 2.9 Shinko's i-THOP; a flip chip package substrate with thin film layers on top of the build-up layer

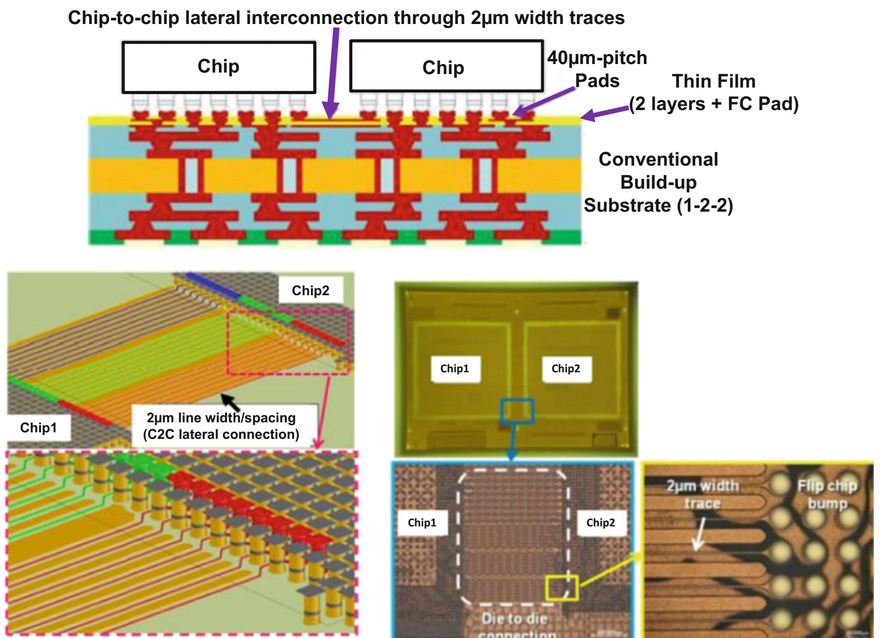


Fig. 2.10 Shinko's i-THOP test vehicle. Two thin-film layers are built on top of the 1-2-2 package substrate

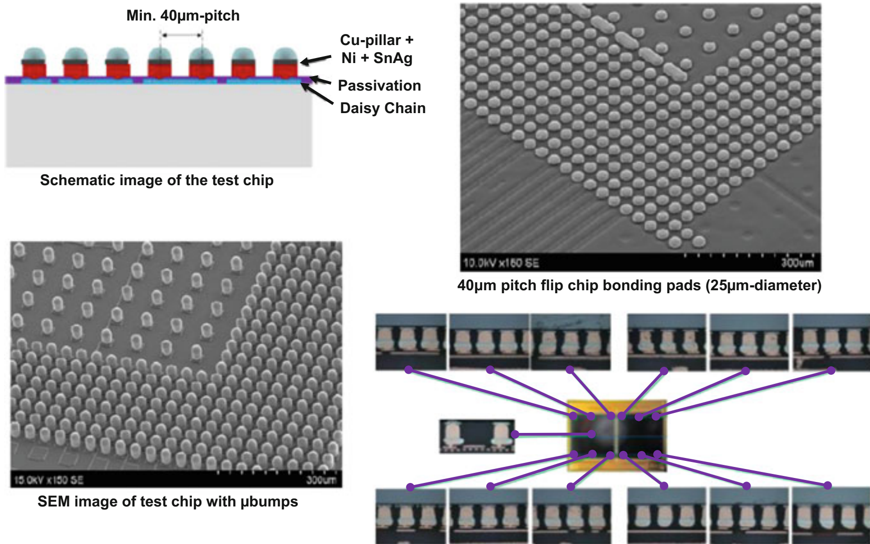


Fig. 2.11 C2 Microbumps at 40 µm pitch. 40 µm pitch flip chip bonding pads (25 µm diameter) on the i-THOP substrate. Good solder joints from optimized condition

i.e., 2 + (1-2-2). Figure 2.11 shows the 40 µm pitch microbumps (Cu pillar + Ni + SnAg) of the test chips and the 40 µm pitch flip chip bonding pads (25 µm diameter). Typical images of the cross section of the flip chip assembly with optimized conditions are shown in Fig. 2.11. It can be seen that good solder joints are confirmed in all areas of the assembly [61].

2.3.3 Coreless Substrate

Coreless substrate was first proposed by Fujitsu [62] in 2006. Figure 2.12 shows the comparison between the conventional organic package substrate with build-up layers and the organic coreless package substrate. It can be seen that the biggest difference is that there is not a core in the coreless package substrate and all the layers of the coreless package substrate are the build-up layers [62–84].

The advantages of the coreless package substrate are [62–84]: (a) because of eliminating the core, the cost of the coreless substrate is lower; (b) by eliminating the core, higher wiring ability can be achieved; (c) better electrical performance because of good high-speed transmission characteristic; and (d) definitely smaller form factor. On the other hand, the disadvantages are [62–84]: (a) because of eliminating the core, the warpage of the coreless substrate is larger; (b) easier to have laminate chipping; (c) poor solder joint yield because of less substrate rigidity;

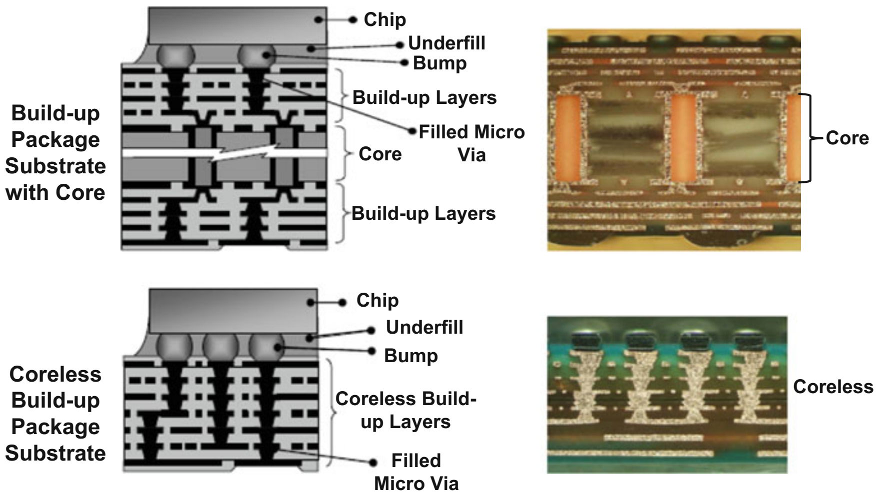


Fig. 2.12 (Top) Flip chip on conventional build-up package substrate. (Bottom) Flip chip on coreless substrate

and (d) new manufacturing infrastructure is necessary. In 2010, Sony manufactured the first coreless package substrate for the cell processor of their PlayStation 3 [74].

Even though coreless substrates have many advantages, they are not popular because of the warpage control issue. One of the key factors affecting the warpage is the coefficient of thermal expansion mismatch of substrate materials. Thus, a proper control of this factor will help reduce the warpage issue of coreless substrates. Another factor affecting the warpage is the package assembly. Thus, a proper package assembly warpage correction control (with vacuum and pressure) will help improve the warpage problem of coreless substrate.

2.3.4 Bump-on-Lead (BOL)

BOL was first proposed by STATS ChipPAC [85–89] and was used by Qualcomm [90] and others [90–93]. A conventional bump-on-capture pad (BOC) or simply bump-on-pad (BOP) flip chip organic substrate layout is shown in Fig. 2.13a. It can be seen that the flip chip pads are on a 210-μm area-array pitch in a solder mask (SR) defined configuration with one signal escape between bump pads resulting in an effective escape pitch of 105 μm. The BOL methodology is shown in Fig. 2.13b; here, the landing pad on the substrate is merely the trace (lead) itself, or a slightly widened version of the trace which results in freeing up of enough routing space to allow routing an additional trace between bumps thereby resulting in an effective escape pitch of 7 μm without changing the design rules (trace width and space) of the substrate. The improved BOL structure is shown in Fig. 2.13c. It can be seen

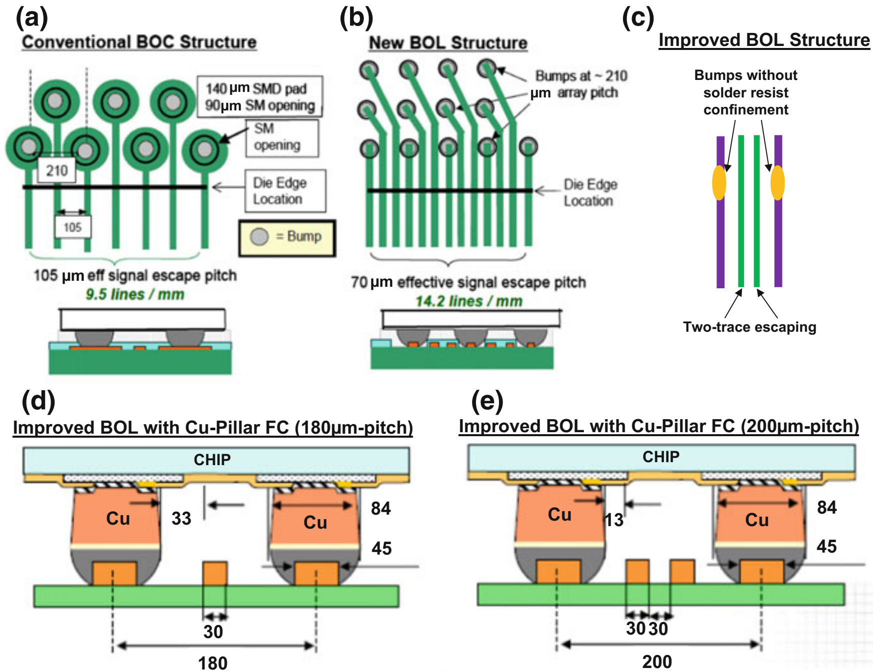


Fig. 2.13 Bump-on-lead (BOL). **a** Conventional BOP. **b** New BOL. **c** Improved BOL. **d** Improved BOL with Cu pillar FC (180 μm pitch). **e** Improved BOL with Cu pillar FC (200 μm pitch)

that the bump pads are without any solder resist confinement, i.e., open SR [90]. The test vehicles, Cu column on BOL, used in Ref. [90] are shown in Fig. 2.13d and e. It can be seen that one trace between the 180 μm bump pitch and up to two traces with the 20 μm bump pitch can be comfortably routed.

Typical cross sections of the perpendicular-to-BOL and longitudinal-to-BOL are shown in the upper portion of Fig. 2.14. A 3D slide finite element model showing the BOL, BOC (or BOP), and solder joint is shown in the middle of Fig. 2.14. The creep strain contours of the BOL solder joint are shown in the lower portion of Fig. 2.14 [93] and are too small to create solder joint reliability problem under most conditions.

2.3.5 *Embedded Trace Substrate (ETS)*

ETS is one of the coreless substrates with fine line width/spacing embedding the top metal trace pattern into prepreg layer [94–98]. The process flow of ETS is shown in Fig. 2.15a. It starts from a carrier board with a removable Cu foil. It is followed by

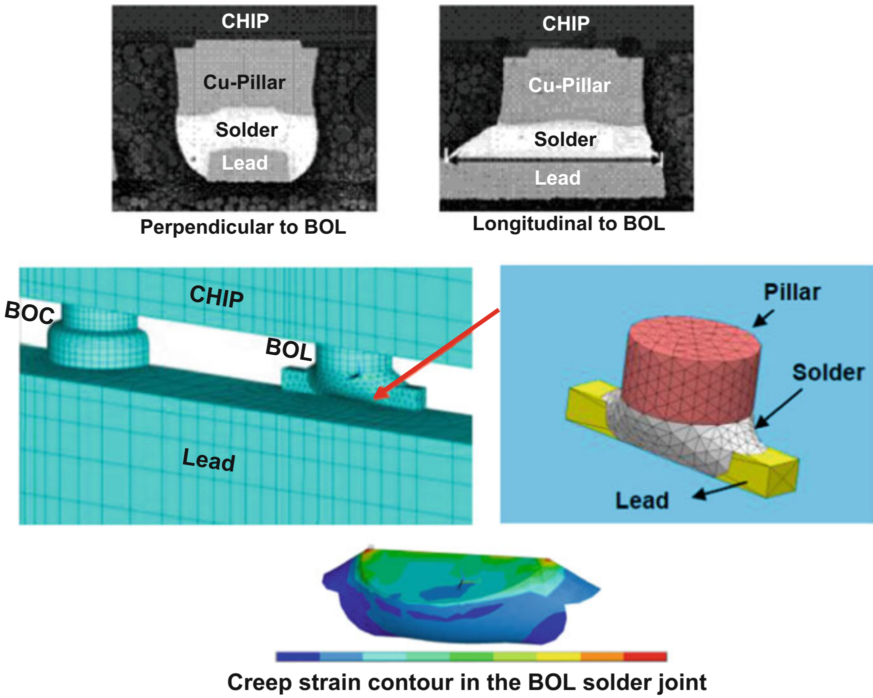


Fig. 2.14 Images of the perpendicular-to-BOL and longitudinal-to-BOL. Finite element models and creep strain contours in the BOL solder joint

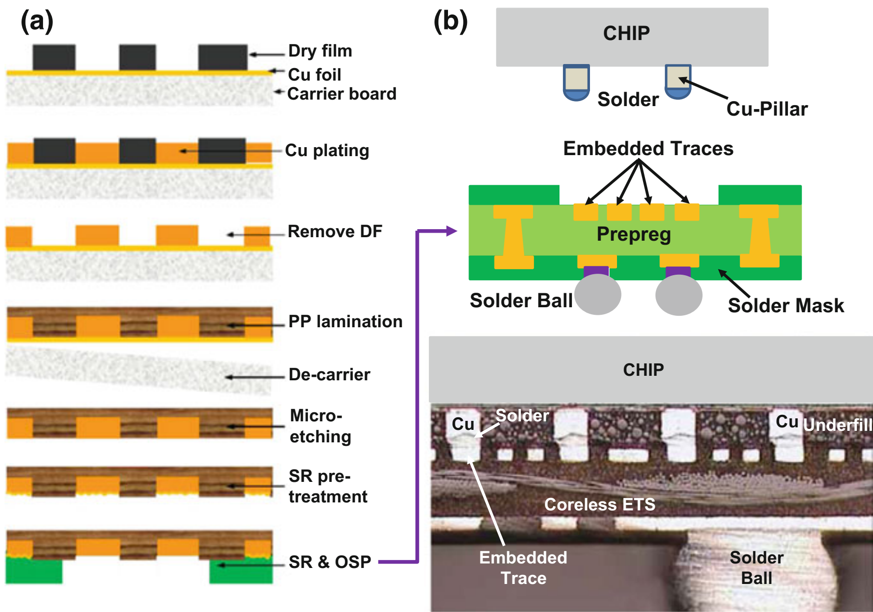


Fig. 2.15 **a** Process flow for fabricating the ETS. **b** Flip chip with C2 bumps on ETS assembly

using a typical electrolytic copper plating method to form the first layer of copper pattern. Then, laminate a prepreg on the copper pattern. It is followed by laser via drilling, electroless copper coating, dry film laminating, exposing and developing, second-layer copper pattern plating, stripping, and micro-etching. Once all the copper pattern layers have been completed, the carrier board will be removed. Since the Cu foil is connected to the first copper pattern, micro-etching is necessary before SR coating. After the SR opening process, it is completed by metal finishes treatment, e.g., organic solderability preservatives (OSPs). Figure 2.15b shows a cross section of a Cu pillar flip chip on ETS assembly by SPIL [97]. Most line width/spacing of ETS in use today is 15/15 µm. However, 13/13 µm line width/spacing is in production by Simmtech [98].

2.4 Flip Chip Assembly

Basically, there are two groups of flip chip assemblies: one is with an intermediate layer between the bonding pads/traces, and the other is not, i.e., nothing! Flip chip assembly with intermediate layers such as solder for mass reflow and Cu pillar with solder cap by TCB is called as indirect bonding, which is the focus of this chapter. Cu-to-Cu diffusion bonding, which does not have anything between the bonding pads/traces on the chip/wafer, is therefore called as direct bonding.

2.4.1 Cu-to-Cu TCB Direct Bonding

Cu-to-Cu diffusion bonding can go down to ultrafine pitch and pad size (the spacing between pads is 5 µm or less). In order to reduce the tendency to form native oxides that strongly affect the bonding quality and reliability, Cu-to-Cu is a TCB and usually operates at high temperature and pressure and long process time [99–101], which are not good for throughput and the device reliability. On the other hand, Cu-to-Cu bonding at room temperature [102–108] leads to the highest throughput and the least amount of device reliability concerns, as well as very low costs. However, the drawbacks of room temperature bonding are the stringent requirements on (a) pad/trace/wafer planarization, (b) surface treatment to ensure smooth hydrophilic surfaces for high-quality bonding, and (c) the class of cleanroom (very high required). Cu-to-Cu TCB is mainly for wafer-to-wafer (W2W) assembly process and is not in high-volume manufacturing yet, and thus, it is discussed at the end of this chapter.

2.4.2 C4 Solder Mass Reflow

Solder mass reflow has been used for flip chip assembly for almost 50 years. Most of the solder C4 bumps are mass reflowed on either silicon, ceramic, or organic substrates. The assembly process is very simple, Fig. 2.16a: (i) use a lookup and lookdown camera to identify the location of the bumps on the chip and the pads on the substrate; (ii) apply flux on either the C4 bumps, or the substrate, or both; and (iii) pick and place the C4-bumped chips on the substrate, then mass reflow with temperature H. Because of the surface tension of the C4 solder bumps during reflow, the process is very robust (self-alignment). Figure 2.17 shows the cross section of iPhone 6 Plus (September 2015). It can be seen that the A9 application processor is housed in a PoP format and the solder-bumped flip chip is mass reflowed on a 2-2-2 organic package substrate. In general, the spacing between the bumps on the solder mass reflow of C4-bumped chips can be as small as 50 μm.

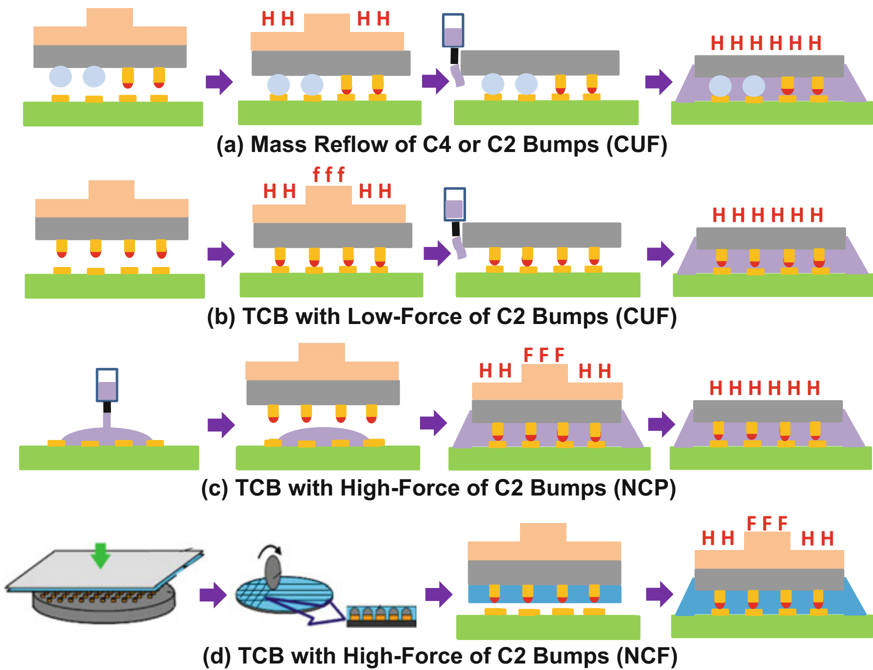


Fig. 2.16 Flip chip assembly with indirect bonding. **a** Mass reflow of chips with C4 or C2 bumps with CUF. **b** TCB with low force of chips with C2 bumps with CUF. **c** TCB with high force of chips with C2 bumps with NCP. **d** TCB with high force of chips with C2 bumps with NCF

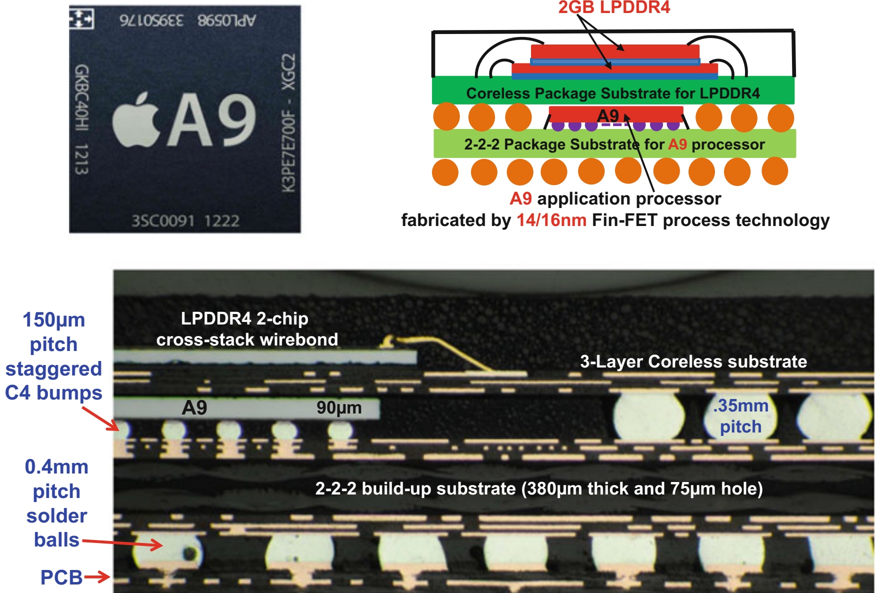


Fig. 2.17 PoP in Apple's smartphone. The C4 solder-bumped flip chip is mass reflowed on a 2-2-2 package substrate

2.4.3 C2 Solder Mass Reflow

In the past few years, solder mass reflow of C2 (Cu pillar with solder cap)-bumped chips on either silicon, ceramic, or organic package substrates has been tried for high pin count and fine-pitch flip chip assemblies. The assembly process, Fig. 2.16a, is exactly the same as that of the C4 bumps, but the self-alignment characteristic is nowhere near the same, and thus, it is seldom being used. In general, the spacing between the pillars on the solder mass reflow of C2-bumped chips can be as small as 25 μm.

2.4.4 C2 TCB

In the past few years, TCB of chips with an intermediate layer such as C2 (Cu pillar with solder cap) bumps on silicon, ceramic, or organic package substrates, has been attracting attention for high-density and ultrafine pitch flip chip assemblies. Basically, there are two methods, one is with low bonding force and the other is with a high bonding force.

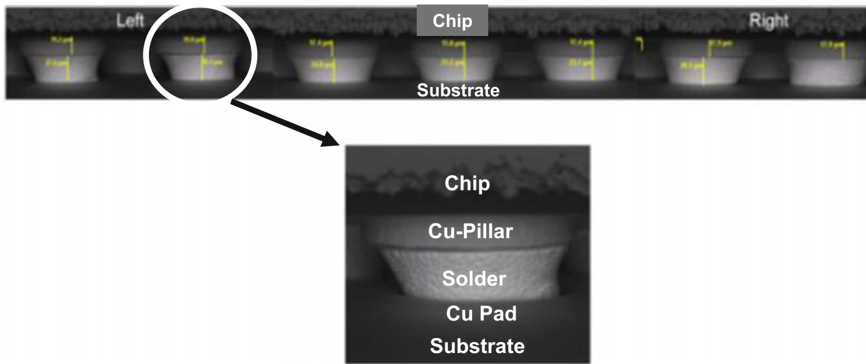


Fig. 2.18 Cross section of a C2 flip chip assembled on an organic package substrate by a TCB with low force (CUF)

2.4.4.1 C2 TCB with Low Bonding Force

For the one with low bonding force, the assembly process is simple, Fig. 2.16b: (i) first, use the lookup and lookdown camera to locate the position of the C2 bumps on the chip and their corresponding pads on the substrate; (ii) apply flux on the solder cap or on the substrate or both; and (iii) pick and place the chip on the substrate and then apply temperature (H) to melt the solder and a low force (f) to hold the chip at a certain distance from the substrate. The above procedure is done one chip at a time and therefore, the throughput is low in comparison with the C2 solder mass reflow process. Figure 2.18 shows a typical cross section of a flip chip assembly with TCB with low force on C2 bumps [109]. In general, the spacing between the pillars on the C2 chip by TCB with a low bonding force can be as small as 8 μm.

2.4.4.2 C2 TCB with High Bonding Force

For TCB with a high bonding force on the C2 chip, the assembly process must be combined with the NCP or NCF underfill, which will be discussed in Sect. 2.5.

2.5 Underfill/Reliability

The reliability of flip chip solder joints is enhanced by the application of underfill [110–124], especially on organic substrate. Most underfills consist of low-expansion fillers such as fused silica (SiO_2) and a liquid prepolymer such as thermosetting resin (adhesive) that can be cured to a solid composite.

In 1987, Hitachi showed that with underfill, the thermal fatigue life of the flip chip solder joints on ceramic substrate increased [125]. In 1992, IBM at Yasu proposed the use of the low-cost organic substrate instead of the high-cost ceramic substrate for flip chip assemblies [35–38]. They showed that with underfill, the large thermal expansion mismatch between the silicon chip (2.5×10^{-6}/°C) and the organic substrate ($15–18 \times 10^{-6}$/°C) is reduced substantially and the solder joints are reliable for most applications. This opened up the doors for today's very popular solder-bumped flip chip on low-cost organic substrate packages used, e.g., in the processors of personal computers, notebooks, smartphones, tablets, etc.

Basically, there are two different procedures to apply the underfill, namely preassembly underfill and post-assembly underfill.

2.6 Post-assembly Underfill

For post-assembly underfill, the application of underfill is after the flip chip assembly, i.e., the flip chip is already on the substrate and the solder joints are already mass reflowed (either with C2 or C4 bumps) or low-force TCB with C2 bumps.

2.6.1 Capillary Underfill (CUF)

For post-assembly underfill, there are basically two methods, namely CUF [126–129] and MUF [130–134]. CUF is the first method that went into volume production [126–129]. For CUF, the underfill is dispensed by a needle or jet w/o vacuum assisted on one (or two) sides of the flip chip on substrate assembly. Because of capillary action, this underfill completely fills the space between the chips, solder joints, and substrates. The chip and the substrate are then firmly bonded by curing the underfill. CUF is performed one chip assembly at a time, and thus, throughput is an issue.

2.6.2 Molded Underfill (MUF)

Molded underfill was first proposed by Cookson Electronics [130] in 2000 and later by, e.g., Dexter [131], Intel [128], Amkor [132], STATS ChipPAC [133], and LETI/STMicroelectronics [134]. For MUF, the modified EMC is transferred molding the chip and filling the gap between the chip, solder joints, and the substrate of the flip chip assembly. The encapsulant of the chip and the underfill are formed at the same time, which will increase the throughputs. However, the challenges of MUF are (a) the flow of MUF between the chip and the substrate is

usually assisted by vacuum; (b) the size of the silica filler of the EMC must be very small for flowability; (c) the cost of EMC for MUF is much higher than that for package molding; (d) package warpage is an issue due to the thermal expansion mismatch between the EMC, chip, and substrate; (e) the molding temperature is limited by the melting point of the solder joints; and (f) the standoff height and pitch of the solder joints cannot be too small.

2.6.3 Printed Underfill

In order to increase the throughput of CUF and avoid the drawbacks of MUF, a method of post-assembly underfill has been proposed by Lucent Technologies [135], where a stencil is used to print the underfill material for flip chips on package substrate assembly as shown in Fig. 2.19. It can be seen that (1) the stencil design is with a wide opening which is at least the size of the chip [135]; (2) the stencil thickness is not above the height of the flip chip assembly [135] (Fig. 2.19); and

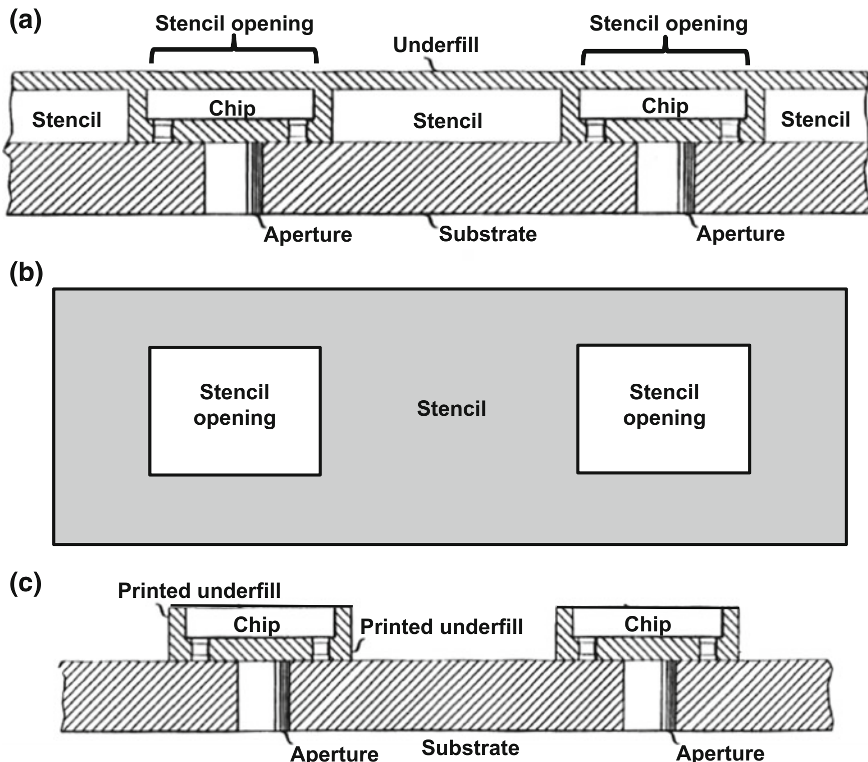


Fig. 2.19 **a** Lucent Technologies' stencil printing of underfill. **b** Stencil openings. **c** Printed underfill

(3) the substrates must have an aperture [135] to let the underfill to flow out. The drawbacks of [135] are (1) lots of underfills are wasted due to the very large opening of the stencil and the flow out of underfill from the aperture of the substrate; (2) there is a very good chance to damage the chip due the very large opening of the stencil (to expose the entire backside of the chip) and the stencil thickness is not taller than the backside of the chip (thus all the squeegee pressure is applied to the backside of the chip) during printing; and (3) an aperture in the substrate is not practical because it is not only affecting the routing but also increasing cost and the size of the substrate.

In the present investigation [136], a new stencil will be designed for printing the underfill for flip chips on organic-panel and Si-wafer assemblies. The effects of the viscosity, thermal enhancement, and multiple prints of underfills will be examined. The cured assemblies will be characterized by the C-SAM, X-ray, shear test, cross-sectioning, and SEM methods.

2.6.3.1 A New Stencil Design

A new stencil designed for printing underfill for flip chips on organic-panel and Si-wafer assemblies is proposed in the present investigation and shown in Figs. 2.20, 2.21, and 2.22. It can be seen that (1) a very small rectangular opening of the stencil is designed for each chip and it is located on one edge of the chip; (2) the stencil is with a dry film underneath with many rectangular openings (one for each chip) and the size is a little larger than the chip size; (3) there is a gap between the stencil and the backside of the chips; and (4) there is a fixture to apply heat to the stencil and underfill to lower the underfill's viscosity as shown in Fig. 2.20. The size of the stencil opening and the thickness of the stencil and dry film determine the underfill volume which should be approximately equal to the space between the chip, solder joints, and the substrate plus the filet on the four sides of the chip.

During printing (Fig. 2.20b), the underfill will fill the opening of the stencil and fall into the space between one edge of the chip and the dry film. After printing (usually, it only takes a few seconds), remove the assembly (Fig. 2.20c) from the stencil printer and place it on a hot plate (~120 °C) for the underfill to flow between the chip, solder joints, and the substrate by capillary action (Fig. 2.20d). Finally, cure the underfill.

Comparing the present stencil design with that of Luncet Technologies, the advantages are (1) for a given chip size, solder joint size, and standoff height, the opening and thickness of the stencil and dry film can be estimated and there will not be any waste of the underfill material; (2) because of the dry film underneath the stencil and the gap between the stencil and the backside of the chip, the chance of damaging the chip is very slim; (3) with the aid of heat, the underfill is easier to be printed and the printed underfill on one edge of the chip is more uniform, and the residue of underfill on the stencil is reduced; and (4) the throughput is higher than that of Lucent Technologies.

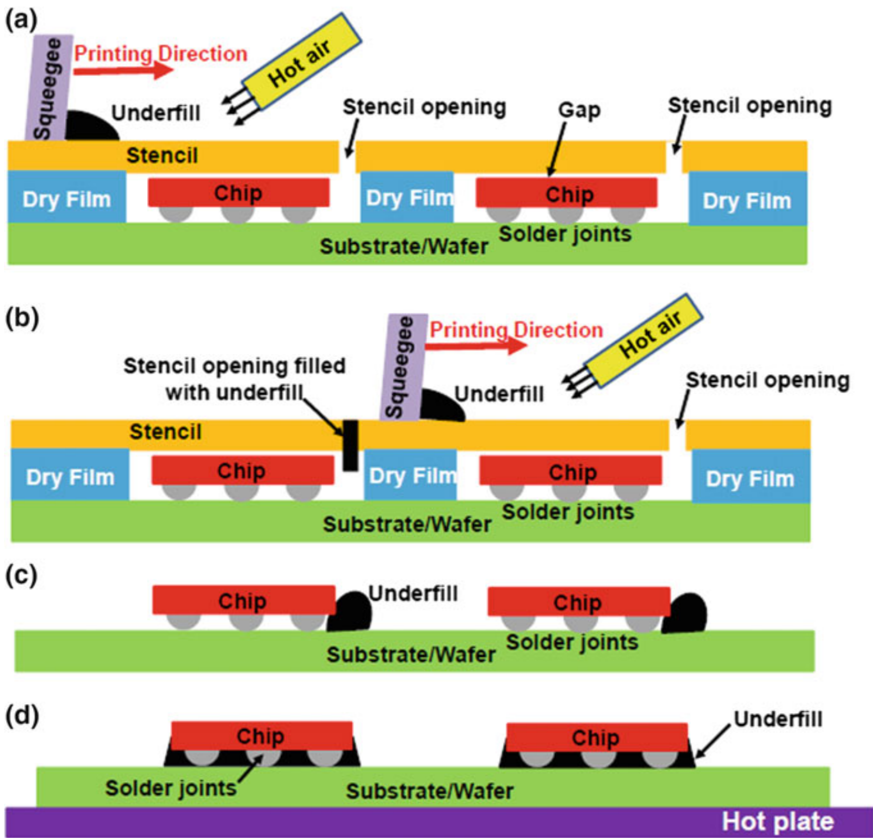


Fig. 2.20 **a** Before printing. **b** During printing. **c** After printing. **d** After capillary action. Hot air (optional)

2.6.3.2 Test Chip

In order to demonstrate the feasibility of the new stencil design for post-assembly underfill, test vehicles are built. The test chip for both organic-panel and Si-wafer assemblies is the same and shown in Fig. 2.23. It can be seen that the chip dimensions are 5 mm × 5 mm × 150 μm and there are 31 × 31 (961) Cu pillar + SnAg solder cap bumps, which are on 160 μm pitch. The diameter of the Cu pillar is 40 μm and its height is 25 μm, while the SnAg solder cap is 17 μm as shown in Fig. 2.23.

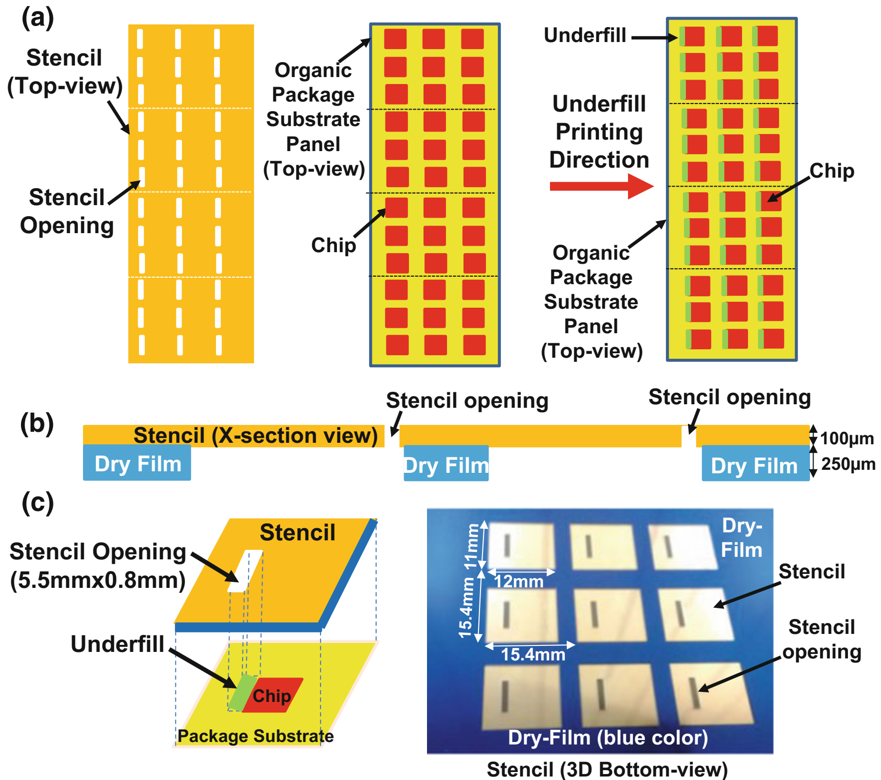


Fig. 2.21 Printing underfill for flip chips on organic substrate. **a** Top view. **b** X-sectional view. **c** 3-D view

2.6.3.3 Test Substrates

In this study, the test substrates for the flip chip assemblies are organic panel and Si wafer and shown, respectively, in Figs. 2.24 and 2.25. It can be seen that, for the organic-panel substrate (Fig. 2.24), the dimensions are 240 mm × 63 mm × 0.32 mm. There are 36 units and the dimensions for each unit are 15.4 mm × 15.4 mm × 0.32 mm. There are pads and traces on each chip site. The diameter of the OSP (organic solderability preservative) Cu pad is 80 µm and is on a 320 µm pitch. The trace (leads) width is 25 µm and will be bump-on-lead (BOL).

Figure 2.25 shows the 200 mm Si-wafer substrate. The dimensions of the chip site are 5 mm × 5 mm × 760 µm. There are 961 Cu pads and are on 160 µm pitch on each chip site. The pad diameter is 60 µm. Because the street (kerf) width between the chip sites on the wafer is too narrow (<160 µm) to place the underfill, every other chip site will be used.

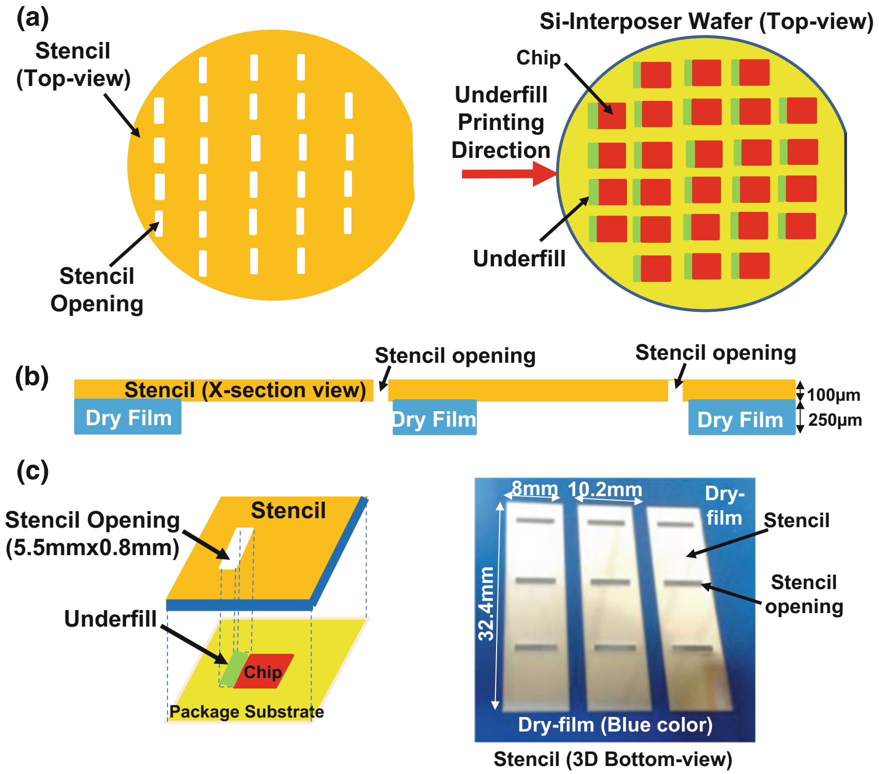


Fig. 2.22 Stencil printing of underfill for flip chips on Si substrate. **a** Top view. **b** X-section view. **c** 3-D view

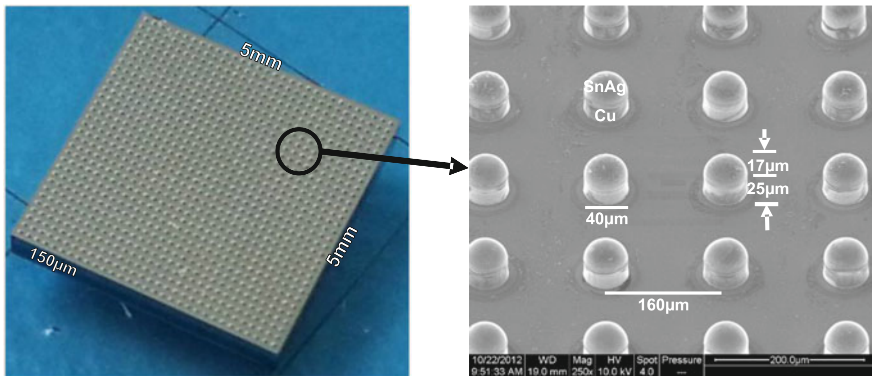


Fig. 2.23 Test chip with Cu pillar + SnAg solder cap

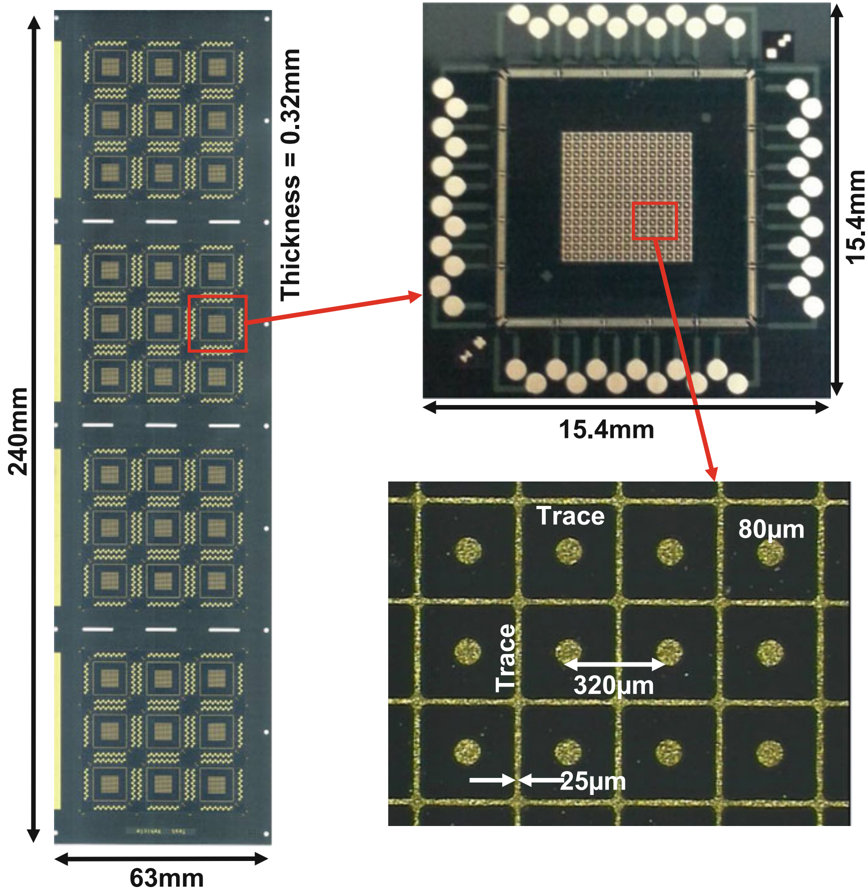


Fig. 2.24 Organic-panel substrate. The diameter of the OSP Cu pads is 80 μm on a 320 μm pitch. The trace width is 25 μm for BOL

2.6.3.4 Flip Chip Assemblies

The flip chips (Fig. 2.23) are dipped into flux, placed on the organic-panel or Si-wafer substrates, and then massed reflowed. The flux residues are cleaned by jetting water at 60 °C. The X-ray image of the flip chip assembly on organic-panel substrate is shown in Fig. 2.26a. It can be seen that there are two kinds of solder joints: one is BOP (bump-on-pad) and the other is BOL (bump-on-lead). The pitch of BOP is 320 μm and that of BOL is 160 μm. The X-ray image of the flip chip assembly on Si-wafer substrate is shown in Fig. 2.26b. It can be seen that the 40-μm-diameter Cu pillar on the chip is soldered on the 60-μm-diameter Cu pad on the substrate. They are on a 160 μm pitch.

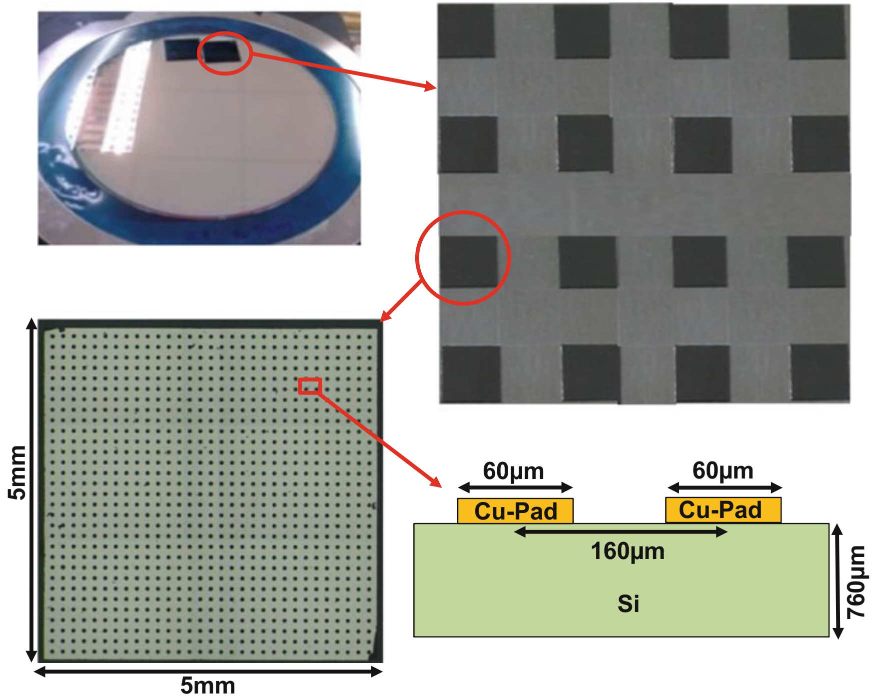


Fig. 2.25 Si-wafer substrate. The diameter of the Cu pad is 60 μm on a 160 μm pitch

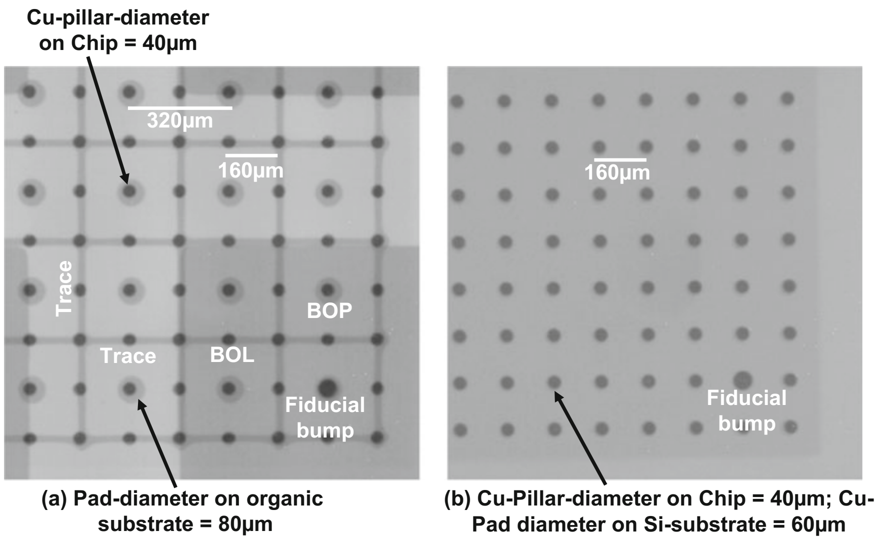


Fig. 2.26 X-ray images. **a** Flip chip assembly on organic substrate that includes BOLs and BOPs. **b** Flip chip assembly on Si substrate

2.6.3.5 Stencil Designs

The stencil designs for the test vehicles are shown in Fig. 2.21 for flip chips on organic-panel substrate and Fig. 2.22 for flip chips on Si-wafer substrate. For both cases, the stencil thickness is 100 μm and the opening is 5.5 mm × 0.8 mm. The dry film thickness underneath the stencil is 250 μm. For the case with organic-panel substrate, the dry film opening underneath the stencil is 11 mm × 12 mm (Fig. 2.21). For the case of Si-wafer substrate, the dry film opening underneath the stencil is 8 mm × 32.4 mm as shown in Fig. 2.22. The dry film (photoresist) is laminated on the stencil with a heater roller (∼125 °C). The opening of the dry film is by UV (ultraviolet) exposure machine and chemical solution.

2.6.3.6 Test Matrix

The test matrix, baking of assemblies, printing process, underfill capillary action, and curing will be briefly mentioned. Three different underfill materials are considered in this study. Their viscosities are Material #1 = 34 Pa.s (RT), Material #2 = 68 Pa.s (RT), and Material #3 = 15000 Pa.s (RT) and are shown in Fig. 2.27. For underfill Materials #3, since the viscosity is so high that the squeegee of stencil hardly moves (even with 60 °C thermal enhancement), it will not be considered for the rest of the studies.

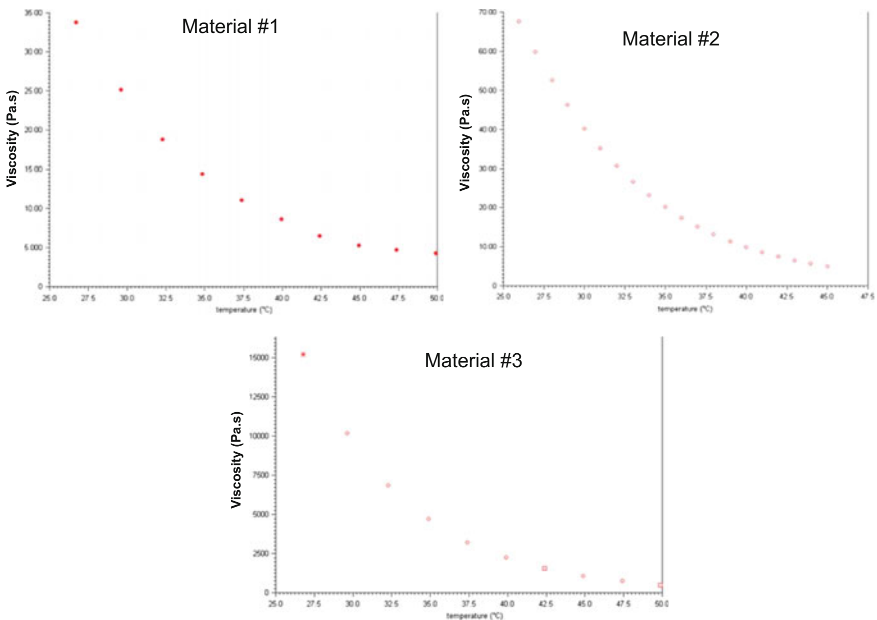


Fig. 2.27 Viscosity versus temperature for underfill materials #1–#3

Table 2.2 Test matrix for stencil printing of underfills for flip chip assemblies

Parameters	Test structures															
	Chip on organic panel								Chip on Si wafer							
Underfills (Pa.s) (Viscosity at 25 °C)	34 Material #1				68 Material #2				34 Material #1				68 Material #2			
Multiple print (times)	1		10		1		10		1		10		1		10	
Thermal enhanced (°C)	25 No	45	25 No	45	25 No	45	25 No	45	25 No	45	25 No	45	25 No	45	25 No	45

The test matrix is shown in Table 2.2. It can be seen that (1) there are two different substrates (organic panel and Si wafer); (2) for each substrate, there are two difference underfill materials (#1 and #2); (3) for each underfill, there are two different print numbers (1 time and 10 times); and (4) for each time, there are two different temperature environments (RT and 45 °C).

2.6.3.7 Baking Substrates

The underfill process begins by baking the organic- and Si-substrate flip chip assemblies. The baking conditions are at 120 °C for 60 min (on a hot plate). This step is critical for voidless underfill. Otherwise, the entrapped moisture in the assemblies will create voids in the underfill as shown in the C-SAM image, Fig. 2.28.

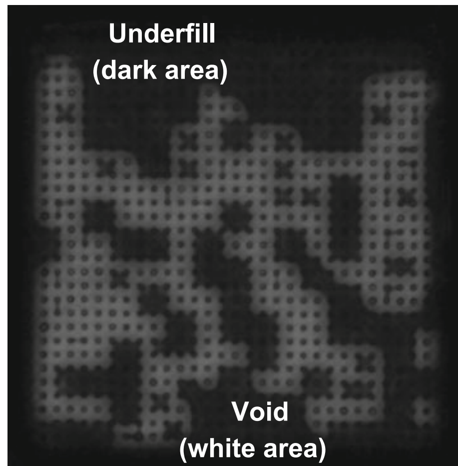


Fig. 2.28 Voids in underfill sample without baking of the assembly

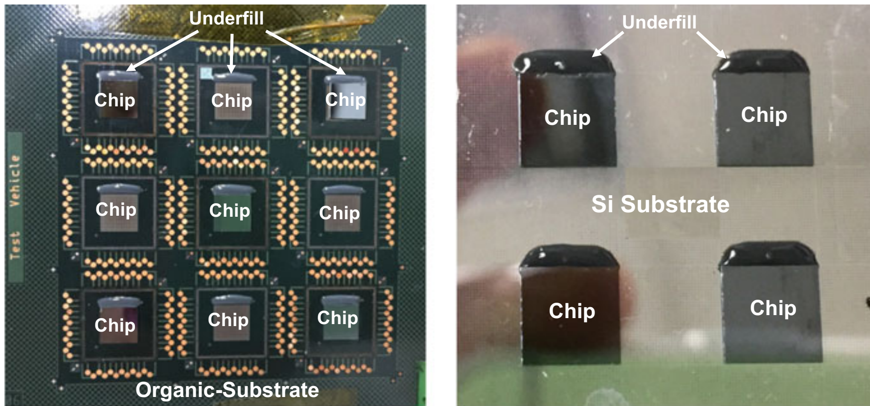


Fig. 2.29 Stencil printing of underfill on organic-panel substrate (left) and Si-wafer substrate (right)

2.6.3.8 Printing Process

After baking, the flip chip assemblies are loaded in a stencil printer (DEK). The underfill is placed on the stencil. The printing speed is between 150 and 290 mm/s, the printing force is 8 kg, and the snap-off height is zero. The printing patterns are quite uniform as shown in Figs. 2.29L for organic substrate and Fig. 2.29R for Si substrate.

2.6.3.9 Capillary Action and Curing

The printed underfill flip chip assemblies are placed on a hot plate with 120 °C. The underfill will flow underneath the chip and fill the space between the chip, solder joints, and substrate by capillary action. After the underfill come out from the other edges of the chip, then cure the underfill.

2.6.3.10 Effects of Underfill Viscosity, Thermal Enhancement, and Multiple Prints

The experimental samples are characterized by C-Mode SAM, X-ray, cross section, shear test, and SEM methods. The experimental results are shown in Table 2.3. It can be seen that there is not significant effect on multiple prints. For both underfills #1 and #2 (with and without thermal enhancement), there are only three chips that have voids and all the others are voidless. Figure 2.30 shows a flip chip assembly that has voids, which are due to the flux residues from the cleaning process. Typical C-Mode SAM images are shown in Fig. 2.31. Figure 2.31 (Top) shows flip chips on Si-substrate assembly with underfill Material #1, while Fig. 2.31 (Bottom)

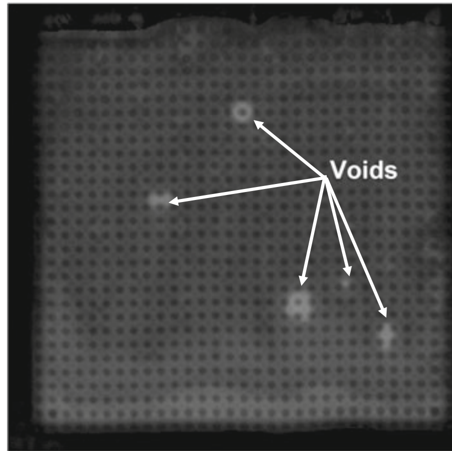


Fig. 2.30 C-mode SAM image of underfill flip chip assembly with voids

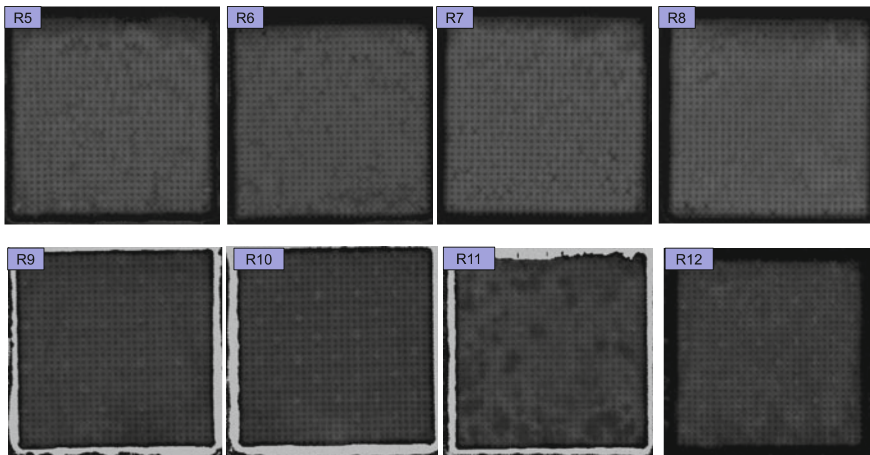


Fig. 2.31 Typical C-mode SAM. Top: flip chip on Si-substrate assemblies with underfill material #1. Bottom: flip chip on organic substrate with underfill material #2

shows flip chips on organic substrate with Material #2. There is not any void in these assemblies.

The effect of thermal enhancement for stencil printing underfill is shown in Fig. 2.32. It can be seen that, for both underfill Materials #1 and #2: (1) there is very little underfill residue after stencil printing underfill at 45 °C, and (2) there are lots underfill residue after stencil printing underfill at RT (no thermal enhancement).

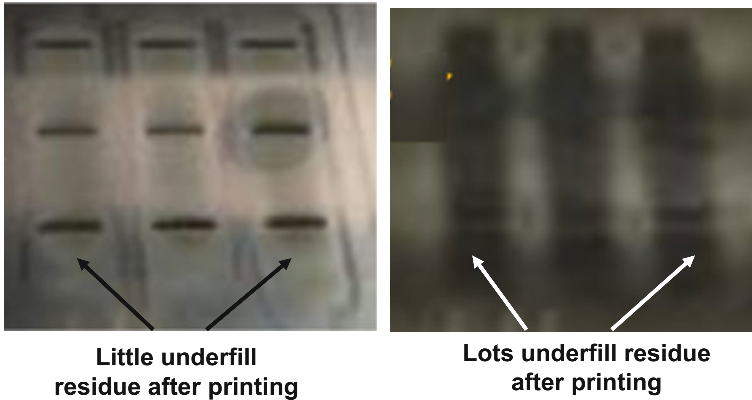


Fig. 2.32 Left: stencil printing underfill at 45 °C. Right: stencil printing underfill at RT

2.6.3.11 Cross Sections

Figure 2.33 shows a typical cross section of the stencil-printed underfill for flip chip on organic-panel assemblies. It can be seen that (1) the underfill filets on the edges of the chip are clearly shown; (2) the underfill between the chip, solder joints, and substrate has no void and is properly processed; and (3) the solder joints on Cu pad (BOP) and lead (BOL) of the organic substrate look very good.

Figure 2.34 shows a typical cross section of stencil-printed underfill for flip chip on Si-wafer assemblies. It can be seen that (1) the underfill filets on the edges of the chip are clearly shown; (2) the underfill between the chip, solder joints, and substrate has no void and is properly processed; and (3) the solder joints with 40-μm-diameter Cu pillar of the chip on 60-μm-diameter Cu pad of the Si substrate look good.

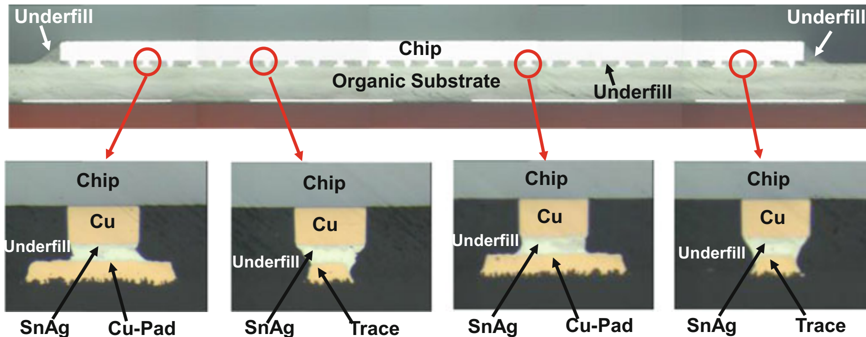


Fig. 2.33 Typical cross section of stencil-printed underfill for flip chip on organic-panel assembly

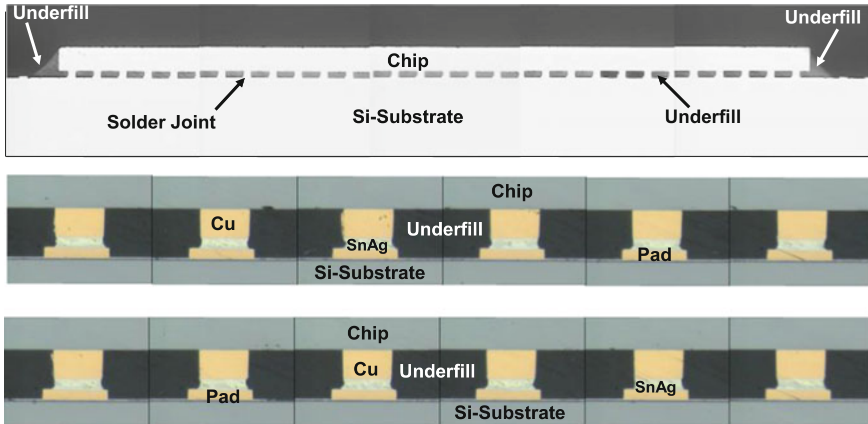


Fig. 2.34 Typical cross section of the stencil-printed underfill for flip chip on Si-wafer assembly

2.6.3.12 Underfill Filler Density

Figure 2.35 shows a flip chip assembly with voidless underfill. It is observed that even there is no void; however, there are darker spots. For example, it is slightly darker between solder joints 7 and 8 than between solder joints 8 and 9 on the cross section shown in the top portion of Fig. 2.35. The SEM images show that the silica fillers between solder joints 7 and 8 are denser than those between solder joints 8 and 9.

2.6.3.13 Shearing Test

The stencil-printed underfill flip chip assemblies are subjected to shearing test. The tip of the shear blade is placed at 30 μm from the substrate surface (near to the bottom of the flip chip). The maximum shear force of the tester is set at 60 kg. Some of the test results are shown in Table 2.3 and Fig. 2.36. It can be seen that many samples passed 60 kg and have no failure. For the failed samples, the failure mode is chip fracture (cracking) and there is not any underfill failure. For some of the flip chip on Si-substrate assemblies, not only the chip fracture but also cracking of the Si substrate as shown in Fig. 2.36. This shows the toughness of the underfill (Fig. 2.36; Table 2.3).

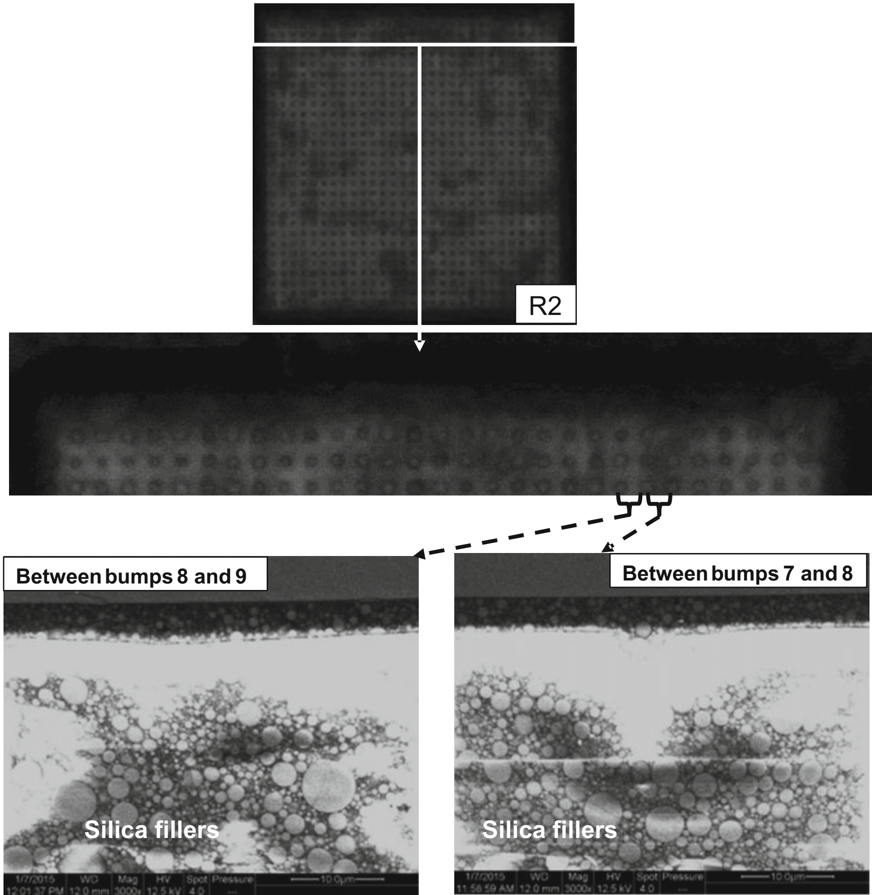


Fig. 2.35 Top: flip chip assembly with voidless underfill but with darker spots. Bottom: SEM images showing the distribution of underfill silica fillers

2.7 Preassembly Underfill

For preassembly underfill, the application of underfill is either on the substrate or wafer and is before the flip chip assembly. Solder reflow of the C4 bumps with underfill on substrates was first proposed by GIT [137] and is called NUF. High bonding force TCB of the C2 bumps with nonconductive paste (TC-NCP) underfill on the substrate, Fig. 2.16c, was first studied by Amkor [138] and has been used to assemble Qualcomm's SNAPDRAGON application processor for Samsung's Galaxy smartphone as shown in Fig. 2.37. The NUF and NCP underfills can be spun on, dispensed by a needle, or vacuum assisted.

By learning from the chip-on-glass technology, high-bonding force TCB of C2 bumps with nonconductive film (NCF) underfill on wafers have been studied by,

Table 2.3 Experimental results

		Runs	Temperature (°C)	Multiple prints	Voids (Y/N)	Die shear force (kg)	Remark
Underfill Material #1	Chip to organic substrate	R1	25	1	N (0/5)	>60	
		R2	25	10	N (0/5)	>60	
		R3	45	1	Y (2/4)	>60	
		R4	45	10	N (0/4)	53	Die crack
	Chip to Si substrate	R5	25	1	N (0/4)	57	Die crack
		R6	25	10	N (0/4)	45	Die crack
		R7	45	1	N (0/4)	43	Die/sub crack
		R8	45	10	N (0/4)	>60	
Underfill Material #2	Chip to organic substrate	R9	25	1	N (0/4)	>60	
		R10	25	10	N (0/5)	>60	
		R11	45	1	N (0/4)	39	Die crack
		R12	45	10	N (0/4)	>60	
	Chip to Si substrate	R13	25	1	Y (1/3)	>60	
		R14	25	10	N (0/4)	26	Die crack
		R15	45	1	N (0/3)	41	Die/sub crack
		R16	45	10	N (0/4)	45	Die crack

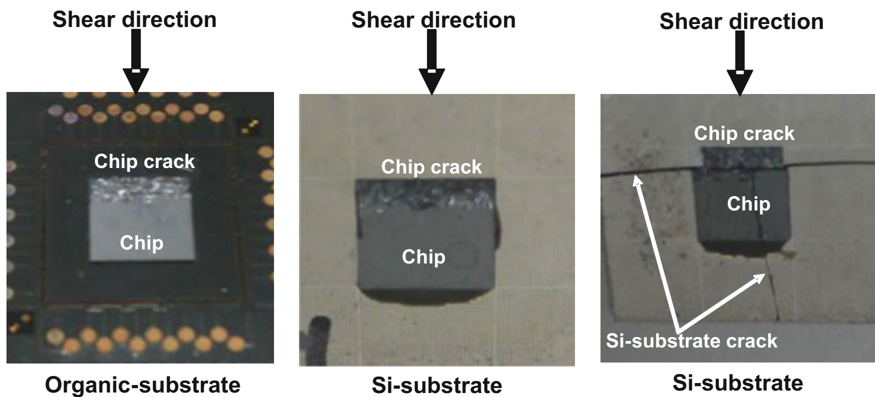


Fig. 2.36 Shearing tests and failure modes

e.g., Sanyo [139], Hitachi [140, 141], Tohoku [142, 143], DOW [144], Hynix [145], KAIST/Samsung [146, 147], Amkor/Qualcomm [148], and Toray [149–151] for 2.5D/3D IC integration [7–10]. Figure 2.38 shows the lamination of NCF on the Cu pillar with a solder cap-bumped wafer.

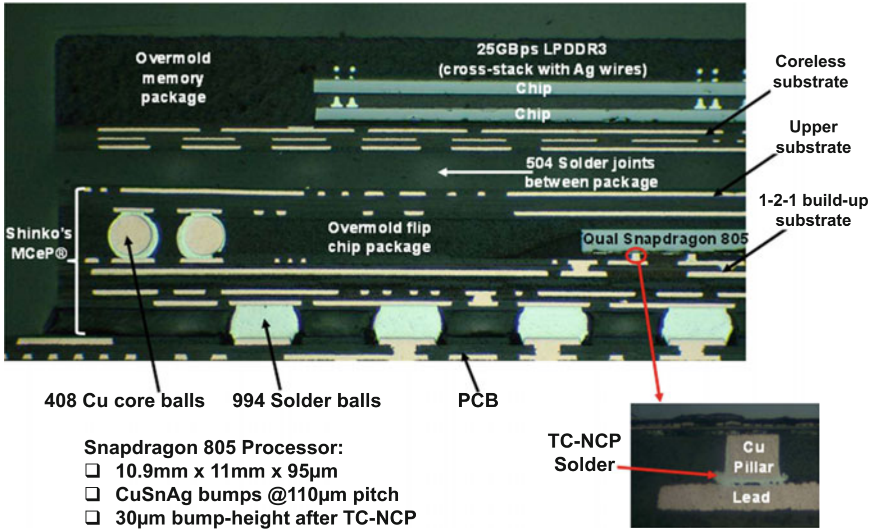


Fig. 2.37 PoP in Samsung's smartphone. The C2 flip chip is TCB with high force on a package substrate (TC-NCP)

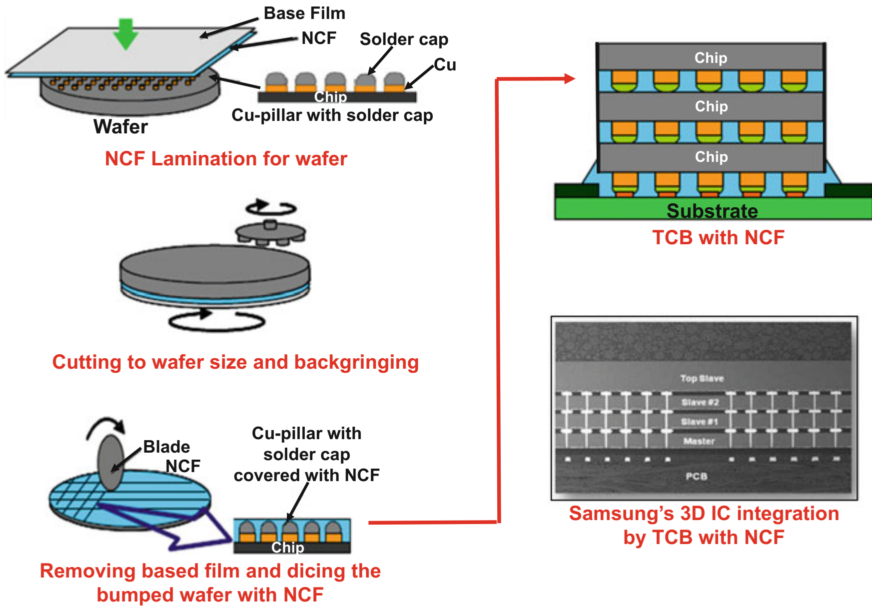


Fig. 2.38 Lamination of NCF on a C2-bumped wafer, dicing, and TCB of NCF flip chips one by one

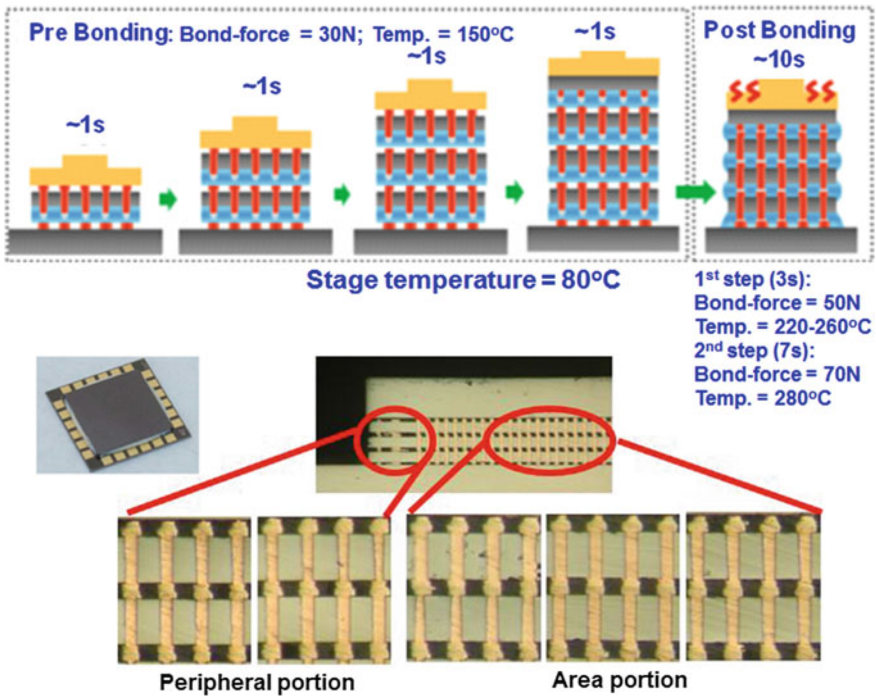


Fig. 2.39 Toray's collective TCB with high force with NCF flip chips

High bonding force TCB of the C2 chips with NCF (after singulation from the laminated wafer) has been in production for 3D IC integration by Samsung on its TSV-based double data rate type 4 dynamic random access memory (DRAM), Fig. 2.38, and by Hynix on the high bandwidth memory (HBM) of AMD's graphic processor unit (GPU) code named Fiji. This 3D memory cube is stacked by high-force TCB of the C2 chips with NCF one chip at a time and each chip takes ~10 s for the underfill film to gel, the solder to melt, the underfill film to cure, and the solder to solidify. Throughput is a problem!

In order to resolve this problem, Toray [150, 151] proposed a collective bonding method which is shown in Fig. 2.39. It can be seen that the C2 chip with NCF is prebond (bond force = 30 N, temperature = 150 °C, and time <1 s) on a stage with temperature = 80 °C. For postbond (first step (3 s): bond force = 50 N, temperature = 220–260 °C, second step (7 s): bond force = 70 N, temperature = 280 °C) on a stage temperature = 80 °C. Thus, instead of using 40 s in stacking up four chips by the conventional method, it only takes less than 14 s by the collective method. Some images of the cross section of the proposed collective bonding method are shown in Fig. 2.39. Reasonable good joints are achieved with optimized conditions.

In general, the spacing between the pillars on the C2 chip with either NCP or NCF by TCB with high bonding force can be as small as 10 μm.

2.8 Cu–Cu Direct Hybrid Bonding

Sony is the first to use Cu–Cu direct hybrid bonding (which bonds the metal pads and dielectric layer on both sides of the wafers at the same time) in high-volume manufacturing (HVM). Sony produced the IMX260 backside illuminated CMOS image sensor (BI-CIS) for the Samsung Galaxy S7, which shipped in 2016. Electrical test results [152] showed that their robust Cu–Cu direct hybrid bonding achieved remarkable connectivity and reliability. The performance of the image sensor was also super. A cross section of the IMX260 BI-CIS is shown in Fig. 2.40. It can be seen that, unlike in [153] for Sony's ISX014 stacked camera sensor, the TSVs are gone and the interconnects between the BI-CIS chip and the processor chip are achieved by Cu–Cu direct bonding. The signals are coming from the package substrate with wire bonds to the edges of the processor chip.

The assembly process of Cu–Cu direct hybrid bonding starts off with surface cleaning, metal oxide removal, and activation of SiO_2 or SiN (by wet cleaning and plasma activation) of wafers for the development of high bonding strength. Then, use optical alignment to place the wafers in contact at room temperature and in a typical cleanroom atmosphere. The first thermal annealing (100–150 °C) is designed to strengthen the bond between the SiO_2 and SiN surfaces of the wafers

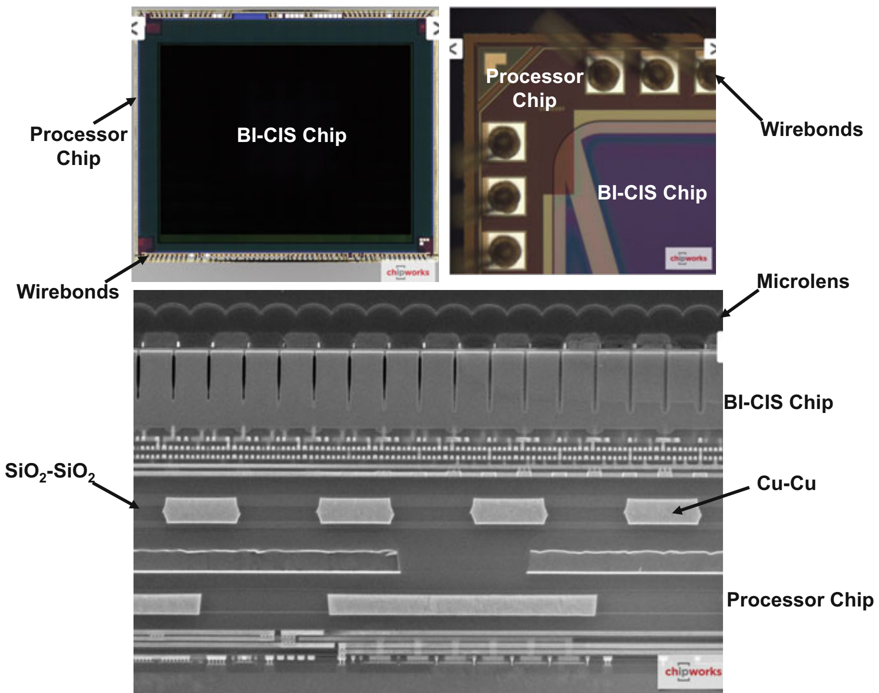


Fig. 2.40 Images of Sony's CIS by Cu–Cu hybrid bonding

while minimizing the stress in the interface due to the thermal expansion mismatch among the Si, Cu, and SiO_2 or SiN. Then, apply higher temperature and pressure (300 °C, 25 kN, 10–3 Torr, N2 atm) for 30 min to introduce the Cu diffusion at the interface and grain growth across the bond interface. The postbond annealing is 300 °C under N2 atm for 60 min. This process leads to the seamless bonds (Fig. 2.40) formed for both Cu and SiO_2 or SiN at the same time.

2.9 Flip Chip Technology Versus FOWLP

Flip chip technology is facing stiff competition. Some of its market share will be taken away by the fan-out wafer/panel-level packaging (FOW/PLP or simply FOWLP) technology [13, 14, 154]. Figure 2.41 shows the schematic and SEM (scanning electron microscope) images of the cross section of the PoP which houses the application processor (AP) and mobile dynamic random access memory (DRAM) of a production smartphone. This PoP is fabricated with the InFO (integrated fan-out) WLP technology [154]. It can be seen from the bottom package that the wafer bumping, fluxing, flip chip assembly, cleaning, underfill dispensing and curing, and build-up package substrate (of the AP shown in Fig. 2.17) have been eliminated and are replaced by the EMC and RDLs (for the AP as shown in Fig. 2.41). This results in a lower cost, higher performance, and lower profile

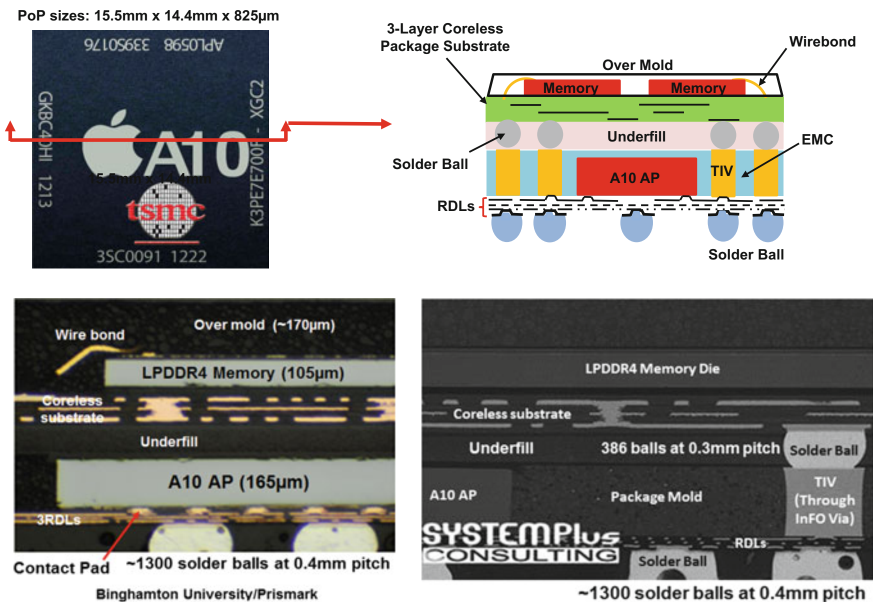


Fig. 2.41 Images of iPhone 7/7 + PoP A10 chipset FOWLP

package. This is very significant, since the smartphone company (Apple) and the component company (TSMC) developing these packages are the “sheep leaders”. Once they use it, then many others will follow. Also, this means that FOWLP is not just only for packaging baseband, RF (radio frequency) switch/transceiver, PMIC (power management integrated circuit), audio codec, MCU (micro-control unit), RF radar, connectivity ICs, etc., it can also be used for packaging high-performance and large (>120 mm^2) SoC such as APs.

2.10 Summary and Recommendations

Wafer bumping, package substrate, assembly, and underfill for flip chip technology have been investigated in this study. Some important results and recommendations are as follows:

- Flip chip technology came from a long way: from the three-bump flip chip to 10,000-bump flip chip, and could be 50,000-bump flip chip by the year of 2020. Also, by that time, the flip chip pitch could be as small as 30 μm as shown in Fig. 2.42 [155, 156].
- Flip chip technology is facing stiff competition and some of its market share will be taken away by the FOWLP technology.
- C2 bumps have better thermal and electrical performance and can go down to finer pitch (smaller spacing between pads) than C4 bumps. However, more research and development works should be done on relative performance characteristics, such as electromigration life, thermal fatigue life, signal speed, chip junction temperature, etc.

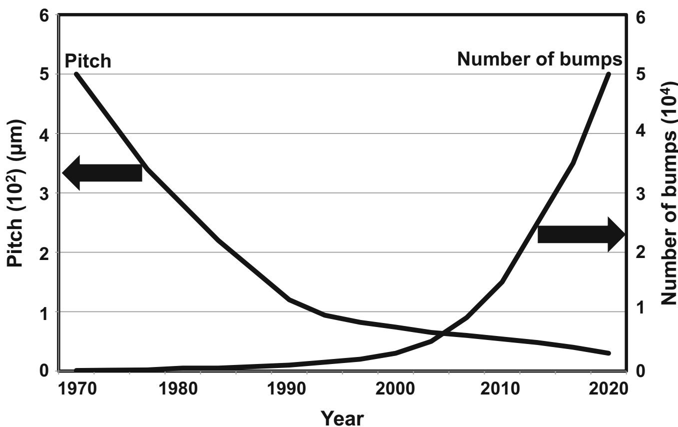


Fig. 2.42 Trend in flip chip bump and pitch

- The self-alignment characteristic (one of the most unique features of flip chip technology) of the C2 bumps is nowhere near the C4 bumps. Thus, mass reflow is usually applied to C4-bumped chips.
- C2-bumped chips are usually assembled by TCB with high force, while low force is sometimes used.
- The advantages of TCB are for higher pin count, finer pitch, thinner chips, higher density, thinner package substrates, and controlling warpage and die tilt. One of the drawbacks of TCB is throughput (compared with mass reflow).
- A package substrate with ten build-up layer (5-2-5) and 10 μm line width and spacing is more than adequate to support most of the flip chips.
- More research and development works should be done on innovative and low-cost ETS and coreless substrates for portable, mobile, wearable, and IoTs applications. More research and development works should be done to effectively use the BOL technique to increase routing density, and thus, lower the cost and reduce the size of organic package substrate.
- For Cu-to-Cu direct diffusion bonding, the spacing between pads is 5 μm or less.
- For mass reflow of C4-bumped chips with either CUF or MUF, the spacing between bumps is as low as 50 μm.
- For mass reflow of C2-bumped chips with either CUF or MUF, the spacing between Cu pillars is as low as 25 μm.
- For TCB with low force of C2-bumped chips with either CUF or MUF, the spacing between Cu pillars is as low as 8 μm.
- For TCB with high force of C2-bumped chips with either NCP or NCF underfills, the spacing between Cu pillars is as low as 10 μm.
- For the post-assembly underfill approach, the CUF or MUF is usually applied to flip chip assemblies with mass reflow and TCB with low bonding force methods.
- For the preassembly underfill approach, the NUF, NCP, or NCF is usually applied before flip chip assemblies; NUF is with mass reflow and NCP or NCF is with high-force TCB. In general, the NUF and NCP are applied on the substrate and the NCF is laminated onto the C2-bumped wafer and then diced into individual chips.
- Toray's collective TCB with high-force method can be a potential high-throughput process for stacking C2 chips with laminated NCF.
- Now that Sony has been in HVM with its BI-CIS with Cu–Cu hybrid bonding, in order to increase the throughput further for 3D IC integration, more research and development should be done on DRAM wafer stacking with Cu–Cu hybrid bonding.

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Chapter 3
Fan-in Wafer-Level Packaging Versus FOWLP

3.1 Introduction

Fan-in wafer-level packaging (WLP) technology [1–19] will be discussed in this chapter. A wafer-level chip scale package (WLCSP) will be designed and fabricated, and then assembled on a printed circuit board (PCB). Emphasis is placed on the key process steps in making the redistribution layer (RDL) of the WLCSP and its PCB solder joint reliability.

Unlike most of the solder joint reliability studies which are to generate enough test data to fit into a life distribution [20–28], one of the objectives of the present study is to determine the crack initiation and crack propagation in solder joints of the WLCSP on PCB assemblies. How does a crack grow (propagate) in WLCSP solder joints during thermal cycling? This is a frequently asked question, and the answer could be useful in designing the reliability of WLCSP solder joints. In this study, the crack length of a WLCSP solder joint is measured as a function of the number of thermal cycles, i.e., to determine experimentally the fatigue crack growth rate of WLCSP solder joints.

Empirical equations for predicting the thermal fatigue life of WLCSP solder joints are proposed that use the crack tip fracture characteristics, such as those shown in Sect. 3.10 (the solder is assumed to be an elastic material) for the stress intensity factors K_I (opening mode) and K_{II} (shearing mode), those shown in Sect. 3.10 (the solder is assumed to be an elasto-plastic material) for the J-integrals, and those shown in Sect. 3.10 (the solder is assumed to be a creep material) for the average creep strain energy density.

Because of die shirking, putting more functions on a die, and the popularity of system-in-package (SiP), fan-in WLP is facing stiff competition from fan-out wafer-level packaging (FOWLP) [29–53], which will be discussed in Chaps. 4, 5, 6, 7, 8, 9, and 11.

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3.2 Fan-in Wafer-Level Packaging (WLP)

Fan-in WLP has been used extensively in mobile, portable, and consumer products in the past 18 years. Specially, it is used for housing the semiconductor devices with low pin counts (≤ 200), small die size (≤ 6 mm $\times$ 6 mm), low-cost, low-end, low-profile, and high-volume applications.

3.3 Wafer-Level Chip Scale Packages (WLCSPs)

The packages made from the fan-in wafer-level packaging technology are called wafer-level chip scale packages (WLCSPs) [1–19]. The unique feature of most WLCSPs is the use of a metal (usually Cu) RDL to redistribute the fine-pitch peripheral-arrayed pads on the chips of a wafer to much larger pitch area-arrayed pads with much taller solder bumps as shown in Figs. 3.1 and 3.2. Thus, with WLCSPs, the demand on the PCB is relaxed and the underfill may not be necessary. From the system houses' point of view, WLCSPs are just like another "solder-bumped flip chip" surface-mount component, except for the following: (a) the solder bumps of WLCSP are much taller and bigger; (b) the PCB assembly of WLCSP is more robust; and (c) they are so happy that they do not have to struggle with the underfill encapsulant.

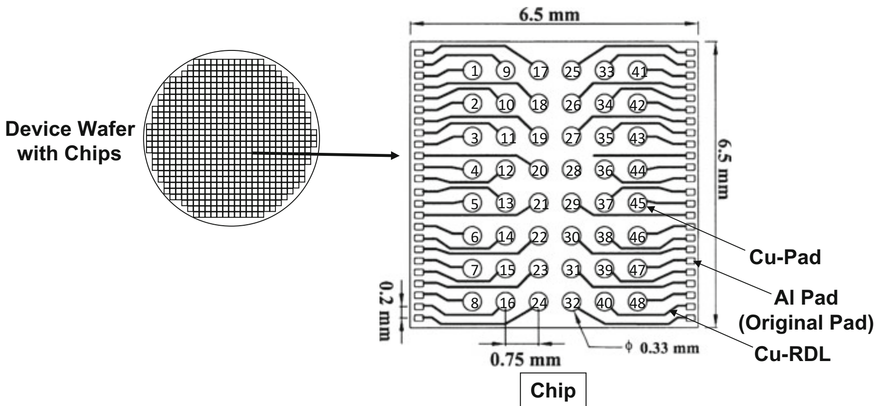

Fig. 3.1 Wafer-level chip scale package (WLCSP)

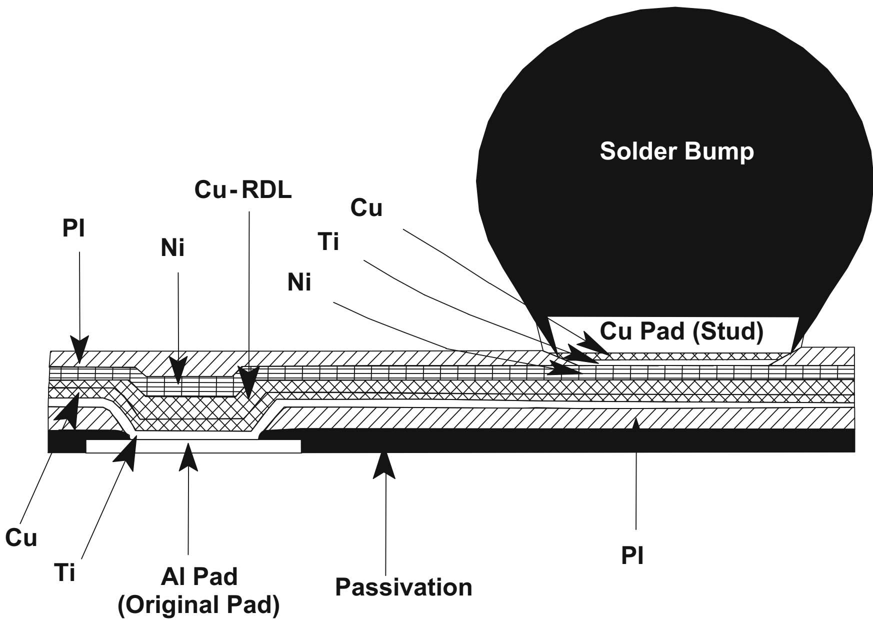

Fig. 3.2 RDL of WLCSP

3.4 WLCSP Test Vehicle

A WLCSP test vehicle is designed and fabricated, and then assembled on PCB to demonstrate its feasibility and reliability [2].

3.4.1 The Chip

Figure 3.1 shows the silicon chip on a wafer under consideration. This chip is 6.5 mm × 6.5 mm × 0.5 mm and has 48 pads (with 0.2 mm pitch) on two opposite sides.

3.4.2 The WLCSP

By adding an additional metal layer on top of the wafer, the fine-pitch peripheral-arrayed pads on the chip can be redistributed to a much larger pitch and area array pads in the interior of the chip. In this case, after wafer-level redistribution, the new pads (0.33 mm in diameter) are in area-arrayed format with 0.75 mm pitch.

The WLCSP consists of a copper conductor layer (RDL) and two low-cost polyimide dielectric layers. Figure 3.2 shows the details of redistribution. It can be seen that the solder bump is supported by a copper core, which is connected to the redistributed Cu–Ni pad through the Cu–Ti under-bump metallurgy (UBM). The redistributed metal layer is made of Cu–Ni.

3.4.3 WLCSP Key Process Steps

The key process steps of the WLCSP (Figs. 3.1 and 3.2) are briefly discussed as follows. First of all, the wafers are ultrasonic cleaned.

- Step 1: Spin the polymers such as polyimide (PI), benzocyclobutene (BCB), or polybenzo-bisoxazole (PBO) on the wafer and cure for 1 h. This will form a 4–7-μm-thick layer.
- Step 2: Apply photoresist and mask and then use photolithography techniques (align and expose) to open vias on top of the PI, BCB, or PBO.
- Step 3: Etch the PI, BCB, or PBO.
- Step 4: Strip off the photoresist.
- Step 5: Sputter Ti and Cu over the entire wafer.
- Step 6: Apply photoresist and mask and then use photolithography techniques to open the redistribution traces locations.
- Step 7: Electroplate Cu in photoresist openings.
- Step 8: Electroplate Ni.
- Step 9: Strip off the photoresist.
- Step 10: Etch off the Ti/Cu.
- Step 11: Same as Step 1 (for UBM).
- Step 12: Apply photoresist and mask and then use photolithography techniques to open vias on the photoresist for the desired bump pads and cover the redistribution traces.
- Step 13: Etch the PI, BCB, or PBO.
- Step 14: Strip off the photoresist.
- Step 15: Sputter Ti and Cu over the entire wafer.
- Step 16: Apply photoresist and mask and then use photolithography techniques to open the vias on the bump pads to expose the areas with UBM.
- Step 17: Electroplate the Cu core.
- Step 18: Electroplate solder.
- Step 19: Strip off the photoresist.
- Step 20: Etch off the Ti/Cu.
- Step 21: Apply flux and Reflow the 63Sn37Pb solder.

A typical cross section of the WLCSP bump is shown in Fig. 3.2. The solder bump height and Cu core height of the WLCSP are measured and the results are shown in Fig. 3.3. It can be seen that the Cu core height and the solder bump height

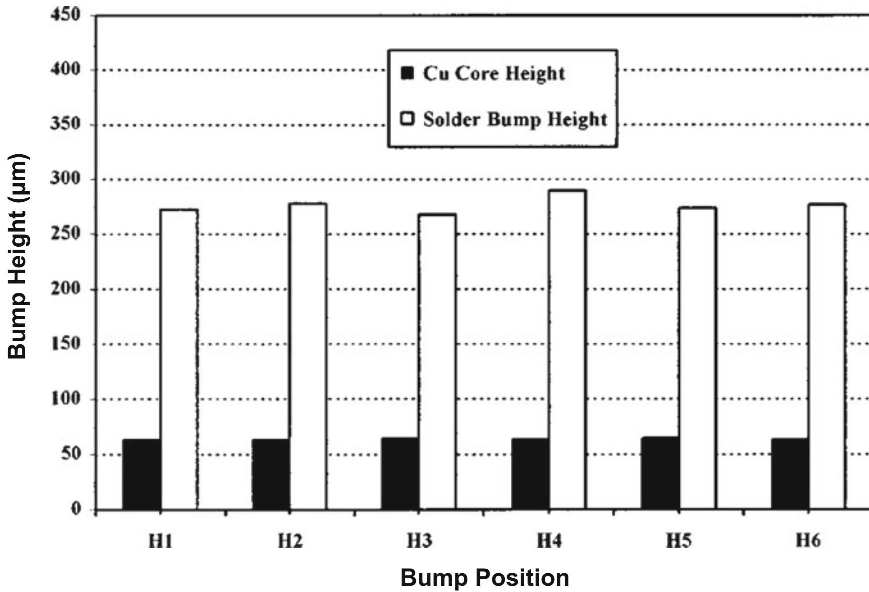

Fig. 3.3 WLCSP bump height and copper core height

are all very uniform. In this chapter, the solders on the chip before joining to the PCB are called solder bumps. After the solder bumps have been reflowed on the PCB, they are called solder joints.

The solder bumps of the WLCSP are subjected to shear test with the following conditions [20]: (1) shear blade speed is 100 μm/s, and (2) the tip of shear blade is 100 μm from the chip surface. The results are shown in Fig. 3.4. It can be seen that the averaged solder bump shear force is 404 gf, which is many times higher than that (50 gf) of the conventional flip chip solder bumps. It is noted that the failure location is in the solder bump (not at the UBM) and the fracture surface is shear dominated, Fig. 3.5.

3.5 PCB Assembly of the WLCSP

It is very easy to assemble the WLCSP on a 0.52-mm-thick FR-4 PCB. After the solder-bumped WLCSP is aligned with the PCB with lookup and lookdown cameras, then a no-clean flux is applied on the PCB, and finally the WLCSP is placed face-down on the PCB with a very minimal force. After the WLCSP is placed, it is put on the conveyor belt of a reflow oven with a maximum on PCB temperature of 235 °C (Fig. 3.6).

Due to the large amount of solder volume and the surface tension during solder reflow, the assembly process is very robust. A typical cross section of the

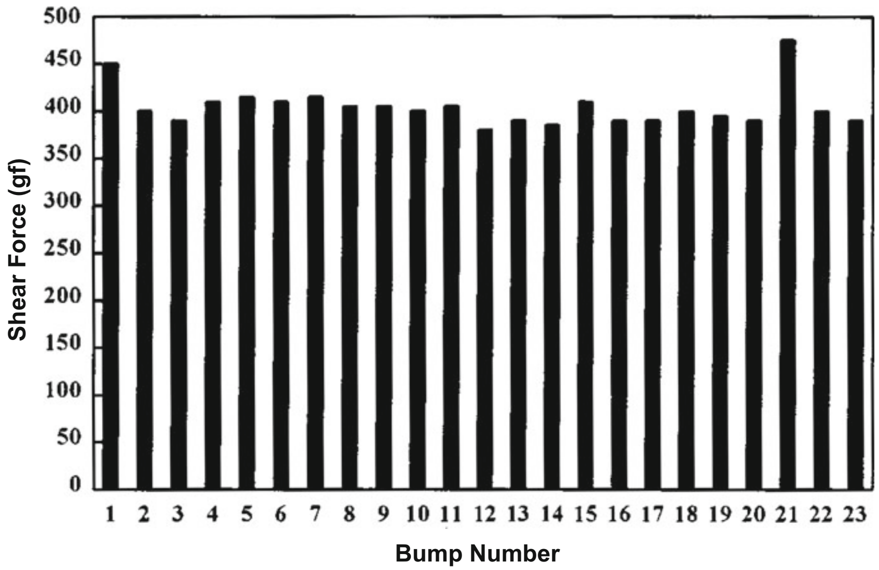

Fig. 3.4 Shear strength of WLCSP solder bumps

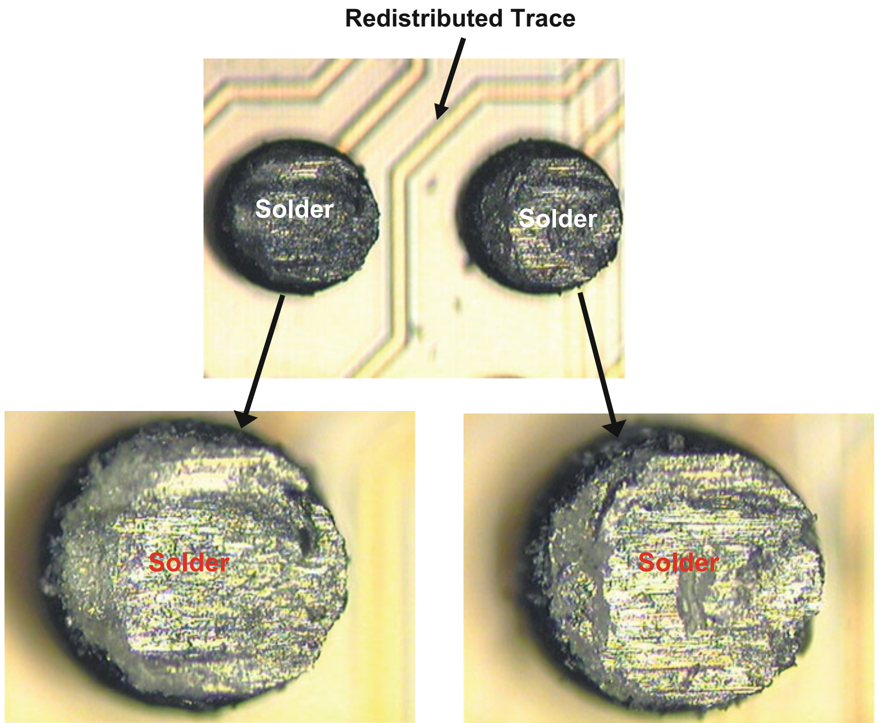

Fig. 3.5 Shear fracture surfaces of WLCSP solder bumps

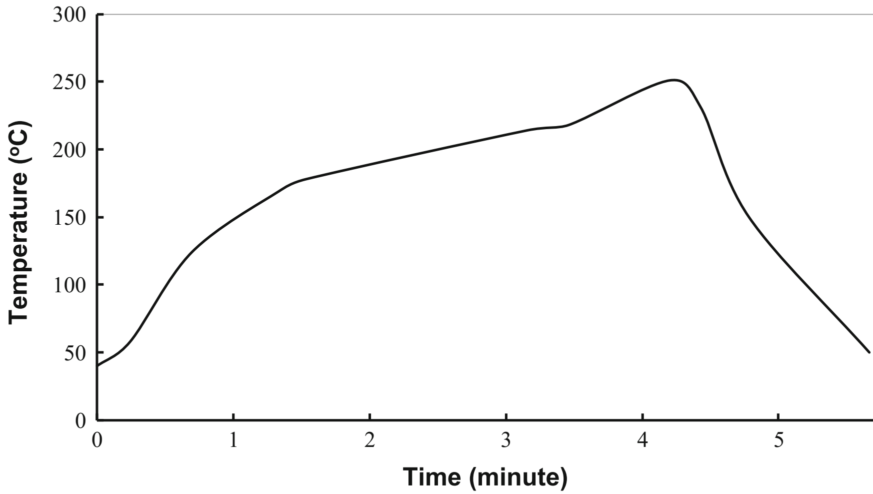

Fig. 3.6 SMT reflow profile

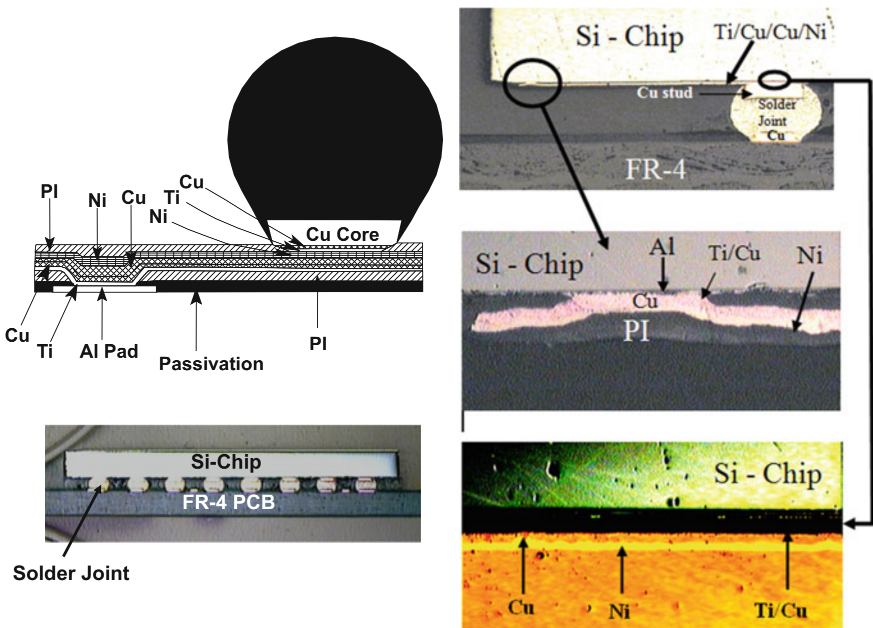

Fig. 3.7 WLCSP PCB assembly and cross-section image

WLCSP-PCB assembly is shown in Fig. 3.7, which clearly demonstrates the unique solder-bumped WLCSP self-alignment acteristics. Also, it clearly shows that the Cu/Ni RDL, Ti/Cu barrier/seed layer, and PI are properly done.

3.6 Thermal Cycling Test of WLCSP-PCB Assembly

3.6.1 Thermal Cycling Condition

The WLCSP on PCB assemblies is subjected to thermal cycling tests. The temperature loading imposed on the assemblies is shown in Fig. 3.8. It can be seen that for each cycle (60 min), the temperature is between −20 and +110 °C, with 15 min ramp, 20 min hold at hot, and 10 min hold at cold. There are two reasons for choosing this temperature profile: (1) the glass transition temperature of the FR-4 PCB is 120 °C and we do not want to introduce additional failure mechanisms of the solder joint due to the degradation of the PCB; and (2) the behavior of solder below −20 °C is not very well understood.

3.6.2 Crack Length Distribution of All Solder Joints

Because the solder joints' distance to neutral point (DNP) is not the same, the crack length of all the solder joints can be different. In general, the solder joint has the largest DNP that will lead to the largest crack length. Figure 3.9 shows the mapping of the crack lengths in the solder joints at 2400 cycles. Indeed, the outer crack lengths of the first-row solder joints (1, 9, 17, 25, 33, and 41) are larger than those of the second and third rows of the solder joints. Also, the corner solder joints have the largest crack length.

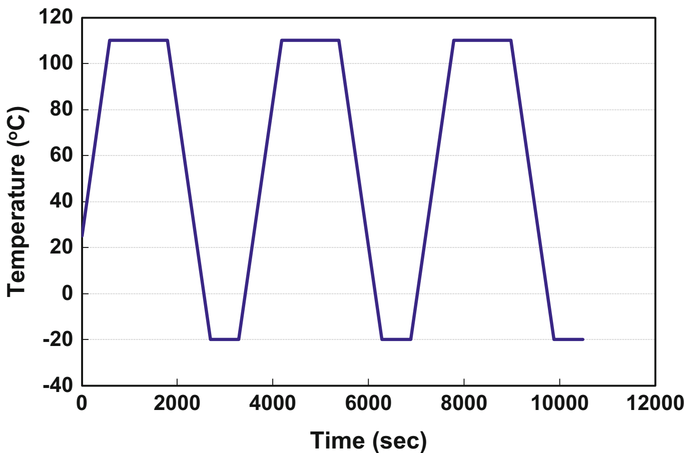

Fig. 3.8 Temperature profile for modeling and thermal cycling test

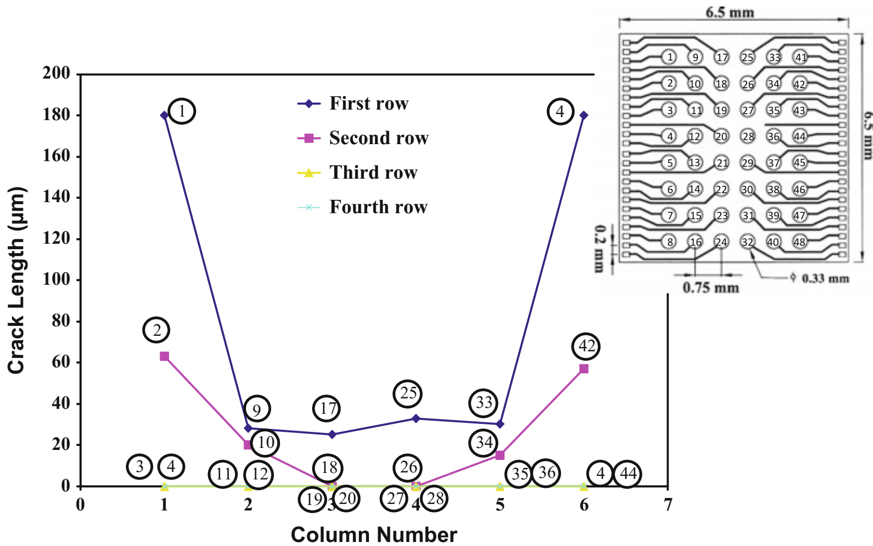

Fig. 3.9 Crack length distribution in solder joints of WLCSP assembly

3.6.3 Crack Propagation of the Corner Solder Joint

It should be pointed out that unlike most of the solder joint reliability studies which are to generate enough test data to fit into a life distribution [20–28], one of the objectives of the present study is to determine the crack initiation and crack propagation in solder joints of the WLCSP on PCB assemblies.

The initiation and propagation of cracks in any structures have always been a very complicated phenomenon. The initial crack length and crack growth length are also difficult to define. In this study, at 100, 200, 500, 800, 1000, 1200, 1500, 2000, and 2400 cycles, three of the WLCSP-PCB assemblies are taken out from the thermal cycling chamber for inspection. Cracks of the cross-sectioned samples are inspected under high-power microscope. Important results are summarized as follows [2, 14–18]:

(1) No obvious cracks in the solder joints up to 800 cycles (Fig. 3.10a and b). It should be pointed out that because of the small amount of sample size (3) and the power of the microscope, there could be some very small tiny cracks initiated much earlier.
(2) Between 800 and 1000 cycles, there are cracks on both sides of the corner solder joint. The inner crack length (toward the center of the chip) = 25 μm and the outer crack length = 40 μm, Fig. 3.10b. The outer crack initiated first as shown in Fig. 3.11b.
(3) Between 1000 and 1200 cycles, the inner crack length propagates to 37 μm while the outer crack length grows to 48 μm, Figs. 3.10c and 3.11c.

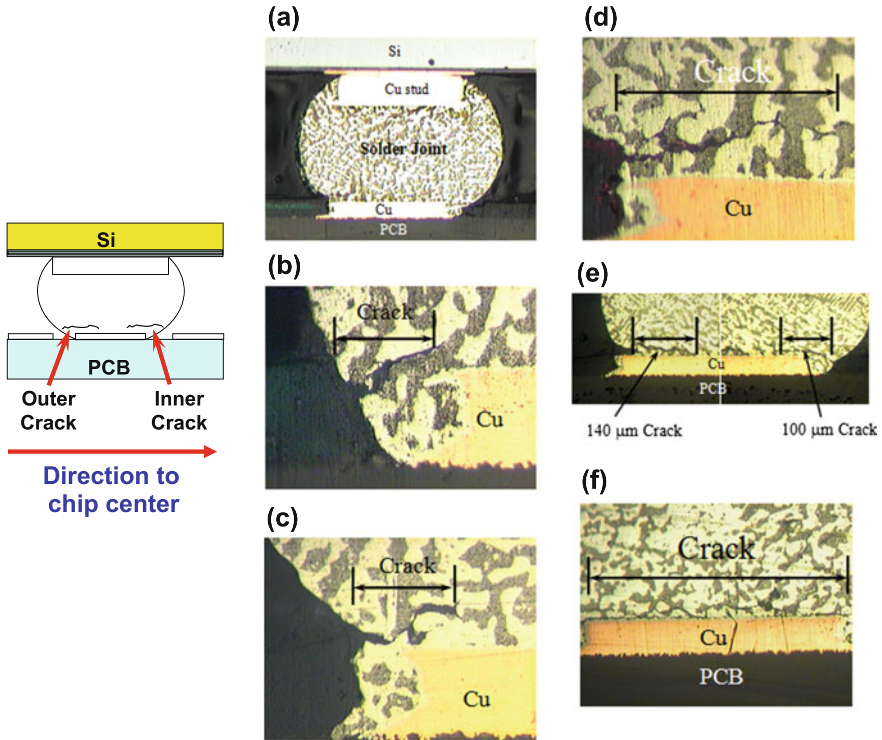

Fig. 3.10 Cross sections of the corner solder joint at different thermal cycles. **a** 800 cycles (no obvious cracks). **b** 1000 cycles with 40 μm crack (outer crack). **c** 1200 cycles with 48 μm crack (outer crack). **d** 1500 cycles with 100 μm crack (outer crack). **e** 2000 cycles with cracks from two edges. **f** 2400 cycles with crack passing through solder joint

(4) Between 1200 and 1500 cycles, the inner crack length = 70 μm and the outer crack length = 100 μm, Fig. 3.10d.
(5) Between 1500 and 2000 cycles, the inner crack length grows to 100 μm and the outer crack length grows to 140 μm, Fig. 3.10e.
(6) Between 2000 and 2400 cycles, the cracks separate the corner solder joint, Figs. 3.10f and 3.11d.
(7) In the corner solder joint, the cracks initiated and grew near the copper pad of the PCB.

3.6.4 Fatigue Crack Growth Rate

Figure 3.12 shows the inner and outer crack lengths of the corner solder joint as a function of the thermal cycling numbers. They can be curve-fitted, as shown in Fig. 3.13, into the following forms:

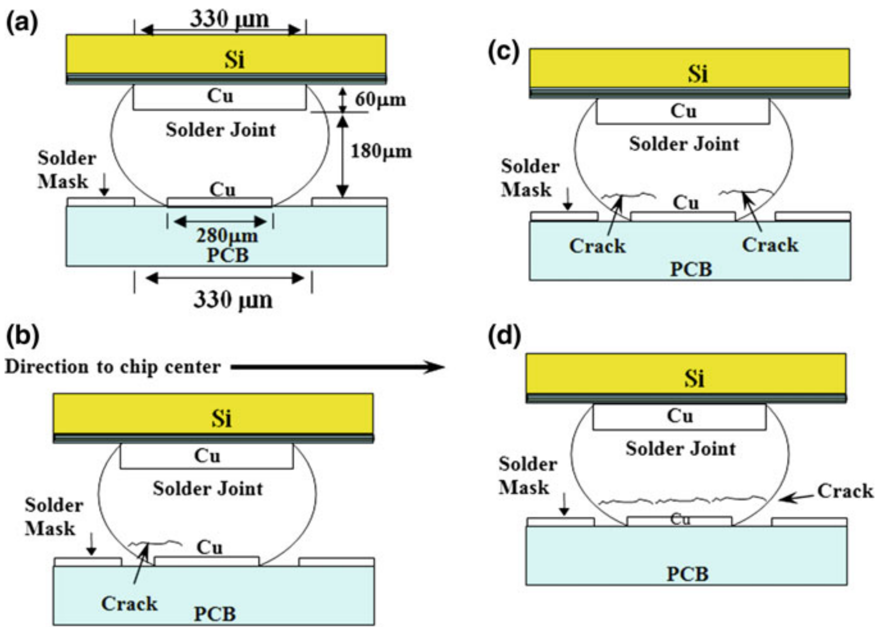

Fig. 3.11 Schematic of the corner solder joint at different stages. **a** No obvious crack when temperature cycles are less than 800. **b** Crack initiates from the outer edge. **c** Crack begins from the inner edge. **d** Cracks grow through the whole solder joint

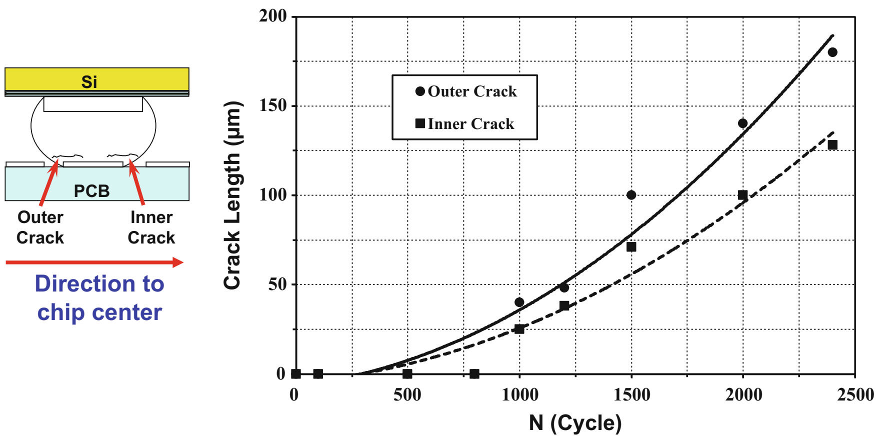

Fig. 3.12 Test results: crack length versus cycle numbers

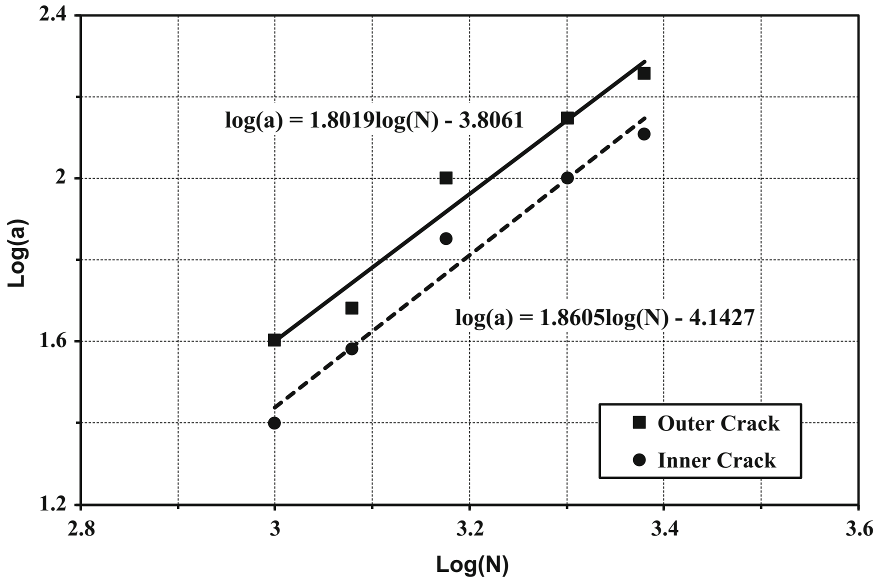

Fig. 3.13 Curve-fitting of crack length versus cycle numbers

$$\log(a) = C_1 \log(N) + C_2 \tag{3.1}$$

or

$$a = 10^{C_2} N^{C_1} \tag{3.2}$$

and

$$N = 10^{-C_2/C_1} a^{1/C_1} \tag{3.3}$$

Differentiating Eq. (3.2) with respect to N yields

$$\frac{\mathrm{d}a}{\mathrm{d}N} = C_1 10^{C_2} N^{(C_1 - 1)} \tag{3.4}$$

Substituting Eq. (3.3) into Eq. (3.4) gives

$$\frac{\mathrm{d}a}{\mathrm{d}N} = C_1 10^{C_2/C_1} a^{(C_1-1)/C_1}, \tag{3.5}$$

where a is the crack length, N is the number of cycles, and C_1 and C_2 are given in Table 3.1. Thus, for the corner solder joint, the length of outer and inner cracks can be determined by Eq. (3.2) for a given number of thermal cycles. Also, the fatigue crack growth rate (da/dN) of the corner solder joint can be obtained from Eq. (3.5).

Table 3.1 Curve-fitting constants: C_1, C_2, C_3, C_4

Curve-fitted	Location	C_1	C_2	C_3	C_4
Crack length versus cycles	Inner crack	1.86	−4.14	–	–
	Outer crack	1.80	−3.81	–	–
Stress intensity factor versus crack length	Inner crack	–	–	0.587	0.485
	Outer crack	–	–	0.610	0.520

3.7 Fracture Characteristics of the Corner Solder Joint—Solder Material and Properties

The solder joint is made of 63Sn–37Pb solder and has a Poisson's ratio of 0.4, and a coefficient of thermal expansion (CTE) of 21×10^{-6}/°C. The Young's modulus (Fig. 3.14) and the stress–strain relations (Fig. 3.15) of the solder are temperature dependent. The Young's modulus, Poisson's ratio, and CTE for copper (Cu) are, respectively, 76 GPa, 0.34, and 17×10^{-6}/°C. The CTE of FR-4 PCB is 18.5×10^{-6}/°C and that of Si WLCSP is 2.5×10^{-6}/°C. The material properties used in the computational modeling are shown in Table 3.2.

The Garofalo-Arrhenius steady-state creep is generally expressed as

$$\frac{\mathrm{d}\gamma}{\mathrm{d}t} = C\left(\frac{G}{\theta}\right)\left[\sin h\left(\omega\frac{\tau}{G}\right)\right]^n \exp\left(\frac{-Q}{k\theta}\right)$$

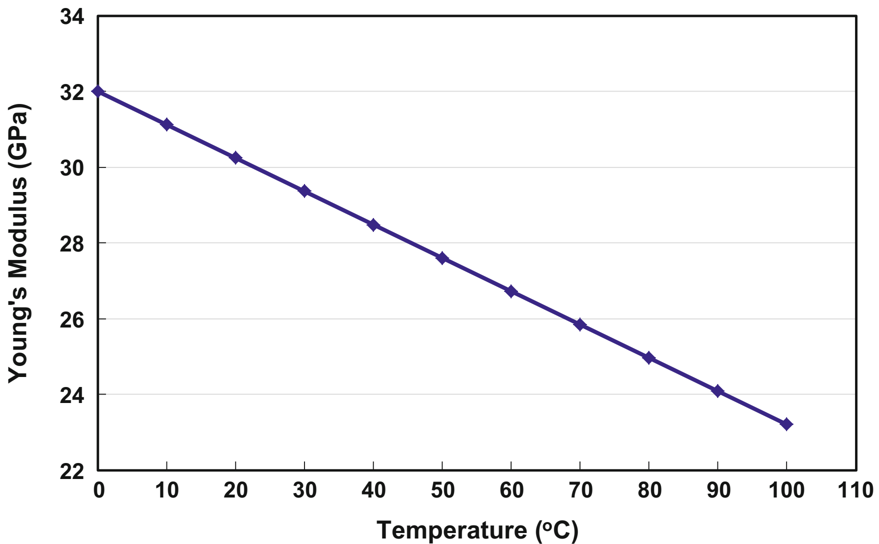

Fig. 3.14 Temperature-dependent young's modulus of solder

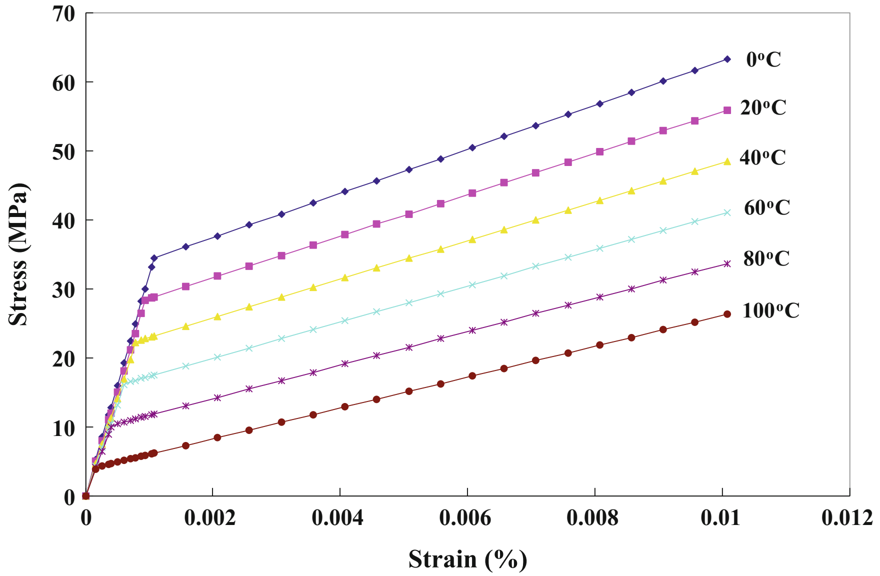

Fig. 3.15 Nonlinear temperature-dependent stress–strain relations of solder

Table 3.2 Material properties for modeling

Material properties	Young's modulus (GPa)	Poisson's ratio	Thermal expansion coefficient (10^{-6}/°C)
FR-4 PCB	22	0.28	18.5
63Sn–37Pb	Temp. Dep.	0.4	21
Polyimide	8.3	0.33	3
Silicon WLCSP	131	0.3	2.8
Solder mask	6.9	0.35	19
Ni	20.5	0.3	12.3
Cu	76	0.35	17

where

γ is the shear creep strain,
$d\gamma/dt$ is the shear creep strain rate,
t is the time,
C is a material constant,
G is the temperature-dependent shear modulus,
θ is the absolute temperature (K),
ω defines the stress level at which the power law stress dependence breaks down, τ is the shear stress,

n is the stress exponent,
Q is the activation energy for a specific diffusion mechanism, and
k is the Boltzmann's constant (8.617×10^{-5} eV/°K).

The Garofalo-Arrhenius creep equation can be rearranged by lumping certain coefficients and expressed as:

$$\frac{d\varepsilon}{dt} = C_1[\sin h(C_2\sigma)]^{C_3}\exp\left(-\frac{C_4}{T}\right)$$

where C_1, C_2, C_3, and C_4 are (not those Cs shown in Table 3.1) determined by creep test (curves) at various sets of constant stress and temperature. It should be noted that the last equation is exactly the same as the input form of the implicit creep model (TBOPT = 8) in ANSYS. In the equation, σ is the effective normal stress, and $d\varepsilon/dt$ is the effective normal creep strain rate. The unit for σ is MPa. For the present study, the creep constitutive equation for the 63Sn–37Pb is given by Lau [21]

$$\frac{d\varepsilon}{dt} = \frac{926(508 - T)}{T}\sin h^{3.3}\left(\frac{\sigma}{37.78 \times 10^6 - 74414T}\right)\exp\left(\frac{-6360}{T}\right)$$

The unit of σ is Pa and of T is °K.

3.8 Fracture Characteristics of the Corner Solder Joint—Geometry

Even though the initiation and propagation of the outer crack and the inner crack (toward to the chip center) of the corner solder joint are not exactly the same, however, for the sake of modeling simplicity, they are assumed to be equal. Figure 3.16 shows the corner solder joint for fracture mechanics finite element modeling. It can be seen that the solder joint is 0.24 mm tall and the diameters of the bottom and top surfaces are 0.28 and 0.3 mm, respectively.

Because of the WLCSP on PCB assembly's global thermal expansion mismatch ($3.2259 \times 130 \times [18.5 - 2.5] \times 10^{-6} = 0.0067$ mm) between the Si WLCSP and the FR-4 PCB, and the thermal expansion of the corner solder joint, the solder joint is subjected to a complex state of stress and strain during thermal cycling condition. These stresses and strains produce the driving force for solder joint failure. Since most of the thermal fatigue life of ductile materials such as solder is spent in propagating the crack (i.e., fatigue crack growth), the stresses and strains (stress intensity factors, J-integral, or creep strain energy density) around the crack tip of different crack lengths in the solder joint are of utmost interest.

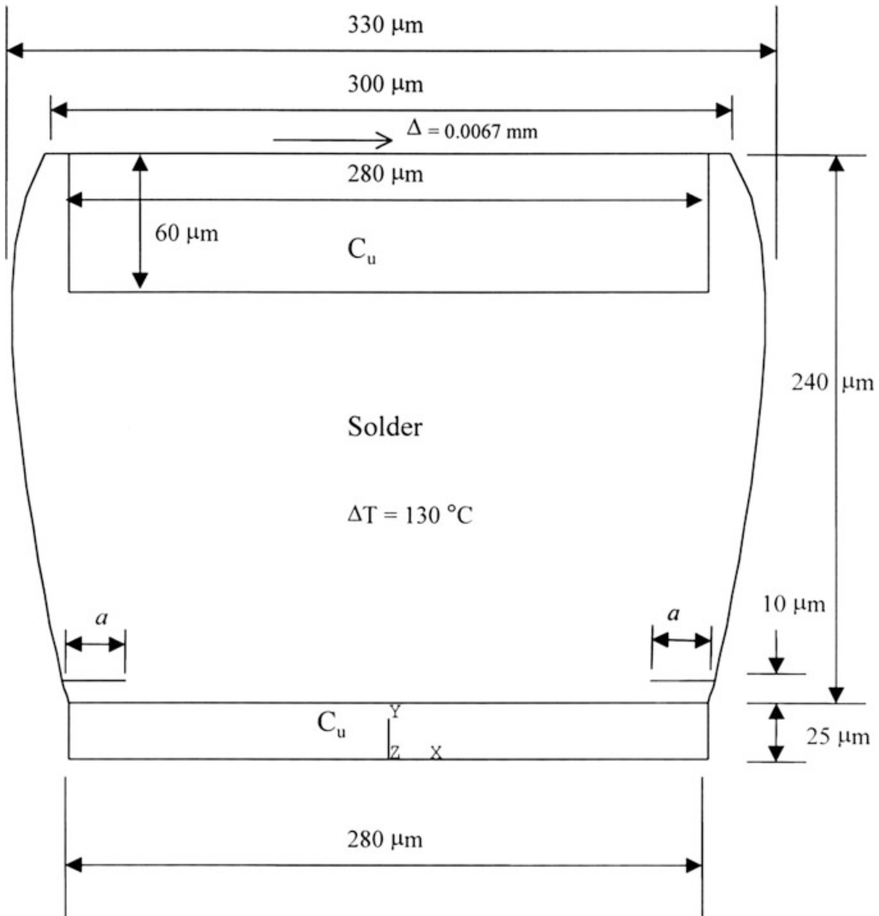

Fig. 3.16 Corner solder joint for modeling

3.9 Fracture Characteristics of the Corner Solder Joint—Elastic Thermal Fatigue Life Prediction Model (ΔK)

3.9.1 Boundary Value Problem

In this study [14], the solder (63Sn–37Pb) is assumed to be an elastic material and five different crack lengths are considered. These cracks are located symmetrically 10 μm above the copper pad on the PCB. The eight-node plain strain element is used in this study and the units are in Newton and mm. At the crack tip, the mid-side nodes are placed at the quarter points to capture the singularity in the stresses. Since most of the thermal fatigue life of ductile materials such as solder is spent in propagating the crack (i.e., fatigue crack growth), the stresses and strains

(stress intensity factor) around the crack tip of different crack lengths in the solder joint are of utmost interest.

The boundary conditions imposed on the corner solder joint are shown in Fig. 3.16, where the bottom surface is fixed, the top surface (nodes) of the solder joint is subjected to a 0.0067 mm displacement, and the whole solder joint is subjected to a temperature change of 130 °C. The top surface is also restrained from rotation by specifying nodal couplings of vertical displacement to those nodes so that the vertical displacements are the same.

With the prescribed loadings, the left crack in Fig. 3.16 is expected to pop open and the right crack should remain close. Instead of using contact elements, nodal couplings are conveniently used to simulate the closing and sliding of the right crack surfaces. In ANSYS (a commercial finite element code), the nodes on the right crack surfaces are nodal-coupled in the vertical direction at the coincident nodes, while free to slide in the horizontal direction. By using nodal couplings, there is no penetration of the crack surfaces when the crack is closed.

Figure 3.17a–e show the deformed (with finite element meshes) and un-deformed shapes of the corner solder joint with different crack lengths: 0.028, 0.056, 0.084, 0.112, and 0.133 mm. The typical von Mises stress contours around the crack tips (with a crack length = 0.112 mm) are shown in Fig. 3.18. It can be seen that, due to stress concentration (Fig. 3.18), the stresses at the crack tip are very large. The stress intensity factors ΔK_{I} (opening mode I) and ΔK_{II} (shearing mode II) at the inner and outer crack tips for different crack lengths of the corner solder joint are shown in Fig. 3.19. It can be seen that the fracture characteristics at the crack tips are dominated by shearing mode of fracture (due to the thermal expansion mismatch between the Si WLCSP and FR-4 PCB) especially at larger crack lengths.

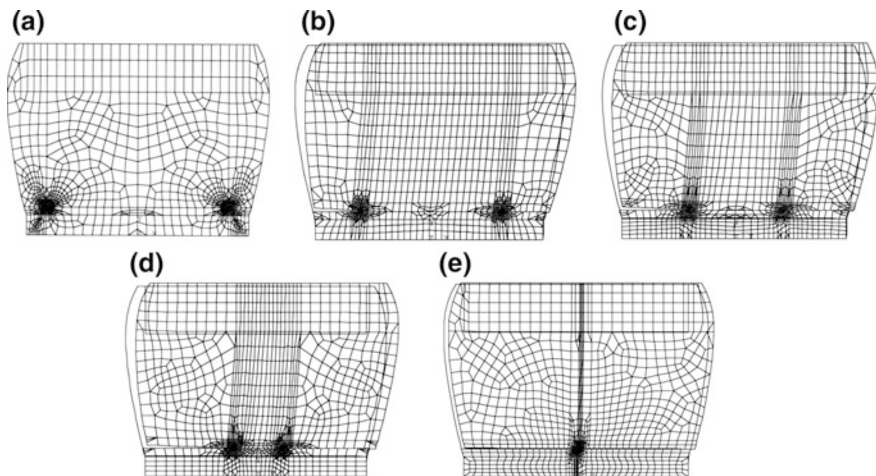

Fig. 3.17 Deformed shape of the corner solder joint. **a** Crack length = 0.028 mm. **b** Crack length = 0.056 mm. **c** Crack length = 0.084 mm. **d** Crack length = 0.112 mm. **e** Crack length = 0.133 mm

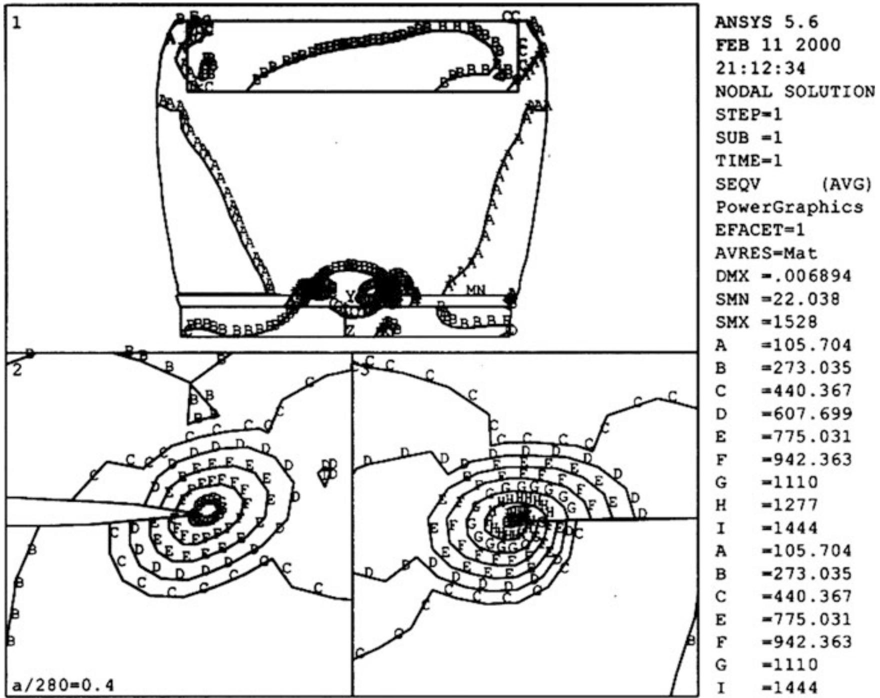

Fig. 3.18 Mises stress contour at the tip of outer (left) and inner (right) cracks (crack length = 0.112 mm)

3.9.2 Thermal Fatigue Life Prediction Model

Define the effective stress intensity factor range ΔK_{eff} as

$$\Delta K_{\mathrm{eff}} = \sqrt{\Delta K_{\mathrm{I}}^2 + \Delta K_{\mathrm{II}}^2} \tag{3.6}$$

The curves in Fig. 3.19 can be curve-fitted, as shown in Fig. 3.20 [only the middle three points are used since the crack initiation (near to the first point) is not very well defined and the solder joint fracture (near the fifth point) is not stable], into the following forms:

$$\log(\Delta K_{\mathrm{eff}}) = C_3 \log(a) + C_4 \tag{3.7}$$

or

$$a = 10^{-C_4/C_3} \Delta K_{\mathrm{eff}}^{1/C_3} \tag{3.8}$$

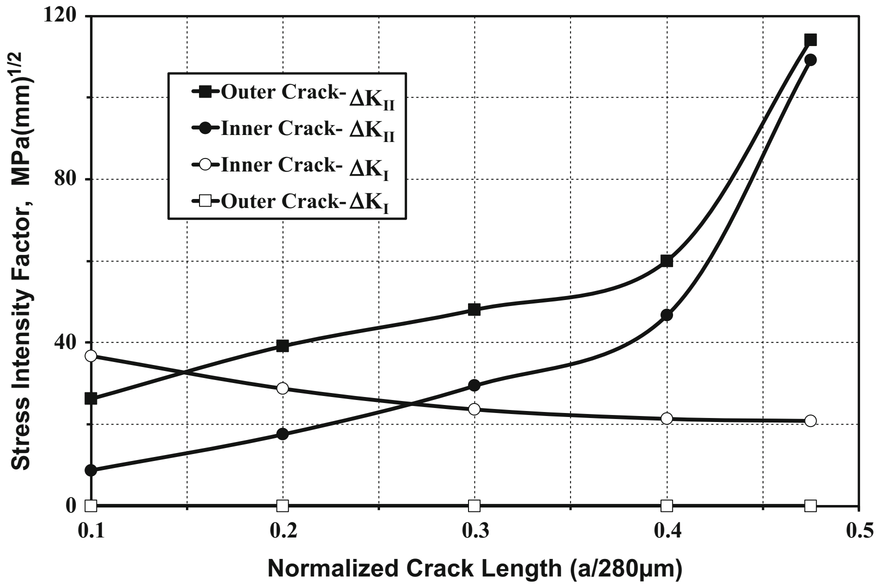

Fig. 3.19 Stress intensity factors range at the crack tip of different crack length in the corner solder joint

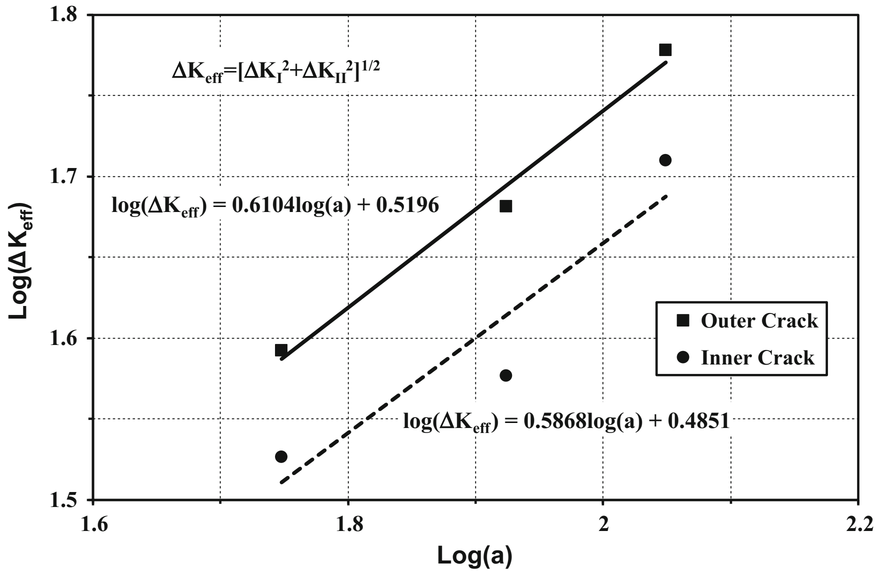

Fig. 3.20 Curve-fitting of the effective stress intensity factors range at the crack tip of different crack length in the corner solder joint

The constants C_3 and C_4 are given in Table 3.1. Substituting Eq. (3.8) into Eq. (3.5) yields

$$\frac{da}{dN} = C_1 10^{(C_2C_3 - C_1C_4 + C_4)/C_1C_3} \Delta K_{\mathrm{eff}}^{(C_1-1)/C_1C_3} \tag{3.9}$$

Thus, for the inner crack (Table 3.1), C_1 = 1.8606; C_2 = −4.1427; C_3 = 0.5868; C_4 = 0.4851, and Eq. (3.9) becomes

$$\frac{da}{dN} = 0.0046 \Delta K_{\mathrm{eff}}^{0.79} \tag{3.10}$$

For the outer crack (Table 3.1), C_1 = 1.8019; C_2 = −3.8061; C_3 = 0.6104; C_4 = 0.5196, and Eq. (3.9) becomes

$$\frac{da}{dN} = 0.0058 \Delta K_{\mathrm{eff}}^{0.73} \tag{3.11}$$

By averaging the coefficients of Eqs. (3.10) and (3.11), the thermal fatigue life prediction equation (in the form of Paris law) for flip chip solder joints can be expressed as

$$\frac{da}{dN} = 0.0052 \Delta K_{\mathrm{eff}}^{0.76} \tag{3.12}$$

Thus, for a given solder-bumped WLCSP assembly, once the effective stress intensity factor range ΔK_{eff} in terms of the crack length (a) is determined for a given temperature-cycling condition by computational modeling, the number of cycle to failure (N) can be estimated by Eq. (3.12).

3.9.3 Summary and Recommendations

Stress intensity factors at the crack tip of different crack lengths of the corner solder joint have been determined by fracture mechanics with the finite element method. Some important results are summarized as follows:

- In the present study, corner solder joint cracks initiate at two different locations, one near the chip center (inner crack) and the other on the opposite side (outer crack) of the solder joint. These cracks are right above the copper pad of the PCB.
- The outer crack of the corner solder joint initiates first and grows slightly larger than the inner crack at higher thermal cycles.
- In the present study, the outer and inner cracks of the corner solder joint meet between 2000 and 2400 cycles. This indicates that the present WLCSP on PCB

solder joints is reliable for use in most of the operating conditions even without underfill encapsulant.

- For the WLCSP on PCB under consideration, the crack length of the corner solder joint as a function of the number of thermal cycles has been measured and determined as shown in Eq. (3.2). Also, the thermal fatigue crack growth rate of the corner solder joint is given by Eq. (3.4) in terms of the number of thermal cycles or Eq. (3.5) in terms of the crack length.
- For the WLCSP on PCB under consideration, the effective stress intensity factor range at the crack tip as a function of the crack length of the corner solder joint has been determined and is given by Eq. (3.8). Also, the thermal fatigue crack growth rate in terms of the effective stress intensity factor range of the corner solder joint is given by Eq. (3.9).
- A new thermal fatigue life prediction model for flip chip solder joints is proposed as shown in Eq. (3.12).

3.10 Fracture Characteristics of the Corner Solder Joint—Plastic Thermal Fatigue Life Prediction Model (Δ*J*)

In this study [19], the solder (63Sn–37Pb) is assumed to be an elasto-plastic material and the Young's modulus (Fig. 3.13) and the stress–strain relations (Fig. 3.14) of the solder are temperature dependent. Since most of the thermal fatigue life of ductile materials such as solder is spent in propagating the crack (i.e., fatigue crack growth), the stresses and strains (*J*-integrals) around the crack tip of different crack lengths in the solder joint are of utmost interest.

In its simplest form, the *J*-integral is defined as a path-independent line integral that measures the strength of the singular stresses and strains near a crack tip (Fig. 3.21). The following equation shows an expression for *J* in its two-dimensional form. It assumes that the crack lies in the global Cartesian *X*–*Y* plane, with *X* parallel to the crack.

$$J = \int_{\Gamma} W \mathrm{d}y - \int_{\Gamma} \left(t_x \frac{\partial u_x}{\partial x} + t_y \frac{\partial u_y}{\partial x} \right) \mathrm{d}s, \tag{3.13}$$

where

Γ any path surrounding the crack tip
W strain energy density
t_x traction along x axis $= \sigma_x n_x + \sigma_{xy} n_y$
t_y traction along y axis $= \sigma_y n_y + \sigma_{xy} n_x$
σ stress component
n unit outward normal to path

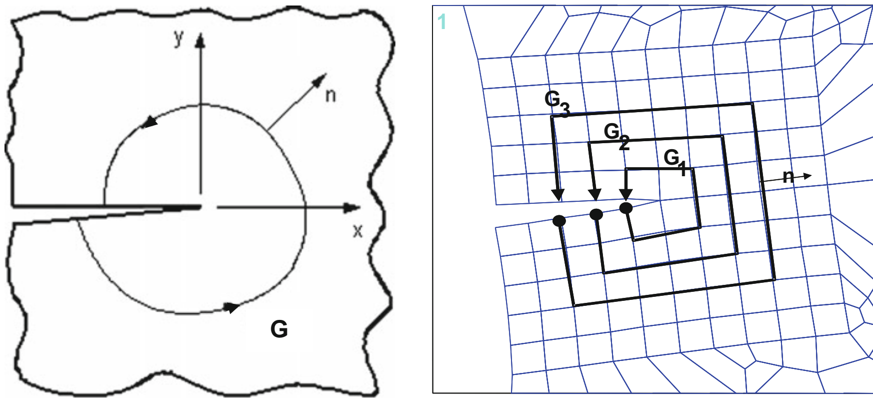

Fig. 3.21 *J*-integral contour path surrounding a crack tip

u displacement
s distance along the path

In this study, five different crack lengths are considered. These cracks are located symmetrically 10 μm above the copper pad on the PCB. The eight-node plain strain element is used in this study and the units are in Newton and mm. At the crack tip, the mid-side nodes are placed at the quarter points to capture the singularity in the stresses.

3.10.1 Boundary Condition and Results

The boundary conditions imposed on the corner solder joint are exactly the same as those in Sect. 3.9 (Fig. 3.16). Figure 3.22a–e show the deformed (with finite element meshes) and un-deformed shapes of the corner solder joint with different crack lengths: 0.056, 0.084, 0.112, 0.1225, and 0.133 mm. The typical von Mises stress contours around the crack tips (with a crack length = 0.112 mm) are shown in Fig. 3.23. It can be seen that, due to stress concentration, the stresses at the crack tip are very large. The *J*-integrals at the inner and outer crack tips for different crack lengths of the corner solder joint are shown in Fig. 3.24.

3.10.2 Thermal Fatigue Life Prediction Model

The curves in Fig. 3.24 can be curve-fitted, as shown in Fig. 3.25 [only four points are used since the solder joint fracture (near the fifth point) is not stable], into the following forms:

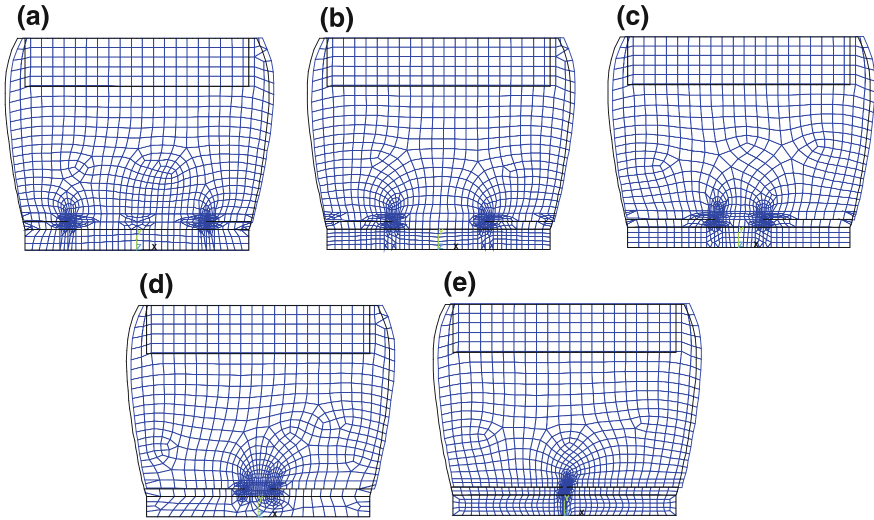

Fig. 3.22 Deformed shape of the corner solder joint. **a** Crack length = 0.056 mm, Δ*J*_inner crack = 0.0704 MPa-mm, Δ*J*_outer crack = 0.0791 MPa-mm. **b** Crack length = 0.084 mm, Δ*J*_inner crack = 0.0918 MPa-mm, Δ*J*_outer crack = 0.126 MPa-mm. **c** Crack length = 0.112 mm, Δ*J*_inner crack = 0.175 MPa-mm, Δ*J*_outer crack = 0.183 MPa-mm. **d** Crack length = 0.1225 mm, Δ*J*_inner crack = 0.284 MPa-mm, Δ*J*_outer crack = 0.313 MPa-mm. **e** Crack length = 0.133 mm, Δ*J*_inner crack = 1.163 MPa-mm, Δ*J*_outer crack = 1.133 MPa-mm

$$\log(\Delta J) = C_3 \log(a) + C_4 \tag{3.14}$$

or

$$a = 10^{-C_4/C_3} \Delta J^{1/C_3} \tag{3.15}$$

The constants C_3 and C_4 are given in Table 3.3. Substituting Eq. (3.15) into Eq. (3.5) yields

$$\frac{da}{dN} = C_1 10^{(C_2C_3 - C_1C_4 + C_4)/C_1C_3} \Delta J^{(C_1-1)/C_1C_3} \tag{3.16}$$

Thus, for the inner crack (Table 3.3), C_1 = 1.8606; C_2 = −4.1427; C_3 = 1.655; C_4 = −4.108, and Eq. (3.16) becomes

$$\frac{da}{dN} = 0.155 \Delta J^{0.279} \tag{3.17}$$

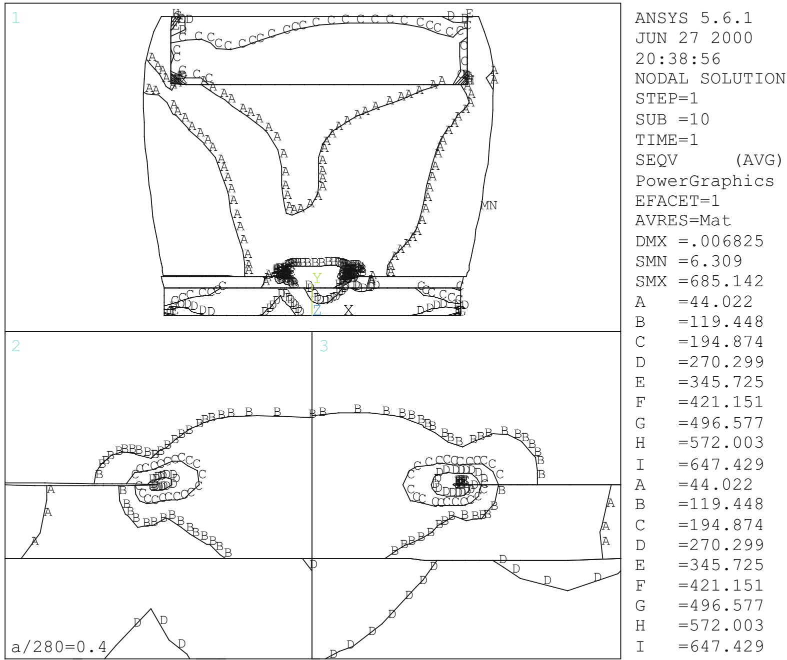

Fig. 3.23 Mises stress contour at the tip of outer (left) and inner (right) cracks (crack length = 0.112 mm)

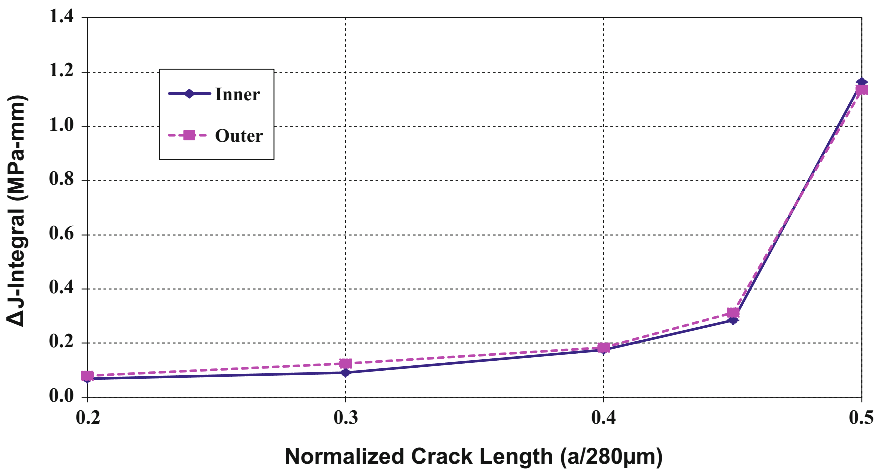

Fig. 3.24 *J*-Integral range of different crack length in the corner solder joint

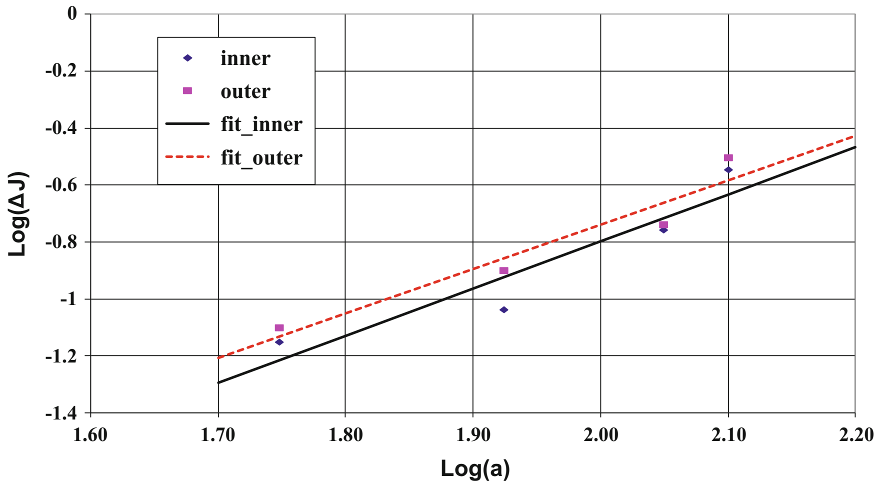

Fig. 3.25 Curve-fitting of the *J*-Integral range of different crack length in the corner solder joint

Table 3.3 Curve-fitting constants C_1, C_2, C_3, C_4 (ΔJ)

Curve-fitted	Location	C_1	C_2	C_3	C_4
Crack Length Vs. Cycles	Inner Crack	1.86	−4.14	–	–
	Outer Crack	1.80	−3.81	–	–
J-integral Vs. Crack Length	Inner Crack	–	–	1.655	−4.108
	Outer Crack	–	–	1.557	−3.854

For the outer crack (Table 3.3), $C_1 = 1.8019$; $C_2 = -3.8061$; $C_3 = 1.557$; $C_4 = -3.854$, and Eq. (3.16) becomes

$$\frac{\mathrm{d}a}{\mathrm{d}N} = 0.176\Delta J^{0.286} \tag{3.18}$$

Equations (3.17) and (3.18) are shown in Fig. 3.26. By averaging the coefficients of Eqs. (3.17) and (3.18), the thermal fatigue life prediction equation (Fig. 3.26) for WLCSP solder joints can be expressed as

$$\frac{\mathrm{d}a}{\mathrm{d}N} = 0.166\Delta J^{0.28} \tag{3.19}$$

Thus, for a given solder-bumped WLCSP assembly, once the *J*-integral range (ΔJ) in terms of the crack length (a) is determined for a given temperature-cycling condition by computational modeling, the number of cycle to failure (N) can be estimated by Eq. (3.19).

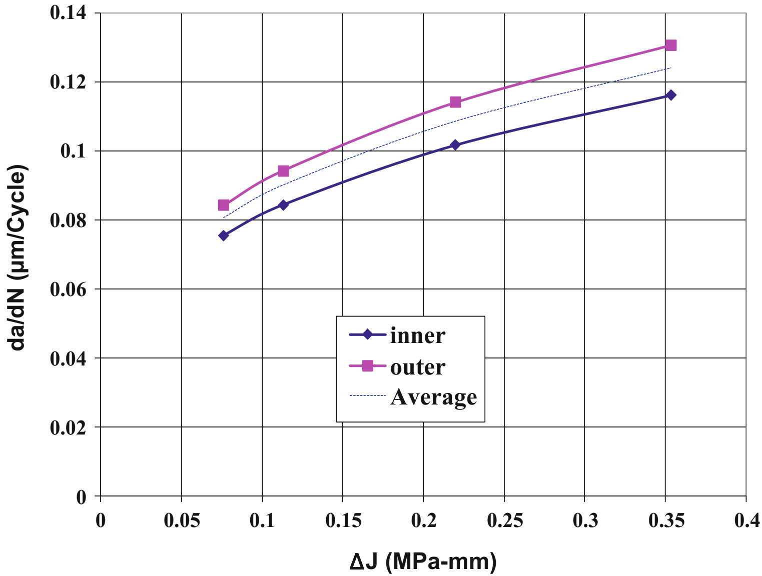

Fig. 3.26 Fatigue crack growth rate curves

3.10.3 Summary and Recommendations

- A simple empirical equation for predicting the thermal fatigue life of solder-bumped flip chip on low-cost PCB has been presented. It is derived by combining the measured thermal fatigue crack growth rate of the corner solder joint and the simulated nonlinear fracture characteristics (*J*-integral) at the crack tip of the corner solder joint with various crack lengths.
- The use of the proposed equation is very simple. For any given 63Sn–37Pb solder-bumped flip chip on FR-4 epoxy PCB assembly, once the *J*-integral range in terms of the crack length is determined for a given temperature-cycling condition by computational modeling, then the number of cycle to failure of the solder joint can be estimated by the integration of the proposed equation.
- In order to verify the accuracy of the proposed equation, more experimental work is necessary. This can be done by testing WLCSPs with different chip sizes and various solder joint geometry.

3.11 Fracture Characteristics of the Corner Solder Joint—Creep Thermal Fatigue Life Prediction Model (ΔW)

3.11.1 Assumptions

In this study [18], the solder (63Sn–37Pb) is assumed to be a creep material (Fig. 3.15). Again, Fig. 3.16 (the corner solder joint) is used for modeling. Due to the global/local thermal expansion mismatch between the Si, FR-4, and solder, the mismatch stresses and strains (such as the creep strain energy density around the crack tip of different crack lengths) produce the driving force for solder joint failure.

In this study, three different crack lengths are considered. These cracks are located symmetrically 10 mm above the copper pad on the PCB. The eight-node plain strain element is used in this study. At the crack tip, the mid-side nodes of the triangular elements, as shown in Fig. 3.27, are placed at the quarter points to capture the singularity in the stresses. Contact elements are used to simulate the closing and sliding of the crack surfaces.

3.11.2 Boundary Conditions

The whole solder joint is subjected to a temperature profile, T (°C), as shown in Fig. 3.28. The bottom surface is fixed, the top surface (nodes) of the solder joint is subjected to a global thermal expansion mismatch displacement, $\Delta = 3.22593 \times T$

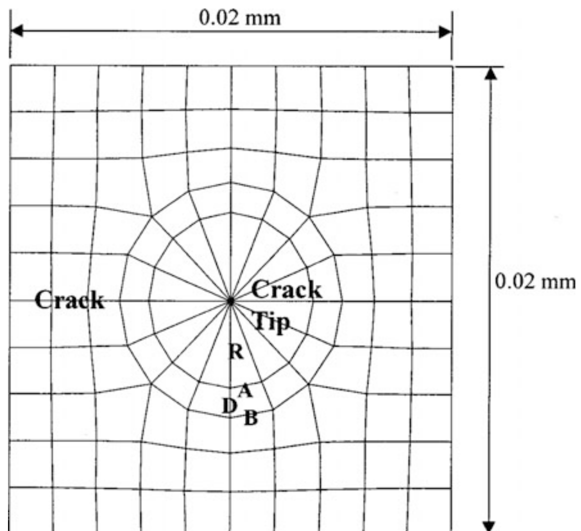

Fig. 3.27 Elements around a crack tip for averaged strain energy density calculation

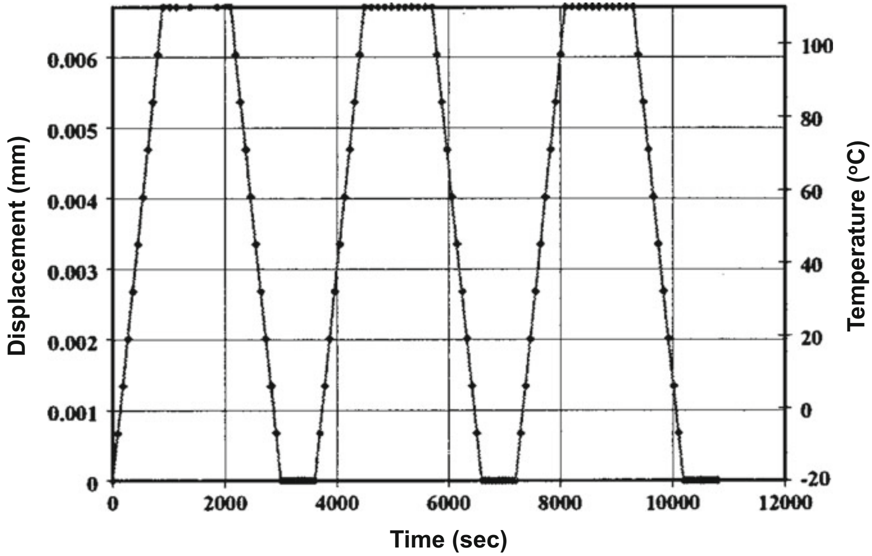

Fig. 3.28 Temperature and displacement boundary conditions

(°C) × [18.5 − 2.5] × 10^{-6} mm, as shown in Figs. 3.28 and 3.16. The top surface is also restrained from rotation by specifying nodal couplings of vertical displacement to those nodes so that the vertical displacements are the same.

3.11.3 Deformed Shape, Stress, and Strain

Figure 3.29a–c shows the deformed (with finite element meshes) and un-deformed shapes of the corner solder joint with different crack lengths: 0.056, 0.084, and 0.112 mm. The typical von Mises stress contours around the crack tips (with a crack length = 0.112 mm) are shown in Fig. 3.30. It can be seen that due to stress concentration the stresses at the crack tip are very large.

Figures 3.31, 3.32, and 3.33 show the shear creep strain history, shear stress history, and shear stress and shear creep strain hysteresis loops at the middle between the crack tips (Fig. 3.29a with crack length = 0.112 mm) of the corner solder joint for three full thermal cycles. It can be seen that the responses are converged. The shear creep strain range is about 0.33 and the shear stress range is about 90 MPa.

Figures 3.34, 3.35, and 3.36 show the shear creep strain history, shear stress history, and shear stress and shear creep strain hysteresis loops at a point near the crack tip (with crack length = 0.112 mm) of the corner solder joint for three full thermal cycles. Again, the responses are converged. However, as expected, the shear creep strain range is very large (about 0.72) and the shear stress range is also very large (about 115 MPa).

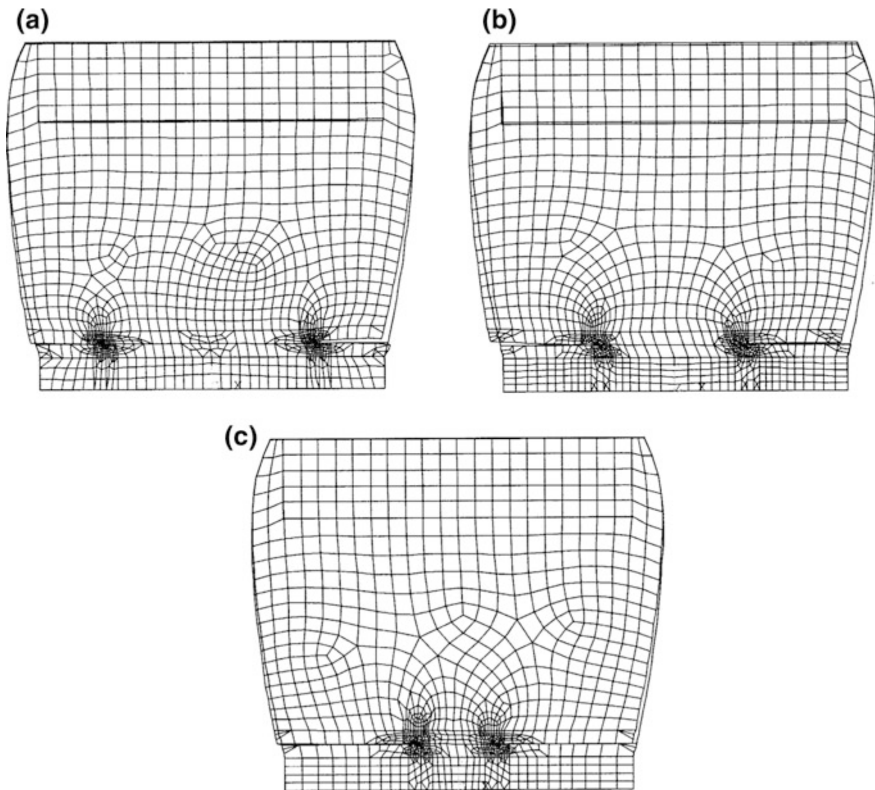

Fig. 3.29 Deformed shape of the corner solder joint. **a** Crack length = 0.056 mm, T = 20 °C. **b** Crack length = 0.084 mm, T = 20 °C. **c** Crack length = 0.112 mm, T = 20 °C

3.11.4 Strain Energy Density Around the Crack Tip

Theoretically speaking, because of singularity, the strain energy density at the crack tip is infinitive. Practically, however, the average strain energy density per thermal cycle around the crack tip is used to determine the thermal fatigue life of solder joints. In this study, the strain energy density around a crack tip is obtained by averaging across the elements in an area of 0.02 mm by 0.02 mm in the two-dimensional model as shown in Fig. 3.27. (For the case of conventional solder-bumped flip chip on board assembly, the radius of the copper pad is about 3–4 mils and the solder joint height is about 1–2 mils for eutectic solder and 3–4 mils for high-temperature solder, then the area for averaging the strain energy density should be 0.008 mm by 0.008 mm.)

There are about 100 elements in the 0.02 × 0.02 mm area^2. The crack tip is modeled with two rows of elements. The elements in the first row are triangular elements with the mid-side nodes skewed to 1/4 points, as suggested by ANSYS for

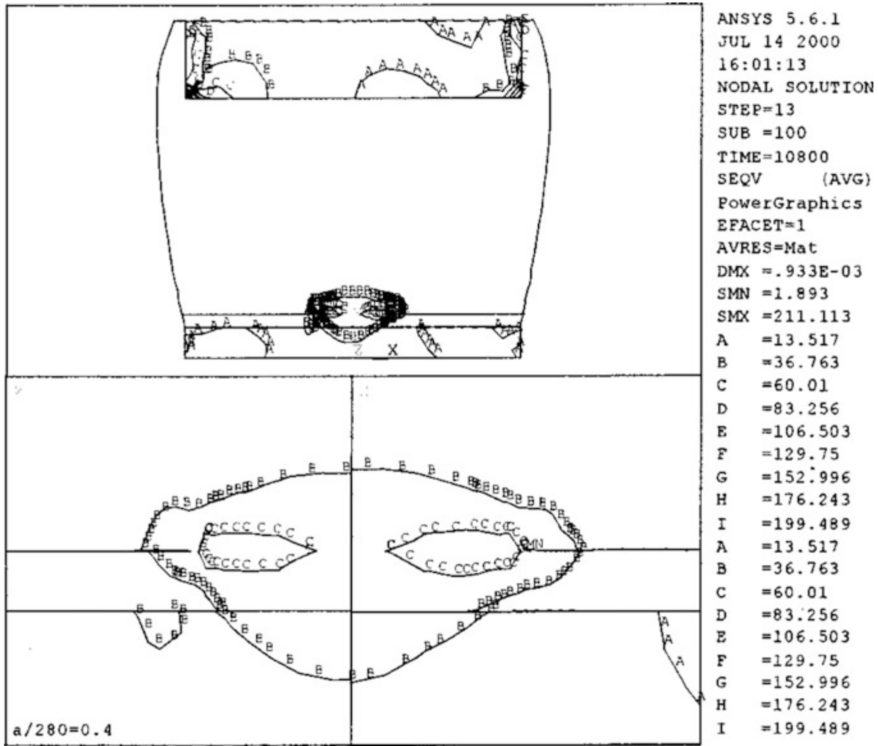

Fig. 3.30 Mises stress contour at the tip of outer (left) and inner (right) cracks (crack length = 0.112 mm)

the effect of crack tip singularity. The radius of the first row is 0.0037 mm, i.e., about 20% of the length of one side (0.02 mm) of the square area as shown in Fig. 3.27 (For the case of conventional flip chip on board assembly, the radius is about 0.0016 mm.). There are 16 uniform angular divisions around the crack tip. The quadrilateral elements on the second row have a radial length being half of that of the first row. Regular meshed are generated for the remaining area used in the strain energy density calculation.

The average strain energy density of the elements in this area at any time instant during the viscoplastic process is normalized by the volume of the elements.

$$W_t = \left(\sum W_{\text{element}} \times V_{\text{element}}\right) / \sum V_{\text{element}}, \tag{3.20}$$

where W_t is the average creep strain energy density at time point t, W_{element} is the creep strain energy density in each element and is directly extracted from ANSYS in its postprocessing, and V_{element} is the volume of each element. For a two-dimensional problem, however, ANSYS gives volume of each element in its

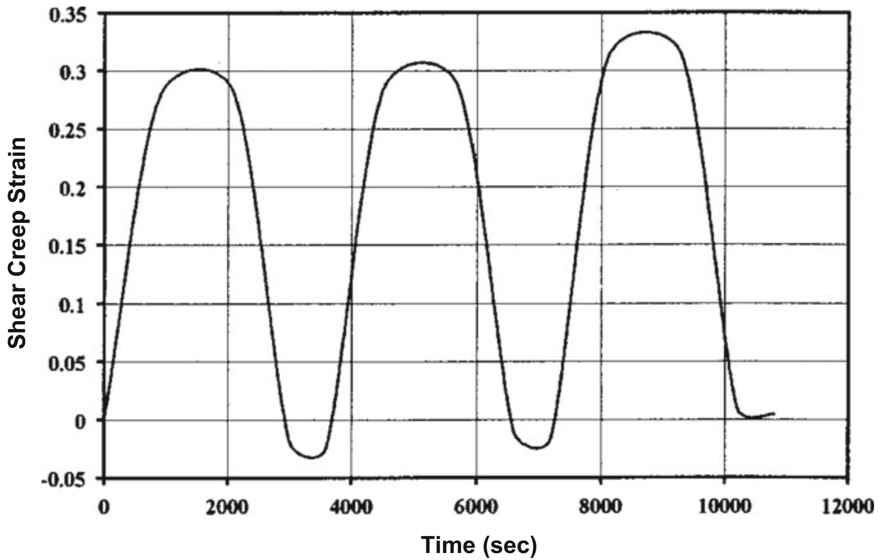

Fig. 3.31 Shear creep strain history at the middle of crack tips of the corner solder joint

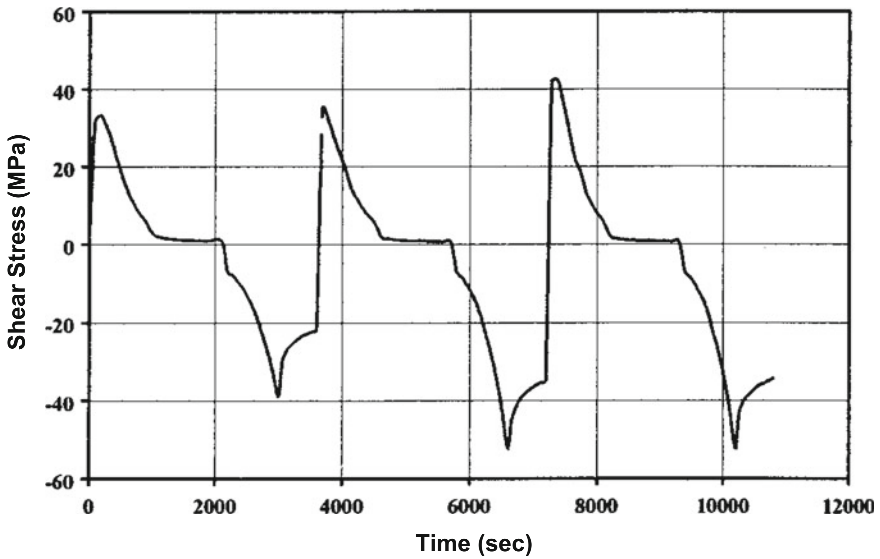

Fig. 3.32 Shear stress history at the middle of crack tips of the corner solder joint

postprocessing by assuming a unit thickness. The accumulated average strain energy density in a complete thermal cycle from time t_1 to time t_2 is calculated by $W_{t2} - W_{t1}$. In this study, t_1 = 7200 and t_2 = 10,800 s at the beginning and ending

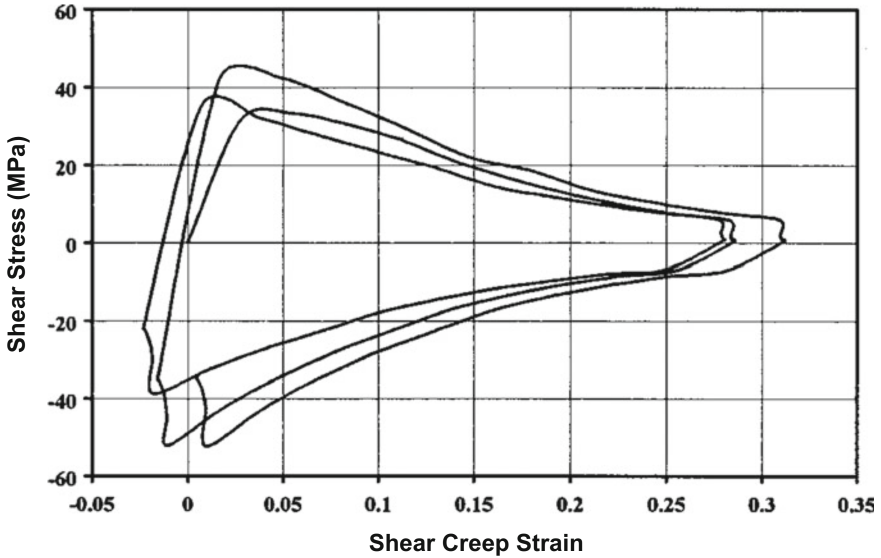

Fig. 3.33 Hysteresis loops at the middle of crack tips of the corner solder joint

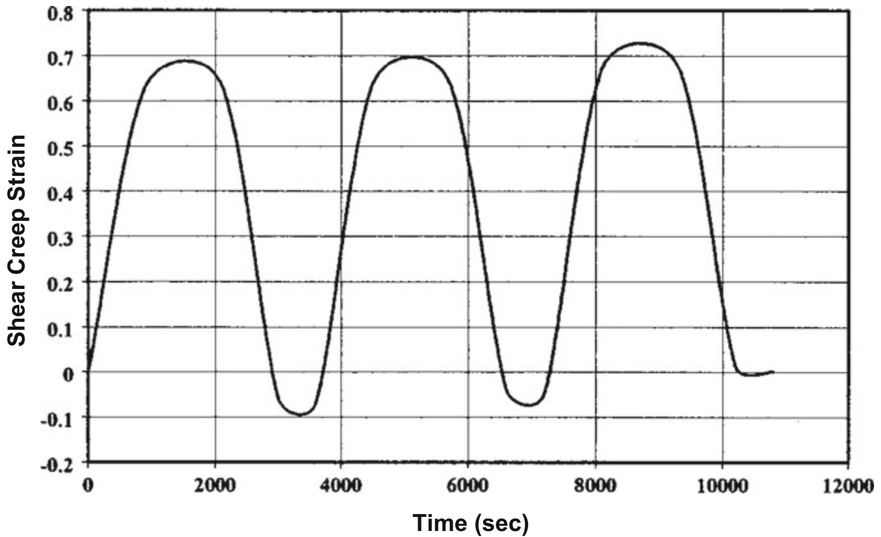

Fig. 3.34 Shear creep strain history near one of the crack tips of the corner solder joint

of the third cycle, respectively, are used. The accumulated average strain energy density range in the third thermal cycle around the inner and outer crack tips for different crack lengths of the corner solder joint is shown in Fig. 3.37. It can be seen

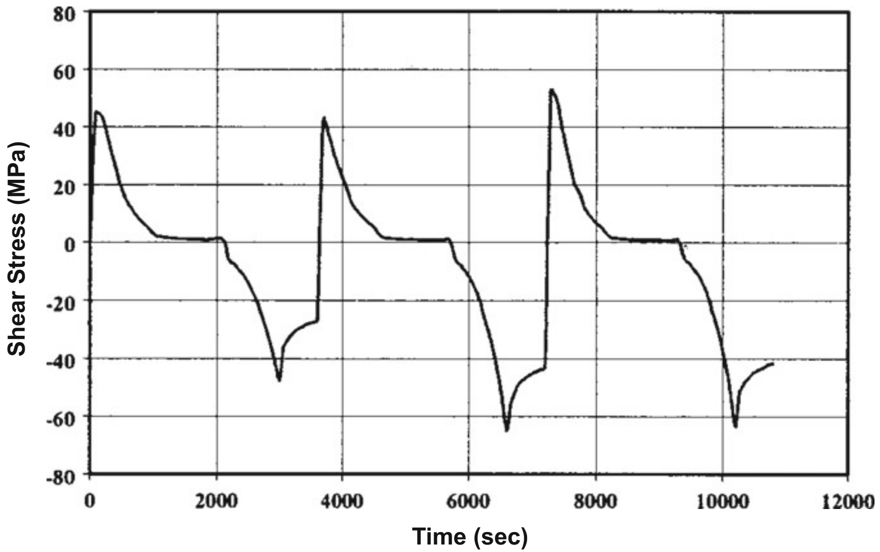

Fig. 3.35 Shear stress history near one of the crack tips of the corner solder joint

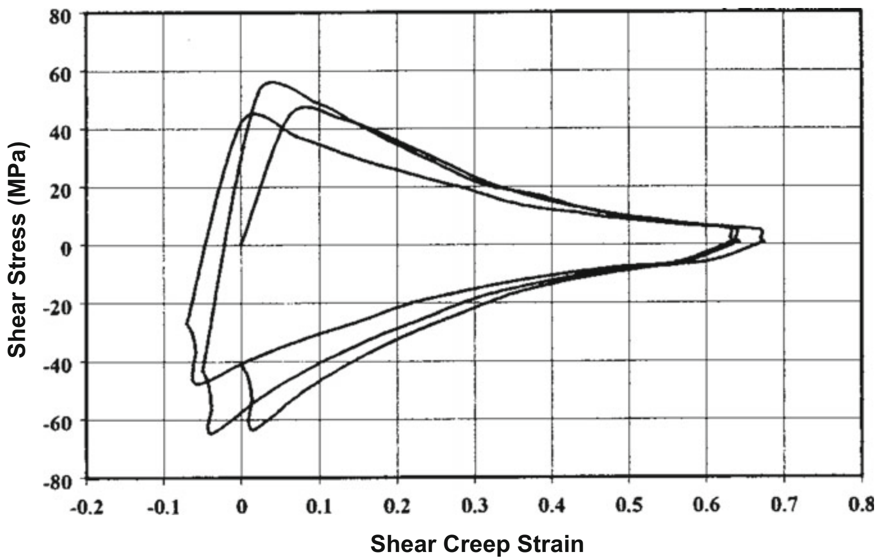

Fig. 3.36 Hysteresis loops near one of the crack tips of the corner solder joint

that the larger the crack length the larger the average strain energy density range. Also, for a given crack length, the average strain energy density range around the outer crack tip is larger than that around the inner crack tip.

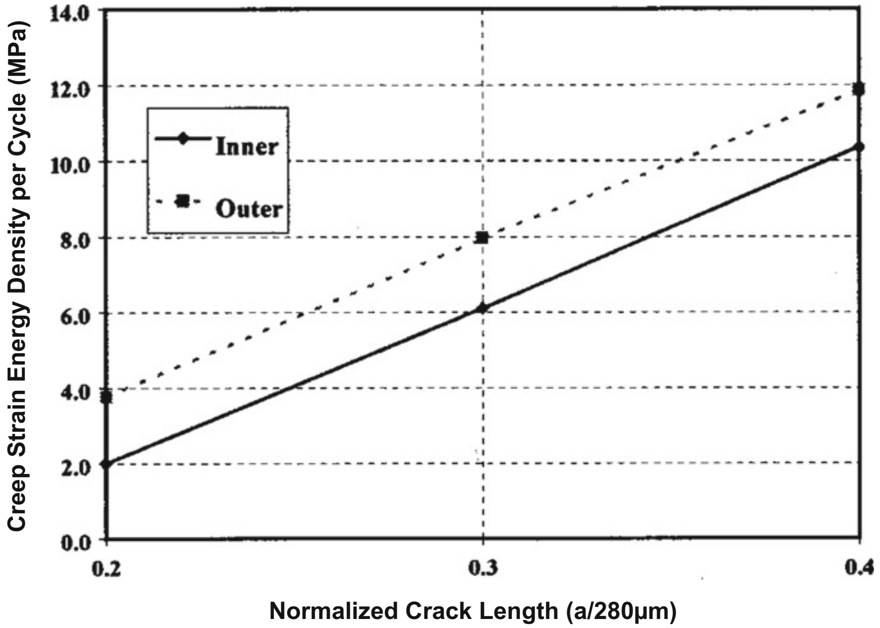

Fig. 3.37 Average strain energy density range of different crack length in the corner solder joint

3.11.5 A New and Simple Thermal Fatigue Life Prediction Model

The curves in Fig. 3.37 can be curve-fitted, as shown in Fig. 3.38 into the following forms:

$$\log(\Delta W) = C_3 \log(a) + C_4 \tag{3.21}$$

or

$$a = 10^{-C_4/C_3} \Delta W^{1/C_3} \tag{3.22}$$

The constants C_3 and C_4 are given in Table 3.4. Substituting Eq. (3.22) into Eq. (3.5) yields

$$\mathrm{d}a/\mathrm{d}N = C_1 10^{(C_2C_3 - C_1C_4 + C_4)/C_1C_3} \Delta W^{(C_1-1)/C_1C_3} \tag{3.23}$$

Thus, for the inner crack (Table 3.4), C_1 = 1.8606; C_2 = −4.1427; C_3 = 2.406; C_4 = −3.887, and Eq. (3.23) becomes

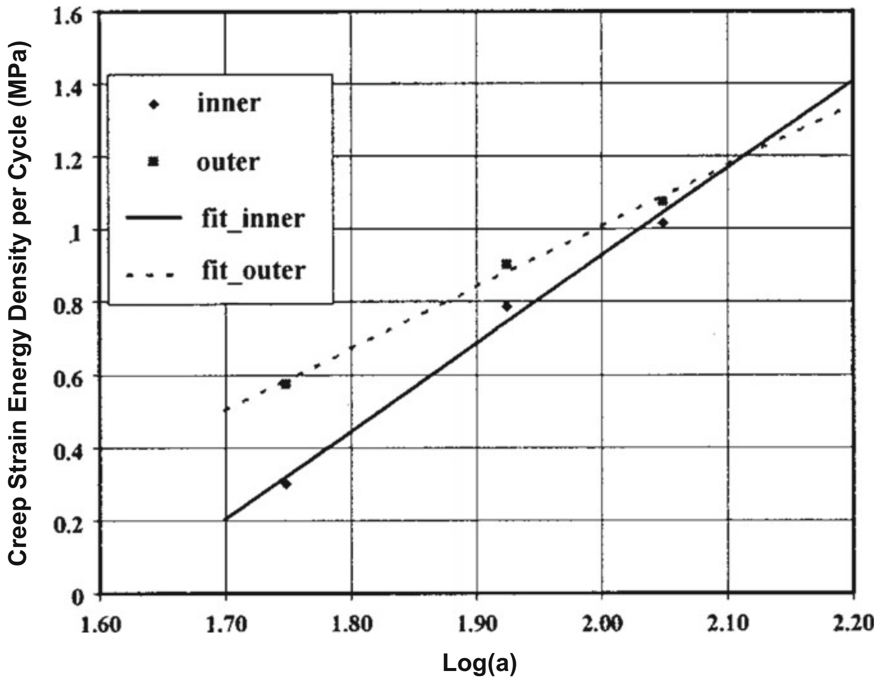

Fig. 3.38 Curve-fitting of the average strain energy density range of different crack lengths in the corner solder joint

Table 3.4 Curve-fitting constants C_1, C_2, C_3, C_4 (ΔW)

Curve-fitted	Location	C_1	C_2	C_3	C_4
Crack Length Vs. Cycles	Inner Crack	1.86	−4.14	–	–
	Outer Crack	1.80	−3.81	–	–
Strain energy Vs. Crack Length	Inner Crack	–	–	2.406	−3.887
	Outer Crack	–	–	1.677	−2.347

$$da/dN = 0.062 \Delta W^{0.192} \tag{3.24}$$

For the outer crack (Table 3.4), $C_1 = 1.8019$; $C_2 = -3.8061$; $C_3 = 1.677$; $C_4 = -2.347$, and Eq. (3.23) becomes

$$da/dN = 0.058 \Delta W^{0.265} \tag{3.25}$$

Equations (3.24) and (3.25) are shown in Fig. 3.39. By averaging the coefficients of Eqs. (3.24) and (3.25), the thermal fatigue life prediction equation (Fig. 3.39) for WLCSP solder joints can be expressed as

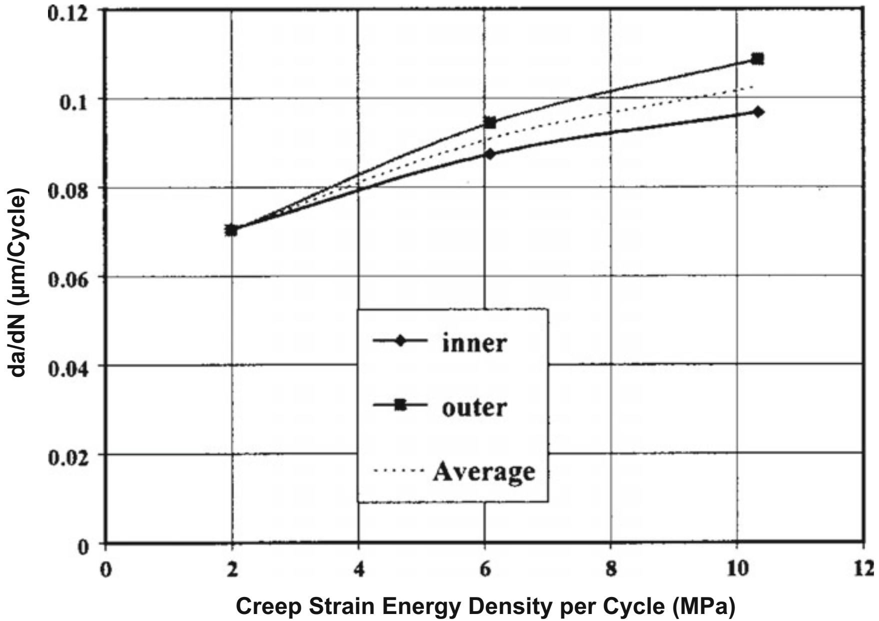

Fig. 3.39 Fatigue crack growth rate curves of the corner solder joint

$$\mathrm{d}a/\mathrm{d}N = 0.06\Delta W^{0.25} \tag{3.26}$$

Thus, for a given solder-bumped flip chip assembly, once the average strain energy range (ΔW) in terms of the crack length (a) is determined for a given temperature-cycling condition by computational modeling, the number of cycle to failure (N) can be estimated by Eq. (3.26).

3.11.6 Summary and Recommendation

- A new and simple empirical equation for predicting the thermal fatigue life of solder-bumped flip chip on low-cost PCB has been presented. It is derived by combining the measured thermal fatigue crack growth rate of the corner solder joint and the simulated nonlinear fracture characteristics $\sim$ average strain energy density per cycle around the crack tip of the corner solder joint with various crack lengths.
- The use of the proposed equation is very simple. For any given WLSCP PCB assembly and solder-bumped flip chip on PCB assembly, once the average strain energy density range per thermal cycle in terms of the crack length is determined for a given temperature-cycling condition by computational modeling, then the

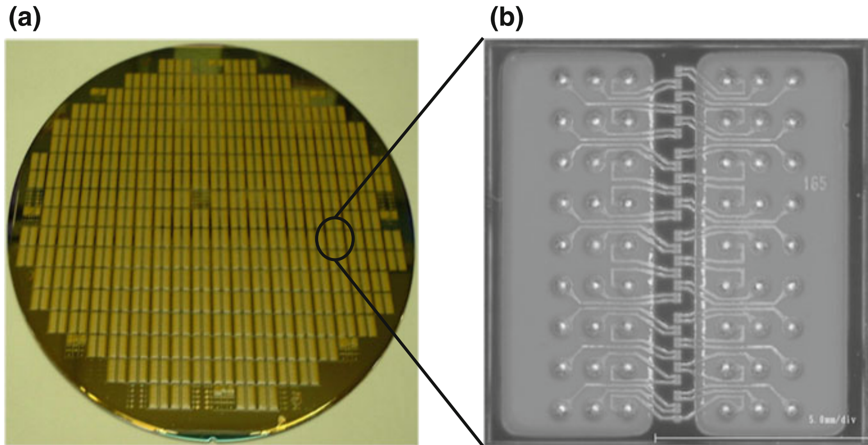

Fig. 3.40 **a** Hitachi's memory chips on an 8-in. wafer. **b** Hitachi's WLCSP with original pads along the centerline and redistributed pads area array within the chip area

number of cycle to failure of the corner solder joint can be estimated by the integration of the proposed equation ~ 8!

- The element sizes and shapes and the area around the crack tip for calculating the average strain energy density are recommended for the WLCSP-PCB assembly. For the conventional solder-bumped flip chip on PCB assemblies, these parameters for determining the average strain energy density are also recommended.

3.12 Hitachi's WLCSP

Figure 3.40a shows a Hitachi's wafer with memory chips. The original pads on the memory chips are very fine-pitch and distributed along the centerline of the chip as shown in Fig. 3.40b.

3.12.1 Hitachi's WLCSP with Stress Relaxation Layer

A metal RDL is used to redistribute the fine-pitch original pads along the centerline of the chips on a wafer to much larger pitch area-arrayed pads all over the area within the chips as shown in Fig. 3.40b. In order to apply to larger chips (e.g., 10 mm $\times$ 10 mm) without underfill, Hitachi introduced [54] a stress relaxation layer between the Si chip and the solder bumps as shown in Fig. 3.41.

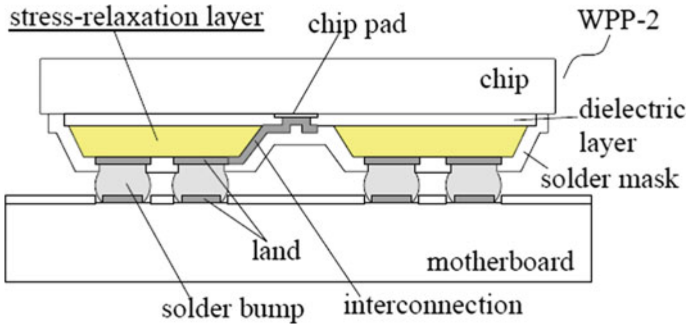

Fig. 3.41 Cross section of Hitachi's WLCSP mounted on a PCB

3.12.2 Key Process Steps for Hitachi's WLCSP

The key process steps of Hitachi's WLCSP (Table 3.5) with a stress relaxation layer are shown in Fig. 3.42. First, the wafer is spin-coated with a photosensitive polyimide (P–PI), and the chip pads and dicing streets are opened up by photolithography. Then, a stress relaxation layer is formed by printing liquid resin on the wafer through a stencil mask with no opening on the pads and dicing streets. The resin will flow through the open edges and form smooth slopes.

To add a layer of metal on the wafer, Hitachi sputters the seed metals (Cr and Cu) on the whole wafer, spin-costs a photoresist layer, and opens up the shapes of interconnections and new pads (in area array format) by photolithography. Then, the interconnections and pads are formed by electroplating the Cu and Ni. The photoresist and seed metals are removed by etching.

Now, the wafer is spin-coating with the P–PI again and the new chip pads and dicing streets are opened up by photolithography. This time, the P–PI acts like a solder mask. After fluxing, the SnAgCu solder bumps are placed on the new land pads on the wafer through a stencil mask with a solder ball mounter. Finally, the wafer is reflowed, cleaned, and diced.

Table 3.5 Hitachi's WLCSP test vehicle

Chip	Size	10 mm × 10mm
	Thickness	0.725 mm
Pad layout	Number of bumps	54 (9 × 6)
	Bump pitch	1.0 mm × 0.8 mm
	DNP	4.7 mm
Solder	Material	SnAgCu
	Ball diameter	400 μm
PCB	Material	FR-4
	Thickness	1.27 mm

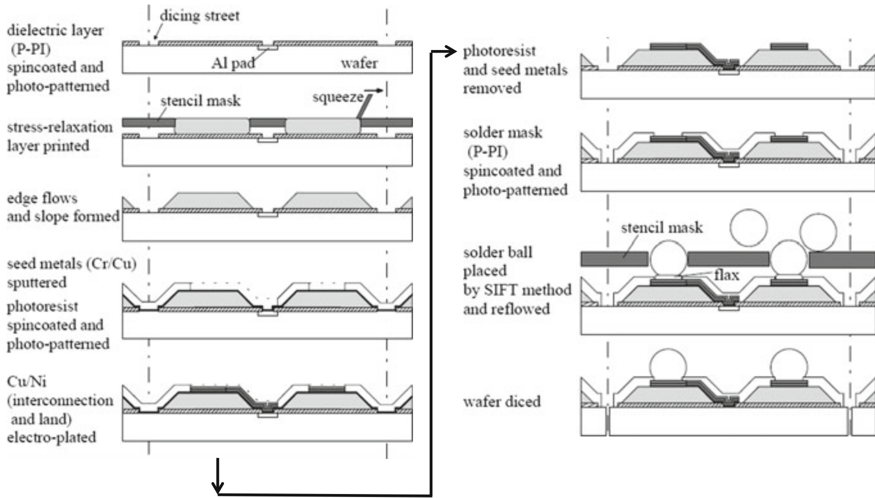

Fig. 3.42 Key process steps of Hitachi's WLCSP with a stress relaxation layer

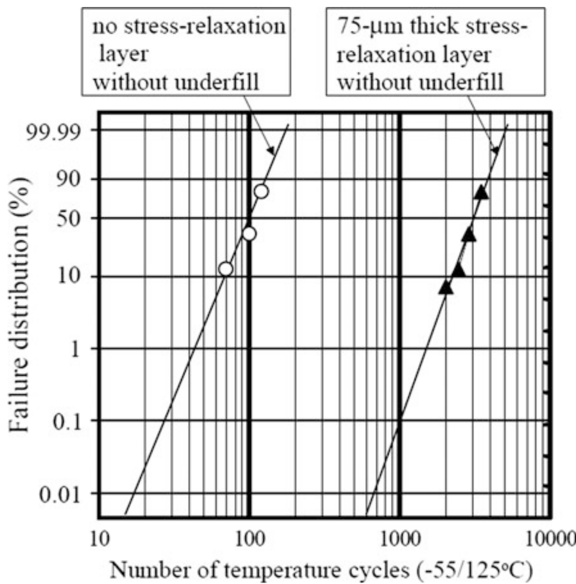

Fig. 3.43 Temperature-cycling test of Hitachi's WLCSP with a stress relaxation layer

3.12.3 Reliability of Hitachi's WLCSP

Figure 3.43 shows the life distribution of the temperature-cycling test (−55 ↔ 125 °C) of the Hitachi's (10 mm × 10 mm) WLCSP (without an

underfill) with a stress relaxation layer on PCB. It can be seen that the characterization life of the WLCSP with a stress relaxation layer is more than 3000 cycles. On the other hand, the characterization life is less than 200 cycles for the same chip size without stress relaxation layer and underfill.

3.13 TSMC's UFI WLCSP

In order to save some process steps, reduce the cost, and lower package profile, TSMC [55] eliminate the under-bump metallurgy (UBM) in their WLCSP, and called it UFI (UBM-free integration) fan-in WLCSP.

3.13.1 TSMC's WLCSP with Protection Layer

Figure 3.44a shows the conventional WLCSP and Fig. 3.44b shows the TSMC's UFI WLCSP. It can be seen that for the UFI WLCSP, the polymer-2 and UBM are gone. Instead, a polymer composite protection layer (PL) is introduced to secure the solder bumps.

3.13.2 Key Process Steps for TSMC's WLCSP

In TSMC's UFI WLCSP, the solder balls are directly mounted on the Cu RDL which routes electrical signals from the original pads of the chip to the desired area array pads. Then, it is followed by the PL deposition to secure the solder bumps.

3.13.3 Reliability of TSMC's WLCSP

Figure 3.45 shows the life distribution of the thermal cycling results of TSMC's UFI WLCSP on PCB. TSMC [55] found that because of: (1) The mechanical

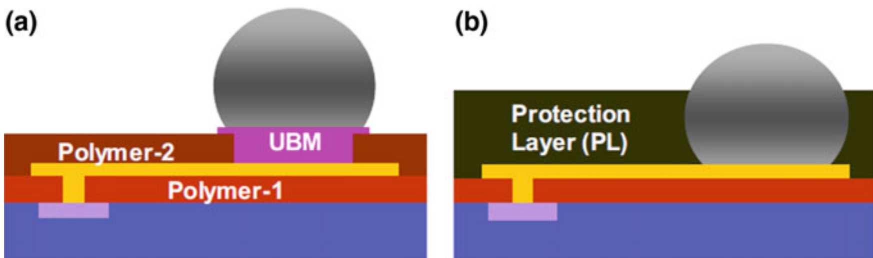

Fig. 3.44 **a** Conventional WLCSP. **b** TSMC's UFI WLCSP

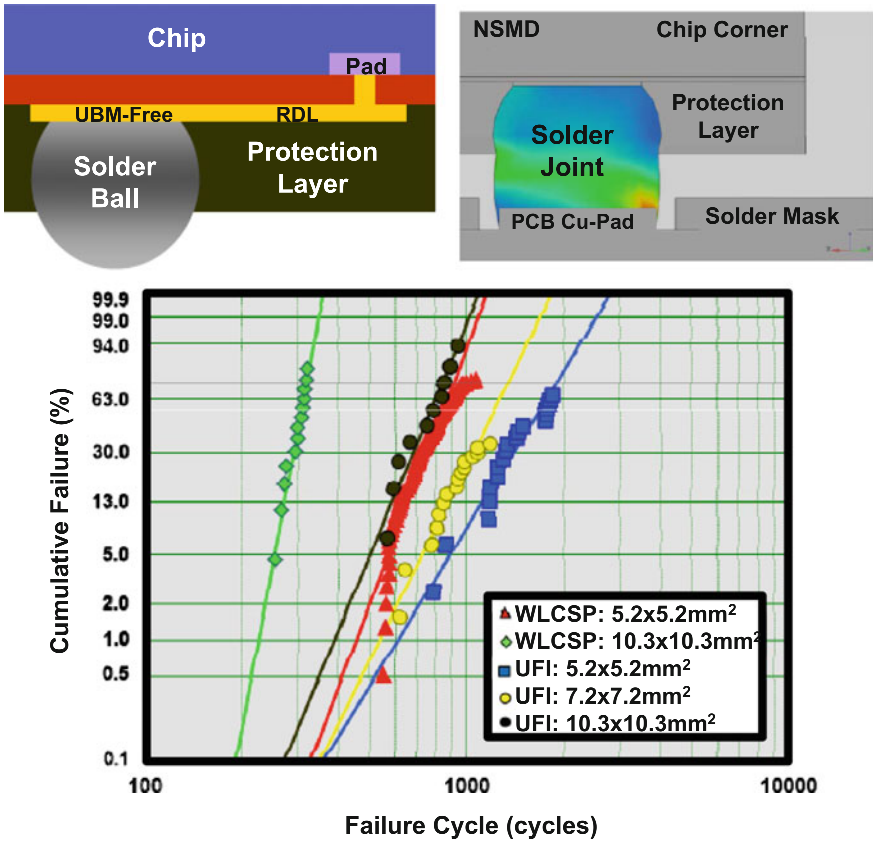

Fig. 3.45 TSMC's UFI WLCSP with polymer composite protection layer

support of the PL, (2) The controlling of the maximum strain location, and (3) The material optimization, the UFI WLCSP solder joint is reliable (the characteristic life is more than 800 cycles and the thermal cycling takes place between the temperatures of −40 and +125 °C, at one cycle per hour) even for a chip size up to 10.3 mm × 10.3 mm without underfill.

3.14 Summary and Recommendations

WLCSP is facing stiff competition from FOWLP. Because of (1) the die shrinking to reduce the device wafer cost, and (2) the more functionality to build into a chip (and thus increase pin outs) to increase efficiency, there is not enough space of the chip to fan-in all the pads. This is compound with the desire/demand to go for system-in-package (SiP) to increase performance and reduce cost, some of the

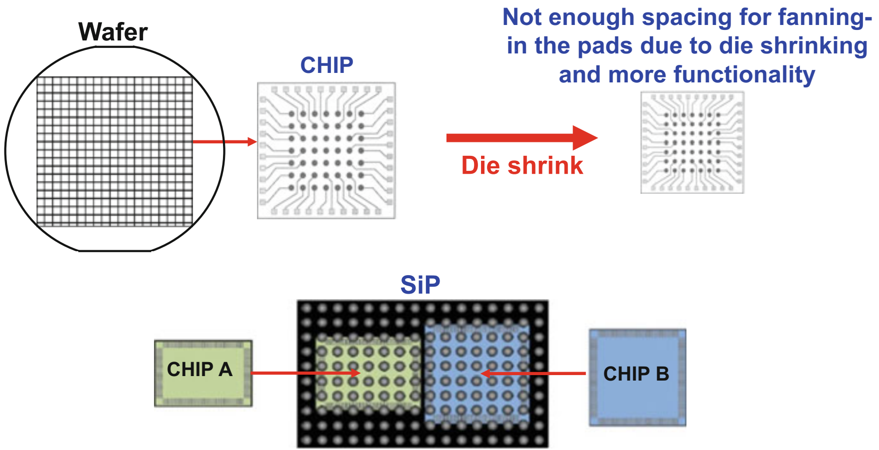

Fig. 3.46 WLCSP versus FOWLP

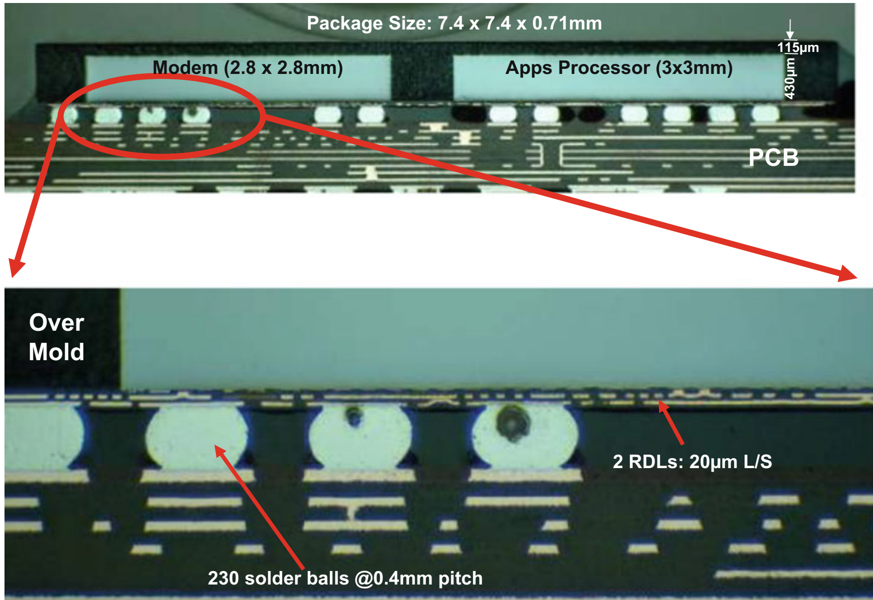

Fig. 3.47 HTC desire 606W (SPREADTRUM SC8502)

market shares are and will be taken away from the FOWLP as shown in Fig. 3.46. Figure 3.47 shows a SiP from a smartphone, HTC Desire 606 W (SPREADTRUM SC8502), which is made by FOWLP technology. The SiP size is 7.4 mm × 7.4 mm × 0.71 mm, which consists of a 2.8 mm × 2.8 mm modem and a 3 mm × 3 mm application processor. There are 2 RDLs.

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Chapter 4
Embedded Chip Packaging

4.1 Introduction

There are many kinds of embedded chip packaging. For example, chips are embedded in epoxy molding compound (EMC) [1–17], chips are embedded in rigid laminated substrates [18], chips are embedded in flexible polyimide substrates [19, 20], chips are embedded in silicon substrates [21, 22], and chips are embedded in glass substrates [23, 24]. Usually, chips embedded in rigid and flexible laminated/ polyimide substrates are in a panel format. In this chapter, except the chips embedded in EMC (which are the focus and will be discussed all over in this book), all the others are briefly mentioned.

4.2 Chips Embedded in Laminated/Polyimide Panel Format

4.2.1 Advantages and Disadvantages

Figure 4.1 schematically shows the embedded passive component and chip. It can be seen from Fig. 4.1a that the passive component is connected to an inner layer by either solder or adhesive first, and then embedded. On the other hand, the chip is mounted on an inner layer/foil first, embedded, and then connected by drilling and Cu plating as shown in Fig. 4.1b. The advantages of embedding passive components and chips are: (a) low profile, (b) low cost with a large panel, (c) better electrical performance with low inductances, and (d) easy to extend to 3D chip stacking. The disadvantages are: (a) cannot rework, (b) infrastructure, and (c) supply chain.

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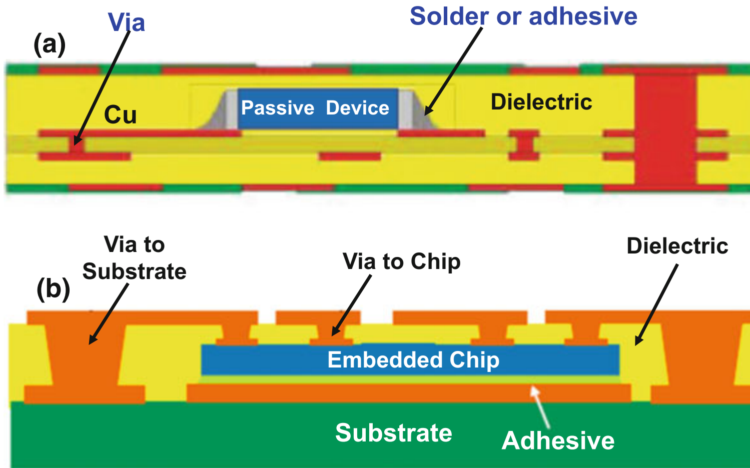

Fig. 4.1 **a** Embedded passive component. **b** Embedded chip

4.2.2 Various Chip Embedding Processes

There are at least two ways to embed the chip in a panel, namely (a) face-up and (b) face-down. Figure 4.2 shows the schematic of the face-up and face-down processes. It can be seen that (a) during the chip attachment process, for the face-up fashion the backside of the chip is attached to the foil and for the face-down fashion the front-side of the chip is attached to the foil, (b) during the embed lamination process, the front-side of the face-up fashion is embedded into the dielectric layer and the backside of the face-down fashion is embedded into the dielectric layer, (c) during the via drilling process, for the face-up fashion the drilling is from the top and stop at the pads of the chip and for the face-down fashion the drilling is from the bottom and stop at the pads of the chip, and (d) during the Cu plating and etching processes, both face-up and face-down fashions electroplate the Cu to fill the vias and make/etch the circuit traces.

4.2.3 Embedded Chip in Rigid Laminated Substrates

Figure 4.3 shows TI's MicroSiP™ [18] manufactured by AT&S. It is a DC/DC converter with an IC chip (PicoStar™) embedded in the substrate (2.9 mm × 2.3 mm) with a solder ball to be attached to PCB. It can be seen from Fig. 4.3 that the IC chip is in a face-down fashion. On top of the substrate, there are the inductor and two capacitors.

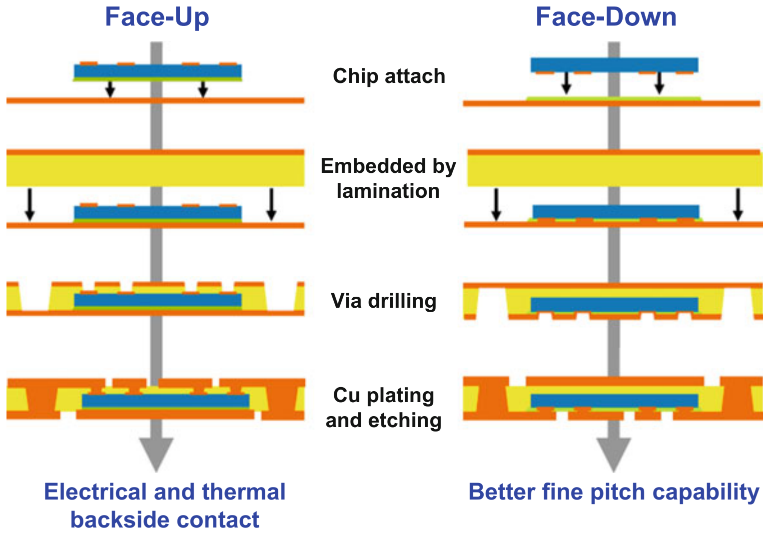

Fig. 4.2 Fabrication processes for the embedded chip in face-up and face-down fashions

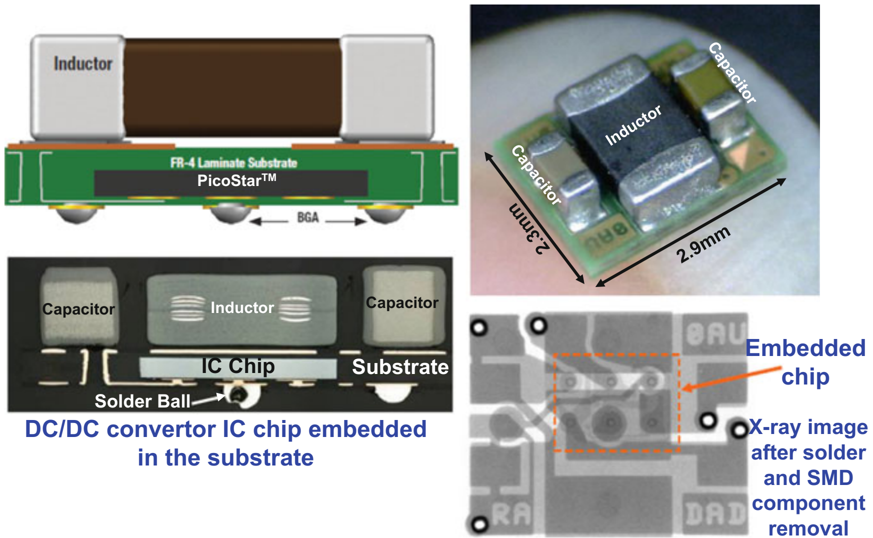

Fig. 4.3 TI's embedded chip in a rigid substrate of a DC/DC converter

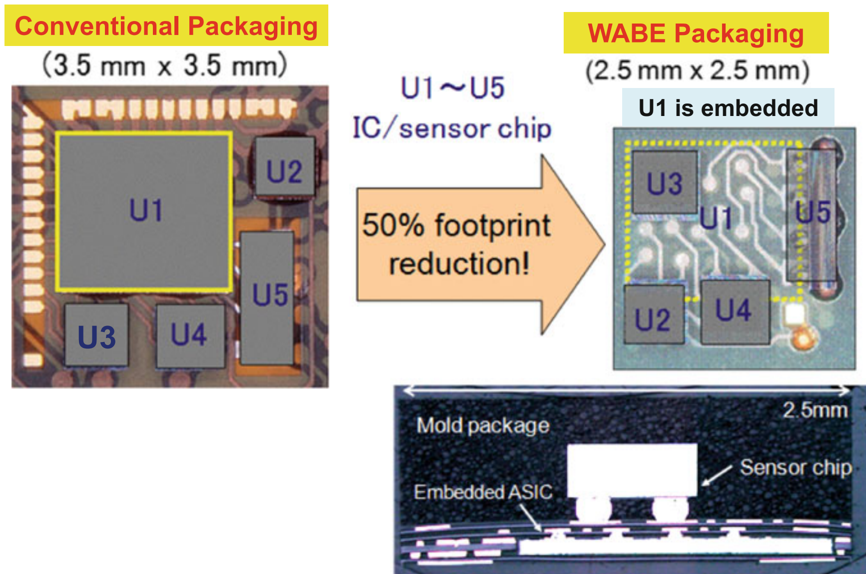

Fig. 4.4 Fujikura's embedded chip in a flexible substrate of a 3D SiP

4.2.4 3D Embedded Chip in Flexible Polyimide Substrates

Figure 4.4 shows schematically the multichip SiP with an embedded chip. It can be seen from the left-hand side of Fig. 4.4 that for the conventional system-in-package (SiP) there are 5 chips (U1 through U5) side-by-side on the substrate (3.5 mm × 3.5 mm). On the left-hand side of Fig. 4.4, it shows that the U1 chip is embedded into the flexible substrate (2.5 mm × 2.5 mm) by Fujikura's WABE (wafer and board level embedded package) technology [19]. The other 4 chips (U2 through U5) are on top of the substrate surface. The package size has been reduced by 50%. The cross section in Fig. 4.4 shows the embedded chip (ASIC or U1) and one sensor chip (the other 3 chips are not in the photo image).

4.2.5 3D Embedded Stacking Chips in Flexible Polyimide Substrates

Figure 4.5 shows the cross-section photo image of a multilayer board embedding two chips in stacked configuration [20] fabricated by the WABE technology. The minimum thickness of these chips is 85 μm and they are interconnected through the Cu traces and vias. There are nine layers of the board and its total thickness is 0.55 mm.

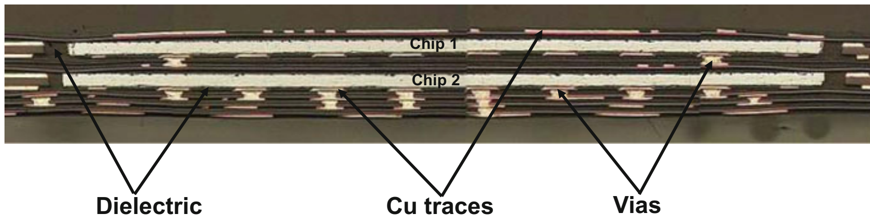

Fig. 4.5 Fujikura's embedded two chips in the stacked configuration

4.3 Chips Embedded in Si Wafer

In 2013, Maxim is the first to present the concept of mold-free silicon wafer-based fan-out technology, i.e., chips embedded in Si wafer [21, 22].

4.3.1 Key Process Steps

Figure 4.6a shows the schematic of Maxim's chips embedded in Si wafer [21, 22] with rectangular-shaped cavities (left-hand side) and trapezoidal-shaped cavities (right-hand side). These cavities are formed on a low-cost silicon wafer using the potassium hydroxide (KOH) wet-etch process. The chips are picked and placed face-up in the cavities filled with epoxy resin as shown in Fig. 4.6b. Then, it is followed by fabricating the dielectric layers and conductor layers (RDLs) and mounting the solder balls as shown in Fig. 4.6c. Figure 4.7 shows the scanning electron microscope (SEM) image of a cross section of the chip embedded in Si wafer. It can be seen that the chip is embedded in the Si substrate and its circuitries are fanned-out through the RDLs to solder balls.

4.3.2 Reliability of Chips Embedded in Si Wafer

Figure 4.8 shows the schematic of a test package (6 mm × 6mm) with 16 × 16 solder balls on a 0.4 mm pitch. It is assembled on a PCB and subjected to a thermal cycling test (−40 °C ↔ +125 °C, one cycle per hour, 15-min dwell, and 15-min ramp) according to the JEDEC standard JESD22-A104 [23]. The test results (Weibull distribution [24]) are shown in Fig. 4.9 and it can be seen that it passes 645 cycles.

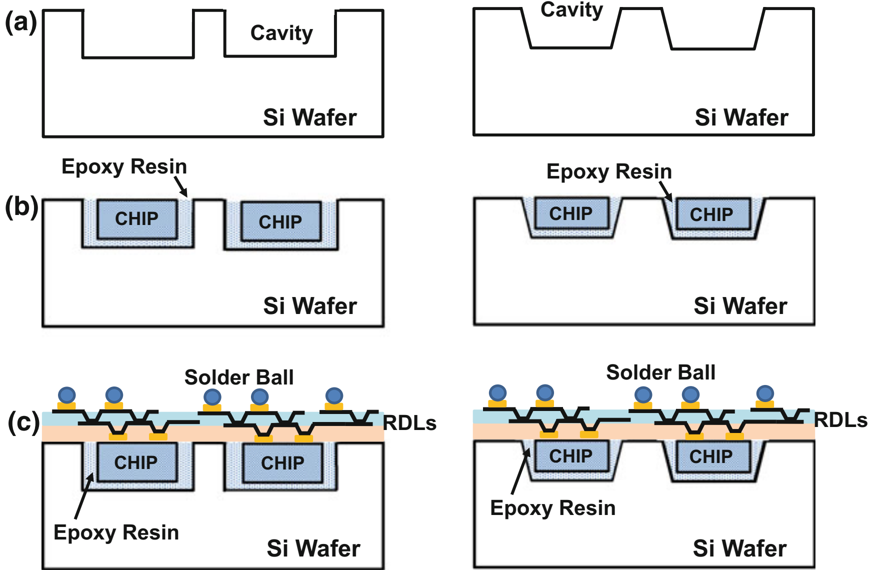

Fig. 4.6 Maxim's chips embedded in silicon wafer. **a** Cavities formation by KOH. **b** P&P chips (face-up) in cavities. **c** RDLs fabrication and solder balls mounting

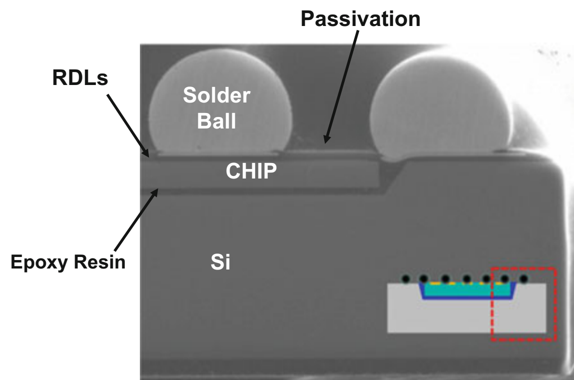

Fig. 4.7 Cross-section SEM image of Maxim's chips embedded in silicon wafer

4.4 Chips Embedded in Glass Panel

In 2017, George Institute of Technology (GIT) is the first to present and demonstrate the concept of mold-free glass panel-based fan-out technology, i.e., chips embedded in glass panel [25, 26].

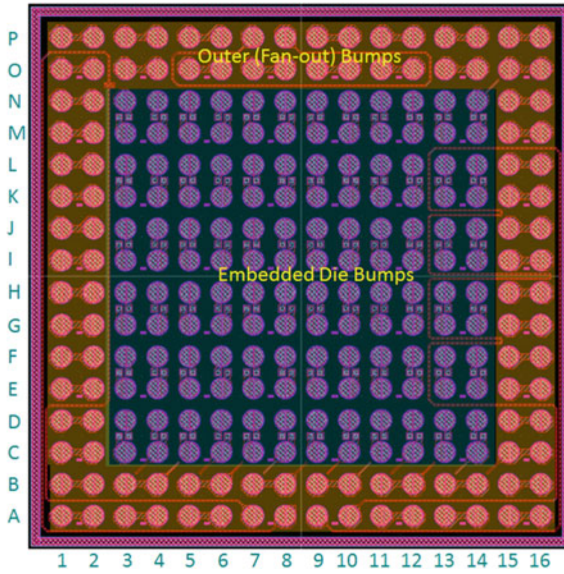

Fig. 4.8 Maxim's chip embedded in silicon substrate (16 × 16 solder balls on 0.4 mm pitch)

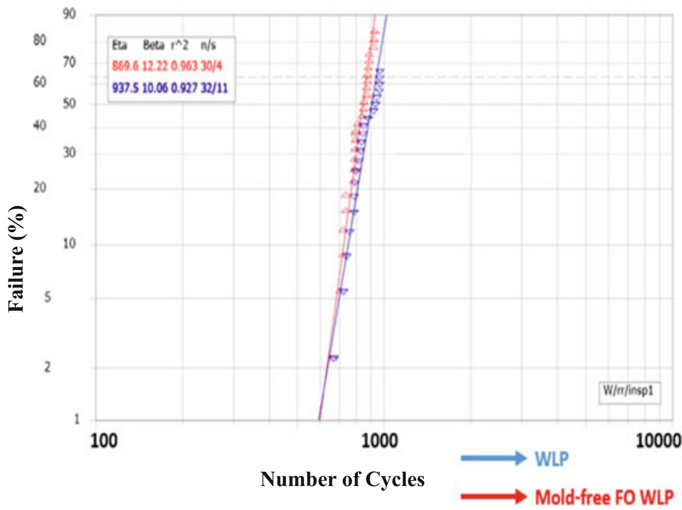

Fig. 4.9 Life distribution of Maxim's chip embedded in silicon substrate under thermal cycling test

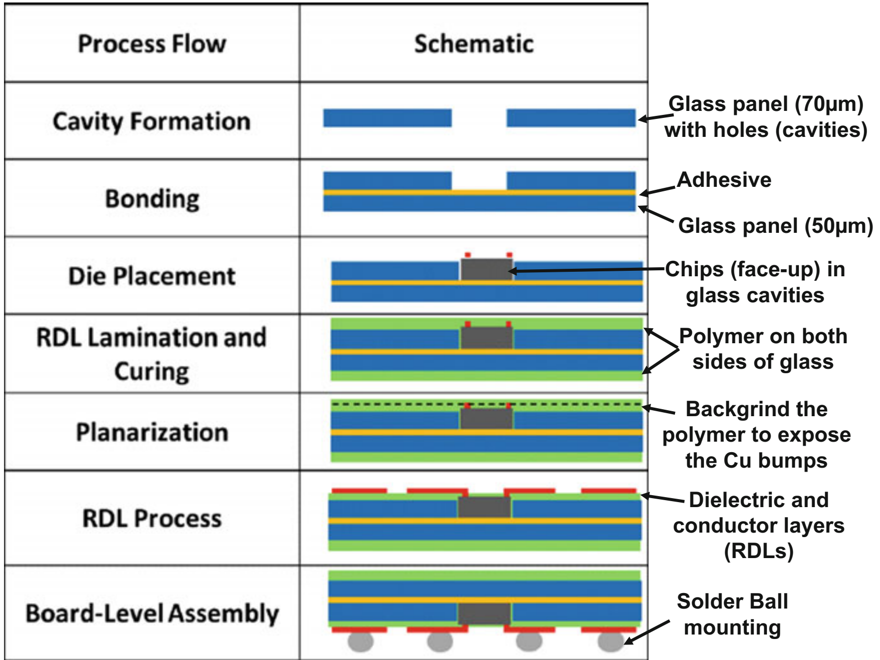

Fig. 4.10 Process flow of GIT's chips embedded in glass panel

4.4.1 Key Process Steps

Figure 4.10 shows the process flow of GIT's chips embedded in glass panel [25, 26]. First, cavities are formed on a 70 µm-thick glass panel. Then, the glass panel with cavities is bonded to another glass of 50 µm thick with adhesive as shown in Fig. 4.11a. It is followed by picking and placing the chips with Cu bumps face-up

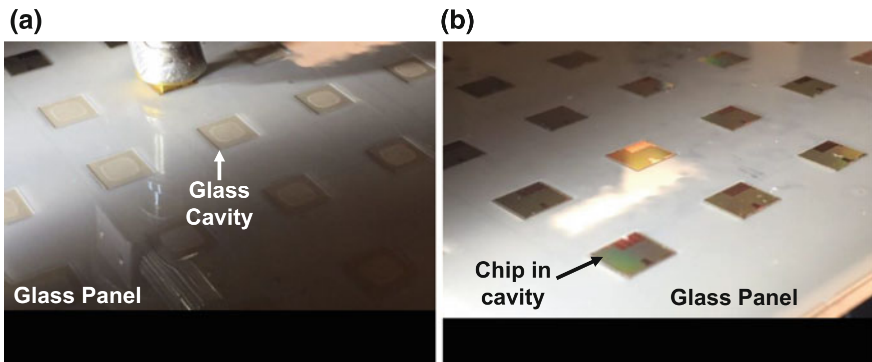

Fig. 4.11 **a** Cavities on GIT's glass panel. **b** Chips embedded in the cavities of GIT's glass panel

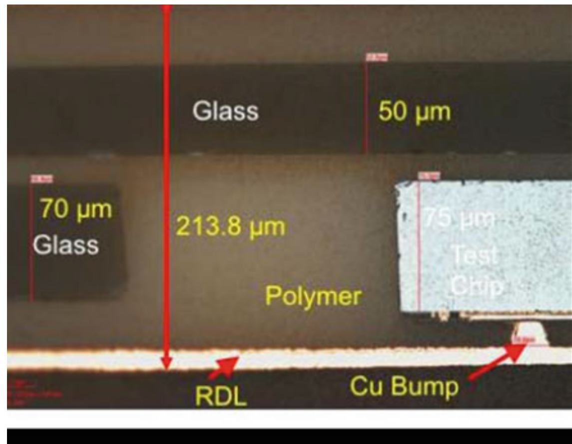

Fig. 4.12 Cross section image of GIT's chip embedded in glass panel

in the cavities as shown in Fig. 4.11b. Then apply polymer on both sides of the glass panel as shown in Fig. 4.10. Because the polymer covers the bumps. Thus, backgrinding the polymer to expose the bumps. Fabricate the dielectric and conductor layers (RDLs) and mount the solder balls. Figure 4.12 shows a typical cross section of the GIT's chips embedded in glass panel. This is the first demonstration of chips embedded in glass panel [25].

4.4.2 Reliability of Chips Embedded in Glass Panel

Reliability data such as drop test and thermal cycling test are on the way and will be published by GIT in the near future.

4.5 Summary and Recommendations

Some important results and recommendations are summarized in the following.

- Embedded chip(s) in rigid/flexible substrate/PCB will be suitable for wearable products.
- In general, chips that are embedded in a laminated rigid substrates and polyimide flexibility substrates cannot be larger than 5 mm × 5 mm, due to the thermal expansion mismatch between the silicon chip (2.5×10^{-6}/°C) and the organic/polyimide substrates (15×10^{-6}/°C – 18×10^{-6}/°C).
- For chips that are embedded in a silicon substrate, in general, the size of the chip cannot be larger than 4 mm × 4 mm (or the size of the silicon package cannot be larger than 5 mm × 5 mm). This is because of the thermal expansion

mismatch between the silicon (package) substrate (not the chip) and the PCB (18×10^{-6}/°C).

- George Institute of Technology (GIT) just demonstrated that they are able to fabricate the chips embedded in glass substrate (panel). However, making the cavities on glass and fabricating the fine line width/spacing RDLs on glass need to be mature. Also, the PCB solder joint reliability under drop and thermal cycling conditions need to be demonstrated.

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Chapter 5
FOWLP: Chip-First and Die Face-Down

5.1 Introduction

The first fan-out wafer-level packaging (FOWLP) U.S. patent was filed by Infineon on October 31, 2001 [1, 2], and the first technical papers were also published (at ECTC2006 and EPTC2006) by Infineon and their industry partners: Nagase, Nitto Denko, and Yamada [3, 4]. At that time, they called it embedded wafer-level ball (eWLB) grid array. This technology eliminates wire bonding or wafer bumping and lead frame or package substrate, and potentially leads to a lower cost, better performance, and lower profile package. Alternatively, this technology requires a temporary (reconstituted) carrier for the known good die (KGD), epoxy molding compound (EMC), compression molding, and the fabrication of the redistribution layers (RDLs). During ECTC2007, Freescale (now NXP) presented a similar technology and called it redistributed chip package [5]. IME extended the FOWLP technology to multi-die and stacked multi-die in 3D format and presented at ECTC2008 [6]. During ECTC2009, IME presented four papers on: (1) a novel method to predict die shift during compression molding [7]; (2) laterally placed and vertically stacked thin dies [8]; (3) the reliability of 3D FOWLP [9]; and (4) the demonstration of high quality and low-loss millimeter-wave passives on FOWLP [10]. In [1, 3–10], they used chip-first and die face-down [11] fan-out wafer-level processing, which will be the focus of this chapter.

During ESTC2010 and ECTC2011, NEC (now Renesas) presented a couple of papers on system-in-wafer-level package (SiWLP) [12], and “RDL-first” FOWLP [13]. Their technology requires besides the fabrication of the RDLs, wafer bumping, fluxing, flip chip assembly, cleaning, and underfills dispensing and curing, and thus is very high cost. Their potential applications are for very high-density and

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high-performance products such as supercomputers, high-end servers, telecommunications, and networking systems. Their technology is chip-last or RDL-first [11] FOWLP processing, which will be discussed in Chap. 7.

At ECTC2012, STATS ChipPAC proposed a package-on-package (PoP) for the application processor (AP) chipset with the FOWLP technology [14]. During ECTC2016, TSMC presented two papers on FOWLP: one is their integrated fan-out (InFO) wafer-level packaging for housing the most advanced AP for mobile applications [15], and the other is to compare the thermal and electrical performance between their InFO technology and the conventional flip chip on buildup package substrate technology [16]. During September 2016, TSMC put the PoP of AP with FOWLP technology into high-volume manufacturing. This is very significant since this means that FOWLP is not just only for packaging baseband, power management IC, radio frequency (RF) switch/transceiver, RF radar, audio codec, microcontroller unit, connectivity ICs, etc., it can also be used for packaging high-performance and large (>120 mm^2) system-on-chip (SoC) such as APs. TSMC used chip-first and die face-up [2, 11] FOWLP processing, which will be discussed in Chap. 6. The applications of FOWLP on PoP will be discussed in Chap. 8.

Recently, through-silicon via (TSV)-less interposer [17] to support flip chips is a very hot topic in semiconductor packaging. At ECTC2013, STATS ChipPAC proposed [18] using the fan-out flip chip-eWLB to make the RDLs for the chips to perform mostly lateral communications. During ECTC2016, ASE [19] and MediaTek [20] used a similar technology to fabricate the RDLs and showed that the TSV interposer, wafer bumping, fluxing, chip-to-wafer bonding, cleaning, and underfill dispensing and curing are eliminated. FOWLP for heterogeneous integration without TSV-interposers will be discussed in Chap. 11.

All pervious mentioned fan-out papers are using the round 200- or 300-mm wafers as the reconstituted carriers for supporting the KGDs and making the molds, RDLs, etc. (This is because of the existing equipment for fabricating the device wafers.) In order to increase the throughput, fan-out panel-level packaging (FOPLP) has been proposed. For example, starting from EPTC2011, J-Devices have been presenting their FOPLP (320 mm × 320 mm) called WFOP™ (Wide Strip Fan-Out Package) [21–23]. Starting from ECTC2013, Fraunhofer has been presenting its evaluation results on compression molding of a large-area (610 mm × 457 mm) FOPLP [24–26]. At ECTC2014, SPIL published two papers on FOPLP called P-FO, one is to develop and characterize a 370 mm × 470 mm P-FO [27] and the other is to measure their warpage [28]. One of the bottlenecks for FOPLP is the availability of panel equipment such as the spin coating, physical vapor deposition (PVD), electrochemical deposition, etching, backgrinding, and dicing for making the RDLs, molds, etc., due to the lack of the standard of panel sizes. Thus, the potential FOPLP users are unanimously calling for the panel-size industry standards. FOPLP will be discussed in Chap. 9.

5.2 Chip-First and Face-Down

FOWLP with the chip-first and die face-down processing is actually the eWLB first proposed by Infineon [1, 2] and HVM by such as STATS ChipPAC, ASE, STMicroelectronics, and NANIUM (now AMKOR). This is the most conventional method to form FOWLPs, and most FOWLP products being manufacturing today are using this method.

Figure 5.1 shows the process flow of chip-first with die face-down FOWLP. First, the device wafer is tested for known good dies (KGDs) and then singulated into individual dies. This is followed by picking up the KGDs and placing them face-down on a temporary carrier that can be round (wafer) or rectangular (panel) with a double-sided thermal release tape. Then, the reconstituted carrier with the KGDs are molded with EMC (epoxy molding compound) using the compression method + PMC (post mold cure) before removing the carrier and the double-sided tape and turning the whole reconstituted carrier (with KGDs) around. Next comes building the RDLs for signals, power, and grounds from the Al or Cu pads.

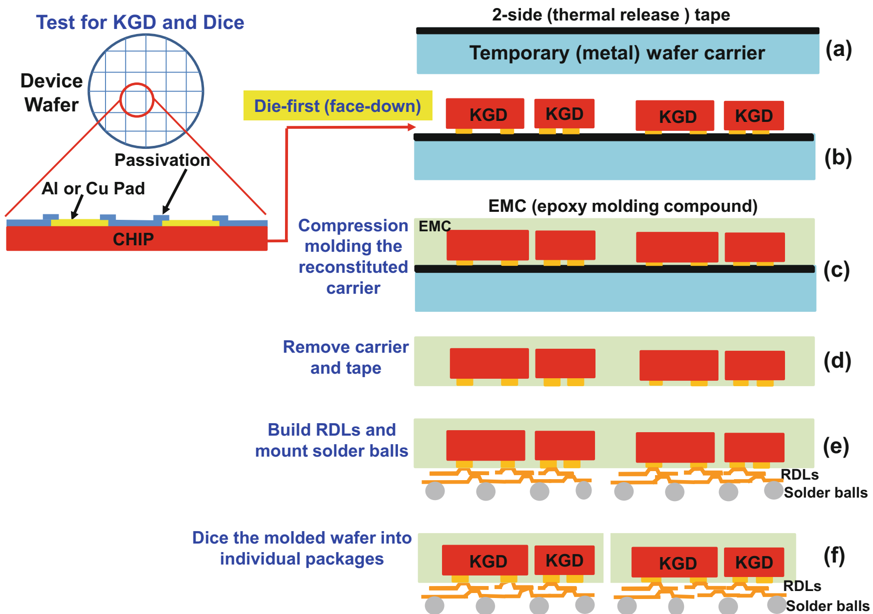

Fig. 5.1 Key process steps for chip-first and die face-down FOWLP

Finally, solder balls are mounted and the whole reconstituted carrier (with KGDs, RDLs, and solder balls) is diced into individual packages as shown schematically in Fig. 5.1.

In this chapter, the feasibility of a SiP (system-in-package) or heterogeneous integration is demonstrated by the chip-first and die face-down FOWLP [29].

5.3 Test Chips

There are two test chips (5 mm × 5mm and 3 mm × 3mm) under consideration. The layout of the 5 mm × 5mm test chip is shown in Fig. 5.2 and the fabricated chip is shown in Fig. 5.3. It can be seen that the chip sizes are 5 mm × 5 mm × 150 μm and there are 160 pads on a pitch = 100 μm (the inner rows.) The SiO_2 passivation opening of the Al pad is 50 μm and the size of the Al-pad is 70 μm × 70 μm. Figure 5.4 shows the layout and fabrication of the 3 mm × 3 mm × 150 μm chip. It can be seen that there are 80 pads on a 100 μm pitch (the inner rows.) The pad condition is the same as that of the 5 mm × 5 mm chip.

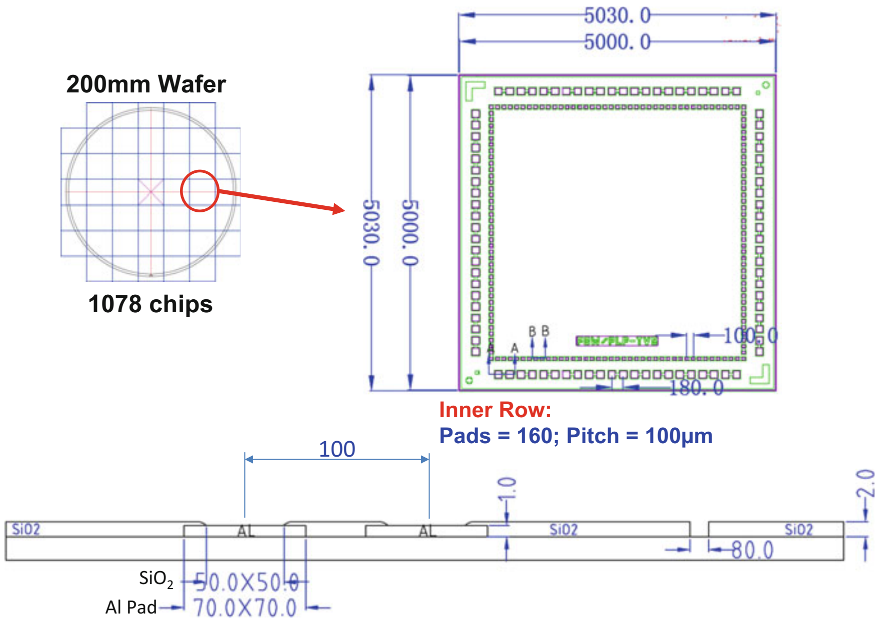

Fig. 5.2 Layout of the 5 mm × 5 mm test chip

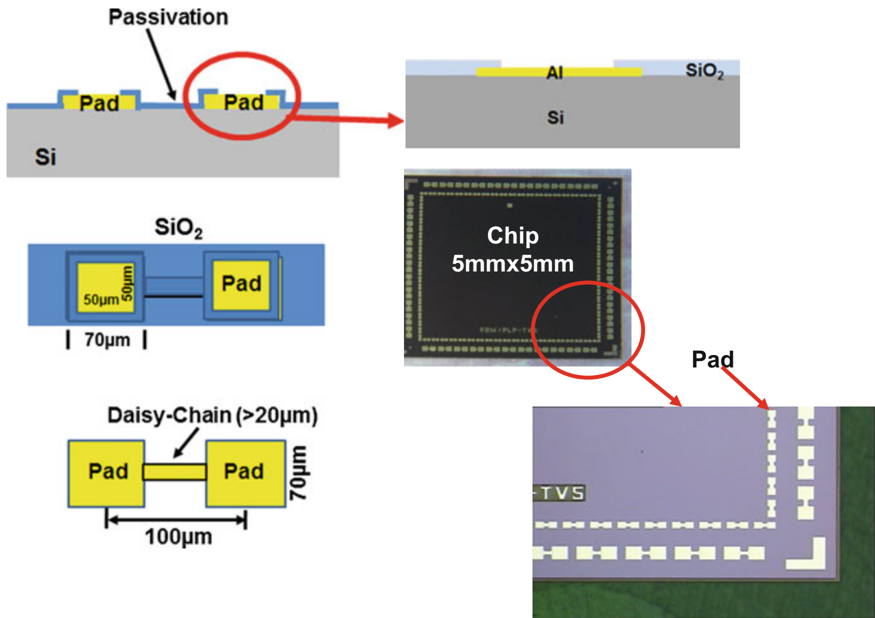

Fig. 5.3 Image of the 5 mm × 5 mm test chip

5.4 Test Package

Figures 5.5 and 5.6 schematically show the test package under consideration. It can be seen that the reconstituted carrier is a 300 mm wafer, Fig. 5.5, and there are 629 test packages with a pitch = 10.04 mm. The layout of the test package is shown in Figs. 5.5 and 5.6. The dimensions of the test package are: 10 mm × 10 mm and there are 4 chips within the package, one 5 mm × 5 mm chip, and three 3 mm × 3 mm chips. The spacing (gap) between the large chip and the smaller chips is 100 μm. The dimensions of a typical pad on the test package are shown in Fig. 5.6. Also, there are 4 capacitors (0402).

Figure 5.7 schematically shows the cross-sectional view of the test package. It can be seen that there are 2 RDLs and the thickness of RDL1 is 3 μm and RDL2 is 7.5 μm. The line width and spacing of RDL1 and RDL2 are 10 μm/10 μm and 15 μm/15 μm, respectively. The dielectric layer thickness of DL1 and DL2 is 5 μm and of DL3 is 10 μm. The via (V_{C1}), through the first dielectric layer (DL1), connecting the Cu contact pad of the test chip to the first RDL (RDL1) is 20–30 μm in diameter. The pad diameter on the RDL1 is 55 μm, which is connected to RDL2

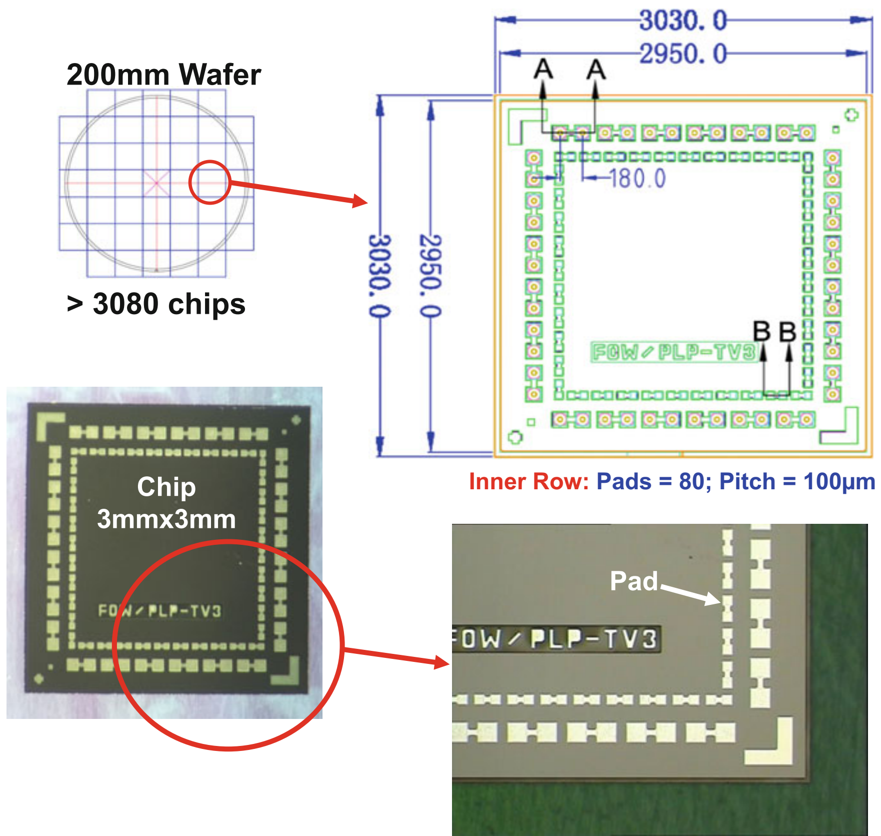

Fig. 5.4 Layout and images of the 3 mm × 3 mm test chip

through the via (V_{12}) with a diameter of 35–45 μm. Finally, 220 μm Cu pads are formed on RDL2 for the solder ball mounting. The opening of the passivation (DL3) is 180 μm. The solder ball size is 200 μm and ball pitch is 0.4 mm.

5.5 The Temporary Carrier

The temporary (round or rectangular) carrier as shown in Fig. 5.1a can be made from silicon, glass, or metal and is reusable. Their thickness and material properties are shown in Table 5.1. Since the thermal expansion of coefficient (TEC) of EMC is about 10×10^{-6}/°C, thus the stainless steel metal carrier (10.6×10^{-6}/°C) is chosen for production. Another reason is that metal is not easy to be broken when it

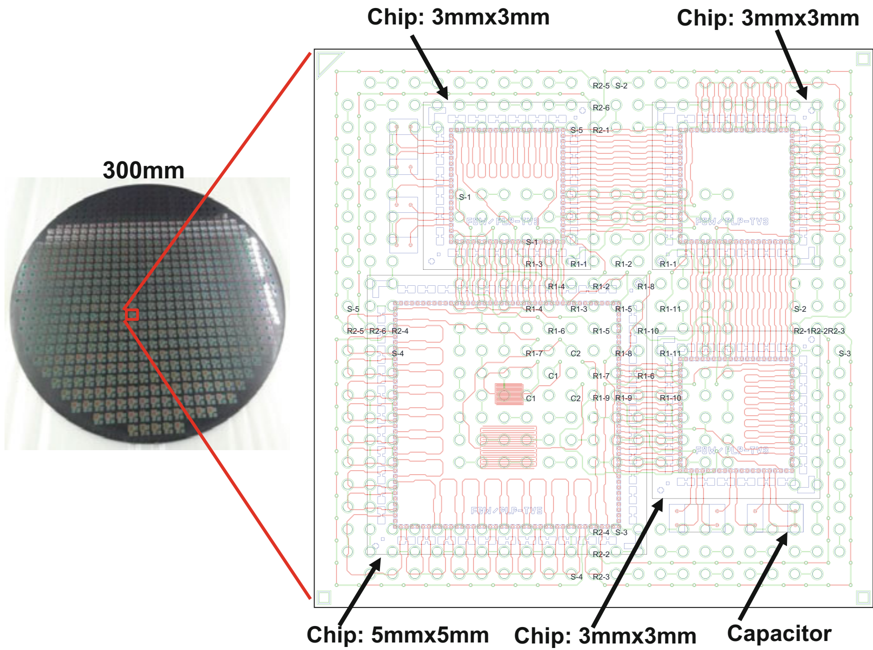

Fig. 5.5 Layout of the reconstituted wafer and test package

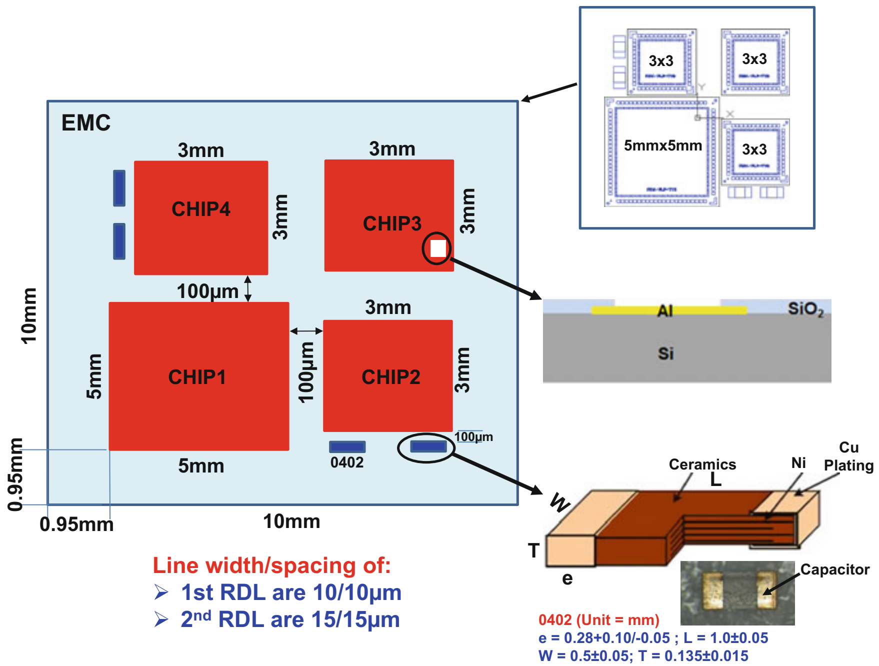

Fig. 5.6 Layout and dimensions of the test package and capacitor

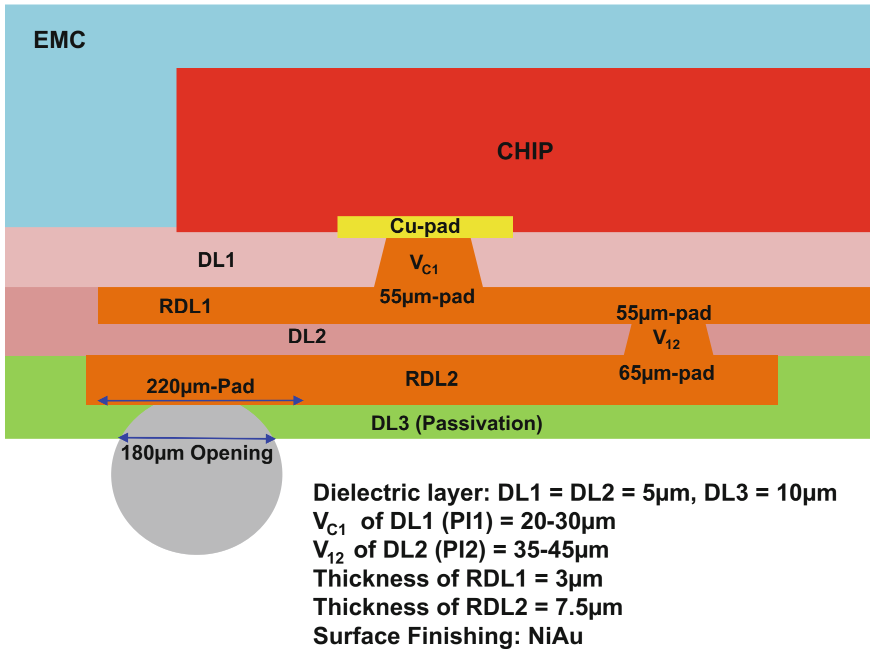

Fig. 5.7 Schematic of the cross section of the test package

is cleaned and reused like the silicon and glass. Also, a thicker metal (1–1.5 mm) carrier can increase the stiffness and is more effective to resist to bending (warpage) of the reconstituted carrier during pick and place of the KGDs and compression molding and PMC of the EMC.

5.6 The 2-Side Thermal Release Tape and Pick and Place

As mentioned earlier, most packages manufactured by the FOWLP (or eWLB) are chip-first and die face-down processing and a two-side thermal release tape as shown in Fig. 5.1a is needed for bonding and debonding the reconstituted carrier. The most commonly used tape is the REVALPHA provided by Nitto Denko as shown in Fig. 5.8. It can be seen that this tape consists of 5 different layers; (1) the top (0.038 mm) and bottom (0.075 mm) release liners; (2) the pressure-sensitive adhesive layer (0.01 mm); (3) the polyester film (0.1 mm), and (4) the thermal release adhesive layer (0.048 mm). This tape is bonded (by peeling off the release

Table 5.1 Carrier material and thickness

Carrier material and thickness	Thermal expansion coefficient (10^{-6}/°C)	Young's modulus (GPa)	Poisson's ratio
Silicon (0.76 mm)	2.6	168	0.28
Glass-1 (0.76 mm)	3.2	73.6	0.3
Glass-2 (1 mm)	7.6	69.3	0.3
Stainless Steel 420 (1.5 mm)	10.5	200	0.3

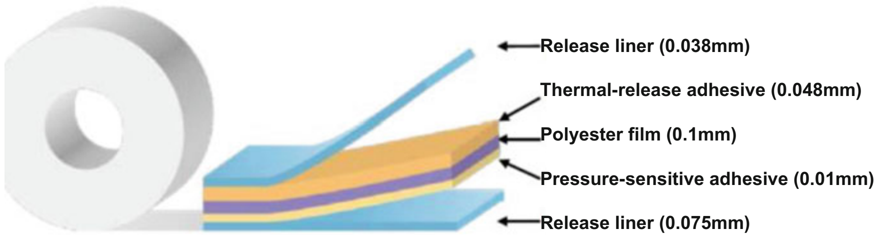

Fig. 5.8 Nitto Denko's REVALPHA tape

liner) to the metal carrier at room temperature. Then, peel off the other release liner and pick and place the KGDs (face-down) on top of the thermal release adhesive as shown in Fig. 5.1b. The debonding temperature of the carrier is 170 °C.

5.7 EMC and Dispensing

The molding of FOWLP is by the compression method with EMC. For chip-first and die face-down FOWLP, the curing temperature of the EMC must be lower than the release temperature of the double-sided tape. There are at least two forms of EMC, namely liquid and solid. The advantages of liquid EMC are better handling, good flowability, less voids, better fill, and less flow marks. The advantages of solid EMC are less cure shrinkage, better stand-off, and less die drift. For chip-first FOWLP, high filler content ($\geq$ 85%) EMC will shorten the time in mold, lower the mold shrinkage, and reduce the mold warpage.

Uniform filler distribution and filler size of the EMC will reduce flow marks/fill and enhance flowability. For example, the filler content (wt.%), maximum filler size, compression mold condition, post mold cure, Tg, and bending stiffness of EMC by Sumitomo (solid) are 90, 55 µm, 7 m/125 °C, 1 h/150 °C, 170 °C, and 30GPa, respectively, and by Nagase (liquid), 85, 25 µm, 10 m/125 °C, 1 h/150 °C, 150 °C, and 19GPa, respectively. In this chapter Nagase's liquid EMC R4507 will be used and the material properties are shown in Table 5.2.

Table 5.2 Nagase liquid epoxy molding compound

Item	R4507
Filler content (%)	85
Filler to cut (μm)	25
Filler average size (μm)	8
Specific gravity	1.96
Viscosity (Pa.s)	250
Flexural Modulus (GPa)	19
Tg (DMA) (°C)	150
CTE1 (ppm/K)	10
CTE2 (ppm/K)	41

- High flowability as suitable for large surface areas and thin film molds
- Liquid at room temperature and able to be dispensed, and dust free as suitable for clean room environments
- Capable of low temperature form molding (125 °C)
- Delivers low reflection in large surface area molds with low stress design
- High reliability
- High purity
- Low α line

Figure 5.9a shows the dispensing of the liquid EMC in a circular pattern on the reconstituted carrier with KGDs. It can be shown in Sect. 6.8.3 that with the circular pattern, there will be less and shorter flow marks.

5.8 Compression Molding and PMC

Due to the large size of the reconstituted wafer or panel, the conventional transfer molding method won't work and the compression molding method is used. After EMC dispensing, it is followed by the compression molding as shown in Fig. 5.1c and Fig. 5.9b. The KOZ (keep-out-zone) method is used and the mold cap diameter is 295 mm (2.5 mm clearance from the 300 mm glass carrier wafer edge). The metal carrier with dies attached is fixed onto the top mold chase by vacuum as shown in Fig. 5.9b. The dispensed EMC on a releasing film is placed on the bottom plunger. After a few experiments, the optimal compression molding parameters are: temperature = 125 °C, pressure = 45 kg/cm^2, time = 10 min, and removing trap air before compression molding. It is followed by post mold cure (PMC) with a temperature = 150 °C, time $\geq$ 60 min, and a dead weight = 15 kg for a better warpage control. Then, it is followed by debonding the metal carrier and peeling off the tape as shown in Fig. 5.1d.

Figure 5.10 shows a typical reconstituted wafer with the chips embedded by the EMC by using compression method and PMC. It can be seen from Fig. 5.10d that those 4 chips are properly fabricated. The total thickness of the reconstituted wafer

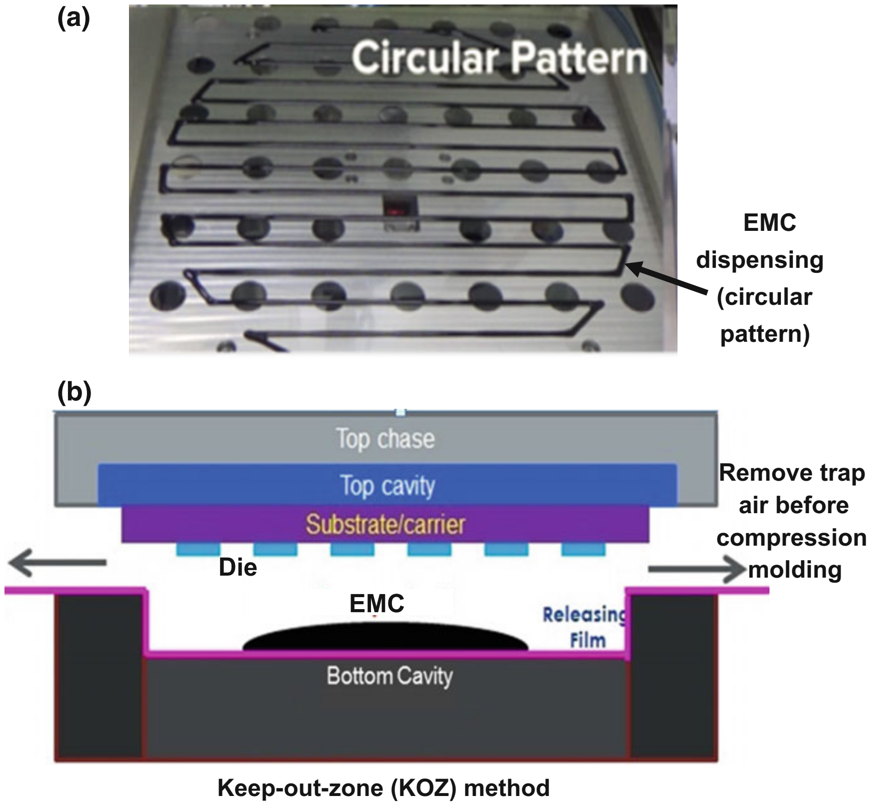

Fig. 5.9 **a** EMC dispensing. **b** Compression molding

is about 250 μm with 100 μm-thick EMC above the backside of the chips with 150 μm thick.

Inspections for molding voids are carried out by C-mode scanning acoustic microscopy (C-SAM). In order to balance the resolution and signal penetration depth, a transducer of 75 MHz is selected for the voids observation. After a couple of parametric studies, there is not any void in the optimal wafers.

5.9 RDL

5.9.1 Debonding the Metal Carrier

In most eWLBs or chip-first and die face-down FOWLP, the total thickness of the reconstituted wafer is ≥ 450 μm. Thus, right after debonding the carrier and peeling off the tape, it is followed by building the RDLs and mounting the solder balls.

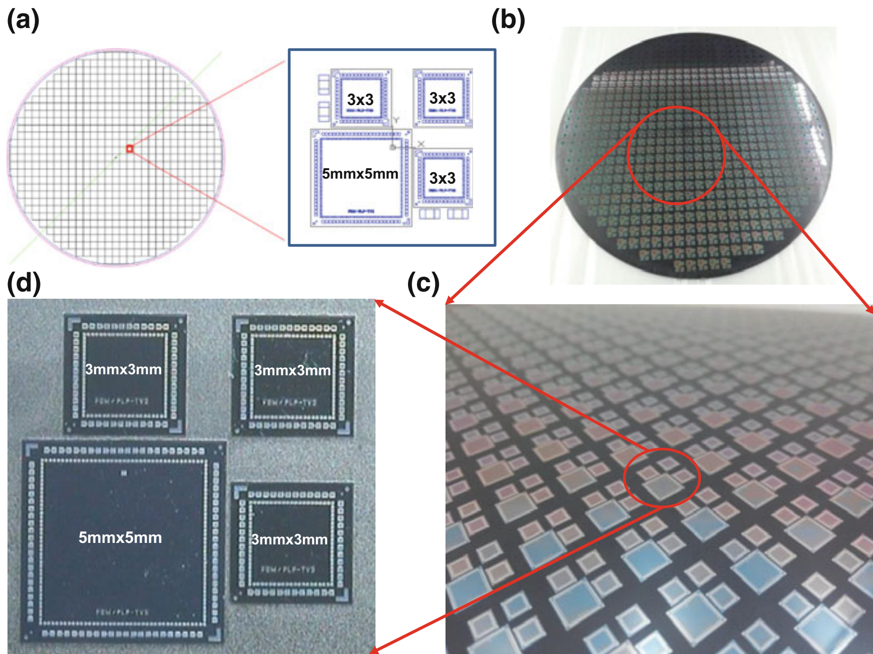

Fig. 5.10 Molded reconstituted wafer. **a** Layout of the SiP. **b** Molded reconstituted wafer. **c** Closed-up of the molded reconstituted wafer. **d** Closed-up of the SiP without capacitors

However, in this study, since we would like to save the EMC materials and have a very low-profile package, the total thickness of our reconstituted wafer is only 250 μm. Thus, the reconstituted wafer is too fragile to fabricate the RDLs and mount the solder balls.

5.9.2 *Temporary Bonding of Another Glass Carrier*

One of the solutions is to attach the reconstituted wafer on another temporary glass wafer with a coated LTHC (light-to-heat conversion) layer (before removing the metal carrier) as shown in Fig. 5.11a. It is followed by making the RDLs as shown in Fig. 5.11c with the method report in [29, 30]. Figure 5.12 shows the line width and spacing of the first RDL. It can be seen that the line width is slightly (10.44 μm) larger than the designed value and the spacing is slightly (9.5 μm) smaller than the designed value. This could be due to the etching of the Ti seed layer.

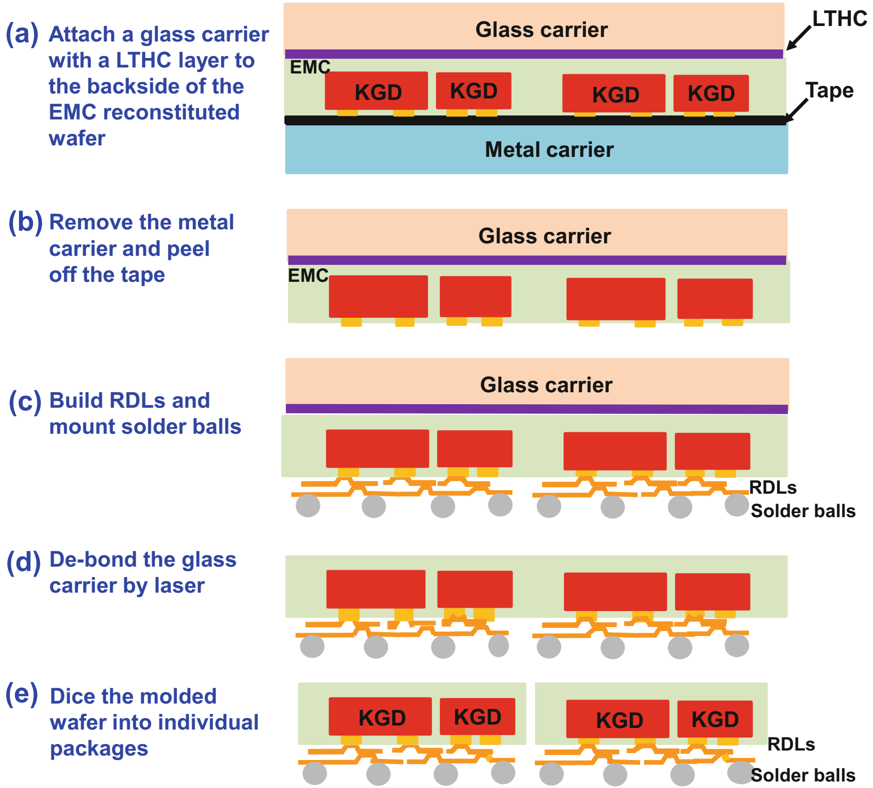

Fig. 5.11 Key process for fabricating the RDLs and solder balls

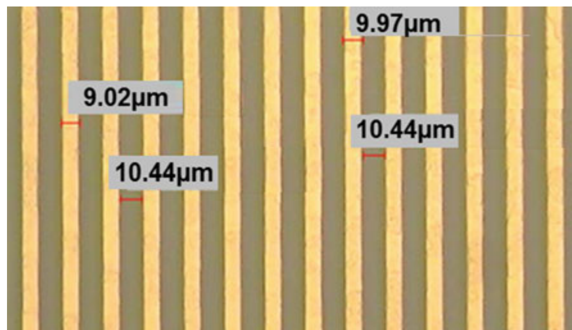

Fig. 5.12 Line width and spacing of RDL1

5.10 Solder Ball Mounting

There are two different stencils for the solder ball mounting, one is for stencil printing the flux and the other is for stencil mounting the solder balls. The solder (Sn3 wt.%Ag0.5 wt.%Cu) balls (200 μm diameter) used are from Indium and are on 0.4 mm pitch. The peak temperature for solder reflow is 245 °C.

5.11 Final Debonding

The de-bonding of the glass carrier as shown in Fig. 5.11d is by scanning a laser (355 nm DPSS Nd: YAG UV laser source is used) from the glass carrier side. The laser spot size is 240 μm, the scanning speed is 500 mm/s and the scanning pitch is 100 μm. When the LTHC layer "sees" the laser light, it converts into powders and the glass carrier is easily removed. It is followed by chemical cleaning. Figure 5.13 shows the reconstituted wafer without any carrier and a closed-up on one of the package. It can be seen that there are 4 chips and 4 capacitors in a package and they are properly fabricated. The reconstituted wafer is diced, as shown in Fig. 5.11e, into individual packages as shown in Fig. 5.14. It can be seen from the x-ray image that the chips and the capacitors are properly fabricated. Also, the vias (V_{c1} and V_{12}), RDLs (RDL1 and RDL2) and solder balls are properly done.

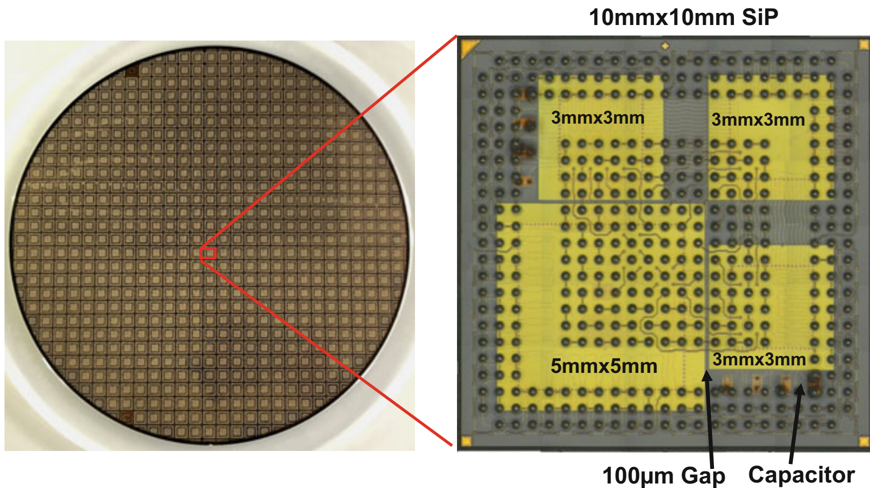

Fig. 5.13 Final debonded reconstituted wafer and closed-up of an individual package

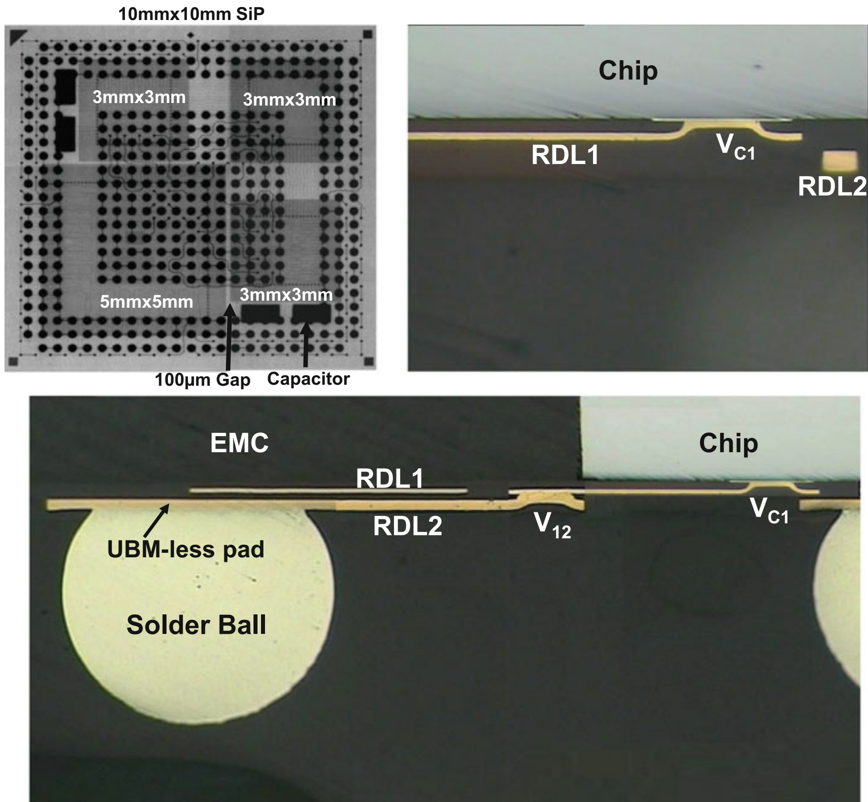

Fig. 5.14 X-ray image, RDLs, and solder balls of an individual package

5.12 Summary and Recommendations

FOWLP with chip-first and die face-down has been presented in this chapter. Some important results and recommendations are summarized as follows.

- The feasibility of a heterogeneous integration of 4 chips and 4 capacitors has been demonstrated.
- There is not visible C-SAM void in the optimal reconstituted molded wafer.
- In order to have a low-profile and less EMC (low-cost) package, the thickness of the reconstituted molded wafer without the temporary carrier is about 250 µm.
- The price we have to pay is to attach the reconstituted molded wafer to another glass wafer with a LTHC layer, then perform the RDL and solder ball fabrication. After that, debond the glass wafer by laser. In this case, including the solder ball, the total thickness of the final package is <450 µm.

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Chapter 6
FOWLP: Chip-First and Die Face-Up

6.1 Introduction

The design, materials, process, fabrication, and reliability of fan-out wafer-level packaging (FOWLP) with chip-first and die face-up method are presented in this chapter. Emphasis is placed on the issues and their solutions (such as reconstituted carrier, die-attach film placement, pitch compensation, die shift, epoxy molding compound dispensing, compression molding, warpage, and Cu revealing) during the fabrication of a very large test chip (10 mm × 10 mm × 150 μm) and test package (13.47 mm × 13.47 mm), and three redistribution layers (RDLs) with the smallest line width/spacing = 5 μm/5 μm. The FOWLP test package on a six-layer printed circuit board (PCB) is subjected to thermal cycling and drop tests. Recommendations of process integration and guidelines on FOWLP with chip-first and die face-up are provided.

6.2 Fan-Out of Chip Circuitries in Semiconductor Packaging

One of the major functions of semiconductor packaging is to fan-out the circuitries from the chip and talk to circuitries from another chip [1]. On July 17, 1967, Kauffman of The Jade Corporation [2] proposed the use of a lead frame to fan-out the circuitries from a chip. Today, just about all electronic products use lead frames such as the gull-wing lead [e.g., plastic quad flat pack (PQFP)], J-lead [e.g., plastic leaded chip carrier (PLCC)], and/or dual in-line package (DIP) to fan-out the circuitries from a chip to a PCB.

On March 2, 1992, Paul Lin, Mike McShane, and Howard Wilson of Motorola proposed [3] the use of an organic carrier or substrate with area-array solder balls (instead of lead frames) to fan-out the circuitries from a chip to a PCB, which is

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J. H. Lau, *Fan-Out Wafer-Level Packaging*,
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called a plastic ball grid array (PBGA) package. Amkor (1993) led the OSATs (outsourced semiconductor assembly and test providers) to license this packaging technology from Motorola—and the BGA era began.

On July 13, 1998, Peter Elenius and Harry Hollack of Flip Chip Technologies proposed [4] the use of RDLs to fan-in the circuitries from the original peripheral bond pads of a chip on a wafer and of solder balls to connect to a PCB without underfill. The packages made by the fan-in wafer-level packaging (WLP) are called wafer-level chip scale package (WLCSP) and one of the most famous is UltraCSP developed and patented by Flip Chip Technologies [5]. In 2001, again Amkor led the OSATs and foundries to license the UltraCSP, and the WLP era began.

On October 31, 2001, Harry Hedler, Thorsten Meyer, and Barbara Vasquez of Infineon proposed [6] the use of RDLs to fan-out the circuitries from the metal pad of the chip on a wafer and solder ball to the metal pads on a PCB without underfill. (At that time, they called it embedded wafer-level ball (eWLB) grid array [7, 8]. Today, we called it FOWLP.) Some of the RDLs having a portion that extends beyond (fan-out) the edges of the chip.

6.2.1 Advantages of FOWLP over PBGA

The advantages of FOWLP over PBGA packages with solder bumped flip chip are [9]: (1) lower cost, (2) lower package profile, (3) eliminating the substrate, (4) eliminating the wafer bumping, (5) eliminating the flip chip reflow, (6) eliminating the flux cleaning, (7) eliminating the underfill, (8) better electrical performance, (9) better thermal performance, and (10) easier to go for system-in-package (SiP) and 3D IC packaging [10, 11].

6.2.2 Advantages of FOWLP over WLCSP

The advantages of FOWLP over fan-in WLP or WLCSP are [9]: (1) the use of known good die (KGD), (2) better wafer-level yield, (3) using the best of silicon, (4) single or multichip, (5) embedded integrated passive devices, (6) more layer of RDLs, (7) higher pin counts, (8) better thermal performance, (9) easier to go for SiP and 3D IC packaging, and (10) higher PCB-level reliability.

6.3 FOWLP with Chip-First and Die Face-Up

As mentioned before, basically there are two methods to form (build) the FOWLP [12]. One is chip-first and the other is chip-last [13, 14]. For the chip-first method, there are two options: face-down (die-down) [15–22] and face-up (die-up) [23–30].

FOWLP with chip-first and die face-down has been presented in Chap. 5. In this chapter, we will present the FOWLP with chip-first and die face-up. The test chip, test package, assembly process on the device (test) wafer, assembly process on the reconstituted wafer, EMC (epoxy molding compound) dispensing, compression molding and PMC (post mold cure), warpage, Cu reveal, RDLs, debonding, solder ball mounting, PCB assembly, thermal cycling test, and drop test will be presented and discussed [31].

6.4 Test Chip

Figure 6.1 shows the test chip under consideration. The layout of the test chip is shown in Fig. 6.1a and the fabricated chip is shown in Fig. 6.1b–d. It can be seen that the chip sizes are 10 mm × 10 mm × 150 μm and there are 1988 pads with a minimum pitch = 150 μm staggered. The polyimide (PI) opening of the Al pad is 40 μm in diameter and is 5 μm-thick. (Later on, because of the Cu smear under backgrinding of the epoxy molding compound (EMC) to expose the Cu contact

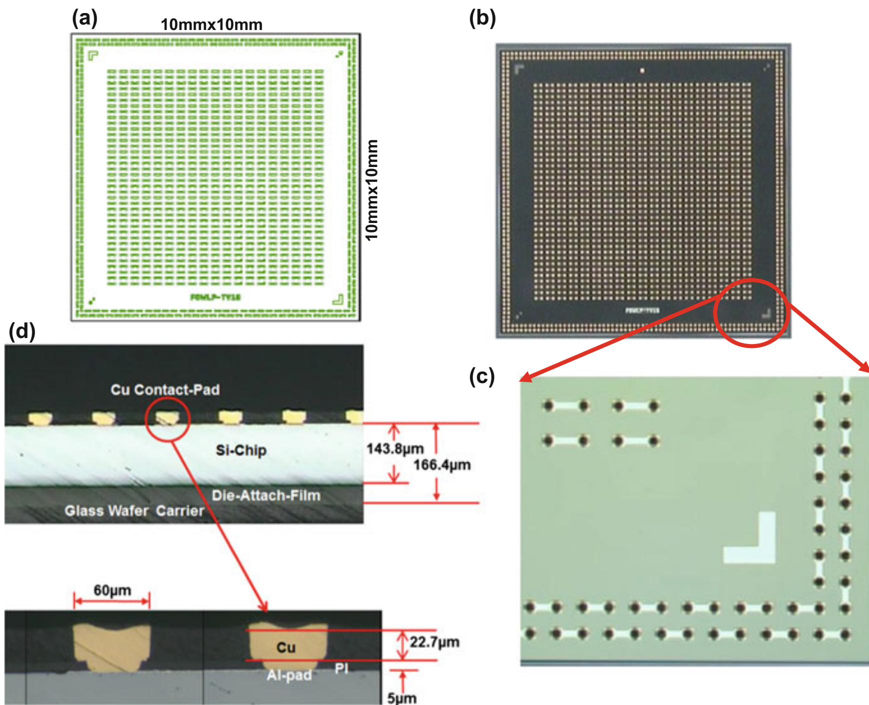


Fig. 6.1 Test chip. **a** 10 mm × 10 mm test chip layout. **b** The fabricated test chip. **c** A close-up look of the test chip. **d** Cross-section image of the test chip

pad, the thickness of the PI has been increased to slightly taller than the Cu contact pad.) The SiO_2 passivation opening of the Al pad is 50 μm × 50 μm and the size of the Al pad is 70 μm × 70 μm. The Cu contact pad is 60 μm in diameter and is 25 μm tall from the Al pad.

6.5 Test Package

Figure 6.2 schematically shows the test package under consideration. It can be seen that the reconstituted wafer is a 300 mm glass wafer, Fig. 6.2a, and there are 325 test packages with a pitch = 13.46 mm. The layout of the test package is shown in Fig. 6.2b. The dimensions of the test package are: 13.42 mm × 13.42 mm as shown in Fig. 6.2c. Thus, a package/chip area ratio = 1.8 and the test package is 1.71 mm all around larger than the test chip. The dimensions of a typical pad on the test package are shown in Fig. 6.2d.

Figure 6.3 schematically shows the cross-sectional view of the test package. It can be seen that there are 3 RDLs and the thickness of RDL1, RDL2, and RDL3 is 3 μm. The line width and spacing of RDL1, RDL2, and RDL3 are, respectively, 5 μm/5 μm, 10 μm/10 μm, and 15 μm/15 μm. The dielectric layer thickness of

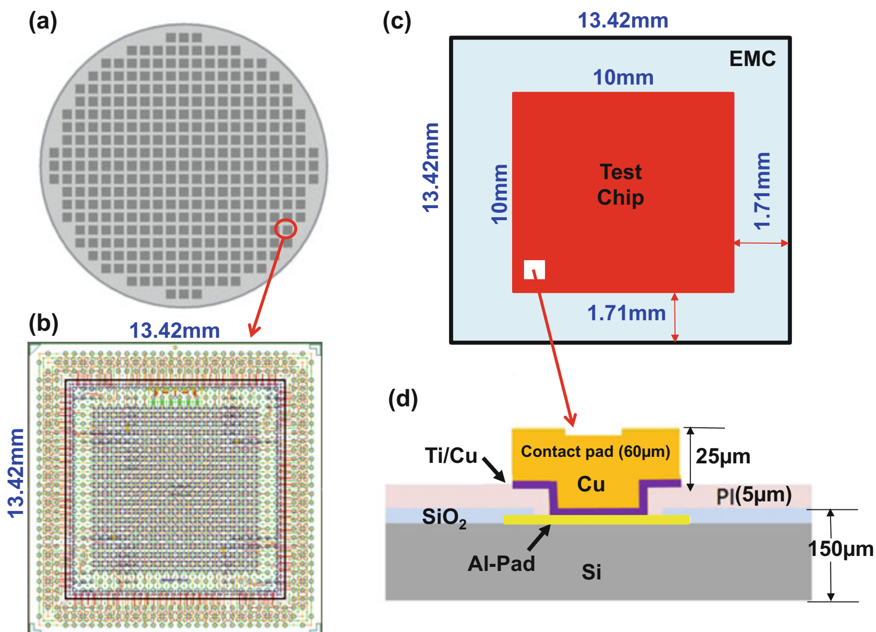


Fig. 6.2 Test package. **a** Schematic of the test packages on a 300 mm reconstituted wafer. **b** Layout of the test package. **c** Schematic of the test package (13.42 mm × 13.42 mm) for the test chip. **d** A schematic of the cross section of a pad on the test chip

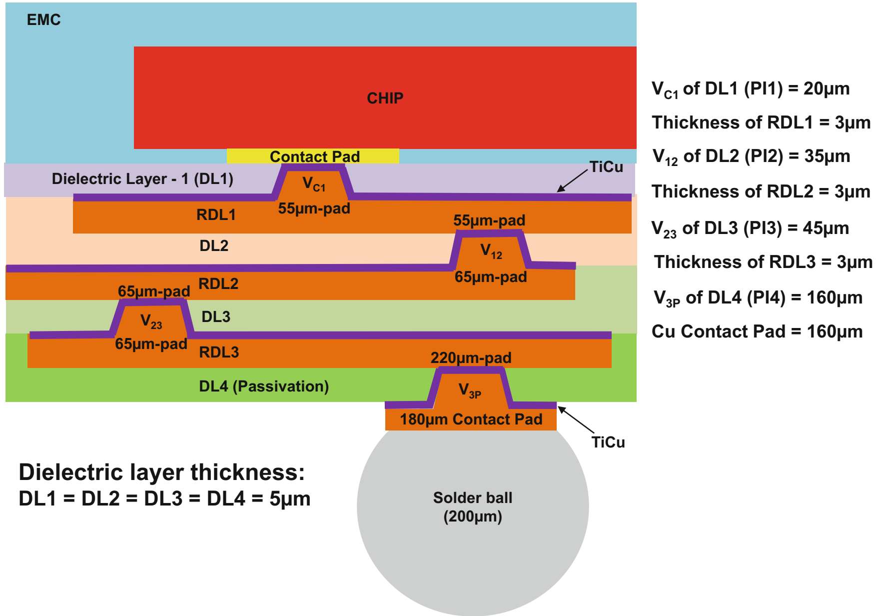


Fig. 6.3 Schematic of the cross section of the test package with conventional solder ball attachment

DL1, DL2, DL3, and DL4 is 5 µm. The via (V_{C1}), through the first dielectric layer (DL1), connecting the Cu contact pad of the test chip to the first RDL (RDL1) is 20 µm in diameter. The pad diameter on the RDL1 is 55 µm, which is connected to RDL2 through the via (V_{12}) with a diameter of 35 µm. Similarly, the pad diameter on the RDL2 is 65 µm, which is connected to RDL3 through V_{23} with a diameter of 45 µm. Finally, 220 µm pads are formed on the bottom side of RDL3 and a V_{3P} with a diameter of 160 µm is formed through the passivation (DL4), a UBM (under bump metallurgy) and a 180-diameter Cu contact pad is formed for the solder ball mounting. Figure 6.4 shows the other case with UBM-less/Cu pad for a solder ball. In this case, 220 µm Cu pads are formed on RDL3 for the solder ball mounting. The thickness of RDL3 is 7.5 µm. The thickness of the passivation (DL4) is 10 µm and the passivation opening is 180 µm. For both cases, the solder ball size is 200 µm and ball pitch is 0.4 mm.

Figure 6.5 shows the partial daisy-chain design of the RDLs of the test package. Basically, there are three objectives of the layout of the daisy-chain of the RDLs: (1) to capture the delamination of the daisy-chain trace; (2) to capture the failure of the daisy-chain trace through the vias, and (3) to identify the failure of the solder joint (after they are assembled on the PCB), during drop and thermal cycling tests.

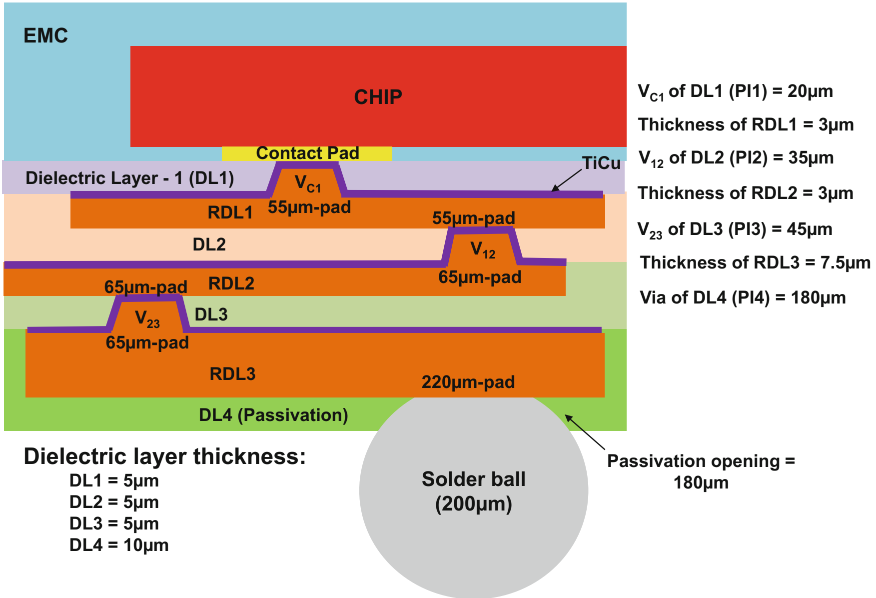


Fig. 6.4 Schematic of the cross section of the test package with UBM-less Cu pad solder ball attachment

6.6 Chip-First (Die Face-Up) FOWLP Assembly Process

Figure 6.6 shows schematically the FOWLP with chip-first and die face-up assembly process. Basically, works must be done on the device (test chip) wafer (Fig. 6.6a, b) and the reconstituted (temporary carrier) wafer (Fig. 6.6c–h).

6.7 Assembly on the Test Chip Wafer

First, the test chip wafer must be modified by sputtering a Ti/Cu as a bottom layer of under bump metallurgy (UBM) with a physical vapor deposition (PVD) on the Al (or Cu) pad, and a Cu contact pad (for building the RDLs later) is electroplated on the UBM, as shown in Fig. 6.6a. This step is followed by spin coating a polymer on top of the test chip wafer and laminating (at ~70 °C) with a (~20 μm) die-attach film (DAF) provided by Hitachi (Fig. 6.7 and Table 6.1) at the bottom of the test chip wafer as shown in Fig. 6.6b. The test chip wafer is then diced into individual chips.

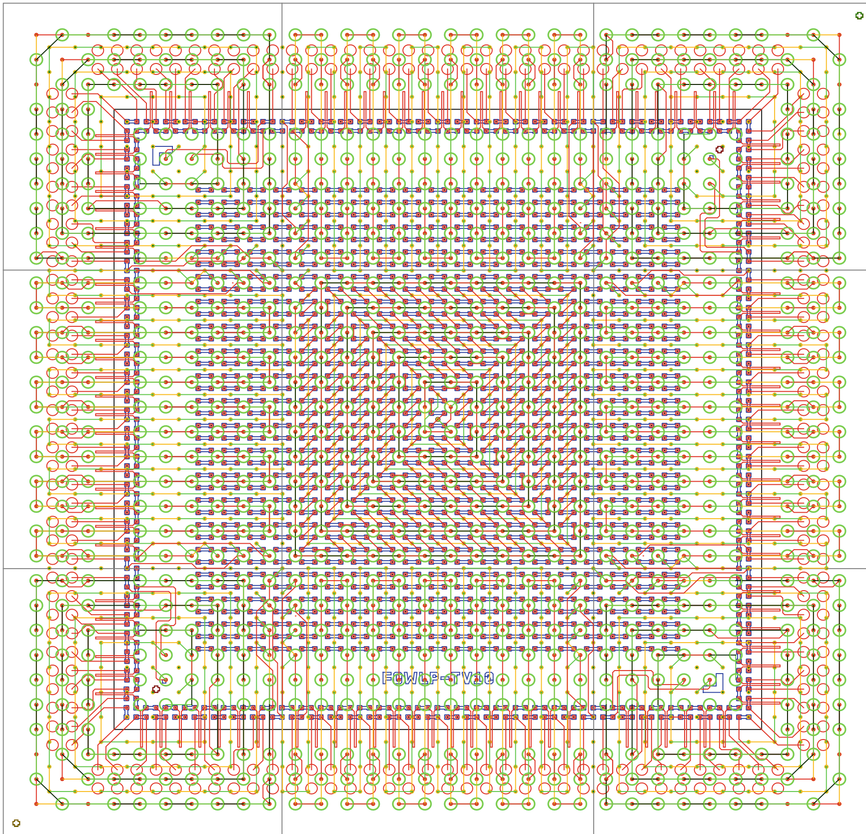


Fig. 6.5 Daisy-chain design of the RDLs of the test package

6.8 Assembly on the Reconstituted Wafer

Figures 6.6c through 6.6h show the FOWLP with chip-first and die face-up process steps on the reconstituted wafer and they will be briefly mentioned below.

6.8.1 Glass Carrier Wafer and LTHC Layer

A light-to-heat conversion (LTHC) layer (about 1 μm) provided by 3M (Table 6.2) is spin coated onto the temporary glass carrier wafer as shown in Figs. 6.6c and 6.8a. In this study, three different glasses with thermal coefficient of expansion (TCE) = 3.26×10^{-6}/°C, 7.6×10^{-6}/°C, and 8.1×10^{-6}/°C are considered. The thickness of the one with 3.26×10^{-6}/°C is 780 μm and with 7.6×10^{-6}/°C and 8.1×10^{-6}/°C is 1 mm.

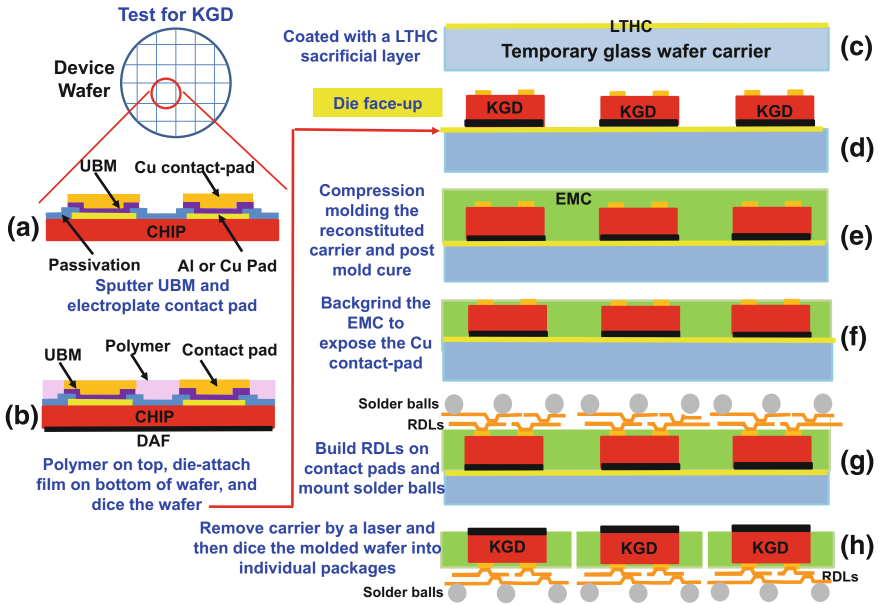


Fig. 6.6 FOWLP with chip-first and die face-up process. **a** Sputter UBM and ECD of Cu contact pad. **b** Polymer on top, die-attach film on bottom of wafer, and dice the wafer. **c** Spin coat a LTHC layer on top of the temporary glass wafer carrier. **d** Pick and place the die face-up on the LTHC layer carrier. **e** Compression mold the reconstituted wafer and post mold cure. **f** Backgrinding the EMC to expose the Cu contact pad. **g** Build RDLs on contact pads and mount solder balls. **h** Remove the carrier and dice the reconstituted wafer into individual packages

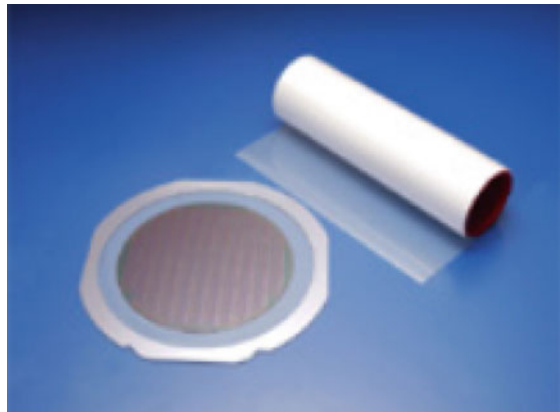


Fig. 6.7 Die-attach film (DAF) provided by Hitachi

Table 6.1 Material properties of the DAF

Item			Unit	FH-9011	Test method
Adhesive thickness			μm	10, 20, 25, 40	–
DC tape properties	Exposure doze		mJ/cm^2	150–400	–
	Adhesive strength between DCT and DBF	Before UV	N/25 mm	1.4	–
		After UV	N/25 mm	<0.1	–
Wafer laminating temp.			°C	60–80	–
Die bonding condition	Temp.		°C	100–160	–
	Load		MPa	0.05–2.0	–
Elastic modulus (35 °C)			MPa	200	DMA
Tg			°C	180	TMA
Die shear strength (260 °C)			N/chip	>100	5 × 5 mm chip

Wafer backside lamination: 60–70 °C
Curing: 125 °C for one hour

Table 6.2 Characteristics of the LTHC material

Product description	3M™ Light-To-Heat Conversion Release Coating (LTHC) ink is a solvent-based coating applied using a spin coating method. This coating forms the light-to-heat conversion layer on a glass substrate for 3M™ Wafer Support System
Features and benefits	Enables stress-free, room temperature debonding of adhesive
Typical properties note	The following technical information and data should be considered representative or typical only and should not be used for specification purposes
Base resin	Acrylic
Color	Black thixotropic liquid
Specific gravity	1.00
Solid	11%
Solvent	• Methoxy-2-propyl acetate • Butoxy ethanol
Flash point	45 °C
General information	Standard container is 20 L Stainless steel drum (UN: 1A1/X/250)
Storage	Store this product under normal conditions of 5–35 °C in original container for maximum storage life
Shelf life	Six months after the date of shipping from 3M
Method of usage	• Product must be stirred/mixed at 600–700 RPM for 12 h before usage • Product must be stirred continuously while in use

6.8.2 Pick and Place

The individual test chips are picked and placed face-up on the LTHC carrier as shown in Figs. 6.6d and 6.8a. In order to cure the DAF, a bonder with temperature and pressure such as the multipurpose high-accuracy NUCLEUS is used. The DAF process is carried out at 120 °C (both bond-head and bond-stage) with the bond force of 2 kg for 2 s. Thus, the reconstituted wafer will expand during chips pick and place. The *X* and *Y* pitch offset (the measured pitch subtract from the designed pitch) of chips are plotting against the column and row and shown in Fig. 6.9. It can be seen that the chip placement offsets can be as large as ±100 µm. However, during patterning/photolithography of the RDLs, it is operated at room temperature. Thus, pitch compensation due to the DAF heating is needed and can be calculated by the following equation:

$$P_{\mathrm{A}} = P_{\mathrm{R}} + \alpha_{\mathrm{L}} \Delta T$$

where P_{A} is die-attach pitch, P_{R} is the designed RDL pitch, α_{L} is the linear thermal coefficient of expansion of the glass carrier, ΔT is the temperature difference between DAF curing temperature and RDL patterning/photolithography temperature. The *X* and *Y* pitch offset of chips after pitch compensation are shown in

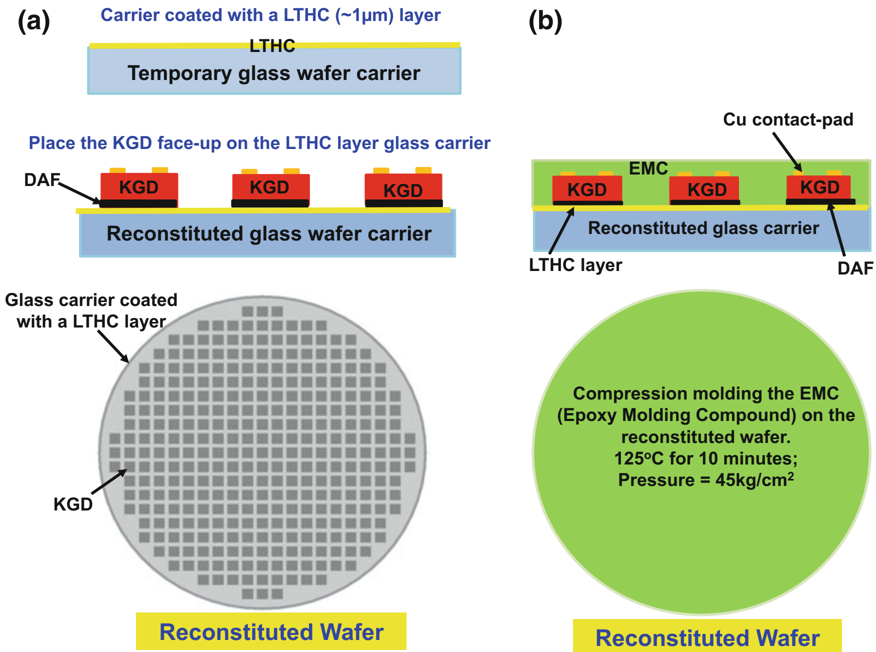


Fig. 6.8 **a** Spin coat a LTHC layer on the carrier and pick and please the chip face-up on the carrier. **b** Compression molding the EMC

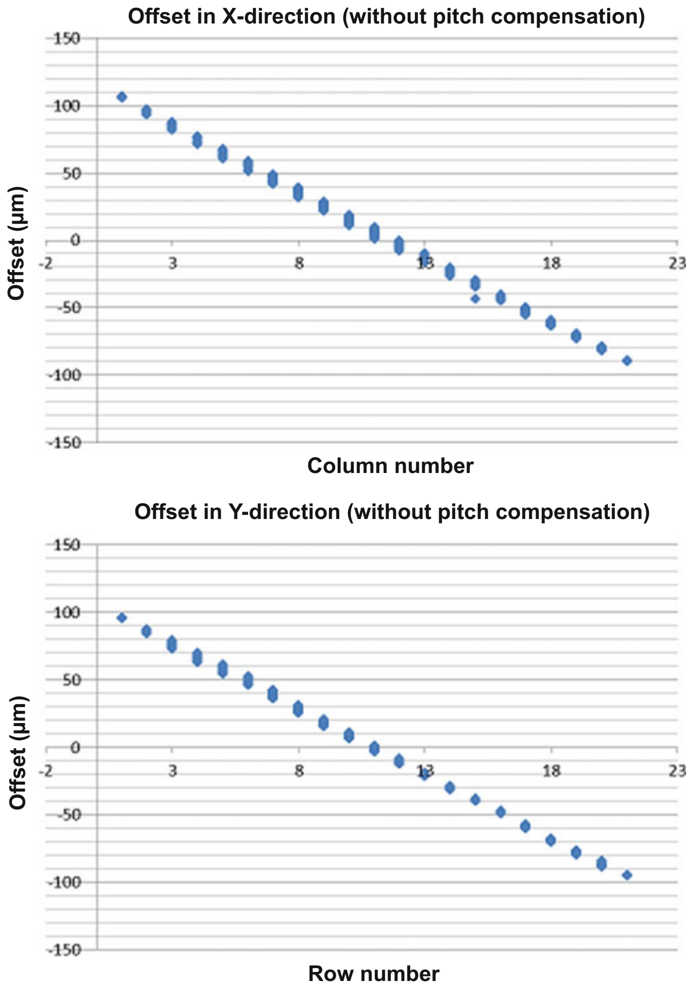


Fig. 6.9 Position offset data: *X*- and *Y*-direction (without pitch compensation)

Fig. 6.10. It can be seen that the placement offset is reduced from ±100 μm (without pitch compensation) to ±4.0 μm (with pitch compensation), and this is a good performance that can meet the process specifications.

6.8.3 EMC Dispensing

The EMC is a liquid-like material (Nagase R4507) and its material properties are shown in Table 6.3. It can be seen that the filler content is 85%. The average size of

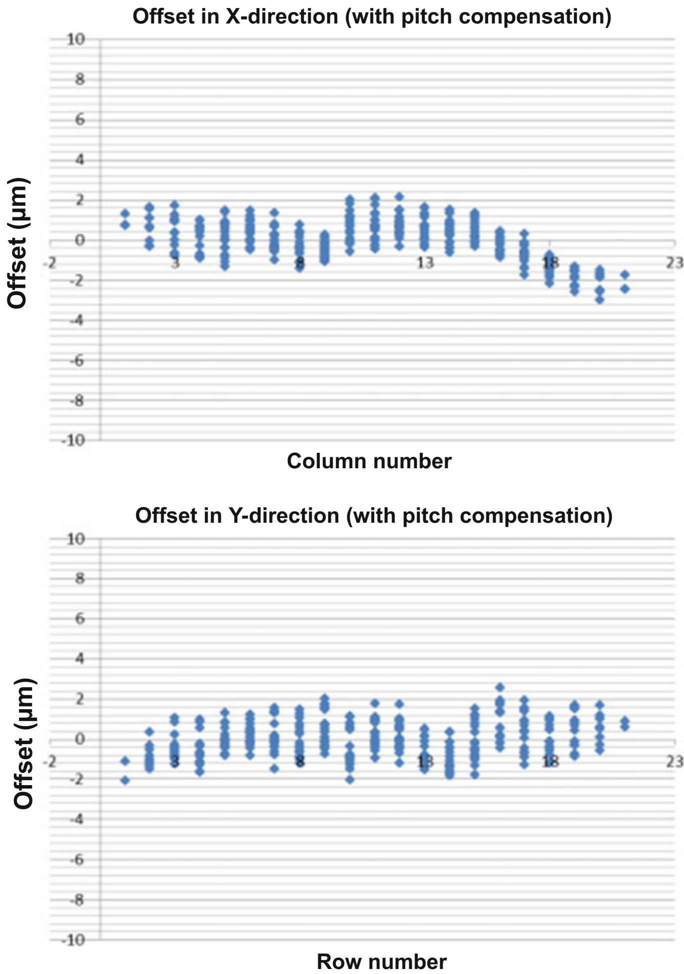


Fig. 6.10 Position offset data: *X*- and *Y*-direction (with pitch compensation)

Table 6.3 Material properties of the EMC

Item	R4507
Filler content (%)	85
Filler to cut (μm)	25
Filler average size (μm)	8
Specific gravity	1.96
Viscosity (Pa s)	250
Flexural modulus (GPa)	19
Tg (DMA) (°C)	150
CTE1 (ppm/K)	10
CTE2 (ppm/K)	41

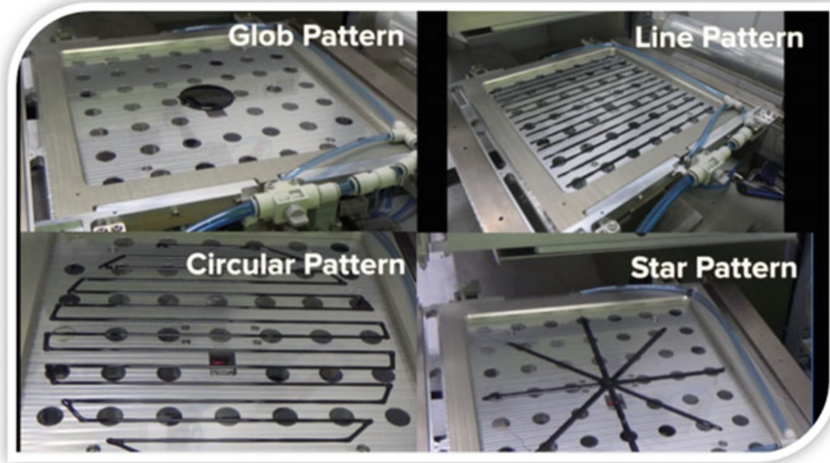


Fig. 6.11 Different liquid dispensing patterns

the filler is 8 μm and the maximum size of the filler is 25 μm. The flexural modulus of the EMC is 19 GPa and the viscosity is 250 Pa s. The transition temperature (Tg) is 150 °C. There are many ways to dispense the EMC such as the glob pattern, line pattern, circular pattern, and star pattern (Fig. 6.11). Experimental results show that there are many flow marks from the glob pattern. (One of the key reasons to have flow marks is the epoxy resin and filler separation and the silica fillers concentrate along those "streamline" shown in Fig. 6.12.) Also, experimental results show that the flow mark length from the glob pattern is very much larger than that from the line pattern as shown in Fig. 6.12. This is because the flow path of liquid EMC for the line pattern is shorter than that of the glob pattern. It should be pointed out that even the experiments are carried out in the square carrier, however the results are also applied to the circular carrier.

6.8.4 Compression Molding, PMC, and Die Shift

After EMC dispensing, it is followed by the compression molding as shown in Figs. 6.8b and 6.13. The KOZ (keep out zone) method is used and the mold cap diameter is 295 mm (2.5 mm clearance from the 300 mm glass carrier wafer edge). The glass carrier with dies attached is fixed onto the top mold chase by vacuum as shown in Fig. 6.13. The dispensed EMC on a releasing film is placed on the bottom plunger. After a few experiments, the optimal compression molding parameters are: temperature = 125 °C, pressure = 45 kg/cm^2, time = 10 min and removing trap air before compression molding. It is followed by post mold cure (PMC) with a

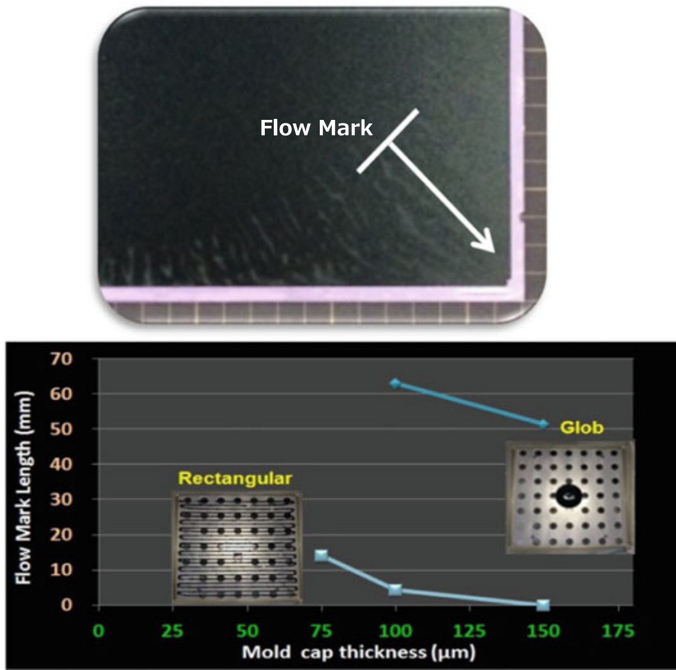


Fig. 6.12 Glob versus rectangular dispensing pattern. Flow mark point of measurement

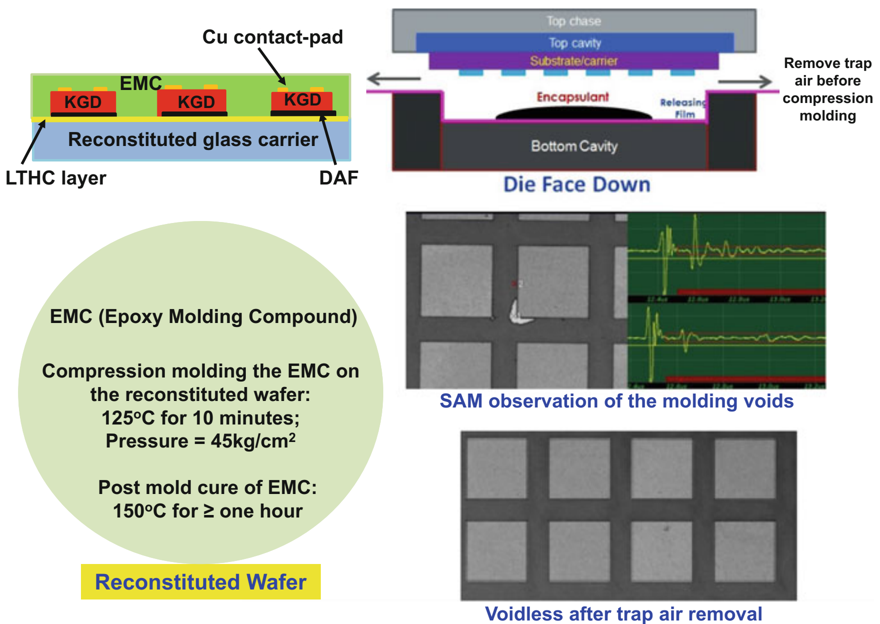


Fig. 6.13 Compression molding of EMC and PMC

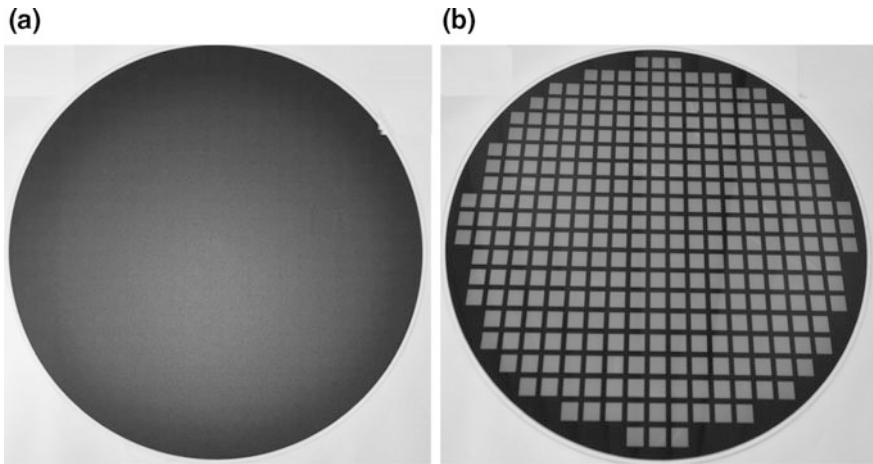


Fig. 6.14 **a** Top view of a molded reconstituted wafer. **b** Bottom view of a molded reconstituted wafer without the LTHC-layer so we can see the test chips

temperature = 150 °C, time $\geq$ 60 min, and a dead weight = 15 kg for a better warpage control. The compression molding is performed by the high-coplanarity accuracy machine ORCAS.

Inspections for molding voids are carried out by C-mode scanning acoustic microscopy (C-SAM). In order to balance the resolution and signal penetration depth, a transducer of 75 MHz is selected for the voids observation. Before compression molding parameter optimization, around 10 voids are detected (especially located at the die edge) in each of the molded wafers as shown in Fig. 6.13. After optimization, the voids are eliminated.

Figure 6.14a shows the top side of the molded test packages on the glass reconstituted wafer with the LTHC layer. In order to see the test chips, some of the reconstituted carrier wafers are without the LTHC layer such as the one shown in Fig. 6.14b. In this case, we can determine the die shift due to compression molding by measuring the position of each chip before and after molding. Figure 6.15 shows the statistical plots of the *X*-position die shift and *Y*-position die shift caused by the compression molding. It can be seen that because of the DAF (which solidly holding the chip to the carrier), the die shift (can be controlled within ±4 μm) is too small to be an issue on making the RDLs.

6.8.5 Warpages

The total thickness variations (TTV) of a few typical molded reconstituted wafers after PMC are shown in Table 6.4. This is a measurement of 8 points around the peripheral and one point at the center of the reconstituted wafer. It can be seen from

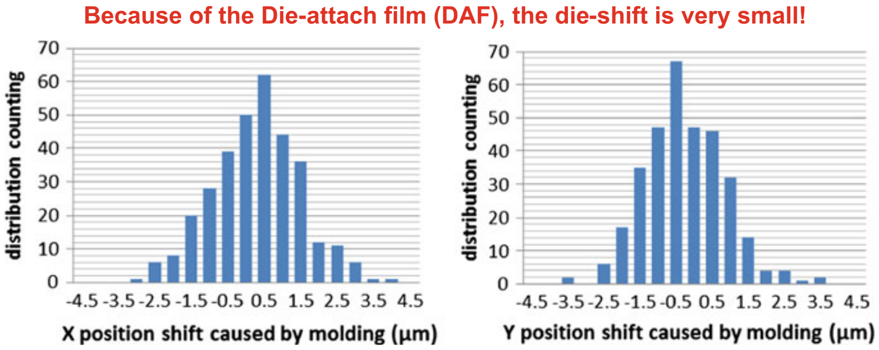


Fig. 6.15 Compression molding-induced die shift distribution data. (L) *X*-direction. (R) *Y*-direction

Table 6.4 TTV of typical molded reconstituted wafers

Position	Wafer-1	Wafer-2	Wafer-3
1	1301	1301	1299
2	1307	1307	1300
3	1308	1308	1303
4	1305	1310	1305
5	1310	1312	1309
6	1307	1312	1307
7	1305	1312	1310
8	1306	1302	1307
9	1309	1310	1306
Range	9 μm	11 μm	11 μm

Table 6.4 that the TTV is about 10 μm. The warpages of several reconstituted wafers after PMC are measured by the shadow Moire method. The results are shown in the table of Fig. 6.16. It can be seen that the maximum average warpage for the glass CTE = 3.25×10^{-6}/°C is 4.003 mm, CTE = 7.6×10^{-6}/°C is 0.38 mm, and CTE = 8.1×10^{-6}/°C is 0.25 mm. It is noted that the CTE of the EMC is 10×10^{-6}/°C (Table 6.3). Thus, as expected, the smaller the CTE mismatch between the glass carrier and the EMC the smaller the warpage.

Finite element simulation results for the glass with CTE = 3.25×10^{-6}/°C and the glass with CTE = 7.6×10^{-6}/°C are reported, respectively, in Fig. 6.16a, b. The measurement results for these two cases are also reported in Fig. 6.16a, b. It can be seen that the measurement and simulation results compare very well. Detail descriptions of the finite element simulation are shown in the following paragraphs.

A. *Material Properties*

Table 6.5 shows the material properties of the key elements of a FOWLP. The coefficient of thermal expansion (CTE) of Si carrier, Glass-1 carrier, and Glass-2

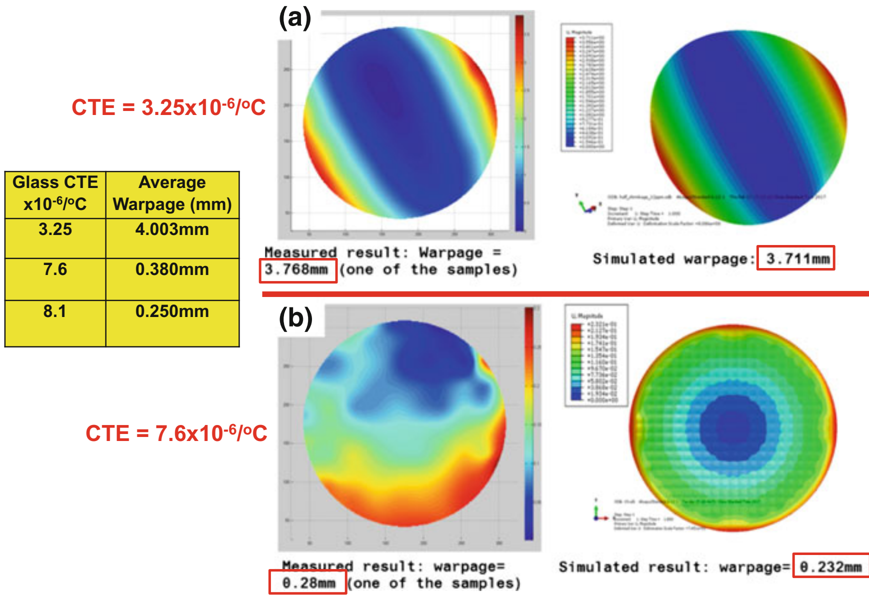


Fig. 6.16 Measured warpage and simulation contours of the molded wafer (after PMC) with **a** carrier CTE = 3.25×10^{-6}/°C, and **b** carrier CTE = 7.6×10^{-6}/°C

Table 6.5 Material properties of the package structure for warpage analysis

Materials	Thermal expansion coefficient (10^{-6}/°C)	Young's modulus (GPa)	Poisson's ratio
Silicon	2.6	168	0.28
EMC	10	19	0.25
DAF	120	2.3 (0 °C) 0.02 (50 °C) 0.006 (100 °C) 0.005 (200 °C)	0.4
Glass-1	3.2	73.6	0.3
Glass-2	7.6	69.3	0.3

Glass-1 (0.76 mm thick)
Glass-2 (1 mm thick)

carrier are, respectively, 2.6×10^{-6}/°C, 3.25×10^{-6}/°C, and 7.6×10^{-6}/°C. The Young's modulus (GPa) of DAF is temperature dependent: 2.3 (0 °C), 0.02 (50 °C), 0.006 (100 °C), and 0.005 (200 °C).

B. *Finite-Element Model*

A bowl shape of the molded wafer is assumed. Due to double symmetries of the molded (reconfigured) wafer shown in Fig. 6.17, only quarter of the wafer is

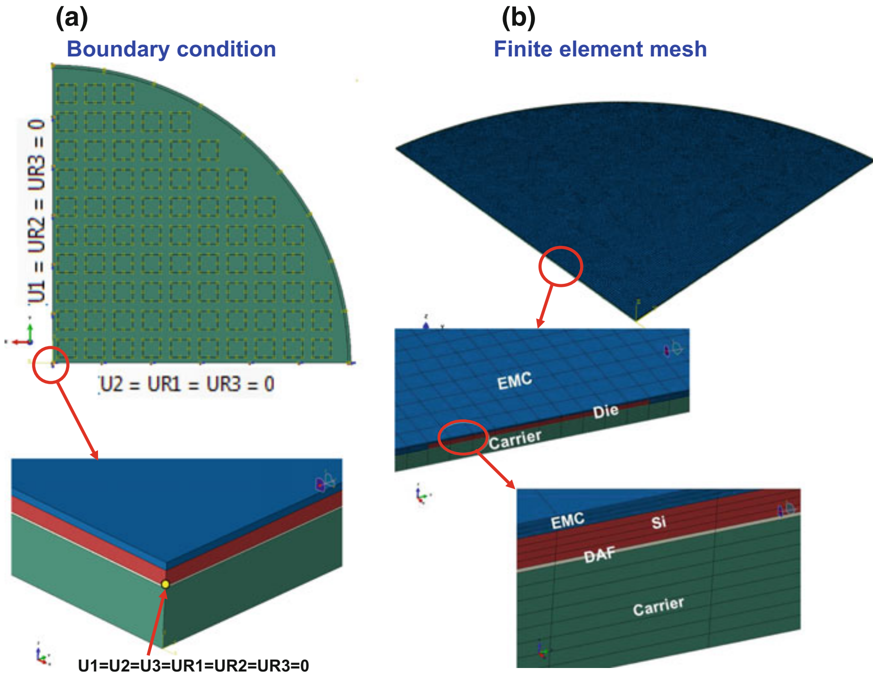


Fig. 6.17 **a** Boundary conditions. **b** Finite element meshes for the warpage analyses of quarter model of the molded reconstituted wafer

modeled (Fig. 6.17a). Figure 6.17b shows the finite element meshes for the Si chip, EMC, DAF, and carrier. Since the LTHC layer is so thin, it is not included in the model. The finite element code (ABAQUS V6.12) with element type: 3D stress and 290,000–340,000 elements (depends on different cases) is used for the simulations.

C. *Boundary Conditions*

The displacement/rotation boundary conditions along the *x*-axis are that there is no displacement in the *y*-direction (U2 = 0), and there is no rotation about the *x*-axis (UR1 = 0) and the *z*-axis (UR3 = 0). The boundary conditions along the *y*-axis are that there is no displacement in the *x*-direction (U1 = 0), and there is no rotation about the *y*-axis (UR2 = 0) and the *z*-axis (UR3 = 0). At the center, the boundary conditions are that there are not any displacement and rotation (U1 = U2 = U3 = UR1 = UR2 = UR3 = 0). The temperature boundary condition is for the reconstituted wafer to cool down from 125 °C (stress-free temperature) to room temperature. That is right after PMC of the EMC. Another boundary condition is for the backgrinding of the EMC of the reconstituted wafer to expose the Cu contact pad for making the RDLs. This will be executed by using the “birth and death” technique that the element to be grinded will be deactivated during the simulation.

However, the backgrinding process parameters such as pressure, speed, fine, or coarse grinding are not modeled.

D. *Comparison between the Simulation and Experimental Results*

In order to compare the simulation and experimental results, the DAF and its temperature-dependent material properties are included in the modeling. Figure 6.16b shows the comparison between the simulation and experimental results for the case of chip dimensions = 10 mm × 10 mm × 150 µm, package/chip area ratio = 1.8, die EMC cap = 100 µm, and glass carrier thickness = 1 mm with CTE = 7.6 × 10^{-6}/°C. A volume shrinkage of the EMC = 0.27% is assumed. It can be seen that the maximum warpage of the double symmetry model is equal to 0.232 mm, which compares reasonably well (17% off) from the maximum experimental result (0.28 mm). It should be pointed out that due to the die uniformity, die pick and place accuracy, EMC filler distribution, EMC dispensing uniformity, compression condition, and die shift, the warpage after PMC is not exactly a bowl shape. Also, these factors cannot (or are very difficult to) be modeled by finite element method, especially for small warpage.

Actually, some of the experimental results (in the cases for very large warpage) show that the warpage is not in a bowl shape but a cylindrical shape. In order to compare the simulation result to these experimental results, half of the structure is modeled as shown in Fig. 6.18. The warpage contour distribution of the measurement result shown in the left-hand side of Fig. 6.16a is for the case of chip dimensions = 10 × 10 × 0.15 mm^3, package/chip area ratio = 1.8, die EMC cap = 100 µm, and glass carrier thickness = 0.78 mm with CTE = 3.26 × 10^{-6}/°C. The warpage contour distribution of the simulation result shown in the right-hand side of Fig. 6.16a compares very well (1%) with the experimental result shown on the left-hand side.

E. *Effect of Carrier Wafer Material and Thickness on FOWLP Warpage*

Based on the above simulation and experimental result, it shows that a reasonable thicker glass with higher CTE (closer to that of EMC) carrier wafer will lead to a lower warpage of the FOWLP. For the case of chip dimensions = 10 mm × 10 mm × 150 µm, the chip EMC cap = 100 µm, and the package/chip area ratio = 1.8, the maximum warpage is 0.28 mm if the reconstituted carrier wafer is 1 mm thick glass with CTE = 7.6 × 10^{-6}/°C. On the other hand, the maximum warpage is larger than 3.7 mm if the reconstituted carrier wafer is 0.78 mm thick with CTE = 3.25 × 10^{-6}/°C, which is equivalent to a Si carrier and a thin glass with low-CTE carrier. This is because, unlike the CTE of Si (2.6 × 10^{-6}/°C), the CTE of glass is closer to the CTE of EMC (10 × 10^{-6}/°C). Also, a thicker glass compensates the lower Young's modulus of the glass (69.3 GPa) than the Si (168 GPa). Furthermore, a thicker glass has less chance to be broken during handling and manufacturing. Thus, for chip-first and die face-up FOWLPs, a glass carrier wafer with CTE = 7.6 × 10^{-6}/°C and a thickness = 1 mm is recommended.

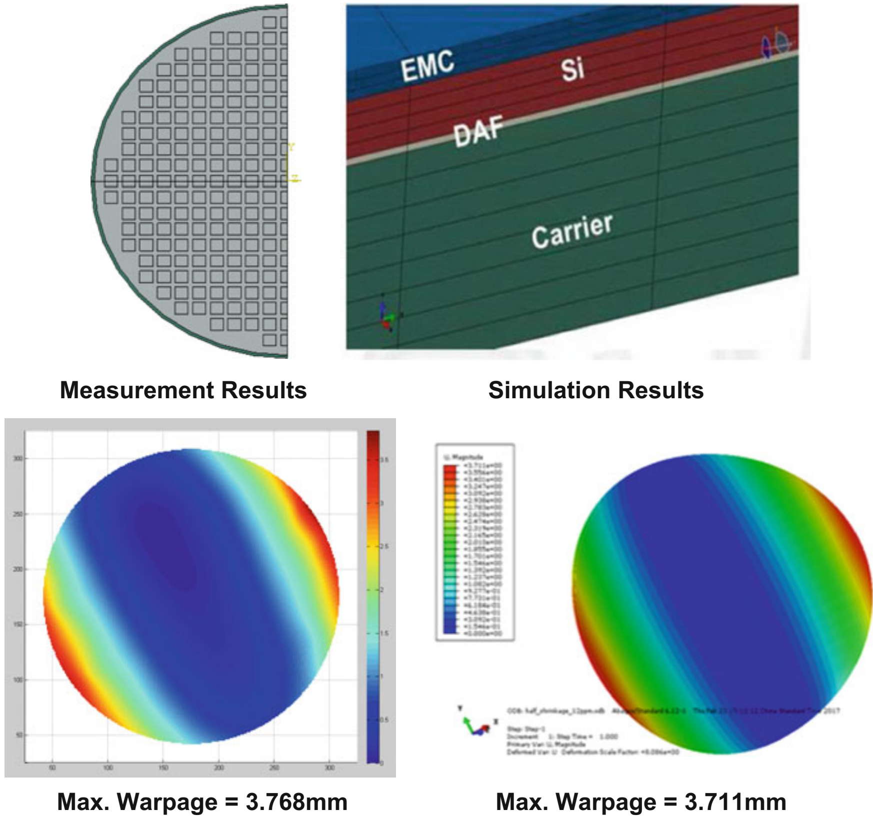


Fig. 6.18 Comparison between the warpage experimental result and simulation result (glass carrier thickness = 0.7 mm and CTE = 3.2 × 10^{-6}/°C)

6.8.6 Cu Revealing

For FOWLP with chip-first and die face-up process, in order to make the RDLs and then mount the solder balls, the molded EMC above the Cu contact pad must be removed (Cu revealing) as shown in Fig. 6.6f. In this study, DISCO's backgrinding machine is used to remove the EMC. During backgrinding, some of the areas have Cu smearing as shown in Fig. 6.19. Because of the Cu smearing, the stepper won't work and the RDLs cannot be fabricated.

Another test chip is fabricated, this time the polymer is much taller (30 μm vs. 5 μm the first time is shown in Fig. 6.2) and covered the Cu contact pad as shown in Fig. 6.20. After pick and place, EMC dispensing, compression molding, PMC, and backgrinding, the resulting surface of the reconstituted structure is shown in Fig. 6.20. It can be seen that because of the polymer, there is not any Cu smearing and the Cu contact pad is ready for the fabrication of the RDLs.

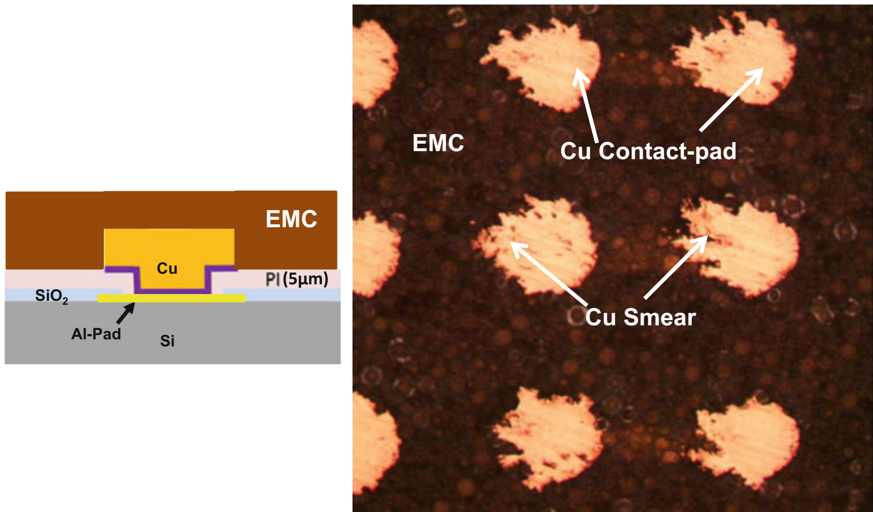


Fig. 6.19 Cu smear during backgrinding of the EMC to expose the Cu contact pad

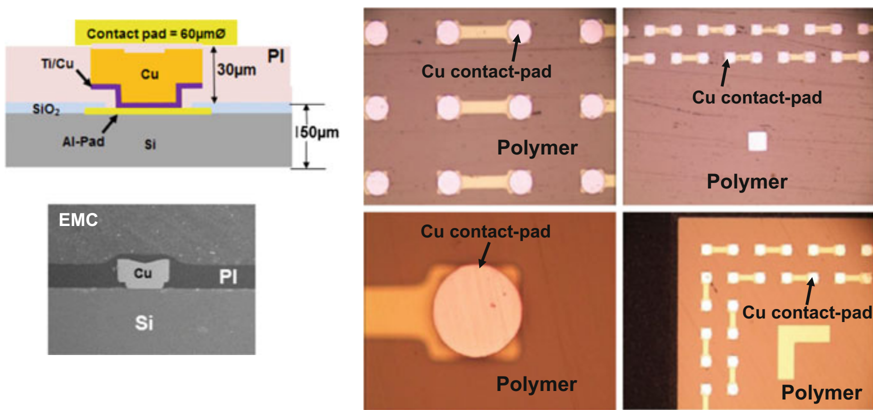


Fig. 6.20 (L) Test chip with the tall polymer (~30 μm) to cover the Cu contact pad and chip surface. (R) After backgrinding the EMC to expose the Cu contact pads (Cu revealing)

6.8.7 RDLs

The key process steps of fabricating the RDLs of the FOWLP (Fig. 6.3, with conventional UBM/Cu pad) are briefly discussed as follows (Fig. 6.21). First of all, the wafers are ultrasonically cleaned.

- Step 1: Spin coat the photosensitive polyimide (PI) on the reconstituted wafer. Apply a stepper (every 4 test packages as a unit) and then use photolithography

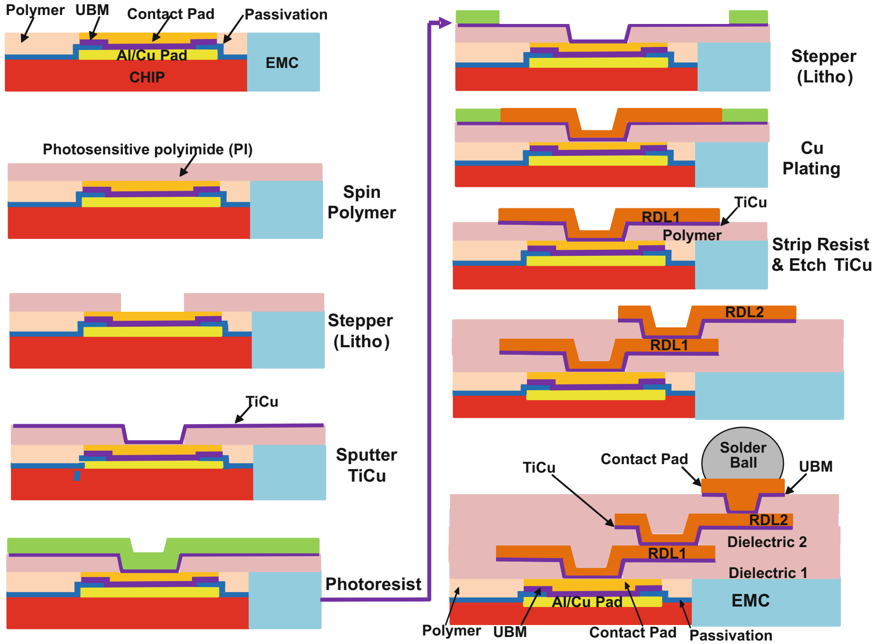


Fig. 6.21 Key process steps in fabricating the RDLs of FOWLP with the conventional attachment of solder balls

techniques to align, expose, and develop the vias of the PI. Finally, cure the PI at 200 °C for one hour. This will form a 4 to 5-μm-thick PI layer. (PI development.)

- Step 2: Sputter Ti and Cu by PVD (175–200 °C) over the entire wafer.
- Step 3: Apply a photoresist and a stepper and then use photolithography techniques to open the redistribution-traces locations.
- Step 4: Electroplate Cu by ECD (room temperature) on Ti/Cu in photoresist openings.
- Step 5: Strip off the photoresist.
- Step 6: Etch off the Ti/Cu. (RDL1 is obtained.)
- Step 7: Repeat Step 1 through Step 6 to obtain RDL2 and RDL3.
- Step 8: Same as Step 1 (for UBM).
- Step 9: Apply a photoresist and a stepper and then use photolithography techniques to open the vias on the photoresist for the desired bump pads.
- Step 10: Sputter Ti and Cu over the entire wafer.
- Step 11: Apply a photoresist and a stepper and then use photolithography techniques to open the vias on the bump pads to expose the areas with UBM.
- Step 12: Electroplate the Cu and Cu pad.
- Step 13: Strip off the photoresist.
- Step 14: Etch off the Ti/Cu. It is ready for solder ball mounting.

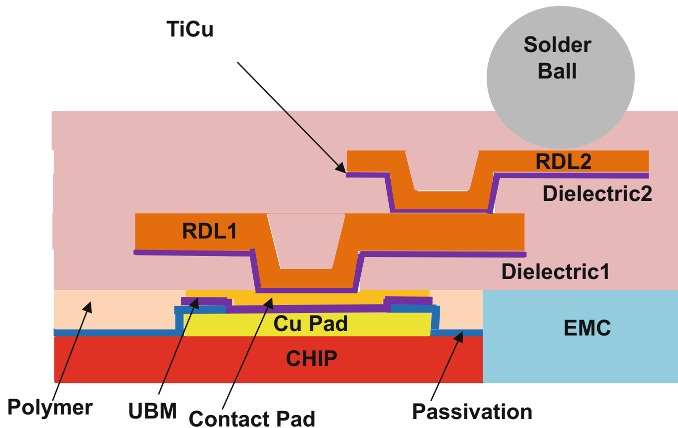


Fig. 6.22 Key process steps in fabricating the RDLs of FOWLP with UBM-less Cu pad for solder balls

The process steps in fabricating the RDLs for Fig. 6.4 with UBM-less Cu pad are the same (from Step 1 through Step 7) as those for Fig. 6.3 with conventional UBM/Cu pad, except Step 8 (same as Step 1) is for PI development as shown in Fig. 6.22. It is ready for solder ball mounting. Step 9 through Step 14 are not needed. From here on, only the case of UBM-less Cu pad for solder ball will be considered.

The thickness of DL1, DL2, and DL3 is 5 μm and that of DL4 is 10 μm. The thickness of RDL1 and RDL2 is 3 μm and that of RDL3 is 7.5 μm. (The thicker RDL3 is for the UBM-less thicker Cu pads to "resist" the Cu consumption from the solder ball reflow and during operation.)

The RDLs are shown in Figs. 6.23, 6.24 and 6.25. Overall, it can be seen that all the RDLs are properly done. However, a closer look at the RDL1, based on the top view as well as cross-sectional measurements, the actual fabricated line width/spacing are (on average) 4.68 μm/5.30 μm. This means the line width is smaller than it should be while the line spacing is larger than the design values (5 μm/5 μm). These errors could be due to (a) the small feature size of line width/spacing, (b) the photoresist opening, and (c) the seed layer (Ti) etching. For RDL2 and RDL3, they are very close to the designed values.

6.8.8 Solder Ball Mounting

There are two different stencils for the solder ball mounting, one is for stencil printing the flux and the other is for stencil mounting the solder balls. The solder (Sn3 wt%Ag0.5 wt%Cu) balls (200 μm diameter) used are from indium and are on

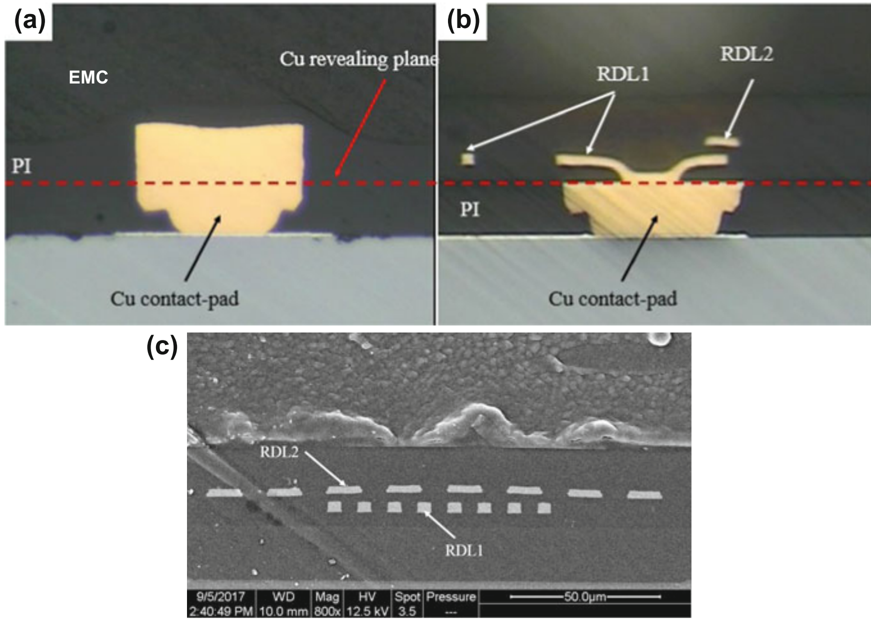


Fig. 6.23 **a** Before Cu revealing. **b** After Cu revealing and 2 RDLs. **c** Cross-section SEM images of RDL1 and RDL2

0.4 mm pitch. The peak temperature for solder reflow is 245 °C. Figure 6.26a shows the reflowed reconstituted wafer, Fig. 6.26b shows the individual package, and Fig. 6.26c shows the close-up view of solder balls on the package.

6.8.9 Debonding

The debonding of the glass carrier is by scanning a laser (355 nm DPSS Nd: YAG UV laser source is used) from the glass carrier side. The laser spot size is 240 μm, the scanning speed is 500 mm/s and the scanning pitch is 100 μm. When the LTHC layer "sees" the laser light, it converts into powders and the glass carrier is easily removed. It is followed by chemical cleaning. The DAF is remained on the backside of the chip as shown in Fig. 6.27. The bottom side of the FOWLP is shown in Fig. 6.28. A cross section of the FOWLP is shown in Fig. 6.29 for the UBM-less case (Fig. 6.4).

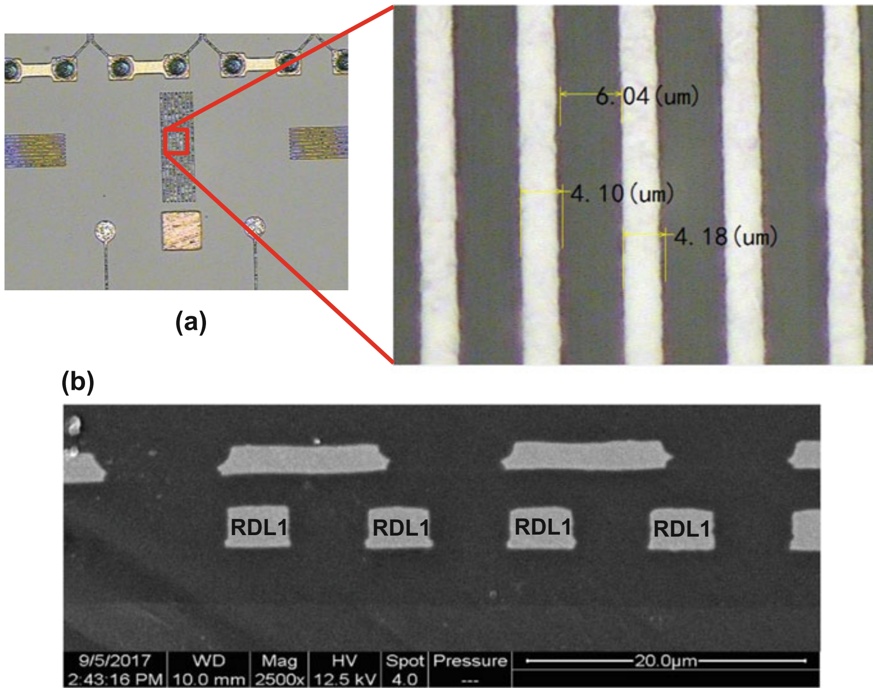


Fig. 6.24 **a** RDL1 (5 μm/5 μm line width/spacing). **b** SEM image of RDL1

6.9 PCB Assembly of FOWLP

The design of the PCB and stencil will be briefly mentioned. The stencil solder paste printing, pick and place, and solder reflow will also be presented. The x-ray images and the cross-section images of the PCB assembly are provided.

6.9.1 PCB

The PCB for the fan-out wafer-level package is made of FR-4 and is shown in Fig. 6.30. It can be seen that there are 4 package sites on the board. The dimensions of the PCB are 103 mm × 52 mm × 0.65 mm and there are 6 layers. There are 908 pads (with a pitch = 0.4 mm) for each package. The pad with a diameter = 0.2 mm is non-solder mask defined and its surface finish is OSP (organic solderability preservative). The solder mask opening diameter is 0.28 mm.

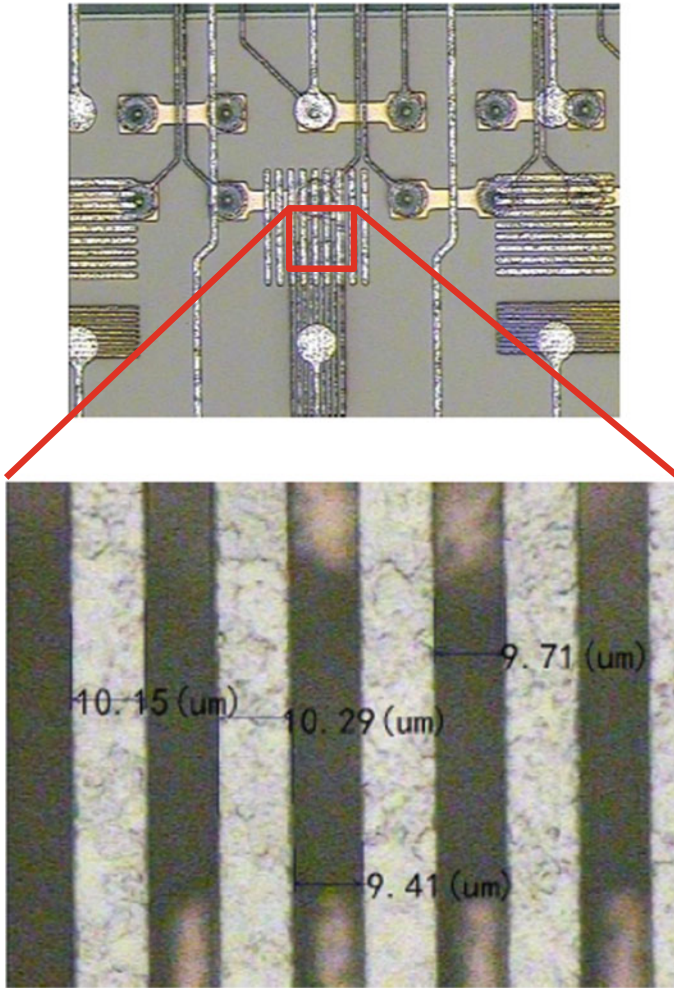


Fig. 6.25 RDL2 (10 μm/10 μm line width/spacing)

6.9.2 *Stencil and Printing*

The stencil is made of stainless steel with a grain size of 2 μm and is 0.08 mm thick. The opening is fabricated by laser and electrical/chemical polishing. The opening is increased from a 0.2286 mm diameter circle to a 0.2413 mm^2 square (a paste volume increased by 41.8%). The SPI (solder paste inspection) data is shown in Fig. 6.31. It can be seen that slight more pastes are printed near the central area (Area 1). The solder paste printing is by the DEK Horizon 9.

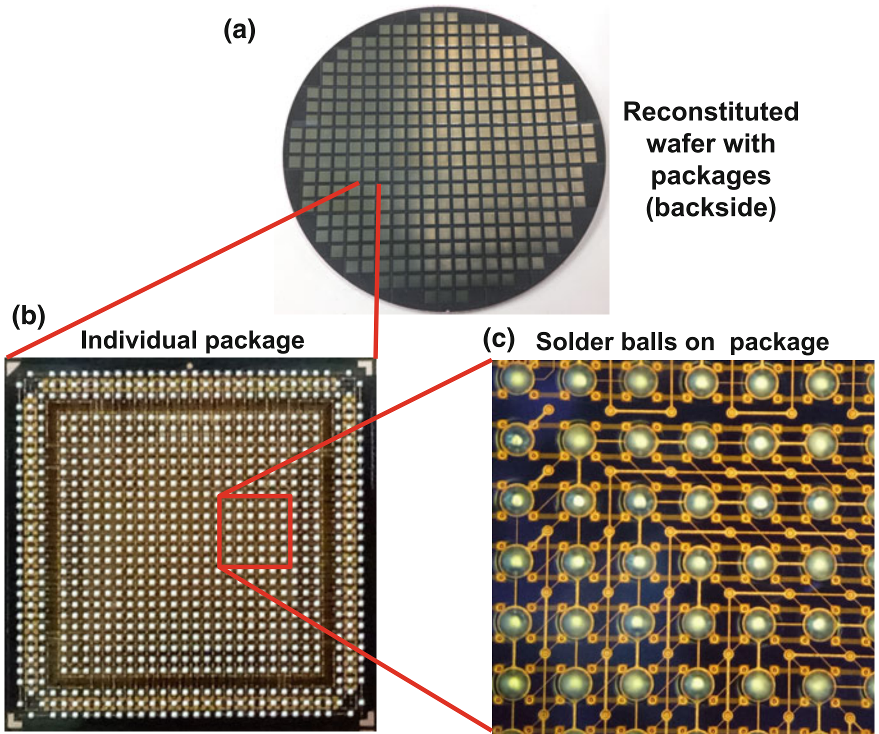


Fig. 6.26 **a** Image of the fabricated reconstituted wafer. **b** Individual FOWLP package. **c** Close-up view of the solder balls

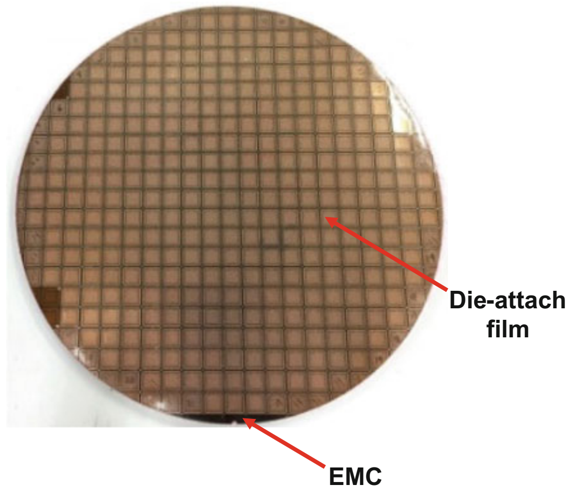


Fig. 6.27 Reconstituted wafer after laser debonding

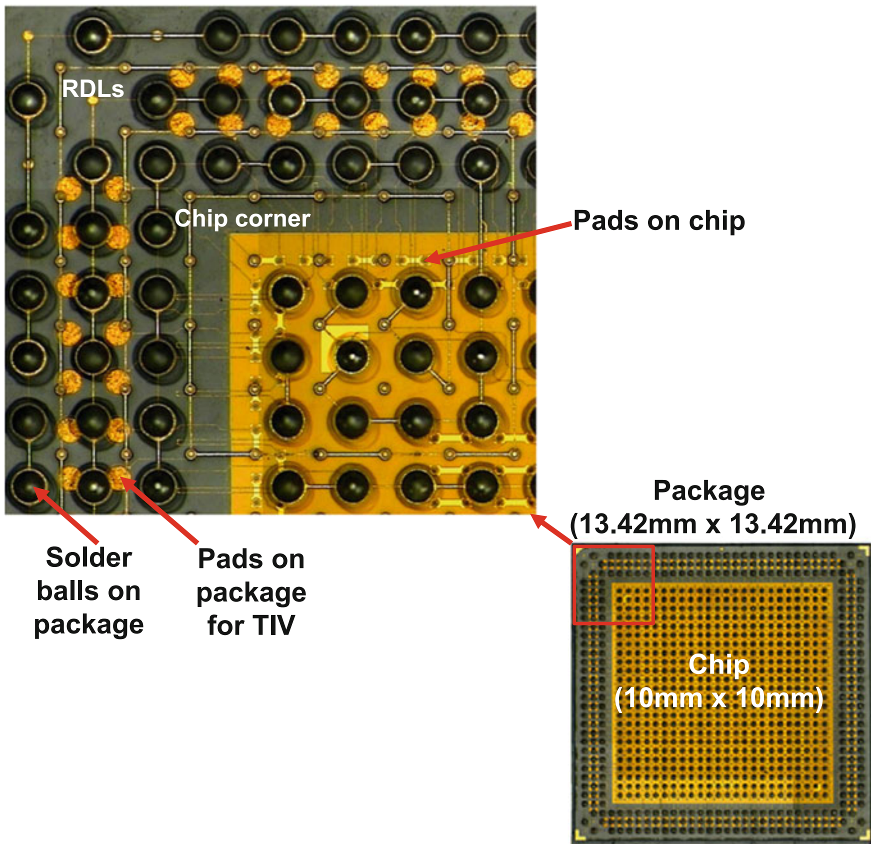


Fig. 6.28 Individual package for the 10 mm × 10 mm chip

6.9.3 Pick and Place and Reflow

The pick and place is by the SiPlace x4s. The 10 temperature zones BYU Pyram nitrogen 150N is used for the reflow of the solder paste. The temperature profile is shown in Fig. 6.32. It can be seen that the maximum temperature is 245 °C and the time above 217 °C is 85 s (it meets the JSTD-020 standard). The PCB assemblies are shown in Figs. 6.33 and 6.34. Figure 6.33 shows the assembled PCB with 4 packages and the x-ray image of one of the packages. It can be seen that the package is properly assembled. Figure 6.34 shows the cross section of one of the packages and the solder joint height measurement. It can be seen that the solder joint are properly made (no bridging and head-in-pillow) and the variation of solder joints height is from 120 to 145 μm.

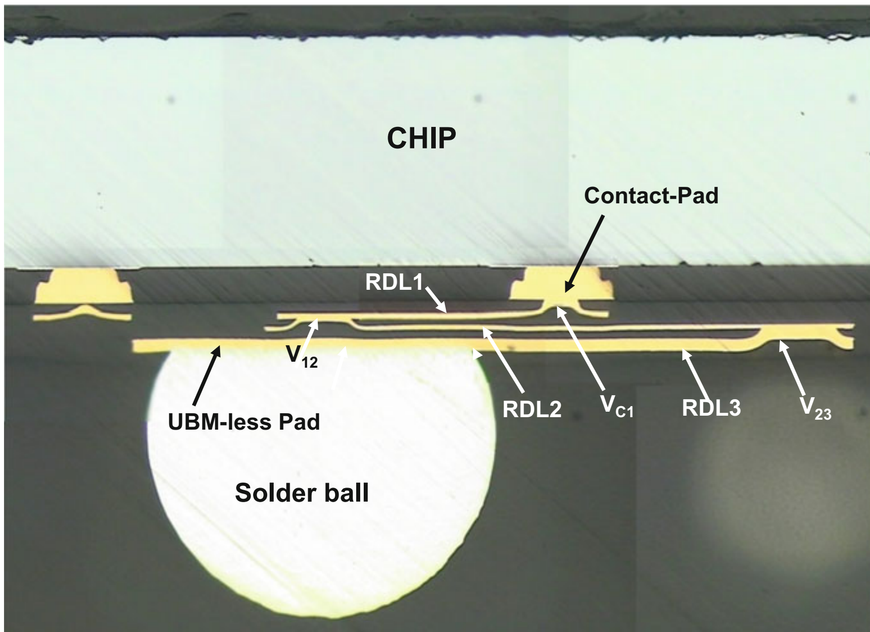


Fig. 6.29 Cross-section image of the assembled fan-out wafer-level package with three RDLs

6.10 Thermal Performance of FOWLP

6.10.1 Structure

Figure 6.35a shows the top view and Fig. 6.35b shows the cross-sectional view of the FOWLP structure for thermal analyses [27]. It can be seen that the chip size is 10 mm × 10 mm with various thicknesses (10, 25, 50, 100, 150, 200, 250, and 300 μm). The molded package size is 13.42 mm × 13.42 mm, i.e., the package/ chip area ratio = 1.8. There are a 100 μm EMC covering the top of the chip and 40 μm-thick RDLs to fan-out the circuitry from the bottom of the chip. The package is with 1024 (0.25 mm diameter) solder balls on a 0.4 mm pitch, which are reflowed on a PCB. The dimensions of the PCB are 25 mm × 25 mm × 0.8 mm.

6.10.2 Material Properties

Table 6.6 shows the thermal conductivity (W/m K) in cross-plane direction (*kz)* and in-plane direction (*kxy)* of the structural elements in Fig. 6.35. For Si, EMC, Cu, and solder, their *kz* and *kxy* are equal due to their homogeneous properties. For the RDL and PCB, they are assumed laminated materials in which there are several

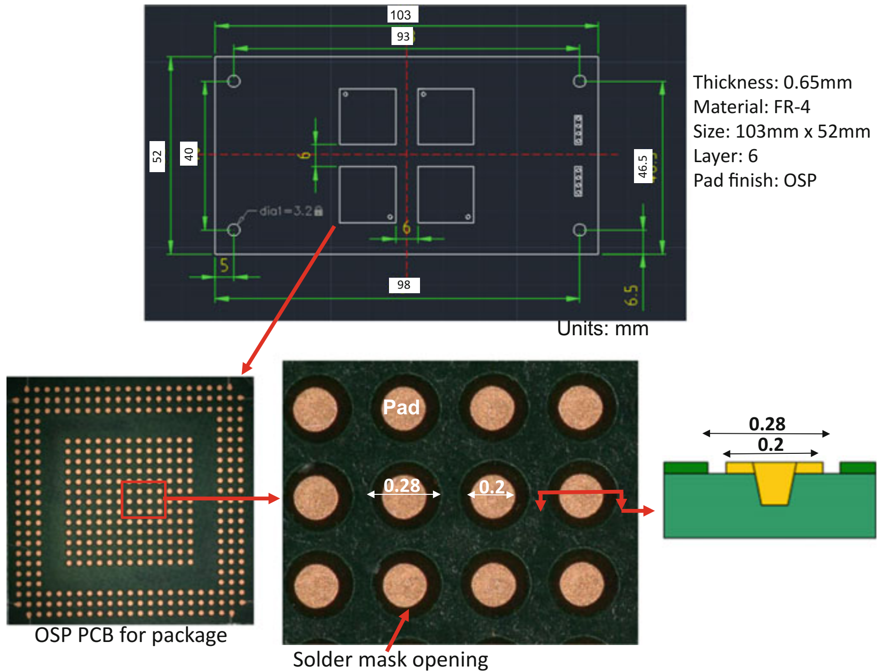


Fig. 6.30 PCB for package assembly and reliability tests

high conductive (Cu) layers inside the lamination, so their effective *kxy* is obviously higher than their effective *kz,* as shown in Table 6.6.

6.10.3 Boundary Conditions

The ambient temperature is assumed to be 25 °C. The boundary condition on the top side and bottom side of the PCB and the top side of the chip is with a convective heat-transfer coefficient, $h = 10$ W/m^2 K, which is to imitate a natural convection condition. The heat dissipation of the chip is 5 W.

6.10.4 Finite-Element Modeling and Analysis

Figure 6.36 shows the finite element model for thermal analysis. It can be seen that due to double symmetries of the chip/package/PCB, only quarter of the structure is modeled. For simplicity and the object of the present study, only steady-state heat-transfer analyses are performed.

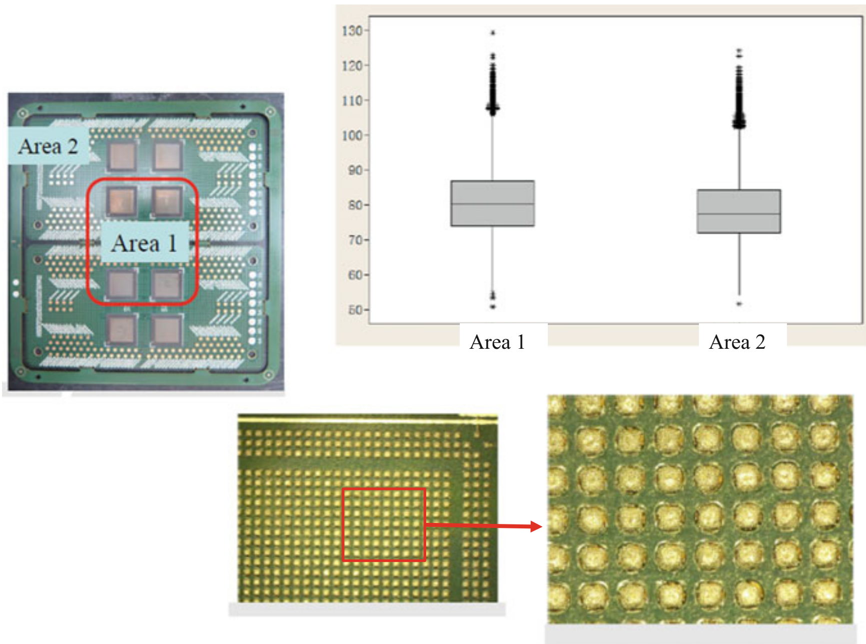


Fig. 6.31 Solder paste SPI

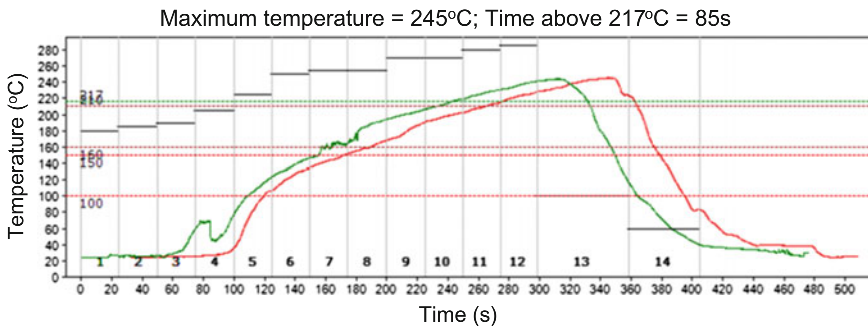


Fig. 6.32 Temperature profile for solder reflow with nitrogen

6.10.5 Analysis Results

The junction-to-ambient thermal resistance (*R*ja) of the 10 mm × 10 mm chip with various thicknesses is shown in Fig. 6.37. It can be seen that the thinner the chip the higher the *R*ja (i.e., the lower the thermal performance). This is because of the inferior thermal spreading capability of thinner chips. The thermal performance degrades rapidly as the chip thickness goes below 100 µm, as shown in Fig. 6.37.

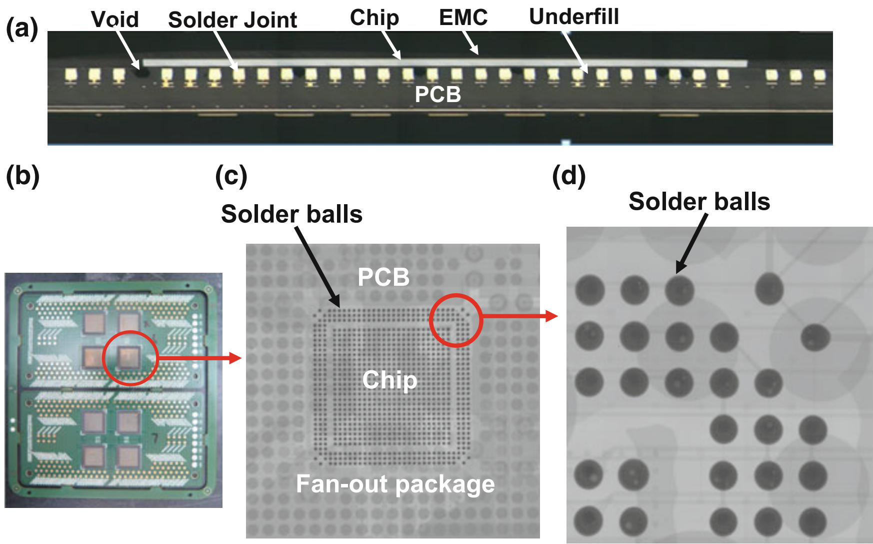


Fig. 6.33 X-ray images for the PCB-assembled package

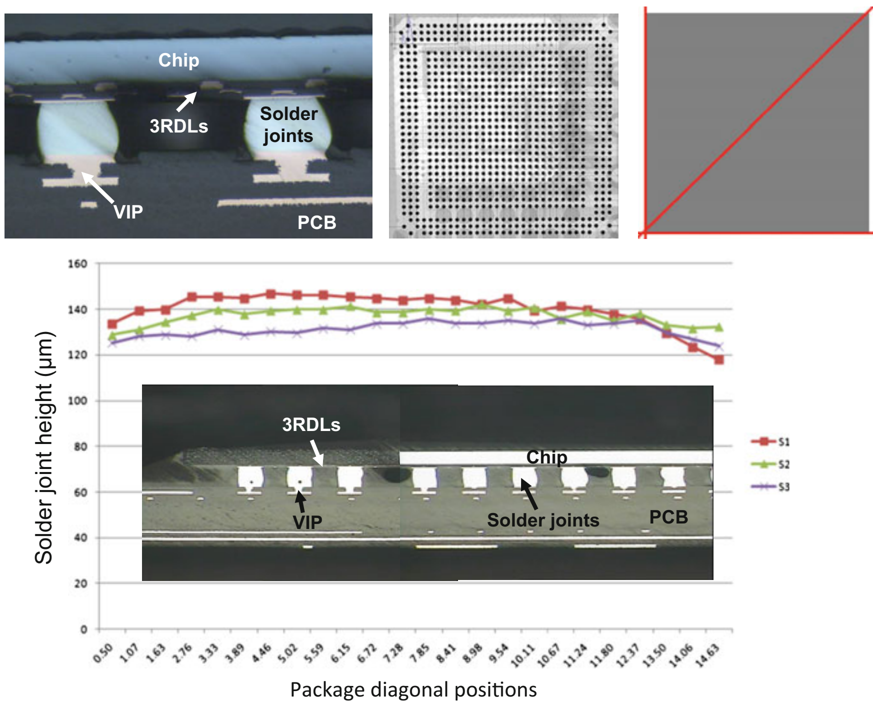


Fig. 6.34 Cross sections of PCB-assembled package

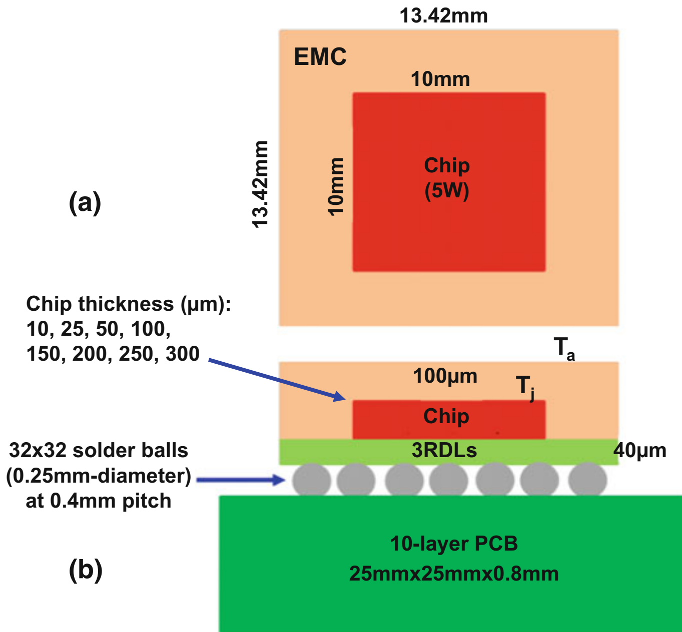


Fig. 6.35 Structure of the FOWLP assembly for thermal analyses. **a** Top view. **b** Cross-sectional view

Table 6.6 Material properties of the package structure for thermal analysis

Material	Thermal conductivity (W/m/K)
Si	148
EMC	0.25
Cu	400
Solder	40
RDL	Kxy = 25.2 Kz = 0.29
PCB	Kxy = 27.4 Kz = 0.35

Figure 6.38 shows a typical temperature contour distribution of a FOWLP (chip sizes are 10 mm × 10 mm × 150 μm, and package sizes are 13.42 mm × 13.42 mm × 290 μm). It can be seen that (1) the maximum temperature is 101.5 °C; (2) the minimum temperature is 89.9 °C; and (3) the Rja is 15.3 °C/W.

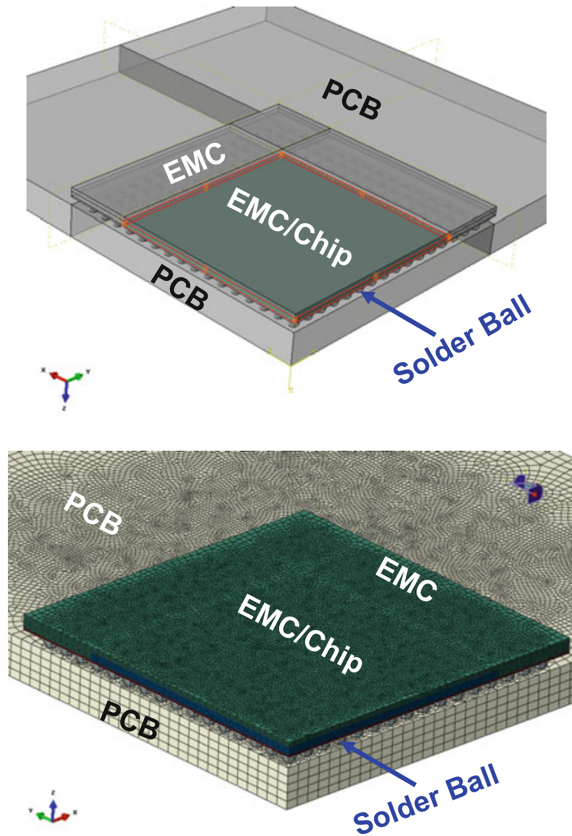


Fig. 6.36 Quarter finite element model for thermal analyses

6.11 Reliability Assessments—Thermal Cycling Test

6.11.1 Test Setup

Fifteen boards (each with 4 packages) are used for the temperature cycling tests [32]. The sample size is 60 packages. Thermal cycling is performed in a Votsch 7027-15 environmental chamber. This unit is capable of achieving chamber temperature as high as 190 °C and as low as −70 °C. Heating and cooling are achieved by forced convection, and the maximum ramp rate is 15 °C per minute. All of the boards are placed vertically in the chamber as shown in Fig. 6.39. The temperature input to the chamber (measured in the air of the chamber) is shown in Fig. 6.39. It can be seen that the temperature cycling is from room temperature to 85 °C and stay there for 15 min, then ramp down to −40 °C and stay there for 15 min, then ramp up to 85 °C and stay there for 15 min, and so for. The ramp up and ramp down times are 15 min each. The acquisition system is an Agilent 30970A data logger.

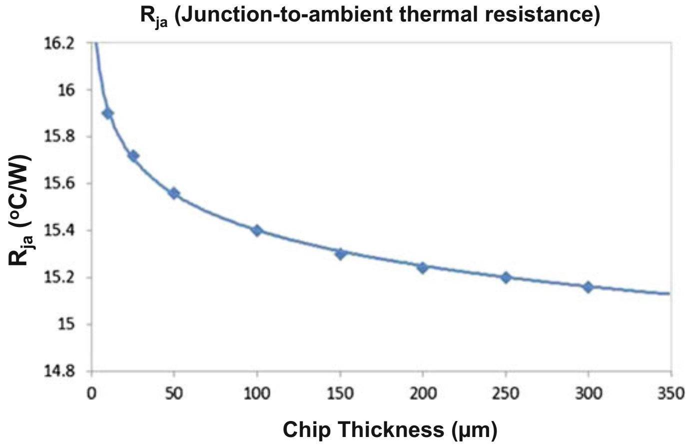
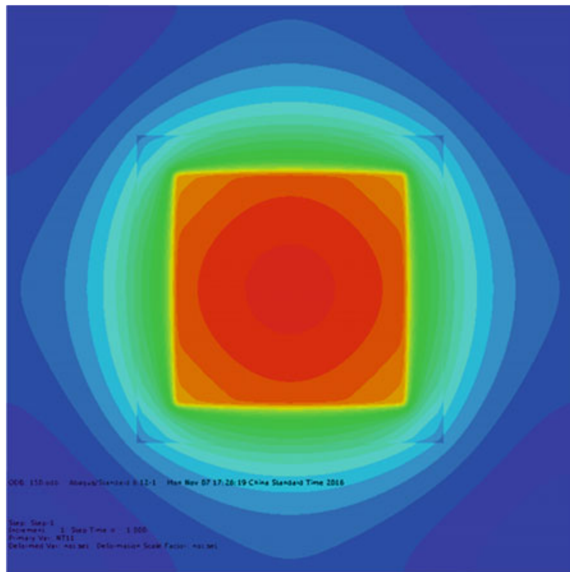


Fig. 6.37 Junction-to-ambient thermal resistance versus various chip thickness

Fig. 6.38 Typical temperature contour distribution of a FOWLP assembly



Chip thickness = 150µm; Power = 5W
Max, temperature = 101.5°C
Min. temperature = 89.9°C

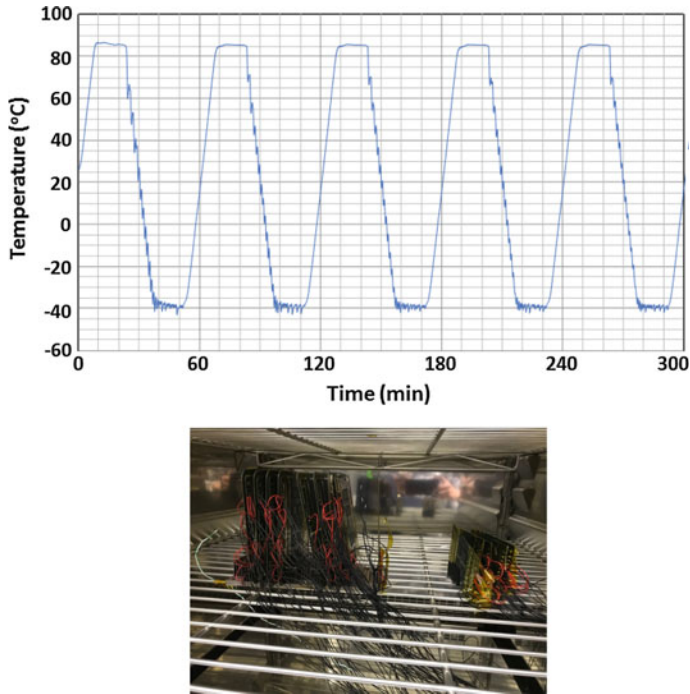


Fig. 6.39 Thermal cycling test setup and temperature profile

6.11.2 *Test Results*

The thermal cycling test results of the FOWLP solder joint (without underfill) reliability are shown in Fig. 6.40. The thermal cycling test stops at 1100 cycles and there are 14 failures (including one early failed at 58 cycles). It can be seen that the characteristic life (63.2% failed) of the Weibull plot is 2382 cycles which is more than adequate for the expecting life (usually is less than 3 years) of mobile product such as the smartphones and tablets.

6.12 Reliability Assessments—Drop Test

6.12.1 *Test Setup*

The test setup is according to JEDEC Standard JESD22-B111 as shown in Fig. 6.41. After more than 20 tries, the right height of the drop table is obtained which yields the drop spectrum with 1500 G/ms as shown in Fig. 6.42 [32].

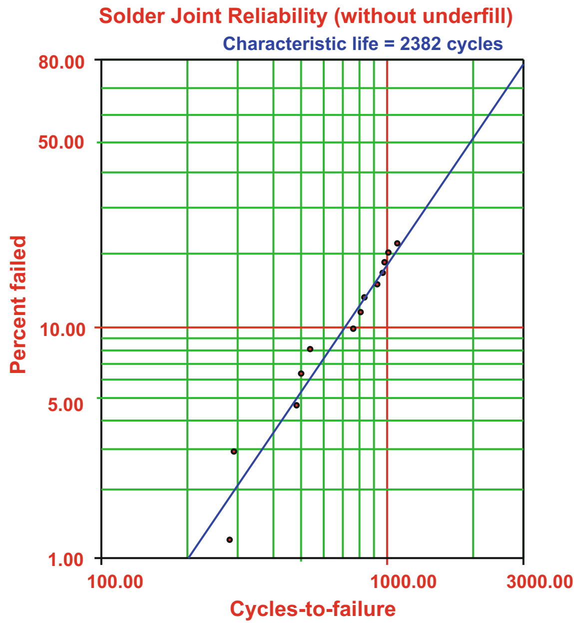


Fig. 6.40 Weibull plot of the package solder joint under thermal cycling test

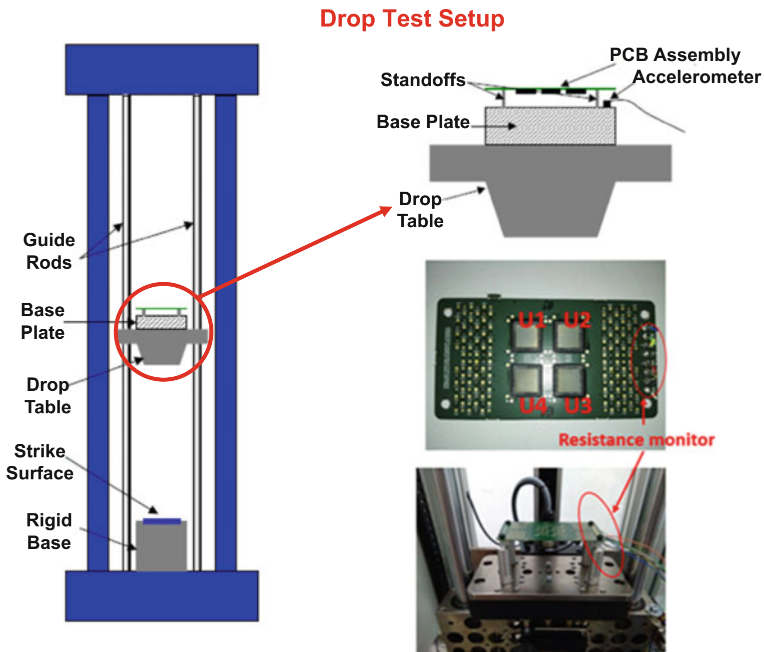


Fig. 6.41 Drop test setup

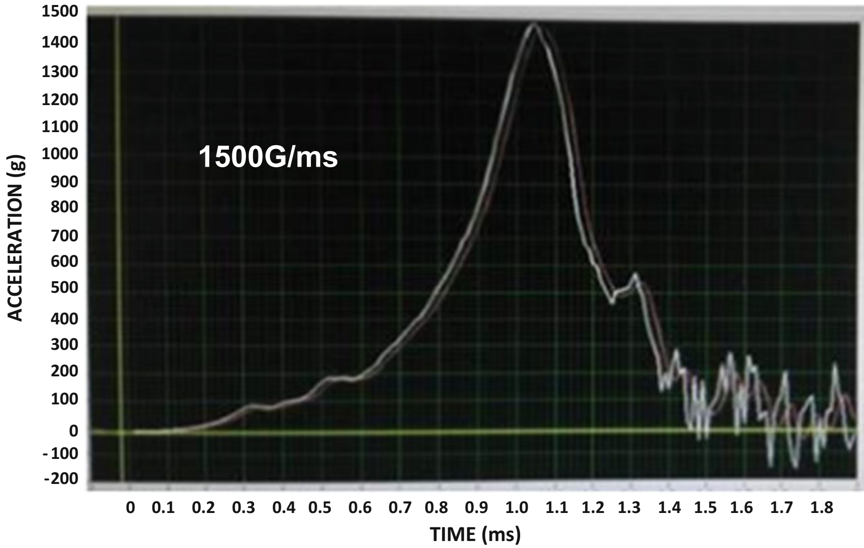


Fig. 6.42 Drop test spectrum

6.12.2 Test Results

The drop condition is 1000 drops. There are 24 samples. The ones without underfill failed very early and the failure mode is the broken of the first RDL near the solder joint as shown in Fig. 6.43.

Another 24 PCB assemblies (samples) are underfilled. The material properties of the underfill are: the filler content = 25%, the maximum filler size = 5 μm, the average filler size = 1–2 μm, the curing time and curing temperature = 8 min @ 135 °C or 5 min @ 150 °C. The Young's modulus, Poisson's ratio, and CTE are, respectively, 4–5 GPa, 0.35, and 50–52 × 10^{-6}/°C. The drop condition is also 1000 drops. The results are shown in Fig. 6.44. It can be seen that the characteristic life of the Weibull plot of the solder joint under drop test is 1187 drops and all 24 samples passed 500 drops without failure. The failure modes after 550 drips are shown in Fig. 6.45. It can be seen that the RDLs are broken. In this case, the EMC also has cracks. However, the solder joint is not failed.

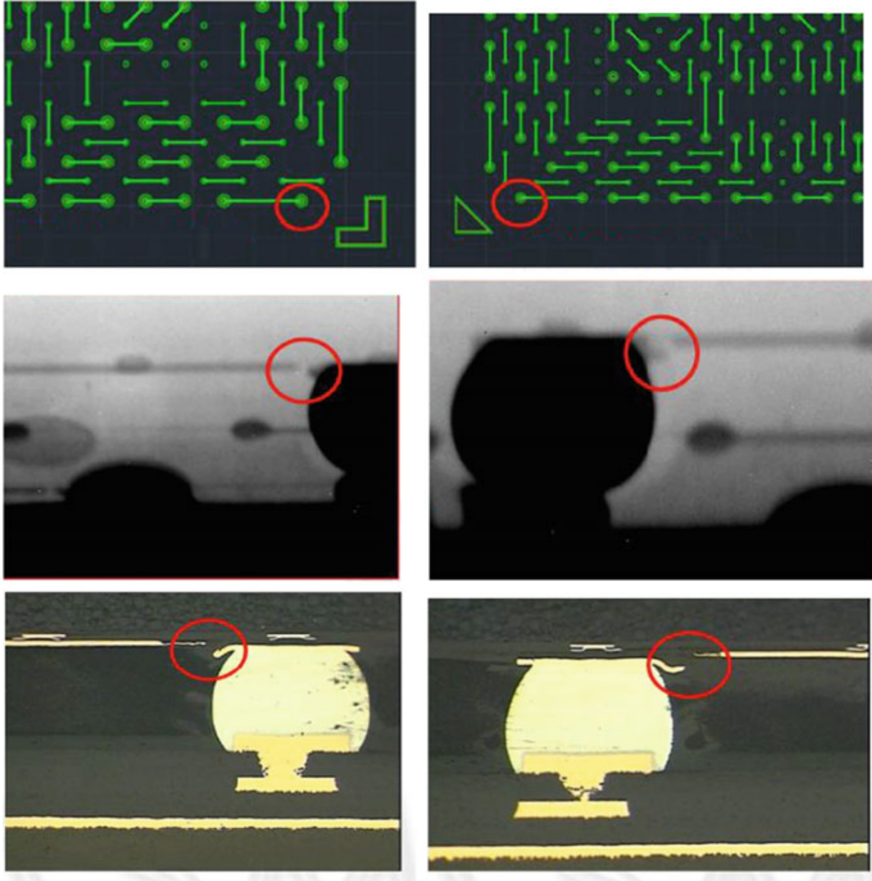


Fig. 6.43 Failure modes (broken) of the RDL1 near the solder joint

6.13 Simulation on Thermal Cycling

(A) The Structure and Boundary Conditions

The PCB assembly of the fan-out wafer-level package shown in Figs. 6.33 and 6.34 is modeled as a three-dimensional strip that captures the construction along a diagonal path from the assembly's geometry center to a corner (Fig. 6.46). Due to the symmetry about the vertical midplane of a full strip, the model is actually a half-strip with the appropriate in-plane restraints placed on one symmetry plane. Coupled in-plane translations are applied to the other symmetry plane to produce a state of generalized plane strain. Using exclusively hexahedral solid elements, the model can capture the precise shape of the packages' solder joint and potential DNP (distance to neutral point) effects while retaining significant computational efficiency over full octant models.

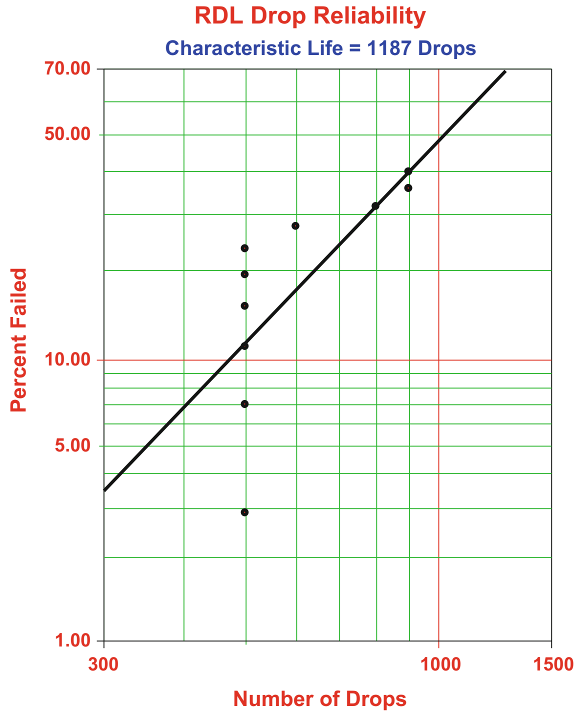


Fig. 6.44 Weibull plot of the package RDL/solder joint under drop test

Despite the overall economy of elements in the strip model, selective mesh refinement is used to concentrate highly refined elements in the solder joints where failure is anticipated. In the present PCB assembly, failure would be predicted in the solder joints with the greatest DNP (the package corner) and near the chip corners as shown in Fig. 6.46. Thus, highly refined meshes are applied to these two solder joints. The other solder joints are coarsely meshed. The C3D8R element of ABAQUS is used for the model.

(B) Material Properties for Thermal Cycling

The material properties of the PCB assembly shown in Figs. 6.33 and 6.34 are shown in Table 6.7. All the material properties are assumed to be constant except for those of solder. The Sn3 wt% Ag0.5 wt%Cu is assumed to follow the generalized Garofalo creep equation:

$$\frac{\mathrm{d}\varepsilon}{\mathrm{d}t} = 500000 \sin h^5 \left(\sigma \times 10^{-8}\right) \exp\left(\frac{-5807}{T(K)}\right)$$

where ε is the strain, σ is the stress in Pa, and K is the Kelvin.

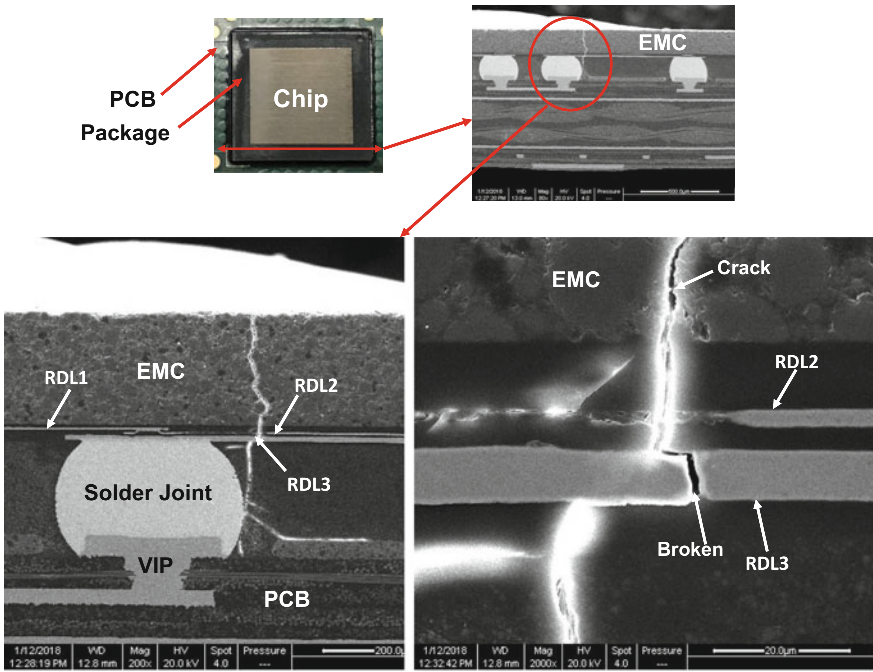
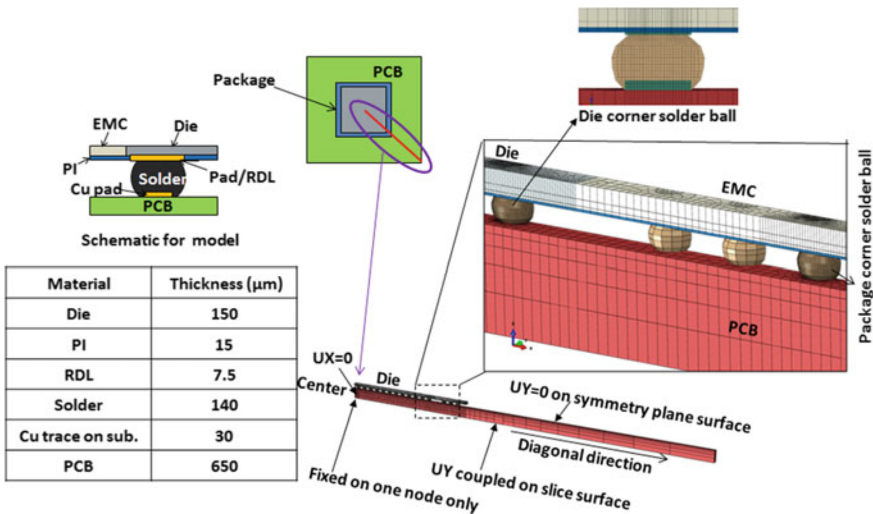


Fig. 6.45 PCB assembly for failure analysis (after 550 drops). Failure modes showing RDLs broken and EMC cracking



Material	Thickness (μm)
Die	150
PI	15
RDL	7.5
Solder	140
Cu trace on sub.	30
PCB	650

Fig. 6.46 The 3D strip model for thermal analysis

Table 6.7 Material properties for thermal cycling modeling

	CTE (ppm/°C)	Young's Modulus (GPa)	Poison's ratio
Copper	16.3	121	0.34
PCB	$\alpha_1 = 18$, $\alpha_2 = 18$, $\alpha_3 = 70$	$E_1 = 22$, $E_2 = 22$, $E_3 = 10$	0.28
Silicon	2.8	131	0.278
Solder	21.3 + 0.017T	49 – 0.07T	0.3
Polyimide	35	3.3	0.3
EMC	10(<150 °C)	19	0.25

(C) Temperature Boundary Condition

The temperature profile shown in Fig. 6.39 is to be imposed on the PCB assembly. Five temperature cycles are executed.

(D) Thermal Cycling Simulation Results

Figure 6.47 shows the shear stress and creep shear strain hysteresis loops at the solder joint under the chip corner. It can be seen that after three cycles, the creep responses converged (become stabilized). The maximum Mises stress occurs at the solder joints near the chip corner and the package corner as shown in Fig. 6.48. The location is at the interface between the bottom of the package and the bulk solder. The maximum Mises stress occurs at –40 °C during the thermal cycling condition shown in Fig. 6.39. The deformed shape of the strip model at –40 °C is shown in Fig. 6.49.

The accumulated creep strain versus time is shown in Fig. 6.50. It can be seen that the creep strain per cycle is equal to 0.0084, which is too small to create solder joint reliability problem, especially for mobile products such as smartphones, whose life is less than 3 years.

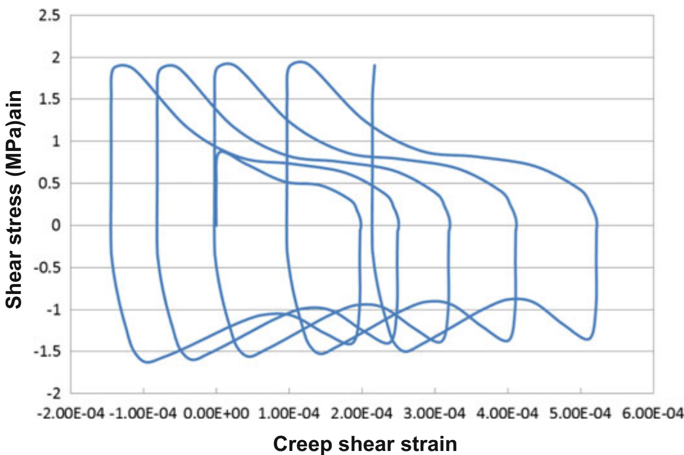


Fig. 6.47 Shear stress and creep shear strain hysteresis loops

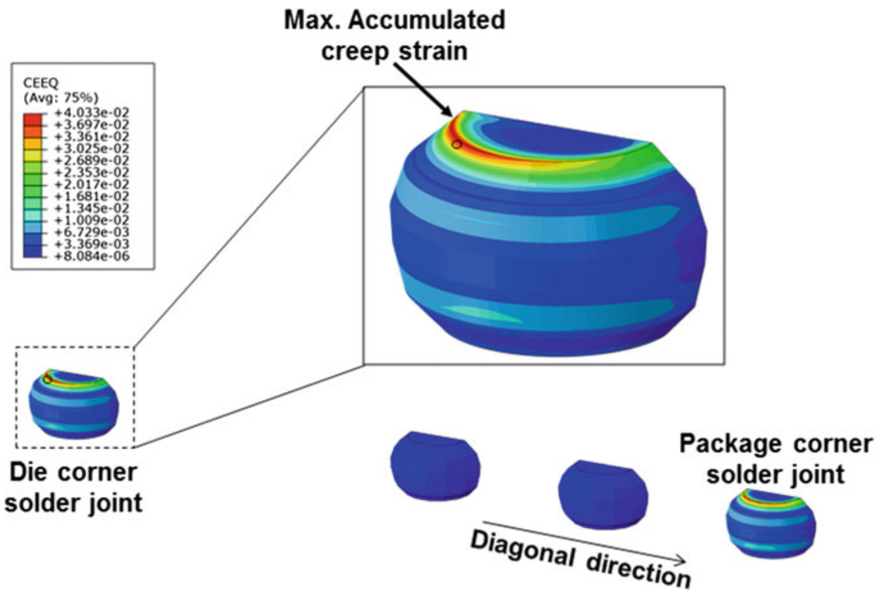


Fig. 6.48 Maximum accumulated creep strain

6.14 Simulation on Shock (Drop)

(A) Structure and Boundary Conditions

The finite element model for drop test is shown in Fig. 6.51. It can be seen that one-fourth of the PCB assembly is modeled. For simplicity, there is only one package at the center of the PCB and the package is subjected to the acceleration shown in Fig. 6.42.

During impact, the most likely failure location is near the corner solder joints of the package and the most likely failure mode is the broken Cu wire in the RDLs and broken Cu trace in the PCB. Thus, finer meshes are applied to the Cu wire of RDLs and Cu trace of PCB near the corner solder joints of the package as shown in Fig. 6.52.

(B) Material Properties for Drop

The material properties for drop analysis are shown in Table 6.8. Since the focus of this analysis is not on the solder joint, all the materials are assumed to be constant. Since the ABAQUS explicit solver is applied for the simulation. Thus, the damping effect is included through the bulk viscosity method in ABAQUS explicit solver. The bulk viscosity introduces damping associated with the volumetric straining. The damping coefficients b_1 and b_2 applied in the analysis are respectively, 0.02 and 0.

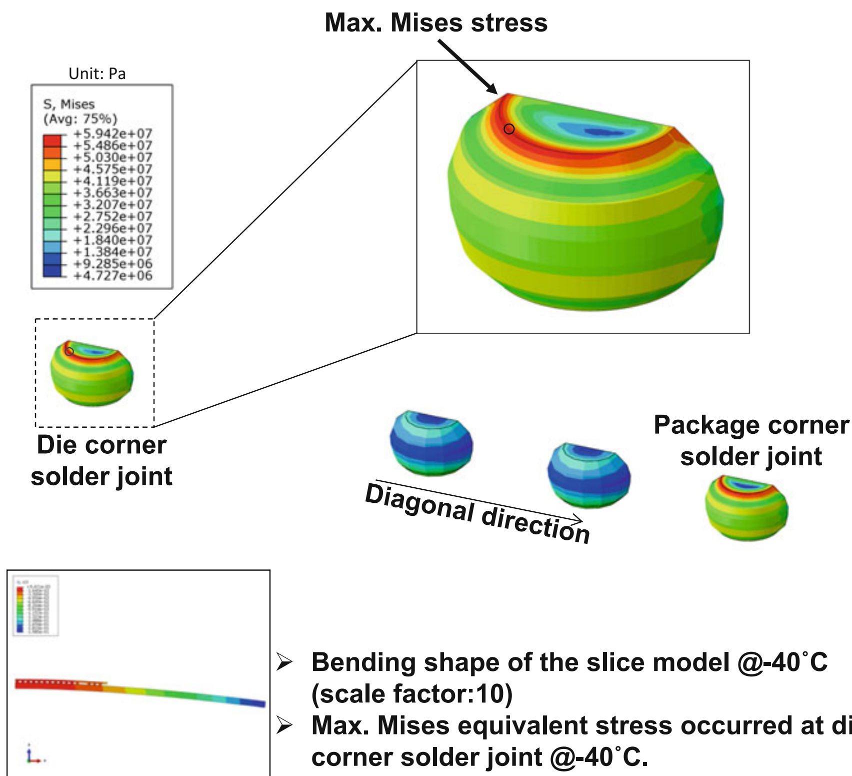


Fig. 6.49 (Top) Maximum Mises stress at chip corner and package corner solder joints at −40 °C. (Bottom) The deformed shape of the quarter structure at −40 °C

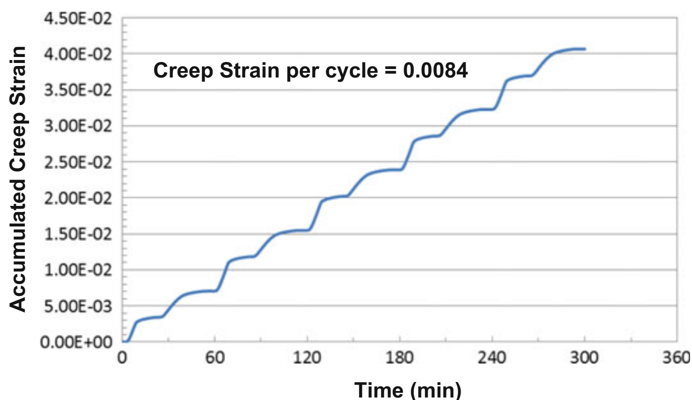


Fig. 6.50 Accumulated creep strain versus time

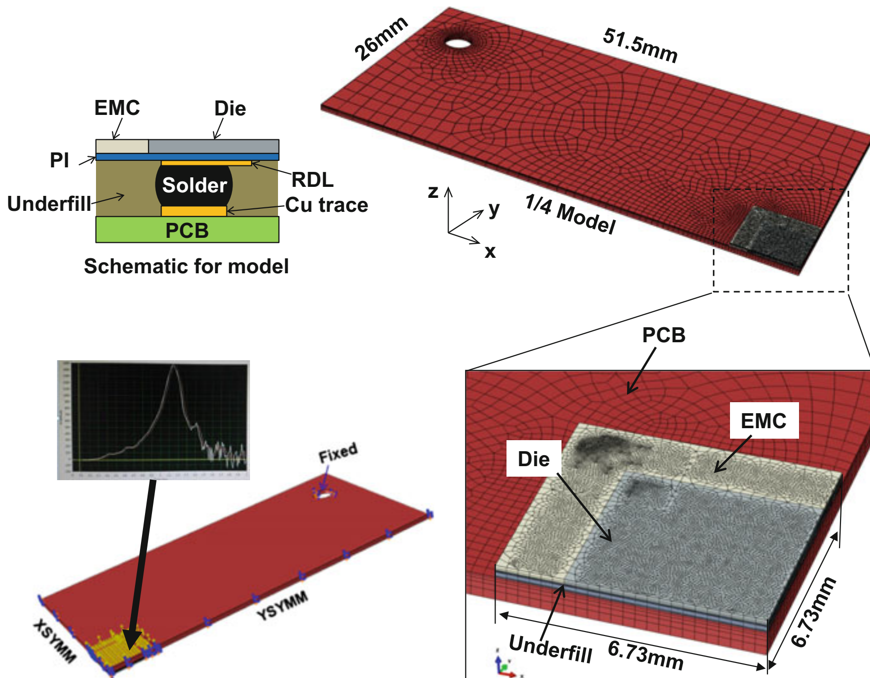


Fig. 6.51 Quarter model for drop analysis and boundary conditions

(C) Drop Simulation Results

The applied acceleration is shown in Figs. 6.42 and 6.51. The time step for the calculation is 1×10^{-8} s. The time histories of strain in the x–direction, ε_{11} (Fig. 6.51) and maximum principal strain acting at the RDL of the package corner are shown in Fig. 6.53. Basically, they behave the same, i.e., the strain is dominated in the x–direction. The maximum deflection of the PCB assembly occurs near the 0.0023 s (Fig. 6.53) and is shown in Fig. 6.52(b). The maximum principal strain = 0.0045 occurs also at that time. The deflection and strains are decreasing with time due to the damping of the structure as shown in Fig. 6.53.

The maximum Mises stress occurs at the same location (at the Cu wiring of RDL near the package corner) as the maximum principal strain as shown in Fig. 6.54 and is equals to 7.724×10^8 Pa, which occurs at 0.0023 s. Thus, any failure should occur at this location. This demonstrates the failure mode that the RDL is broken after > 550 drops during the drop test.

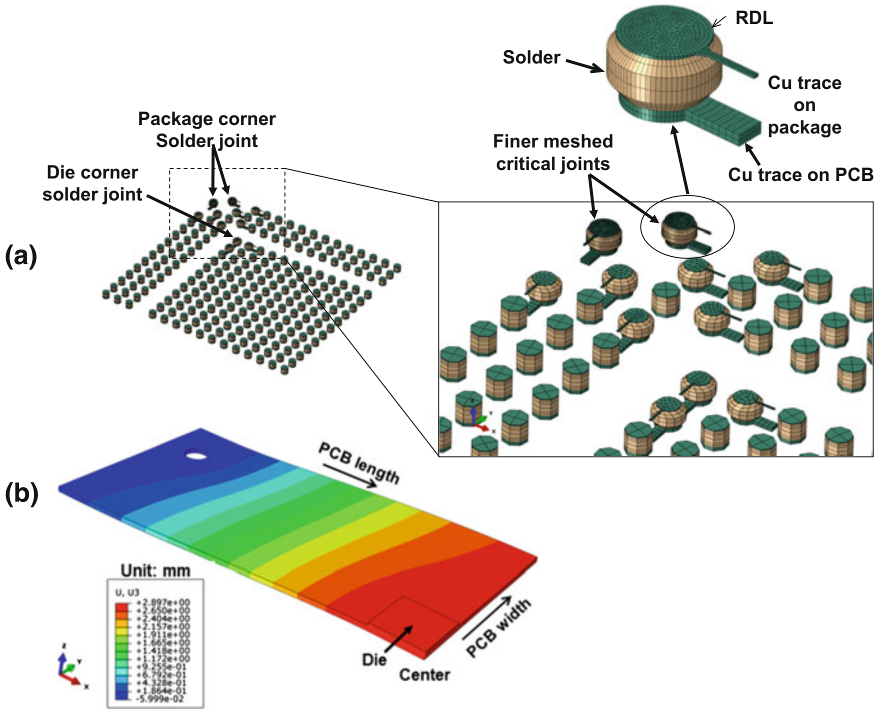


Fig. 6.52 **a** Mesh at corner solder joint, RDL on package, and Cu trace on PCB. **b** Deformed shape of the quarter of PCB assembly

Table 6.8 Material properties for drop modeling

	Density (Kg/m^3)	Young's Modulus (GPa)	Poison's ratio
Copper	8954	121	0.34
PCB	1800	$E_1 = 22$, $E_2 = 22$, $E_3 = 10$	0.28
Silicon	2330	131	0.278
Solder	7400	49	0.30
Underfill	1560	4.5	0.3
Polyimide	1420	3.3	0.3
EMC	1960	19	0.25

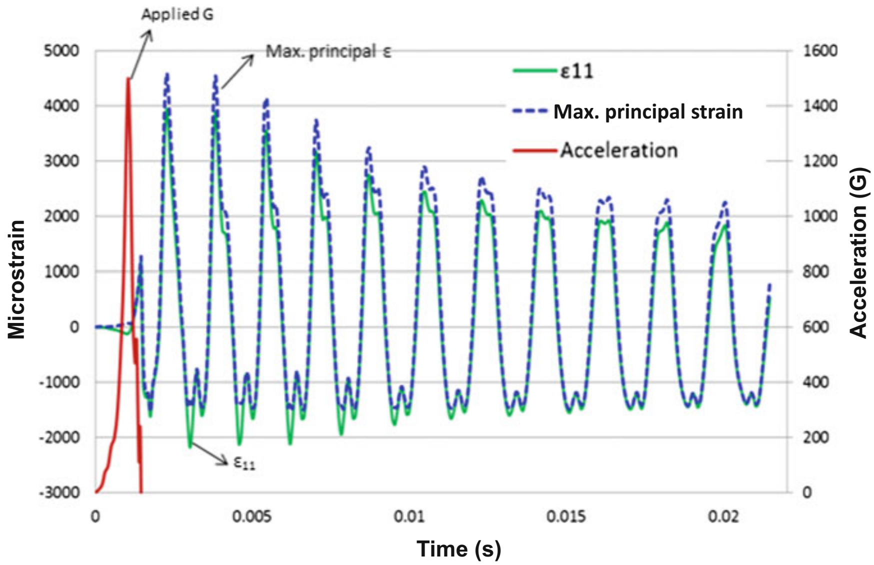


Fig. 6.53 The applied acceleration. The time-history maximum principal strain and ε_{11} at the RDL of the package

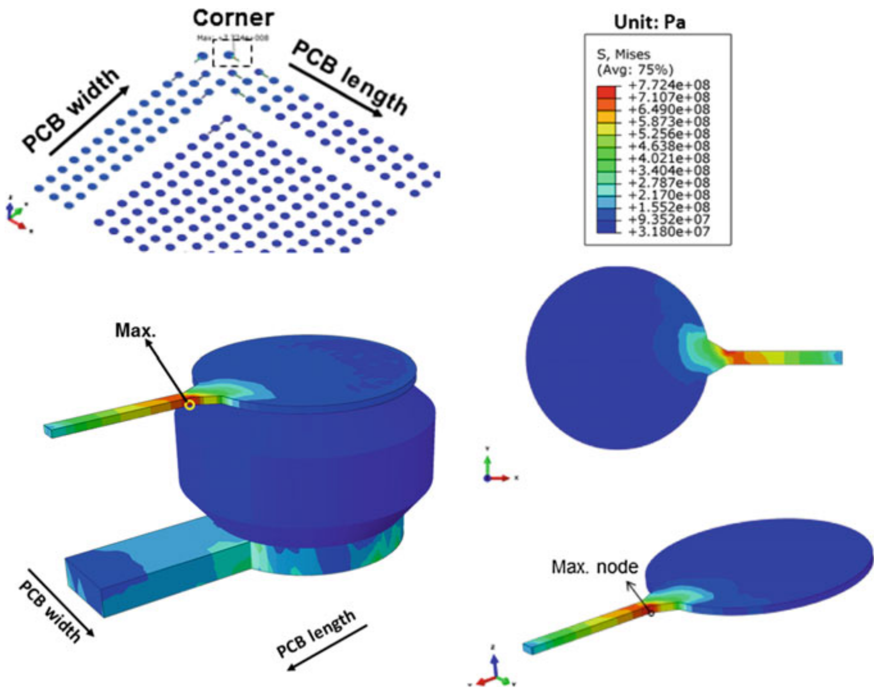


Fig. 6.54 Maximum Mises stress occurs at the RDL of the package

6.15 Summary and Recommendations

The design, materials, process, fabrication, and reliability of FOWLP with chip-first and die face-up method have been investigated in this chapter. The lessons learned from the problems and solutions have also been provided. Some important results and recommendations are summarized in the following.

- A test package, 13.42 mm × 13.42 mm, (with a package/chip ratio = 1.8 and a chip-top EMC cap = 100 μm) has been designed and fabricated. This test package has three RDLs; the line width/spacing of the first RDL is 5 μm/5 μm, of the second RDL is 10 μm/10 μm, and of the third RDL is 15 μm/15 μm.
- DAF helps! There is not any die shift issue for chip-first with die face-up FOWLP.
- The price must pay is to do the P&P pitch compensation due to the thermal expansion mismatch between the silicon chip and the glass carrier wafer during the heating of the DAF (both bond-head and the bond-stage temperature = 120 °C with the bond force of 2.0 kg for 2 s).
- For liquid EMC dispensing, in order to reduce the area and length of flow marks, the line pattern is recommended.
- Remove trap air before compression molding is a must and the optimal conditions are: temperature = 125 °C, time = 2 min, and pressure = 45 kg/cm^2. The PMC is at 150 °C for ≥ 1 h, and a dead weight = 15 kg for a better warpage control.
- For the present study, in order to have the minimum warpage (≤ 0.3 mm), the glass thickness is 1 mm and the glass thermal expansion coefficient is 8 × 10^{-6}/°C.
- During Cu revealing (backgrinding of the EMC to expose the Cu contact pads), there are Cu smears for the short (5 μm) polyimide and there is not any Cu smear for the tall (~ 30 μm) polyimide.
- Reliability thermal cycling test of a sample size of 60 package assemblies shows that the characteristic life is more than 2380 cycles, which is adequate for most applications of mobile products such as smartphones and tablets.
- Reliability drop test of a sample size of 24 package assemblies with underfill shows that all the samples passed 500 drops and the characteristic life is more than 1187 drops, which is adequate for most applications of mobile products such as smartphones and tablets.

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Chapter 7
FOWLP: Chip-Last or RDL-First

7.1 Introduction

Since 2006, NEC Electronics Corporation (now Renesas Electronics Corporation) has been developing a novel SMAFTI (SMArt chip connection with feedthrough interposer) packaging technology for inter-chip wideband data transfer [1, 2], 3D stacked memory integrated on logic devices [3–7], system in wafer-level package (SiWLP) [8], and "RDL-first" fan-out wafer-level packaging [9]. The feedthrough interposer (FTI) used in SMAFTI is a film with ultrafine line width and spacing RDLs. The dielectric of the FTI is usually SiO_2 or a polymer, and the conductor wiring of the RDLs (redistribution-layers) is Cu. The FTI not only supports the RDLs underneath within the chip but it also provides support beyond the edges of the chip. Area array solder balls are mounted at the bottom side of the FTI, which are to be connected to the PCB. EMC is used to embed the chip and support the RDLs and solder balls [10].

In 2015, Amkor announced a very similar RDL-first technology called SWIFT™ (silicon wafer integrated fan-out technology) [11]. In 2016, IME presented the large multichip RDL-first FOWLP (fan-out wafer-level packaging) on printed circuit board (PCB) [12, 13]. In 2016, SPIL demonstrated the first hybrid integration of the fine line plasma-enhanced chemical vapor deposition (PECVD) RDL and the RDL with polymeric dielectrics [14]. In 2017, Amkor announced a very similar hybrid RDLs for their SLIM™ (Silicon-Less Integrated Module) [15, 16]. In this chapter, the RDL-first or chip-last FOWLP process and the hybrid RDLs will be discussed. The reasons for chip-last or RDL-first will be briefly mentioned first.

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7.2 Reasons for Chip-Last or RDL-First FOWLP

According to [8, 9], one of the challenges of chip-first FOWLP (Chaps. 5 and 6) and the key reasons for them to introduce the chip-last or RDL-first FOWLP is the production yield during the RDL process is low because the KGDs are already embedded. This is true only if the chip-last (RDL-first) FTI is fully functionally tested before the chip-to-wafer bonding. Otherwise, the KGDs still have to be thrown away for the case of an FTI with bad RDLs after a system test. Also, it should be noted that fully functionally tests of RDLs on an FTI are not only very costly but very difficult, if not possible [10].

7.3 Methods for Chip-Last or RDL-First FOWLP

There are at least three methods for making the chip-last (RDL-first) FOWLP. One is by using PECVD to make the SiO_2 dielectric layer and Cu damascene + CMP (chemical mechanical polishing) to make the conductor layer of all the RDLs, e.g., [10]. One is by using the polymer to make the dielectric layer and Cu plating + etching to make the conductor layer for all the RDLs, e.g., [12, 13]. The third one is by using PECVD and Cu damascene + CMP to make the first fine line width and spacing RDL and then using the polymer to make the dielectric layer and Cu plating + etching to make the conductor layer for the rest of not so fine line width and spacing RDLs [14–16]. The last one is also called hybrid RDLs [14]. All these three methods will be discussed in the followings.

7.4 Chip-Last (RDL-First) by PECVD and Cu Damascene + CMP

7.4.1 Key Process Flow

Figure 7.1 shows the process flow of the chip-last with face-down or “RDL-first” FOWLP. This is very different from the chip-first FOWLP discussed in Chaps. 5 and 6. First of all, this only works on a wafer carrier. Also, RDL-first FOWLP requires (1) building up the RDLs on a bare silicon wafer (the FTI); (2) performing the wafer bumping; (3) performing the fluxing, chip-to-wafer bonding, and cleaning; and (4) performing the underfill dispensing and curing. As to wafer bumping, chip-to-wafer bonding and underfilling, please see Chap. 2 and [17]. Each of these tasks is a major undertaking and requires additional materials, process, equipment, manufacturing floor space, and personal effort. Therefore, compared to chip-first FOWLP, chip-last (RDL-first) FOWLP incurs very high cost and has a higher

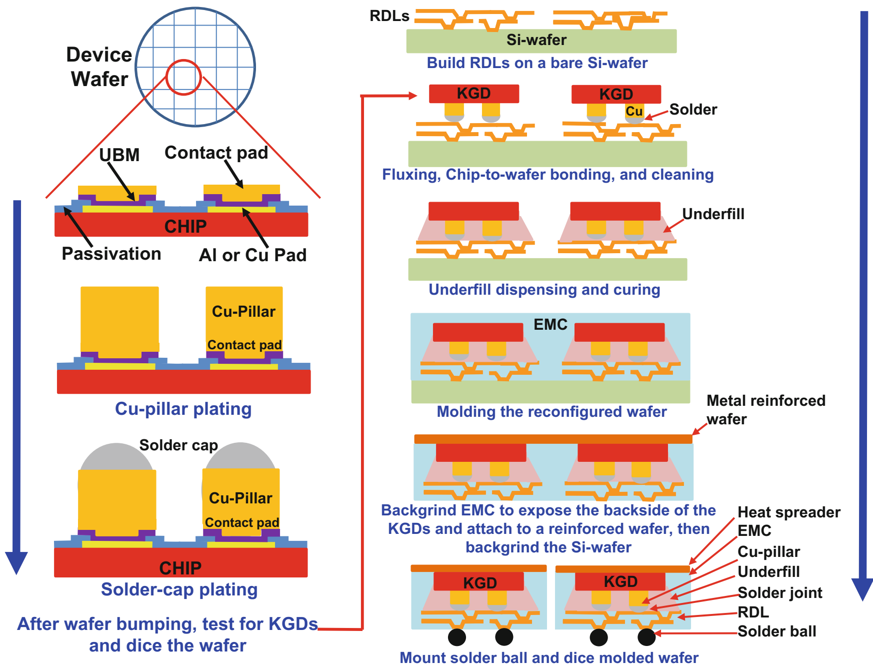


Fig. 7.1 Chip-last (RDL-first) FOWLP key process steps

probability of greater yield losses. It can only be afforded by very high-density and performance applications such as high-end servers and computers.

The very first step in RDL-first is to build the RDLs on a bare silicon wafer, which will be detailed later. On the device wafer, the first step is to perform wafer bumping as shown in Sect. 2.2. The next step is to test for KGDs and then dice the wafer into individual KGDs as shown in the left-hand side Fig. 7.1. Next, the KGDs are picked up, flux is applied, and then the KGDs are placed face-down on the contact pad (which is on top of the RDLs) of the full-thickness silicon wafer prior to performing chip-to-wafer bonding. That step is followed by cleaning the flux residue and then dispensing the underfill and curing. Next comes molding the whole reconstituted wafer carrier using the compression method with EMC (epoxy molding compound). Then, backgrinding is done to remove the silicon carrier. (Another way is to backgrind the EMC to expose the backside of the KGDs, which are attached to a metal-reinforced wafer, and then backgrinding is done to remove the silicon carrier as shown in Fig. 7.1). Finally, the solder balls are mounted on the bottom RDL and the reconstituted wafer is diced into individual packages.

7.4.2 RDLs by PECVD and Cu Damascene + CMP

Figure 7.2 shows the process flow of fabricating very fine line width/spacing (<5 μm) RDLs for chip-last (RDL-first) FOWLP. First, use PECVD to form a thin layer of SiO_2 (or SiN) on a full-thickness bare silicon wafer and then use a spin coater to laminate the photoresist. These steps are followed by using a stepper to open up the resist and a reactive ion etch (RIE) to remove the SiO_2. Then, a stepper is used to open the resist wider and RIE to etch more of the SiO_2. Next, strip off the resist, sputter the TiCu, and electrochemical deposition (ECD) the Cu on the whole wafer. These steps are followed by chemical mechanical polishing (CMP) to remove the overburden Cu and the TiCu, and then we have the first RDL1 and V01 (the via connecting the Si and RDL1) as shown in Fig. 7.2. This is called the dual Cu damascene method [18, 19]. Repeat all the processes to get the second RDL2, the third RDL3, and so forth. V12 is the via connecting RDL1 and RDL2. Figure 7.3 shows an example of fabricated RDLs by the dual Cu damascene method [18, 19]. It can be seen that there are three RDLs and on top of RDL3, there are a UBM and a Cu contact pad; the contact pad is to be connected to the microbump for chip-to-wafer bonding.

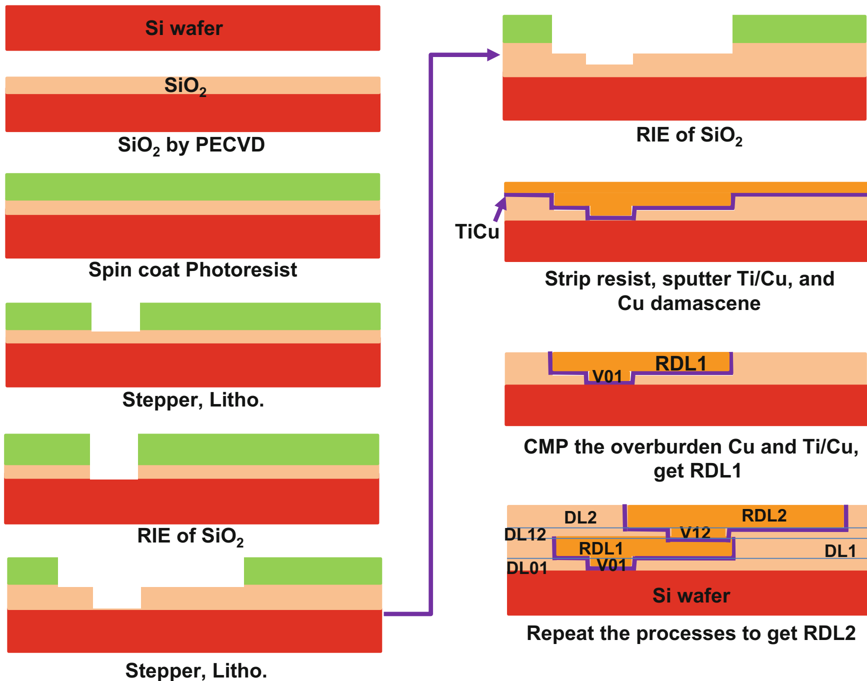


Fig. 7.2 Key process steps of RDLs by PECVD and dual Cu damascene + CMP method

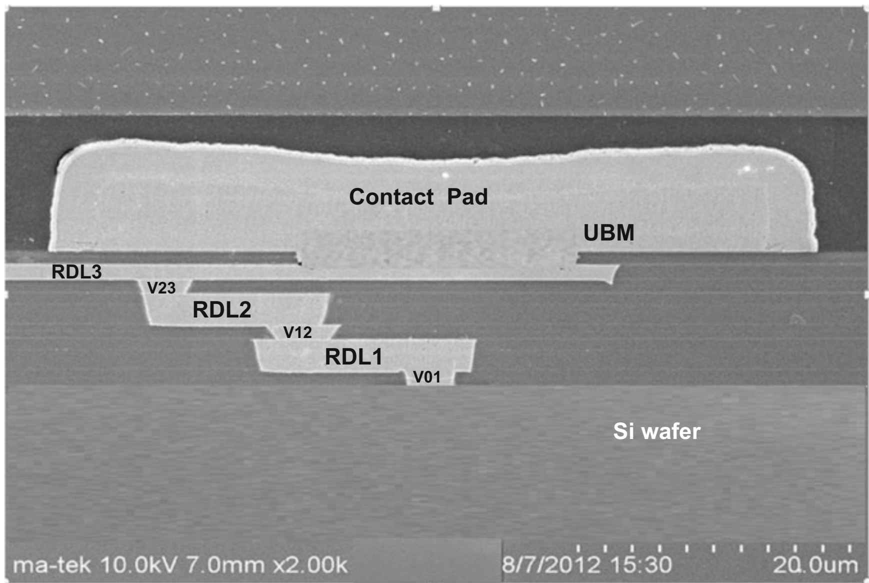


Fig. 7.3 SEM image of RDLs by PECVD and dual Cu damascene + CMP method

7.4.3 UBM/Cu Contact Pad/Solder Ball

After fluxing, chip-to-wafer bonding, cleaning, underfill dispensing and curing, and molding, it is time to remove the silicon bare wafer and attach the solder balls. Figure 7.4 shows the process flow. The steps are as follows: (1) backgrind the silicon wafer to a few microns from the via (V01), (2) then use CMP on the silicon wafer, and then (3) TiCu and passivation to expose the Cu of V01. These steps are followed by (4) PECVD to form a SiO_2 layer and then (5) spin coating a photoresist. Then, (6) use a stepper to open the resist and an RIE to remove the SiO_2, and then (7) strip off the resist. It is followed by sputtering the Ti/Cu and electroplating the Cu. Then, (8) CMP the overburden Cu and TiCu and obtain the UBM and Cu contact pad. Finally, (9) mount the solder balls on the Cu contact pads as shown in Fig. 7.4.

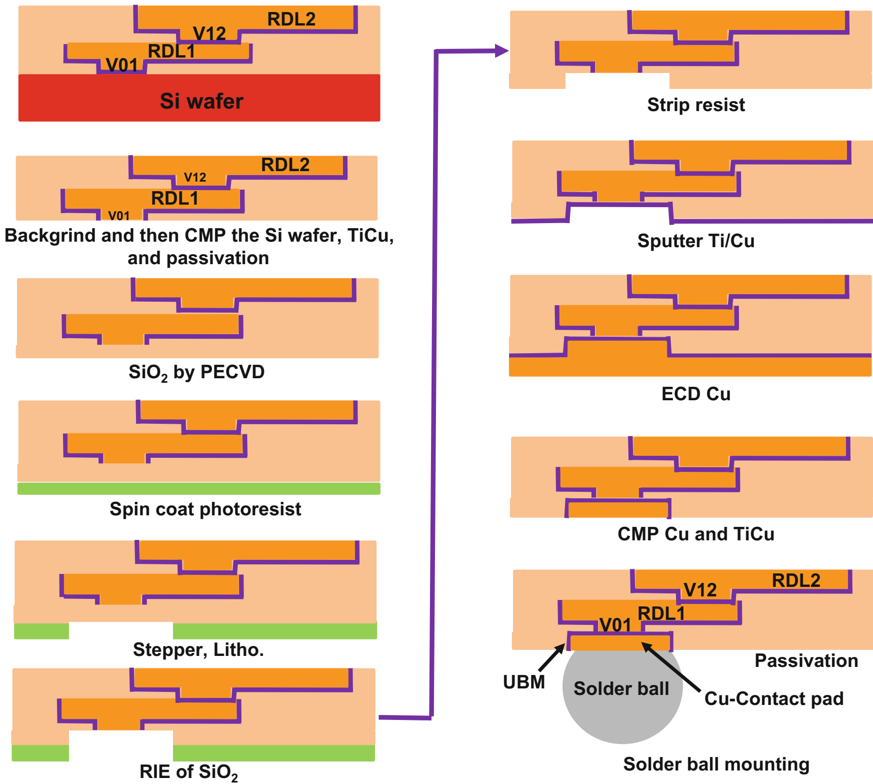


Fig. 7.4 Silicon wafer removal and solder ball mounting

7.5 Chip-Last (RDL-First) by Polymer and Cu Plating + Etching

7.5.1 Key Process Steps

Figure 7.5 shows the key process steps for chip-last (RDL-first) by polymer and Cu plating + etching. It can be seen that wafer bumping of the Cu pillar and solder cap is a must (the left-hand side of Fig. 7.5). The RDLs are built on a glass carrier coated with a sacrificial layer (Sect. 7.5.2). It is followed by fluxing, chip-to-wafer bonding, cleaning, and underfill dispensing and curing. Then, mold the reconstituted wafer with EMC by compression method. It is following by laser debonding to remove glass carrier and solder ball mounting as shown in the right-hand side of Fig. 7.5.

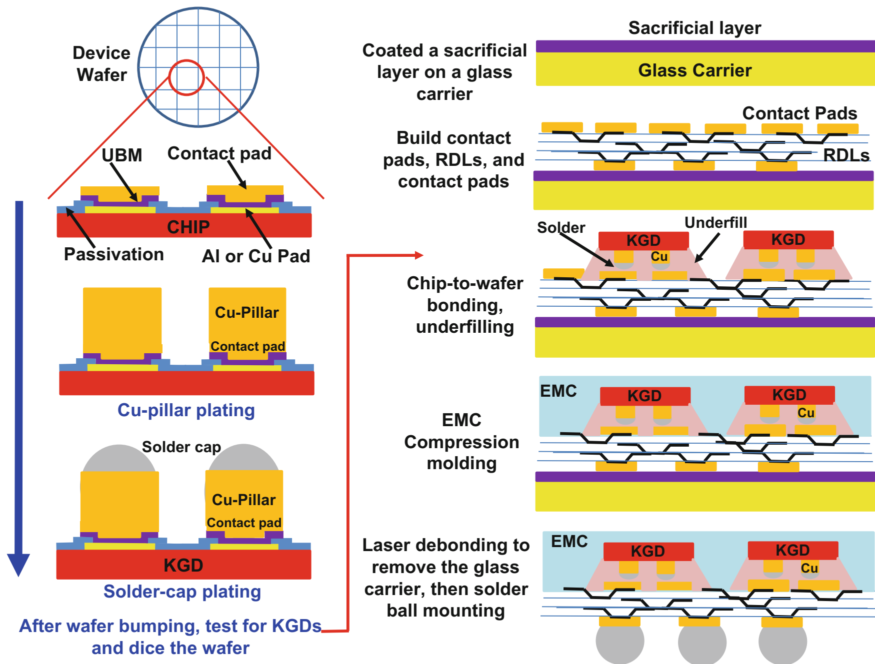


Fig. 7.5 Key process flow of chip-last (RDL-first) FOWLP by polymer and Cu plating + etching

7.5.2 RDLs by Polymer and Cu Plating + Etching

The key process steps in making the RDLs and contact pads by polymer and Cu plating + etching are basically the same as those shown in Fig. 6.21 in Chap. 6, except it used the photosensitive polymer.

7.6 Chip-Last (RDL-First) by Hybrid RDLs

7.6.1 Key Process Steps

Just like all the other chip-last (RDL-first) FOWLP, wafer bumping is a must, which is omitted in this section. The key process steps for chip-last by hybrid RDLs are shown in Fig. 7.6. It can be seen that a glass carrier-1 is coated with a sacrificial layer as shown in Fig. 7.6a. Then, the contact pad and the first RDL (RDL1) are fabricated by the PECVD for the SiO_2 dielectric layer, and dual Cu damascene + CMP for the conductor layer (Fig. 7.6b). The remaining RDLs are fabricated by the polymer and Cu plating + etching method (also called organic RDLs). Attach another carrier-2 to the other side of the reconstituted wafer,

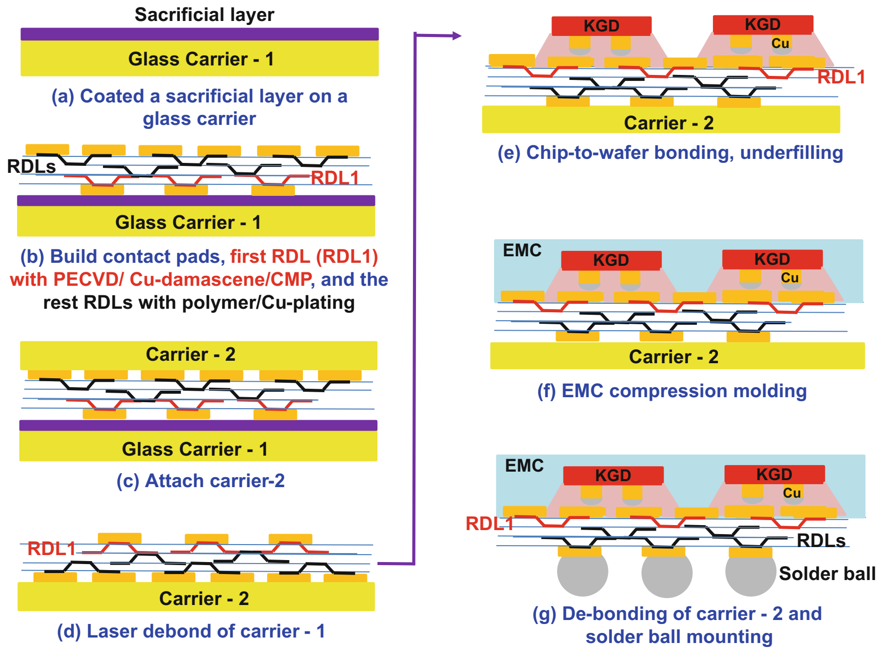


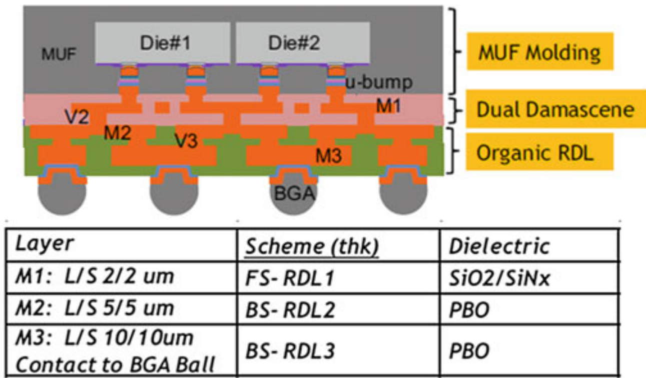
Fig. 7.6 Key process flow of chip-last (RDL-first) FOWLP with hybrid RDLs

Fig. 7.6c. It is followed by laser debonding of the carrier-1 as shown in Fig. 7.6d. It is followed by fluxing, chip-to-wafer bonding, cleaning, underfill dispensing, and curing as shown in Fig. 7.6e. Then, mold the reconstituted wafer with EMC by compression method, Fig. 7.6f. It is following by debonding the carrier-2 and solder ball mounting as shown in Fig. 7.6g.

7.6.2 *Examples of Hybrid RDLs*

Figure 7.7 shows the drawing and SEM (scanning electron microscope) images of a chip-last (RDL-first) FOWLP with hybrid RDLs fabricated by SPIL [14]. It can be seen that the line width and spacing of the first RDL (M1) are 2 μm, of the second RDL2 (M2) are 5 μm, and of the third RDL3 (M3) are 10 μm. The dielectric material for RDL1 is SiO_2, and for RDL2 and RDL3 is PBO (polybenzoxazole). Instead of the capillary underfill and EMC, they used the MUF (molded underfill).

Figures 7.8 and 7.9 show the images of a RDL-first (chip-last) FOWLP with hybrid RDLs fabricated by Amkor [15, 16] for their SLIM™. It can be seen that the size of the package is 15 mm × 15 mm. The line width and spacing of the first RDL1 are 0.5 μm, of the second RDL2 are 5 μm, and of the third RDL3 are 10 μm. The dielectric material for RDL1 is SiN or SiO_2, and for RDL2 and RDL3 is a



Layer	Scheme (thk)	Dielectric
M1: L/S 2/2 um	FS- RDL1	SiO2/SiNx
M2: L/S 5/5 um	BS- RDL2	PBO
M3: L/S 10/10um Contact to BGA Ball	BS- RDL3	PBO

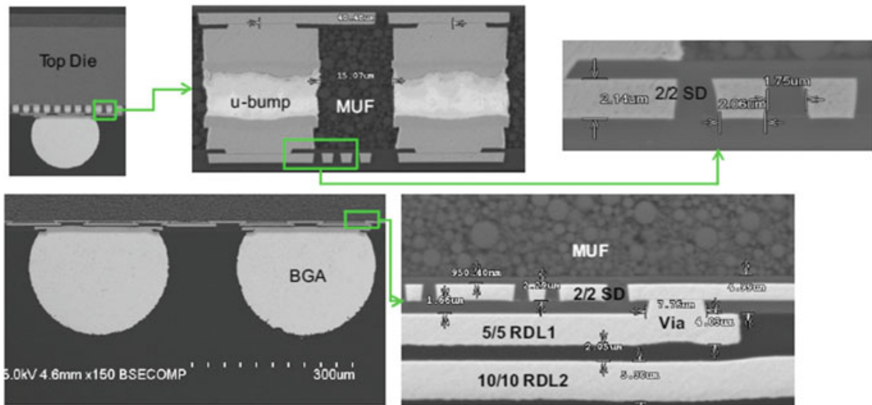


Fig. 7.7 SPIL's chip-last FOWLP with hybrid RDLs

polymer. The chip-to-wafer bonding is mass reflowed even the pitch of the microbumps is only 30 μm. The capillary underfill is dispensed and cured and EMC is compression molded.

7.7 Summary and Recommendations

Different methods in making the FOWLP with chip-last (RDL-first) have been presented. Also, three different processes in fabricating the RDLs have been provided. Some important results and recommendations are as follows:

- The first method of making the FOWLP with RDL-first is by using PECVD to make the SiO_2 (or SiN) dielectric layer and Cu damascene + CMP to make the conductor layer of all the RDLs, which are called the inorganic RDLs.

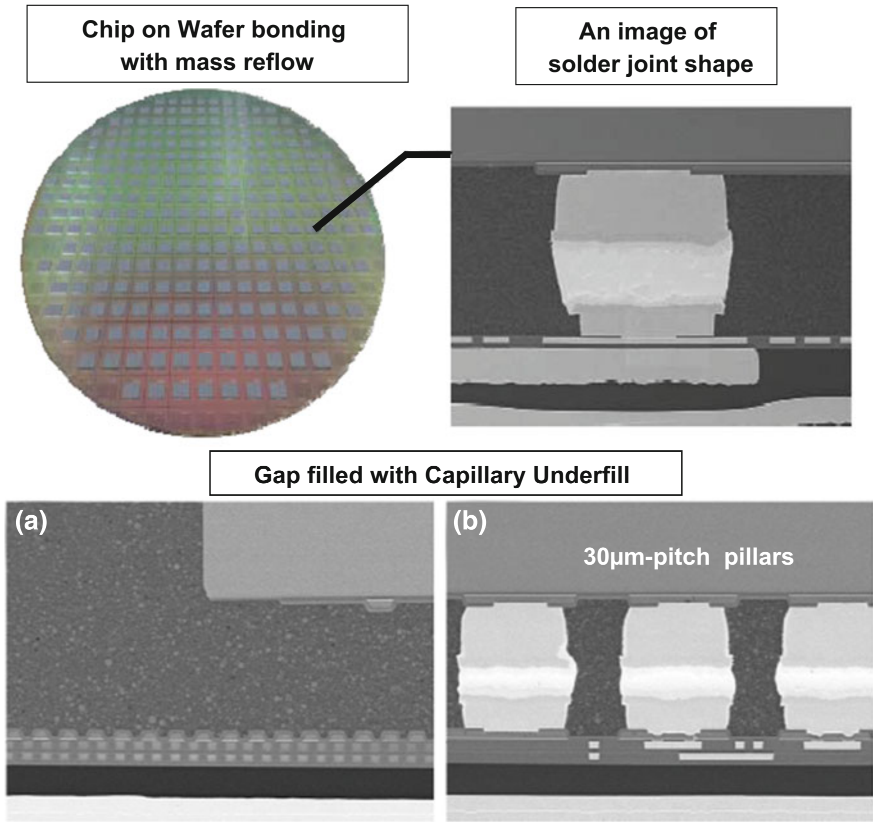


Fig. 7.8 Amkor's chip-last FOWLP with hybrid RDLs

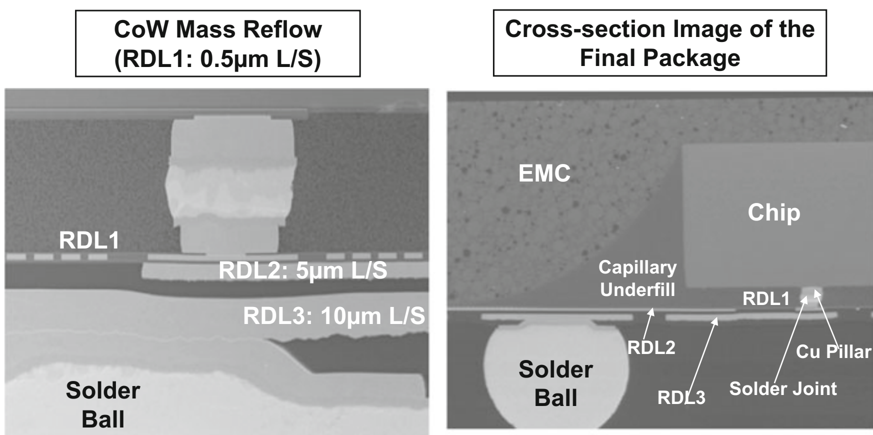


Fig. 7.9 Amkor's chip-last FOWLP with very fine line width and spacing (0.5 μm) hybrid RDLs

- The second method in making the FOWLP with RDL-first is by using the polymer to make the dielectric layer and Cu plating + etching to make the conductor layer for all the RDLs, which are called organic RDLs. A simpler process can be achieved by the photosensitive polymer as shown in Sect. 6.8.7.
- The third method in making the FOWLP with RDL-first is by using PECVD and Cu damascene + CMP to make the first fine line width and spacing RDL and then using the polymer to make the dielectric layer and Cu plating + etching to make the conductor layers for the rest of not so fine line width and spacing RDLs. This is the so-called hybrid RDLs method.
- Because of wafer bumping, fluxing, chip-to-wafer bonding, cleaning, underfill dispensing and curing, etc., compared to chip-first FOWLP, chip-last (RDL-first) FOWLP incurs very high cost and has a higher probability of greater yield losses. It can only be afforded by very high-density and performance applications such as high-end servers and computers.
- On the other hand, for high-density and performance applications, why insist on the FOWLP technology because there are many packaging alternatives.

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Chapter 8
FOWLP: PoP

8.1 Introduction

Package-on-package (PoP) has been used for housing the application processor (AP) chipset for a few years as shown in Fig. 2.17. Usually, the top package is used to house the mobile memory and the bottom package is used to house the AP. STATS ChipPAC proposed a PoP for the AP chipset with the FOWLP technology [1, 2]. During ECTC2016, TSMC presented two papers on FOWLP: one is their integrated fan-out (InFO) wafer-level packaging [3–8] for housing the most advanced AP for mobile applications [9], and the other is to compare the thermal and electrical performance between their InFO technology and the conventional flip chip on buildup package substrate technology [10]. In September 2016, TSMC put the PoP of AP chipset with FOWLP technology into high-volume manufacturing (HVM).

This is very significant since this means that FOWLP is not just only for packaging baseband, power management IC, radio frequency (RF) switch/transceiver, RF radar, audio codec, microcontroller unit, connectivity ICs, etc. as shown in Chap. 5, but it can also be used for packaging high-performance and large (>120 mm^2) system-on-chip (SoC) such as APs. TSMC used chip-first and die face-up [3–15] FOWLP processing as shown in Chap. 6. In this chapter, PoP for AP chipset with FOWLP technology by STATS ChipPAC and TSMC will be presented and discussed.

8.2 STATS ChipPAC's PoP for AP Chipset with eWLB

The first concept of using FOWLP to house the AP chipset in a PoP format was proposed by STATS ChipPAC in 2010 [1]. In 2012, they demonstrated the feasibility of the concept [2].

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8.2.1 The Structure

Figures 8.1, 8.2, and 8.3 show, respectively, the schematic of and the SEM (scanning electron microscope) images of the cross sections of the PoP for the AP chipset by FOWLP technology developed by STATS ChipPAC. It consists of a bottom package which is a fan-out embedded wafer-level ball grid array package (eWLB) or FOWLP and a top package which is a memory package. It can be seen that (a) the eWLP contains the logic, baseband, or application processor; (b) the eWLB is only 450 μm thick; (c) the top package is 520 μm thick and is housing the memory chips with wire bonding; and (d) the interconnection is from the PCB, solder balls, redistribution layers (RDLs), to processor, and solder balls, memory substrate, to the memory chips. The interconnections between the top package and the bottom package are through the solder, which is filled into the via hole of the EMC ablated by laser as shown in Figs. 8.2 and 8.3. This package is a potential candidate for mobile and wearable products.

8.2.2 Structural Warpages

Two package sizes are considered, namely 12 mm × 12 mm and 14 mm × 14 mm. The warpage results are shown in Fig. 8.4. It can be seen that (1) in general,

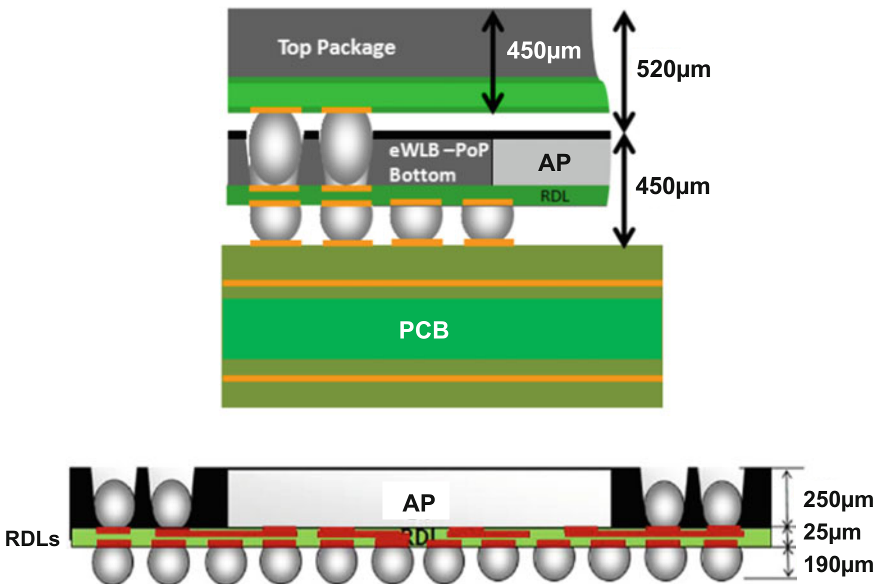


Fig. 8.1 STATS ChipPAC's PoP with FOWLP for the application processor chipset

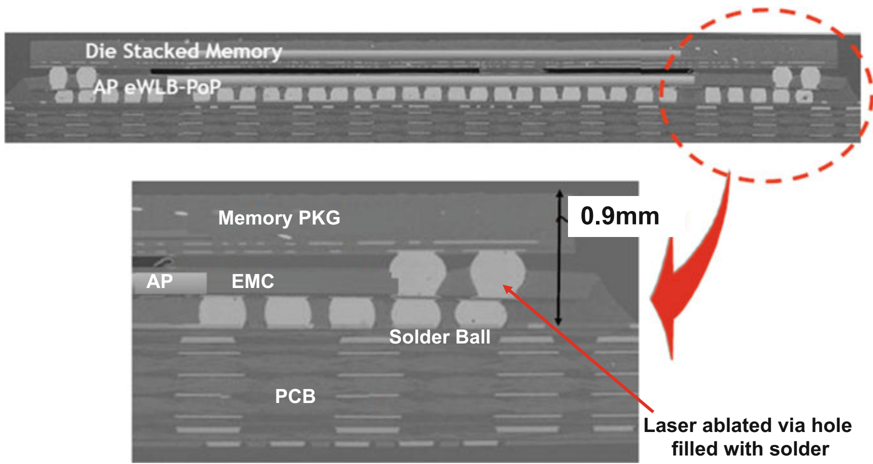


Fig. 8.2 SEM images of STATS ChipPAC's PoP with FOWLP for the application processor chipset and through mold via filled with solder

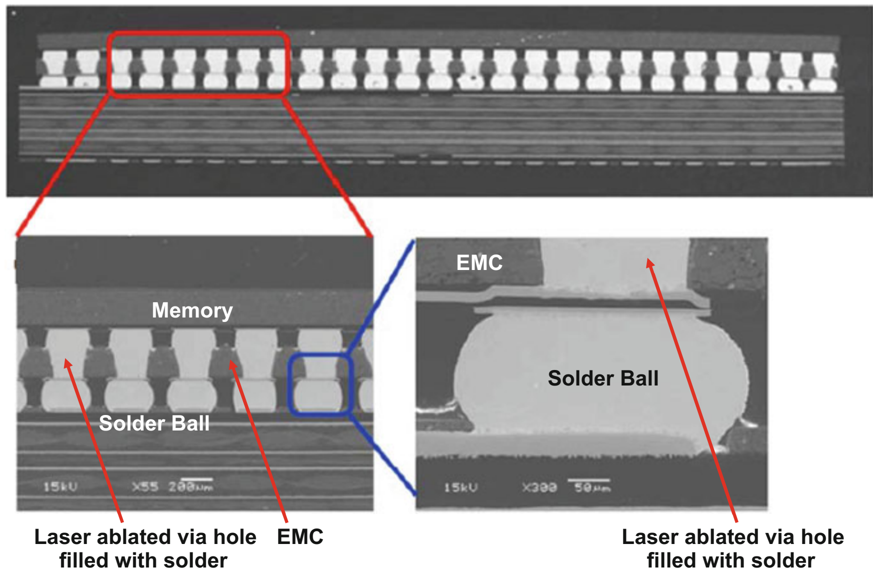


Fig. 8.3 SEM images of STATS ChipPAC's PoP with through mold via filled with solder

the larger the package size the larger the warpage, (2) the largest warpage of the 196 mm^2 package is ±50 µm, and (3) the largest warpage of the 144 mm^2 is ±40 µm. These values are within the allowable (±100 µm).

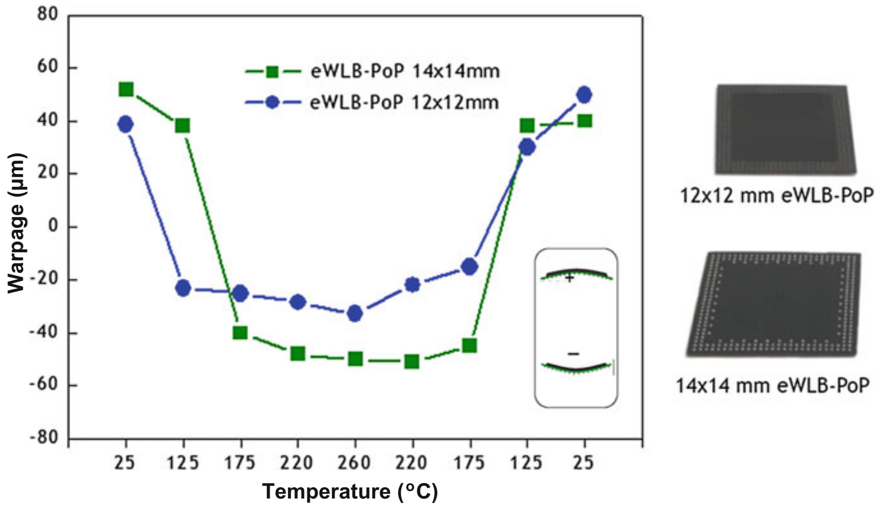


Fig. 8.4 Individual package warpage versus temperature

8.2.3 Component-Level Reliability Assessments

Two package sizes are considered, namely 10 mm × 10 mm and 14 mm × 14 mm. Both packages go through component-level reliability assessments. The tests and conditions are (1) MSL1 + 3X Reflows (JESD20-A120): 85 °C/85%RH @ 168 h, (2) Unbiased HAST (w/MSL1) (JESD22-A118): 130 °C/85%RH @ 168 h, (3) Temperature Cycling (TC-B, w/MSL1) (JESD22-A104): −55 to 125 °C; 2 cycles/h @ 1000 cycles, and (4) High-Temperature Storage (HTS w/o PC) (JESD22-A103): 150 °C @ 1000 h. Both packages passed all the tests [2].

8.2.4 Board-Level Reliability Assessments

Two package sizes are considered, namely 10 mm × 10 mm and 14 mm × 14 mm. Both packages go through board-level drop reliability assessments. The JEDEC Standard JESD22-B111 is adopted for the drop test. The first failure of the 10 mm × 10 mm package is 161 drops and that of the 14 mm × 14 mm package is 98 drops. These are more than adequate for most drop reliability.

The 10 mm × 10 mm package goes through the board-level thermal cycling test (JEDEC Standard JESD, −40 to 125 °C on an 8-layer board). The 10 mm × 10 mm package passed 1000 cycles without failure.

8.3 TSMC' PoP for AP Chipset with FOWLP

During September 2016, TSMC HVM the AP (A10) with their InFO-PoP technology. In September 2017, again TSMC HVM the AP (A11) with their InFO-PoP technology. A10 and A11 are SoC (system-on-chip) designed by Apple, please read Chap. 11 for more information.

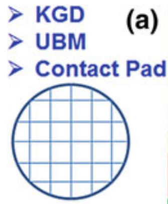
8.3.1 TSMC' InFO

One of the most famous FOWLPs is TSMC' integrated fan-out WLP (InFO-WLP). Figure 8.5 shows a typical cross section of the InFO-WLP [16]. It starts off by KGD testing of a device wafer. Then, under bump metallization (UBM) is performed by sputtering (e.g., Ti/Cu) with physical vapor deposition (PVD), and the Cu contact pad (or post) accomplished using electroplating. These steps are followed by spin coating a polymer [e.g., polyimide (PI), benzocyclobutene (BCB), or polybenzobisoxazole (PBO)] on the top of the whole wafer and laminating a die-attach film on the bottom of the whole wafer, and then singulating the device wafer into individual dies (Fig. 8.5a). The individual KGD is placed (face-up) on a temporary round glass carrier with a LTHC (light to heat conversion) layer as shown in Fig. 8.5b, and then compression molding is done on the whole temporary carrier with KGDs to form the molded reconstituted wafer (Fig. 8.5c). It is followed by backgrinding the EMC of the reconstituted wafer to expose the Cu contact pad (Fig. 8.5d), building up the RDLs, and mounting the solder ball (Fig. 8.5e). Finally, remove the temporary carrier by a laser and singulate the reconstituted wafer into individual units, and then we have the fan-out package (Fig. 8.5f) by InFO-WLP.

8.3.2 TSMC' InFO-PoP for AP Chipset

TSMC have been working on a new package-on-package (PoP) called InFO-PoP for the application processor (AP) chipset (mobile DRAM + AP SoC). Just like TSMC' CoWoS (chip-on-wafer on substrate) technology (please see Chap. 10), they called this PoW (package-on-wafer) technology [6]. PoW means the mobile DRAM package is stacked on the AP InFO reconstituted wafer and the connection between the memory package and the AP InFO package is by through InFO via (TIV). If this happens, then the wafer bumping, flip chip assembly, flux cleaning, underfill, and package substrate are eliminated, and it results into a lower profile and cost PoP.

During September 2016, TSMC put the AP chipset with their InFO-PoP technology into HVM—the very first in the world. Figures 8.6 and 8.7 show the schematic and the SEM images of the cross sections of the PoP for the AP (A10)


➢ KGD
➢ UBM
➢ Contact Pad
(a)
Polymer
UBM
Cu Contact Pad
Cu post
Pad
Passivation
Pad
SiO_2
Si
Chip
Die attach film
(b)
Polymer
Cu post
UBM
Cu Contact Pad
Pad
Passivation
Pad
SiO_2
Si
Chip
Die attach film
LTHC
Temporary round glass carrier
(c)
EMC
Polymer
Cu Contact Pad
UBM
Cu post
Pad
Passivation
Pad
SiO_2
Si
Chip
Die attach film
Temporary round glass carrier
LTHC
(d)
EMC
Polymer
Cu post
UBM
Cu Contact Pad
Pad
Passivation
Pad
SiO_2
Chip
Si
Die attach film
Temporary round glass carrier
LTHC
(e)
Solder Ball
UBM
Solder Ball
UBM
RDL
RDL
Polymer/Dielectric
Polymer/Dielectric
EMC
Polymer
Cu post
UBM
Cu Contact Pad
Pad
Passivation
Pad
SiO_2
Chip
Si
Die attach film
Temporary round glass carrier
LTHC
(f)
Die attach film
Si
Chip
SiO_2
EMC
Pad
Passivation
Pad
Cu Contact Pad
UBM
Cu post
Polymer
Polymer/Dielectric
Polymer/Dielectric
RDL
RDL
Solder Ball
UBM
Solder Ball
UBM

◂**Fig. 8.5** **a** Test for KGD. Electroplate Cu contact pads and then spin coat a polymer on top of the wafer. Laminate a DAF at the bottom of the wafer. **b** Singulate the wafer into individual KGD and place it face-up on a LTHC-coated glass reconstituted wafer. **c** Compression molding an EMC. **d** Backgrind the EMC to explore the Cu contact pads. **e** Build up the RDLs and mount the solder balls. **f** De bond the glass carrier by a laser and singulate the reconstituted wafer

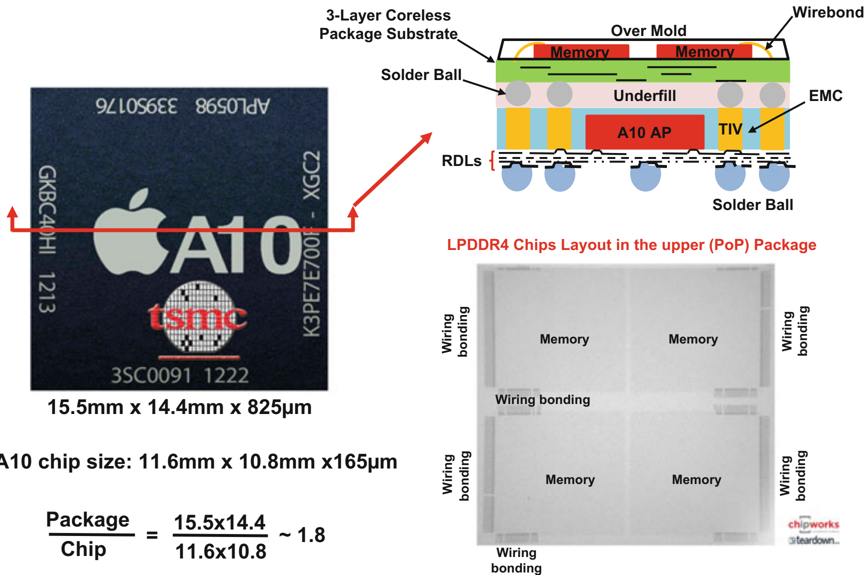


Fig. 8.6 PoP for Apple's iPhone 7 AP chipset

chipset by InFO-WLP technology manufactured by TSMC. It can be seen that (1) the dimensions of the A10 are 11.6 mm × 10.8 mm × 150 μm, (2) the package dimensions are 15.5 mm × 14.4 mm × 825 μm, (3) the package/chip ratio = 1.8, (4) there are 3 RDLs, (4) the TIV (through InFo via) is electroplated with Cu, (5) the mobile DRAMs are wirebonded on a three-layer coreless package substrate, (6) the DRAMs and the wires are over molded, (7) there are 386 solder balls (at 0.3 mm pitch) between the top package and the bottom package, (8) there is underfill between the top and bottom packages, (9) there are ~1300 solder balls (at 200 μm diameter and 0.4 mm pitch) at the bottom package, and (10) there is underfill between the PoP and the PCB (printed circuit board).

Figure 8.8 shows the schematic and SEM images of the PoP for the AP (A11) chipset by InFO-WLP technology HVM by TSMC during September 2017. Basically, the PoP for both APs (A10 and A11) is very similar. However, because TSMC used 10 nm process technology to fabricate the A11 (instead of the 16 nm process technology for the A10), the chip dimensions are much smaller (10 mm × 8.7 mm × 150 μm), ~30% chip area reduction from A10. Since the dimensions of the new package do not change much (13.9 mm × 14.8 mm), only ~8%

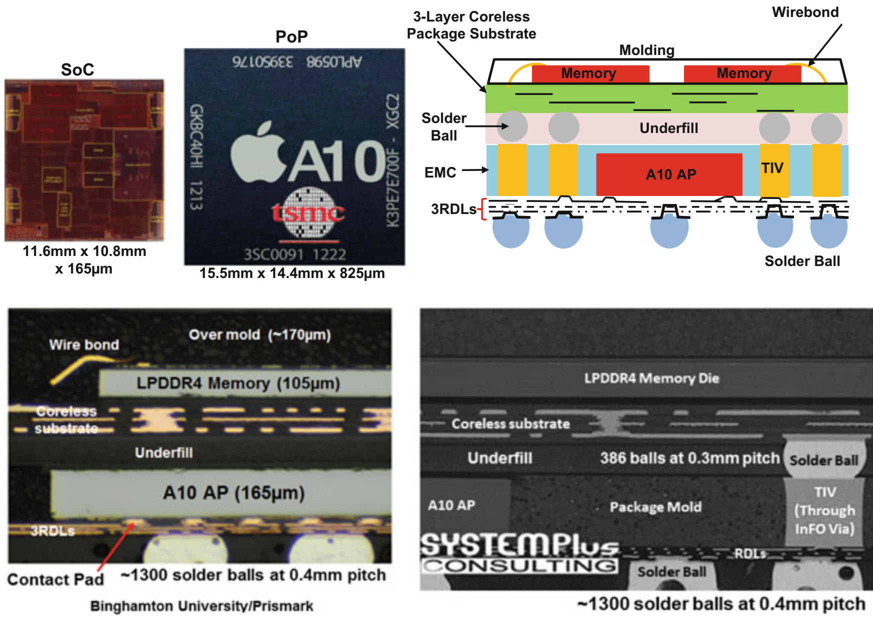


Fig. 8.7 PoP for Apple's iPhone 7 showing the FOWLP for the AP chipset

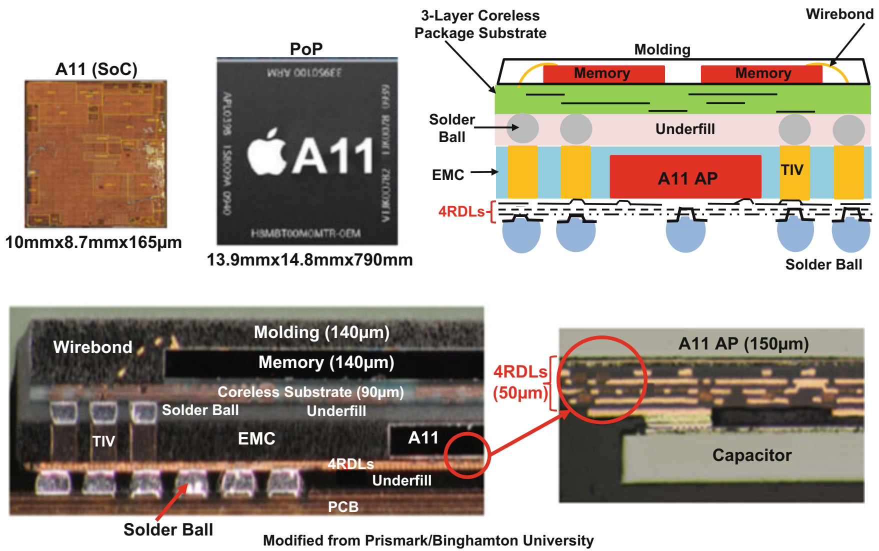


Fig. 8.8 PoP for Apple's iPhone 8 showing the FOWLP for the AP chipset

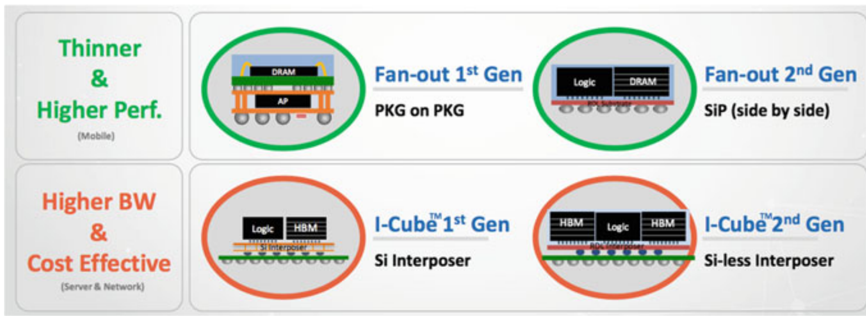


Fig. 8.9 Samsung's next generation packaging technology for housing the AP chipset

package area reduction from the old one, thus the package/chip ratio of A11 increases from 1.8 to 2.3. Also, the number of RDLs increases from 3 to 4. The line width and spacing of those 4 RDL are 10 μm.

8.4 Summary and Recommendations

PoP for AP chipset with FOWLP technology by STATS ChipPAC and TSMC have been presented and discussed. Some important results and recommendations are summarized as follows.

- The first concept on using FOWLP to house the AP chipset in a PoP format was proposed and demonstrated by STATS ChipPAC. They showed that the package warpage is within the allowable limit. Also, they showed that the package is qualified with most JEDEC component standards and the solder joints are reliable under the board-level drop and thermal cycling tests.
- The first HVM of PoP for AP chipset with FOWLP is by TSMC' InFO-PoP technology. They showed that [9, 10] the InFO-PoP is better than the conventional PoP (Fig. 2.17) in (a) package profile, (b) electrical performance, and (c) thermal performance.
- Recently, Samsung announced their packaging technology for their AP chipset. They proposed that (Fig. 8.9) the application processor (logic) and the mobile DRAM are placed side-by-side and communicated by RDLs (they called it RDL interposer, or Si-less interposer)—a heterogeneous integration. For more information about heterogeneous integration by FOWLP on AP chipset, please read Chap. 11.

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Chapter 9
Fan-Out Panel-Level Packaging (FOPLP)

9.1 Introduction

All previously mentioned fan-out technologies are using the round 200 or 300 mm wafers as the temporary carriers for making the molds, RDLs, etc. (This is because of the existing equipment for fabricating the device wafers.) In order to increase the throughput, fan-out panel-level packaging (FOPLP) has been proposed. For examples, starting from EPTC2011, J-Devices have been presenting their FOPLP (320 mm × 320 mm) called WFOP™ (Wide Strip Fan-Out Package) [1–3]. Starting from ECTC2013, Fraunhofer has been presenting their evaluation results on compression molding of a large area (610 mm × 457 mm) FOPLP [4–6]. At ECTC2014, SPIL published two papers on FOPLP called P-FO: one is to develop and characterize a 370 mm × 470 mm P-FO [7] and the other is to measure their warpage [8]. One of the bottlenecks for FOPLP is the availability of panel equipment such as the spin coating, physical vapor deposition, electrochemical deposition, etching, backgrinding, dicing, etc. for making the RDLs, molds, etc. due to the lack of the standard of panel sizes. Thus, the potential FOPLP users are unanimously calling for the panel-size industry standards.

9.2 J-Devices' WFOP™

J-Devices is the first company to use panel for making the fan-out packages. The structure and key process steps of J-Devices' WFOP™ will be briefly mentioned in this section.

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https://doi.org/10.1007/978-981-10-8884-1_9

9.2.1 Structure of J-Devices' WFOP™

The structure of J-Devices' WFOP™ is shown in Fig. 9.1. It can be seen that there is no epoxy molding compound (EMC). However, there is a metal plate to support the whole package. Their RDLs (redistribution layers) are fabricated by a printed circuit board (PCB) technology [1–3] called semi-additive process (SAP).

9.2.2 Key Process Steps of J-Devices' WFOP™

The key process steps for J-Devices' WFOP™ are as follows (Fig. 9.2). First, they place the KGD face-up with adhesive on a metal panel carrier (320 mm × 320 mm). Then, coat a photosensitive resin (as the dielectric layer of the RDL) on top of the KGDs on the whole panel. It is followed by exposing and developing the opens of the KGD's window and direct current (DC) sputtering a seed layer for Cu plating. Apply (coat) a photoresist and then pattern the redistributed interconnections by photolithography techniques. Then, Cu plating, photoresist stripping, and seed layer etching are done. It is followed by solder mask coating, contact pad patterning, surface finishing, and solder ball mounting. Then, the panel and resin (dielectric) layers are diced into individual units (packages). A metal panel carrier with 320 mm square is shown in Fig. 9.3, where a WFOP™ package with 20 μm line width and spacing RDL is also shown.

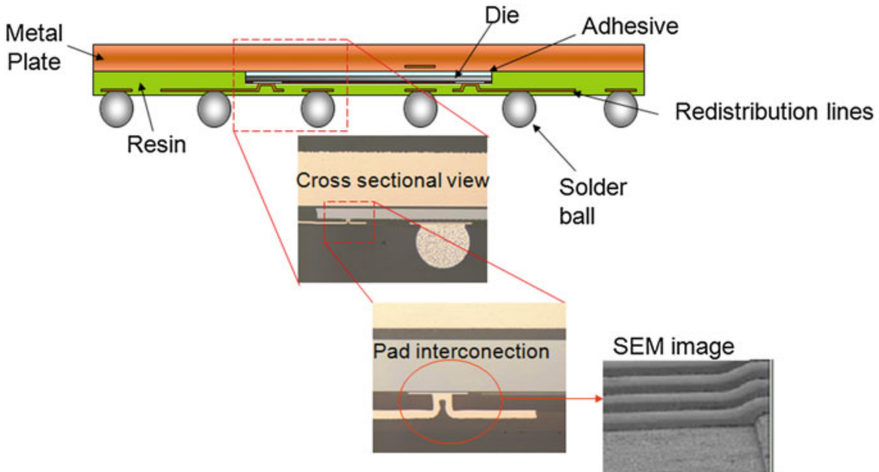


Fig. 9.1 J-Devices' WFOP™

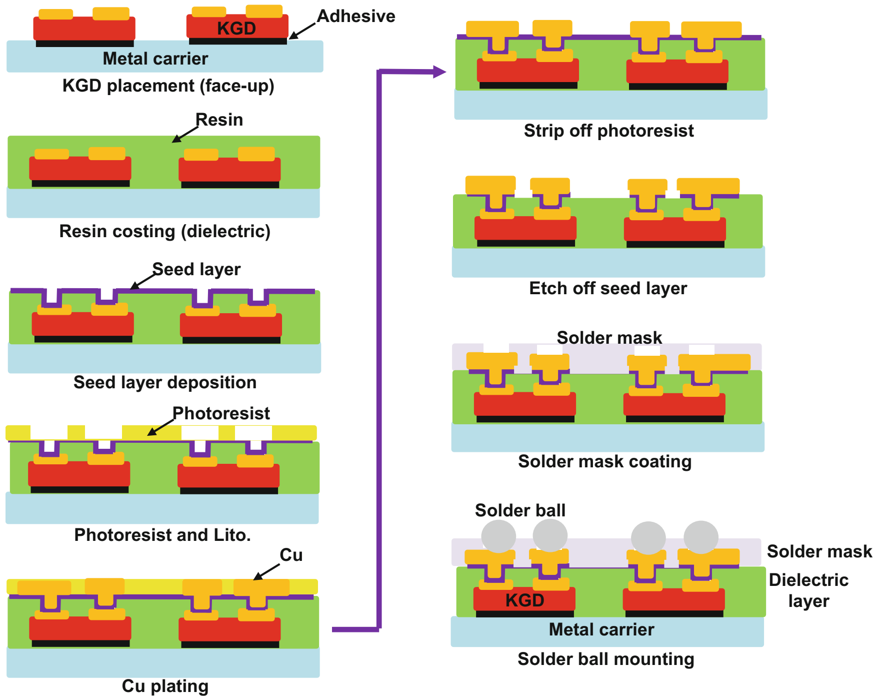


Fig. 9.2 Key process steps of J-Devices' WFOP™

9.3 Fraunhofer's FOPLP

Fraunhofer IZM summarized its 3-year development on fan-out panel-level packaging (FOPLP) in [4–6]. They showed that with surface mount technology (SMT) equipment for picking and placing the dies and passive devices and PCB technology + LDI (laser direct imaging) for making the RDLs, they are able to fabricate FOPLP at a very low cost (with a large panel instead of a wafer) for low end, low pin count, small chip sizes, and high-volume applications. Their test vehicle is a standard PCB size (610 mm × 457 mm) rectangular panel which is 3.8 times (in area) of the 300 mm wafer, as shown in Fig. 9.4.

9.3.1 Fraunhofer's FOPLP Integration Line

A complete Fraunhofer FOPLP integration line is shown in Fig. 9.5. It can be seen that there is not any semiconductor foundry equipment. They use the ASM SiPlace CA3 for pick and place the chips, Towa for compression molding the EMC, Lauffer/Burkle for lamination, Siemens Microbeam/Schmoll Picodrill for laser

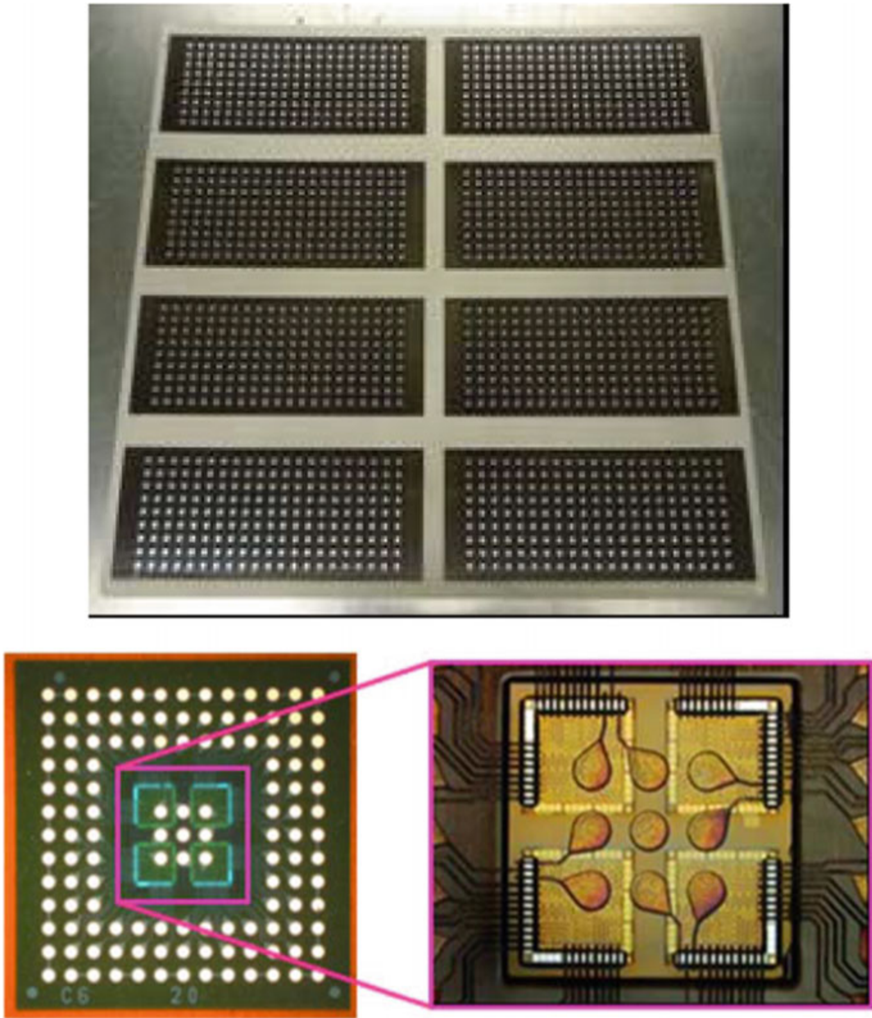


Fig. 9.3 J-Devices' panel and individual package

drilling, Schmoll for mechanical drilling, Ramgraber for Cu plating, Octotech for LDI, and Schmid for etching.

9.3.2 Fraunhofer's RDLs Key Process Steps

Fraunhofer's FOPLP key process steps are shown in Fig. 9.6, which are very similar to those shown in Chap. 5. Their RDLs key process steps are shown in

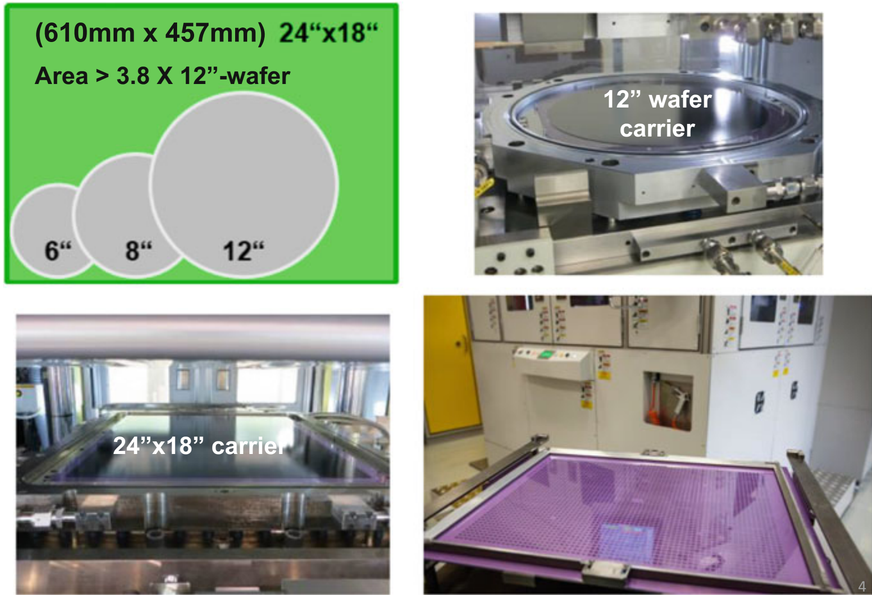


Fig. 9.4 Fraunhofer's FOPLP

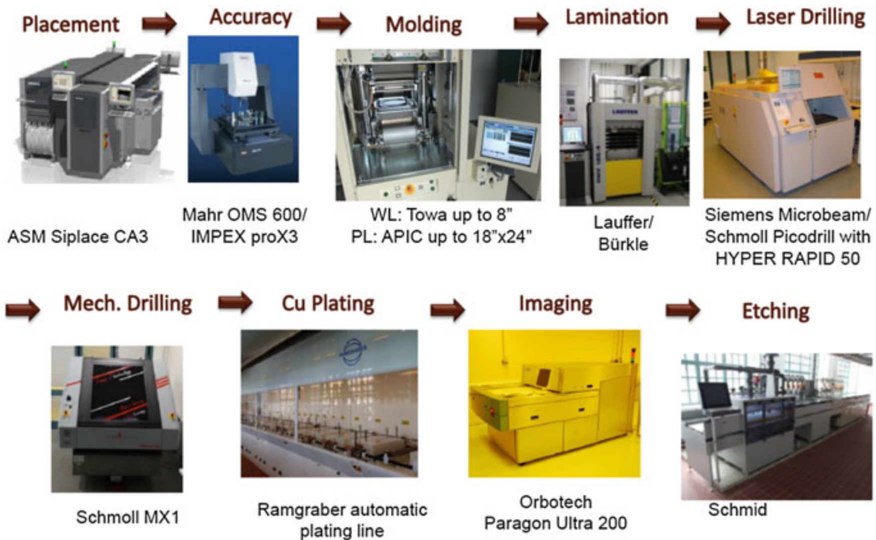


Fig. 9.5 Fraunhofer's FOPLP integration line

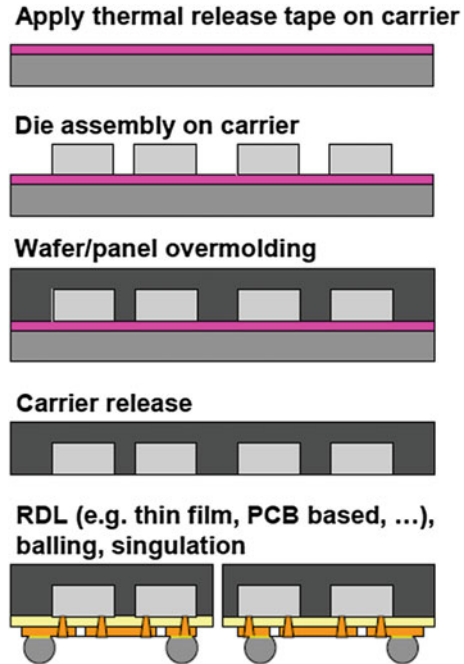


Fig. 9.6 Key process steps of Fraunhofer's FOPLP

Fig. 9.7. First, laminate a resin-coated copper (RCC) on the reconstituted panel. Then, use a mechanical or laser drill to make holes into the RCC. It is followed by PCB Cu plating to fill the holes and connect to the Al or Cu pads. Laminate a dry film photoresist and use an LDI to remove the resist. Perform the Cu etching and strip off the resist. We then have the first RDL1 and can repeat all the processes to get the other RDLs. The final RDL can be used as a contact pad. Next, we laminate, photolithograph, and cure the solder mask (in either a solder mask defined or a non-solder mask defined formats) before mounting the solder balls. For this process, no material and equipment are needed from the semiconductor arena except a PCB shop. Figure 9.8a shows the 610 mm × 457 mm panel and Fig. 9.8b shows the X-ray image of the 8 mm × 8 mm package which is housing two chips with dimensions of 2 mm × 3 mm.

9.4 SPIL's P-FO

Based on a PCB technology, thin-film transistor liquid-crystal display (TFT-LCD) 2.5G (generation) technology (panel dimensions = 370 mm × 470 mm), and backend technology, SPIL developed their P-FO technology [7, 8].

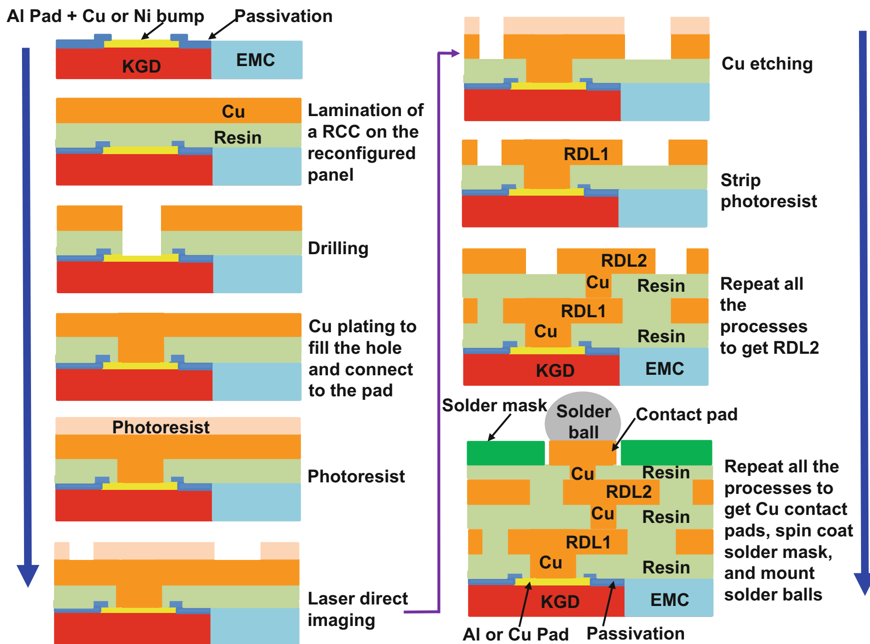


Fig. 9.7 Key process steps in making the RDLs of Fraunhofer's FOPLP

9.4.1 Structure of SPIL's P-FO

The structure of SPIL's P-FO is shown in Fig. 9.9a. It can be seen that the chip is embedded in a dry film and it is not in an EMC. Currently, there is only one layer of RDL.

9.4.2 Key Process Steps of SPIL's P-FO

The key process steps in making the SPIL's P-FO package are as follows. First, apply an adhesive on top of a glass panel (370 mm × 470 mm) carrier 1 as shown in Figs. 9.9b and 9.10a. Then, pick and place the KGDs face-down on the glass carrier 1, Fig. 9.10b, by using a PCB technology to laminate a dry film on top of the whole panel as shown Fig. 9.10c. It is followed by debonding the glass carrier 1 and attaching another carrier 2 on the other side of the reconstituted panel. Then, use the TFT-LCD 2.5G processing technology to fabricate the RDL on top of the Al or Cu contact pads and dry film as shown in Fig. 9.10e. It is followed by solder ball mounting as shown in Fig. 9.10f and dicing of the reconstituted panel as shown in Fig. 9.10g. A test package (9 mm × 9 mm) embedded a chip (6 mm × 6 mm) has been demonstrated and is shown in Fig. 9.9a.

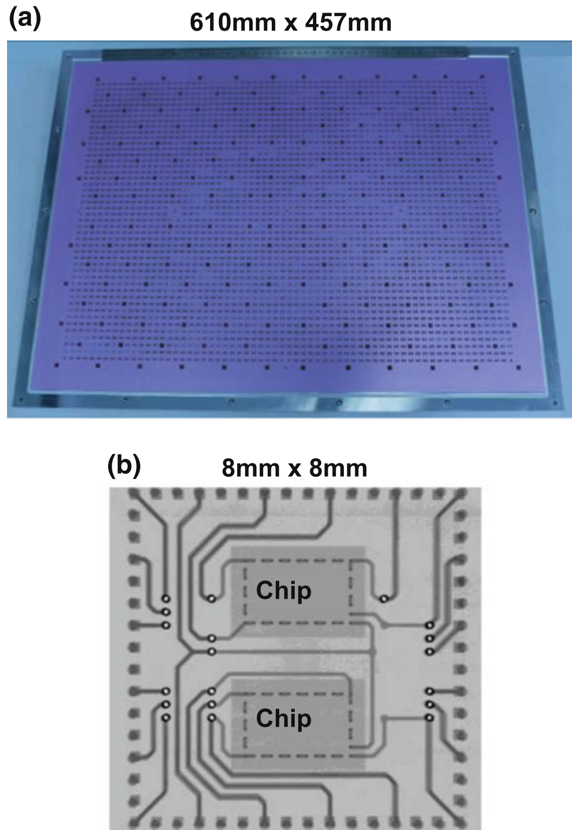


Fig. 9.8 Fraunhofer's FOPLP panel and individual package

9.5 Panel Versus Wafer

Simple mathematic shows that, compared to FOWLP, FOPLP will increase throughput and potentially lower the cost. However, there are many issues of FOPLP and they should be noted and resolved.

9.5.1 Issues of FOPLP

Some of the typical issues of FOPLP are shown as follows.

- Most OSATs and Foundries already have the necessary equipment for FOWLP. For FOPLP, new capital will have to be expended on newly developed equipment.
- Inspection of wafers is a well-known process. FOPLP inspection must be developed.

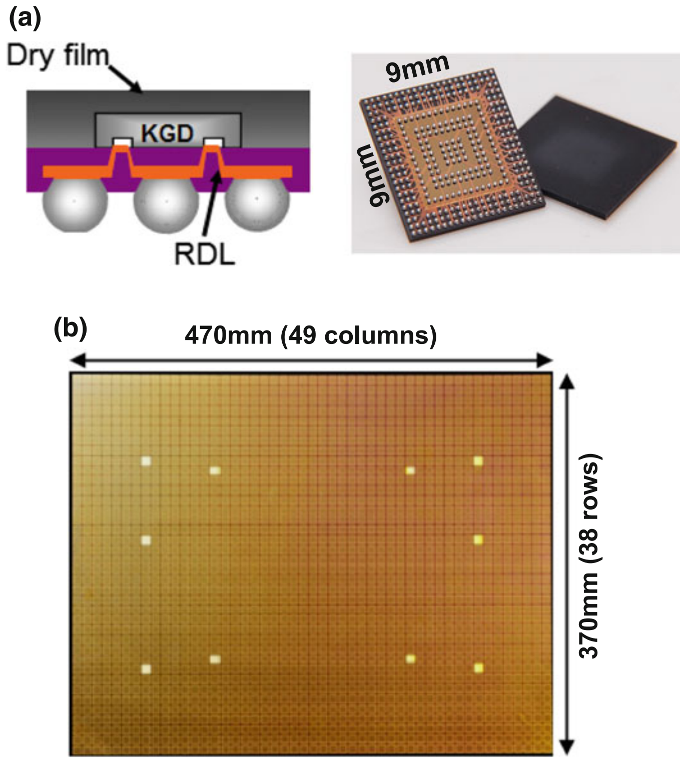


Fig. 9.9 SPIL's P-FO panel and individual package

- The yield of FOWLP is higher than that of FOPLP. (Assuming the size of panel is larger than that of wafer.)
- The cost advantages of panel over wafer need to be carefully determined. (Yes, the throughput is higher, but the pick-and-place time is longer, the EMC dispensing time is longer, and the yield is lower.)
- A fully loaded high-yield wafer line might be cheaper than a partially loaded low-yield panel line.
- The panel equipment takes longer to clean than wafer equipment.
- Unlike FOWLP, the FOPLP is for small to medium chip size and line width and spacing RDLs.
- There are only a few companies in the world capable of doing panel. You must have a materials background, equipment automation support, and IP. You also need to manage the dimensional stability and yield of the panel in a large format.
- Lack of panel standard for FOPLP, thus the equipment suppliers cannot make the equipment.
- If, indeed, the panel processing is developed and is high yield for fine line width and spacing, there is a chance to produce a major oversupply of capacity.

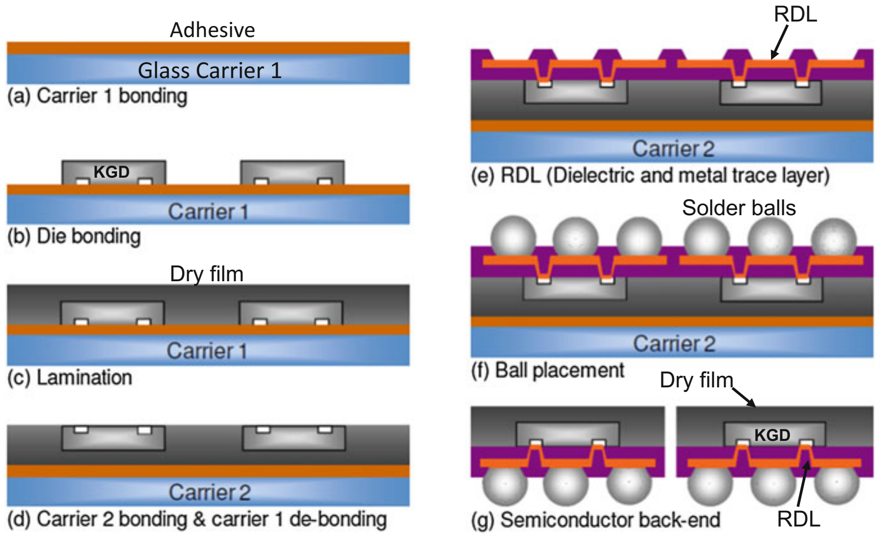
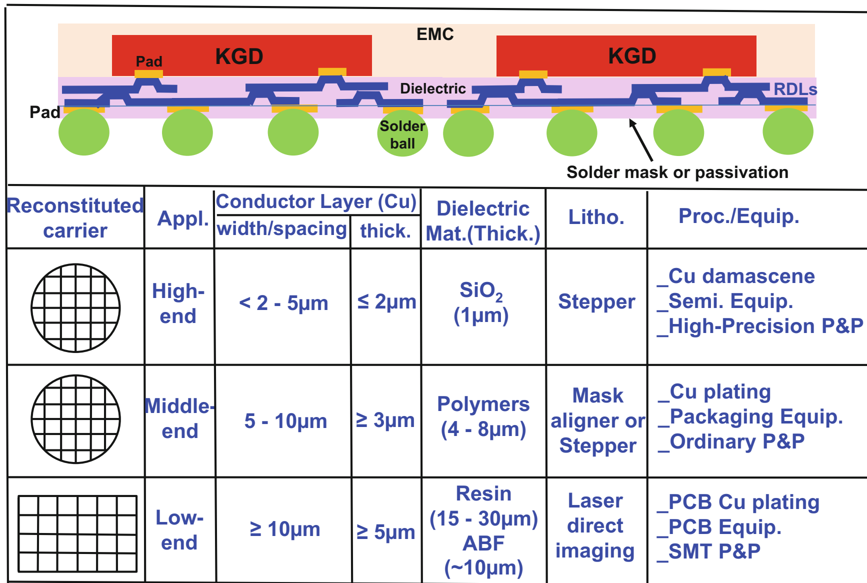


Fig. 9.10 Key process steps in making SPIL's P-FO

The choice between panel and wafer will depend on applications. Figure 9.11 shows the applications, geometry, material, process, and equipment for fan-out wafer/panel WLP.



Reconstituted carrier	Appl.	Conductor Layer (Cu) width/spacing	Conductor Layer (Cu) thick.	Dielectric Mat.(Thick.)	Litho.	Proc./Equip.
	High-end	< 2 - 5µm	≤ 2µm	SiO_2 (1µm)	Stepper	_Cu damascene _Semi. Equip. _High-Precision P&P
	Middle-end	5 - 10µm	≥ 3µm	Polymers (4 - 8µm)	Mask aligner or Stepper	_Cu plating _Packaging Equip. _Ordinary P&P
	Low-end	≥ 10µm	≥ 5µm	Resin (15 - 30µm) ABF (~10µm)	Laser direct imaging	_PCB Cu plating _PCB Equip. _SMT P&P

Fig. 9.11 Wafer versus panel (line width and spacing of RDLs)

9.5.2 Reconstituted Wafers for High-End Applications

The RDL line width/spacing and thickness are, respectively, ≤ 5 and 2 μm right now. But very soon they are going down to ≤ 2 and 1 μm, and the lithography process is accomplished using a stepper. The Cu conductor lines of the RDLs are fabricated by the Cu damascene + CMP (chemical mechanical polishing) method. The dielectric layer (SiO_2 or SiN) is 1 μm thick and fabricated by the plasma-enhanced chemical vapor deposition (PECVD) method. A high-precision pick-and-place (P&P) bonder is needed for die placement.

9.5.3 Reconstituted Wafers for Middle-End Applications

The RDL line width/spacing and thickness are, respectively, 5–10 and 3 μm, and the lithography is accomplished using a mask aligner or stepper to increase the yield. The conductor lines of the RDLs are fabricated by the electrochemical deposition Cu + etching method. The dielectric layer comprises polymers such as the PI (polyimide), BCB (benzocyclobutene), or PBO (polybenzobisoxazole), and is 4–8 μm thick. An ordinary pick-and-place bonder should be able to perform the die placement.

9.5.4 Reconstituted Panels for Low-End Applications

The RDL line width/spacing and thickness are, respectively, 10–20 and ≥ 5 μm. They are fabricated using PCB technology. First of all, the Al pad is coated with a Cu or Ni bump. A RCC sheet is laminated on the reconstituted panel. Microvias are drilled through the RCC layer to the die pads and electrically connected by Cu plating. RDL formation is done by LDI (laser direct imaging) in combination with a dry film resist and copper etching. The dielectric layer (resin) ranges from 15 to 30 μm. An SMT pick and place is adequate for die placement.

There is a small overlapping area between the high end and middle end, and the middle end and low end.

9.6 Summary and Recommendations

Fan-out panel-level packaging has been briefly presented and discussed in this chapter. Some important results and recommendations are summarized as follows.

- J-Devices' WFOP™ does not use an EMC and the package is supported by a metal plate. The RDLs are fabricated by a PCB technology called SAP. The line width and spacing of the RDL are 20 μm. The panel dimensions are 320 mm × 320 mm.

- Fraunhofer's FOPLP is very similar to the eWLB (Chap. 5), except they use SMT to perform the pick and place of the chips and PCB + LDI to make the RDLs. Their panel dimensions are 610 mm × 457 mm.
- SPIL's P-FO does not use an EMC. Instead, they laminate a dry film on top of the whole panel by PCB technology. The RDL on top of the Al or Cu contact pads and dry film is fabricated by the TFT-LCD 2.5G processing technology. The panel dimensions are 370 mm × 470 mm.
- The dielectric and conductor layers of the RDLs fabricated by the Fraunhofer's ECC method are too thick. Another method [9] which can reduce their thickness is shown in Fig. 9.12. It can be seen that instead of the ECC, laminate an ABF (Ajinomoto build-up film) on the panel. It is followed by laser drilling through the ABF and electroless Cu deposition of the seed layer. Then, laminate a dry film photoresist and use the LDI to pattern (dry film development) the interconnect traces. It is followed by PCB Cu plating. Then, strip off the photoresist and etch off the seed layer and get RDL1. Repeat all the processes to get the other RDLs. The final RDL can be used as a contact pad. Next, we laminate, photolithograph, and cure the solder mask (in either a solder mask defined or a non-solder mask defined formats) before mounting the solder balls. In this case, the dielectric layer thickness can be as little as 10 μm and the conductor layer thickness can be as little as 5 μm. Figure 9.13 shows the panel (340 mm × 340 mm) and the packages with 4 chips, and the cross section of the PCB assembly of a package made by the presented method, where RDL1 and RDL2 are shown.

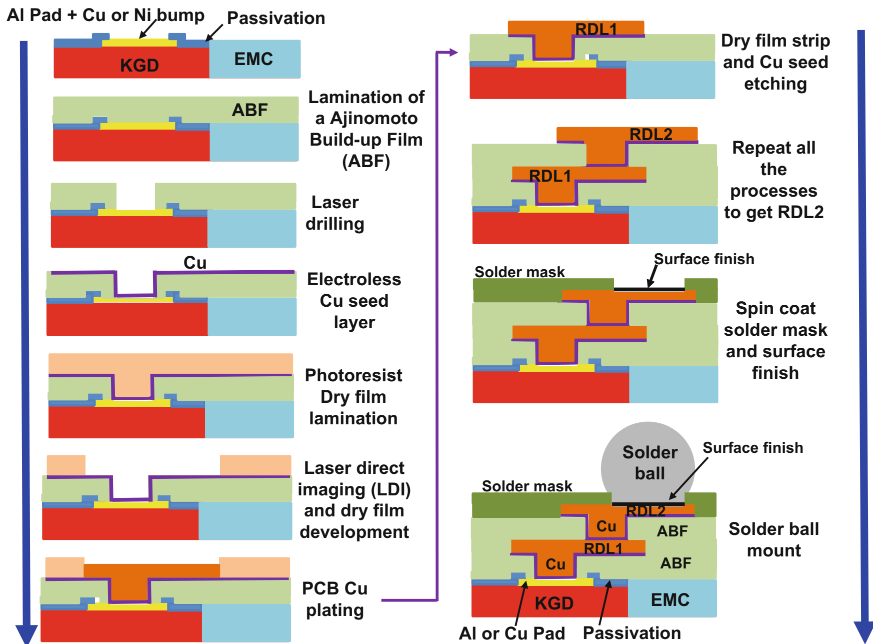


Fig. 9.12 A new method in making RDLs with PCB technology

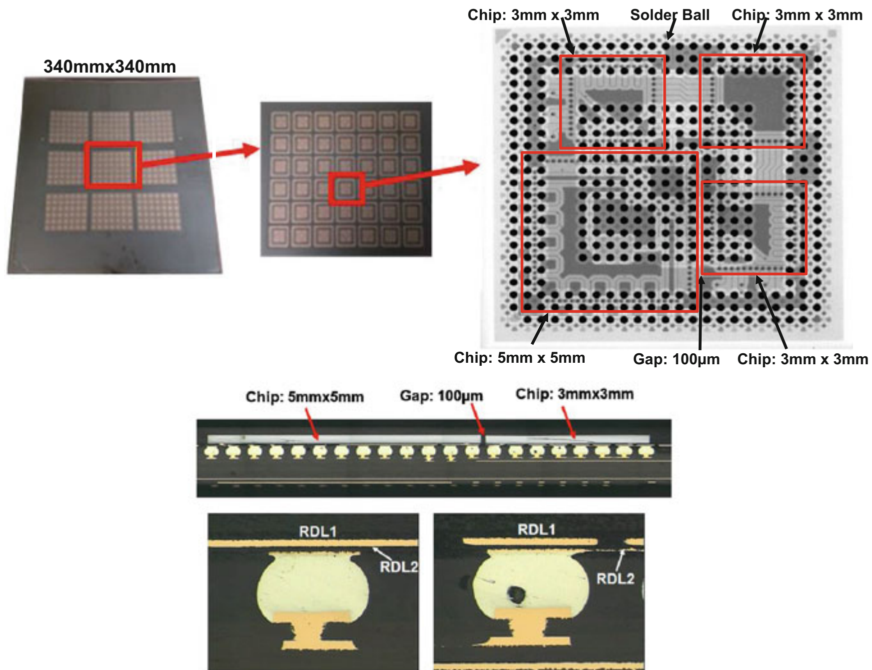


Fig. 9.13 Cross section of the PCB assembly of the test package with RDL1 and RDL2

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Chapter 10
3D Integration

10.1 Introduction

The Electronics Industry has been the largest industry since 1996 and may well reach 2 trillion dollars by the end of 2018 [1–3]. The most important invention of the Electronics Industry is arguably the transistor (1947), which earned John Bardeen, Walter Brattain, and Shockley the 1956 Nobel Prize in Physics. The invention of the IC (integrated circuit) by Kilby in 1958 (which earned him the 2000 Nobel Prize in Physics), and 6 months later by Noyce (who did not share the Nobel Prize with Kilby because he passed away in 1990) excited the generations of IC integrations. The proposal of doubling the number of transistors on an IC chip (for minimum costs and innovations) every 24 months by Moore in 1965 (also called Moore's law) [4] has been the most powerful driver for the development of the microelectronics industry in the past 50+ years. This law emphasizes lithography scaling and integration (on a 2D surface) of all functions on a single chip, perhaps through system-on-chip (SoC). On the other hand, the integration of all these functions can be achieved through 3D integrations such as 3D IC packaging [1], 3D IC integration [1–3, 5–89] and 3D Si integration [1–3, 69–125] as shown in Fig. 10.1 [1–3]. They are different, and in general, the through-silicon via (TSV) separates the 3D IC packaging from 3D Si integration and 3D IC integration, because the latter two use TSVs (through-silicon vias), but 3D IC packaging does not.

TSV was invented almost 60 years ago [1, 126] by the 1956 Nobel Laureate in Physics, Shockley. (Yes, the same Shockley who coinvented the transistor, which is generally considered the greatest invention in Semiconductor industry.) He filed the patent "Semiconductive wafer and method of making the same" on October 23, 1958, and was granted the U.S. Patent (3,044,909) on July 17, 1962. One of the key claims is shown in Fig. 10.2, which gets the semiconductor world so excited today. Basically, the "deep pits" (which are called TSVs today) on the wafer allow the signals from its top side to its bottom side and vice versa.

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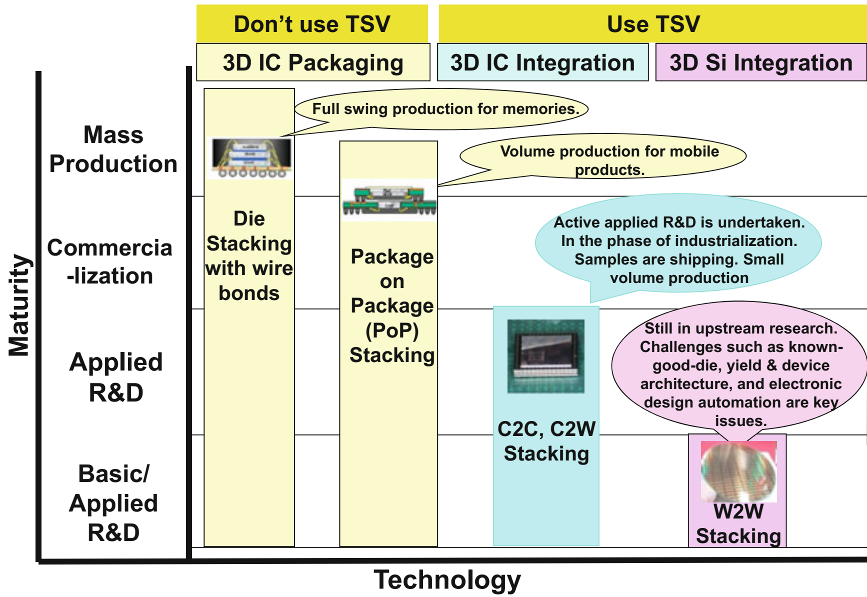


Fig. 10.1 3D integration technologies versus maturity

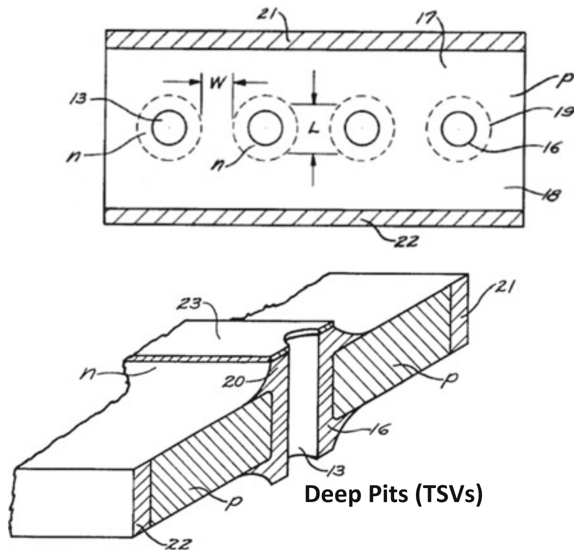


Fig. 10.2 TSV invented by Shockley (US Patent #3,044,909)

TSV is the heart of 3D Si integration and 3D IC Integration [1, 127]. It provides the opportunity for the shortest chip-to-chip interconnects and the smallest pad size and pitch of interconnects. Compared with other interconnection technologies, such

as wire bonding, the advantages of TSV include: (a) better electrical performance, (b) lower power consumption, (c) wider data width and thus bandwidth, (d) higher density, (e) smaller form factor, and (f) lighter weight, [1–3, 5–125].

TSV is a disruptive technology. As with all disruptive technologies, the questions to ask are: "What is it displacing?" and "What is the cost?" Unfortunately, TSV is trying to replace the wire bonding technology, which is a most mature, high-yield, and low-cost technology [128]. However, just like solder-bumped flip chip technology [129, 130], because of their unique advantages, TSVs will be here to stay and for a very long time for wide bandwidth, high-performance and high-density applications.

TSV has been in volume production for microelectromechanical systems [131, 132] and complementary metal-oxide semiconductor (CMOS) image sensor [133, 134]. However, they are out of the scope of this study, which is focused on memory, logic, processor, and SoC. 3D (IC and Si) integration is a very old idea [69, 70] which consists of two or more layers of active electronic components that are integrated vertically through TSV (it used to be called vertical interconnection) into a single circuit. It was triggered by the advance of the silicon-on-insulator (SOI) technology first reported by Gat and his colleagues more than 35 years ago [135], when semiconductor people thought Moore's law could be hitting the wall by the 1990s. Of course, the fact showed otherwise.

3D IC integration is to stack up the thin chips with TSVs and microbumps. While 3D Si integration is to stack up the thin wafers/chips with TSVs alone, i.e., bumpless. The advantages of 3D Si integration over 3D IC integration are: (1) better electrical performance, (2) less power consumption, (3) lower profile, (4) less weight, and (5) higher throughput.

The most powerful proponent on 3D IC/Si integration is the 1965 Nobel Physics laureate, Richard Feynman. More than 30 years ago, during his lecture, Computing Machines in the Future in 1985, he said "Another direction of improvement (of computing power) is to make physical machines three dimensional instead of all on a surface of a chip. That can be done in stages instead of all at once—you can have several layers and then add many more layers as time goes on." In this chapter, the overview, challenge, and outlook of 3D IC integration, and 3D Si integration will be presented and discussed [64]. 3D IC packaging will be briefly mentioned first.

10.2 Overview and Outlooks of 3D IC Packaging

Figure 10.1 shows that chip stacking by wire bonding and package-on-package (PoP) are now mature for high-volume manufacturing (HVM). Chip-to-chip interconnects and 3D embedded fan-out wafer-level packaging are getting tractions.

10.2.1 Chip Stacking by Wire Bonding

The first paper on stacking of memory chips in 3D by die-attach material and Au wire bonding was published by nCHIP [136] more than 20 years ago. Since then, memory chip (especially the NAND Flash) stacking by Au wire bonding has been in high volume production for, e.g., the smartphones, tablets, and solid state drives as shown in Figs. 10.3 and 10.4. Because of the surge in Au prices and research and development progress in Cu wire bonding technology, many companies have been looking for low-cost solutions, and the shift from Au to Cu wire bonding as shown in Fig. 10.5 is genuinely picking up. In 2017, the world uses of Cu wires excess the Au wires.

10.2.2 PoP

PoP comes from many different forms. Figure 10.6 shows a wire bond package on top of a flip chip package. It can be seen that the top package consists of two chips cross stacked and wire bonded on a package substrate and then over molded. The bottom package consists of a solder-bumped flip chip on another package substrate with underfill. All these package substrates are with solder balls. Again, PoP is in high-volume production for, e.g., the smartphones and tablets [6].

Figure 10.7 shows the cross-section scanning electron microscope (SEM) images of a 3D fan-out embedded wafer-level package [137] developed by STATS ChipPAC. It consists of a bottom package which is an embedded fan-out

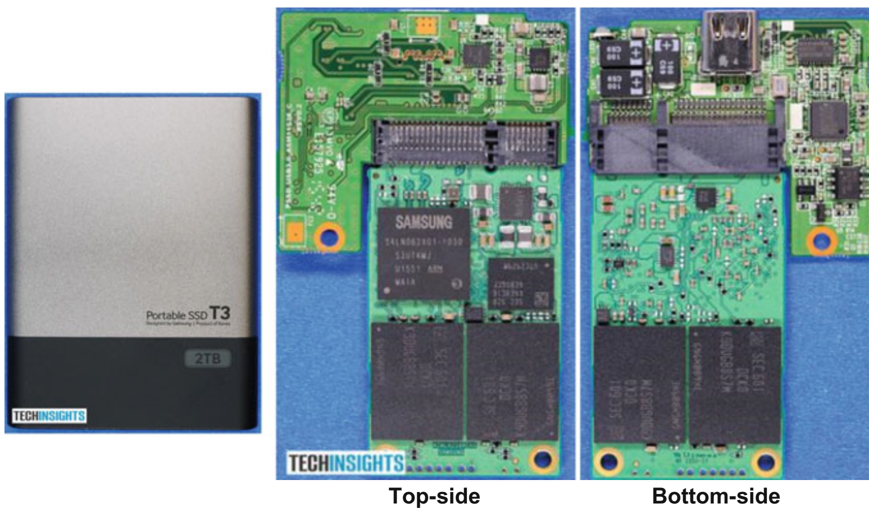


Fig. 10.3 Samsung's 48-layer V-NAND 3D flash memory in a solid state drives (SSD)

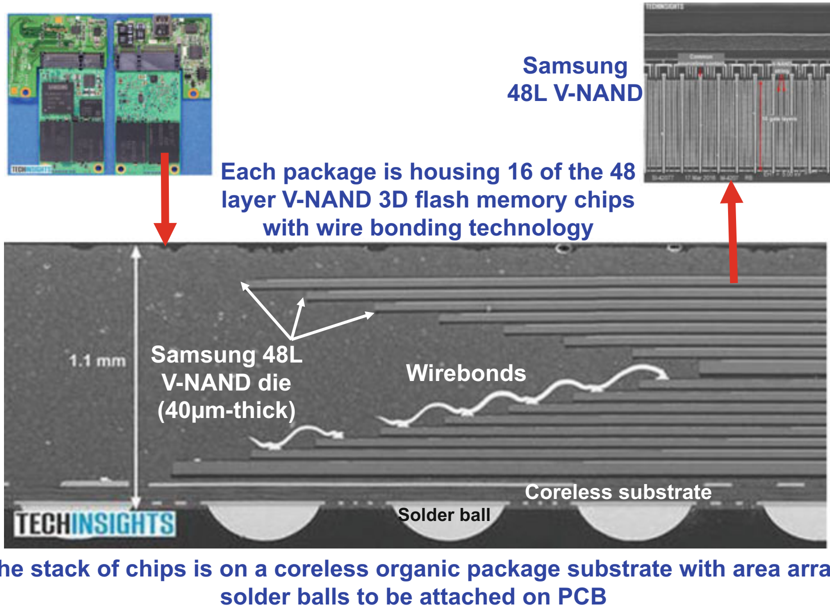


Fig. 10.4 16 stacked Samsung 48L V-NAND dies

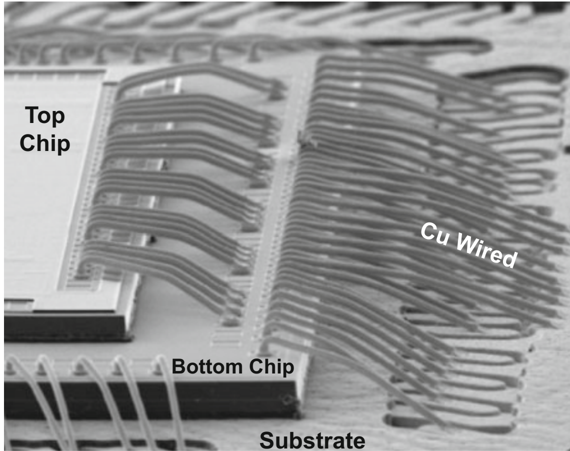
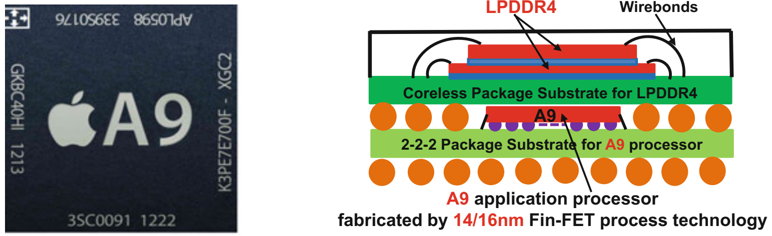


Fig. 10.5 3D stacked of chips with Cu wire bonding

wafer-level ball grid array package (eWLB) and a top package which is a memory package. It can be seen that: (a) the eWLP contains the logic, baseband, or application processor, (b) the eWLB is only 450 µm thick, (c) the top package is 520 µm thick and is housing the memory chips with wire bonding, and (d) the interconnection is from the PCB, solder balls, redistribution layers (RDLs), to processor, and solder balls, RDL, to the memory chips. This package is a potential candidate



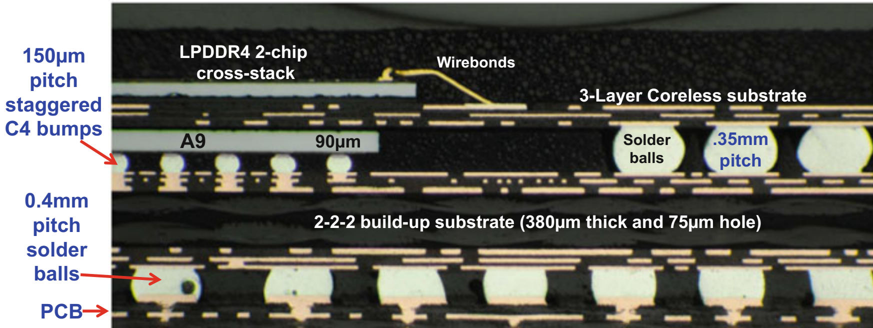


Fig. 10.6 Apple's A9 is solder-bumped flip chip packaged in a PoP

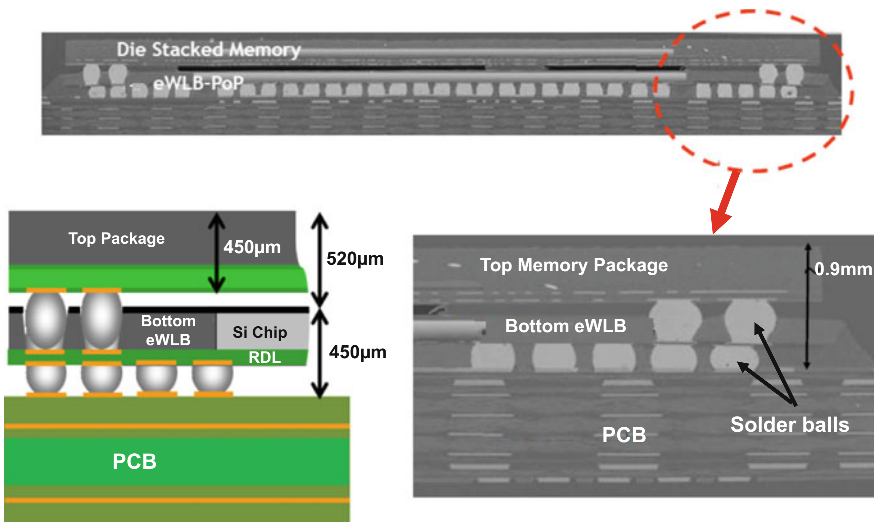


Fig. 10.7 3D IC packaging (STATSChipPAC's package-on-package.) Memory package on top and eWLB package for the application processor at the bottom

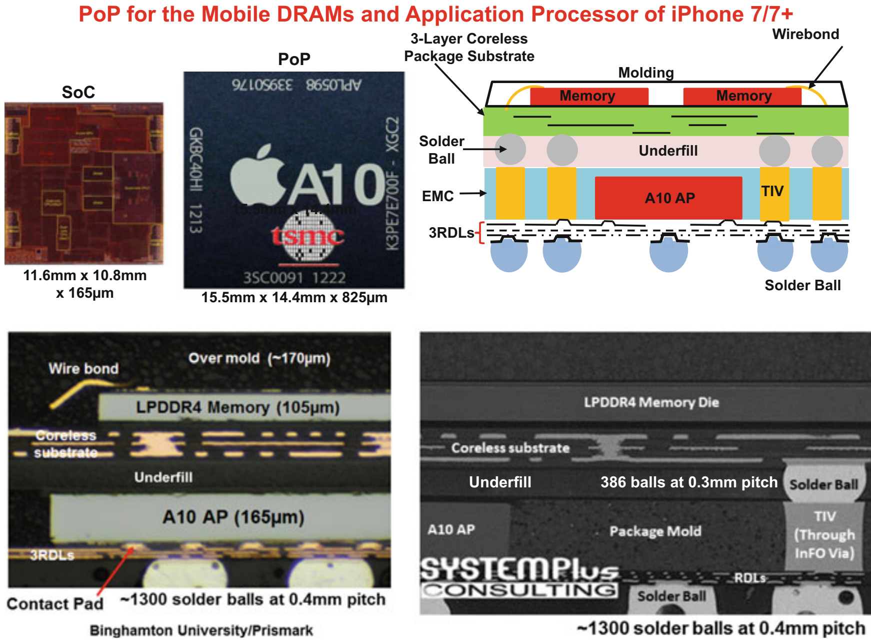


Fig. 10.8 Cross section images of iPhone 7/7+ A10-chipset packaging

for mobile and wearable products. On September 15, 2016, TSMC used their InFO (integrated fan-out) wafer-level packaging to package the application processor (A10) for the iPhone 7 and iPhone 7+ as shown in Fig. 10.8.

10.2.3 Chip-to-Chip Interconnects

Figure 10.9 shows the schematic of a 3D chip-to-chip interconnect [138] developed by IME. It consists of the mother chip which is face-to-face connected to a daughter chip. The backside of the mother chip can be attached to a heat spreader (and a heat sink if necessary). The whole module is attached (through the flip chip mother die) to a rigid or flexible substrate. It is a very cost-effective 3D IC package without using the TSVs. In 2012, SONY's PlayStation (CXD53135GG) attached Samsung's 1 GB wide input/output (I/O) synchronous dynamic random access memory face-to-face to the processor and then wire bonded to the next level interconnects. The packages shown in Fig. 10.9 are not in manufacturing yet; however, they are the potential candidates for medium-range performance applications.

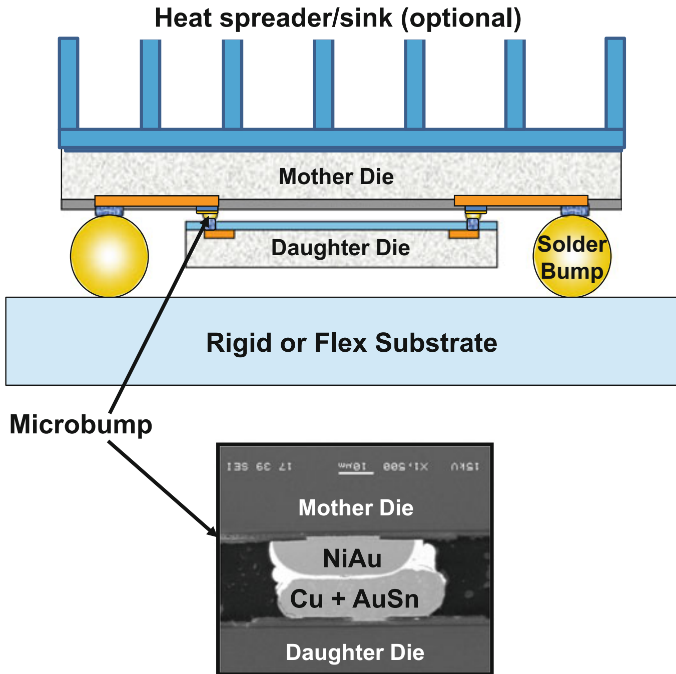


Fig. 10.9 Chip-to-chip (Face-to-face) 3D IC packaging

10.2.4 Outlook of 3D IC Packaging

The outlook of 3D IC packaging is great! Stacked dies with wire bonding and PoP are in HVM for commercial products such as wearables, smartphones, and tablets. Chip-to-chip interconnects are getting tractions and into manufacturing soon. 3D fan-out embedded wafer-level package is already in production. All these 3D IC packaging technologies have been keeping 3D IC/Si integration technologies away from HVM.

10.3 Overview, Challenges, and Outlook of 3D Si Integration

10.3.1 Issues of 3D Si Integration

Basically, wafer to wafer (W2W) is the only way to perform the bonding operation for 3D Si integration and yield is a critical issue (e.g., some bad chips are forced to bond on the good chips). In addition, the absence of (or an infinitesimal) gap

between wafers and thermal management could be a big problem. Furthermore, the requirements of the bonding conditions, such as the surface cleanness, surface flatness, and the class of clean room for 3D Si integration are very high.

10.3.2 Cu-to-Cu Bonding and Oxide-to-Oxide Bonding

There are at least two different W2W bonding methods for 3D Si integration, namely, Cu-to-Cu bonding and oxide-to-oxide bonding, as shown in Figs. 10.10 and 10.11, respectively. In general, for Cu-to-Cu bonding, the TSVs have to be fabricated before bonding. On the other hand, for oxide-to-oxide bonding, the TSVs are fabricated after bonding.

Figure 10.10a shows a high-quality bonding interface by IBM and RPI [90–92]. Before bonding, the Cu interconnects (pads) are fabricated with the standard back-end-of-line (BEOL) damascene process, followed by the oxide chemical mechanical polishing (CMP) process (oxide touch-up) to recess the oxide level to 40 nm lower than the Cu surface. The bonding temperature is ramped up to 400 °C. Figure 10.10b shows a cross section of the interface between the bumpless Cu-to-Cu electrodes (pads) given by the NIMS/AIST/Toshiba/University of Tokyo [93–99].

Figure 10.11a shows a cross section of MIT's oxide-to-oxide bonding structure of three-layer 3D (ring oscillator) bonded at 275 °C [100–106]. It can be seen that: (1) the layers are bonded and interconnected with W-plugs, (2) the conventional inter-level connections are in the bottom two layers, and (3) the 3D vias are located in the isolation (field) region between transistors. Figure 10.11b shows

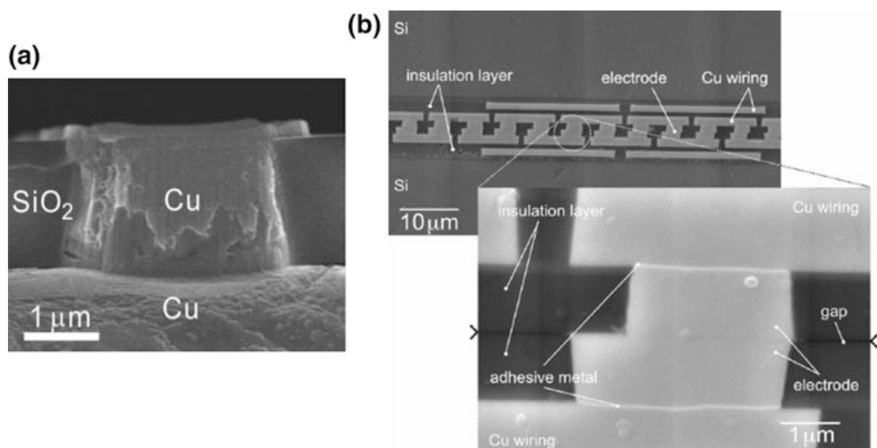


Fig. 10.10 3D Si integration: **a** IBM/RPI's Cu-to-Cu bonding. **b** NIMS/AIST/Toshiba/ University of Tokyo's Cu-to-Cu bonding

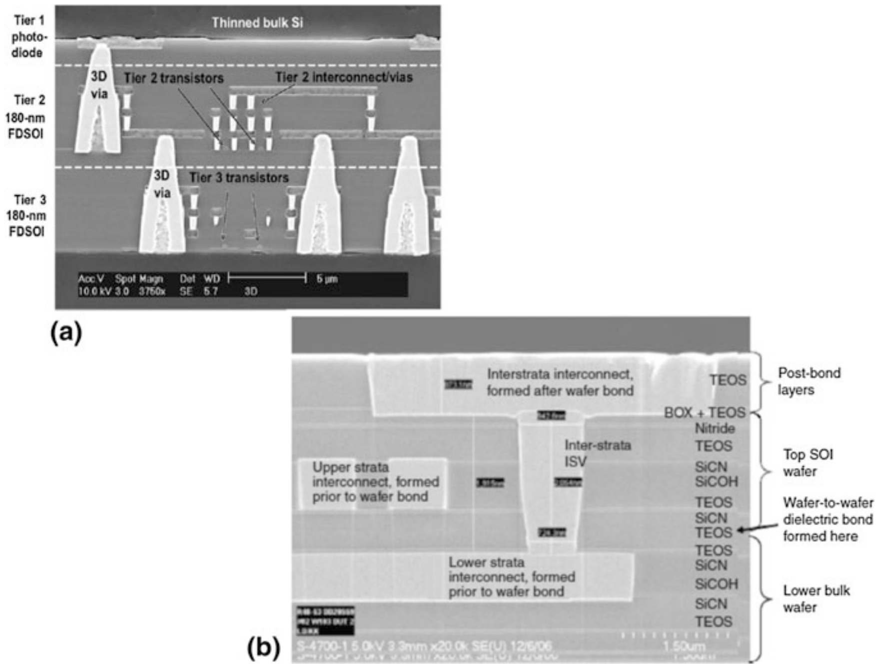


Fig. 10.11 3D Si integration: **a** MIT's oxide-to-oxide bonding. **b** Leti/Freescale/STMicroelectronics' oxide-to-oxide bonding

Leti/Freescale/STMicroelectronics' dielectric-to-dielectric bonding structure of two device layers bonded at 400 °C [107–109]. It can be seen that: (a) first, a metal level is formed on a 200 mm bulk wafer and SOI wafer; next, these wafers are bonded face-to-face, and then the bulk silicon of the SOI wafer is removed down to the buried oxide layer, (b) the 1.5 μm interstrata vias (ISVs) are formed, which make contact from upper strata to lower strata, (c) a metal layer is formed at the top of the back side of the SOI wafer, and (d) this ISV makes contact with both the top and bottom metal layers.

10.3.3 R&D in 3D Si Integration

In order to use the 3D Si integration technology to HVM products, many research and development efforts have to be performed. Besides thermal management, vias formation, thin-wafer handling, more research and development efforts should also be placed on areas such as: cost reduction, design and process parameter optimization, bonding environment, W2W bonding alignment, wafer distortion, wafer bow (warpage), inspection and testing, contact performance, contact integrity, contact reliability, and manufacturing yield issues. In addition, packaging the 3D Si

integration module systematically and reliably to the next level of interconnect pose another great challenge.

Besides technology issues just mentioned, the electronic design automation (EDA) which is the soul of 3D Si integration [127] is far from ready. Urgently, the industry needs to build standard and infrastructure and form an ecosystem for 3D Si integration. Then, the EDA can write the design, simulation, analysis and verification, manufacturing preparation, and test software with the following guidelines: (1) design automation from high-level description to layout generation/optimization, (2) verification of all dedicated and tuned to 3D integration, (3) addressing the third dimension not like a packaging bumping, (4) addressing the true third dimension, with partitioning, floor planning, automatic placing, and routing, (5) full extraction with the third dimension, full 3D design rule checks, 3D layout versus schematic with all tiers together in a same database, and (6) the 3D integrations have then to be seen as a whole system distributed in several tiers, and not just a stack of predefined chips.

10.3.4 Outlooks of 3D Si Integration

In the next 10 years, the industry will be hard-pressed for HVM with the 3D Si integration technology, except for very niche applications. However, it should be noted and emphasized that 3D Si integration is the right way to go and compete with Moore's law. The industry should strive to make this happen!

10.3.5 Hybrid Bonding

It is worthwhile to mention that there is another kind of W2W bonding, namely hybrid bonding which bonds the metal pads and dielectric layer on both sides of the wafers at the same time. SONY is the first to use Cu–Cu direct hybrid bonding in HVM [139]. SONY produced the IMX260 backside illuminated CMOS image sensor (BI-CIS) for the Samsung Galaxy S7, which shipped in 2016. Electrical test results showed that their robust Cu–Cu direct hybrid bonding achieved remarkable connectivity and reliability. The performance of the image sensor was also super. A cross section of the IMX260 BI-CIS is shown in Fig. 10.12. It can be seen that, unlike in [140] for SONY's ISX014 stacked camera sensor, the TSVs are eliminated and the interconnects between the BI-CIS chip and the processor chip are achieved by Cu–Cu direct bonding. The signals are coming from the package substrate with wire bonds to the edges of the processor chip.

The assembly process of Cu–Cu direct hybrid bonding starts off with surface cleaning, metal-oxide removal, and activation of SiO_2 or SiN (by wet cleaning and plasma activation) of wafers for the development of high bonding strength. Then, use optical alignment to place the wafers in contact at room temperature and in a

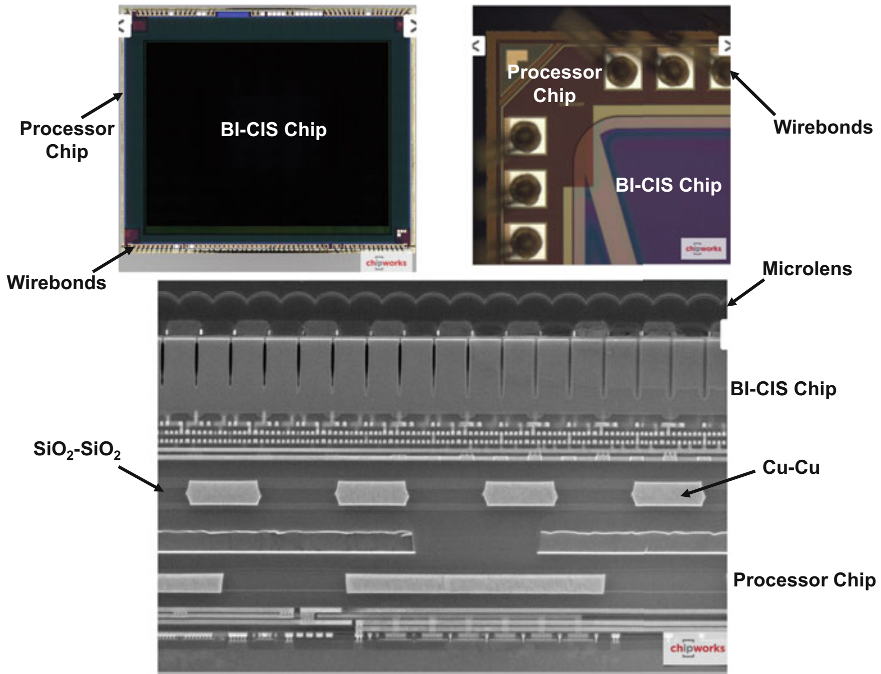


Fig. 10.12 Sony's Cu–Cu hybrid bonding

typical clean room atmosphere. The first thermal annealing (100–150 °C) is designed to strengthen the bond between the SiO_2 or SiN surfaces of the wafers while minimizing the stress in the interface due to the thermal expansion mismatch among the Si, Cu, and SiO_2 or SiN. Then, apply higher temperature and pressure (300 °C, 25 kN, 10-3 Torr, N2 atm) for 30 min to introduce the Cu diffusion at the interface and grain growth across the bond interface. The post-bond annealing is 300 °C under N2 atm for 60 min. This process leads to the seamless bonds (Fig. 10.12) formed for both Cu and SiO_2 or SiN at the same time.

10.4 Overview, Challenges, and Outlook of 3D IC Integration

Unlike 3D Si integration, 3D IC Integration stacks up thin IC chips in the third dimension with TSVs and microbumps (<25 μm) [1] to achieve performance, low power consumption, wide bandwidth, and small form factor. The ones which are in and going into low volume production are: memory stacking with TSVs, wide I/O DRAM, wide I/O DRAM 2, high-bandwidth memory (HBM), hybrid memory cube (HMC), and 2.5D IC integration (passive interposer).

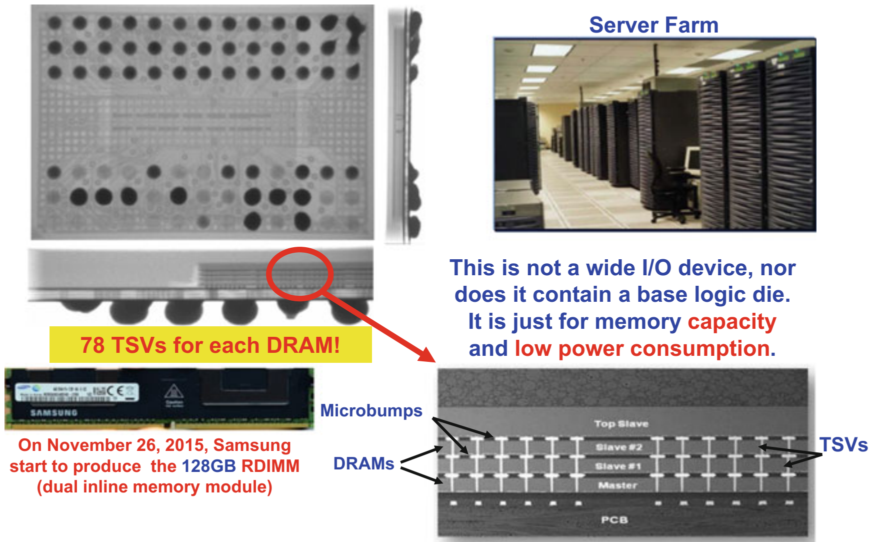


Fig. 10.13 Samsungs' DRAM stacking with TSVs

10.4.1 Memory Stacking with TSVs

Samsung mass-produced (August 2014) the industry's first TSV-based 64 GB double data rate type 4 (DDR4) DRAM stack module (Fig. 10.13). Each stack has 4 DRAMs, each DRAM die has 78 TSVs, and the 64 GB DDR4 DRAM stacks are on a printed circuit board (PCB). The module performs twice as fast as a module that uses wire bonding packaging technology, while consuming approximately half the power. The module is for environmentally friendly server applications. On November 26, 2015, Samsung started to produce the 128 GB registered dual inline memory module (RDIMM).

10.4.2 Wide I/O DRAM and Wide I/O 2

JEDEC standard (JESD229) [141], Wide I/O Single Data Rate (Wide I/O SDR), was published in Dec. 2011 and JEDEC standard (JESD229-2) [141], Wide I/O 2 (Wide I/O2), was published in August 2014. They are meant for a stack of DRAMs with TSVs on a logic controller with TSVs. The microbumps are divided into four quadrants with signal assignments mirrored both horizontally and vertically as shown in Fig. 10.14, where the bump pitch (40 μm) of the area array is also shown. The dimensions of each quadrant are 2880 μm × 200 μm. There will be a space between quadrants in the *x*-direction (1000 μm) and in the *y*-direction (120 μm) [141].

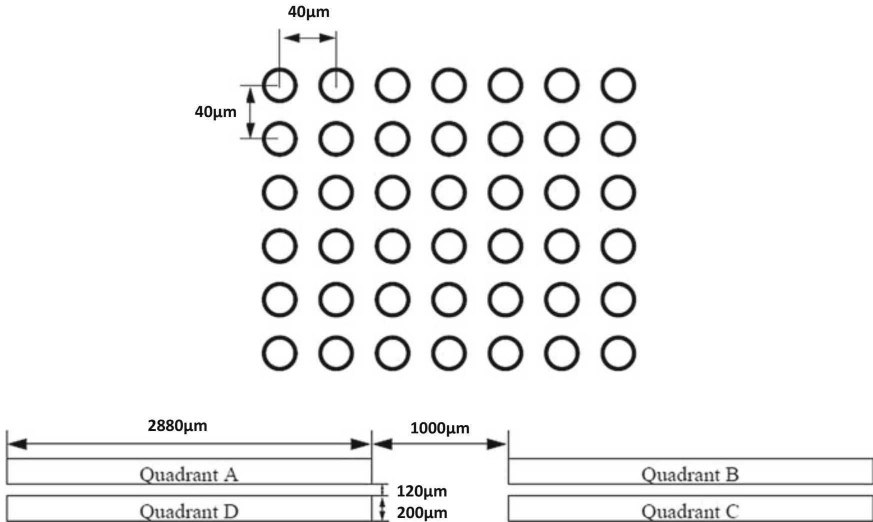
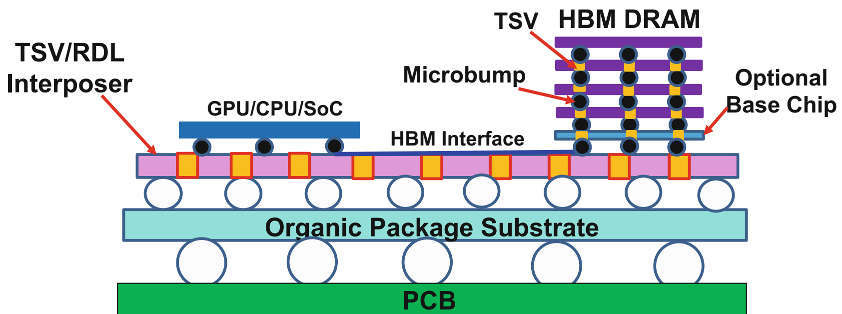


Fig. 10.14 Schematic of JEDEX's Wide I/O 2

10.4.3 High-Bandwidth Memory (HBM)

JEDEC standard (JESD235) [142], high-bandwidth memory (HBM) DRAM, was published in December 2013. It is meant for the graphics applications supporting bandwidth from 128 to 256 GB/s. A TSV/RDL interposer is used to support/connect mainly the lateral communication (HBM interface) between the HBM DRAM memory cube with TSVs and the SoC such as graphic processor unit or CPU without TSVs. The optional base chip is used for buffering and signal rerouting of the HBM DRAM cube (Fig. 10.15).



Underfill is needed between the interposer and the organic substrate. Also, underfill is needed between the interposer and the GPU/CPU and the HBM cube

Fig. 10.15 Schematic of JEDEX's High-Bandwidth Memory (HBM)

10.4.4 AMD's Graphic Processor Unit with HBM

Figure 10.16 shows AMD's Radeon R9 Fury X graphic processor unit (GPU) shipped in the second-half of 2015. The GPU is built on TSMC's 28 nm process technology and is supported by four high-bandwidth memory (HBM) cubes manufactured by Hynix. Each HBM consists of four DRAMs with C2 bumps and a logic base with TSVs straight through them. Each DRAM chip has >1000 TSVs. The GPU and HBM cubes are on top of a TSV interposer (28 mm × 35 mm), which is fabricated by UMC with a 64 nm process technology. The final assembly of the TSV interposer (with C4 bumps) on a 4-2-4 organic package substrate (fabricated by Ibiden) is by ASE.

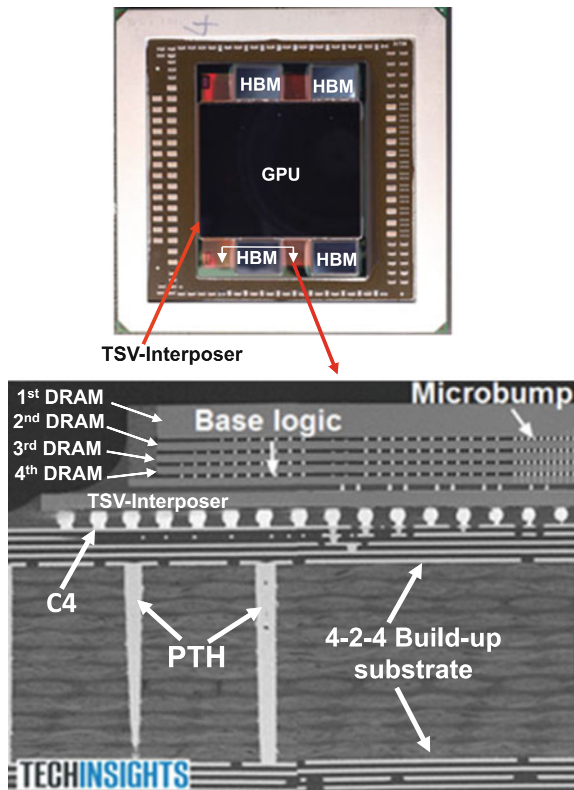


Fig. 10.16 AMD's GPU with Hynix's HBM and UMC's TSV interposer

10.4.5 Nvidia's Graphic Processor Unit with HBM2

Figure 10.17 shows Nvidia's Pascal 100 GPU, which shipped in the second-half of 2016. The GPU is built on TSMC's 16 nm process technology and is supported by four HBM2 (16 GB) fabricated by Samsung. Each HBM2 consists of four DRAMs with C2 bumps and a base logic die with TSVs straight through them. Each DRAM chip has >1000 TSVs. The GPU and HBM2s are on top of a TSV interposer (1200 mm^2), which is fabricated by TSMC with a 64 nm process technology. The TSV interposer is attached to a 5-2-5 organic package substrate with C4 bumps.

Both Samsung and Hynix use the high bonding force TCB of the C2 bumped DRAMs with NCF as shown in Fig. 2.16d to fabricate the 3D IC integration stack. This 3D memory cube is stacked one chip at a time and each chip takes $\sim$10 s for the underfill film to gel, the solder to melt and solidify, and the film to cure.

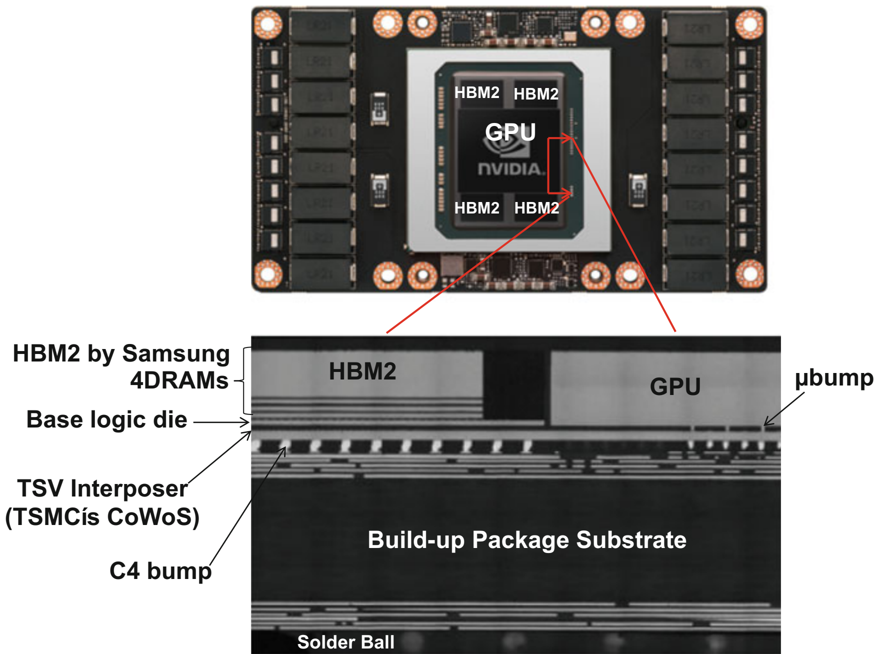


Fig. 10.17 Nvidia's GPU with Samsung's HBM2 and TSMC's TSV interposer

10.4.6 Intel's CPU with Micron's HMC

Figure 10.18 shows Intel's Knights Landing CPU with Micron's HMC (hybrid memory cube) [143], which have been shipping to Intel's favorite customers since the second-half of 2016. It can be seen that the 72-core processor is supported by 8 multichannel DRAMs (MCDRAM) based on Micron's HMC technology. Each HMC consists of 4 DRAMs and a logic controller (with TSVs), and each DRAM has >2000 TSVs with C2 bumps. The DRAM+ logic controller stack is attached to an organic package substrate. Micron reports that having such HMC in the CPU package is expected to deliver 5X the sustained memory bandwidth versus GDDR5 (graphics double data rate type 5) with one-third the energy per bit in half the footprint. Micron's current HMC assembly process is different from that of Samsung and Hynix. Instead of using high-force TCB-NCF (Fig. 2.16d), Micron uses low-force TCB with CUF (Fig. 2.16b). Again, just like Samsung and Hynix, Micron has to do it one DRAM at a time.

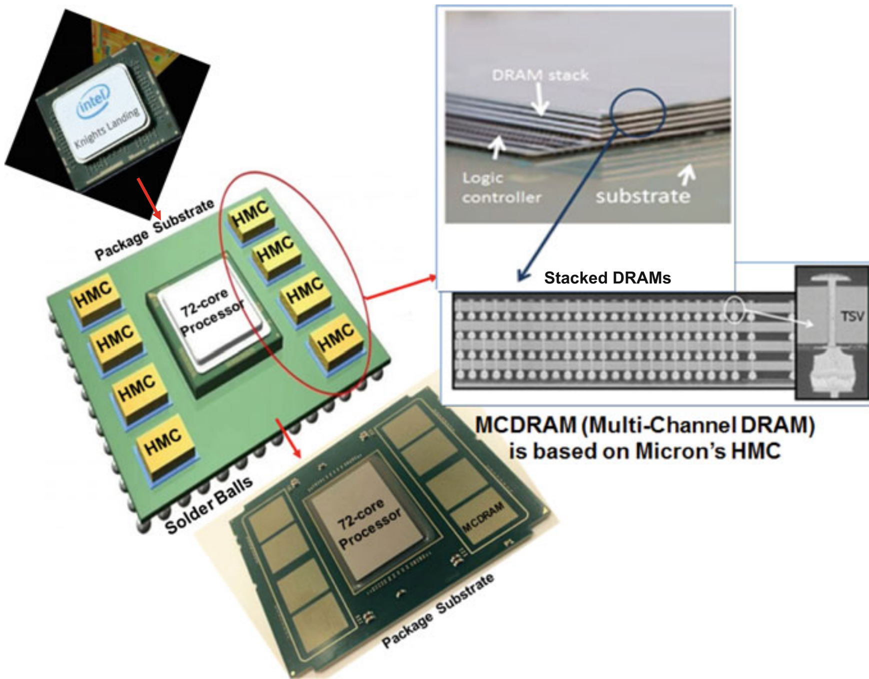


Fig. 10.18 Intel's knights landing processor unit with Micron's HMC

10.4.7 Passive Interposer (2.5D IC Integration)

A 2.5D IC integration is a TSV/RDL interposer system which consists of a piece of deviceless silicon with TSVs, RDLs, and IC chips without TSVs. This piece of deviceless TSV silicon (also called a passive TSV interposer) is used to support the high-performance, high-density, fine-pitch chips and has RDLs (mainly) for lateral communication between the chips as shown schematically in Fig. 10.19. Figure 10.20 shows a sample designed and fabricated by Altera/TSMC [41, 42]. It can be seen that even with more than 12 buildup layers (6-2-6) on the package substrate, it is still not enough to support the four-sliced 28 nm FPGA (field-programmable gate array) chips. In addition, a passive TSV interposer with 200,000 + microbumps on 45 μm pitch and four RDLs (three Cu damascene layers and one aluminum layer) at a minimum of 0.4 μm pitch is needed. This type of structure (Figs. 10.19 and 10.20) is called by TSMC as chip on (interposer) wafer on (package) substrate (CoWoS) and has been in small production for Xilinx since the early of 2013.

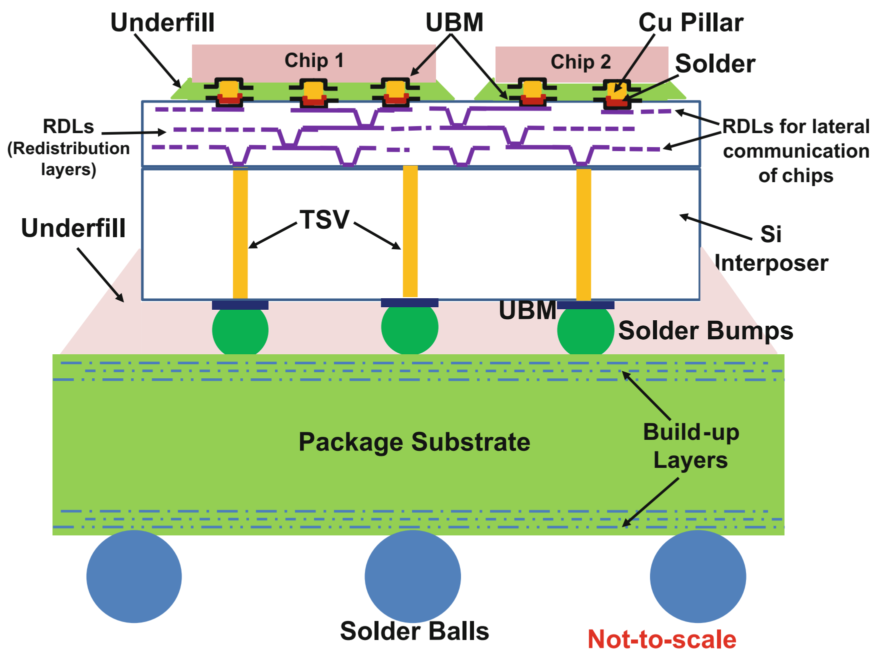


Fig. 10.19 TSV/RDL passive interposer supporting chips on package substrate

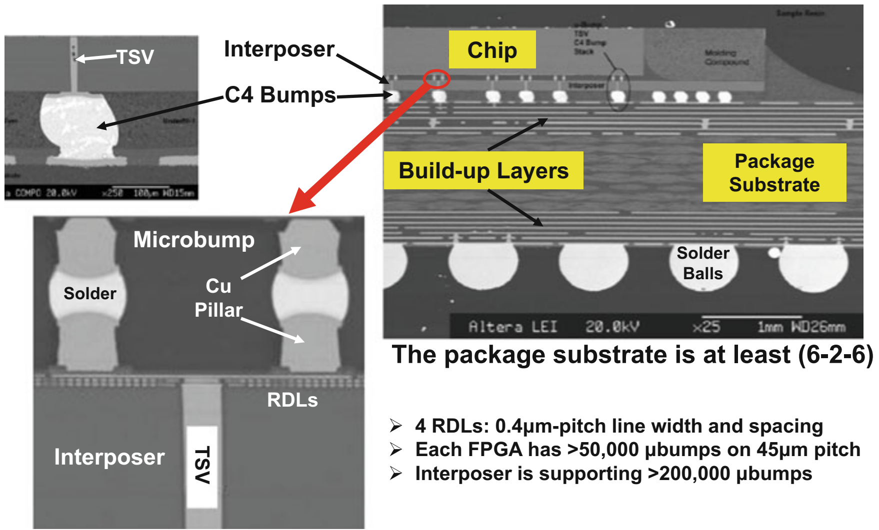


Fig. 10.20 Altera/TSMC's chips on wafer on substrate (CoWoS)

10.4.8 Fabrication of TSVs

The fabrication process of TSVs for interposer is shown in Fig. 10.21. The process starts with a SiN_x/SiO_x insulation layer by either thermal oxidation or PECVD (plasma enhanced chemical vapor deposition) as shown in Fig. 10.21. After photoresist and TSV lithography, the TSV is etched into the Si substrate by Bosch-type deep reactive ion etch (DRIE) [45] to form a high aspect ratio (10.5) via structure. The etched TSV structure is then processed with a SiO_x liner by sub-atmosphere chemical vapor deposition, a Ta barrier layer and a Cu seed layer by physical vapor deposition (PVD) [17]. Cu electroplating is used to fill the TSV structure. The final blind TSV has a top opening of approximately 10 µm in diameter and a depth of about 105 µm, which gives an aspect ratio of 10.5. In such a high aspect ratio via structure, a bottom-up plating mechanism is applied to ensure a seamless TSV with a reasonably low Cu thickness in the field.

The SEM cross-sectional images are shown in Fig. 10.22. It can be seen that the diameter of the TSV is slightly decreased at the bottom, which is expected from the etching process. The Cu thickness at the field is <5 µm. The post-plating anneal is at 400 °C for 30 min. To complete the TSV process, excess Cu in the field is removed by CMP [13].

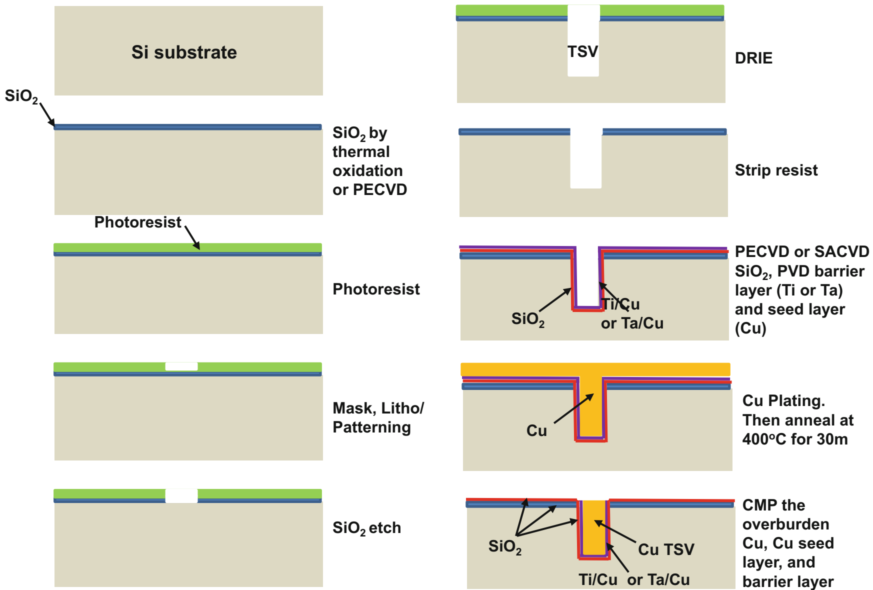


Fig. 10.21 TSV fabrication process flow

10.4.9 Fabrication of RDLs

There are at least two ways to fabricate RDLs [1–3, 5]. The first method is by using polymers, such as polyimide (PI) PWDC 1000 (Dow Corning), benzocyclobutene cyclotene (BCB) 4024-40 (Dow Chemical), polybenzo-bisoxazole (PBO) HD-8930 (HD Micro Systems), and the fluorinated aromatic AL-X 2010 (Asahi Glass Corporation) to make the dielectric layer and electroplating (such as Cu) to make the metal layers. This method has been used by the outsourced semiconductor assembly and test providers (OSATs) to fabricate RDLs for wafer-level (fan-in) chip scale package [130], embedded wafer-level (fan-out) ball grid array package [144–148], and (fan-out) redistribution chip package [149, 150]. The second method is the Cu damascene method, which is primarily modified from the conventional semiconductor BEOL to make the Cu metal RDLs such as those shown in Fig. 10.23. In general, much thinner structures (both dielectric layers and Cu RDLs), finer pitches, smaller line widths, and spacing can be obtained with the dual Cu damascene method, which will be briefly stated in the following.

If starting with the wafer from Fig. 10.21, the fabrication process of RDLs with a dual Cu damascene technique is primarily based on the semiconductor BEOL process. The details are shown in Fig. 2.23 and listed in the following [5]: (1) SiO_2 layer by PECVD, (2) apply photoresist and mask, then use photolithography techniques (align and expose) to open vias on the SiO_2, (3) RIE of SiO_2, (4) strip off portion of the photoresist, (5) repeat step 3, (6) strip off the photoresist, (7) sputter

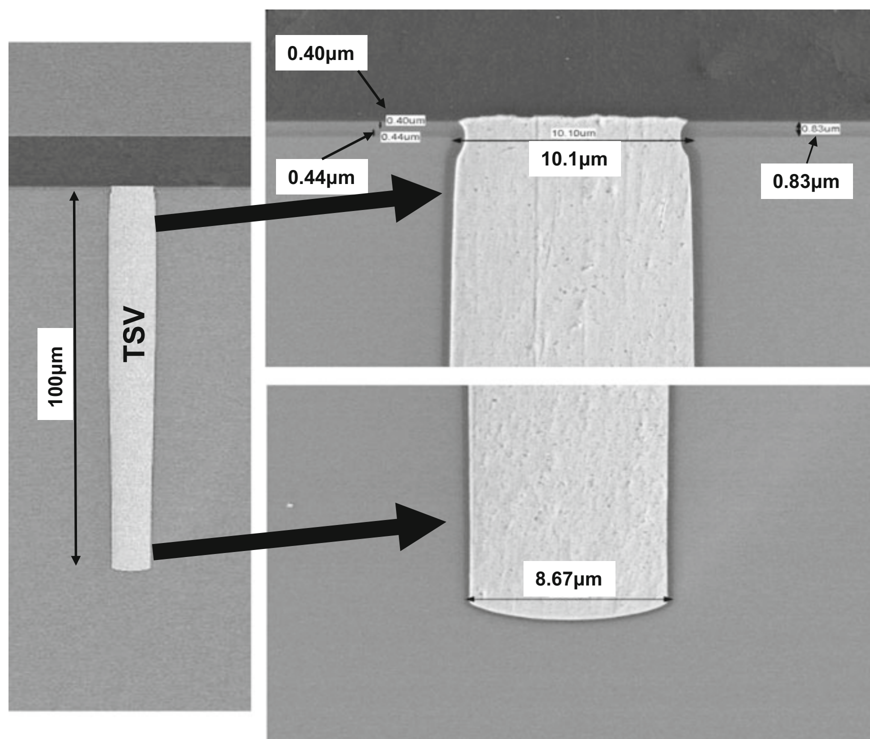


Fig. 10.22 SEM images of TSV cross sections

Ti and Cu and electroplate Cu over the entire wafer, (8) CMP the Cu and Ti/Cu and RDL1 is completed, and (9) repeat steps 1–8 to complete RDL2 and any additional layers. SEM images of the RDL cross sections fabricated by the Cu damascene technique are shown in Fig. 10.24. The minimum RDL line width is 3 µm. The thickness of RDL1 and RDL2 is 2.6 µm and of RDL3 is 1.3 µm. The dielectric thickness between RDLs is 1 µm.

10.4.10 Backside Processing and Assembly

The process flow of backside and assembly [5] is shown in Fig. 10.25. It can be seen that after the fabrication of TSV, RDLs, passivation, and UBM (under bump metallurgy), the topside of the interposer wafer is temporarily bonded to a carrier by adhesive. The next step is backgrinding the interposer wafer, Si etching, low-temperature passivation, and Cu revealing. Next, backside RDL (optional), UBM, and C4 (controlled collapse chip connection) wafer bumping are carried out. After that, the next step is to temporary bond another carrier wafer to the backside

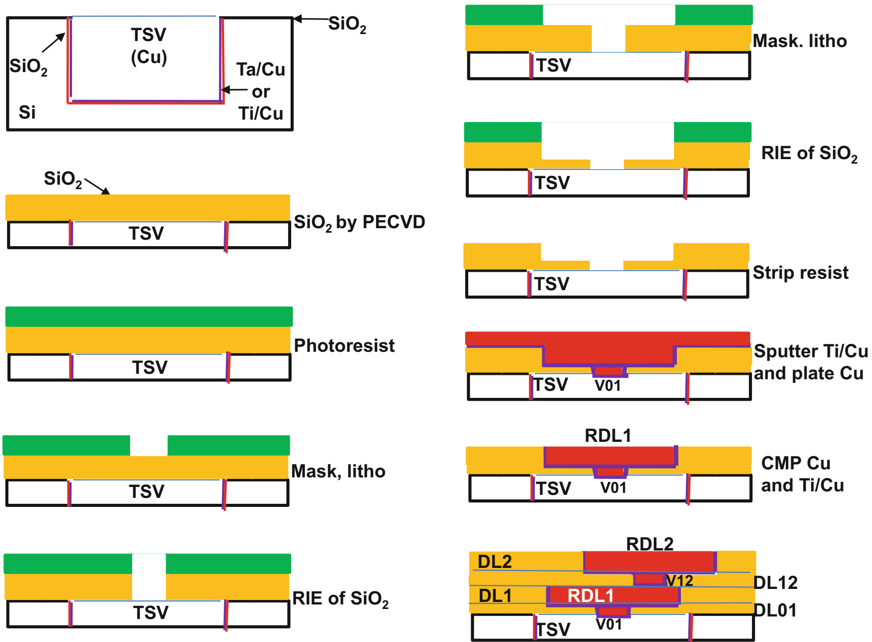


Fig. 10.23 Process flow for fabricating RDLs by dual Cu damascene

(with solder bumps) and debond the first carrier wafer. This step is followed by chip-on-wafer bonding and underfilling. After the whole (chip on) interposer wafer is completed, the next step is to debond the second carrier wafer and transfer the thin interposer wafer with attached chips to a dicing tape and ring for singulation. The individual TSV/RDL interposer with chips is attached to the package substrate by natural reflow and then underfilled.

10.4.11 Cu Revealing

Figure 10.26 shows more details on Cu revealing. Right after the temporary bonding of the support carrier, backgrind the wafer to a few microns to the tip of TSVs, Si dry etching (by RIE) to a few microns below the tip of TSVs, and low-temperature passivating the SiN/SiO$_2$ are performed. Then, CMP for SiN/SiO$_2$ buffing and barrier and Cu seed layers polishing are carried out. Cu revealing is completed and shown in Fig. 10.27 [5]. These processes also apply to device TSV wafers.

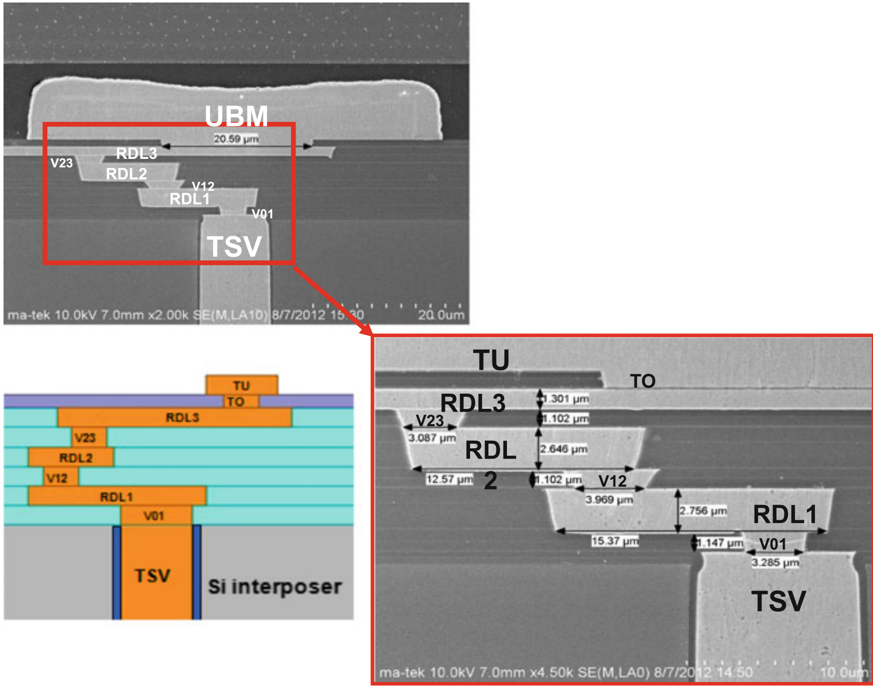


Fig. 10.24 SEM images of cross sections of RDLs fabricated by the Cu damascene method [5]

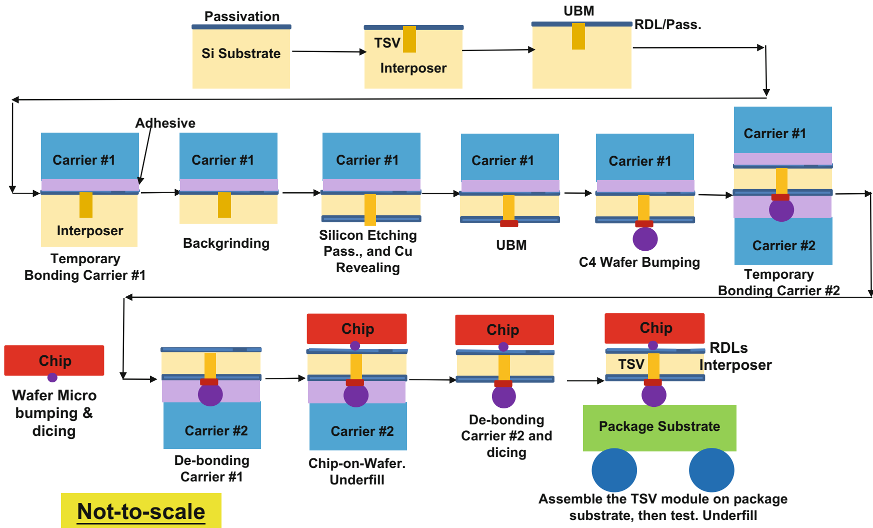


Fig. 10.25 Conventional process flow for chip on interposer wafer on package substrate [8]

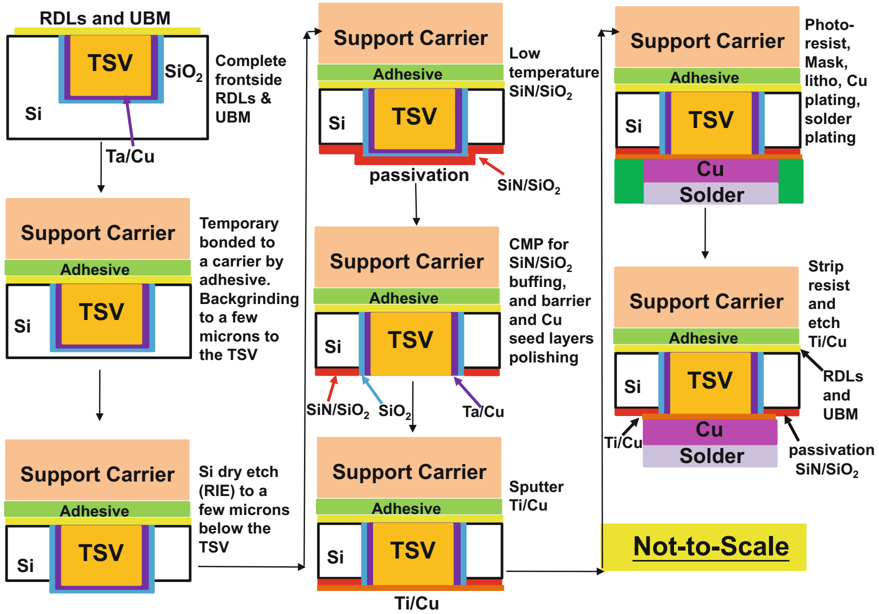


Fig. 10.26 Backside Cu reveal and UBM/solder plating process flow

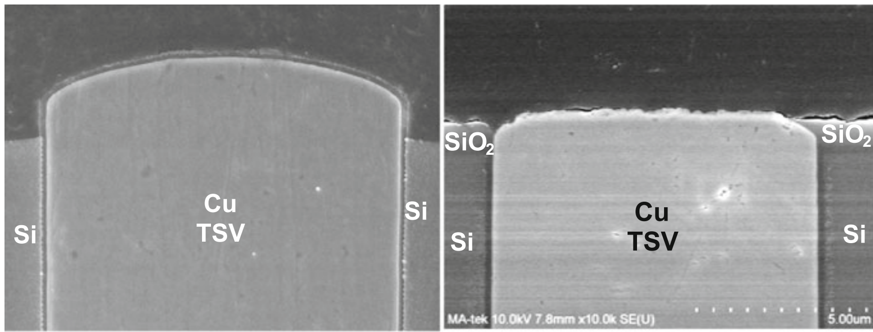


Fig. 10.27 TSV Cu revealing. (Left) Before dry etch of Si. (Right) After Si dry etching, low-temperature SiN/SiO_2, and removal (CMP) of the isolation, barrier, and seed layer

10.4.12 Outlook of 2.5D/3D IC Integration

TSVs straight through the same memory chips, e.g., DRAMs to enlarge the memory capacity, increase the bandwidth, lower the power consumption, lower the latency (enhance the electrical performance), and reduce the form factor is the right thing to do and will be the major application of 3D IC integration [151]. The memory stacking, HMC, HBM, and HBM2 are examples, which are targeted for

such as high-performance computing, cloud computing, in-memory database, graphic, networking, energy, wireless communications, transportation, security, and high-end servers.

TSV/RDL interposer (2.5D IC integration) is in small volume manufacturing by Xilinx/TSMC for the sliced FPGAs, which cannot be supported by the package substrate even with 12 buildup layers. Thus, interposer is for very high performance, high-density, high-I/O, and fine-pitch applications such as big data, cloud, augmented reality, substitutional reality, mixed reality, and artificial intelligence, networking, communications, high-end servers, etc.

10.5 Supply Chains Before the TSV Era

Before the TSV era, the technology supply chains are very well defined and understood. Descriptions of the various entities comprising the supply chain before the TSV era are presented below.

10.5.1 Front-End-of-Line (FEOL)

This is the first portion of IC fabrication where the individual devices such as transistors or resistors are patterned. This process is from a bare wafer to (but not including) the deposition of metal layers. FEOL is usually performed in semiconductor fabrication plants (fabs).

10.5.2 BEOL

This is the fabrication in which active devices are interconnected with wiring on the wafer. This process starts from the first layer of metal to bonding pads with passivation. It also includes insulators and metal contacts which are called middle-of-the-line (MOL). The term "MOL" is seldom used and embedded in the BEOL. Again, BEOL is usually performed in the fabs.

10.5.3 OSATs

Outsourced semiconductor assembly and test providers (OSATs) is also called packaging, assembly and test. The process starts when the passivated wafer is received from the fab and then goes through circuit probing, bumping, thinning, dicing, wiring bonding, flip chip, fan-in or fan-out RDLs, molding, ball mounting, final testing, and etc.

10.6 Supply Chains for the TSV Era—Who Makes the TSV?

The following steps in the TSV fabrication process impact the various considerations that must be addressed:

10.6.1 TSVs Fabricated by the via-First Process

The TSVs are fabricated before the FEOL. This can only be done by the fab. However, even in the fab, this seldom happens because the devices (e.g., transistors) are much more important than the TSVs.

10.6.2 TSVs Fabricated by the via-Middle Process

The TSVs are fabricated right after the FEOL (e.g., transistors) and MOL (e.g., metal contacts), and before the BEOL (e.g., metal layers). In this case, the MOL is no longer embedded in the BEOL because the TSV fabrication process is between them. Owing to logistics and equipment compatibilities, usually the TSV by the via-middle process is done by the fab.

10.6.3 TSVs Fabricated by the via-Last (from the Front-Side) Process

The TSVs are fabricated (from the front-side of the wafer) after the FEOL, MOL, and BEOL. As of today, there is not a single creditable paper published with this process.

10.6.4 TSVs Fabricated by the via-Last (from the Backside) Process

The TSVs are fabricated (from the backside of the wafer) after the FEOL, MOL, and BEOL process flows. The CMOS image sensor is an example. Strictly speaking, CMOS image sensors are not examples of 3D IC integration. For CMOS device sample wafers, the only creditable publication is given by LETI [152]. However, because of technical issues, such as hitting the various embedded alignment targets in the *x*-, *y*-, and *z*-directions (to enable the alignment between the

metal layers on the topside of the wafer and the positioning of TSVs formed from the backside), TSVs fabricated by the via-last (from the backside) process should be avoided until these issues are resolved. Based on the above discussions, it seems that for active device wafers being used for 3D IC integration applications, TSVs are better fabricated using the via-middle process. Also, the TSVs should be fabricated by the fabs, where all the equipment and expertise already exist and the cost to fabricate the TSVs is less than 5% of the cost in fabricating the (≤ 32 nm) device wafers!

10.6.5 How About the Passive TSV Interposers?

When the industry defined the TSV processes for 3D IC integration, there were no passive TSV interposers yet. Also, since there is no active device in the passive interposers, thus they do not fit into any of the preceding!

10.6.6 Who Wants to Fabricate the TSV for Passive Interposers?

Both the fab and OSATs want to do it! It depends on the layout, design, and fabrication capabilities, especially the line width and spacing of the RDLs and the diameter of the TSVs. Usually, for a few microns of line width and spacing of the RDL and ≥ 5 μm of TSV diameter it can be done by the OSATs. Otherwise, it should be done by the fabs. Today, there is not a single OSATs in HVM of TSVs for passive interposers.

10.7 Supply Chains for the TSV Era—Who Does the MEOL?

For the thicknesses of memory chip stacking and DRAMs in HMC and HBM, and interposers under consideration, all the TSVs fabricated are blind vias. The blind TSV wafer is followed by temporary bonding, backgrinding, TSV revealing, thin wafer handling, debonding, cleaning, solder bumping, etc., which, taken together, are called MEOL (middle end of line). Except for the vertically integrated companies (e.g., TSMC and Samsung), it is better for the MEOL process flow to be performed by the OSATs.

10.8 Outlook of HVM Supply Chains for TSVs and MEOL

For device wafers, the TSVs should be fabricated by the via-middle process and manufactured by the fabs. For deviceless wafers, it depends on the line width/spacing of the RDLs and the diameter of the TSVs, but it should also be done by the fabs. As to the MEOL, for both device and deviceless wafers, it should be done by the OSATs.

10.9 Summary and Recommendations

The overview, challenge, and outlook of 3D IC packaging, 3D IC integration, and 3D Si integration have been presented and discussed. The fabrication processes of TSVs and RDLs have also been mentioned. Furthermore, the supply chains of TSVs and 3D IC integration at HVM have been examined. Some important results and recommendations are summarized as follows:

- The driving forces for consumer products such as smartphones, tablets, and wearables are cost, cost, and cost. The cost-effective 3D IC packaging such as the stacked dies by wire bonding, PoP, chip-to-chip interconnect, and 3D embedded fan-out wafer-level packaging (FOWLP) are just the right technologies for these products.
- The driving forces for high-performance computing, cloud computing, networking, wireless communications, high-end servers are performance and reliability. The considerable high-cost 2.5D/3D IC integrations such as memory chip stacking with TSVs, HMC, HBM, and passive interposer are the right technologies for these products.
- For device wafers, the TSVs should be fabricated by the via-middle process and manufactured by the fabs. For interposer wafers, if the diameter of the TSVs is ≥ 5 μm and the line width/spacing of the RDLs is ≥ 3 μm, then it can be manufactured by the fabs and OSATs; otherwise, it should be done by the fabs. However, since most interposers are for very high performance, high-density, and fine-pitch applications, thus the TSV diameters and RDLs line width and spacing are most likely falling into the fabs' territory.
- As to the MEOL, assembly, and test of both the device and deviceless TSV wafers they should be performed by the OSATs except the vertical integrated companies such as TSMC and Samsung. There are many important tasks in MEOL, assembly, and test, thus the OSATs should strive to make themselves ready for a robust and high-yield manufacturing process.

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Chapter 11
3D IC Heterogeneous Integration by FOWLP

11.1 Introduction

Two 3D IC heterogeneous integrations by Fan-Out Wafer-Level Packaging (FOWLP) technology are presented in this chapter. The emphasis of the first such method is on the design, and of the other method, the emphasis is on the manufacturing process. The heterogeneous integration versus SoC (system-on-chip) will be briefly discussed. Some examples on the TSV (Through-Silicon Via)-less heterogeneous integration by FOWLP will also be presented. Since MCM (multichip module) is the *frontier* of heterogeneous integration and thus it will be briefly mentioned first.

11.2 Multichip Module (MCM)

MCM integrates different chips and discrete components side-by-side on a common substrate such as ceramic, silicon, or organic to form a system or subsystem for high-end networking, telecommunication, servers, and computer applications. Basically, there are three different kinds of MCM, namely, MCM-C, MCM-D, and MCM-L.

11.2.1 MCM-C

MCM-C are multichip modules that use thick film technology such as fireable metals to form the conductive patterns, and are constructed entirely from ceramic or glass-ceramic materials, or possibly, other materials having a dielectric constant above five. In short, an MCM-C is constructed on ceramic (C) or glass-ceramic substrates [1].

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11.2.2 MCM-D

MCM-D are multichip modules on which the multilayered signal conductors are formed by the deposition of thin-film metals on unreinforced dielectric materials with a dielectric constant below 5 over a support structure of silicon, ceramic, or metal. In short, MCM-D uses deposited (D) metals and unreinforced dielectrics on a variety of rigid bases [1].

11.2.3 MCM-L

MCM-L are multichip modules which use laminate structures and employ PCB (printed circuit board) technology to form predominantly copper conductors and vias. These structures may sometimes contain thermal expansion controlling metal layers. In short, MCM-L utilizes PCB technology of reinforced organic laminates (L) [1].

There was much research performed on MCMs during the 1990s. Unfortunately, at that time, due to the high cost of ceramic and silicon substrates and the limitation of line width and spacing of the laminate substrate, compounded with business models such as difficulty in getting the bare chips, the high-volume manufacturing (HVM) of MCMs never materialized, except some niche applications. Actually, since then, MCM has been a "dirty" word in semiconductor packaging.

11.3 System-in-Package (SiP)

11.3.1 Intention of SiP

SiP integrates different chips and discrete components, as well as 3D chip stacking of either packaged chips or bare chips (e.g., wide-bandwidth memory cubes and memory on logic with TSVs) side-by-side on a common (either silicon, ceramic, or organic) substrate to form a system or subsystem for smartphones, tablets, high-end networking, telecommunication, server, and computer applications. SiP technology performs horizontal as well as vertical integrations. Some people also called SiP vertical MCM or 3D MCM.

11.3.2 Actual Applications of SiP

Unfortunately, because of the high cost of TSV technology [2, 3] for smartphones and tablets, it never materialized. Most SiPs that went into HVM in the past

10 years are actually MCM-L for low-end applications such as smartphones, tablets, smart watches, medical, wearable electronics, gaming systems, consumer products, and internet of things (IoT)-related products [4] such as smart homes, smart energy, and smart industrial automation. Most actual applications of SiPs by OSATs (outsourced semiconductor assembly and test providers) integrate two or more dissimilar chips and some discrete components on a common laminated substrate.

11.3.3 Potential Applications of SiP

The applications of SiP for the high-price, high-margin, and high-end products are, e.g., dual-lens camera modules. However, right now this SiP cannot be all done by the OSATs, but also involves optical design, testing, lenses, micromotors, flexible substrate, and system integration capabilities which still need to be strengthened.

11.4 System-on-Chip (SoC)

Moore's law [5] has been driving the system-on-chip (SoC) platform. Especially in the past 10 years, SoCs have been very popular for smartphones, tablets, and the like. SoCs integrate different-function ICs into a single chip for a system or sub-system. Two typical SoC examples are shown in the followings.

11.4.1 Apple Application Processor (A10)

The application processor (AP) A10 is designed by Apple and manufactured by TSMC using its 16 nm process technology. It consists of a 6-core graphics processor unit (GPU), two dual-core central processing unit (CPUs), 2 blocks of static random access memories (SRAMs), etc. The chip area (11.6 mm $\times$ 10.8 mm) is 125 mm^2, Fig. 11.1a.

11.4.2 Apple Application Processor (A11)

The application processor A11 is also designed by Apple and manufactured using TSMC's 10 nm process technology. The A11 consists of more functions, including a tri-core Apple-designed GPU, neural engine for face ID, etc. However, the chip area (89.23 mm^2) is about 30% smaller than that of the A10 because of Moore's law, i.e., the feature size is from 16 nm down to 10 nm, Fig. 11.1b.

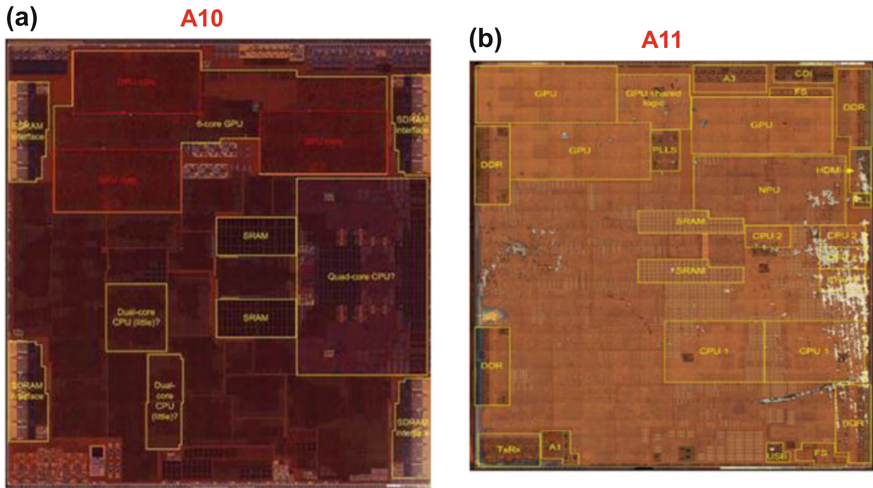


Fig. 11.1 SoC platforms for the A10 and A11 APs

11.5 Heterogeneous Integration

Some of the early researches in heterogeneous integration have been provided by Georgia Institute of Technology [6–8], where they reported a differential Si CMOS (complementary metal–oxide semiconductor) receiver IC (operating at 1 Gbps) integrated with a large-area thin-film InGaAs/InP I-MSM (metal–semiconductor–metal) photodetector (Fig. 11.2). Today, most heterogeneous integrations focus on higher density, finer pitch, and more complex system.

11.5.1 Heterogeneous Integration Versus SoC

Why is the heterogeneous integration of such great interest? One of the key reasons is because the end of Moore's law is fast approaching and it is more and more difficult and costly to reduce the feature size (to do the scaling) to make SoCs.

Heterogeneous integration contrasts with SoCs as follows. The heterogeneous integration uses packaging technology to integrate dissimilar chips (either side-by-side or stack) with different functions from different foundries, wafer sizes, and feature sizes (as shown in Fig. 11.3) into a system or subsystem on different (e.g., organic, silicon, or RDL) substrates, rather than integrating most of the functions into a single chip and going for a finer feature size. Heterogeneous integration and SiP are similar, except that heterogeneous integration is for finer pitch and higher density applications.

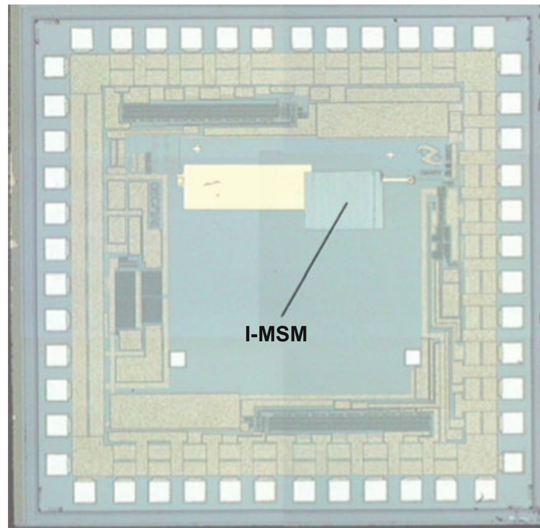


Fig. 11.2 InGaAs/InP I-MSM integrated onto differential Si CMOS receiver IC

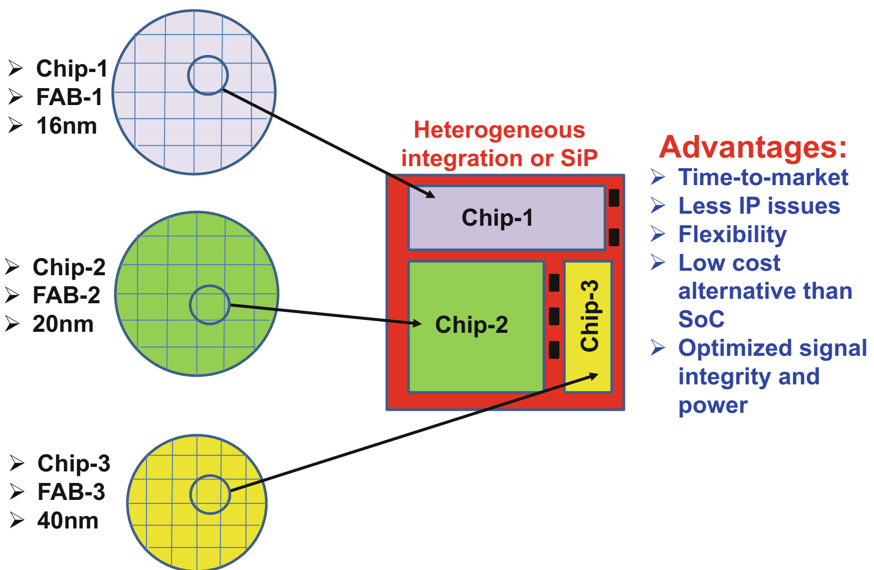


Fig. 11.3 Heterogeneous integration or SiP

11.5.2 Advantages of Heterogeneous Integration

For the next few years, we will see more of a higher level of heterogeneous integration, whether it is for time-to-market, performance, form factor, power consumption, signal integrity, or cost. Heterogeneous integration is going to take some of the market shares away from SoCs on high-end applications such as high-end smartphones, tablets, wearables, networkings, telecommunications, and computing devices. How should these dissimilar chips talk to each other, however? The answer is redistribution layers (RDLs) [9]! How should those RDLs be made? One key method is by FOWLP technology.

11.6 Heterogeneous Integration on Organic Substrates

Today, the most common applications of heterogeneous integration are on organic substrates, or the so-called SiP. The assembly methods are usually SMT (surface mount technology) including flip chips with mass reflow as shown in Fig. 2.16a and wire bonding chips on board. In general, this is for low-end to middle-end applications.

11.6.1 Amkor's SiP for Automobiles

Amkor's SiP for automobiles focuses on autonomous driving, infotainment, and ADAS (advanced drive assist systems), and computer in a car. Figure 11.4a, b shows a couple of examples of Amkor's SiP for automobiles. It can be seen from Fig. 11.4a that the 42.5 mm × 42.5 mm infotainment organic substrate is supporting the processor and DDR (double data rate) memories. While from Fig. 11.4b, the 55 mm × 72 mm organic substrate is supporting the network switch, ASIC (application-specific integrated circuit), and memories.

11.6.2 Apple Watch II (SiP) Assembled by ASE

Through USI (Universal Scientific Industrial), ASE is a sole backend provider for Apple's custom-designed S2 SiP modules (Fig. 11.5) for use in the Apple Watch II. It can be seen from Fig. 11.5 that there are 42 chips and are on an organic substrate. Some of these chips are discrete passive components such as capacitors and resistors, ASIC, processors, controller, converter, DRAM (dynamic random access memory), NAND, Wi-Fi, NFC (near-field communication), GPS (global positioning system), sensors, etc.

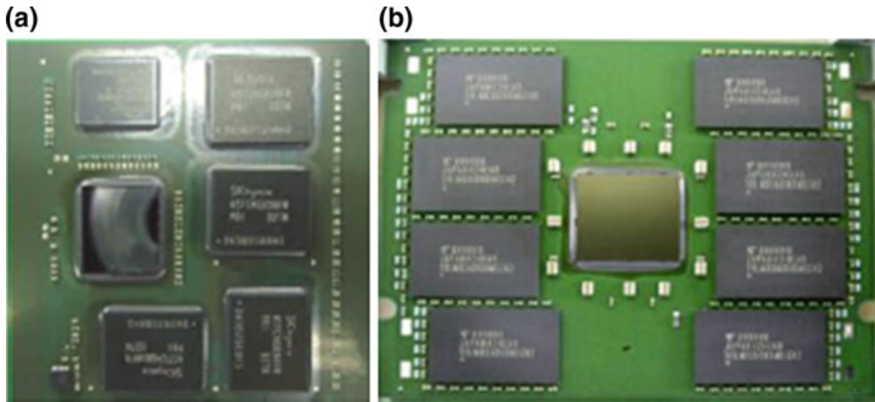


Fig. 11.4 Amkor's SiP for automobiles. **a** 42.5 mm × 42.5 mm infotainment. **b** 55 mm × 72 mm organic substrate

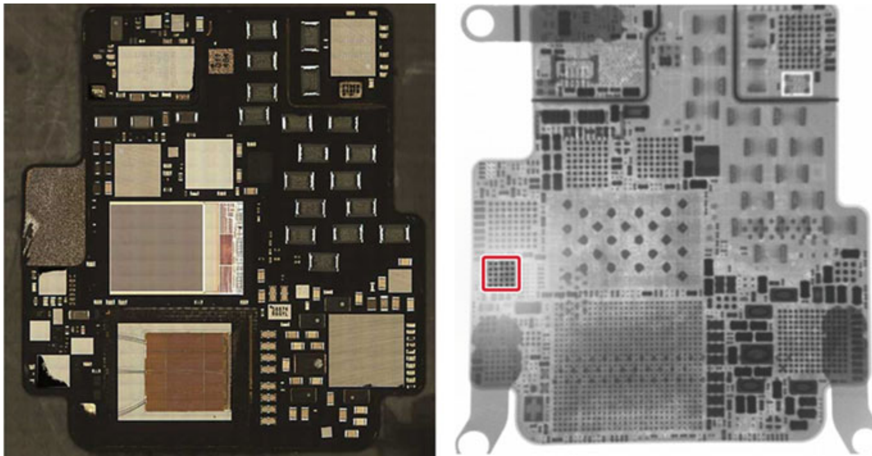


Fig. 11.5 Apple's smart watch SII assembled by ASE

11.6.3 Cisco's ASIC and HBM on Organic Substrate

Figure 11.6 shows a 3D system-in-package (SiP) designed and manufactured with a large organic interposer (substrate) with fine-pitch and fine-line interconnections by Cisco/eSilicon [10]. The organic interposer has a size of 38 mm × 30 mm × 0.4 mm. The linewidth, spacing, and thickness of the front-side and backside of the organic interposer are the same and are, respectively, 6, 6, and 10 µm. A high-performance ASIC die measured at 19.1 mm × 24 mm × 0.75 mm is attached on top of the organic interposer along with four HBM (high-bandwidth memory) DRAM die stacks.

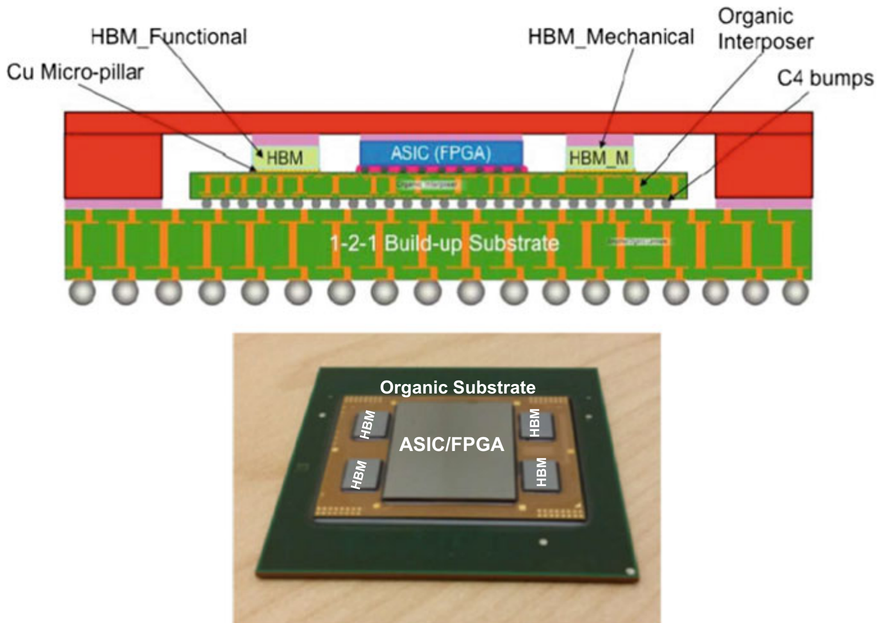


Fig. 11.6 Cisco's networking system with organic interposer

The 3D HBM die stack with a size of 5.5 mm × 7.7 mm × 0.48 mm includes one base buffer die and four DRAM core dice, which are interconnected with TSVs and fine-pitch micro-pillars with solder caps. This is for the high-end application.

11.6.4 Intel's CPU and Micron's HMC on Organic Substrate

Figure 11.7 shows Intel's Knights Landing CPU with Micron's HMC (hybrid memory cube), which have been shipping to Intel's favorite customers since the second-half of 2016. It can be seen that the 72-core processor is supported by 8 multichannel DRAMs (MCDRAM) based on Micron's HMC technology. Each HMC consists of 4 DRAMs and a logic controller (with TSVs), and each DRAM has >2000 TSVs with C2 bumps (Fig. 2.6). The CPU and the DRAM + logic controller stack are attached to an organic package substrate. Micron's current HMC assembly process is by using a low-force TCB (thermocompression bonding) with CUF (capillary underfill) as shown in Fig. 2.16b. This is for the high-end application.

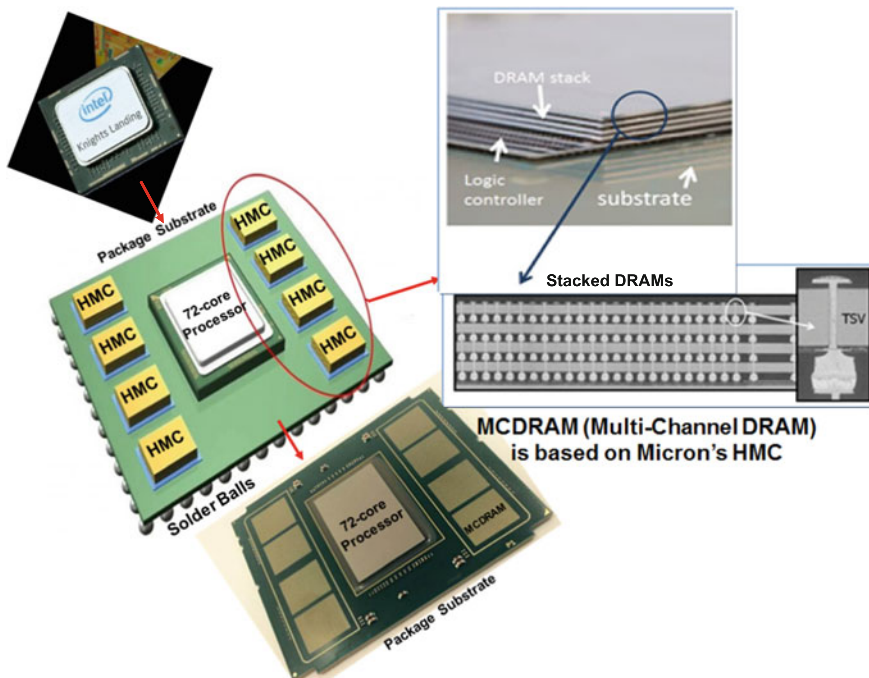


Fig. 11.7 Intel's Knights Landing and micron's HMC on an organic substrate

11.7 Heterogeneous Integration on Silicon Substrates (SoW)

In general, heterogeneous integrations on silicon substrates are for multichips on silicon wafer or system-on-wafer (SoW). The assembly methods are usually flip chips-on-wafers (CoW) with TSVs (through-silicon vias) with mass reflow (Fig. 2.16a) or with thermocompression bonding (Fig. 2.16b, c) for very fine pitches. In general, this is for high-end applications.

11.7.1 Leti's SoW

One of the early applications of SoW is given by Leti [11, 12] as shown in Fig. 11.8. It can be seen that a system of chips such as ASIC and memories, PMIC (power management IC) and MEMS (microelectromechanical systems) are on a silicon wafer with TSVs. After dicing, the individual unit becomes a system or subsystem and can be attached on an organic substrate or stand alone.

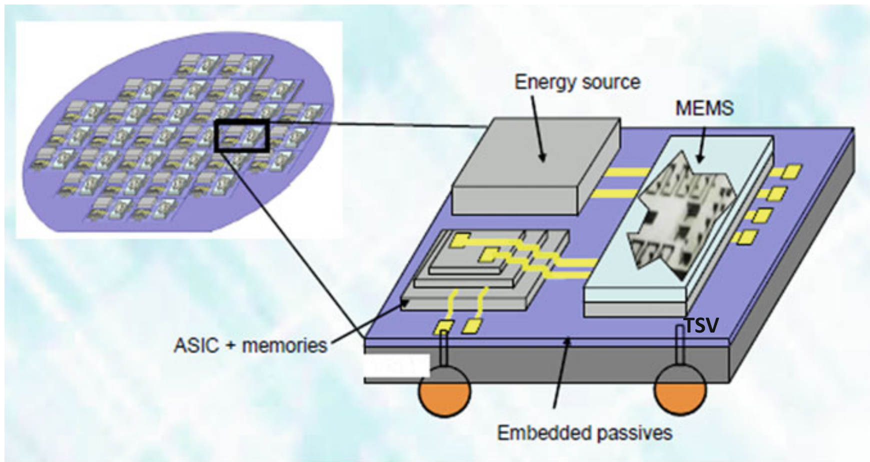


Fig. 11.8 Leti's SoW

11.7.2 Xilinx/TSMC's CoWoS

In the past few years, because of the very high-density, high I/Os, and ultrafine pitch requirements such as the sliced field-programmable gate array (FPGA), even a 12 build-up layers (6-2-6) organic package substrate is not enough to support the chips and a TSV-interposer is needed [13–22]. For example, Fig. 11.9 shows the Xilinx/TSMC's sliced FPBG chip-on-wafer-on-substrate (CoWoS) [15–17]. It can be seen that the TSV (10 μm diameter) interposer (100 μm deep) has four top RDLs: three Cu damascene layers and one aluminum layer. The 10,000+ of lateral interconnections between the sliced FPGA chips are connected mainly by the 0.4 μm pitch (minimum) RDLs of the interposer. The minimum thickness of the RDLs and passivation is <1 μm. Each FPGA has more than 50,000 microbumps (200,000+ microbumps on the interposer) at 45 μm pitch as shown in Fig. 11.9.

11.7.3 Analog Devices' MEMS on ASIC Wafer

Figure 11.10 shows Analog Devices' MEMS on ASIC wafer. It can be seen that the MEMS chip is bonded on the ASIC wafer with TSVs. After dicing the wafer into individual units, then they can be attached to the PCB (printed circuit board) with solder bumps (balls).

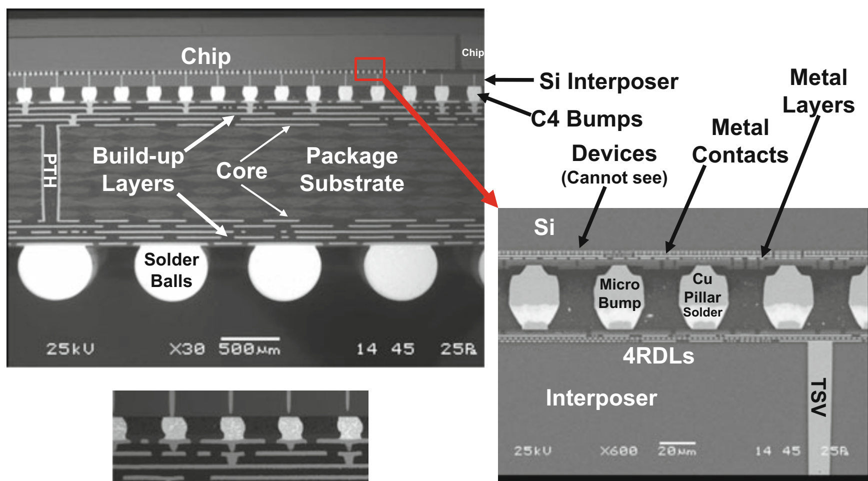
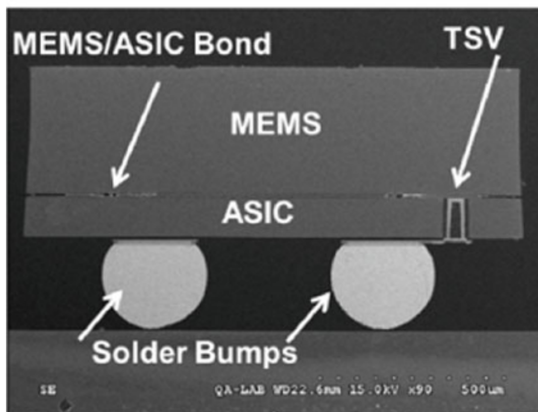


Fig. 11.9 Xilinx/TSMC's CoWoS



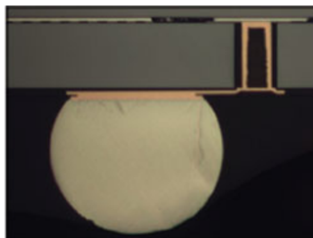


Fig. 11.10 Analog devices' MEMS on ASIC wafer

11.7.4 AMD's GPU and Hynix's HBM on TSV-Interposer

Figure 11.11 shows AMD's Radeon R9 Fury X graphic processor unit (GPU) shipped in the second-half of 2015. The GPU is built on TSMC's 28 nm process technology and is supported by four HBM cubes manufactured by Hynix. Each HBM consists of four DRAMs with C2 bumps and a logic base with TSVs straight through them. Each DRAM chip has >1000 TSVs. The GPU and HBM cubes are on top of a TSV interposer (28 mm × 35 mm), which is fabricated by

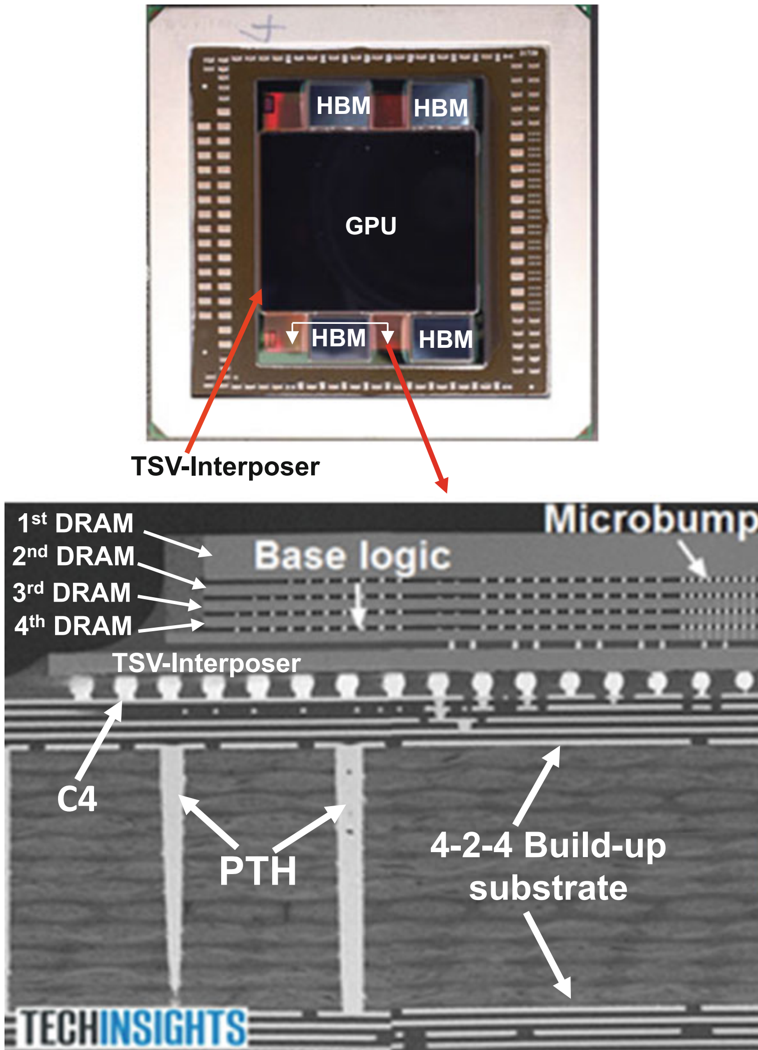


Fig. 11.11 IMD's GPU and Hynix's HBM on Si interposer

UMC with a 64 nm process technology. The final assembly of the TSV interposer (with C4 bumps as shown in Fig. 2.4) on a 4-2-4 organic package substrate (fabricated by Ibiden) is by ASE.

11.7.5 Nvidia's GPU and Samsung's HBM2 on TSV-Interposer

Figure 11.12 shows Nvidia's Pascal 100 GPU, which was shipped in the second-half of 2016. The GPU is built on TSMC's 16 nm process technology and is supported by four HBM2 (16 GB) fabricated by Samsung. Each HBM2 consists of four DRAMs with C2 bumps and a base logic die with TSVs straight through them. Each DRAM chip has >1000 TSVs. The GPU and HBM2s are on top of a TSV interposer (1200 mm^2), which is fabricated by TSMC with a 64 nm process technology. The TSV interposer is attached to a 5-2-5 organic package substrate with C4 bumps.

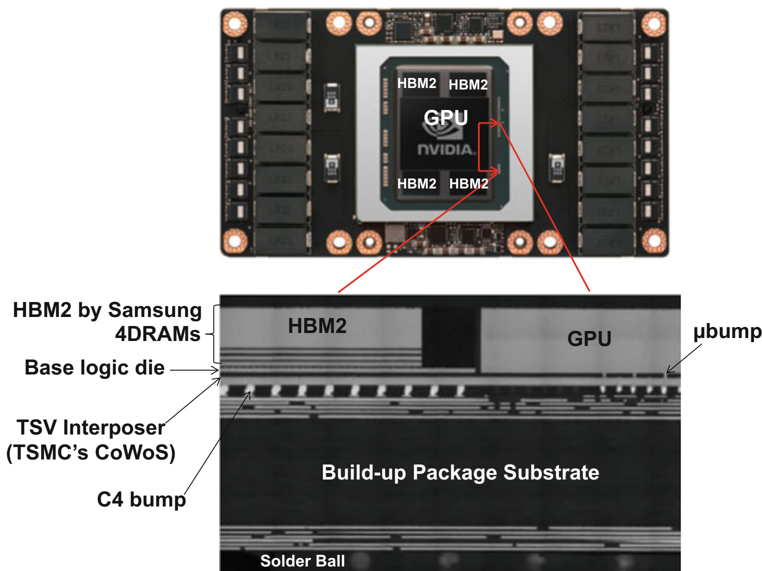


Fig. 11.12 Nvidia's GPU and Samsung's HBM2 on Si interposer

11.7.6 UCLA's SoW

Figure 11.13 shows the complete fabricated Si-IF (silicon interconnect fabric) by UCLA [23]. It can be seen that the test Si-IF has 4 dielets of size (4 mm × 4 mm) with an interconnect pitch of 10 μm and with a total of 640,000 connections. The Si-IF is fabricated using conventional Si-based BEOL (back end of line) processing with up to four levels of conventional Cu damascene interconnects with wire pitches in the range of 1–10 μm and is terminated with Cu pillars of 2–5 μm height and diameter also using a damascene process. Au-capped Cu–Cu thermocompression direct bonding has been used.

11.8 Heterogeneous Integration on RDLs

Recently, in order to lower the package profile, enhance the performance, and lower the cost, the heterogeneous integration on RDLs have been very popular, especially with the FOWLP technology. In general, this is for middle-end to high-end applications.

11.8.1 Xilinx/SPIL's TSV-Less SLIT

In the past few years, through-silicon via (TSV)-less interposer [24] to support flip chips is a very hot topic in semiconductor packaging. In 2014, Xilinx/SPIL

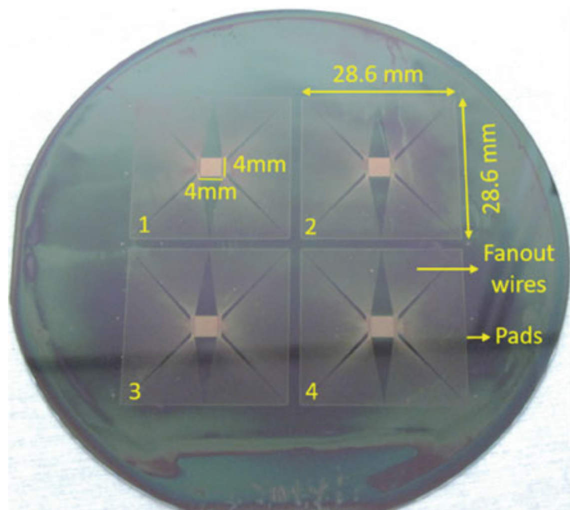


Fig. 11.13 UCLA's SoW

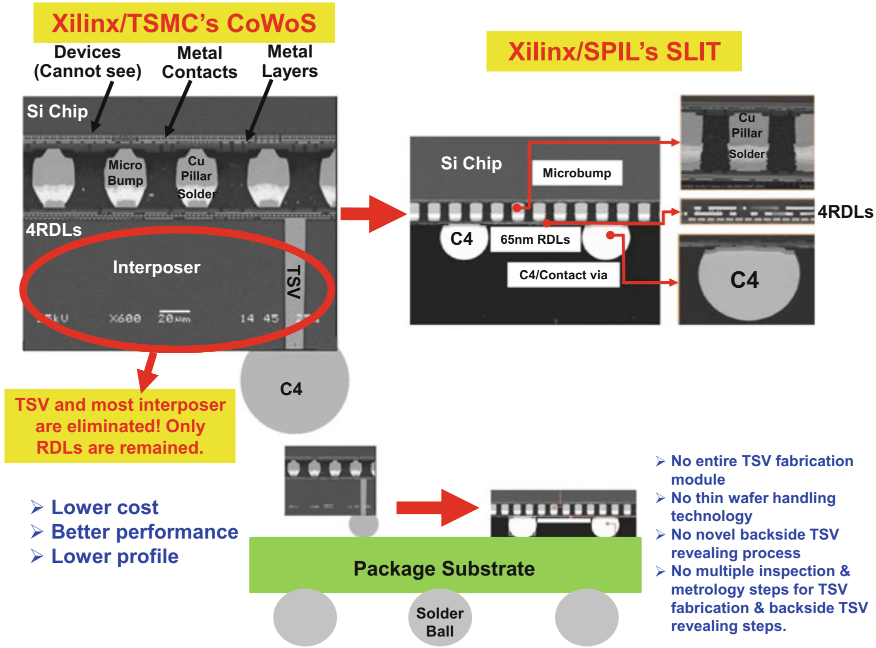


Fig. 11.14 Xilinx/SPIL's SLIT

proposed a TSV-less interposer for sliced FPGA chips called silicon-less interconnect technology (SLIT) [25]. The upper right-hand corner of Fig. 11.14 shows the new packaging structure along with the old one, which is shown in the left-hand corner. It can be seen that the TSVs and most of the interposer are eliminated and only the four RDLs needed for performance, mainly, the lateral communication of the sliced FPGA chips, remain.

The SLIT process flow is shown in Fig. 11.15. It starts off by fabricating the RDLs—examples on a bare silicon wafer can be seen in [9] (Fig. 11.15a). That process is followed by chip-to-wafer bonding (i.e., bonding the FPGA chip to the silicon wafer with RDLs; Fig. 11.15b), and underfilling/curing (Fig. 11.15c). These processes are followed by overmolding the whole wafer with an epoxy mold compound (EMC) (Fig. 11.15d). It is followed by backgrinding the over mold to expose the backside of the chips and attaching an optional reinforcement wafer on the backside of the chips (Fig. 11.15d). Then, backgrind the silicon wafer (Fig. 11.15e). Next come passivation, photoresist, mask, patterning, etching, sputtering TiCu, photoresist, mask, and patterning (Fig. 11.15f). Finally, Cu-contact pad plating (Fig. 11.15g), photoresist stripping, TiCu etching, and controlled-collapse chip connection (C4) wafer bumping are done (Fig. 11.15h). The final assembly of the heterogeneous integration package on the substrate and then on PCB is shown in Fig. 11.16.

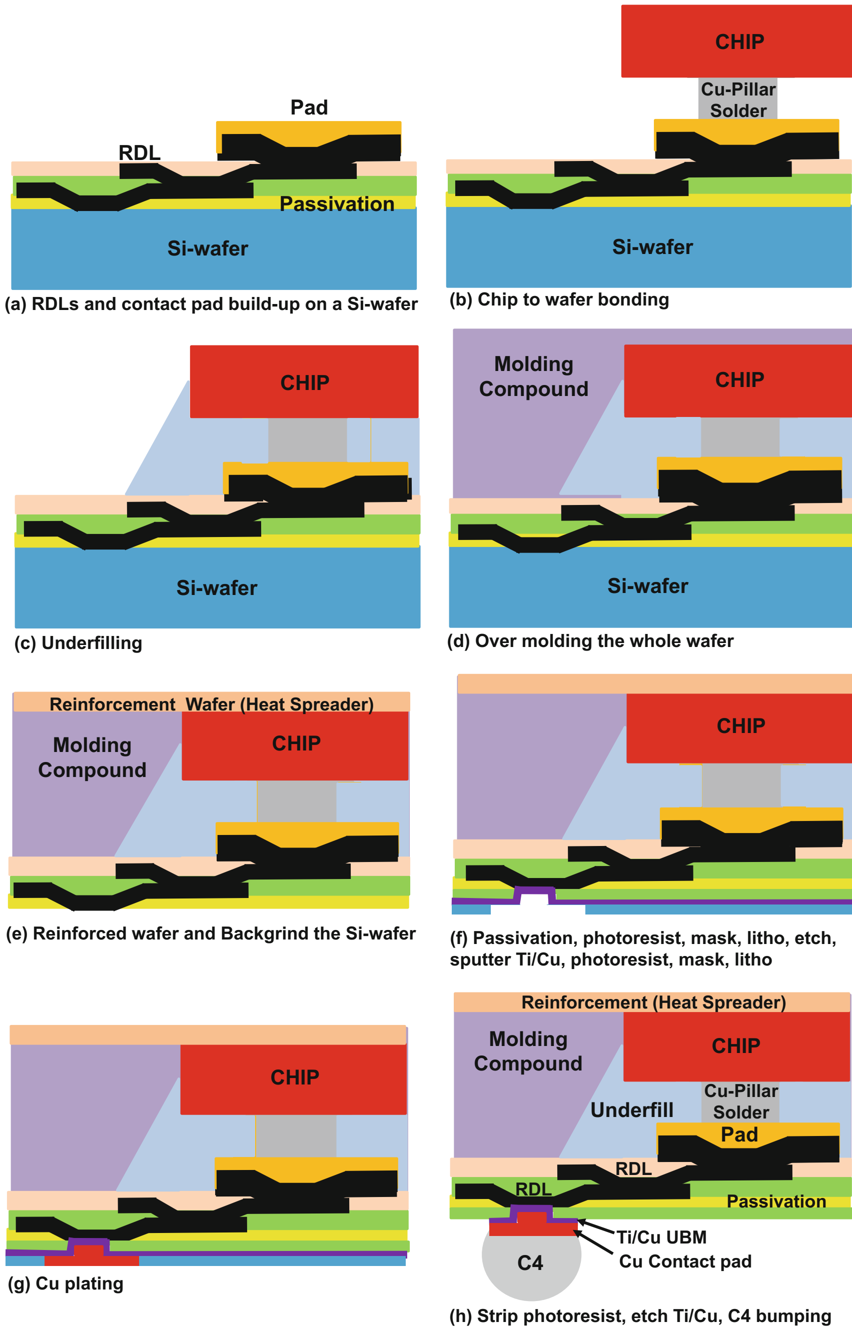


Fig. 11.15 Process flow for implementing SLIT technology

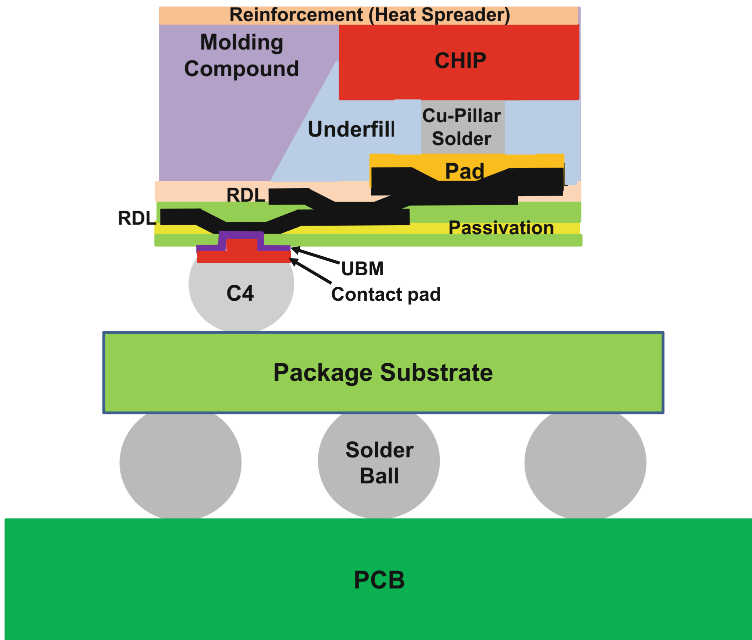


Fig. 11.16 Final assembly of the Xilinx/SPIL's SLIT

Depending on the linewidth/spacing of the RDLs' conductive wiring, the fabrication method of the RDLs can be accomplished either by using a polymer for the dielectric layer and Cu plating of the conductive wiring (line width/spacing ≥ 5 µm), or by using plasma-enhanced chemical vapor deposition (PECVD) to make the SiO_2 dielectric layer and Cu damascene plus chemical mechanical polishing (CMP) to make the conductive wiring (linewidth/spacing <5 µm). In 2016, SPIL/Xilinx published a similar paper [26] with more characterization results including warpage data and called it non-TSV interposer (NTI).

11.8.2 Amkor's TSV-Less SLIM

In 2015, Amkor announced a very similar technology to SLIT and is called silicon interposer-less integrated module (SLIM) [27].

11.8.3 Intel's TSV-Less EMIB (RDL) for FPGA and HBM

Intel proposed an embedded multi-die interconnect bridge (EMIB) [28] RDLs to replace the TSV interposer [29]. The lateral communication between the chips will be taken care of by the silicon embedded bridge and the power/ground and some signals will go through the organic package substrate as shown in Fig. 11.17. There are two major tasks in fabricating the organic package substrate with EMIB. One is to make the EMIB, and the other is to make the substrate with EMIB. To make the EMIB, one must first build the RDLs (including the contact pads) on a Si wafer. The way to make the RDLs depends on the line width/spacing of the conductive wiring of the RDLs. Finally, attach the non-RDL side of the Si wafer to a die-attach film, and then singulate the Si wafer.

To make the substrate with an EMIB, first place the singulated EMIB with the die-attached film on top of the Cu foil in the cavity of the substrate, Fig. 11.18a. It is followed by laminating a resin film on the whole organic package substrate. Then, drilling (on epoxy resin) and Cu plating to fill the holes (vias) to make connections to the contact pads of the EMIB. Continue Cu plating to make lateral connections of the substrate as shown in Fig. 11.18b. Then, it is followed by laminating another resin film on the whole substrate and drilling (on resin) and Cu

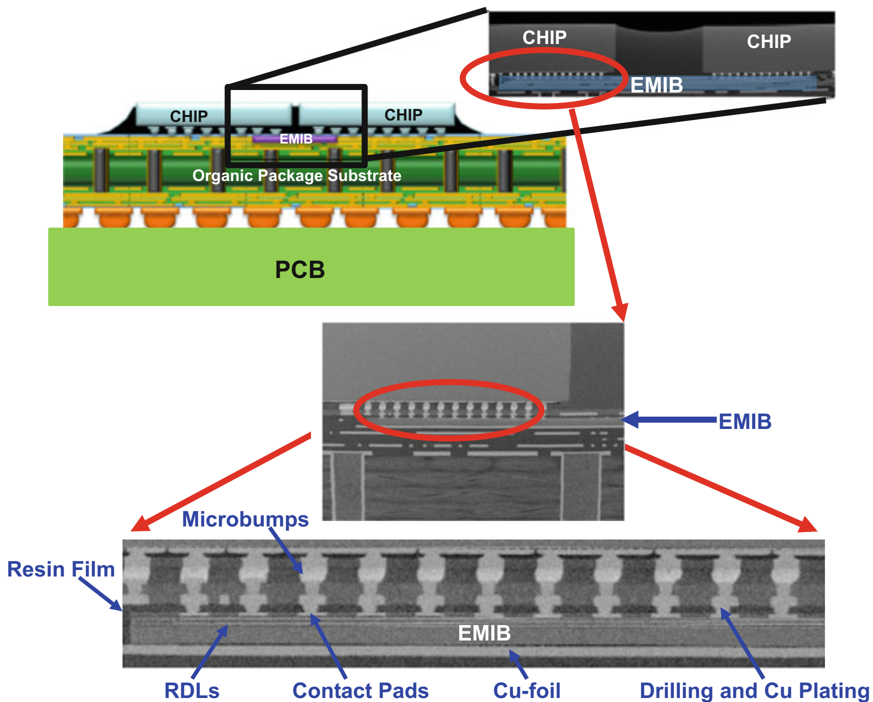


Fig. 11.17 Intel's TSV-less interposer—EMIB

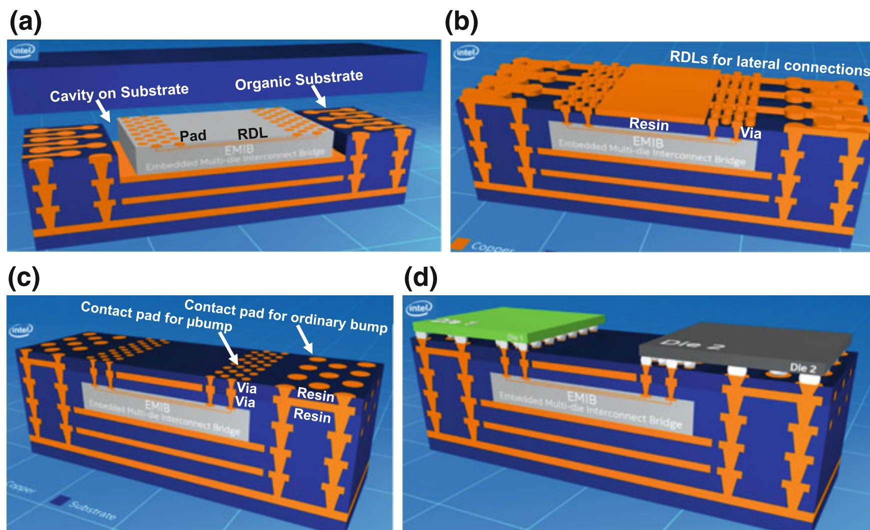


Fig. 11.18 Assembly process of Intel's EMIB

plating to fill the holes and make contact pads, Fig. 11.18c. (Smaller pads on a finer pitch are for microbumps, while larger pads on a gross pitch are for ordinary bumps). The organic package substrate with an EMIB is ready for bonding of the chips as shown in Fig. 11.18d.

On November 9, 2015, Altera/Intel announced the industry's first heterogeneous integration devices that integrate stacked HBM from SK Hynix with high-performance Stratix® 10 FPGAs and SoCs as shown in Fig. 11.19. It can be seen that the TSV interposer is gone and replaced by Intel's EMIB.

It is interesting to note that in order to use the EMIB, the chips will have different kinds/sizes of bumps as shown in Fig. 11.19, i.e., C4 bumps and microbumps (Cu pillar + solder cap). Wafer bumping and flip chip assembly could be challenging.

11.8.4 EMIB (RDL) for Intel's CPU and AMD's GPU

On November 6, 2017, Intel has formally revealed it has been working on a new series of processors that combine its high-performance ×86 cores CPUs with AMD GPUs (Radeon Graphics), as shown in Fig. 11.20, into the same processor package (heterogeneous integration) using Intel's own EMIB multi-die technology. If that wasn't enough, Intel also announced that it is bundling the design with the latest high-bandwidth memory, HBM, as shown schematically in Fig. 11.21.

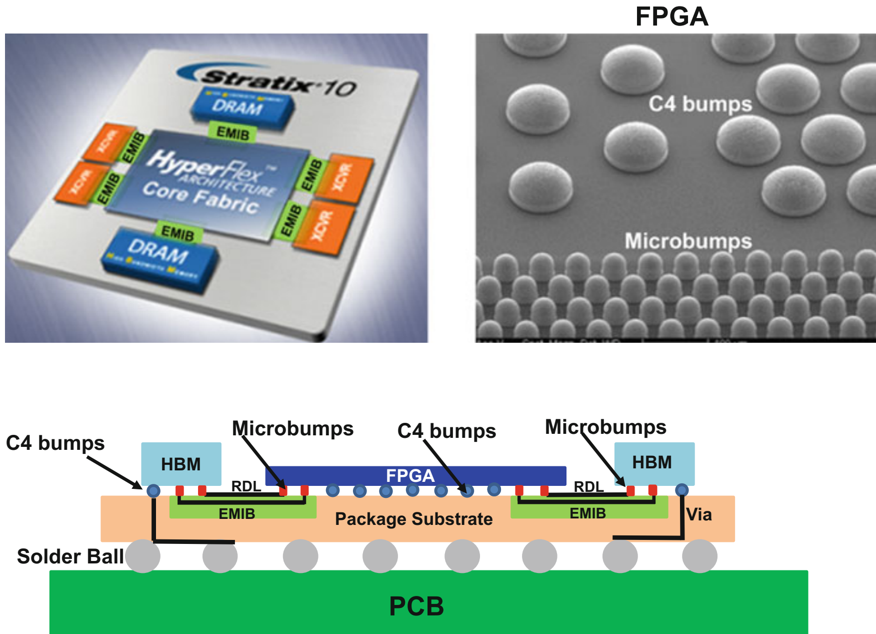
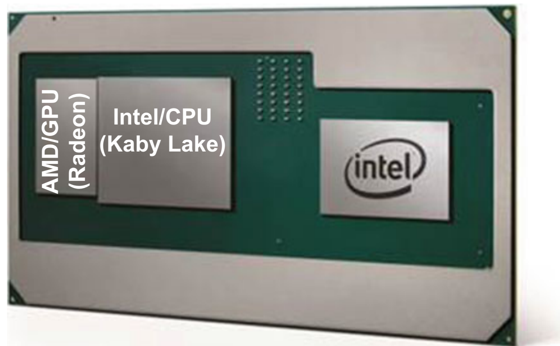


Fig. 11.19 Intel's FPGA and HBM on EMIB

Fig. 11.20 Intel's CPU and AMD's GPU on EMIB



11.8.5 STATS ChipPAC's FOFC-eWLB

At ECTC2013, STATS chipPAC proposed [30, 31] using the fan-out flip chip (FOFC)-eWLB to make the RDLs for the chips to perform mostly lateral communications as shown in Fig. 11.22. It can be seen that the TSV interposer, wafer bumping, fluxing, chip-to-wafer bonding, cleaning, and underfill dispensing and curing are eliminated.

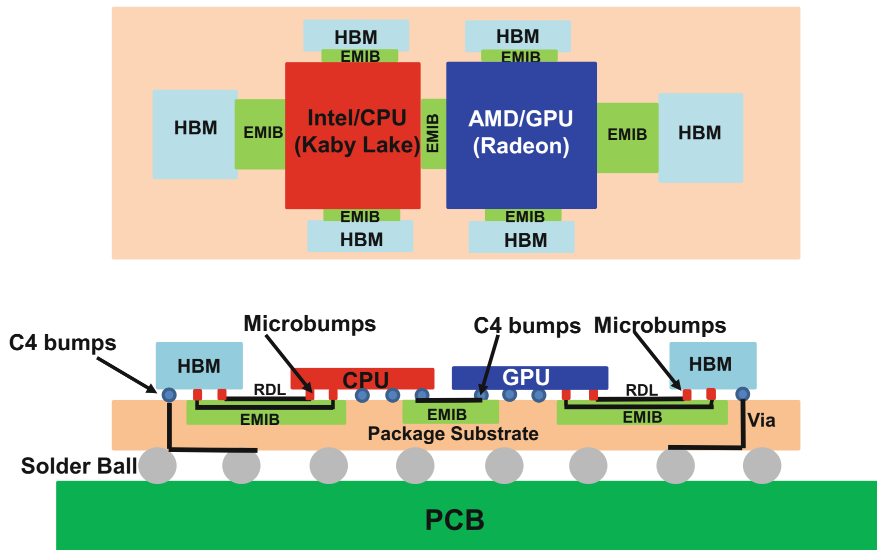
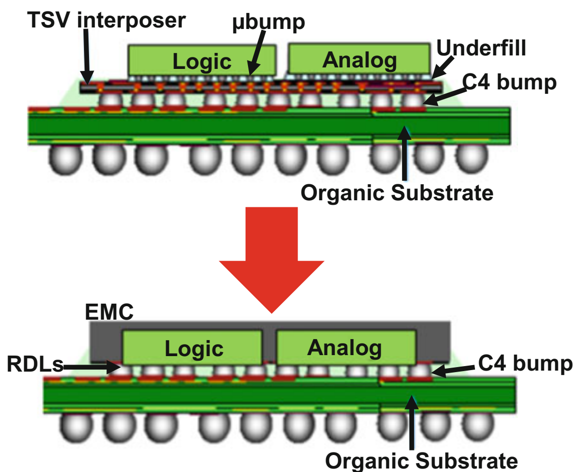


Fig. 11.21 Schematic of Intel's CPU, AMD's GPU, and Hynix's HBM on EMIB

Fig. 11.22 STATSChipPac's TSV-less FOFC-eWLB



11.8.6 ASE's FOCoS

In 2016, ASE [32] proposed using the fan-out wafer-level packaging (FOWLP) technology (chip-first and die-down on a temporary wafer carrier and then over-molded by the compression method) to make the RDLs for the chips to perform mostly lateral communications as shown in Fig. 11.23; the technology is called

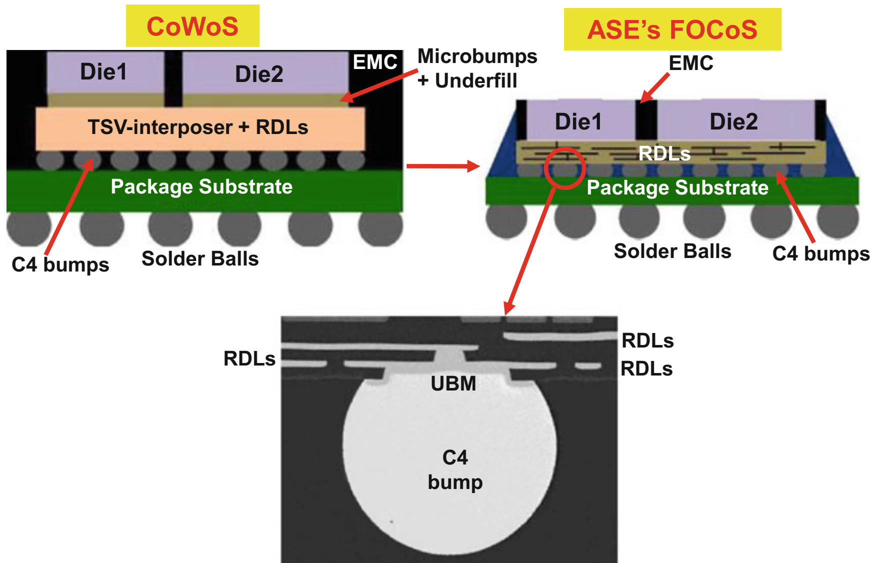


Fig. 11.23 ASE's FOCoS

fan-out wafer-level chip-on-substrate (FOCoS). The TSV interposer, wafer bumping of the chips, fluxing, chip-to-wafer bonding, and cleaning, and underfill dispensing and curing are eliminated. The bottom RDL is connected to the package substrate using under bump metallurgy (UBM) and the C4 bump as shown in Fig. 11.23.

11.8.7 MediaTek's RDLs by FOWLP

In 2016, MediaTek [33] proposed similar TSV-less interposer RDLs fabricated with FOWLP technology as shown in Figs. 11.24 and 11.25. Instead of the C4 bump, they used a microbump (Cu pillar + solder cap) to connect the bottom RDL to the 6-2-6 package substrate.

11.9 3D IC Heterogeneous Integration by FOWLP

A low-profile and low-cost 3D IC heterogeneous integration of the application processor chipset by FOWLP is presented in this section. The emphasis is placed on the design of the package.

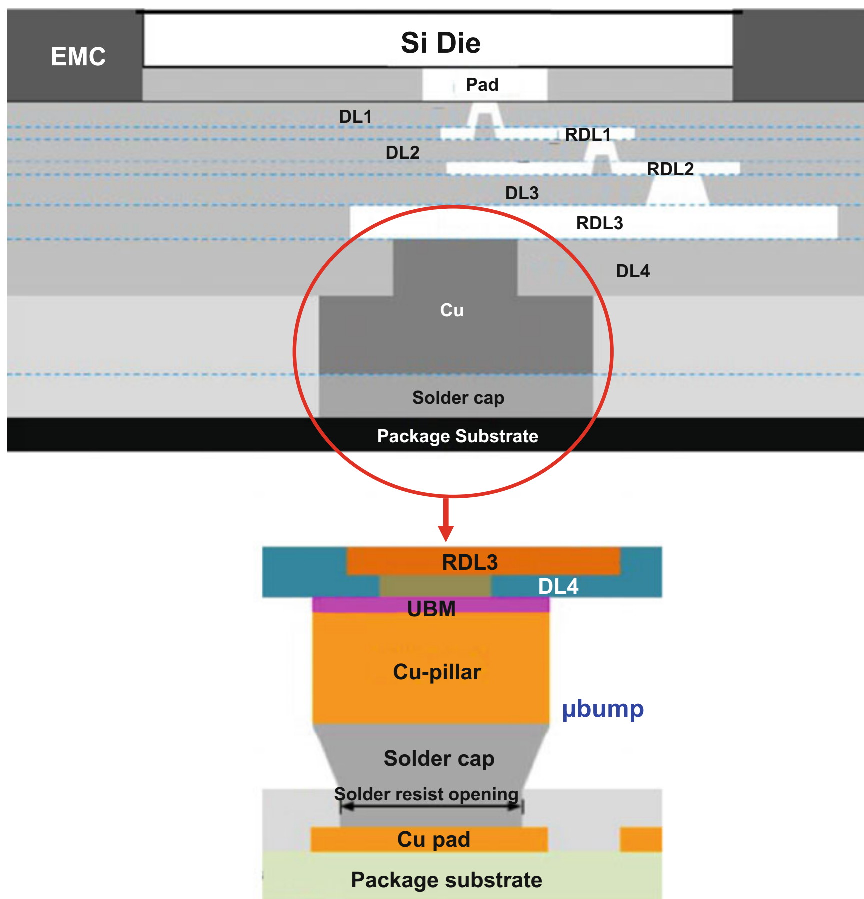


Fig. 11.24 Schematic of MediaTek's RDLs by FOWLP

11.9.1 Application Processor with FOWLP

The A10 and A11 application processors are packaged using TSMC's InFO (integrated fan-out) wafer-level packaging method [34–44]. The mobile dynamic random access memories (DRAMs) are wire bonded on a 3-layer core-less package substrate and the substrate is area-array solder balled on top of the application processor package—a package-on-package (PoP) format as shown schematically in Fig. 11.26. The interconnections between the application processor and the mobile DRAMs are mainly through the RDLs, through-InFO vias (TIVs), solder balls, and core-less substrate.

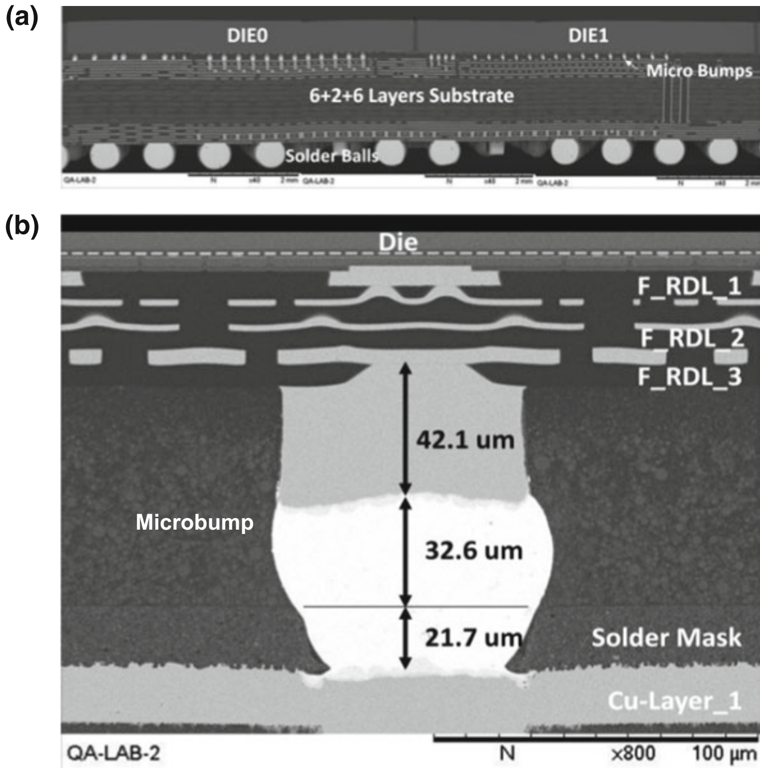


Fig. 11.25 SEM images of MediaTek's RDLs by FOWLP

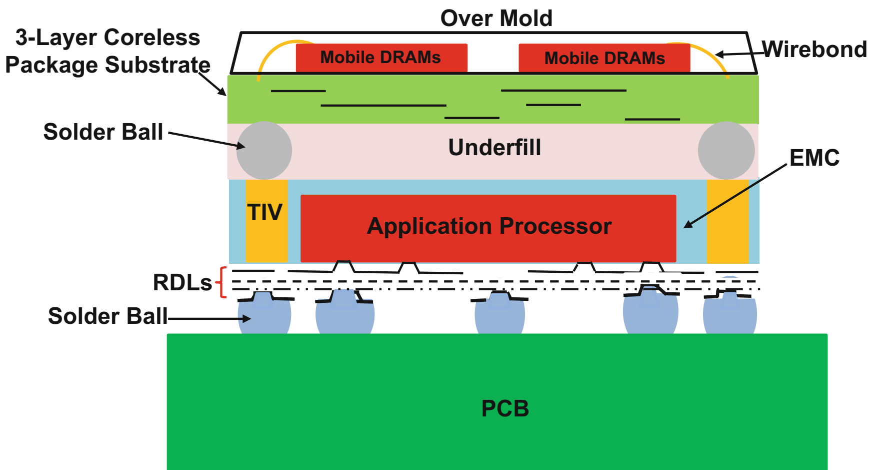


Fig. 11.26 PoP for packaging the application processor and mobile memory

11.9.2 Application Processor by 3D IC Heterogeneous Integration with FOWLP

A new 3D IC heterogeneous integration by FOWLP, as shown in Fig. 11.27, is proposed in this chapter. It consists of the SoC, chips, and the mobile DRAMs. Their interconnections are mainly through the RDLs, which can be fabricated by the FOWLP method. Depending on the number of layers of the RDLs, usually the total thickness of a 3-layer RDL is about 40 μm. The DRAMs ($\leq$ 50 μm thick) are cross-stacked with wire bonds and then encapsulated. The diameter of the solder ball is usually 200 μm.

Figure 11.28 shows a special case of Fig. 11.27 (when there is no other chip and the SoC is the application processor). Comparing the new design (Fig. 11.28) with that of Fig. 11.26 (the 3D IC heterogeneous integration vs. the PoP), it is obvious that: (1) the new design leads to a lower package profile; (2) the new design has less interconnects; (3) the new design is more reliable because of less interconnects; (4) the new design has better electrical performance; and (5) the new design leads to lower cost.

The manufacturing process of the proposed 3D IC heterogeneous integration is very simple. First, the device wafer has to be modified by sputtering an under bump metallurgy (UBM) and electroplating a Cu contact pad (for building the RDLs later), as shown in Fig. 11.29. This step is followed by spin coating a polymer on top of the device wafer and laminating a die-attach film (DAF) at the bottom of the device wafer. Meanwhile, a light-to-heat conversion (LTHC) layer is spin coated onto the temporary glass carrier wafer. Then the individual known-good die (KGD) (chip) from the device wafer is placed face-up on the LTHC carrier. This step is followed by epoxy molding compound (EMC) dispensing, compression molding, and finally, post mold cure (PMC). These steps are followed by backgrinding the EMC and polymer to expose the Cu contact pad for making the RDLs and for mounting the solder balls, as shown in Fig. 11.29. This is the conventional FOWLP method to package the application processor [34–44], as shown in Chap. 6.

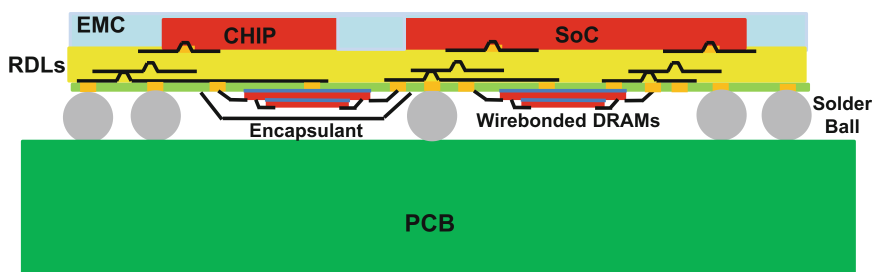


Fig. 11.27 3D IC heterogeneous integration by FOWLP

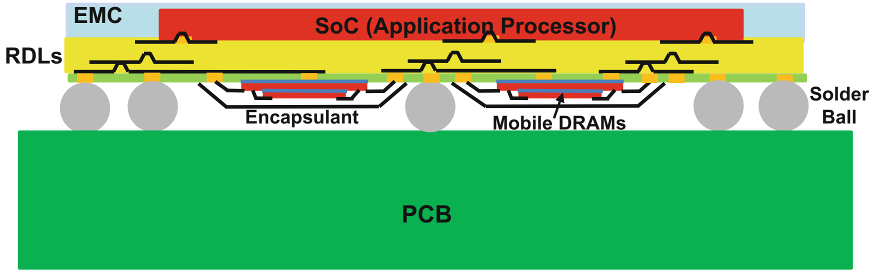


Fig. 11.28 3D IC heterogeneous integration to package the application processor chipset

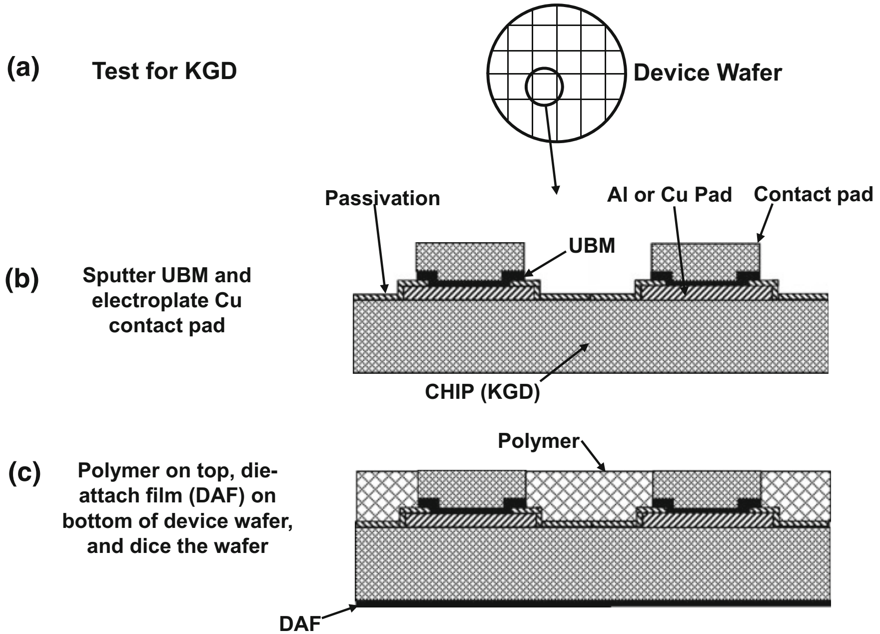


Fig. 11.29 Manufacturing process for packaging the application processor chipset

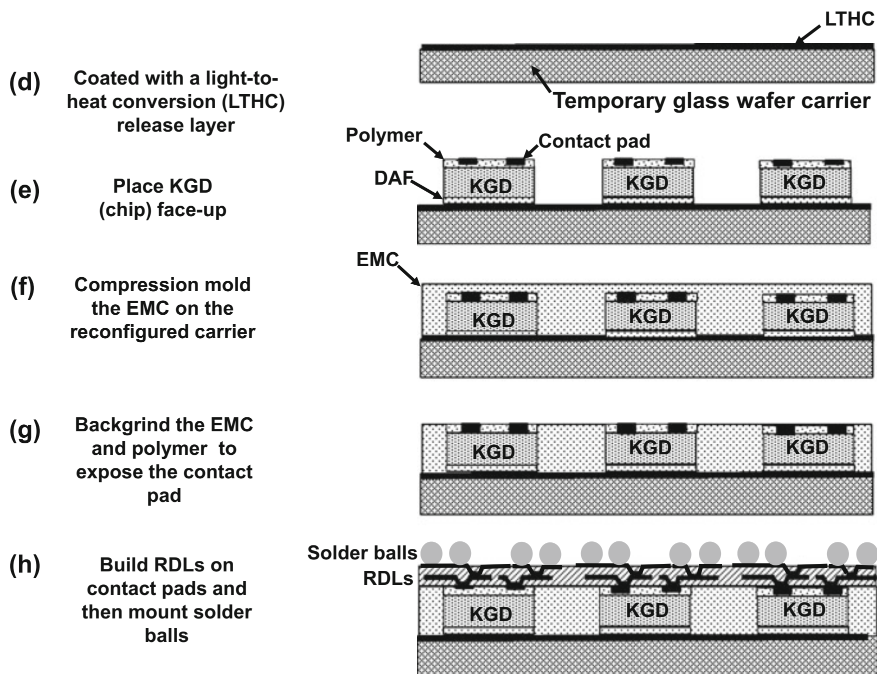


Fig. 11.29 (continued)

There are two methods to attach the mobile DRAMs to the bottom of the application processor fan-out wafer-level package. The first method comprises the following steps: (1) removing the glass carrier by a laser (Fig. 11.30a); (2) dicing the reconstituted wafer into strips with individual packages (Fig. 11.30b); (3) wire bonding the memory chips to the bottom side of the individual package (Fig. 11.30c, d); (4) and then glob topping the wires and memory chips with an encapsulant (Fig. 11.30c, d).

The second method to attach the mobile DRAMs to the bottom of the application processor fan-out wafer-level package comprises the following steps: (1) wire bonding the memory chips to the bottom side of every package on the reconstituted wafer; (2) glob topping the wires and memory chips with an encapsulant; and (3) then dicing the reconstituted wafer into individual packages (Fig. 11.31).

Figure 11.32 is a special case of Fig. 11.27. This is when it is difficult and costly to reduce the feature size to make the SoC. Therefore, some of the functions (for example, the GPU) are not integrated into the SoC and the GPU chip is placed side-by-side with the SoC.

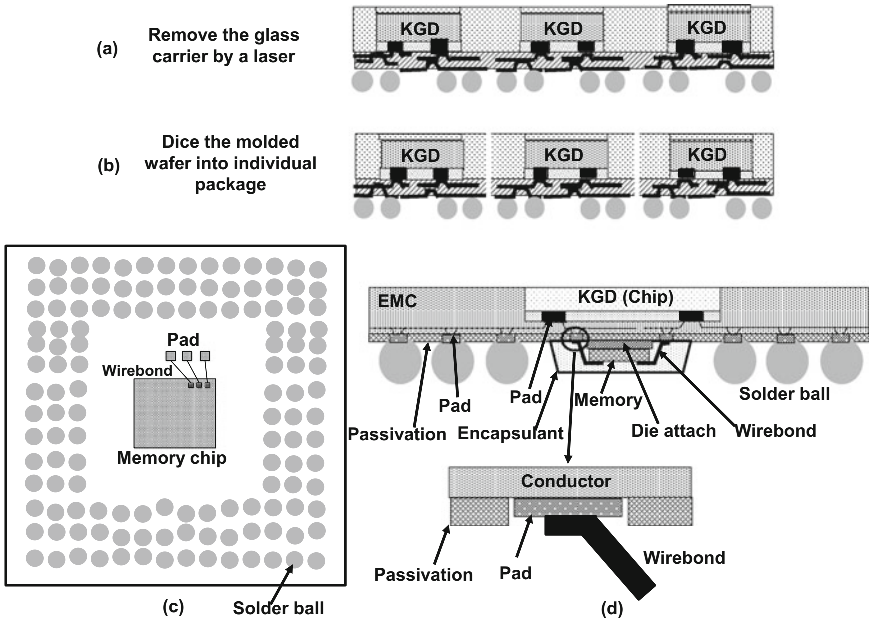


Fig. 11.30 Wire bonding memory chip at the bottom of the individual application processor package

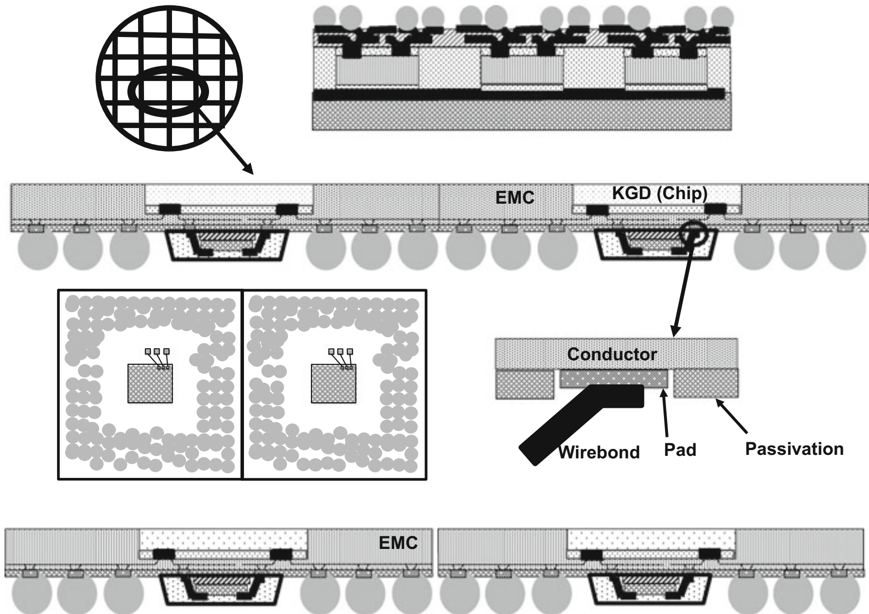


Fig. 11.31 Wire bonding memory chip at the bottom of the application processor package on a wafer

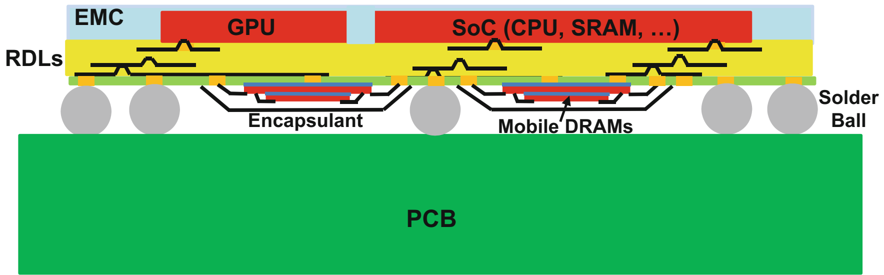
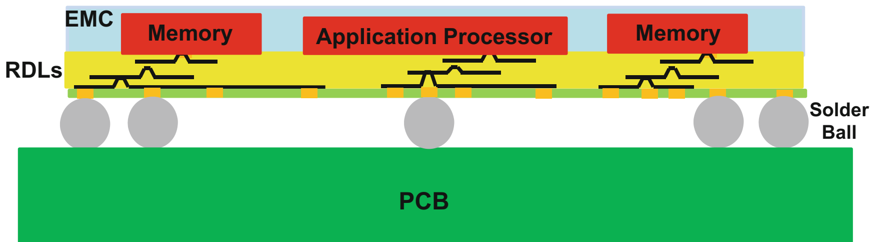


Fig. 11.32 3D IC heterogeneous integration to package the application processor chipset



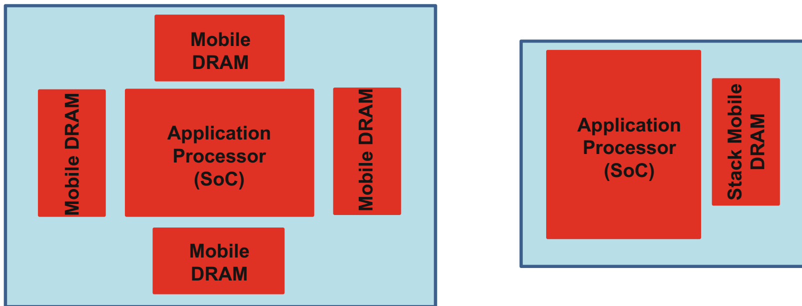


Fig. 11.33 2D/3D IC heterogeneous integration to package the application processor chipset

In [21], we asked the question: "What if there is no PoP for the application processor chipset?" We proposed to place the application processor and the mobile DRAMs side-by-side on a build-up package substrate. The memory chips can be either cross-stacked or individually placed by wire bonding. Also, the memory chips can be placed individually by solder-bumped flip chips. The memory chips can even be stacked and have TSVs. In this study, because we used the FOWLP method to construe the RDLs for the interconnections between the SoC and mobile DRAMs as shown in Fig. 11.33, the build-up package substrate was eliminated.

11.10 3D IC High-Performance Heterogeneous Integration by FOWLP

A high-performance 3D IC heterogeneous integration of CPU, GPU, FPGA, ASIC, HBM, etc., is presented in this section. The emphasis is placed on the manufacturing process.

11.10.1 High-Performance 3D IC Heterogeneous Integration System

Figure 11.34 schematically shows a 3D IC high-performance heterogeneous integration by FOWLP technology. It can be seen that it consists of a GPU, a FPGA (field-programmable grid array), CPU, or a high-performance application-specific integrated circuit (ASIC), and is surrounded by high-bandwidth memory (HBM) cubes. Each HBM cube consists of four DRAMs and a logic base with through-silicon vias (TSVs) [2, 3] straight through them. Each DRAM chip has >500 TSVs. The interconnections between the GPU/FPGA/CPU/ASIC and HBMs are through the RDLs. The major heat path of this structure is from the backside of the GPU/FPGA/CPU/ASIC to the heat spreader. A heat sink can be added on top of the heat spreader if it is necessary.

11.10.2 Manufacturing Process

In this case, the emphasis is placed on the manufacturing method (process) of this structure. This method comprises these steps: (1) testing for KGD of device wafers; (2) sputtering UBM; (3) electroplating the Cu contact pad; (4) spin coating a polymer on top of the device wafers; and (5) painting a thermal interface material (TIM) on the bottom (backside) of the device wafers (Fig. 11.35). The last step is different from the conventional method (the first case) which is laminating a DAF on the bottom of the device wafers.

After the steps outlined above are completed, the following are done: (1) the individual KGDs are picked and placed face-up on a metal such as copper, aluminum, steel, and an alloy 42 (with thermal expansion coefficient = 8 to 10×10^{-6}/°C) carrier about 1 mm thick; (2) molding the EMC on the reconstituted wafer is accomplished by using the compression method and then post mold curing (PMC) of the EMC; (3) backgrinding the EMC and polymer to expose the Cu contact pad; (4) building up the RDLs; and (5) mounting the solder balls. Then, the reconstituted wafer is diced into individual packages (Fig. 11.35). (Note: this process is different from the conventional method, which used a glass carrier and was coated with an LTHC release layer).

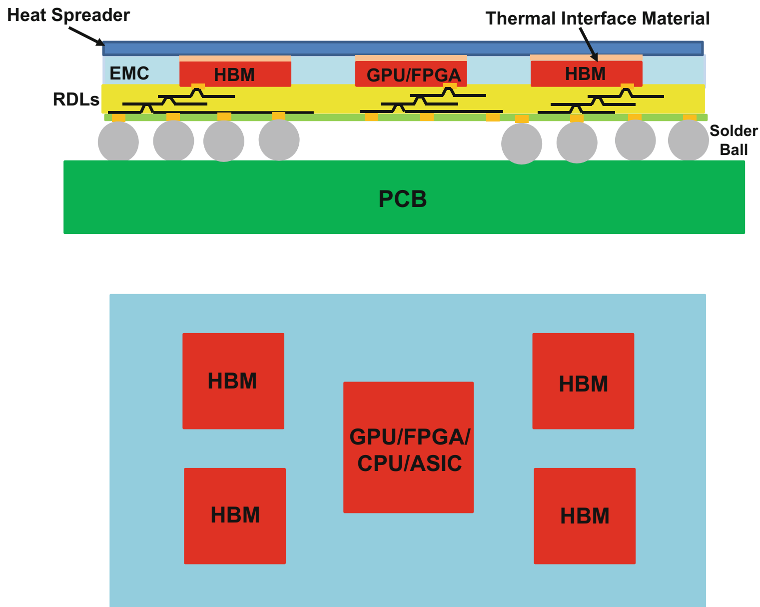


Fig. 11.34 3D IC high-performance heterogeneous integration by FOWLP

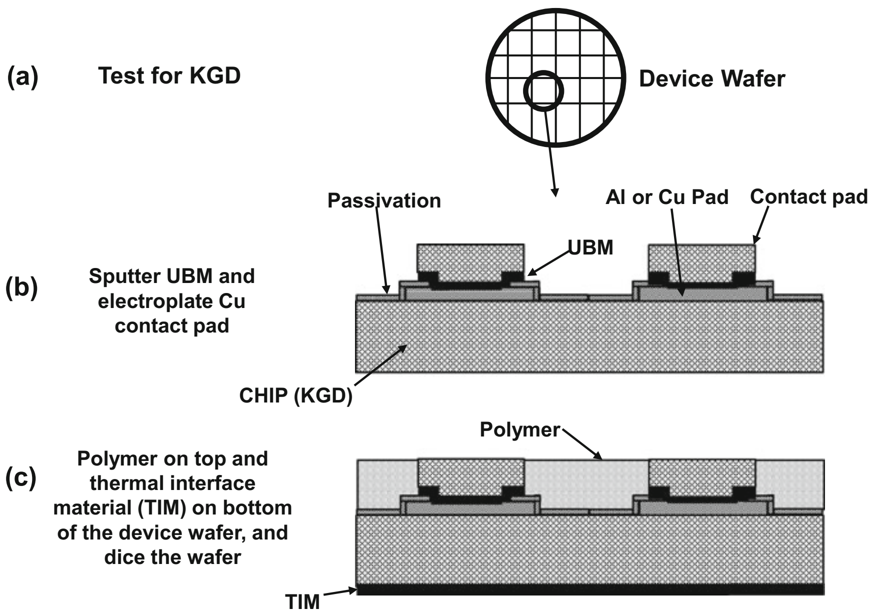


Fig. 11.35 Manufacturing method for 3D IC high-performance heterogeneous integration

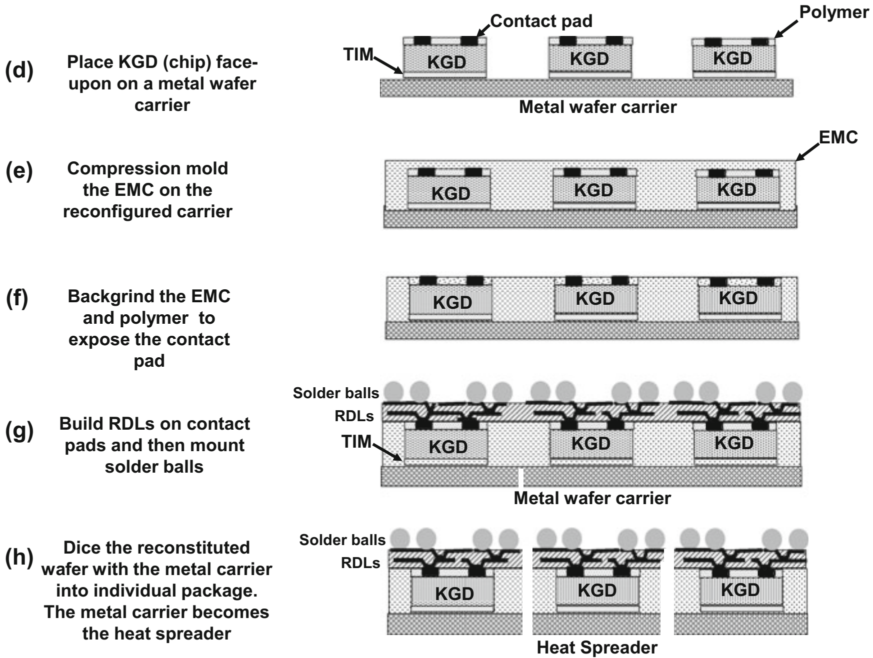


Fig. 11.35 (continued)

11.10.3 Advantages of the New Manufacturing Process

It should be emphasized that unlike the conventional method, there is no debonding of the carrier. The metal carrier becomes the heat spreader of the individual high-performance heterogeneous integration package. This new method of manufacturing high-performance chips and memory cubes in a heterogeneous integration scheme with the FOWLP technology results in fewer assembly steps, lower cost, faster time-to-market, and higher assembly yield. Also, because of the metal carrier, the warpage is reduced during all the process steps. Furthermore, because of the metal carrier, the individual package size can be larger.

11.11 Summary and Recommendations

Two 3D IC heterogeneous integrations by FOWLP technology have been presented. The first 3D IC heterogeneous integration is emphasized on the design and the other 3D IC high-performance heterogeneous integration is on the manufacturing method. Some important results and recommendations are as follows:

- A 3D IC heterogeneous integration of the application processor chipset has been proposed. The interconnections between the application processor and mobile DRAMs are through the RDLs, which are fabricated using the FOWLP method. The manufacturing processes for making the 3D IC heterogeneous integration have also been presented.
- When it is difficult and costly to reduce the feature size to make the SoC, one way is not to integrate some of the functions (for example, the GPU) into the SoC and instead place the GPU chip side-by-side with the SoC.
- The simplest heterogeneous integration of the application processor chipset is to place the application processor and the mobile DRAMs side-by-side on RDLs. One consideration is that the package size could be too large to be reliable. One of the alternatives is to stack up the mobile DRAMs by wire bonding (for lower cost) or TSV (for wider bandwidth.)
- A 3D IC high-performance heterogeneous integration of GPU/FPGA/CPU/ASIC and HBM/HBM2 by FOWLP technology has been proposed. Emphasis is placed on a simple and effective manufacturing method to fabricate the structure. Unlike the conventional method, there is no debonding of the temporary metal carrier. The metal carrier becomes the heat spreader of the individual high-performance heterogeneous integration package.
- The advantages of heterogeneous integration are time-to-market, performance, form factor, power consumption, signal integrity, and cost.
- In order to lower the package profile and enhance the electrical and thermal performance of the application processor chipset for mobile applications such as smartphones and tablets, the current PoP format should be eliminated.
- The recent advances of heterogeneous integrations on organic substrates, silicon wafers, and RDLs have been briefly mentioned.

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