The Improvement of Voltage Reference Below 1 V with Low Temperature Dependence and Resistant to Variations of Power Supply in CMOS Technology

Amirreza Piri

Abstract In this article, the objective is designing a linear voltage reference based on CMOS technology and a structure which is insensitive to variations of temperature and supply power. In such a case, accuracy of circuit output will be optimal under different conditions. Among such sensitivities, one could point to variation of output in relation to temperature, variation due to output performance of the structure and currents, noises and turbulence. First, different voltage references, their structures and advantages and disadvantages will be reviewed individually. Then, output startup method will be explained through bulk transistor and parallel combination of transistors in output for control of output leakage current. This is followed by elaboration of reference building designed based on this method. Consequently, intended structure will designed by taking above-mentioned objectives into account. The circuit simulation and circuit layout will be done through H-Spice Software and Cadence applications respectively. The pre-layout and post-layout results signify improved results and resistance of suggested circuit against substrate noise and noise of power supply. Simulations will be done through 0.18 um CMOS technology.

Keywords Low voltage · Band-gap reference · Low noise · CMOS Voltage reference

1 Introduction

Rapid development of CMOS manufacturing process led to reduced top limit of supply voltage and allowable power consumption in analogue, digital and RF integrated circuits. At the moment, is the most significant challenge of design of Nano-Electronic chips, Further limitation of linear performance area of dynamic

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range and added sensitivity of outputs to noise of power supply are among such challenges. The band gap voltage generator circuit is one of the common circuits the output voltage of which should vary insignificantly with temperature. This is while common band gap circuits are not suitable for low voltage applications due to relatively high output voltage (which increases required supply voltage) and non-linear variation of output with higher orders than a specific temperature (Tn). Therefore, adoption of certain methods should be accompanied by lower supply voltage requirement and minimized dependency of circuit output on sentences with higher orders than T. These problems increase when design of integrated circuits for portable systems is concerned since such systems supply their required energy from weak energy sources such as micro-batteries or energy sources that are available in nature. In order to increase the lifetime of batteries and minimize supply noise, designs of such circuits should be characterized by high-efficiency reference voltage supplies and low occupational and output noise levels. In micro-electronics, these supplies are essential parts of analogue and digital systems. The primary role of these supplies is generating precise and stable voltage against variations of temperature. They also should generate linear voltage for other parts such as operational amplifiers, comparators, analogue to digital convertors and digital to analogue convertors. Since introduction of silicon band gap voltage reference by Widlar in 1970s, who suggested that total bass-emitter voltage with positive temperature coefficient could be generated by a stable voltage reference, these blocks and their combinations have been widely used in bipolar manufacturing processes and CMOS. During previous years, significant efforts were made to improve the performance of a band gap reference. Most of these efforts were targeted at adding to independence of size of output voltage from variation of temperature, power supply and manufacturing process. Designs of these references are intended to reduce number of system batteries, areal of chip and power consumption of the system [1].

In this paper, some of these methods will be introduced and a new method is introduced which uses two temperature independent currents (of first order). The two currents were generated by relatively simple low voltage band gap circuits.

The objective of design of voltage reference circuit is generating a voltage which is independent of power supply, process and temperature. There are different solutions for developing a fixed supply which could be grouped into 3 categories:

1. Use of a Zener diode which breaks down at reverse bias of certain voltage. Major disadvantages of this method is that the method does not generate a continuous value and it cannot be used in CMOS technology. In addition, breakdown voltage of Zener diode is usually higher than the supply used in current circuits [2].
2. Use of difference between threshold voltages of an incremental transistor and a discharge transistor. The disadvantage of this method is that most of CMOS circuits cannot access discharge transistors. In addition, if access to such transistors is enabled determination and stabilization of threshold voltage of transistors are difficult [3].

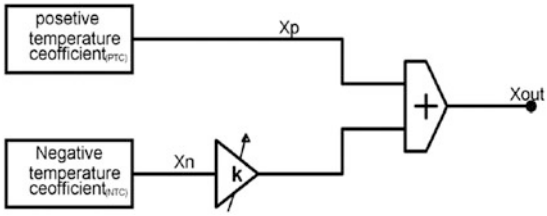

Fig. 1 Generatio of band gap reference voltage with positive and negative temperature coefficient

3. Use of band gap circuits in which current of a PTAT element eliminates thermal dependence. Today, this method is widely used for design of integrated circuits. Usually, a PN bond is used as CTAT element. In this case, diagram of a band gap circuit could be represented in the following manner [4] (Fig. 1).

If two quantities with different temperature coefficients and proper weights are summed, zero temperature coefficients will result. For instance, for two voltages of *V1* and *V2* which change opposite to each other in relation to temperature we select $\propto_1$ and $\propto_2$ in a way that we have:

$$\propto_1 \frac{\partial V_1}{\partial T} + \propto_2 \frac{\partial V_2}{\partial T} = 0 \tag{1}$$

In order to obtain the reference voltage $V_{REF} = \propto_1 V_1 + \propto_2 V_2$ with zero temperature coefficient TC = 0, two voltages with positive and negative temperature coefficients should be obtained. Among different parameters of a transistor made based on semiconductor technologies, bipolar transistors have generable quantities through which negative and positive temperature coefficients could be obtained. Although CMOS parts are candidates for generation of reference, the core of such circuits is made up of bipolar transistors.

Development of voltage references with low volume, low supply voltage, low power and high performance contributed to their extensive use in analogue and mixed mode circuits (e.g. DC–DC convertors, PLI, A/D, and D/A).

Voltage references, temperature independent DC voltage, develop power supply for manufacturing process. Typical voltage references are usually based on band gap voltages which limit minimum supply voltage of the whole circuit. In addition, band gap voltage circuits are impractical without bipolar transistor.

In this case, techniques of body biasing and body effect approximation techniques were used. A critically significant CMOS voltage reference without certain resistance and parts is introduced here. The suggested circuit is completely insensitive to temperature and supply voltage. With at supply voltage of less than 1 V and input current of less than 235 nA, the reference could operate in all temperature ranges. In addition, the circuit is characterized by low output resistance and ability to eliminate variations of power supply and noise.

Linear Matching of Threshold Voltage (V_{TH}) and Thermal Voltage (V_T).

As primary approximation, threshold voltage could be regarded as linearly reducing with temperature [1, 2]. Here, K is coefficient of temperature dependent model.

$$V_{TH} = V_{TH}(T0) - k(T - T0) \tag{2}$$

Since V_{TH} has negative thermal coefficient, equation of output current will be:

$$I_{DS} = \frac{1}{2}\mu C_{ox} K (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \tag{3}$$

If modulation effect of channel length is exclude ($\lambda = 0$), we have:

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_{DS}}{K\mu C_{ox}}} \tag{4}$$

A simple solution for determination of zero thermal coefficient, is generation of current as described in the following. The bias current should be linearly dependent on carrier mobility and it should be a coefficient of reference V_T. In this case, we have:

$$I = a\mu C_{ox} \tag{5}$$

$$V_{GS} = V_{TH} + \alpha V_T \tag{6}$$

Since V_{TH} has negative thermal coefficient and V_T has positive thermal coefficient, a reference voltage with zero thermal coefficient could be generated. This means that reference voltage is independent of temperature.

A reference voltage, generated by linear combination of VTH and VT, could obtained by a current supply and MOSFET diode connection. Figure 2 shows reference voltage at output A.

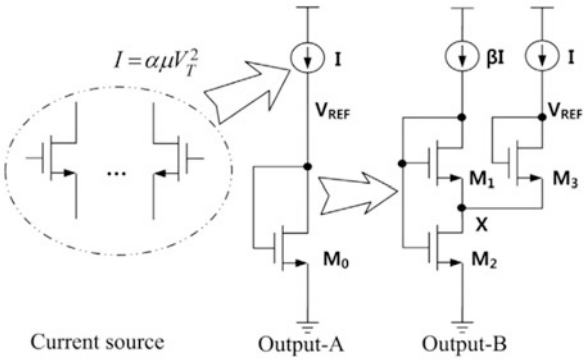

Fig. 2 Schematic representation of suggested reference voltage

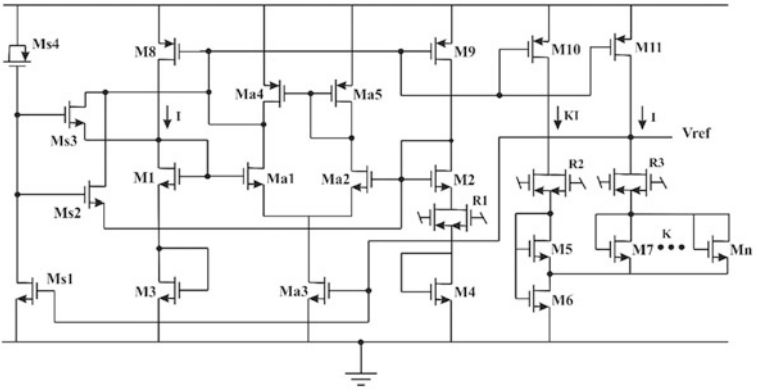

Fig. 3 Schematic representation of suggested circuit

The structure of transistor circuit is represented in the following Fig. 3.

In general, the circuit is made up of three parts: current supply, startup circuit and output each of which will be detailed individually in the following.

- Current Supply

The current supply of the circuit is as shown in the following Fig. 4.

The current supply used to generate current I is the current source connected to output circuit. In this circuit, M8 and M9 are below the threshold and of identical dimensional ratios. The branch made up of M8, M1 and M3 has similar structure to the branch made up of M4, M2 and M9 but M1 and M2 have different dimensional ratios and the same is the case for dimensional ratios of M3 and M4. The design guarantees that M1 and M2 are at saturation zone and M3 and M4 are below bias threshold. This is due to generation of higher current by CMOS transistors when they are in saturation zone. Therefore, bias was located in saturation zone.

A differential input amplifier was used to maintain M1 and M2 at identical gate voltage and to keep drain-source voltage of M8 and M9.

In order to achieve identical bias current, M1 offers higher conductivity as it has larger dimensions. Therefore, negative input of amplifier is connected to B node since M1 has quicker variation of current than voltage variations.

$$V_{GS1} + V_{GS3} = V_{GS2} + V_{GS4} \tag{7}$$

Since length of M1–M2 channel is not sufficiently large, modulation of length of channel was excluded and gate-source voltage was determined through following equation:

$$V_{GS} = V_{TH} + \sqrt{\frac{2I_{DS}}{K\mu C_{ox}}} \tag{8}$$

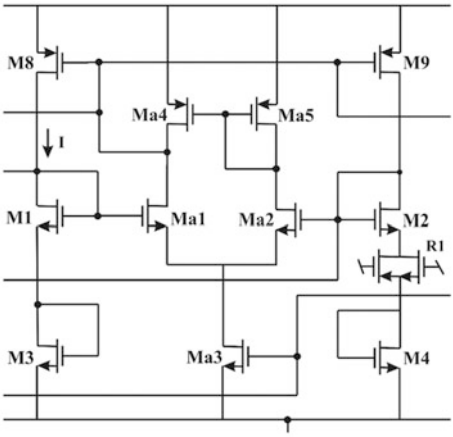

Fig. 4 Current supply of circuit

Supposing that currents of two branches are identical, we have:

$$V_{GS3} + V_{TH1} + (\eta - 1)V_{GS3} + \sqrt{\frac{2I}{\mu C_{ox} K_1}} = V_{GS4} + V_{TH2} + (\eta - 1)V_{GS4} + \sqrt{\frac{2I}{\mu C_{ox} K_2}} \tag{9}$$

Since M3 and M4 are below threshold, currents of these transistors are obtained approximately through following equation:

$$I_{DS} = \mu C_{ox} K (\eta - 1) V_T^2 exp\left(\frac{V_{GS} - V_{TH}}{\eta V_T}\right) \times \left[1 - exp\left(\frac{-V_{DS}}{V_T}\right)\right] \tag{10}$$

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Based on suppositions of design of this part of reference voltages [13, 16], we have:

$$V_{DS} > 4V_T.$$

In this circuit, we have:

$$V_{TH1} = V_{TH2}$$

$$\eta \left[V_{TH3} - V_{TH4} + \eta V_T In \frac{K_4}{K_3}\right] = \sqrt{\frac{21}{\mu C_{ox}}}\left(\sqrt{\frac{1}{K_2}} - \sqrt{\frac{1}{K_1}}\right) \tag{12}$$

$$I = \frac{1}{2}\mu C_{ox}\left[\eta^2 V_T \frac{\sqrt{K_1 K_2}}{\sqrt{K_1}\sqrt{K_2}} In \frac{K_4}{K_3}\right]^2 \tag{13}$$

Above equation could be rewritten in the following manner:

$$I = a\mu C_{ox} V_T^2 \tag{14}$$

$$I = \frac{1}{2}\mu C_{ox}\left[\eta^2 V_T \frac{\sqrt{K_1 K_2}}{\sqrt{K_1}\sqrt{K_2}} In \frac{K_4}{K_3}\right]^2 \tag{15}$$

In regard to current supply, approximate difference or deviation of body effect and approximation of I–V characteristic should be considered. In the suggested circuit, transistors M3 and M4 operate blow threshold zone, namely:

$$V_{SB1,2} = V_{GS3,4} = V_{DS3,4} \tag{16}$$

The output part of the circuit is as shown in the following Fig. 5.

The output circuit used for generating reference voltage with temperature compensation is made up of three branches. In a branch with current source biased by I1 current, identical dimensional ratio (M1 transistor) is identical while second branch is biased by I2.

$$V_{REF} = V_{th}(T0) - K(T - T0) + V_T Ln \frac{(1+\beta)K_5}{\beta(\eta - 1)K_6 K_7} \tag{17}$$

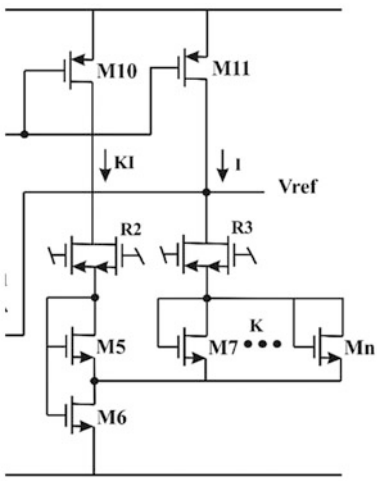

Fig. 5 Output part of circuit

Substituting Eq. 14 into Eq. 16, we have:

$$V_{REF} = V_{th}(T0) - K(T - T0) + V_T Ln\left[\left(\eta^2 \frac{\sqrt{K_1 K_2}}{\sqrt{K_1} - \sqrt{K_2}} In \frac{K_4}{K_3}\right)^2\right]^{1/2} \frac{(1+\beta)K_5}{\beta(\eta-1)K_6 K_7} \tag{18}$$

Since we have $\partial V_{ref}/\partial T = 0$, the following temperature-independent reference voltage output will be obtained:

$$\frac{1}{2}\left(\eta^2 \frac{\sqrt{K_1 K_2}}{\sqrt{K_1} - \sqrt{K_2}} In \frac{K_4}{K_3}\right)^2 \frac{(1+\beta)K_5}{\beta(\eta-1)K_6 K_7} = exp \frac{kp}{\eta k_B} \tag{19}$$

Since TC of reference voltage (V_{REF}) is equal with zero, drain current of M7 (I) at room temperature is determined through following equation:

$$I = \mu C_{ox} V_T^2 \frac{K_6 K_7 \beta(\eta-1)}{K_5(1+\beta)} exp \frac{kT_0}{\eta V_T} \tag{20}$$

The quiescent current of the whole current is determined by current I since currents of other branches is sourced by I. In the case of fixed β, quiescent current represented by I in Eq. 19 deceases by increase of dimensional ratio of M5 and decrease of dimensions of M6, M7. Basically, both circuits of supply source and output are sources of CMOS current. In order to reduce modulation effect of channel length which causes mismatch between currents of branches, lengths of channels of transistors M8–M11 were presumed to be significant.

Startup Circuit:

Reference voltage requires a startup circuit. In this case, transistors MS1–MS4 act as startup circuit (Fig. 6).

Since we have $V_{GS8} = V_{GS9} = V_{GS10} = V_{GS11}$, selection of different W/Ls makes transistors identical or a factor of each other. Because a current is a factor of V_T^2 and transistors M8 and M9 operate blow threshold zone, output currents are a factor of V_T^2 too. Mathematical and manual calculations of sizes of transistors are represented in the following.

Simulation and Results

In this paper, different threshold voltages are used by drawing on body bias techniques and using similar part. In this case, structural steps of certain parts are excluded and variations of previous works were ignored. Therefore, body effect was excluded altogether.

Figure 9 shows dependence of threshold voltage on V_{BS} in room temperature [16]. In this case, SMICA 18 mm technology was used (Fig. 7).

Therefore, V_{TH} has an approximate linear correlation with V_{BS}.

Current Source:

The current source used for current I is current source input to output circuit. In this circuit, M8 and M9 are blow threshold and of identical dimensional ratio.

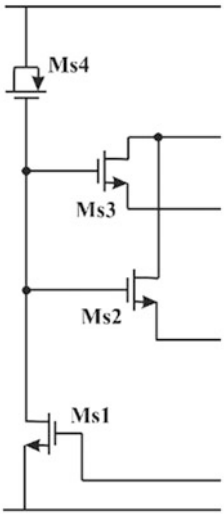

Fig. 6 Startup circuit

The branch made up of M3, M1 and M8 has similar structure to the branch made up of M4, M2 and M9. However, dimensions of M1 and M2 are different and the same is the case for dimensions of M3 and M4. Design should be done carefully so as to guarantee that M1 and M2 are in saturation zone and M3 and M4 are below bias threshold.

A differential input amplifier was used for maintaining M1 and M2 at identical gate voltage and to maintain drain-source voltage of M8 and M9 (i.e. transductor).

In the case of identical bias current, m1 with larger dimension has higher conductivity. Therefore, negative input of amplifier is connected to node B since M1 has quicker current variation than voltage variation. In addition, amplifier improved the performance of PSRR.

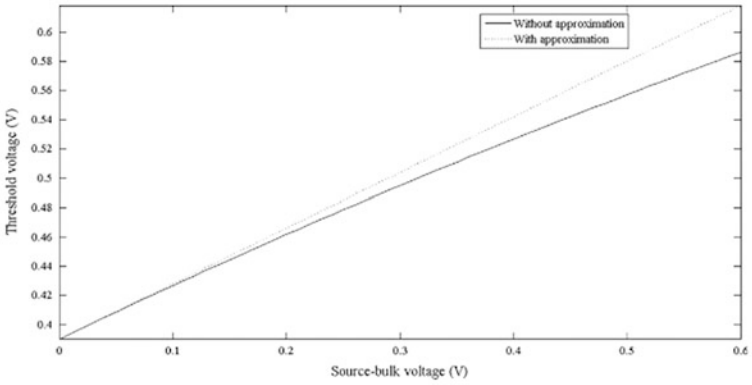

Fig. 7 Dependence of threshold voltage on V_{BS} [16]

Voltage of gate M1–M2 is explained in terms of sum of gate-source voltage of M1 and M3 and sum of gate-source voltage of M2 and M4.

Because of clamp action of amplifier, gate voltages of M1 and M2 are identical. Since lengths of channel M1, M2 is sufficiently large, modulation of length of channel was excluded and gate-source voltage was obtained through its relevant equation.

In regard to current source, approximate difference (deviation) of body effect and approximation of I–V characteristic should be considered. In case of suggested circuit, both transistors M3 and M4 operate below threshold. In this design, $V_{GS4} = 192$ mV and $V_{GS3} = 224$ mV are presumed as they offered better performance.

The output circuit used for generation of reference voltage with temperature compensation is made up of two branches. A branch is biased by current source which is characterized by current I and identical dimensional ratio (transistor M11). This is while second branch is biased at ratio B. Basically, current source circuit and output circuit are sources of CMOS current.

In order to reduce modulation effect of channel length which creates a mismatch between currents of branches, lengths of channels of transistors M8–M11 were opted to be quite significant. Reference voltage requires a startup circuit and transistors MS1–MS6 act as startup circuit.

Variation of Voltage and Output Current per Variations of Supply for 18 um Technology.

In this case, output voltage of supply ranges between 0.85 and 2.5 V and it is equal with 0.6 V which is identical with results of this paper. In order to achieve this result, voltage of supply should be increased from 0 to 2.5 V and the voltage generated by the supply is higher than 0.6 V. The output does not change. Figure 8 represents similar analysis of variation of current. Similarly, when voltage of supply exceeds 0.6 V the current will be fixed at 26 nA (Fig. 9).

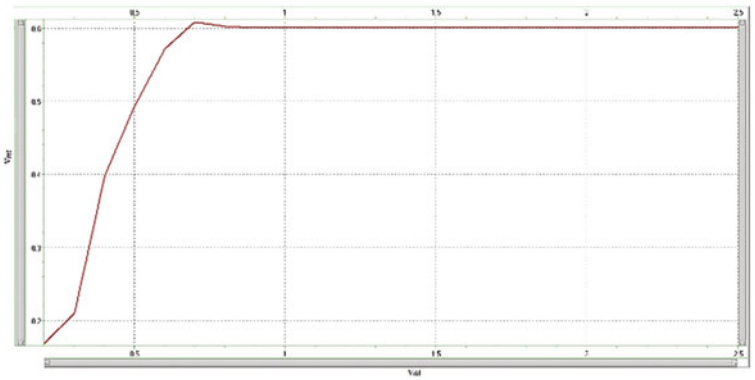

Fig. 8 Variation of output voltage versus variations of supply

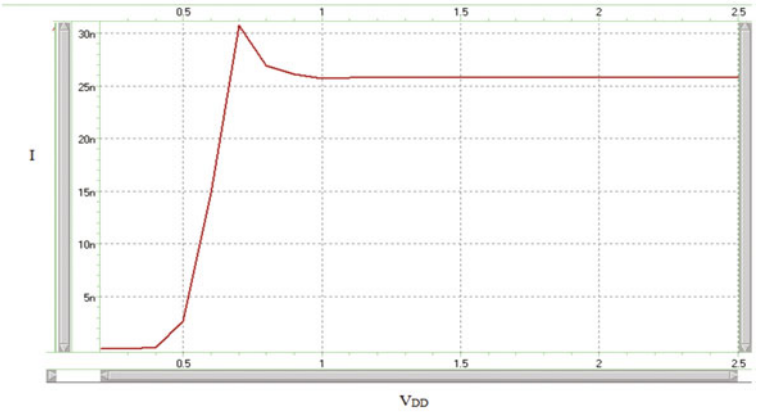

Fig. 9 Variations of current output versus variations of supply voltage

The 0.18 um technology led to 3 mV reduction. The variations are due to increase in voltage range of voltage supply. In the following, analysis of variation of voltage output per variation of supply at 0.5 um scale as well as variation of current output per variation of variation of supply at 0.5 um scale are represented. The results signify proper performance of suggested circuit. The only difference is that in this technology, final and stable solution is obtained when voltage output to the supply exceeds 2.2 V.

The layout of suggested circuit was made through Cadence Software (Fig. 10).

Then, variations of output voltage and output currents at different temperatures ranging from −20 to 100 °C as well as different supply voltages were determined (Fig. 11).

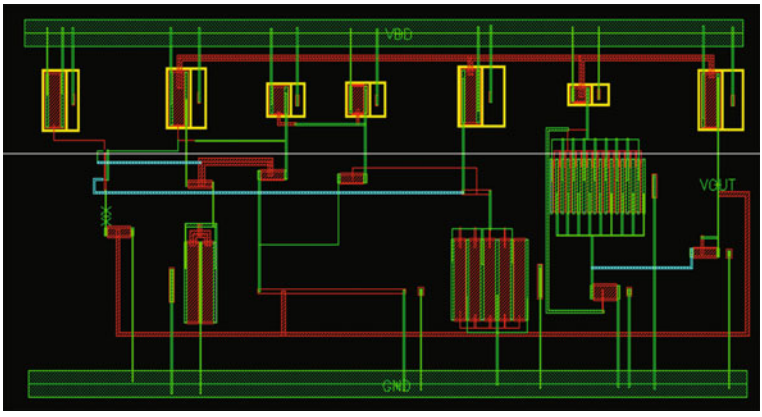

Fig. 10 Schematic representation of circuit

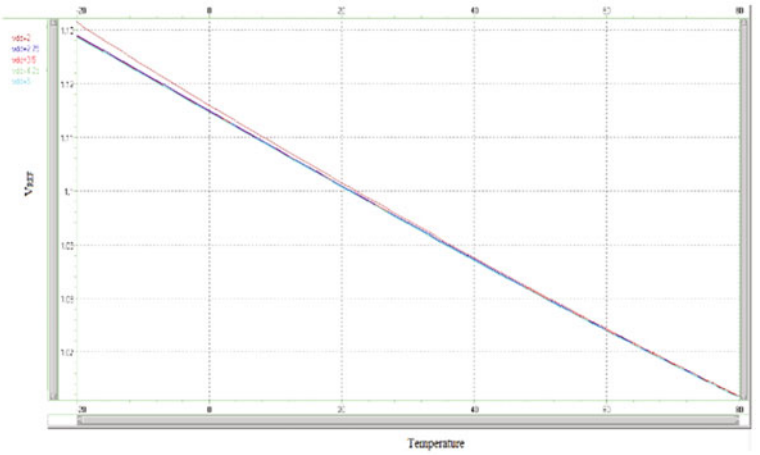

Fig. 11 Variation of output voltage for different temperatures after layout

In this case, variations of output voltage for different temperatures ranging from −20 to 80 °C are represented and they are similar to findings of simulation in H-Spice Software (Fig. 12).

Finally, simulation was done at different corners of the process and obtained results are as shown in the following Fig. 13.

Observably, time to attain steady state is dissimilar for different corners. In SS corner, more time is needed for circuit to attain steady state. The results were obtained after circuit layout (Fig. 14).

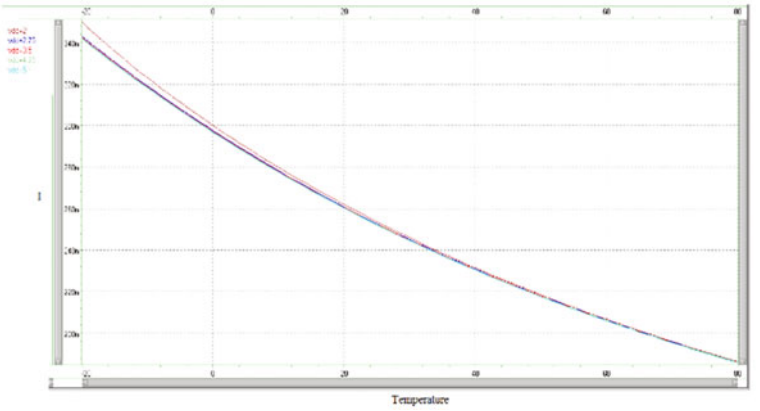

Fig. 12 Variation of output current for different temperatures after layout

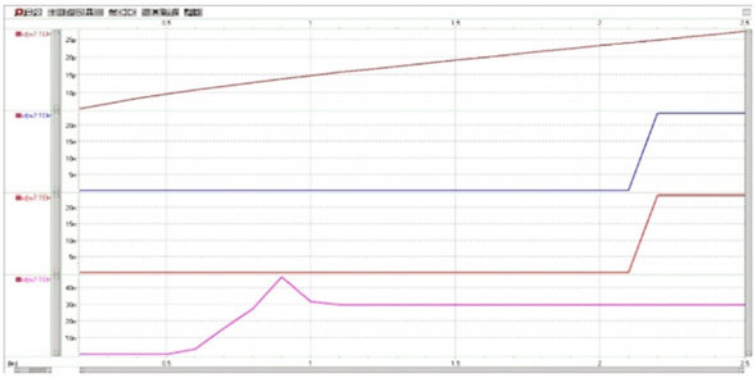

Fig. 13 Variation of output current for different corners after circuit layout

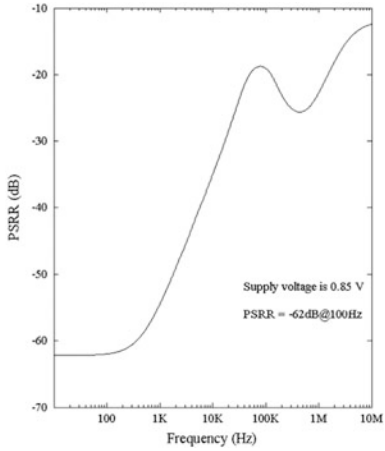

Fig. 14 Calculation of PSRR based on frequency variation (0.85 V)

Maintaining power supply rejection ratio (PSRR) is possible when reference voltage of amplifiers is from a voltage supply in which there are voltage dividers. Usually this issue (i.e. isolation of variation of voltage supply and its noises from reference voltage of amplifiers) is ignored during design of circuits.

This is a significant problem since real voltage supplies of circuits are not quite ideal and any AC signal on supply line could be fed back into the circuit and be amplified. Under logical conditions, this situation may lead to unwanted variation.

This problem is addressed in internal designs of modern op-amps as a parameter called PSRR is included in relevant data sheets which represents power and ranges from −80 to −100 dB. In common op-amps, value of this parameter ranges from −40 to −100 dB and this should be noted in future designs (Fig. 15).

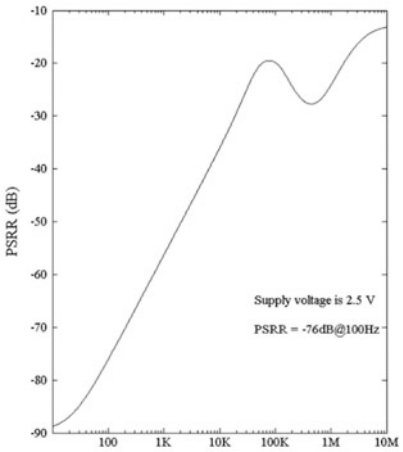

Fig. 15 Calculation of PSRR based on frequency variation (2.5 V)

Observably, PSS for 0.85 V voltage supply is −62 dB at 100 Hz frequency while for 2.5 V voltage supply and similar frequency it is equal with −76 dB. At the end of this chapter, a comparative table is included so as to compare the results with findings of previous studies.

2 Conclusion

Based on the comparison, one could suggest that low technology used to complete this thesis led to coverage of a supply voltage ranging from 0.085 to 2.5 V. In terms of operating voltage range, the results signify improvement in comparison with previous findings. In addition, significant improvement of operating temperature range were made and output current was lower than previous studies. Finally, comparison of circuit layouts with previous works suggest that the circuit occupies less space than integrated circuit (Table 1).

Table 1 Results of comparison between present study and previous studies

Parameter	Reference [4]	Reference [5]	Reference [8]	Reference [9]	This work
Process (μm)	0.35	0.18	0.35	0.13	0.18
Supply voltage	2–3.5	0.45–2	1.4–3	1–2.3	0.085–2.5
Temp (°C)	0–80	0–125	−20 to 80	1–2.3	0.085–2.5
Vref (mV)	800	263.5	747	0–100	−20 to 100
Supply current (μA)	0.4@2 V	0.4@0.45 V	2.1@1.4 V	8.1@1.2 V	0.235@2 V
PSRR (dB)	−51.4 @100 Hz	−45 @100 Hz	−45 @100 Hz	−44 @100 Hz	−62 @100 Hz
Area (mm^2)	0.041	0.043	0.055	0.053	0.023

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