Modeling and Simulation of 1/f Noise During Threshold Switching for Phase Change Memory

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1 Introduction

The ITRS considers phase change memory (PCM) as an existing baseline and prototypical memory technology [1–3]. It is currently most mature of the new memory technologies under research. Development of PCM with high speed, density, nonvolatility, decreased energy consumption, scalability, 3D integration, endurance, retention, and multi-bit operation would initiate a revolution in computer architecture, known as nanostores, which will be the future of information processing. PCM has potential to be a universal memory that works across multiple layers of memory hierarchy.

PCM relies on chalcogenide material typically $Ge_2Sb_2Te_5$ (GST) which features the capability to change from amorphous to polycrystalline phase and vice versa by giving electrical pulses and subsequent joule heating. Figure 1 shows the schematic of a PCM device. It comprises a thin GST film, heater (TiN), top and bottom electrode contacts, and an active GST that undergoes phase transition between high resistance amorphous state (RESET state) and low resistance polycrystalline GST (SET state) when the PCM cell is stimulated thermally. The active region thickness of u_a and the contact area, A, shall be used to study the effect of scaling on threshold switching. The polycrystalline GST surrounds the active GST and it does not change during program. With proper heating applied, Joule heating is induced resulting in current crowding near the heater-active area interface, and hence phase change of the active GST.

In the reset state, PCM exhibits a threshold switching behavior in the I–V characteristics which is a negative differential resistance (NDR) effect beyond threshold voltage, V_T. It defines a boundary between read and write current and voltages which determines the speed for programming the memory cell. It is therefore important to estimate threshold switching and speed for developing PCM memory. Threshold switching corresponds to two distinct electronic states of the amorphous material which are subthreshold state (OFF state) at low current and a high current ON state.

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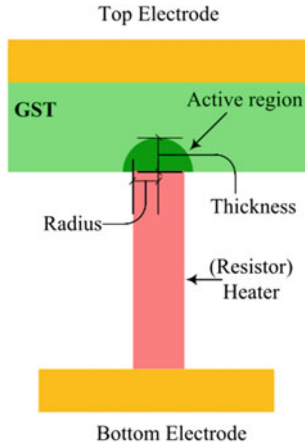

Fig. 1. Structure of a PCM cell

For modeling and design purpose, it is significant to predict the dependence of I–V characteristics on PCM device physical parameters, voltages, and temperature for amorphous chalcogenide during subthreshold conduction and threshold switching. In addition, low-frequency 1/f-like noise is a matter of concern for nanoscaled nonvolatile memory devices, as it produces fluctuations in current which can cause errors during memory readout. Research by Lavizzari et al. has addressed the impact of 1/f fluctuating current during threshold switching by measuring the effect on PCM cell and developed a physical model to account for the statistical delay in the device [4]. A compact model for 1/f noise during threshold switching that can be accounted for simulating PCM array is still missing. In this work, we have developed a compact model for PCM cell in VerilogA of Cadence environment [5] which accounts for subthreshold conduction and threshold switching considering 1/f noise.

2 Modeling and Simulation of 1/F Noise in Threshold Switching

PCM compact model developed in VerilogA is based on analytical model that can address subthreshold conduction, threshold switching, negative differential resistance region, and ON regime. The model constitutes Poole–Frenkel (PF) conduction mechanism in deep traps in the amorphous material [4, 6]. The model was further developed to account for 1/f current fluctuations which can predict delay statistics in PCM. The model developed in VerilogA is implemented in Spectre Circuit Simulator and Virtuoso Analog Design Environment of Cadence. This has a facility of schematic editor for design and simulation of hybrid PCM circuits with CMOS, active and passive devices. Figure 2 shows the schematic implemented in Cadence environment to study the threshold switching during transient simulation. Figure 3 shows I–V curves of a PCM cell in different programmed states benchmarked with that presented by Ielmini

et al. [6]. Reset pulses with different amplitudes equal to 3.2 V, 3.5 V, and 5 V are applied at source V_A for amorphous layer thickness of 18 nm, 27 nm, and 39 nm, respectively, and transient simulation carried out to get the I–V curves. The list of the model parameters used in the simulation is listed in Table 1.

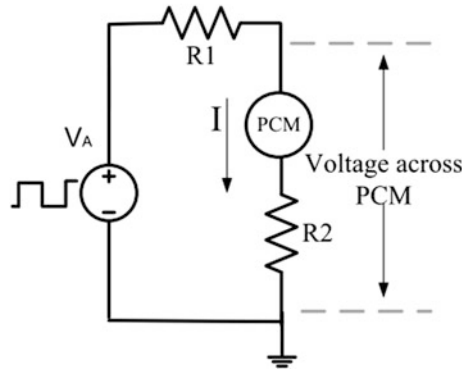

Fig. 2. Schematic for transient simulation of a PCM cell

There is just a little decrease in programmed resistance corresponding to different pulse amplitudes even though the pulse width is reduced to 10 ns. This is because of a delay to achieve a thermal steady state in the heated volume due to large thermal resistivity of the GST film. A RESET pulse of 10 ns and SET pulse of 20 ns are sufficient for a decade change in the resistance of a PCM cell resulting in a sufficient read margin [7]. In addition, reduction in reset pulse width improves PCM cell endurance.

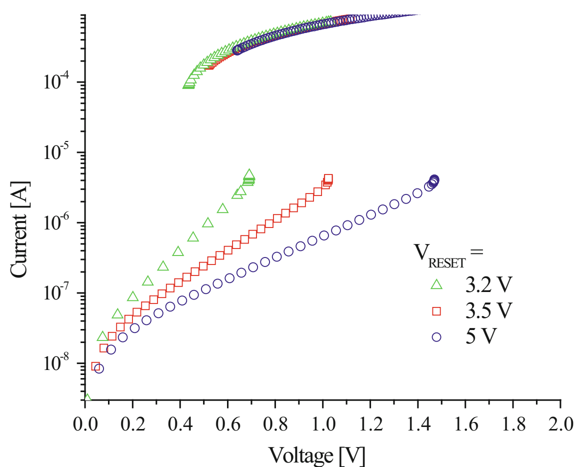

Fig. 3. Simulated I–V characteristics of a PCM cell using the compact model

Table 1. Amorphous chalcogenide physical parameters used in the circuit simulation [6]

PCM device parameters	Values
Elementary charge, q	1.6e–19 C
Average intertrap spacing, Δz	7 nm
Electronic vibration time, τ_0	1e–15 s
Energy distance between equilibrium Fermi level E_F and the conduction band-edge energy E_C, $(E_C - E_F)$	0.36 eV
Boltzmann constant, k_B	8.617e–5 eVK^{-1}
Sample temperature, T	300 K
Concentration of deep states, N_{T1}	1e19 cm^{-3}
Shallow-trap concentration, N_{T2}	1e19 cm^{-3}
Effective time for electron relaxation from shallow to deep traps, τ_n	1e–9 s
Fowler–Nordheim coefficient, B_{12}	1e9 Vm^{-1}
Energy distance between deep-trap energy E_{T1}, and the shallow-trap energy E_{T2}, E_{T2}–E_{T1}	0.29 eV

3 PCM Transient Simulation with 1/f Noise Fluctuations

Transient simulation of the PCM cell considering 1/f noise was carried out as shown in Fig. 4 with applied bias voltage V_A of 800 mV just below V_T for a PCM device thickness of 21 nm and radius of 13.8 nm. As seen in the diagram, 1/f noise can result in statistical variation of the delay time. When the applied voltage is close to V_T, noise fluctuations can lead in current to exceed the threshold voltage which triggers the switching event. This can result in large delay time as shown below. During read operation, threshold switching must not occur else it can disturb the state of the cell. Thus, the delay time can impact the device operation resulting in read disturb and programming errors.

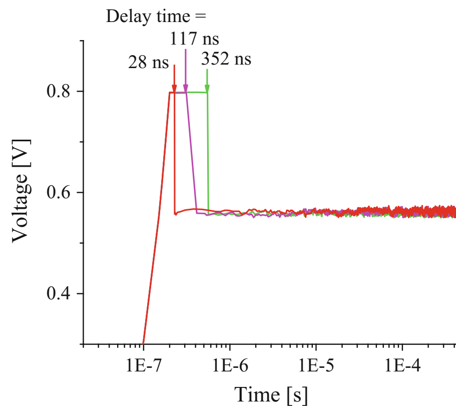

Fig. 4. Simulation result of transient behavior of a PCM device with 1/f noise fluctuations

4 Effect of PCM Device Scaling on Threshold Switching Considering 1/f Noise

The scaling capability is an important virtue of the PCM device as it allows the technology to be scaled for many years. As shown in Fig. 1, the size of the bottom electrode determines the writing current since the heat generated depends on the current density. With reduction in contact size, the current density increases and hence the Joule heating. Thus, a lower reset current can achieve the required temperature. The smaller the active GST material, the less the power will be needed to heat up and hence less programming current. The power dissipated (P) at the GST and heater interface can be given by [7],

$$P = V_h \mathrm{I} + \eta R_{heater} I^2 \tag{1}$$

Here, V_h is the voltage drop inside the chalcogenide, I is the programming current, η is the heater efficiency, and R_{heater} is the heater resistance. Transient simulation

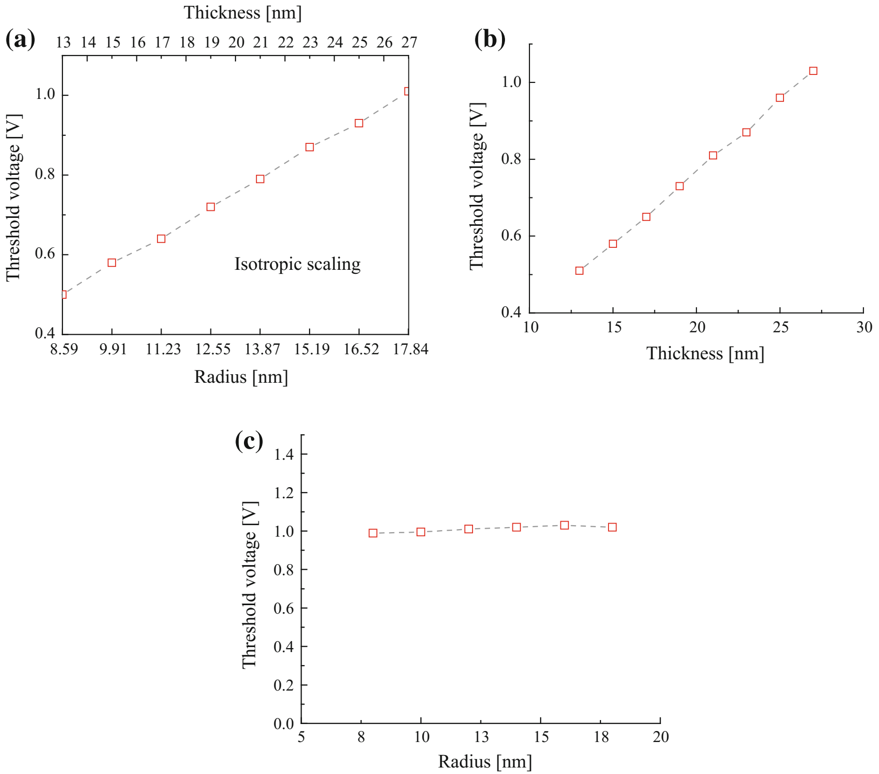

Fig. 5. PCM device simulation result. **a** Threshold voltage dependence on thickness and radius of the amorphous chalcogenide of a PCM device in case of isotropic scaling. **b** Threshold voltage dependence on amorphous chalcogenide layer thickness for a fixed area. **c** Threshold voltage dependence on amorphous chalcogenide layer radius for a fixed thickness

considering 1/f noise is used to study the effect of phase change device scaling on the threshold switching voltage. The PCM device shown in Fig. 1 can be scaled down by shrinking the amorphous chalcogenide layer thickness, its contact area, or both.

Figure 5a shows the plot of V_T versus amorphous chalcogenide layer radius and thickness for an isotropic scaling wherein a constant aspect ratio = thickness/radius = 1.5 initially obtained from thickness = 27 nm for A = 1000 nm^2 is maintained. The graph shows that V_T increases with PCM dimensions in case of isotropic scaling. Figure 5b shows the effect of varying amorphous layer thickness on V_T while keeping its area constant to 1000 nm^2. It can be seen that V_T increases with increase in amorphous chalcogenide layer thickness. Figure 5c shows that V_T remains almost constant in spite of changing contact radius while maintaining a fix thickness (27 nm). This is because, by decreasing the heater thickness, the overall thermal resistance, R_{th} and R_{heater}, increases. The programming current must decrease by the same factor to melt the GST by providing a temperature change of $\Delta T = R_{th}$ P of 630 °C [7]. As a consequence, the overall voltage drop V, across the cell that is equal to $V_h + R_{heater}$ I, remains unchanged. Minor deviation in the graph is because of the 1/f noise.

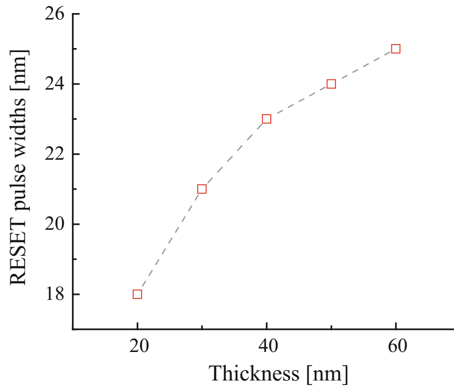

Fig. 6. Effect of amorphous chalcogenide layer thickness on minimum required RESET pulse width

Further, the thickness of the amorphous layer effects the programming speed. By observing minimum RESET pulse width that can induce cell amorphization, it is possible to measure the programming speed of a PCM cell. To study the effect by simulation, we fix the pulse amplitude to 3.5 V with rise and fall time as 1 ns. Figure 6 shows that with increase in thickness of the amorphous chalcogenide the minimum width of the reset pulse also increases.

5 Conclusion

We have simulated a compact VerilogA model of a PCM cell which can predict the subthreshold characteristics and threshold switching. The compact model is developed from a numerical model based on PF conduction and energy gain for the transient simulation of threshold switching. Then, 1/f current fluctuations are added to the PCM model in VerilogA which is able to account for delay statistics and contributes to an insight of the physics during the switching transients.

Simulation results for delay time for an applied voltage just below V_T show a large statistical variation that can result in read disturb and programming errors. In addition, the simulation results for the threshold voltage versus PCM scaling shows that the threshold voltage increases with thickness and remains almost constant with the increase in the area of the amorphous chalcogenide layer. Finally, the simulation result shows that PCM cell with thinner layer has a shorter pulse width for RESET operation and hence low-power consumption.

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