Modeling and Behavioral Simulation of PID-Controlled Phase-Locked Loop

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1 Introduction

The earliest research work towards the phase-locked loop (PLL) goes back to 1932. Because of the number of tuned stages in a superheterodyne receiver, a new type of receiver was developed, called the homodyne. Later on, it was renamed as synchrodyne receiver. In synchrodyne system, a local oscillator tuned the desired input frequency and multiplied it with the input signal. An automatic correction signal is applied to the oscillator, maintaining it in the same phase and frequency as desired. This type of feedback circuit initiated the evolution of the PLL [1, 2]. The basic PLL concepts were published by de Bellescize in 1932 [2–4]. The techniques were mainly used for synchronous reception of radio signals [3]. The PLL is widely used in communication systems. Some of its uses include frequency synthesizer, clock data recovery, FM demodulation, mobile phones, microprocessors, and satellite communications.

In certain applications, such as, in frequency hopping spread spectrum (FHSS) and wireless local area networks (WLANs) which require fast frequency switching methods, the settling time of the PLL is a very important parameter [5, 6]. In this paper, we propose a proportional–integral–derivative (PID)-controlled PLL model by placing a PID control block into the loop for decreasing the settling time.

1.1 Brief Overview of PLL

The PLL is a negative feedback control system which has the ability to align output phase and frequency to the phase and frequency of the reference signal at locked condition. It includes a phase frequency detector (PFD), a loop filter (LF), and a voltage-controlled oscillator (VCO) in the forward path and a frequency divider (FD) in the feedback path as shown in Fig. 1. The PFD is basically a comparator which compares the phase and frequency error between the reference signal and VCO signal. The PFD output is followed by LF to remove any unwanted high-frequency components and generate a dc signal for controlling the VCO. The VCO produces a high-frequency signal which is feedback to the input of the PFD. The FD in the feedback path is usually used to generate a low-noise, high-frequency digitally programmable signal from a low-frequency low-noise crystal oscillator [7]. In free running state of the PLL, there is no input voltage applied to the PFD. In capture range, VCO

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begins to change and produce an output frequency. When output frequency and phase is adjusted to become equal to the frequency and phase of the input signal, then this state is called locked state of the PLL.

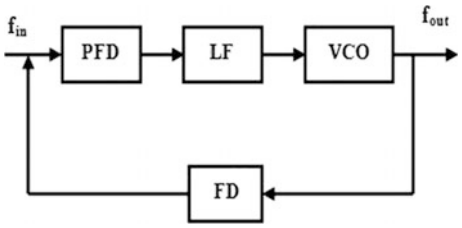

Fig. 1. Different blocks of PLL

2 Related Works

H. U. Uyanik and N. Tarrim in 2007 reported a novel aided-acquisition technique based on PID-controlled PLL where a significant reduction in the settling time is observed from 1.114 μs to 293 ns with an improvement of around 75% [5]. In 2009, V. Minambres, M. I. Milanes, B. Vinagre, and E. Romero designed and analyzed a proportional–integral (PI), a PID, and a novel fractional–proportional–integral (FPI) controller in continuous time domain to solve the phase tracking by improving time response, phase error, and overshoot. Phase margin is obtained to be 32.8°, 26.1°, and 42.9°, and settling time is obtained to be 0.22 s, 0.16 s, and 2.5 s for PI, PID, and FPI controller, respectively [8]. In 2011, P. Karuppanan and K. K. Mahapatra reported a PID controller with PLL synchronization controller based shunt active power filter for compensating harmonic currents and reactive power under both balanced and unbalanced conditions [9]. L. A. dos Santos, M. dos Santos Kaster, and S. A. O. da Silva in 2012 developed an adaptive nonlinear PID controller applied in a single-phase PLL algorithm which provides a transient response of 2.3 times faster than the conventional PI [10]. K. Bora and T. Bezboruah developed and implemented a PID-controlled higher order PLL model with low settling time in the year 2013. They obtained the settling time for second-, third-, and fourth-order PLL with LPF to be 1.49×10^{-5} s, 1.08×10^{-8} s, and 5.4×10^{-9} s, respectively, and for PID-controlled PLL, it is obtained to be 4.4×10^{-9} s [6]. In 2014, S. Golestan, M. Monfared, Francisco D. Freijedo, and Josep M. Guerrero developed a systematic and efficient approach to design the control parameters of the synchronous reference frame PLL (SRF-PLL) with pre-filtering stage [11]. In 2015, S. Golestan, Francisco D. Freijedo, and Josep M. Guerrero presented a systematic approach to design high-order PLLs control parameters for first-, second-, third-, and fourth-order LPF, respectively, and they observed that the reduced-order model provides good accuracy in all the cases [12].

3 Objective and Methodology

The main objective of the proposed work is to design and simulate a PID-controlled PLL. A PID controller is inserted in place of LPF in an attempt to reduce the settling time of the system. The simulation of the proposed model is performed in MATLAB platform to study (i) the stability, (ii) settling time, (iii) phase margin (PM), and (iv) bandwidth (BW) of the system.

The methodologies toward implementation of the proposed work are: (a) derivation of TF in s-domain for each block of the model, (b) derivation of the system transfer function by integrating individual TF of each block of the model, and (c) simulation of the model in MATLAB platform to study the various aspects of the system.

4 Theoretical Estimation for the PLL Components

The block diagram of the proposed model is given in Fig. 2.

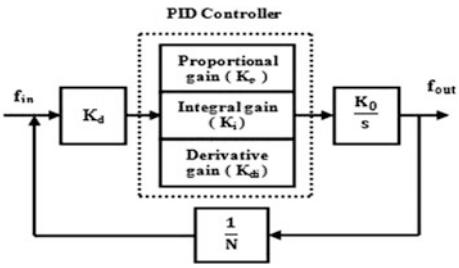

Fig. 2. Functional block diagram of the model

4.1 Estimation for PFD

For linear analysis of the model [2], it is assumed that the loop is locked and the PFD is linear [13]. Then, the PFD output voltage can be written as:

$$V_{PD} = K_d(\phi_{ref} - \phi_{out})$$

$$K_d = \frac{V_{PD}}{(\phi_{ref} - \phi_{out})}, \tag{1}$$

where ϕ_{ref} is the phase of the reference signal, ϕ_{out} is the phase of the VCO output signal, K_d is the PFD gain constant measured in volts/radian, and V_{PD} is the PFD output in volt.

4.2 Estimation for VCO

For linear analysis of the loop [14], the VCO output can be expressed as:

$$\phi_{out} = K_0 \int V_{tune} dt,$$

where K_0 is the VCO gain factor and V_{tune} is the VCO control voltage.

The TF of the VCO can be written as

$$\frac{\phi_{out}}{V_{tune}} = \frac{K_0}{s}, \tag{2}$$

where $K_0 = \frac{1}{CR}$; C and R are the capacitance and resistance used in VCO design.

4.3 Estimation for LF

We have used second- and third-order passive LPF in the loop as shown in Fig. 3a and b.

The TF of the second-order passive LF can be derived as:

$$F_{2nd}(s) = \frac{1 + sT_2}{sA_0(1 + sT_1)}, \tag{3}$$

where $A_0 = C_1 + C_2$, $T_1 = \frac{C_1 C_2 R_2}{C_1 + C_2}$, and $T_2 = C_2 R_2$.

Thus, putting these values in Eq. (3), the TF for second-order LF can be simplified as:

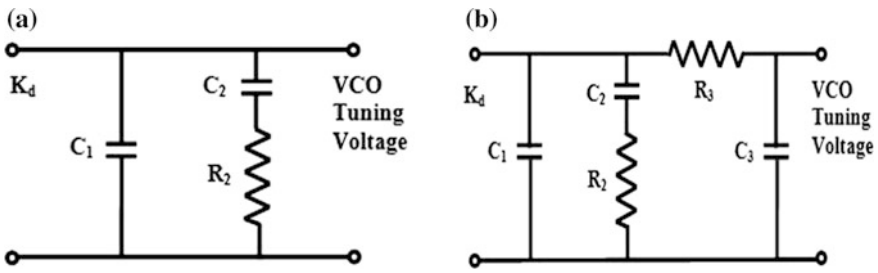

Fig. 3. **a** Second-order passive LPF. **b** Third-order passive LPF

$$F_{2nd}(s) = \frac{1 + sC_2R_2}{s^2C_1C_2R_2 + s(C_1 + C_2)} \tag{4}$$

The TF of the third-order passive LF can be derived as:

$$F_{3rd}(s) = \frac{1 + sT_2}{sA_0(1 + sT_1)(1 + sT_3)}, \tag{5}$$

where $A_0 = C_1 + C_2 + C_3$, $T_1 = \frac{C_1C_2R_2}{C_1 + C_2 + C_3}$, $T_2 = C_2R_2$, and $T_3 = C_3R_3$.

Putting these values in Eq. (5), the TF for third-order LF can be simplified as:

$$F_{3rd}(s) = \frac{1 + sC_2R_2}{s^3C_1C_2C_3R_2R_3 + s^2\{C_1C_2R_2 + C_3C_3R_2 + C_3R_3(C_1 + C_2)\} + s(C_1 + C_2 + C_3)} \tag{6}$$

4.4 Estimation for FD

An FD takes an input signal of a frequency f_{in} and produces an output signal of frequency f_{out}, where $f_{out} = f_{in}/n$; and n is an integer.

The TF for the FD can be derived as:

$$F_{div} = \frac{1}{N}, \tag{7}$$

where N is the division ratio.

4.5 Estimation for PID Controller

The TF of PID controller can be expressed as

$$C(s) = K_p + \frac{K_i}{s} + sK_{di} \tag{8}$$

where K_P is the proportional gain, K_i is the integral gain, and K_{di} is the derivative gain.

4.6 The System TF of the Model

The system TF of the proposed model can be derived as:

$$H(s) = \frac{Forward\ gain}{1 + Loop\ gain} \tag{9}$$

4.6.1 System TF with LF

The forward gain of the model can be expressed as:

$$Forward\ Gain = K_dF(s)\frac{K_0}{s} \tag{10}$$

The loop gain is the product of the individual TF of each block used in the model and it can be derived as:

$$Loop\ Gain = \frac{K_d K_0 F(s)}{Ns} \tag{11}$$

Combining Eqs. (4), (9), (10), and (11), the system TF with second-order LF can be derived as:

$$H_{2nd}(s) = \frac{K_d K_0 (1 + sC_2R_2)}{s^3 C_1 C_2 R_2 + s^2 (C_1 + C_2) + sC_2 R_2 K + K}, \tag{12}$$

where $K = \frac{K_d K_0}{N}$ = loop gain constant [15].

Combining Eqs. (6), (9), (10), and (11), the system TF with third-order LF can be derived as:

$$H_{3rd}(s) = \frac{K_d K_0 (1 + sC_2R_2)}{s^4 C_1 C_2 C_3 R_2 R_3 + s^3 \{C_1 C_2 R_2 + C_3 C_3 R_3 + C_3 R_3 (C_1 + C_2)\} + s^2 (C_1 + C_2 + C_3) + sC_2 R_2 K + K} \tag{13}$$

4.6.2 System TF with PID Controller

Combining Eqs. (8), (9), (10), and (11), the system TF with PID controller can be derived as:

$$H_{pid}(s) = \frac{K_d K_0 \left(s^2 K_{di} + sK_p + K_i\right)}{s^2 \left(\frac{K_d K_0 k_{di}}{N} + 1\right) + s\left(\frac{K_d K_0 K_{di}}{N}\right) + \frac{K_d K_0 K_{di}}{N}} \tag{14}$$

5 Simulations

We simulate the system TF of the model given in Eqs. (12), (13), and (14) in s-domain by using MATLAB to study various aspects of the system. We analyzed the behavior and performance of the model by considering different parameters, namely: (i) K_d, (ii) K_o, (iii) N, (iv) second- and third-order LF components R_2, R_3, C_1, C_2, and C_3, and (v) PID controller gain K_p, K_i, and K_{di}. Various test cases for experiments with second- and third-order LF and also with PID controller are given in Table 1 and Table 2, respectively. The value of capacitor C_2 for second-order LF is chosen at least three times of that of the VCO input capacitance. The capacitor C_3 for third-order LF is chosen at least four times of that of the VCO input capacitance and R_3 is chosen as small as possible.

5.1 Simulation for Settling Time

The step response is used to determine the settling time of the system and provides information about stability. For PLL, settling time is the time for the system output response to reach and stay within 2–5% of its steady-state value. The settling time is set

by the LF components, K_d, K_o, and N. It is directly related to loop BW. The LF BW may be widened to speed up settling time and is also used to optimize PM [15, 16]. We simulate the system TF of the model with second- and third-order LF and with PID controller to evaluate the settling time. Four sample step responses of simulations are given in Fig. 4a, b (Sl No. 2, 4, 12, 15 as highlighted in Table 1) and Fig. 4c (Sl No. 4, 12, 14, 16 as highlighted in Table 2).

Table 1. Second- and third-order LF parameters of the model

Sl No.	Second-order LF parameters			Third-order LF parameters					K_d (V/rad)	K_0 (MHz/V)	N
	C1 (pF)	C2 (pF)	R2 (Ω)	C1 (pF)	C2 (nF)	C3 (pF)	R2 (Ω)	R3 (Ω)			
1	1.000	0.6	0.100	0.100	2.2	0.6	1.00	1.0	0.7	1.00	1.0
2	**0.100**	**0.6**	**0.200**	**0.100**	**1.2**	**1.2**	**1.50**	**1.0**			
3	0.100	2.2	0.200	0.010	2.2	1.5	1.00	1.0			
4	**0.100**	**0.1**	**0.500**	**0.002**	**4.7**	**1.5**	**1.20**	**1.0**			
5	0.500	1.0	0.100	0.001	1.0	2.2	1.20	1.0			
6	0.400	1.2	0.100	0.010	1.0	2.2	1.00	1.0			
7	1.500	1.5	0.100	0.050	6.0	1.2	1.50	1.0			
8	4.700	2.2	0.047	0.010	3.3	1.0	1.00	1.0			
9	3.300	1.5	0.047	0.002	1.0	1.5	1.00	1.0			
10	2.200	1.0	0.100	0.050	2.2	2.2	0.47	1.0			
11	6.000	3.3	0.050	0.100	1.2	1.2	1.00	1.0			
12	**0.600**	**1.0**	**0.150**	**0.002**	**9.0**	**0.9**	**1.00**	**1.0**			
13	1.200	1.5	0.075	1.000	4.7	1.2	1.00	1.0			
14	0.001	4.4	4.700	1.000	6.0	2.2	0.68	1.0			
15	**0.005**	**1.5**	**1.200**	**1.000**	**1.0**	**0.6**	**0.68**	**1.0**			
16	0.001	4.7	0.075	1.000	2.2	0.1	1.00	1.0			
17	0.010	3.3	0.075	1.200	1.0	2.2	0.68	1.0			
18	0.010	1.5	0.050	0.900	1.2	4.7	0.68	1.0			
19	1.200	2.2	0.100	0.900	6.0	1.2	1.00	1.0			
20	1.000	1.2	0.047	0.200	1.2	0.9	1.00	1.0			

Table 2. PID-controlled PLL parameters of the model

Sl No.	K_d (V/rad)	K_o (kHz/V)	N	K_p	K_i	K_{di}
1	0.1	1.00	1.00	0.1×10^{9}	0.1×10^{-9}	0.1×10^{-9}
2	0.1	1.00	2.00	1.5×10^{9}	1.5×10^{-9}	1.5×10^{-9}
3	0.5	1.00	1.00	0.2×10^{9}	1.5×10^{-9}	1.5×10^{-9}
4	**0.7**	**1.00**	**1.50**	$\mathbf{0.3 \times 10^{9}}$	$\mathbf{0.1 \times 10^{-9}}$	$\mathbf{0.5 \times 10^{-9}}$
5	1.0	1.00	5.00	1.0×10^{9}	0.5×10^{-9}	0.5×10^{-9}
6	0.1	0.10	2.00	2.5×10^{9}	0.1×10^{-9}	0.6×10^{-9}
7	0.1	0.50	4.00	0.1×10^{9}	0.1×10^{-10}	0.9×10^{-9}

(*continued*)

Table 2. (*continued*)

Sl No.	K_d (V/rad)	K_o (kHz/V)	N	K_p	K_i	K_{di}
8	1.0	0.50	1.00	0.6×10^{9}	2.2×10^{-9}	1×10^{-10}
9	0.1	1.00	10.00	3.3×10^{9}	2.2×10^{-9}	1.5×10^{-9}
10	0.1	1.00	5.00	6.6×10^{9}	1.5×10^{-10}	1×10^{-10}
11	0.9	0.10	2.00	1.5×10^{10}	3.3×10^{-10}	2.5×10^{-10}
12	**0.7**	**1.00**	**5.00**	$\mathbf{1.5 \times 10^{9}}$	$\mathbf{6.6 \times 10^{-10}}$	$\mathbf{3.3 \times 10^{-10}}$
13	0.7	0.40	5.00	2.2×10^{9}	0.12×10^{-9}	1.2×10^{-9}
14	**0.1**	**1.00**	**1.00**	$\mathbf{5.0 \times 10^{9}}$	$\mathbf{0.09 \times 10^{-9}}$	$\mathbf{1.0 \times 10^{-9}}$
15	0.2	2.50	1.00	1.2×10^{9}	0.7×10^{-9}	0.8×10^{-9}
16	**0.1**	**1.00**	**4.00**	$\mathbf{1.1 \times 10^{9}}$	$\mathbf{1.5 \times 10^{-10}}$	$\mathbf{1.5 \times 10^{-10}}$
17	0.2	10.00	9.0	0.5×10^{9}	1.5×10^{-10}	1×10^{-10}
18	0.1	1.00	5.00	6.0×10^{9}	0.09×10^{-9}	9×10^{-9}
19	0.1	0.20	1.00	1.2×10^{10}	0.1×10^{-10}	1×10^{-10}
20	0.1	1.25	1.00	1.5×10^{9}	0.6×10^{-9}	0.8×10^{-9}

5.2 Simulation for PM and System BW

Bode plot is a useful tool that directly gives the relative stability in terms of PM and gain margin. The PM is equal to 180° plus the phase shift of the TF in an open-loop condition [2, 16]. System stability is related to PM and a system is considered to be stable if the PM value is positive [13, 15]. In PLL system, the loop BW is the frequency at which the magnitude of the open-loop TF is equal to 1. The choice of loop BW typically involves a trade-off between spur level and lock time [15]. We simulate the TF of the model for PM and loop BW by using Bode function. Few sample bode responses are shown in Fig. 5a, b (Sl No. 2, 4, 12, 15 as highlighted in Table 1) and Fig. 5c (Sl No. 4, 12, 14, 16 as highlighted in Table 2).

6 Results and Discussion

The results obtained from the simulated responses for various test cases of the model with second- and third-order LF and PID-controlled PLL for different response parameters are given in Table 3. It shows that the settling time for PLL with second- and third-order LF is in the range from 0.103 ns to 31.8 ns and 0.109 ns to 7.68 ns, respectively, whereas the PLL with the PID controller in the loop shows a settling time ranging from 0.062 ps to 31.3 ps. However, the minimum PM for PLL with second- and third-order LF is 40.9° and 42.6°, where as the maximum comes out to be 76.9° and 71.7°, respectively. For PID-controlled PLL, the minimum PM is observed to be 90.1° and the maximum to be 90.6°. With the change in the settling time, the three systems show a different BW which varies within the range of 119.87 MHz to 6141.4 MHz for the PLL with second-order LF. The PLL with third-order LF and the PLL with PID controller shows a variation from 56.441 MHz to 192.75 MHz and 19.846 GHz to 9923.62 GHz, respectively.

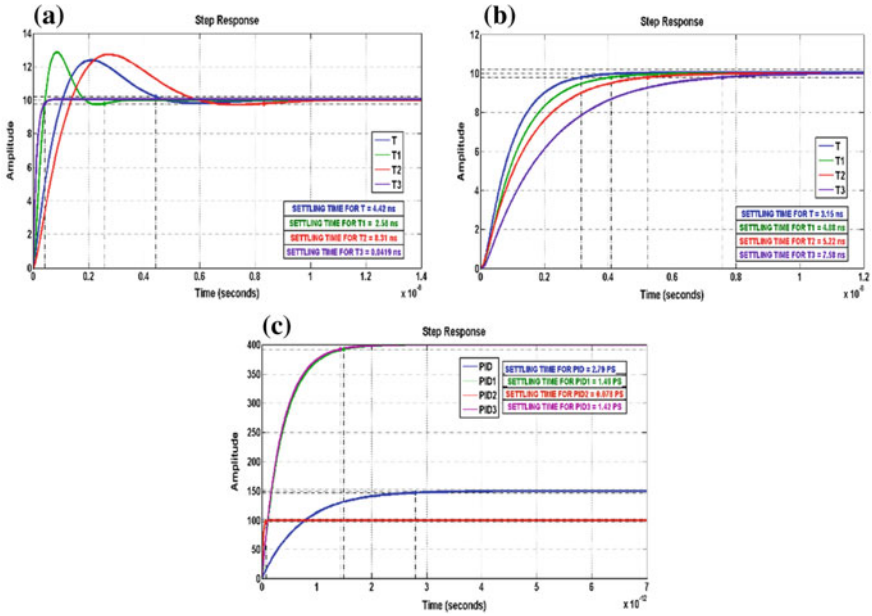

Fig. 4. **a** Step responses of the simulated second-order LF model. **b** Step responses of the simulated third-order LF model. **c** Step responses of the simulated PID controller model

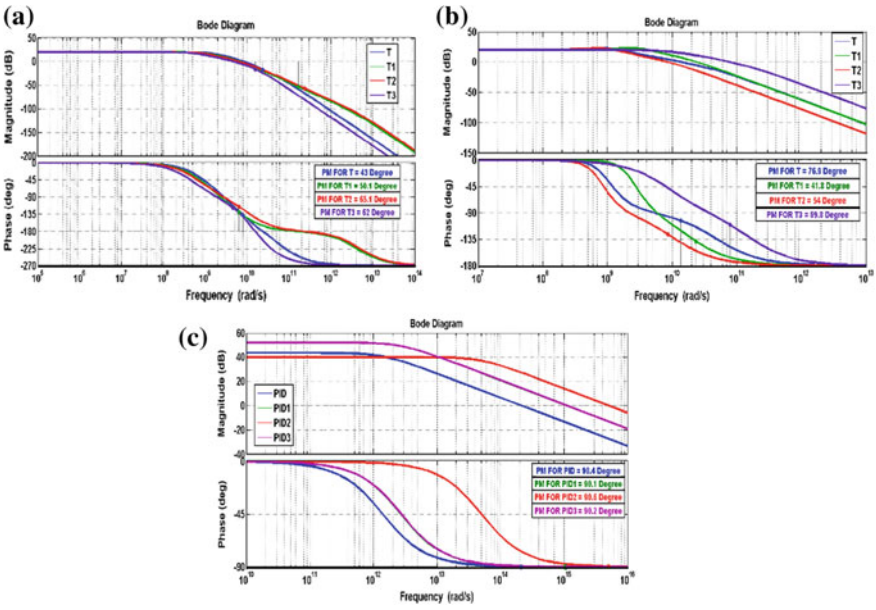

Fig. 5. **a** Bode responses of the simulated second-order LF model. **b** Bode responses of the simulated third-order LF model. **c** Bode responses of the simulated PID controller model

Table 3. Simulation results for second- and third-order LF and PID-controlled PLL model

Sl No.	PM (Degree)			Settling time			BW		
	Second-order LF	Third-order LF	PID-controlled model	Second-order LF (ns)	Third-order LF (ns)	PID-controlled model (ps)	Second-order LF (MHz)	Third-order LF (MHz)	PID-controlled model (GHz)
1	51.6	69.3	90.6	13.3	5.05	3.910	272.71	117.31	158.77
2	**76.9**	0.43	90.3	4.49	3.15	5.220	345.30	**192.75**	119.08
3	71.2	53.8	90.6	5.86	4.82	0.391	485.54	123.94	1587.7
4	41.8	62.6	90.4	2.58	5.06	2.790	887.51	119.68	222.29
5	0.69	**42.6**	90.1	12.2	3.64	0.196	231.14	159.10	3175.6
6	73.6	45.7	90.3	0.10	4.77	3.130	216.41	130.53	198.46
7	50.5	46.4	90.1	11.2	3.27	**31.30**	200.88	191.84	**19.846**
8	0.48	50.1	90.6	**31.8**	4.08	1.560	137.32	151.93	4763.34
9	47.8	0.54	90.1	31.6	5.04	0.130	161.68	123.97	52.39
10	**40.9**	65.1	**90.1**	15.9	5.22	2.960	220.71	118.66	209.59
11	46.9	55.2	90.3	30.1	5.12	5.800	**119.87**	122.25	107.17
12	0.54	61.8	90.1	8.31	**0.109**	1.860	269.71	**56.441**	333.42
13	62.5	0.62	90.1	15.7	7.58	3.180	183.85	80.742	195.61
14	45.9	**71.7**	**90.6**	**0.103**	7.54	0.078	**6141.4**	79.348	7938.80
15	69.8	58.3	90.6	0.419	5.08	0.652	1413.0	120.92	952.66
16	0.70	59.1	90.2	13.7	4.92	1.420	311.43	121.07	436.64
17	62.6	68.7	90.6	13.6	7.65	0.352	367.77	79.742	1764.23
18	0.76	66.5	90.2	0.20	**7.68**	0.326	176.66	79.897	1905.40
19	56.4	60.5	90.6	12.4	5.14	0.163	180.78	119.93	3810.64
20	59.3	57.5	90.1	26.5	5.18	**0.062**	188.78	120.47	**9923.62**

7 Conclusion

From the analysis of the proposed PID-controlled PLL model and PLL with second- and third-order LF, we can conclude that the settling time of PID-controlled PLL is too much faster (0.062 ps) than that of the PLL with LF (0.103 ns for second-order LF and 0.109 ns for third-order LF). Bode responses for PM of the model show that the PM values for both the cases of PLL with LF and PID-controlled PLL are well within the limit of stability. Also, it is observed that the PID-controlled PLL system is highly stable. So, the model may be applied as a trade-off for research and industrial applications for acquiring better settling time in communication system.

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