A 50 MHz–4 GHz Low-Noise Amplifier for Wideband Applications

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1 Introduction

Wideband technology has attracted many researchers because a wide range of future and modern communication system has been proposed that operates over a bandwidth of several gigahertz such as cognitive radio, software defined radio, etc. Wideband systems are capable of transmitting data over a wide spectrum of frequency bands with very low power and high data rates up to gigabits per second. The broadband behavior of wideband transceivers is mainly determined by the low-noise amplifiers. Low-noise amplifier has significant impact on the overall performance of the receivers as they are the first block of the receiver. Therefore, to achieve good performance parameters like ultrawide bandwidth with reasonable noise figure (NF) and good input (close to 50 Ω) and output impedance matching across the bandwidth of interest, it poses a more stringent requirement on the LNA.

Trade-off between voltage headroom, noise figure, bandwidth, and linearity has been done for optimal low-noise amplifier design. Several topologies for wideband low-noise amplifiers exit in literature such as common gate amplifiers, negative feedback amplifiers, distributed amplifiers [1–7], and inductive source degeneration amplifiers. The topology used for a particular application begins with requirements of input matching. Most of the existing wideband LNAs are operated at high frequencies only. The proposed design operates at both high frequency and low frequency so it can be used for wideband applications and also for cognitive radio that operates in the frequency range of 50 MHz–10 GHz.

In this paper, a low-noise amplifier is designed based on cascode structure. The paper is organized in the following manner: In Sect. 2, wideband input matching techniques are described. Section 3 provides concept of proposed circuit. Section 4 discusses the simulation results. In the end, Sect. 5 presents the conclusion.

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2 LNA Topologies

There are several topologies to design a wideband LNA and the choice of topology begins with the input matching requirements, and thus the first task of LNA design is to create 50 Ω resistive input impedance. The noise figure of LNA (about 2–3 dB of overall noise figure of a typical receiver) directly adds to the receiver, and thus the LNA should be designed in a way that it adds minimum noise in the input signal path. The input matching topologies used for LNAs have several forms such as inductively degenerated common source (CS) stage, gain stage with resistive feedback, common gate (CG) stage, and combination of CS and CG stages [8, 9]. Figures 1 and 2 shown below are inductively degenerated common source stage and common gate stage, respectively. The CS LNA has superior noise performance because inductive degeneration is ideally noiseless and the RF input signal is pre-amplified by the input matching series resonant network, whereas the CG LNA uses a parallel resonant network to match the input impedance at resonance ($\frac{1}{g_m}$) to 50 Ω [9]. Also, CG LNA provides a wideband input match that is less sensitive to the input parasitic capacitances.

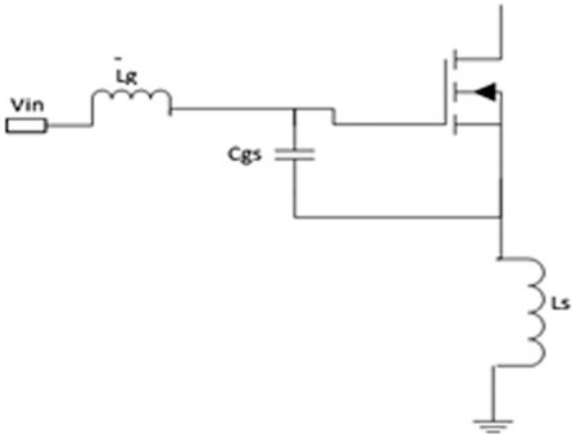

Fig. 1. Inductively degenerated common source

The inductive source degeneration topology provides perfect matching without adding noise and without imposing any restriction on the transconductance [10]. To obtain the perfect matching, two inductors L_s and L_g are used as shown in Fig. 1. The circuit proposed in the paper is designed using inductive degeneration. Figure 3 shows the small signal equivalent circuit of the inductively degenerated CS stage.

Since for a low-noise amplifier the input impedance is an important parameter and is set to be 50 Ω, we will find the expression for input impedance. The input impedance of the circuit shown in Fig. 3 is capacitive and is given by

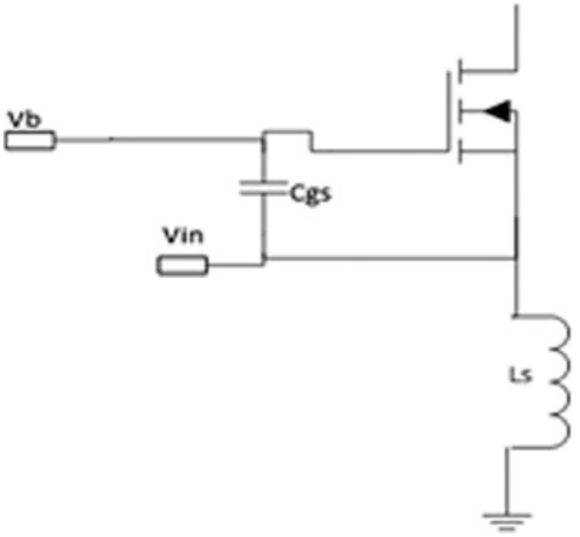

Fig. 2. Common gate stage

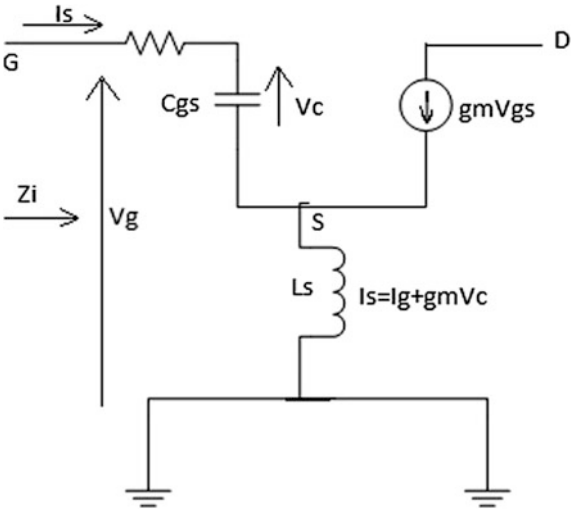

Fig. 3. Small signal equivalent circuit of inductively degenerated CS stage

$$Z_i = \frac{V_g}{I_g} = \frac{\left(I_g R_g + V_c + j\omega I_s L_s\right)}{I_g}, \tag{1}$$

where

$$V_c = \frac{I_g}{sC_{gs}}, I_s = I_g + g_m V_c \tag{2}$$

Using (2) in (1), we get

$$Z_i = \frac{I_g R_g + \frac{I_g}{sC_{gs}} + s\left(I_g + g_m \frac{I_g}{sC_{gs}}\right) L_s}{I_g} \tag{3}$$

Putting s = jω and on solving (3) we get

$$Z_i = R_g + \frac{L_s g_m}{C_{gs}} + j\left(\omega L_s - \frac{1}{\omega C_{gs}}\right) \tag{4}$$

For MOSFET, value of R_g is chosen as zero. Hence, the input impedance has only two components. For a low-noise amplifier, the input impedance should be resistive; hence, another inductance L_g is added to the gate terminal so that the capacitive effect is canceled out at resonant frequency, i.e.,

$$j\left(\omega L_s - \frac{1}{\omega C_{gs}}\right) = 0 \tag{5}$$

3 Proposed Circuit

The proposed circuit using cascode inductive source degeneration topology is shown in Fig. 4.

In this, M1 and L_s form a CS inductive degeneration amplifier which is the input stage of cascode circuit driven by the input signal source V_{in}. This input stage drives the M2 transistor act as common gate amplifier with output signal V_{out}. M2 reduces the Miller feedback capacitance C_{gd} of M1 by providing low input impedance to M2, thereby reducing voltage gain of M1. Thus, by introducing M2, isolation and low-frequency gain improve. However, the gain, linearity, and noise figure at high frequency degrade due to the parasitic capacitances of M2. To overcome these degradations, inductor L_D is used in between M1 and M2. L_D partially cancels the parasitic capacitance at the source of cascode transistor M2. The noise contributed by LD remains less than that of M1 even at relatively high frequencies. M3 and L2 are used to bias the transistor M1. R_D is the load impedance of M2.

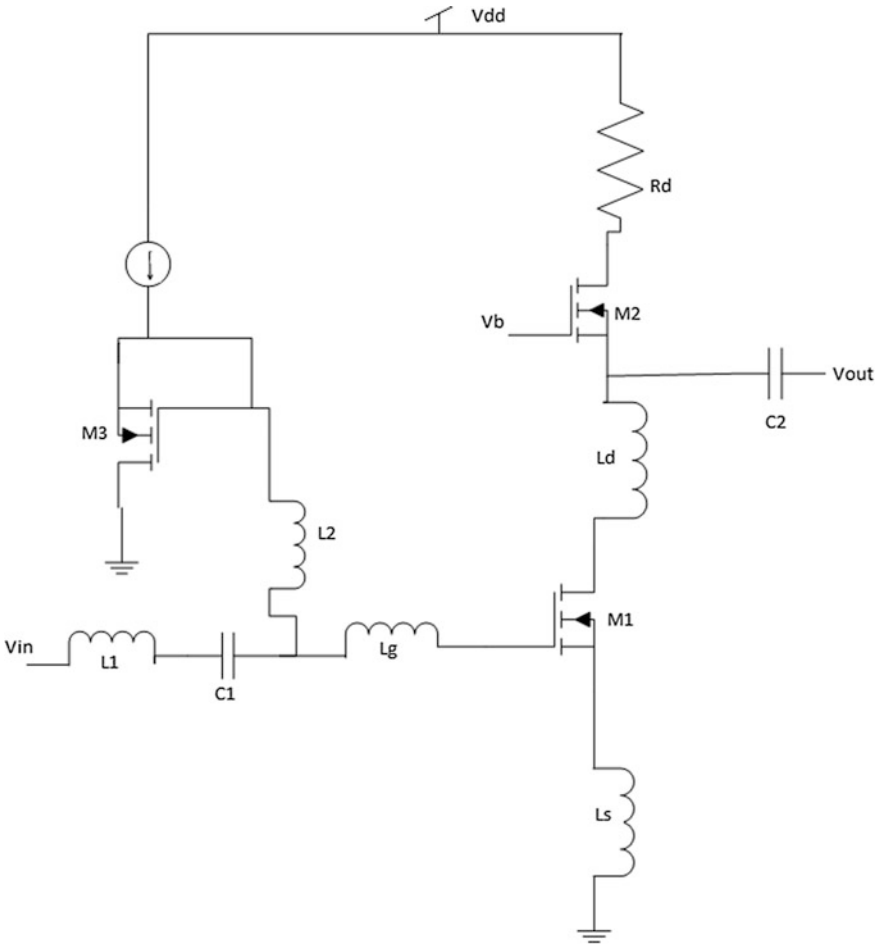

Fig. 4. Proposed LNA

4 Simulation Results

The proposed circuit is designed using 180 nm CMOS technology and simulations were carried out using EldoRF tool. The proposed circuit consumes 10.2 mW power from 1.8 V supply.

Figure 5a shows that the input return loss S11 is less than −10 dB over all the bandwidth. Figure 5b shows the gain versus the power curve where power ranges from −20 to 10 dB. The noise figure of the circuit is shown in Fig. 5c which lies between 2.45 and 2.62 dB. The noise figure of the proposed circuit is close to the desired noise figure of 2.5 dB. Figure 5d illustrates the third-order intercept point which is less than −14 dBm. The performance of the proposed LNA and comparison with the existing circuits are summarized in Table 1.

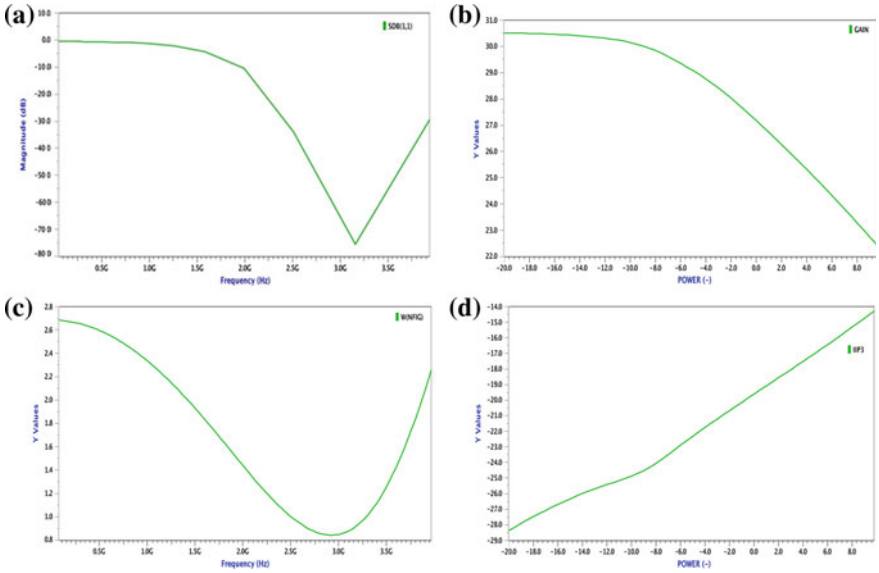

Fig. 5. **a** Input return loss (S11). **b** Gain versus power. **c** Noise figure. **d** IIP3 versus power

Table 1. Performance summary and comparison with different wideband LNAs

References	Frequency (GHz)	Gain (dB)	NF (dB)	IIP3 (dBm)	Power consumption (mW)	Process technology (nm)	Supply (V)
Hidayov et al.[1]	0.7–2.7	17	2.5	1.5	13.5	180	1.8
Guo et al. [2]	0.1–2	17.5	2.9–3.5	10.6–14.3	9.7	180	2.2
Liao et al. [3]	0.5–3.5	17–22	2.68	–	32.8	180	1.8
Ma et al. [4]	0.1–1.45	16.9	2.5	5.5	9.3	180	1.8
Ito et al. [5]	0.8–1.8	13.4	2.7	−7	6.5	180	1.8
Wang et al. [6]	0.47–3	13.6	2.5	−3.5	27	180	1.8
This Work	0.05–4	22.2	2.64	−14.2	10.02	180	1.8

5 Conclusions

Table 1 above helps to draw a conclusion that the present work offers better gain (22.2 dB) as compared to existing works, and also the power consumption (10.02 mW) and noise figure (2.64 dB) are competitive to the existing works. Further, these improvements occur for a wider frequency band (0.05–4 GHz).

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