

# A Radiation-Immune Low-Jitter High-Frequency PLL for SerDes

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**Abstract.** A radiation-tolerant phase-locked loop (PLL) is designed in 65 nm CMOS technology. A double feedback loop self-sampling structure is proposed to improve the anti-radiation capability. A High matched current-based charge pump is hardened by using sensitive nodes compression and transformation technology. The simulation results show that the proposed PLL has no significant variations under heavy-ion and it could output good jitter signals with high frequency.

**Keywords:** PLL · Radiation-Harden · Low-Noise · High frequency  
Double loop · Self-Sampling

## 1 Introduction

The performance of aerospace chip is improving rapidly. To meet the demand of high data rates transmission, SerDes (SERializer-DESerializer) is widely used. Increasing the communication data rates lead a more stringent specification the PLL clock jitter in terms of both random Gaussian jitter and deterministic jitter [1].

Previous studies have demonstrated that PLLs are vulnerable to single-event transients (SETs), resulting in missing pulses and phase displacement [2]. Due to single-event effects (SEEs), high energy particle will pass through semiconductor materials and deposit charge in sensitive devices. It is challenging to design high-performance phase-locked loops (PLLs) for space applications.

The traditional harden technology is unsuitable for PLL in SerDes. Because the existing technology in radiation-hardened PLL is based on the trade-off between anti-radiation ability and performance(jitter and frequency). The charge pump (CP) was identified as the most sensitive module. A voltage-based charge pump was proposed to significantly improve the single-event tolerance with considerable noise degradation [3]. Besides, the voltage-controlled oscillator (VCO) was studied to present increased susceptibility to single-event upsets (SEUs) in advanced technology nodes [4]. Triple modular redundancy (TMR) technique has been commonly utilized in the VCO circuit and frequency divider [5] to eliminate soft errors, but with great area and frequency penalties

In this paper, a radiation-immune PLL is proposed to improve the anti-radiation ability without degradation of jitter and frequency performance. In Sect. 2, PLL radiation hardening by process in 65 nm process is discussed. In Sect. 3, the novel

double loop feedback self-sampling structure is proposed to remove the SET effect of divider and PFD. Current-based charge pump with sensitivity node transformation technology is proposed to improve the jitter performance of PLL. In Sect. 4, layout design and simulation analysis are discussed. In Sect. 5, conclusion is given.

## 2 Radiation Hardening by Process

The 65 nm process provides deep Nwell technology to achieve low noise. From the aspect of radiation-hardening, the deep Nwell can also absorb the SET current of heavy-ion strike.

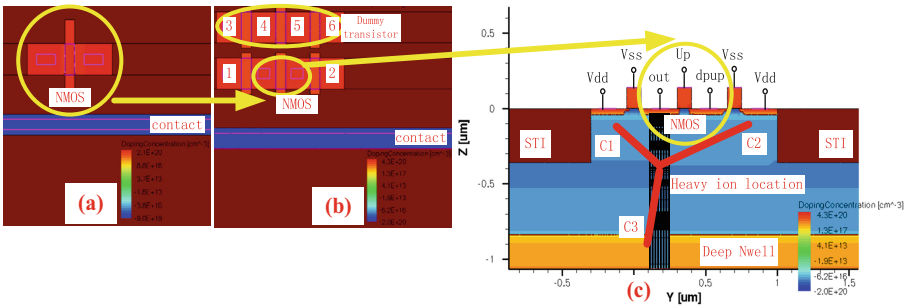


Fig. 1. Layout harden with dummy transistors by deep Nwell technology

The heavy-ion simulations have been performed using TCAD software. The simulation result is shown in Fig. 1. LET is 37.6 meV·cm<sup>2</sup>/mg, and the ion strike is irradiated normal to the chip surface.

As shown in Fig. 2(a), the SET current is all absorbed by the deep Nwell and the dummy transistor. The Fig. 2(b) shows that the voltage has no significant variations under heavy-ion when switch gate and the dummy transistors are built in deep Nwell.

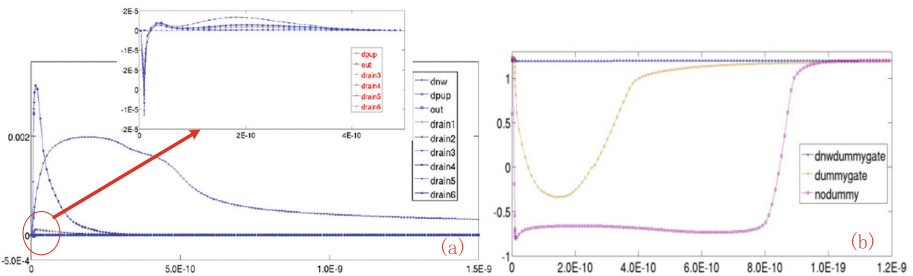


Fig. 2. SET current and voltage variation

### 3 Radiation Hardening by Design

Traditional PLL is single loop negative feedback system consists of PFD, CP, LPF, DIV and VCO. When SET happen at one of the five components, it may lead the PLL out of lock state and the error bit rate of SerDes will increase.

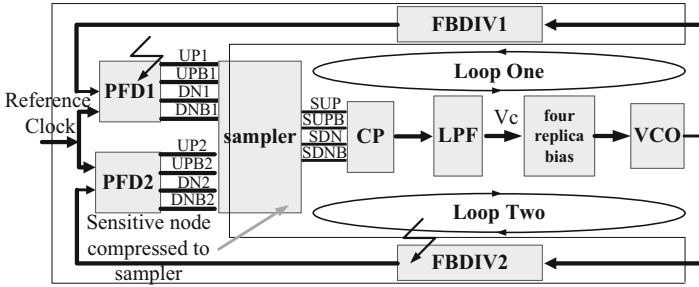


Fig. 3. SET current and voltage variation Double feedback loop self-sampling PLL

The PFD and Divider are digital circuits and are very sensitive to SET, because they use the minimum gate length. To improve the anti-SET capability, we adapt the double loop to feedback the divided signals from VCO to PFD in Fig. 3. The advantage of this structure is that, it will largely reduce the sensitivity of feedback loops. As shown in Fig. 4, if the iron strikes the PFD1 and FBDIV2, it will only induce one loop to produce error signal in UP1 or UP2. The other loop operation remains good and will produce right UP and DN signals at the same time. The sampling circuit in Fig. 4 will let correct up and down signals(SUP, SUPB, SDN, SDNB) pass through. This double loop structure will compress the sensitive nodes of all the FBDIV and PFD into AND gates in sampler.

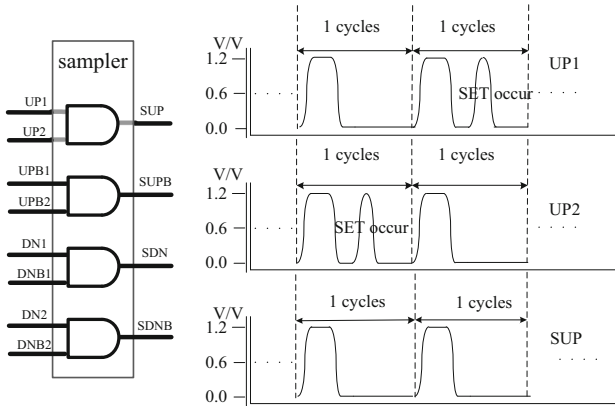


Fig. 4. Function of sampler

Previous study of voltage-based CP (V-CP) [4] employs large reference spurs and phase noise, which is not suitable for SerDes application. The proposed CP is especially suitable for low jitter application because its mismatch is quite low, as shown in Fig. 5. The differential structure of CP we used in this paper has alleviated the charge sharing of traditional charge pump by using two pairs of charge pump. It is similar to the structure of [6].

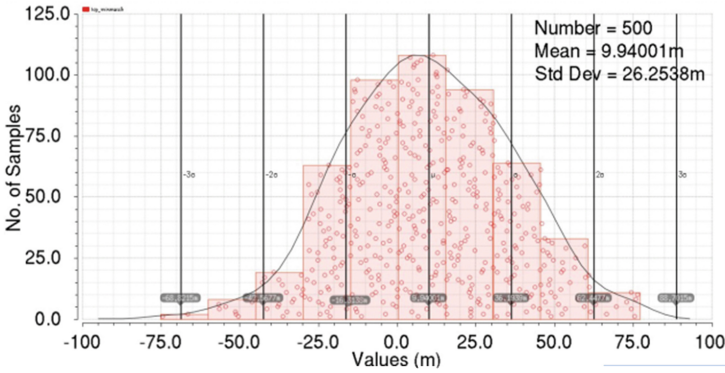


Fig. 5. The Current Waveform and DC mismatch

To improve the anti-radiation ability of CP, M8 is added. It is called sensitive nodes transformation technology, as shown in Fig. 6, the sensitive nodes of replica charge pump in the left is compressed to M8. As the sensitive nodes of CP are compressed into M8, the switch gate should be hardened at circuit level and layout level. As shown in Fig. 6, the original switch gate is one NMOS transistor, to absorb the large SET current, the dummy transistors are located round the switch gate. The gates of dummy transistors are all connected to ground and the drains of dummy transistors are all connected to power rail. The dummy transistors will not affect the operation of CP, but it will absorb the SET current when the ion strikes the sensitive nodes of CP.

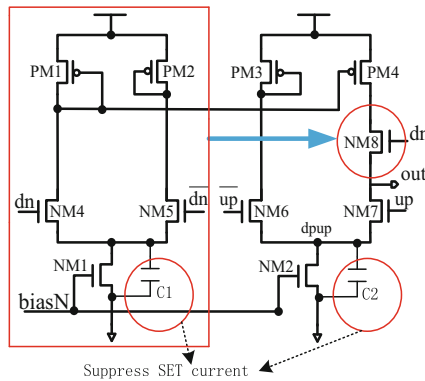


Fig. 6. Circuits of charge pump

## 4 Layout Design and Simulation Analysis

The test chip layout of PLL is shown in Fig. 7. We simulate the PLL with 65 nm process model to testify the low jitter and high frequency performance of this PLL. The RMS jitter and stability are calculated by Matlab program. The result is shown in Fig. 8. The  $R_j$  will not exceed 2.17 ps and the  $D_j$  is 6.5 ps, when the PLL is locked at 3.125 GHz.

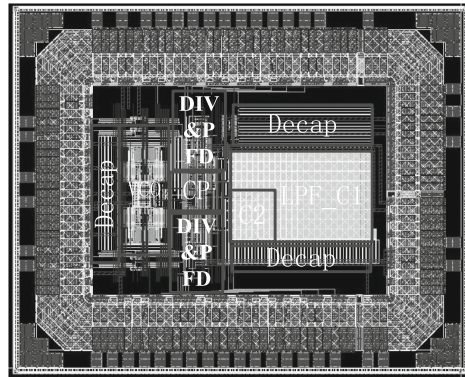


Fig. 7. Test chip layout of PLL

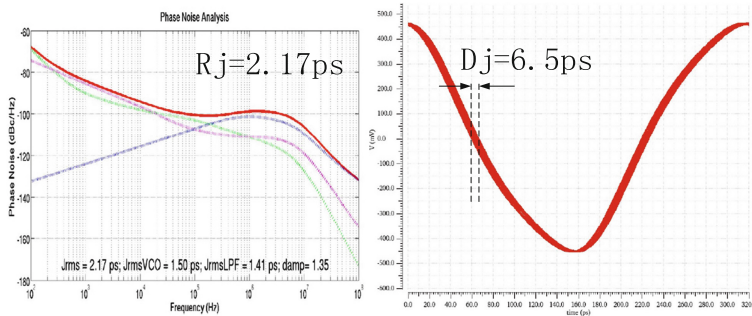
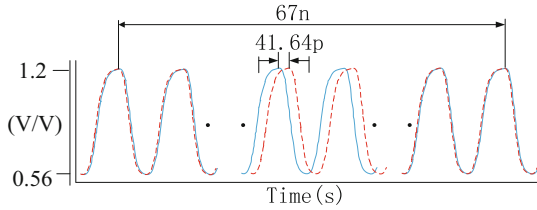


Fig. 8. PLL output noise

The SET current model is added when the PLL is locked at 3.125 GHz, the unit interval of SerDes is 320 ps. To sample the correct RX data, the clock skew can not exceed 0.5UI. As shown in Fig. 9, the maximum skew that the VCO would produce is 41.64 ps, and the recovery time is 67 ns. Theoretically, the SET would not happen again in the 67 ns. The SerDes system will not have error data when SET happened in PLL.



**Fig. 9.** SET current and voltage variation

We compare the proposed PLL with some recently published papers in Table 1. The deterministic jitter is 6.5 ps@65 nm. The integrated RMS jitter is 2.17 ps@65 nm. The jitter performance is good among all the references means that the charge pump can achieve better jitter performance than other PLLs. The proposed PLL will not decrease the error data rate when the PLL has SEE effects. Although Ref. [7] is more advanced in jitter and power consumption, but it is not suitable for radiation hardening because of interpolative phase-coupled oscillator DCO structure, the SET effect will lead the PLL out of lock state.

**Table 1.** Comparison among Different PLLs

Ref. Year	[7] 2014	[8] 2010	[9] 2016	This Work
Tech.(nm)	65	45	130	65
Power(V)	0.8	2.5	1.2	1.2
Power (mW)	0.78	70	8.54	43.6
RMS Jitter(ps)	1.7@0.9 GHz	0.99@2.5 GHz	7.1@0.5 GHz	2.17@3.125 GHz
Output [MHz]	390–1410	2500	500	1250–3125
Input [MHz]	40–350	100	100	100–300

## 5 Conclusion

A radiation-tolerant PLL was designed and fabricated in 65 nm process. The PLL hardened by process was discussed. Various radiation hardening by design techniques were employed in order to have comprehensive radiation tolerance. A novel double loop feedback self-sampling structure was proposed to mitigate radiation effects of divider and PFD. Radiation hardened current based CP with sensitive nodes transformation technology was proposed to make the CP have smaller sensitive nodes. The simulation results demonstrate the good jitter performance of PLL when SET happens.

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