A Programmable Pre-emphasis Transmitter for SerDes in 40 nm CMOS

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Abstract. Based on 40 nm standard CMOS process, this paper proposes an easy realized, programmable pre-emphasis transmitter. The circuit is used in high performance SerDes (Serializer-Deserializer) chip, which utilizes a 2-tap current-mode pre-emphasis technique, resulting less design complicacy as well as low noise. Furthermore, a tail current DAC enables equalization to be configurable in order to adapt to various data rate condition. Simulation results show 0–6 db pre-emphasis ability and 0–1.3 V differential output voltage swing under 2.5–6.25 GB/s transmission rate, which meet specifications of high speed serial link standards such as PCIE2.1 and RapidIO2.2.

Keywords: Current-mode driver · Feed forward equalization
SerDes · Programmable pre-emphasis

1 Introduction

The demand of bandwidth for the transmission has increased a lot with the rapidly development of integrated circuit, which caused interface bandwidth become a bottleneck for performance improvement in digital systems [1]. Traditional parallel interface need more chip pins to provide enough bandwidth but its signal attenuation also become a serious problem while data rate beyond 1 Gbps [8]. However, high-speed serial link which based on SerDes (Serializer, De-serializer) can work at dozens of Gbps and consume less energy [3], such as PCIE and RapidIO, which attract many researchers interest. SerDes chips adopt analog and digital circuit mixed design technology to resolve signal integrality problems such as channel attenuation and Inter Symbol Interference (ISI)[10].

Transmitter is an important part in SerDes which consume a large percentage of serial-link power. Most transmitters adopt 2-tap pre-emphasis that data code and pre-emphasis code combine with voltage or current mode to form a pre-emphasis driver. Young-Hoon song and Samuel Palermo designed a voltage-mode transmitter with current-mode equalization in 90-nm CMOS baud rate achieving 6 Gbps [6], which makes full use of current mode pre-emphasis and low power consumption characteristics. Huang proposed a 80 mw 40 GB/s transmitter with automatic serializing time window search and 2-tap pre-emphasis

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in 65 nm CMOS technology [4], but it is not programmable. This paper proposes a programmable pre-emphasis transmitter for SerDes, which not only realizes traditional function of driver circuit, but also adds extensibility and programmable ability with little complexity. This transmitter realize programmable pre-emphasis and output amplitude based on 40 nm COMS process. Moreover, it can work in different channel conditions at 2.5–6.25 GB/s transmission rate, and satisfying variety of standard protocols.

The paper is organized as follows: Sect. 2 explains the pre-emphasis technique and the overall architecture of the SerDes. The circuit design of functional blocks is described in Sect. 3. Section 4 shows the implementation and simulation results. Finally, a conclusion is made in Sect. 5.

2 Pre-emphasis Technique

An ideal rectangular wave can be decomposed into different frequency cosine harmonic [7], and the attenuation always occurs on high frequency due to the low pass characteristics of transmission channel. Moreover, the high frequency components mainly affect the signal jump edge, so compensating attenuation means compensating signal jump edge, i.e. pre-emphasis technique [5]. Figure 1 shows the pre-emphasis amplifies the high frequency components, which can offset emphasis and attenuation to obtain a smooth response [2].

The basic structure of the 2-tap pre-emphasis driver as shown in Fig. 2(a), *imain* and *ipos* are two tail currents Rt is a 50 Ω resistor network to match channel impedance, and *vptx* is supply voltage. The serializer provides differential bits *mainp*/*mainn* and pre-emphasis bits *pos*1*p*/*pos*1*n*, and combining them in form of current or voltage to realize pre-emphasis.

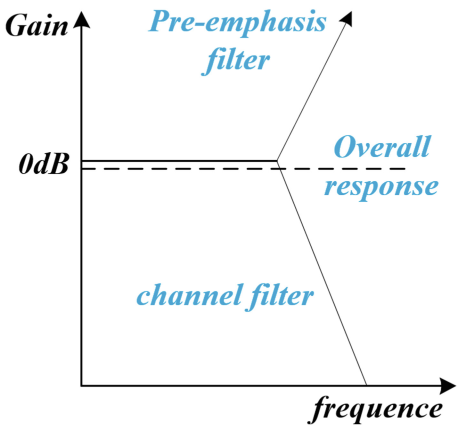


Fig. 1. The function of pre-emphasis

We list the voltages of *txp*, *txn* and their difference in Table 1, and the corresponding values of differential bits *MAIN* and pre-emphasis bits *POS*1 are list in Fig. 2(b).

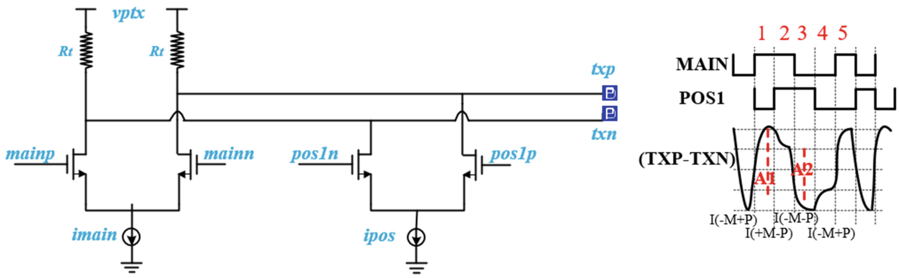


Fig. 2. Two-tap current mode pre-emphasis driver. (a) is the driver circuit, (b) is the input data code

Table 1. The output voltage of driver (Rt = 50 Ω)

Tap	1	2	3	4
txp	vptx	vptx-ipos*Rt	Vptx-(imain+ipos)*Rt	Vptx-imain*Rt
txn	vptx-(imain+ipos)*Rt	vptx-imain*Rt	vptx	vptx-ipos*Rt
txp-txn	(imain+ipos)*Rt	(imain-ipos)*Rt	-(imain+ipos)*Rt	-(imain-ipos)*Rt

According to the Table 1, the output differential swing A1 and the differential swing A2 (without emphasis) is:

$$\mathrm{A1} = \mathrm{txp} - \mathrm{txn} = (\mathrm{imain} + \mathrm{ipmos}) * \mathrm{Rt} \tag{1}$$

$$\mathrm{A2} = (\mathrm{imain} - \mathrm{ipmos}) * \mathrm{Rt} \tag{2}$$

The pre-emphasis gain is:

$$\mathrm{EQ(dB)} = 20\mathrm{log}\frac{\mathrm{A}_1}{\mathrm{A}_2} = 20\log(1 + \frac{2\mathrm{ipos}}{\mathrm{imain} - \mathrm{ipos}}) \tag{3}$$

When output swing A1, pre-emphasis gain and termination resistors Rt are fixed, the *imain* and *ipos* can be calculated base on (1) and (2):

$$\mathrm{imain} = 0.5 * (1+\frac{A2}{A1}) * \frac{A1}{Rt} \tag{4}$$

$$\mathrm{ipos} = 0.5 * (1-\frac{A2}{A1}) * \frac{A1}{Rt} \tag{5}$$

3 Circuit Design

The overall structure of the proposed transmitter is shown in Fig. 3, which consists of synchronization module, serializer and driver.

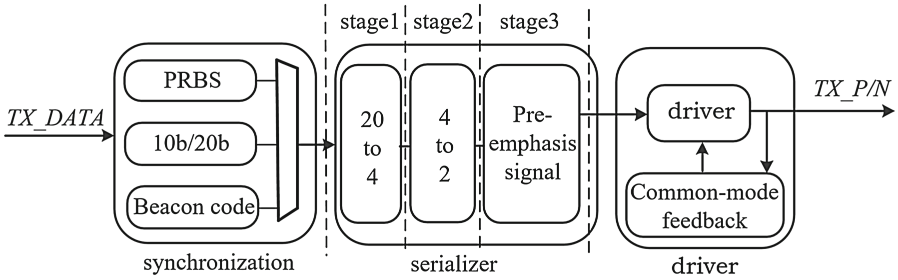


Fig. 3. The overall structure of transmitter

Synchronization module preprocesses the data which come from data link layer that transfer it into 20 bits. Then, choosing one in three base on the control bits, and the three choices include 20 bits parallel data, the output of PRBS generator, and Beacon code. This module can be realized by Verilog programming.

Serializer adopts multi-phase single-stage and single-phase multi-stage circuit to realize serialization, which can raise the clock frequency step by step and reduce this modules working at high frequency clock. 20 bits parallel data are serialized to 1 bit after three stage serialization in its correspond clock frequency.

The driver converts digital signal to analog signal and realizes pre-emphasis before signals are sent to the channel. The width of the final output waveform and swing are determined by driver when impedance is matched.

3.1 Serializer Circuit Design

The structure of serializer is shown in Fig. 4, serializer converts parallel data to serial bit through three stages. Firstly, the input parallel data (20 bits) are divided into four channels each is 5 bits, and then sent them into four identical 5:1 selectors respectively to obtain 4 bits parallel data. Secondly, the 4 bits data are divided into two groups: data_a/b and data_c/d, taking data_a/b as a example, let data_a and data_b align with the posedge and the negedge of the 5*ft clock respectively to obtain signal a/b. Then a/b are sent into 2:1 selector for the second serialization under the 5*ft clock (sa). The selector is static CMOS circuit, their signal processing obeys:

$$\text{out} = \overline{\overline{sa \bullet a} \bullet \overline{sb \bullet b}} = sa \bullet a + sb \bullet b \tag{6}$$

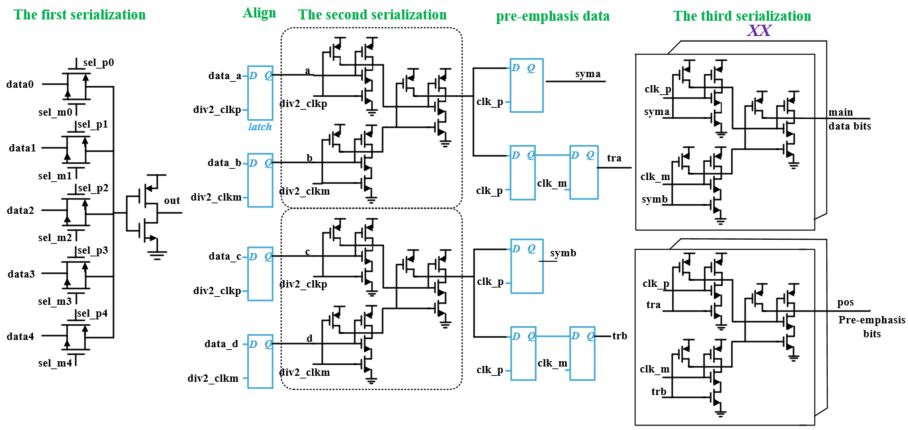


Fig. 4. The overall structure of transmitter

By the way, the pre-emphasis data obtained by utilizing a latch delay a clock cycle for the output data of the second serialization.

The third serialization realizes 2:1 conversion for the data bit and pre-emphasis bit using two selectors under the 10 ft clock. The structure of the selector is the same as the second serialization. In Fig. 4, XX means a number of parallel identical selectors, because multiple parallel selectors can increase the current and make the serialization work faster [9].

3.2 Pre-emphasis Programmable Design

According to Eq. (3), the effect of pre-emphasis can be expressed as:

$$\mathrm{EQ(dB)} = 20\log\left(1 + \frac{2}{\frac{\mathrm{imain}}{\mathrm{ipos}} - 1}\right) \tag{7}$$

In order to realize programmable pre-emphasis, i.e. programmable *ipos*, this paper design current steering DAC circuit is shown in Fig. 5, in which *iref* is a reference current, tr_h[4:0] and tr_hn[4:0] are control bits, so *ipos* is determined by:

$$ipos = \sum\nolimits_{i=0}^{i=4} tr\_h[i] \bullet iref \tag{8}$$

Speed requirement is not strict to this DAC [11], because of current *ipos* is fixed when control bits are configured. In this paper, in order to get an accurate and steady current, we adopt cascode source current.

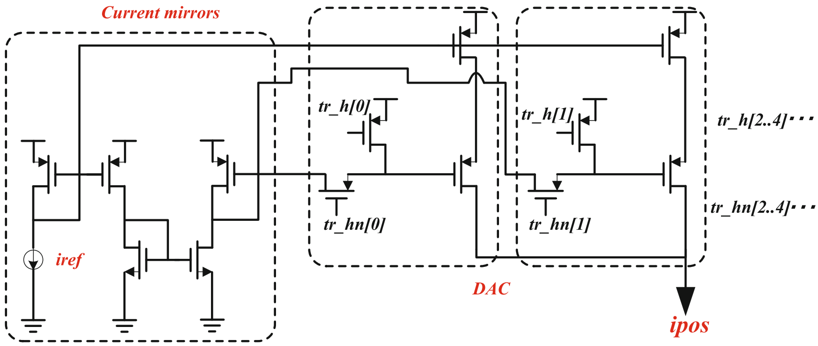


Fig. 5. Current tail DAC circuit

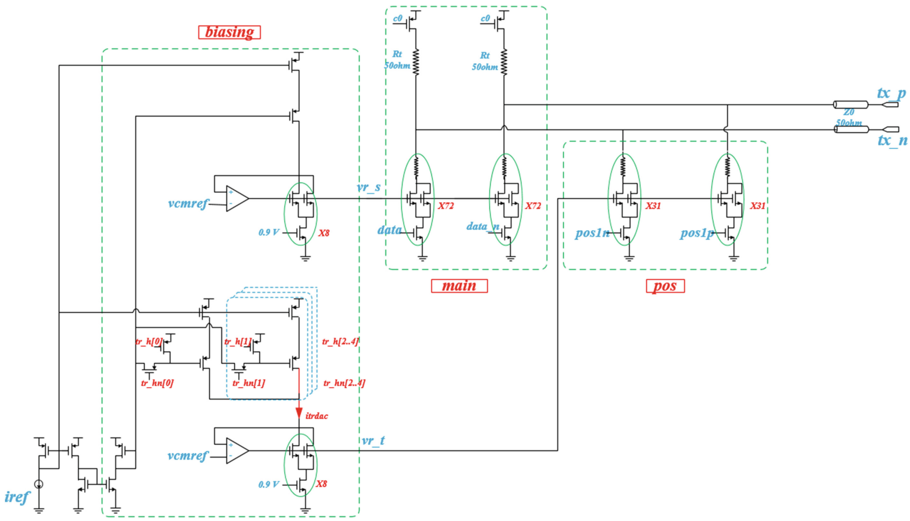
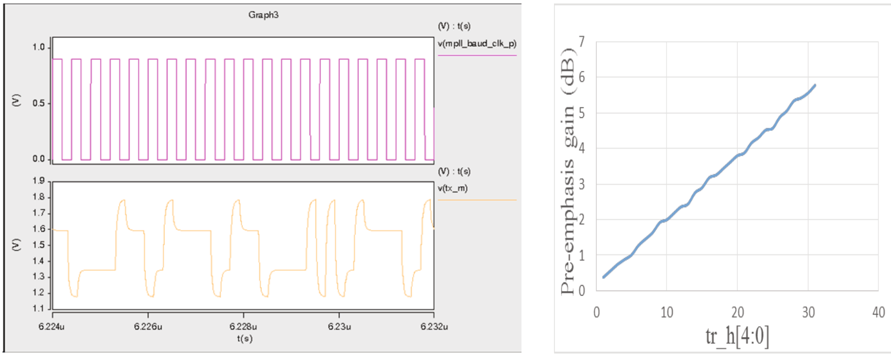


Fig. 6. The overall structure of transmitter

3.3 Driver Circuit Design

Figure 6 illustrates three modules of the driver in this paper, the biasing module produces current *imain* with the reference of current *iref*, the lower part is pre-emphasis programmable circuit which produces *ipos*. Main module and *pos* module are current mode driver.

When tr_h[4:0] = 10001 and Rt = 50 Ω, the result of simulation is shown in Fig. 7(a). The serial data baud rate is 5 GB/s and the pre-emphasis gain (EQ) is about 2 dB. Figure 7(b) shows indicate that there is liner correlation between tr_h[4:0] and EQ.



(a) (b)

Fig. 7. The simulation results of pre-emphasis. (*a*) tr_h[4:0] = 10001(Hspice) (*b*) Correlations between tr_h[4:0] and EQ

4 Simulation Results

4.1 Simulation in Normal Transmission State

Figure 8 illustrates output waveforms and eye diagram in normal transmission state, we set tr[4:0] = 11011, common mode voltage is 1.2 V, EQ is 6 dB, and the output serial data baud rate is 6.25 Gbps.

Table 2 lists the simulation result in different corner. Take TT as a example, the output differential swing is 979.35 mV, EQ is 6.08 dB, the rise and fall time is

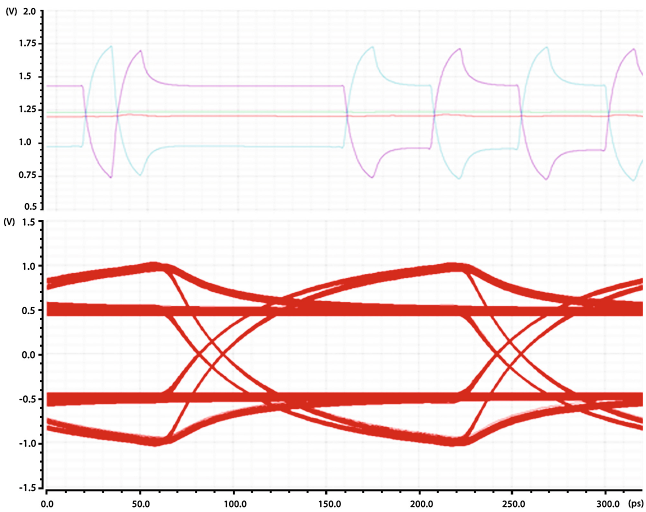


Fig. 8. The output waveform and eye diagram of transmitter

Table 2. The simulation result in normal transmission state

Index	RapidIO$^{\alpha}$	RapidIO$^{\beta}$	PCIE2.1	TT	SS	FF
VTX-DIFF-PP	0.4–0.75 V	0.8–1.2 V	0.8–1.2 V	0.98 V	0.90 V	1.0 V
VTX-DE-RATIO	*	*	5.5–6.5 dB	6.08 dB	5.62 dB	6.47 dB
T_tr,T_tf	>30 ps	>30 ps	>0.15 UI	68 ps	74 ps	63.7 ps
T_Vcm	0.1–1.7 V	0.1–1.7 V	0–3.6 V	1.234 V	1.05248 V	1.4074 V
	0.63–1.1 V	0.63–1.1 V				
TTXEYE	>0.7 UI	>0.7 UI	>=0.75 UI	0.906 UI	0.905 UI	0.906 UI

α represents the RapidIO2.2 Level 2 (short distance);
β represents the RapidIO2.2 Level 2 (long distance);
$VTXDIFFPP$: The differential output peak voltage;
$VTXDERATIO$: The pre-emphasis gain;
T_tr: The rise time of eye diagram;
T_tf: The fall time of eye diagram;
$T - Vcm$: The common mode voltage;
$TTX - EYE$: The width of eye diagram.

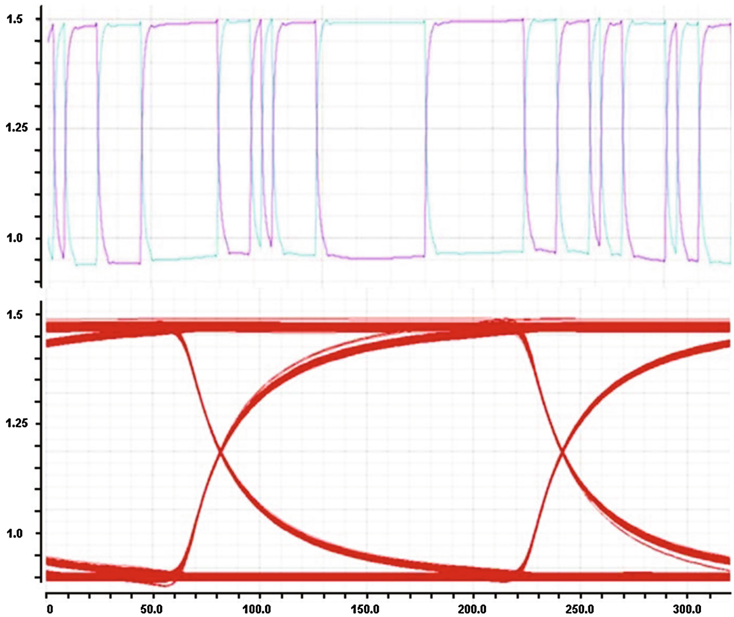


Fig. 9. The wave and eye diagram of short-distance transmission (corner: TT)

68ps on average with 0.906-UI eye width, common mode voltage is 1.234 V. All the parameters meet the requirements of RapidIO 2.2 and PCIE 2.1. Because of the length of channel is short in short distance RapidIO2.2, pre-emphasis is unnecessary and need some extra simulation.

For the situation of short-distance transmission, The attenuation can be ignored due to the channel is short, so we set the control bits tr[4:0] = 0000 to close pre-emphasis and lower the signal swing to decrease power consumption. Figure 9 shows the simulation wave when the level[5:0] = 100011, the output wave swing is 0.55 V in this moment.

4.2 Simulation with Package

Figure 10 shows the simulation result when the pre-emphasis is 6 dB, common mode level is 1.2 V and the input data is PRBS7 code. The output signal differential swing of driver is about 1 V, and waveform becomes smooth through the channel due to the pre-emphasis offsets the decay of high frequency. The swing is reduced to approximately 0.6 V which is approximately equivalent to 10 dB attenuation.

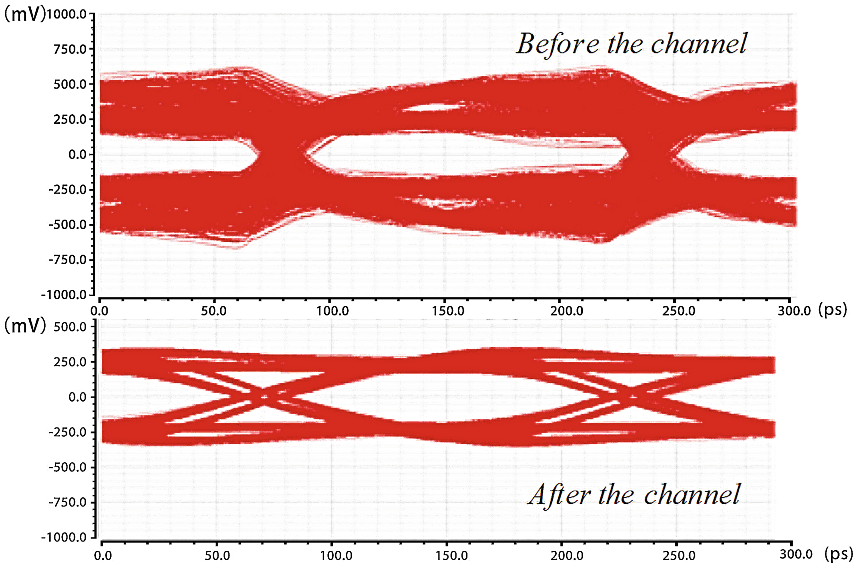


Fig. 10. The overall structure of transmitter

5 Conclusion

This paper proposes a transmitter based on 40 nm process, which can work at 2.5–6.25 GB/s data rate, offer 0–6 dB programmable pre-emphasis, common mode, and meeting PCIE2.1 and RapidIO2.2 protocols. By using simple DAC and amplifier, this design not only realizes traditional function of driver circuit, but also adds extensibility as well as programmable ability with little complexity which is the trend in multi-protocol supporting circuit design. The most difficult part of this design is that it needs more transistors due to the large total current of branches.

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References

1. Balamurugan, G., Kennedy, J., Banerjee, G., Jaussi, J.E., Mansuri, M., O'Mahony, F., Casper, B., Mooney, R.: A scalable 5c15 Gbps, 14c75 mw low-power i/o transceiver in 65 nm cmos. IEEE J. Solid-State Circuits **43**(4), 1010–1019 (2008)
2. Bassi, M., Radice, F., Bruccoleri, M., Erba, S., Mazzanti, A.: A high-swing 45 gb/s hybrid voltage and current-mode pam-4 transmitter in 28 nm cmos fdsoi. IEEE J. Solid-State Circuits **51**(11), 2702–2715 (2016)
3. Hu, C., Chen, S., Huang, P., Liu, Y., Chen, J.: Evaluating the single event sensitivity of dynamic comparator in 5 Gbps serdes. Ieice Electron. Express **12**(23), 1–10 (2015)
4. Huang, K., Wang, Z., Zheng, X., Zhang, C., Wang, Z.: A 80 mw 40 gb/s transmitter with automatic serializing time window search and 2-tap pre-emphasis in 65 nm cmos technology. IEEE Trans. Circuits Syst. I Regul. Papers **62**(5), 1441–1450 (2015)
5. Lin, C.H., Wang, C.H., Jou, S.J.: 5 Gbps serial link transmitter with pre-emphasis. In: Asia and South Pacific Design Automation Conference, Proceedings of the ASP-DAC 2003, pp. 795–800 (2003)
6. Song, Y.H., Palermo, S.: A 6-Gbit/s hybrid voltage-mode transmitter with current-mode equalization in 90-nm cmos. IEEE Trans. Circuits Syst. II Express Briefs **59**(8), 491–495 (2012)
7. Yan-Hua, X.I.: Periodic signal's decomposition and composition based on matlab. Comput. Mod. 234–242 (2011)
8. Yang, N.: Signal attenuation and its variation range analysis in the transmitter-receiver input circuit of the double frequency carrier relaying system with directional comparison. Autom. Electr. Power Syst. **46**(2), 362–366 (1983)
9. Yuan, S., Wu, L., Wang, Z., Zheng, X., Zhang, C., Wang, Z.: A 70 mw 25 GB/s quarter-rate serdes transmitter and receiver chipset with 40 dB of equalization in 65 nm cmos technology. IEEE Trans. Circuits Syst. I Regul. Papers **63**(7), 939–949 (2016)
10. Zhou, N., Huang, K., Lve, F., Wang, Z., Zheng, X., Zhang, C., Li, F., Wang, Z.: A 76 mw 40-GB/s serdes transmitter with 64:1 mux in 65-nm cmos technology. In: International Conference on Electronics Information and Emergency Communication, pp. 155–158 (2016)
11. Zite, S.E.: Design of a unit current cell for a 12-bit 3.2 GHz current steering digital-to-analog converter (2006)