An Efficient Model for Soft Error Vulnerability of Dynamic Circuits

Yan Sun(✉), Yuesheng Cao, Jinwen Li, and Tiejun Li

College of Computer, National University of Defense Technology,
Changsha 410073, Hunan, People's Republic of China
yansun@nudt.edu.cn

Abstract. Dynamic circuits are widely used in high-speed circuit. However, dynamic circuits are very vulnerable to soft errors. An analytical model of critical charge for vulnerable nodes of dynamic circuits is developed. As the accurate model is too complex to calculate, a simplified efficient model is proposed by using an approximate method. Proposed model are verified by SPICE simulation and error analysis respectively. Results demonstrate that these models have high accuracy and can be used both in the efficient analysis and automatic CAD tools.

Keywords: Soft error · Dynamic circuit · Critical charge
Domino logic

1 Introduction

Dynamic circuits are widely used in high performance design because of their increased speed and reduced implementation area, such as ALUs, register files, and multiplexers. However, with the progress of VLSI technology, the scaling down of supply voltage and feature size increase the vulnerability of circuits to soft errors, and especially worsen the reliability of dynamic circuits [1].

The objective of this paper is to character and quantify the impact of soft errors on dynamic circuits. The profile of soft error vulnerability in dynamic circuits is studied, then an accurate and an efficient model for soft error vulnerability estimation of dynamic circuits are proposed.

2 Vulnerability Profile of Dynamic Circuits

Domino logic is widespread representative of dynamic logic, we will refer to domino logic as the typical dynamic circuits in this paper. A domino logic module

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consists of an n-type dynamic logic block followed by a static inverter, and it has two phases of operation. In the precharge phase, the output of the dynamic gate is charged to logic “1”; in the evaluate phase, the output node either remains at “1” or discharged to “0” depending on inputs. Figure 1 shows a domino inverter chain. Cha *et al.* reported that any gate can be always mapped into equivalent inverters [2], so in this paper a domino inverter chain is taken as an example to research the character of dynamic circuits’ vulnerability to soft errors.

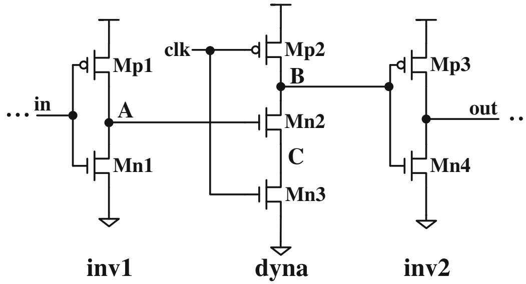

Fig. 1. A segment of a domino inverter chain.

In combinational circuits, single event transient (SET) becomes a dominant source of soft errors [3]. A SET may propagate to a flip-flop input and get latched. Same as critical charge defined for memory elements, the SET critical charge (Q_{SET}) can be defined as the minimum amount of collected charges at a circuit node which may give rise to a SET in subsequent gate [4]. A typical domino inverter chain is made up of a group of dynamic and static CMOS inverters, as shown in Fig. 1. In order to estimate vulnerability of it, just need to analyze characters of nodes A, B and C.

When an SET occurs at node A, B or C, the impact on output is various. It can be classified into 12 cases, as shown in Table 1. Q_{SET} of case B1, B3, C1 are almost the same and $Q_{\mathrm{SET,B3}} < Q_{\mathrm{SET,B1}} < Q_{\mathrm{SET,C1}}$; Q_{SET} of case C2, C3, C4 are rather larger. Therefore, in order to estimate soft error vulnerability of domino inverter chain, only need to analyze Q_{SET} of A4, B2, B3 and B4.

3 Vulnerability Quantitative Modeling of Dynamic Circuits

A particle strikes in susceptible nodes can cause a transient current impulse. To analyze soft error vulnerability, the transient current impulse can be described as a rectangular pulse with amplitude I_0 and width t_m.

3.1 Case A4, B2 and B3

Set static and dynamic inverters of circuit in Fig. 1 to be minimal size. For case A4, a particle strike in node A can cause a positive current impulse when $in = 1$ and $clk = 1$, and the impulse can be described by Eq. (1).

Table 1. Soft error vulnerabilities of susceptible nodes in a domino inverter chain

Case	*in*	*clk*	Polarity of SET	Impact on out	Q_{SET}
A1	0	0	Negative	No impact	Infinite
A2	0	1	Negative	No impact	Infinite
A3	1	0	Positive	No impact	Infinite
A4	1	1	Positive	0→1	Small
B1	0	0	Negative	0→1→0	Small
B2	0	1	Positive	1→0→1	Small
B3	1	0	Negative	0→1→0	Small
B4	1	1	Negative	0→1	Very small
C1	0	0	Negative	0→1→0	Small
C2	0	1	Positive	1→0→1	Large
C3	1	0	Negative	0→1→0	Large
C4	1	1	Negative	0→1	Large

$$I_a(t) = G_{n1}V_a(t) + C_{tot,a}\frac{dV_a(t)}{dt}, \tag{1}$$

where G_{n1} is conductance of Mn1. $C_{tot,a}$ is total capacitance of node A. For case A4, $C_{tot,a}$ is sum of diffusion capacitance of Mp1 and Mn1, and gate capacitance of Mn2. When $0 \le t \le t_m$, voltage of node A can be solved:

$$V_a(t) = \frac{I_0}{G_{n1}}\left[1 - \exp\left(-\frac{G_{n1}}{C_{tot,a}}t\right)\right]. \tag{2}$$

Once voltage of node A overtakes switch threshold of devices followed, SET generated in node A would propagate to next stage. In this case, the minimal collected charge is Q_{SET} of node A. If switch threshold of devices followed node A is V_T, the critical condition of SET propagate to next stage is $V_a(t_m) = V_T$. In Fig. 1, V_T is threshold voltage of transistor Mn2, $V_{T,n2}$. Accumulated charge reaches to maximum at time t_m. Take $t = t_m$ to Eq. (2) and I_{0,t_m} can be solved:

$$I_{0,\mathrm{t_m}} = \frac{V_{T,n2}G_{n1}}{1 - \exp\left(\dfrac{-t_m G_{n1}}{C_{tot,a}}\right)}. \tag{3}$$

And then, the Q_{SET} of case A4 can be calculated:

$$Q_{\mathrm{SET,A4}} = \frac{V_{T,n2}t_m G_{n1}}{1 - \exp\left(\dfrac{-t_m G_{n1}}{C_{tot,a}}\right)}. \tag{4}$$

Using the same method, $Q_{\mathrm{SET,B2}}$ and $Q_{\mathrm{SET,B3}}$ also can be solved:

$$Q_{\mathrm{SET,B2}} = \frac{V_{T,inv2}t_m G_{n2,n3}}{1 - \exp\left(\dfrac{-t_m G_{n2,n3}}{C_{tot,b}}\right)}, \tag{5}$$

$$Q_{\mathrm{SET,B3}} = \frac{(V_{DD} - V_{T,inv2})t_m G_{p2}}{1 - \exp\left(\dfrac{-t_m G_{p2}}{C_{tot,b}}\right)}. \tag{6}$$

In Eqs. (5) and (6), $V_{T,inv2}$ is switch threshold of inv2; $G_{n2,n3}$ is conductance of Mn2-Mn3 pull-down path; $C_{tot,b}$ is total capacitance of node B; V_{DD} is supply voltage; G_{p2} is conductance of Mp2. It can be found that Q_{SET} of case A4, B2 and B3 have similar expression, and they can be united to one equation:

$$Q_{\mathrm{SET}} = \frac{V_T^* t_m G_d}{1 - \exp\left(\dfrac{-t_m G_d}{C_{tot}}\right)}, \tag{7}$$

where G_d is drive transistors conductance of target node; C_{tot} is total capacitance of target node; V_T^* is switch threshold of next stage, which is $V_{DD} - V_T$ or V_T for particular cases. Generally, drive transistors work in linear area, therefore G_d in Eq. (7) can be expressed approximately as:

$$G_d = \mu C_{ox} \frac{W}{L} (V_{GS} - V_T) = k_g W, \tag{8}$$

where μ is mobility of electron or hole; C_{ox} is capacitance of gate oxide per unit area; V_T is threshold voltage of transistors; W and L is equivalent channel width and length of transistors respectively. k_g is a constant related to technology and circuit, which can be expressed as $k_g = \mu C_{ox} (V_{GS} - V_T) / L$.

Assume that number of transistors source or drain connected to target node is n, and gate connected to target node is r. Equation (7) can be written as:

$$C_{tot} = \sum_{i=1}^{n} C_{diff,i} + \sum_{j=1}^{r} C_{G,j}, \tag{9}$$

where $\sum_{i=1}^{n} C_{diff,i}$ is total diffusion capacitance of target node; $\sum_{j=1}^{r} C_{G,j}$ is total gate capacitance of target node. For a single MOSFET, $C_{diff} = C_j LW + C_{jsw}(2L + W) = k_{c0} + k_{c1} W$, and $C_G = (C_{ox} L + 2C_o) W = k_{c2} W$. Where C_j, C_{jsw}, C_{ox} and C_o are technology constant. In addition, channel length of transistors are minimum value. Consequently, k_{c0}, k_{c1} and k_{c2} are constant.

According to Eq. (7), Q_{SET} of case A4, B2 and B3 can be expressed as:

$$Q_{\mathrm{SET}} = \frac{V_T^* t_m k_g W_d}{1 - \exp\left(\dfrac{-t_m k_g W_d}{\sum_{i=1}^{n} (k_{c0,i} + k_{c1,i} W_i) + \sum_{j=1}^{r} (k_{c2,j} W_j)}\right)}, \tag{10}$$

where W_d is equivalent channel width of transistors in drive logic; W_i is channel width of transistors connected to target node in drive logic; W_j is channel width of transistors in fan-out logic. Other variables are all constant and are related to technology and circuit structure.

3.2 Case B4

For case B4, both Mp2 and Mn2 are closed. A negative impulse would be generated when a particle strikes in node B. Because node B doesn't have path to supply or ground, the current can be described in Eq. (11):

$$C_{tot} = \sum_{i=1}^{n} C_{diff,i} + \sum_{j=1}^{r} C_{G,j}, \tag{11}$$

where $C_{tot,b}$ is total capacitance of node B. When $0 \le t \le t_m$, $I_b(t) = I_0$. Voltage of node B can be expressed:

$$V_b(t) = \frac{1}{C_{tot,b}} \int_0^t I_b(t)dt = \frac{I_0}{C_{tot,b}} t. \tag{12}$$

Once the voltage of node B overtakes switch threshold of devices followed, SET generated in node B would propagate to next stage. In this case, the minimal collected charge is Q_{SET} of node B. If switch threshold of devices followed node B is $V_{DD} - V_{T,nv2}$, the critical condition of SET propagate to next stage is $V_b(t_m) = V_{DD} - V_{T,inv2}$. Accumulated charge of node B reaches to maximum at time t_m, so the Q_{SET} of case B4 can be calculated:

$$Q_{\mathrm{SET},B4} = \frac{C_{tot,b}\left(V_{DD} - V_{T,inv2}\right)}{t_m} t_m = C_{tot,b}\left(V_{DD} - V_{T,inv2}\right). \tag{13}$$

Because source or drain of Mp2 and Mn2 are connected to node B, gate of Mp3 and Mn4 are connected to node B, Eq. (14) can be solved:

$$C_{tot,b} = \left(C_{diff,p2} + C_{diff,n2}\right) + \left(C_{G,p3} + C_{G,n4}\right). \tag{14}$$

Same as case A4, Q_{SET} of case B4 can be expressed:

$$\begin{aligned} Q_{\mathrm{SET}} = \Big[&(k_{c0,p2} + k_{c1,p2}W_{p2}) + (k_{c0,n2} + k_{c1,n2}W_{n2}) \\ &+ (k_{c2,p3}W_{p3} + k_{c2,n4}W_{n4}) \Big] \left(V_{DD} - V_{T,inv2}\right), \end{aligned} \tag{15}$$

where W_{p2}, W_{n2}, W_{p3} and W_{n4} are effective channel width of Mp2, Mn2, Mp3 and Mn4, respectively. Other variables are constant related to technology and circuit structure.

From above analysis, Q_{SET} of vulnerable nodes in dynamic circuits are only related to transistor size for a certain technology and circuit structure. Transistor sizing is an effective technique to improve Q_{SET} of vulnerable nodes [5], thereby reduce vulnerability to soft errors of dynamic circuits.

4 Model Simplifying for Vulnerability of Dynamic Circuits

SET critical charges of vulnerable nodes can be calculated using Eqs. (10) and (15) accurately. However, accurate model is too complex to calculate, especially

for case A4, B2 and B3. It is necessary to research simpler model for efficient analyzing and automatic CAD tools.

For a certain technology and circuit structure, Q_{SET} is only related to channel width of drive and load transistors when channel length of transistors are minimum value, and PMOS-NMOS in inv1, dyna, inv2 are asymmetric structure. Set channel width of load (or drive) transistors as minimum size, and observe trends of Q_{SET} with variation of channel width of drive (or load) transistors. It is can be found that the trends are approximately linear. Based on this observation, Eq. (10) can be simplified to:

$$Q_{\mathrm{SET}}(W_d, W_f) \approx \frac{AW_d}{1 - \exp\left(\dfrac{-BW_d}{CW_d + DW_f + E}\right)}, \tag{16}$$

where A, B, C, D and E are parameters related to technology and circuit structure, and they are all positive numbers; W_d and W_f are equivalent channel width of drive transistors and load transistors, respectively. Because B is much larger than C, D and E, Eq. (16) can be expressed approximately as Eq. (17) when W_f takes the minimum value $W_{f,min}$:

$$Q_{\mathrm{SET}}(W_d, W_{f,\mathrm{min}}) \approx AW_d = V_T^* t_m k_g W_d. \tag{17}$$

For case A4, B2 and B3, Q_{SET} of vulnerable nodes is proportional to W_d approximately. W_f can be ignored because Q_{SET} is almost independent on it.

When W_d is very small, make:

$$\frac{-BW_d}{CW_d + DW_f + E} = S, \tag{18}$$

Equation (16) can be transferred to:

$$Q_{\mathrm{SET}}(W_d, W_f) \approx \frac{-A\dfrac{S\left(DW_f + E\right)}{SC + B}}{1 - \exp\left(S\right)}. \tag{19}$$

When W_d is much smaller than W_f, it can be considered that $W_d \to 0$, so $S \to 0$. According to Maclaurin expansion, Eq. (19) can be expressed as:

$$Q_{\mathrm{SET}}(W_d, W_f) \approx \frac{AS\left(DW_f + E\right)}{S^2C + SB} \sim \frac{A}{B}\left(DW_f + E\right), \tag{20}$$

where $A/B = V_T^*$. Constant E can be ignored as it is about 8∼9 orders of magnitude smaller than D. When W_d takes the minimum value $W_{d,min}$, Eq. (16) can be expressed as:

$$Q_{\mathrm{SET}}(W_{d,\mathrm{min}}, W_f) \approx AW_{d,\mathrm{min}} + V_T^* DW_f, \tag{21}$$

where $A = V_T^* t_m k_g$, and $D = k_{c2}$, take them to Eq. (21):

$$Q_{\mathrm{SET}}(W_{d,\mathrm{min}}, W_f) \approx V_T^* t_m k_g W_{d,\mathrm{min}} + V_T^* k_{c2} W_f, \tag{22}$$

where k_{c2} is a constant related to gate capacitance of load transistor; the product of t_m and k_g is about one order of magnitude larger than k_{c2}. From this, we obtain the approximate expressions of $Q_{\mathrm{SET}}(W_d, W_{f,min})$ and $Q_{\mathrm{SET}}(W_{d,min}, W_f)$.

If $Q_{\mathrm{SET}}(W_d, W_f)$ is a linear function with two unknown variables, it can be assumed:

$$Q_{\mathrm{SET}}(W_d, W_f) = aW_d + bW_f + c, \tag{23}$$

where a, b and c are constant. If the expressions of $Q_{\mathrm{SET}}(W_d, W_{f,min})$ and $Q_{\mathrm{SET}}(W_{d,min}, W_f)$ are known, then:

$$\begin{aligned} Q_{\mathrm{SET}}(W_d, W_f) = Q_{\mathrm{SET}}(W_d, W_{f,\mathrm{min}}) + Q_{\mathrm{SET}}(W_{d,\mathrm{min}}, W_f) \\ - Q_{\mathrm{SET}}(W_{d,\mathrm{min}}, W_{f,\mathrm{min}}). \end{aligned} \tag{24}$$

Therefore, as long as we can prove that $Q_{\mathrm{SET}}(W_d, W_f)$ is a linear function, we can get the expression. According to Eq. (10), Q_{SET} in case A4, B2 and B3 can be expressed as a function of W_d and W_f. Take technology parameters to the equation and obtain three-dimensional surfaces as shown in Fig. 2.

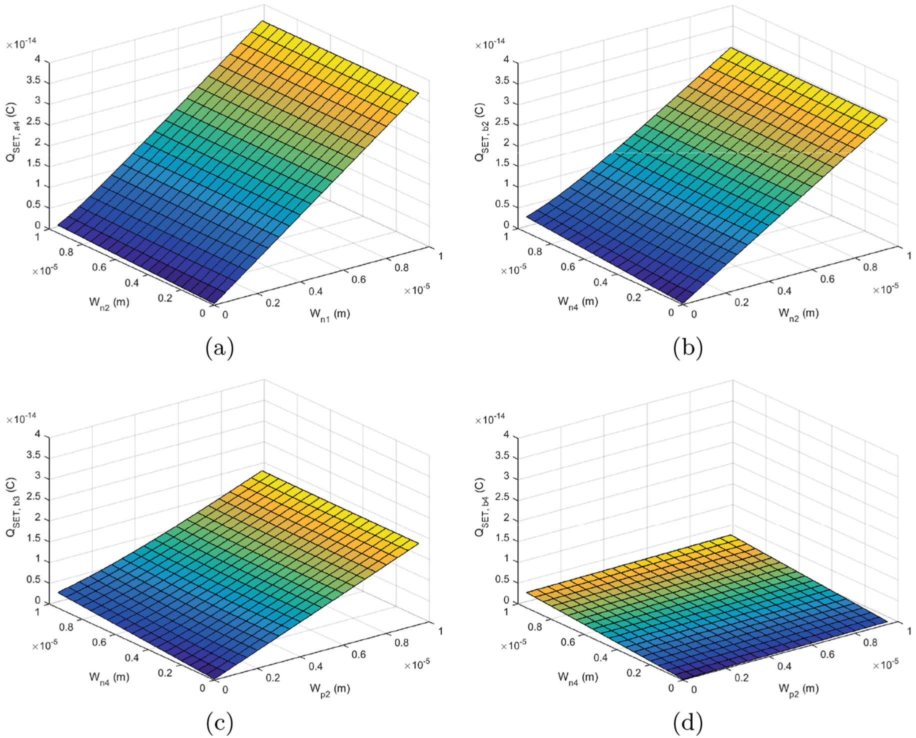

Fig. 2. Distribution of Q_{SET} in case (a) A4, (b) B2, (c) B3 and (d) B4.

According to Fig. 2, surfaces (a), (b) and (c) are nearly flat. In the approximate calculation, Q_{SET} can be roughly considered as a linear function of W_d and W_f. Thus:

$$Q_{\mathrm{SET}}(W_d, W_f) = V_T^* \left(t_m k_g W_d + k_{c2} W_f \right). \tag{25}$$

By now, an efficient model of Q_{SET} in the case of A4, B2 and B3 is obtained.

For case B4, the model in Eq. (15) is already linear. Assume the ratio of W_{p2} and W_{n2} is α, W_{p3} and W_{n4} is β. Q_{SET} for case B4 can be expressed as:

$$\begin{aligned} Q_{\mathrm{SET}} = \Big[&(k_{c0,p2} + k_{c0,n2}) + (\alpha k_{c1,p2} + k_{c1,n2}) W_{n2} \\ &+ (\beta k_{c2,p3} + k_{c2,n4}) W_{n4} \Big] (V_{DD} - V_{T,inv2}). \end{aligned} \tag{26}$$

In general, k_{c0} can be ignored as its magnitude far less than k_{c1} and k_{c2}. Let $\alpha k_{c1,p2} + k_{c1,n2} = k_{c1}$, $\beta k_{c2,p3} + k_{c2,n4} = k_{c2}$, $V_{DD} - V_{T,inv2} = V_T^*$, then:

$$Q_{\mathrm{SET}}(W_d, W_f) = V_T^* \left(k_{c1} W_d + k_{c2} W_f \right). \tag{27}$$

Thus, a simplified model of Q_{SET} for four cases is obtained. It is found that Eqs. (25) and (27) are identical except the coefficient W_d. In the case of A4, B2 and B3, Q_{SET} depends mainly on the switch threshold of fan-out logic, the conductance of drive transistor and the gate capacitance of load transistor. Q_{SET} in B4 is mainly determined by the switch threshold of fan-out logic, the diffusion capacitor of drive transistor and the gate capacitance of load transistor. In all cases, the Q_{SET} is proportional to the switch threshold of subsequent logic.

5 Experiment and Model Verification

SPICE simulations and error analysis were performed to verify vulnerability profile of dynamic circuits, proposed analytical model and efficient model.

Q_{SET} of vulnerable nodes were evaluated by current source injection. The benchmark experiment was performed in a 28 nm CMOS technology using a SPICE circuit simulation. The injected current source is given by the following equation [6]:

$$I(t) = \frac{Q}{T} \sqrt{\frac{t}{T}} \exp\left(-\frac{t}{T} \right), \tag{28}$$

where Q is charge collection due to energetic particles; T is the time parameter associated with technology. When the technology is determined, T is a constant.

Figure 3(a) shows the Q_{SET} distributions of the vulnerable nodes under various conditions in the current injection experiment. Results show that Q_{SET} of A4, B1, B2, B3, B4, and C1 are relatively small in all cases, and the experimental distributions are coincide with the soft error vulnerabilities profile analysis.

Figure 3(b) shows a Q_{SET} comparison of simulation and analytical model in case A4, B2, B3, and B4. x1 represents the minimum size domino inverter chain, and x4 and x8 represent the chain scaled by a factor of 4 and 8, respectively. The Q_{SET} trend calculated by analytical model conforms to the SPICE simulation results, and errors are very small. Errors could be caused by three factors: G_d and C_{tot} are approximations; t_m is slightly different from the actual situation; and V_T^* varies with the actual operating point.

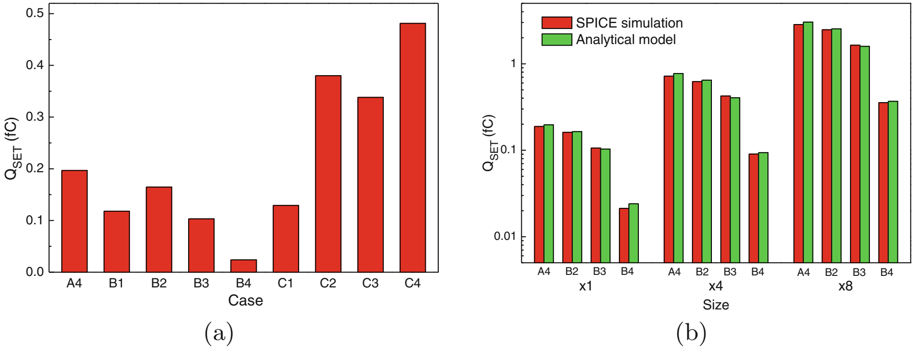

Fig. 3. (a) Q_{SET} distributions, (b) SPICE simulation and analytical model.

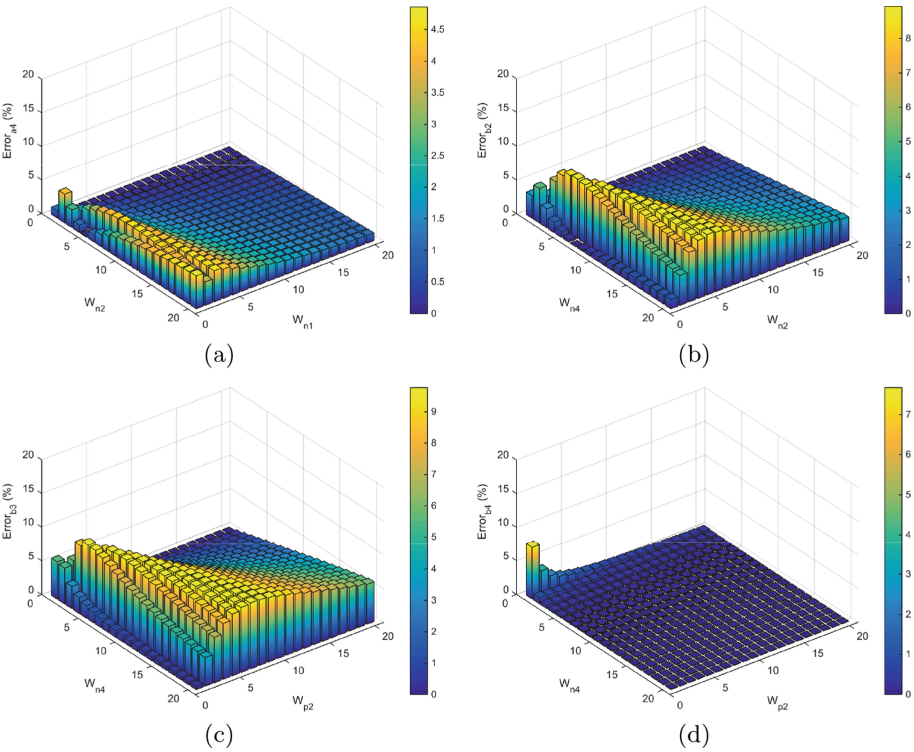

Fig. 4. Errors of efficient model in case (a) A4, (b) B2, (c) B3 and (d) B4.

To verify the accuracy of the simplified efficient model, results of the model were compared with the analytical model, and errors of the efficient model are analyzed. Figure 4 shows errors of Q_{SET} calculated by analytical model and efficient model of case A4, B2, B3 and B4 in 28 nm CMOS technology.

In Fig. 4, the widths of drive and load transistors are in the range from 50 nm to 10 µm. We choose 20×20 groups error data for every case. In four cases, the maximum errors of Q_{SET} are 4.86%, 8.82%, 9.65% and 7.68%, respectively. The average errors of Q_{SET} are 1.48%, 3.72%, 5.13% and 0.19% respectively, and the maximum error of all cases is less than 9.7%. The model can meet the general accuracy requirements in approximate calculation of manual or CAD tools.

6 Conclusion

The soft error vulnerability of dynamic circuits is analyzed and studied, and an efficient analysis model of soft error vulnerability is proposed. Firstly, the profile of soft error vulnerability in dynamic circuit is analyzed. Then a quantitative model of SET critical charges for vulnerable nodes of dynamic circuits is deduced. As the precise model is too complex, a reasonable approximation of the model is made according to the specific situation, and a simplified and efficient model for the critical charge of sensitive nodes in dynamic circuits is deduced. Finally, experimental verification and error analysis are performed. Experimental and analytical results show that the proposed model achieves high accuracy and can be used for efficient estimation of soft error vulnerability of dynamic circuits.

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