A Low TC Voltage Reference Generator Suitable for Low Temperature Applications

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Abstract. A low temperature coefficient (TC) CMOS voltage reference generator suitable for low temperature is proposed. It exploits temperature mutual compensation relationship between threshold voltage and thermal voltage, and provides a mean reference voltage of 692 mV. A proportional to absolute temperature (PTAT) current containing the thermal voltage which has a positive TC is generated, and then it is injected into a diode-connected NMOS transistor that supply the threshold voltage which has a negative TC. The mixing of the two voltages produces a reference voltage with zero TC. The proposed circuit is implemented with SMIC CMOS 0.18 um process technology. The simulation results show that the power consumption is 2.1 uW and the TC is 9.3 ppm/°C. The temperature range is from −75°C to 65°C, which indicates that the proposed circuit can be applied in low temperature environment.

Keywords: Voltage reference · Low TC · CMOS · Subthreshold voltage

1 Introduction

The IoT (Internet of Things) carries on the information exchange and the communication through internet, in order to realize the object recognition, localization, tracking, monitoring and management. RFID (Radio Frequency Identification) is the key technologies of the IoT that enable automatic identification and management of specific object in a variety of situations [1]. However, many RFID tags can not work well in many high latitudes because of low temperature. This leads to RFID applications being hindered in these regions. Therefore, it is necessary to develop a RFID tag suitable for low temperature applications.

Many voltage reference circuits were proposed. The most commonly used method is the bandgap voltage reference, where a CTAT (complementary to absolute temperature) source is balanced by a PTAT (proportional to absolute temperature) source, resulting in the silicon bandgap voltage as the reference voltage. Some advanced bandgap voltage references based on parasitic bipolar transistor with lower power consumption than the traditional bandgap reference is invented [2]. Meanwhile, voltage

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reference circuits based on the fact that the threshold voltage of transistor with different gate oxide thickness in the same CMOS technology exhibit different temperature characteristic is proposed [3], but it requires additional fabrication steps. Recently, the dependence of V_{th} with respect to the channel length is exploited in order to obtain different V_{th} is proposed [4], however, its temperature range is very small and is not suitable for low temperature environment. The subthreshold characteristics of transistors have been widely exploited in the field of reference voltage. In this way, voltage difference between the gate-source of two transistors operating in the subthreshold region were used to generate a PTAT voltage [5]. A novel voltage reference is introduced in [6, 7], it consists of standard transistors operating in subthreshold regime. It generates a threshold voltage with negative TC and a multiple of the thermal voltage with positive TC, and then adds them to produce a voltage reference with zero TC. But its temperature coefficients are not ideal.

In this work, we propose a novel voltage reference circuit. It generates a PTAT current containing the thermal voltage with a positive TC and then injected into a diode-connected NMOS transistor which supplies the threshold voltage with a negative TC to achieve an output voltage reference near zero TC. Simulation results show that this work has low TC and wide temperature range that from −75°C to 65°C. Thus it can be used in extremely cold conditions.

2 Circuit Design

The architecture of the proposed voltage reference generator is shown in Fig. 1. It consists of a current generator and an active load. The current generator formed by transistors number from M1 to M10 generates a PTAT current I_0. Such current is

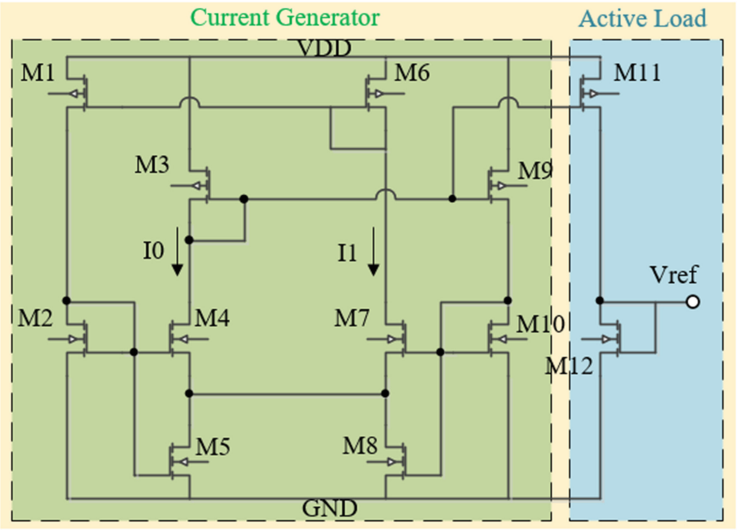

Fig. 1. The proposed circuit

injected into the active load that formed by M11 and M12 to generate the reference voltage V_{ref}. The current I_0 and the gate-source voltage of M12 that are dependence of temperature are compensate each other, then the V_{ref} is independence of temperature.

All the transistors except for M4, M5, M7 and M8 are operated in the saturation. The M4 and M7 are operated in the subthreshold region, and the M5 and M8 are operated in deep triode region. The core of the current generator circuit is represented by transistors M2, M4, M5, M7, M8 and M10, which determine the value of the current I_0. Meanwhile the current mirror consisted by M3 and M9 supply equal current I_0 in M4, M5 and M10, and the current mirror consisted by M1 and M6 supply equal current I_1 in M2, M7 and M8. It is a very important point in the design that the current I_0 and I_1 are equal by adjusting the parameters of the transistor. The current-voltage characteristic of a transistor that operates in the subthreshold region and in the subthreshold region can be approximated by (1) and (2), respectively.

$$I_D = \frac{\mu C_{ox}}{2} K (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS}) \tag{1}$$

$$I_D = KI \exp\left(\frac{V_{GS} - V_{TH}}{mV_T}\right) \times \left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right] \tag{2}$$

where K is the aspect ratio $(= W/L)$ of the transistor (W and L are the channel width and length), V_{GS} and V_{DS} are the gate-source voltage and the drain-source voltage, respectively. $I = \mu C_{ox}(m-1)V_T^2$, μ is the electron mobility in the channel, C_{ox} is the gate-oxide capacitance, $V_T = (K_B T/q)$ is the thermal voltage (K_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge), V_{TH} is the threshold voltage, λ is the channel length modulation coefficient, and m is the subthreshold slope factor. The gate-source voltages of M2 (M10) that operates in saturation with drain current I_1 (I_0) can be extracted from (1) and of M4 (M7) that operates in subthreshold with drain current I_0 (I_1) can be extracted from (2). Then we have,

$$\begin{cases} V_{GS4} - V_{th4} = mV_T \ln \dfrac{I_0}{K_4 I} \\ V_{GS2} - V_{th2} = \sqrt{\dfrac{2I_1}{\mu_n C_{ox} K_2}} \end{cases} \tag{3}$$

$$\begin{cases} V_{GS10} - V_{th10} = mV_T \ln \frac{I_0}{K_{10} I} \\ V_{GS7} - V_{th7} = \sqrt{\frac{2I_1}{\mu_n C_{ox} K_7}} \end{cases} \tag{4}$$

Where we neglect the channel length modulation of M2 and M10 since they are long channel devices. Meanwhile, we also can set the second square brackets in Eq. (2) to unity when $V_{DS} \geq 0.1V$ is met [7]. Obviously, because the source of M2 and M10 are grounded, and the source of M4 and M7 are connected with each other, the body effect plays no role and we have $V_{th4} = V_{th7}$ and $V_{th10} = V_{th2}$. By subtracting the upper from the lower in Eqs. (3) and (4), we can get the following two equations.

$$V_{GS2} - V_{GS4} = V_{th2} - V_{th4} + \sqrt{\frac{2I_1}{\mu_n C_{ox} K_2}} - mV_T \ln \frac{I_0}{K_4 I} \tag{5}$$

$$V_{GS10} - V_{GS7} = V_{th10} - V_{th7} + \sqrt{\frac{2I_0}{\mu_n C_{ox} K_{10}}} - mV_T \ln \frac{I_1}{K_7 I} \tag{6}$$

Because the drain of the transistor M5 and M8 are connected, the drain potential of them is equal. The left side of the Eqs. (5) and (6) equals the drain voltage of the transistor M5 and M8, respectively. Therefore, the right side of Eqs. (5) and (6) is equal. By subtracting (5) from (6), we can extract the expression of the current I_0.

$$I_0 = \frac{\mu_n C_{ox} m^2 V_T^2 \ln^2\left(\frac{K_7}{K_4}\right)}{2\left(\frac{1}{K_2} + \frac{1}{K_{10}}\right) - 4\sqrt{\frac{1}{K_2 K_{10}}}} \tag{7}$$

What we needs to be explained is that the two currents I_0 and I_1 are equal not realized by an electric current mirror, but by adjusting the parameters of the circuit. From Eq. (7) we can found some conditions need to be satisfied that it is $K_2 \neq K_{10}$ and $K_7 \neq K_4$. When the gate potential of M5 and M8 is different, the same drain current of the M2 and M10 and $K_2 \neq K_{10}$ can be satisfied at the same time. Obviously, the gate source voltages of M4 and M7 are also different. However, the drain currents of M4 and M7 are the same which make the condition $K_7 \neq K_4$ is established.

The current I_0 is then mirrored into the diode connected transistor M12 through M11 to get a temperature compensated reference voltage. The relationship between the drain current of M12 and the current I_0 can be obtained by M3 and M11. The transistor M12 operates in the saturation region and the reference voltage can be expressed as (8).

$$V_{ref} = V_{th12} + \left| mV_T \ln\left(\frac{K_7}{K_4}\right) \right| \sqrt{\frac{K_{11}}{K_{12} K_3 \left[\left(\frac{1}{K_2} - \frac{1}{K_{10}}\right) - 2\sqrt{\frac{1}{K_2 K_{10}}}\right]}} \tag{8}$$

The channel length modulation effect is mainly related to the drain source voltage and can be avoided by the diode-connected form. The best way to drastically reduce the channel length effect is to increase the parameter L. Thus, the channel length of all the transistors in the current mirrors and of M5, M8 must be quite large. Meanwhile, the drain-source voltage of M4, M7 which operate in the subthreshold region must be much large than the thermal voltage to eliminate the dependence of current on V_{DS} in (2).

3 Supply Voltage Dynamic Range

The minimum supply voltage is determined by the current generator circuit. In particular, we have to meet the condition that $V_{DS5} < V_{GS5} - V_{th5}$ to ensure the M5 operates in the deep triode region, and the drain-source voltage of M4 larger than

100 mV, and that M3 operates in saturated with $|V_{GS3}| > V_{th5}$. Consequently, the following expression has to be satisfied,

$$V_{DD} > |V_{GS3}| + V_{DS4} + V_{DS5} \tag{9}$$

Simulation results show that the supply voltage must be larger than 1 V in the SMIC 0.18 um CMOS process. Such voltage is also sufficient to ensure the M2 operates in the saturation region. The maximum supply voltage is determined by the maximum drain-source voltage allowed for M11, thus we have,

$$V_{DD} < |V_{DS11MAX}| + V_{ref} \tag{10}$$

Since the maximum drain-source voltage of a transistor is 1.8 V in the SMIC 0.18 um CMOS process. As a result, the maximum supply voltage of the circuit is about 2.5 V.

4 Temperature Compensation

As an approximation, we can consider that the temperature dependence of the threshold voltage can be given by (11).

$$V_{TH}(T) = V_{TH}(T_0) + \alpha(T - T_0) \tag{11}$$

where T_0 is the reference temperature which is $300°K$ and α is a negative value [8]. Substituting Eq. (11) and $V_T = K_B T/q$ in Eq. (8), the reference voltage V_{ref} can be rewritten as:

$$V_{ref} = V_{th12}(T_0) + \alpha(T - T_0) + \left| m\frac{K_B T}{q} \ln\left(\frac{K_7}{K_4}\right) \right| \sqrt{\frac{K_{11}}{K_{12}K_3\left[\left(\frac{1}{K_2} + \frac{1}{K_{10}}\right) - 2\sqrt{\frac{1}{K_2 K_{10}}}\right]}} \tag{12}$$

By differentiating (12) with respect to the temperature on can obtains,

$$\frac{\partial V_{ref}}{\partial T} = \alpha + m\frac{K_B}{q} \left| \ln\left(\frac{K_7}{K_4}\right) \right| \sqrt{\frac{K_{11}}{K_{12}K_3\left[\left(\frac{1}{K_2} + \frac{1}{K_{10}}\right) - 2\sqrt{\frac{1}{K_2 K_{10}}}\right]}} \tag{13}$$

As we can see from (13), the TC is independent of the carrier mobility which dependence of temperature. Thus, the temperature dependence of the mobility is suppressed due to the topological structure of the circuit. This leads to a smaller TC compared to the mobility is introduced at the reference voltage. By setting (13) to zero, we obtain the condition (14).

$$-\alpha = m\frac{K_B}{q}\left|\ln\left(\frac{K_7}{K_4}\right)\right|\sqrt{\frac{K_{11}}{K_{12}K_3\left[\left(\frac{1}{K_2}+\frac{1}{K_{10}}\right)-2\sqrt{\frac{1}{K_2K_{10}}}\right]}} \tag{14}$$

If (14) is satisfied, the Eq. (13) will be equal to zero for any temperature. As shown in Fig. 2, across the temperature from −75 °C to 65 °C, the total variation of the reference voltage is only about 0.9 mV and the TC is 9.3 ppm/°C which shows a good insensitivity to the temperature.

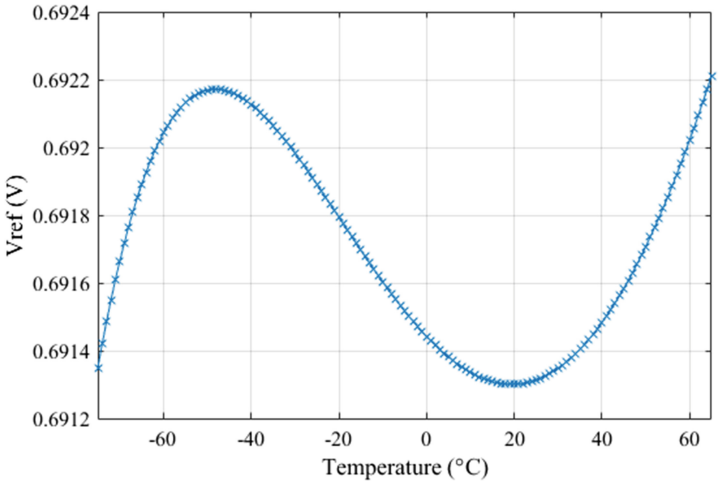

Fig. 2. The reference voltage V_{ref} versus temperature

5 Channel Length Modulation Effect

The Eq. (7) will be recalculated if we take the channel length modulation effect into account. The I-V characteristics of a MOS in the saturation region and in the sub-threshold region can be written as in (1) for $\lambda \neq 0$ and as in (2) for $\exp(-V_{DS}/V_T) \neq 0$. we only need to consider the channel length modulation effect on M4 and M7, because of M2 and M10 is diode-connected. Under such conditions, using the same procedure to recalculate the Eq. (7), the current I_0 is expressed by (15).

$$I_0 = \frac{\mu_n C_{ox} m^2 V_T^2}{2\left(\frac{1}{\sqrt{K_2}}-\frac{1}{\sqrt{K_{10}}}\right)^2}\ln^2\left[\frac{K_7}{K_4}\frac{1-\exp(-\frac{V_{DS7}}{V_T})}{1-\exp(-\frac{V_{DS4}}{V_T})}\right] \tag{15}$$

By using first-order Taylor series expansion to rewrite (15),

$$I_0 = I_{0NOM}\left[1+\ln\left(\frac{K_4}{K_7}\frac{V_{DS7}}{V_{DS4}}\right)\right]^2 \tag{16}$$

Where I_{0NOM} is the current I_0 when the channel length modulation effect is neglected $(\exp(-V_{DS}/V_T) = 0)$. By using (8) and (16), the reference voltage can be rewritten as (17).

$$V_{ref} = V_{ref0} + m\frac{K_B T}{q}\left|\ln\left(\frac{K_7}{K_4}\right)\right|\left|\sqrt{\frac{K_{11}K_2K_{10}}{K_{12}K_3}}\right|\frac{1}{\sqrt{K_{10}}-\sqrt{K_2}}\left(\left|1+\ln\left(\frac{K_4}{K_7}\frac{V_{DS7}}{V_{DS4}}\right)\right|-1\right) \quad (17)$$

Where V_{ref0} is the reference voltage calculated by (8). The drain-source voltage of M4 and M7 can be expressed by (18) and (19).

$$V_{DS4} = V_{DD} - \left|\frac{2I_0}{\mu_p C_{ox} K_4} + \left|V_{tp4}\right|\right| - V_{DS5} \quad (18)$$

$$V_{DS7} = V_{DD} - \left|\frac{2I_0}{\mu_p C_{ox} K_7} + \left|V_{tp7}\right|\right| - V_{DS8} \quad (19)$$

Where V_{tp} is the threshold voltage of a PMOS transistor. Because the drain terminal of M5 and M8 are connect with each other, we have $V_{DS5} = V_{DS8}$. By assuming that $K_4 = K_7$, then $V_{DS4} = V_{DS7}$. We can rewrite (17) as $V_{ref} = V_{ref0}$. Thus the channel length modulation effect can be compensated by setting $K_4 = K_7$ in the proposed voltage reference. Thanks to the topology used and to proper dimensioning, the channel length modulation is compensated, leading to a very good temperature coefficient.

6 Experimental Results

To verify the performance of the proposed design, we use the SPICE simulator to simulate the circuit with SMIC 0.18 um CMOS process. Measurements show that the proposed voltage reference generates a mean reference voltage of about 692 mV with a variation of 50 mV at all corner, when the temperature varies from −75 °C to 65 °C, as shown in Fig. 3. The PSRR (power supply rejection ratio), without any filtering capacitor, is −41.5 dB at 1 kHz and −31.3 dB at 10 MHz when VDD = 1 V, and decreases to −49.7 dB at 1 kHz and to −36.1 dB at 10 MHz when VDD = 1.8 V, as shown in Fig. 4. Figure 5 shows the output reference voltage versus VDD at all corner. With VDD ranging from 1 to 2.5 V, the measured line sensitivity is 1.9%/V at TT corner. In order to evaluate the sensitivity of the reference voltage to process variations, Monte Carlo analysis assuming WID mismatch variations in all MOSFETs were considered. Figure 6 shows the distribution of average output voltage V_{ref} at 1 V power supply. We assumed a Gaussian distribution (δ_{vth}) for the WID variation. The average voltage V_{ref} was about 691.7995 mV in this simulation. The coefficient of variation (δ/μ) in 30 runs was 0.48%. Figure 7 shows Monte Carlo simulation with 30 different samples of the reference voltage. Table 1 summarize the main performance of the proposed circuit and compares with previous works.

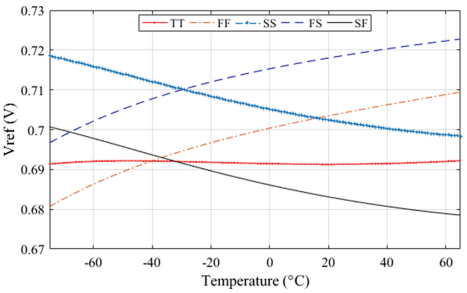

Fig. 3. Measured V_{ref} at all corners

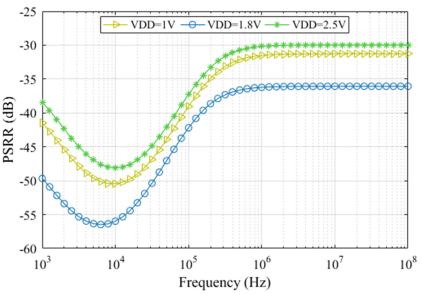

Fig. 4. The PSRR at different supply power

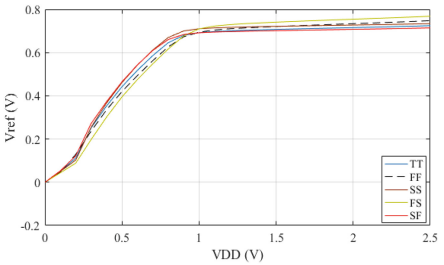

Fig. 5. The reference voltage V_{ref} versus voltage at all corner

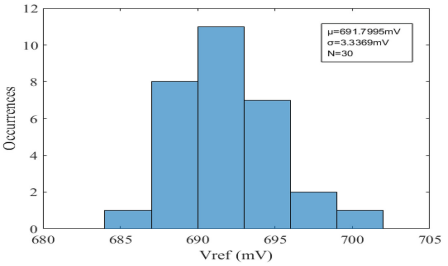

Fig. 6. Distribution of V_{ref} for 30-point supply Monte Carlo simulations

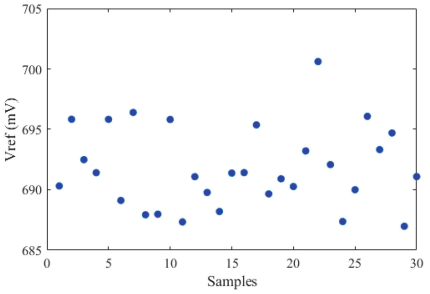

Fig. 7. Monte Carlo simulation with 30 samples

Table 1. Performance comparison

	[4]	[5]	[6]	[7]	This work
Supply voltage (V)	0.3–1.2	0.45–1.8	1–3	0.3	1–2.5
Technology (nm)	130	180	180	65	180
Power	7 pW	18.7 nW	0.23 uW	70 nW	2.1 uW
Vref (mV)	85	118.41	610	168	692
PSRR	−18 dB @100 Hz	−50.3 dB @100 Hz	−15.4 dB @10 MHz		−49.7 dB@1 kHz −36.1 dB@10 MHz
Temperature range (°C)	0–120	−40–85	−40–120	−20–100	−75–65
TC (ppm/°C)	17.4	59.4	66.9	142	9.3

7 Conclusion

A novel approach for low TC and wide temperature range voltage reference generator is presented. The proposed circuit has been implemented in SMIC 0.18 um CMOS process with the reference voltage of 692 mV. Due to the topology used and to proper dimensioning, channel length modulation and body effect are compensated, leading to a very good temperature coefficient of 9.3 ppm/°C. Monte Carlo simulation show a $\delta/\mu = 0.48\%$ spread for reference voltage, when considering both average process and mismatch variations. The circuit can work well under the temperature varies from −75 °C to 65 °C. This shows that the circuit can work in extremely cold high latitudes.

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References

1. Park, S.: A development of UHF RFID device for mobile IoT service. In: UEMCON 2016, pp. 1–7. IEEE (2016)
2. Sanborn, K., Ma, D., Ivanov, V.: A Sub-1-V low noise bandgap voltage reference. IEEE J. Solid-State Circuits **42**, 2466–2481 (2007)
3. Yang, Z., Jiang, M.: Nanopower CMOS voltage reference circuit with 16 ppm/°C from 0°C to 150°C without resistors. In: ICCE-TW, pp. 424–425. IEEE (2015)
4. de Oliveira, A.C., Caicedo, J.G.: 0.3 V supply, 17 ppm/°C 3-transistor picowatt voltage reference. In: LASCAS, pp. 263–266. IEEE (2016)
5. Zhu, Z., Hu, J., Wang, Y.: A 0.45 V, nan0-watt 0.033% line sensitivity MOSFET-only subthreshold voltage reference with no amplifiers. IEEE Trans. Circuits Syst. I Regul. Pap. **63**, 1370–1380 (2016)
6. Li, J., Li, J. and Yang, L.: A nanopower, high PSRR full CMOS voltage reference circuit consisting of subthreshold MOSFETs. In: ASICON, pp. 1–4. IEEE (2015)

7. Lu, T.C., Ker, M.D., Zan, H.W.: A 70nW, 0.3 V temperature compensation voltage reference consisting of subthreshold MOSFETs in 65 nm CMOS technology. In: VLSI-DAT, pp. 1–4. IEEE (2016)
8. Ueno, K.: A 300 nW, 15 ppm/°C, 20 ppm/V CMOS voltage reference circuit consisting of subthreshold MOSFETs. IEEE J. Solid-State Circuits **44**, 2047–2054 (2009)
9. Filanovsky, I.M., Allam, A.: Mutual compensation of mobility and threshold voltage temperature effects with application in CMOS circuits. IEEE Trans. Circuits Syst. I Fundam. Theory and Appl. **48**, 876–884 (2001)