An Optimized Design of Complex Multiply-Accumulate (MAC) Unit in Quantum Dot Cellular Automata (QCA)

G. Ambika, G. M. Shanthala, Preeta Sharan and Srinivas Talabattula

Abstract Multiply-accumulate (MAC) unit finds the large number of applications including computers and processors. In this chapter, we are implementing the optimized design of MAC unit using emerging nanotechnology called Quantum dot Cellular Automata (QCA). The multiplexer is the key unit in the design of MAC and we have achieved 34.78% reduction in total area in the design of multiplexer using QCA. As QCA has advantages such as reduced area and cell count, simulation time, less complexity with low power consumption, quality output with high efficiency is achieved.

Keywords QCA · Multiply-accumulate unit · Multiplexer

1 Introduction

CMOS technology played a vital role in the semiconductor industry in the past few decades by implementing very large-scale integrated devices. Due to the physical limits of this technology, researchers have switched to novel nanotechnology such as Quantum dot Cellular Automata (QCA), which is a top emerging technology

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with potential application in future computers. QCA is based on Coulombic interaction instead of the current used in CMOS with advantages such as high switching speed, extremely low power consumption without using transistors. QCA cell is the building block of QCA devices, which consists of four quantum dots with two mobile electrons.

The basic building block of QCA circuit is majority gate and using majority gate and inverter basic gates can be built. Complex logic circuits are constructed very easily with the help of QCA basic gates. In this chapter, we are implementing the design of 2:1 multiplexer using QCA which is the basic block of MAC. In real-time DSP systems, many applications such as speech codecs, MP3, etc., require MAC operations. In this chapter, we propose a new design methodology for 2:1 multiplexer using QCA Designer software with a decreased number of cells giving efficient output.

2 Quantum Dot Cellular Automata

The square nanostructure of electron wells which confines free electrons is basically called as QCA. Each cell constitutes four quantum dots, which are situated at the corners of a square coupled by means of tunneling barrier. As physical occupancy of quantum dots varies in nanometer range, they are capable of entrapment of electrons in three dimensions. Two electrons occupy nonadjacent corners representing two polarizations by Coulombic repulsion. Here, binary "Low" is represented by $P = -1$ and $P = +1$ represents binary "High". Figure 1a, b represents how charge designation of $P2$ is affected by its neighbor $P1$.

Majority gate is the basic unit of QCA which consists of five cells, three inputs, one output, and a middle cell. Middle cell is named as device cell as it determines

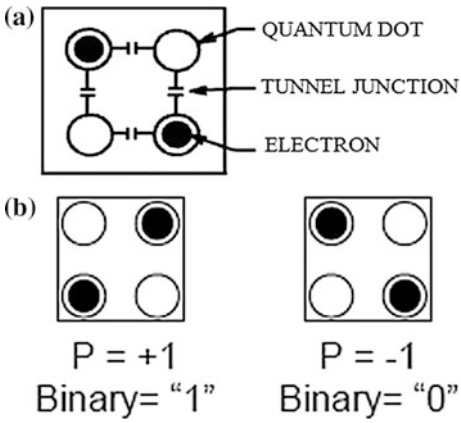

Fig. 1 **a** Basic quantum dot. **b** Polarization states

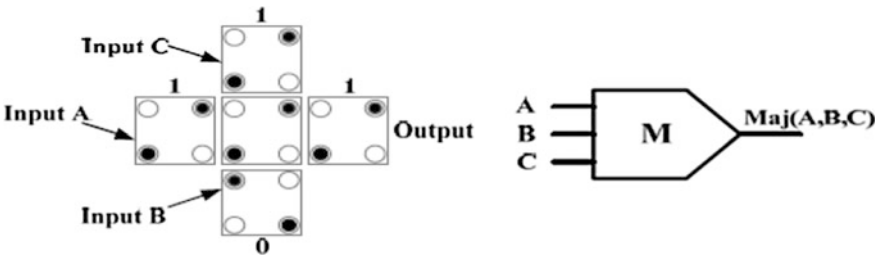

Fig. 2 Majority gate

the stable output by switching the device to major polarization. Using majority gate basic AND and OR gates can be designed by fixing one of the inputs to $P = -1$ or $P = +1$ respectively. Boolean expression for majority gate is represented as (Fig. 2):

$$\mathrm{M}(\mathrm{A}, \mathrm{B}, \mathrm{C}) = \mathrm{AB} + \mathrm{BC} + \mathrm{AC} \tag{1}$$

3 Design

Multiply-accumulate unit architecture is as shown in Fig. 3, which mainly consists of several 2:1 multiplexers. We are implementing 2:1 multiplexer which uses less area with high switching speed and low power consumption, which will lead to efficient MAC design.

The basic functional block of 2:1 multiplexer is as follows (Fig. 4).

Output of the multiplexer is based on select input. 2:1 multiplexer consists of two inputs A and B, depending upon the select line either A or B is produced at the output. Truth table is represented in Table 1, using this output expression can be given as

$$\mathrm{C} = \mathrm{A.SEL}' + \mathrm{B.SEL} \tag{2}$$

Majority gate implementation of 2:1 multiplexer is represented as (Fig. 5).

Using QCA Designer 2.0.3 multiplexer design is implemented which is the basic block for MAC unit. This design is very efficient compared to previous designs in terms of number of cells and area usage (Fig. 6).

The proposed design is compared with the previous designs and results are tabulated and plotted as (Table 2; Fig. 7).

This design is compared with the classical logic gate design and it is summarized as follows (Table 3; Fig. 8).

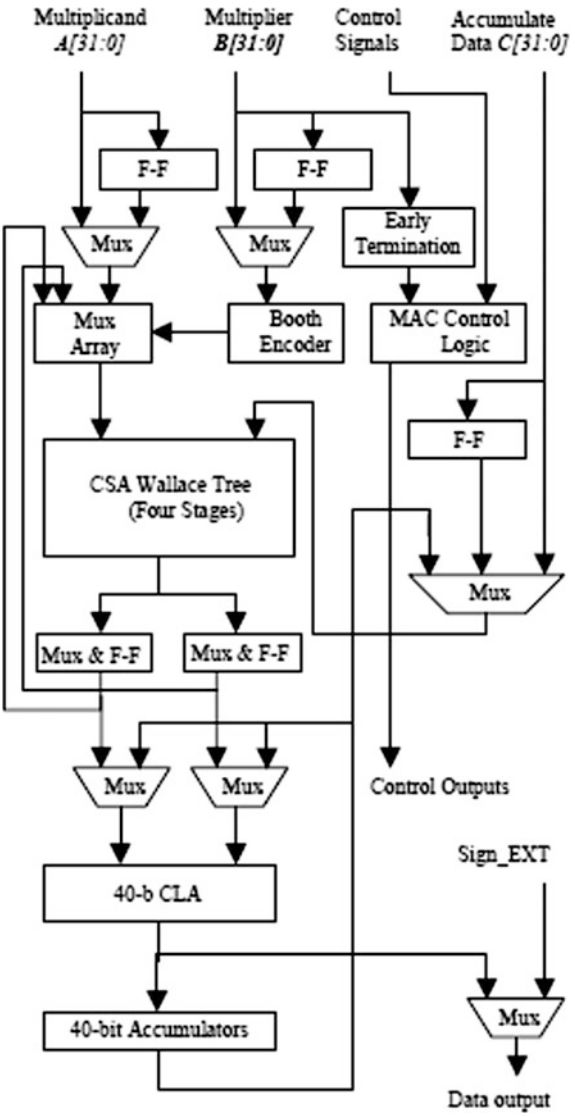

Fig. 3 MAC architecture

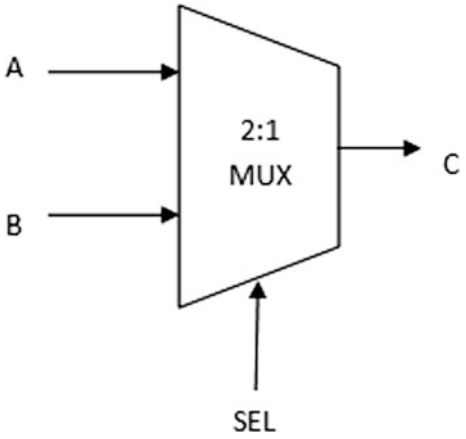

Fig. 4 Functional block of 2:1 multiplexer

Table 1 Truth table of 2:1 multiplexer

Select I/P = SEL	O/P = C
0	A
1	B

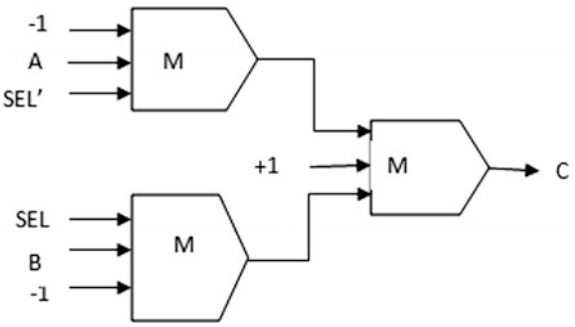

Fig. 5 Outline of the proposed 2:1 multiplexer

4 Simulation Results

Circuit functionality is verified using QCA Designer 2.0.3 [1]. Following parameters are used for bistable approximation:

- Number of samples = 12,800
- Convergence tolerance = 0.00100

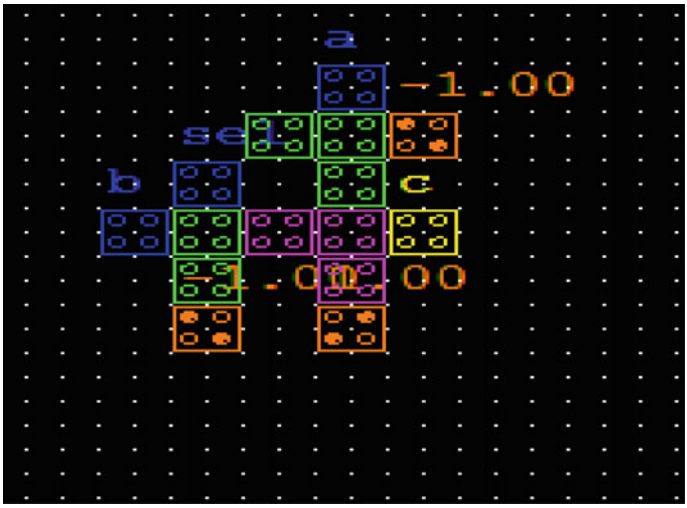

Fig. 6 Layout of 2:1 multiplexer in QCAD

Table 2 Comparison of the proposed design with some previous designs

Parameters	2:1 mux as in paper [2]	2:1 mux as in paper [3]	2:1 mux as in paper [4]	2:1 mux as in paper [5]	2:1 mux as in paper [6]	Proposed design
No. of cells	63	49	31	27	23	15
Area of cells (sq nm)	28,512	14,904	37,908	23,328	18,144	13,688
Total area (sq μm)	0.14	0.08	10,044	8748	7452	4860
Input to output delay	Seven clock zone	Four clock zone	Five clock zone	Four clock zone	Four clock zone	Four clock zone

- Radius of effect = 65 nm
- Cell size = 35 nm
- Relative permittivity = 12.9
- Clock high = 9.8e−22
- Clock low = 3.8e−23
- Clock amplitude factor = 2 (Fig. 9).

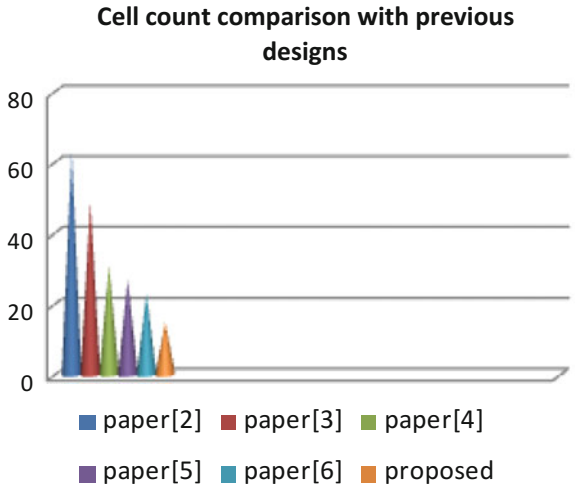

Fig. 7 Cell count comparison graph

Table 3 Comparison of cell area in the design of multiplexer using logic gates and QCAD

	Logic gates	QCAD
Cell area (sq μm)	100	0.02

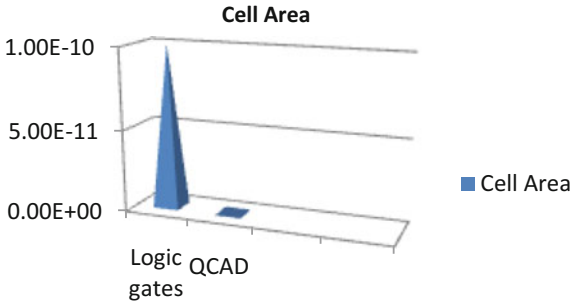

Fig. 8 Cell area comparison of QCAD result with logic gates

Simulation results shown above give the working of 2:1 multiplexer and this design is used for MAC architecture.

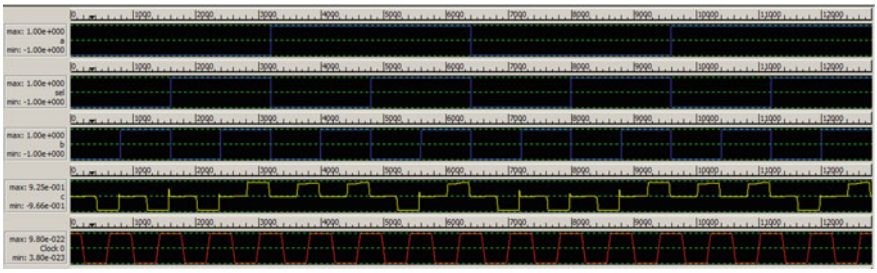

Fig. 9 Simulation results

5 Conclusion

Our proposed design of multiplexer is very simple and efficient with a remarkable reduction in the number of cells and is utilized in the architecture of MAC unit which has a large number of applications including future computers. As the design is implemented in QCA, we achieve advantages such as reduced cell area by 34.78% and it uses only 15 cells with high switching speed and low power consumption giving more efficient output when compared to previous designs. Hence, our proposed design is the promising step toward the goal of low power design.

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