A Low Power, Frequency-to-Digital Converter CMOS Based Temperature Sensor in 65 nm Process

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Abstract. A low power all CMOS based smart temperature sensor is introduced without using any bandgap reference or any current/voltage analog-to-digital converter. With the intention of low cost, power and area consumption, the proposed temperature sensor operates in sub-threshold region generating a temperature dependent frequency from the proportional to absolute temperature current. A digital output is obtained from the temperature dependent frequency by using a 12-bit asynchronous counter. A temperature insensitive ring oscillator is designed used a reference clock signal in counter. The temperature sensor is implemented using 65 nm CMOS standard process and its operation is validated through post-layout simulation results, at a power supply of (0.5–1)-V. The sensor has an uncalibrated accuracy of +2.4/–2.1 °C for (–55 to 125) °C and a resolution of 0.28 °C for the same range. The power and area consumed by the sensor is 1.55 μW and 0.024 mm^2 respectively.

Keywords: Calibration · Counter · Low power · PTAT · Temperature sensor
Temperature insensitive ring oscillator

1 Introduction

Due to the progression in pervasive computing, internet of things (IoTs) and the increase in demand of portable and miniature electronic devices, demand of low-cost, high performance temperature sensor is increased. The aggressive scaling techniques and increased transistor integration results in amplified junction temperature gradient. These junction temperature variations affect the lifetime, performance and reliability of the electronic device by increasing the leakage power, timing issues, gate delay, self-heating and the overall cost [1]. Temperature sensors have become an important element in every system on chip (SoC), especially the on-chip temperature sensors, mostly because of their compactness, low cost, high performance and low power consumption. The low power consumption helps in mitigating the self-heating issues of these sensors. The on-chip temperature sensors are mostly used for thermal compensation and power consumption control in SoCs.

Different types of temperature sensors have been realized in CMOS technology. The conventional block diagram of sensor with its interface is shown in Fig. 1.

B. K. Kaushik et al. (Eds.): VDAT 2017, CCIS 711, pp. 657–666, 2017.
https://doi.org/10.1007/978-981-10-7470-7_62

A conventional temperature sensor is designed using bipolar junction transistors (BJTs) [2]. The BJT based temperature sensors measure the temperature by comparing the temperature independent voltage with a temperature dependent voltage. These two voltages are created using the characteristics of a vertical PNP voltage [3–6]. The ratio between the proportional to absolute temperature (PTAT) and the reference voltage is fed to an analog to digital converter (ADC) for digital output. The BJT based temperature sensors are able to achieve good resolution with high precision data converters, but result in more sensing errors. In order to mitigate the error, complex calibration techniques involving dynamic element matching (DEM) and chopping techniques are used making the output interface bulky and increasing the overall cost [2]. This resulted in tradeoff between sensing error, power consumption and sensor size. Moreover, the compatibility issue of BJT with CMOS technology increased the overall cost of the sensor. To overcome these issues, metal-oxide-semiconductor (MOS) based temperature sensors are introduced [7–16]. These sensors mostly exploit the thermal dependency of threshold voltage or leakage current of MOS devices. The output of MOS based sensors is usually temperature dependent current, voltage or frequency, with a typical accuracy of ±2 °C [2].

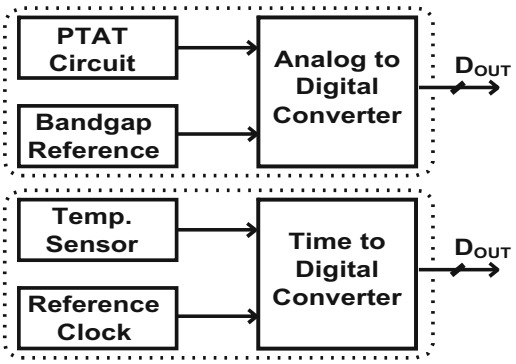

Fig. 1. Conventional ADC and TDC based temperature sensor [2].

In this paper, a current-mode MOS based temperature sensor is introduced without using any BJTs. It employs a PTAT frequency generator, operating in sub-threshold region for low power operation, and a low power temperature insensitive ring oscillator (TIRO) used as a reference clock signal for counter. The output of both the temperature sensor and the TIRO is given to a 12-bit asynchronous counter for digital output. The sensor, realized in 65 nm CMOS standard process, results in high resolution, small size and power consumption and is compatible with common CMOS process. The temperature sensor results in an average temperature resolution of 0.28 °C over the military range (–55 °C to 125 °C) and has an uncalibrated inaccuracy of +2.4/–2.1 °C for the same temperature range.

The rest of the paper is organized as follows. Section 2 discusses the block diagram and working principle of the proposed temperature sensor followed by the operation of

different sub-blocks. The operation of the sensor is validated through post-layout simulations in Sect. 3. Finally, Sect. 4 presents the conclusion.

2 Proposed CMOS Based Temperature Sensor

The block diagram of the proposed temperature sensor is shown in Fig. 2. The different blocks of the temperature senor are: A PTAT current generator, reference current generator, a temperature insensitive ring oscillator and a 12-bit asynchronous counter. The sensor employs the concept of current to frequency translation, where the proportional to absolute temperature current (I_{PTAT}) generates a temperature dependent frequency at the capacitor output. The frequency variation due to temperature is given to the counter and a digital output is achieved with respect to the clock frequency of ring oscillator An *Enable* switch is used to reduce the static power consumption.

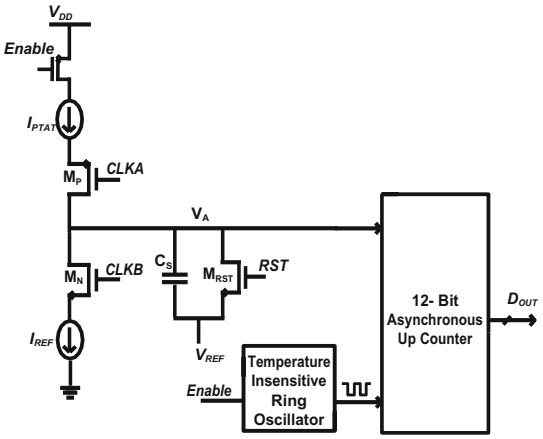

Fig. 2. Block diagram of temperature sensor.

2.1 Temperature Sensor Core

The schematic of the proposed temperature sensor is shown in Fig. 2. The reference current (I_{PTAT}) charges the capacitor (C_S) to voltage (V_A) with a slope of I_{PTAT}/C_S, whereas the PTAT current (I_{PTAT}) discharges the C_S with a slope of I_{REF}/C_S. The PTAT current generator operating in sub-threshold region is adopted from [10], where the switched capacitor circuit is replaced by a resistor and a startup-circuit is added. The rate of charging and discharging of C_S translates a varying waveform in time corresponding to temperature variations, as given by:

$$V_{A,max} - V_{REF} = (I_{PTAT}/C_S) \times t_r = (I_{REF}/C_S) \times t_f \quad (1)$$

where $V_{A,max}$ is the maximum value of V_A and V_{REF}, C_S, t_r and I_{REF} are considered as constants. Therefore, from Eq. (1):

$$t_r \propto I_{PTAT} \propto T \tag{2}$$

where T is the temperature (°C). Moreover, from Eq. (1), the C_S has a negligible effect on the current charging and discharging as $I_{PTAT} \times t_r = I_{REF} \times t_f$. Therefore, the accuracy of the temperature sensor is insensitive to capacitor variation. The clock signals CLKA, CLKB and RST are generated from the CLK signal. The RST is used as C_S reset signal. The timing diagram of all clock signals and the charging and discharging of C_S at different temperatures (T_1, T_2, T_3 and T_4) is shown in Fig. 3 and the

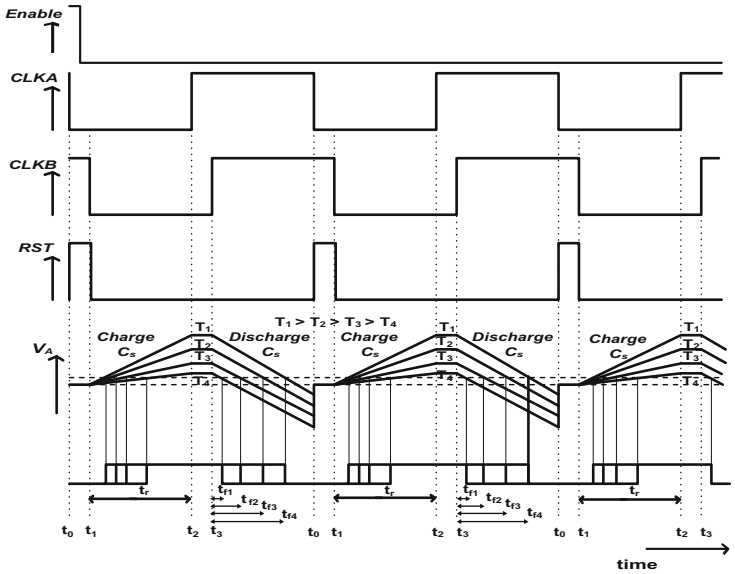

Fig. 3. Timing diagram of different signals.

Table 1. Operation of temperature sensor at different clock phases.

Time interinterval	Clock signal	Operation
During t_0-t_1	RST = HIGH	$V_A = V_{REF}$
At t_1	Falling edge of RST	C_S is charged by I_{PTAT}
At t_2	Rising edge of CLKA	M_P = OFF; Charging of C_S stops
During t_2-t_3	CLKA = HIGH	C_S holds on the charge, making V_A constant
At t_3	Rising edge of CLKB	M_N = ON; I_{REF} sinks to discharge C_S
During t_3-t_0	CLKB = HIGH	Conversion is done; Output holds a digital value

operation is explained in Table 1. As the absolute temperature (T) and t_f have linear relationship, the output count-value of counter represents the absolute temperature.

2.2 Temperature Insensitive Ring Oscillator

The TIRO, adopted from [17], consists of five stages, where each stage composed of a bootstrap circuit and a driver stage. The schematic of TIRO is shown in Fig. 4. The transistors M_{P2} and M_{N2} are used as switches controlled by the input signal (V_{IN}). The capacitors C_{BP} and C_{BN} behave as bootstrap circuit and are pre-charged by transistors MP1 and MN1, respectively. The INV_N and INV_P perform as drivers. To reduce the static power consumption, a NAND gate is employed at the first stage to prevent the unnecessary oscillations. The bootstrapped inverter gives an output swing of $-\beta V_{DD}$ to $2\ \beta V_{DD}$, where β is the boosting efficiency and V_{DD} is the power supply. The increase in the swing improves the driving capability of the transistors M_{P2} and M_{N2} and that of driver stage, so that a high frequency can be attained near the threshold voltage region. Besides the advantages highlighted in [17], this bootstrapped ring oscillator (BTRO) can be used as TIRO, if designed carefully. At a power supply approximately equal to the threshold voltage of MOS transistors, the BTRO operates in sub-threshold or linear

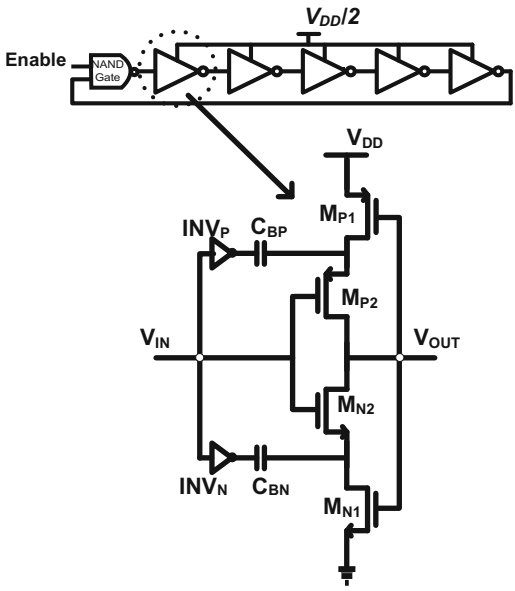

Fig. 4. 5-stage TIRO [17].

region during the turned-on transient. Therefore, for one period of oscillations, the BTRO has two operating behaviors during the tuned-on transient operation. The period of BTRO remains invariant with temperature due to the opposite temperature behavior during the tuned-on transients.

The total delay (τ_{total}) of a single stage TIRO is given as:

$$\tau_{total} = \tau_{lin} + \tau_{sub} \tag{3}$$

where τ_{lin} and τ_{sub} are the delay in linear and sub-threshold region, respectively. Considering, the current flowing in both the linear and sub-threshold region are equal, therefore the driving capability of both nMOS and pMOS transistors is same. Then, the τ_{total} is given as:

$$\tau_{total} = \frac{k_f.C_L.(V_{DD} - V_o)}{\mu.C_{dep}.W/L.V_T^2.\exp(\frac{V_{DD}-V_{TH}}{nV_T})} + \frac{C_L(V_o - V_{50\%})}{\mu.C_{ox}.W/L.(\beta 2V_{DD} - V_{TH})} \tag{4}$$

where C_{dep} and C_{ox} are the depletion and oxide capacitors, μ is the effective mobility, W/L is the aspect ratio of the transistors and k_f is the fitting parameter.

2.3 Counter

The frequency signal generated from the temperature sensor converted into digital output through asynchronous counter. The TIRO is used as a reference signal for the counter. The size of the counter is chosen so that it does not overflows the countvalue, mostly at high temperatures. Although more bits can be added to the counter but it increases the static power and will also impact the dynamic power, as the most significant bit (MSB) switching activity is small. A 12-bit asynchronous counter is realized using JK flip-flops, AND gate and buffers, as shown in Fig. 5.

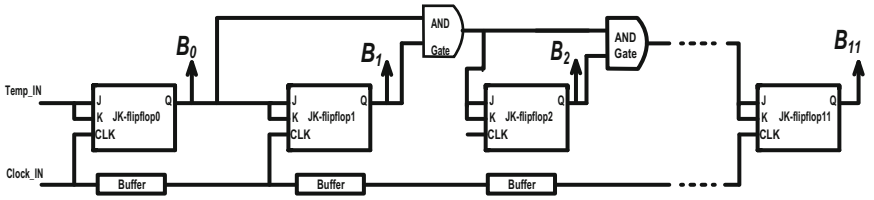

Fig. 5. 12-bit asynchronous counter.

3 Post-layout Simulation Results

The proposed temperature sensor is realized in 65-nm CMOS process, at (0.5–1) V power supply, and its operation is validated through post-layout simulation results using Cadence IC617 environment. The total area consumed by the sensor (excluding the input/output pads) is 0.024 mm^2, as shown in Fig. 6.

The variation of power consumption with respect to temperature (−55 °C to 125 °C) is shown in Fig. 7. The sensor consumes a power of 1.55 µW at room temperature. The variation of VPTAT with temperature is shown in Fig. 8. It is concluded that the slope of the VPTAT varies almost by 50% with rise in temperature.

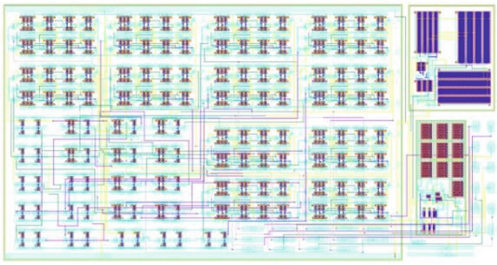

Fig. 6. Layout of the proposed temperature sensor.

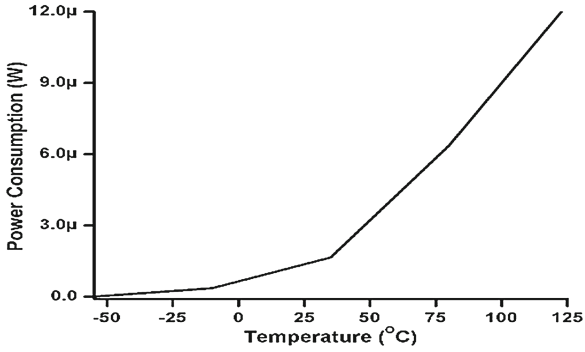

Fig. 7. Variation of power consumption with temperature.

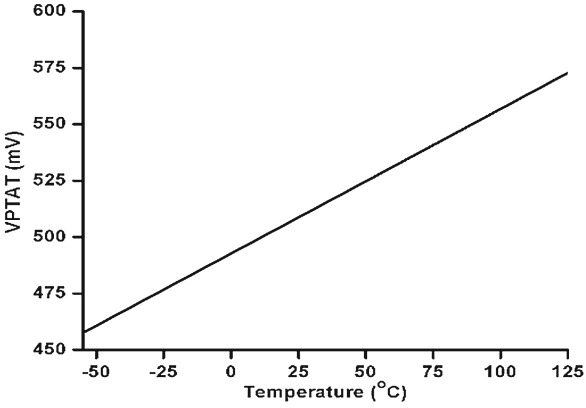

Fig. 8. Variation of VPTAT with temperature.

The variation of the reference clock signal used at the counter with temperature is shown in Fig. 9. As can be seen, the TIRO has a frequency of 50 kHz at room temperature and varies within ±10% of the clock frequency over the defined temperature range.

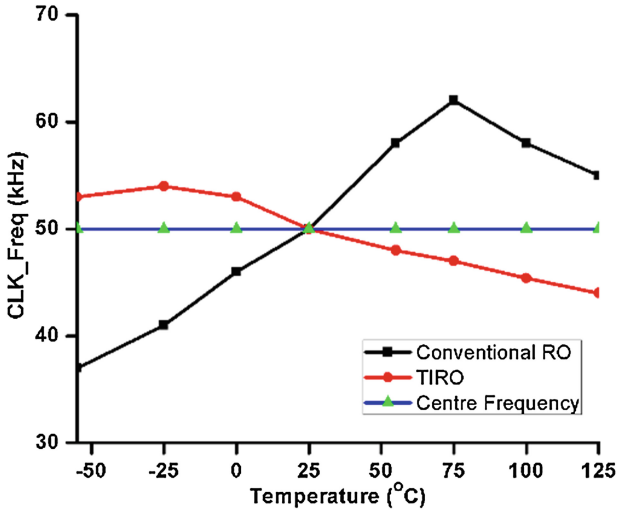

Fig. 9. Transient response of TIRO.

The characteristic plot of asynchronous counter is shown in Fig. 10. The count value is taken with respect to a calibration table. As the results are based on post-layout simulation, the actual calibration issues weren't dealt. The sensor has an uncalibrated accuracy of +2.4/–2.1 °C and a resolution of 0.28 °C. Then from the linear fitting curve for a value of R^2 = 0.9978, the temperature value is translated from the count value as:

$$Temperature = -0.285 \times count_{value} + 395.3 \tag{5}$$

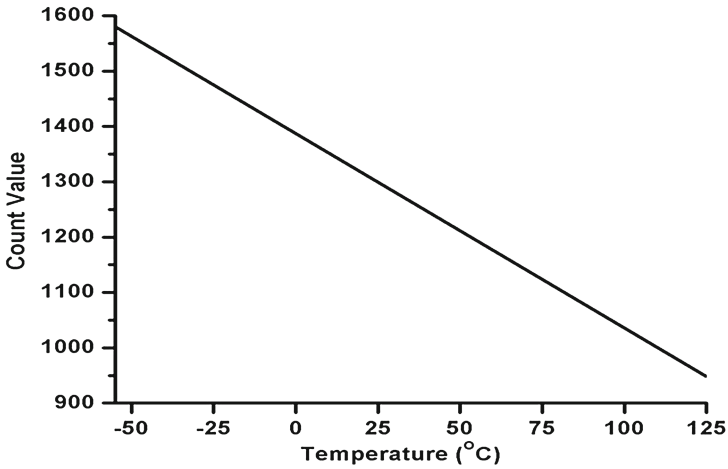

Fig. 10. Count characteristics for the temperature sensor.

Table 2. Performance comparison with related works.

This Work[a]		[11]	[12][a]	[15]	[16]
Year	2017	2010	2014	2013	2013
Sensor type	Temperature to frequency	Temperature to pulse	Temperature to frequency	Temperature to pulse	Temperature to pulse
Temperature range [°C]	−55 to 125	0 to 90	−50 to 125	0 to 100	−40 to 110
CMOS technology [nm]	65	350	65	350	65
VDD [V]	0.5–1	3.3	0.3–1	2.7–3.3	1.2
Resolution [°C]	0.28	0.05	————	0.2	0.34
Calibration	Two	Two	————	Two	One
Accuracy [°C]	+2.4/–2.1[b]	±0.6	±0.8	+1.0/–0.8	+2.7/–2.9
Power consumption [μW]	1.55	27.5	3.7	1.5	400
Area [mm^2]	0.024	0.25	————	0.025	0.0013

[a]Post-layout simulation results
[b]Uncalibrated accuracy

4 Conclusion

In this paper, a low power, frequency to temperature based CMOS smart temperature, operating in sub-threshold region for a temperature range of –55 °C to +125 °C, is introduced in 65-nm CMOS process. The proposed temperature sensor employs two current sources: ideal and proportional to absolute temperature. Based on the charging and discharging of capacitor due to these two current sources with temperature, a varying frequency is generated. A 12-bit asynchronous counter is used for analog-to-digital conversion. The counter uses a slow reference clock of 50 kHz, generated on chip by employing a five stage temperature insensitive ring oscillator. The overall temperature sensor consumes a power and area of 1.55 μW and 0.024 mm2, respectively. The sensor achieves a resolution of 0.28 °C and an uncalibrated accuracy of +2.4/–2.1 °C for a temperature range of –55 °C to +125 °C. To improve the resolution and accuracy of the temperature sensor, vernier time to digital converter or analog-to-digital converter and dynamic element techniques or autozeroing techniques can be employed (Table 2).

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