A 10T Subthreshold SRAM Cell with Minimal Bitline Switching for Ultra-Low Power Applications

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Abstract. High noise margins and low power dissipation are the major attributes of the SRAM cells used in ultra-low power applications. This paper proposes a 10T Static Random-Access memory (SRAM) with data aware dynamic feedback control and disturb free read which enhances the noise margins in the sub-threshold region. Exploiting the dynamic threshold MOS transistors (DTMOS) technique reduces the read access time of the proposed memory cell. As this cell offers single ended write operation with the bitlines kept at logic HIGH which leads to large saving in dynamic power due to charging/discharging operation on bitlines. Therefore, proposed SRAM reduces the activity factor of discharging the bitlines for each write pattern. The simulation has been carried out in 65 nm technology node to show the comparison among the existing techniques and proposed cell. The proposed memory cell has write static noise margin (WSNM) of 1.7x and 1.48x compared to iso-area 6T and Schmitt Trigger based (ST2) SRAM cells respectively at supply voltage of 300 mV. Read operation is data controlled which improves the read margin. Dynamic threshold technique increases read current for faster read operation. Read SNM is 2x, 1.16x and 1.4x of iso-area 6T, differential data aware 9T and Schmitt trigger SRAM (ST2) respectively. These features enable the cell for ultralow power applications.

Keywords: Activity factor · Dynamic power · SRAM · Subthreshold
Write margin

1 Introduction

Memory occupies major portion of chip area. It is anticipated that the memory area will increase further in future version of mobile electronic devices, high-end processor and microcontrollers. In order to increase the battery life of mobile devices, low power memory design is essential. Operating the memory in the sub-threshold region of the transistor can lead to significant reduction of power consumption due to the reduction of dynamic power, gate leakage and standby current of the design. Hence, sub-threshold memory is one of the viable option to achieve low power dissipation. Quadratic reduction in dynamic power and linear reduction in leakage power with respect to supply voltage can be achieved in subthreshold memory cell [1]. As reported in [2], 60% of the dynamic power in memory is due to the charging and discharging of the bitlines during

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write operation. Reducing this dynamic power consumption will significantly improve the battery life of mobile devices.

In the subthreshold region, the data stability of memory cell is severely affected due to (1) the reduction in on-current to off-current ratio (*Ion/Ioff*), (2) local threshold voltage variation and (3) reduction in supply voltage [3]. The traditional 6T Static Random-Access Memory (SRAM) cannot behave properly under such stringent constraints. Several read and write assist techniques have been proposed to improve read and write stability of 6T SRAM which include virtual-ground (CVSS) bias [4, 5], differential CVSS [6], boosted [7] or reduced wordline voltage [7], dual supply scheme [8, 7], and write back schemes [4]. Even with these techniques, the V_{min} (minimum operating voltage) of 6T SRAM lies in the range of 0.45 V to 0.7 V.

Several architectures have been proposed in recent years that aim to increase the write and read stability by increasing number of transistors used by making one or more design modifications. Breaking the feedback between the inverters during write/read stage increase write/read stability as in 7T [9] and 7T [10] cells. However, the stability depends on the transistor that controls the feedback loop. Due to the impact of process variation, feedback may fail to work which leads to marginal benefit in cell stability. 8T [11] isolates storage nodes from the bitlines by inserting buffer between bitlines and storage nodes which improves read stability. However, the write margin remains low and read access delay is increased. The half select stability failure is one of the major issues of that work.

Several techniques to save dynamic write power have been proposed that includes reducing the voltage swing of bitlines and capacitance [12, 13]. In [13], extra logic circuitry in row decoder and DC-to-DC converters are used to precharge and discharge the bitlines which leads to increase in area, reduction in speed and noise margins. Reducing the capacitance of bitlines and wordlines and datalines leads to saving in dynamic write power of the SRAM cell.

In this paper, a new 10T subthreshold SRAM cell is proposed that provides high noise margins and reduced dynamic power dissipation without extra logic circuitry. The major contributions of the paper are as follows:

- The proposed 10T cell reduces the activity factor of SRAM cell to almost *'0'* during write operation by keeping both the bitlines at logic high value for write operations. The data to be written is managed by *WBL* and *WBLB* control signals.
- Read operation is disturb free by isolating storage nodes from bitlines. DTMOS (Dynamic threshold MOS) technique [14] in read operation reduces threshold voltage for faster read operation.
- As the read and write access transistors are different. They can be sized efficiently to improve the read and write SNMs.
- Leakage current is reduced due to stacking of pull down transistors in read and hold state. Symmetric structure offers symmetric layout and lower mismatch.
- Half select issue arising due to *BL* and *BLB* is reduced.

2 Proposed 10T SRAM Cell Design

To achieve higher noise margins and minimum dynamic power consumption, a 10T SRAM cell is designed as shown in Fig. 1. The transistors *M7*, *M8*, *M9* and *M10* have been added to the conventional 6T cell. The transistor *M11* is common to all the SRAM cells in a row. The transistors *M1–M5–M7* and *M2–M6–M8* form two cross coupled inverter pairs. The transistors *M3*, *M4* and *M9*, *M10* act as access transistors for the write and read operations respectively. The symmetric layout structure is drawn to reduce the impact of local process variations. The structure uses the *LE* and *RE* signals to control the transistors *M7* and *M8* which breaks the feedback between inverters using dynamic feedback control. It increases the write margin. *RWL* and *WBL*, *WBLB* signals control the read and write operations respectively. The write operation in the cell exploits write assist dynamic feedback control technique. Even there are two bit-lines, the write operation is functionally single ended. The bit-lines are kept at high value during both write '*0*' and write '*1*' operations. *M9* and *M10* work as switches, only one of them is on during one write operation transferring data to adjacent node and other node value is changed due to inverting operation of another inverter attached to that node. Since bit-line values are never changed and write operation is controlled by switches according to the data to be written power consumed in switching bitlines is fully saved. Read operation is differential and controlled by data stored. Hence read is disturb free leading to higher read margin equivalent to hold margin. The status of the control signals is shown in Table 1.

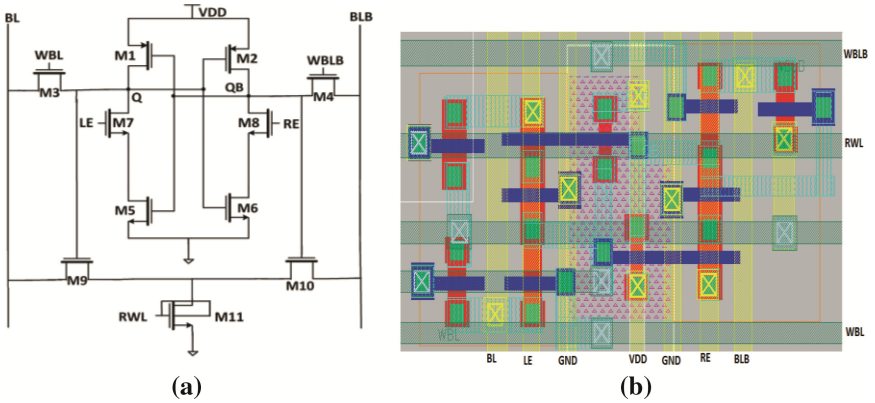

Fig. 1. (a) Proposed 10T SRAM Cell (*M11* is common to all the SRAM cells in a row) (b) Layout of Proposed design

Table 1. Truth table for proposed design

	RWL	*BL*	*LE*	*RE*	*BLB*	*WBL*	*WBLB*
Write 1	0	1	0	1	1	1	0
Write 0	0	1	1	0	1	0	1
Read	1	1	1	1	1	0	0
Hold	0	1	1	1	1	0	0

2.1 Write Operation

Unlike the conventional SRAM cells, both the bit-lines *BL* and *BLB* are kept high during write operation. In contrast to general writing pattern of SRAM, where data to be written is controlled by values on *BL* and *BLB*, it is controlled by control signals *WBL* and *WBLB* in this proposed SRAM cell. The write operation in the proposed SRAM cell is single ended that is one access transistor is used to write desired value and other one is *OFF*.

For writing '*1*' to the SRAM cell, *RWL* is made logic low which switches off *M11*. *BL* and *BLB* are kept logic high. *WBL* is kept at logic high which makes *M3 ON*. *WBLB* is kept at logic low which turns *M4* off such that write operation becomes single ended. To make the feedback loop cutoff to help in write operation, Data Aware Dynamic Feedback Control write assist technique is employed. For write '1', *M7* is turned off and *M8* is turned ON using $LE = 0$ V and $RE = V_{DD}$. Since *M7* is turned OFF, feedback loop of the cross-coupled inverter pair is cut-off. There is no pull down path connecting node *Q* to ground to help it maintain its value. It is now directly connected to *BL* through *M3*. Thus, *BL* generates a high voltage bump at node *Q*, which leads to change its value to '*1*' with significant increase in write margin. With *Q* changing its value, the inverter (*M2–M8–M6*) connected directly at *Q* changes the value at *QB* to '0'. As *M1* source is connected to V_{DD}, pull up speed at *Q* is high in this case as compared to conventional CVDD write assist technique. Write '*1*' to the cell is shown in Fig. 2(a). Similarly, the procedure of writing '*0*' is shown in Fig. 2(b).

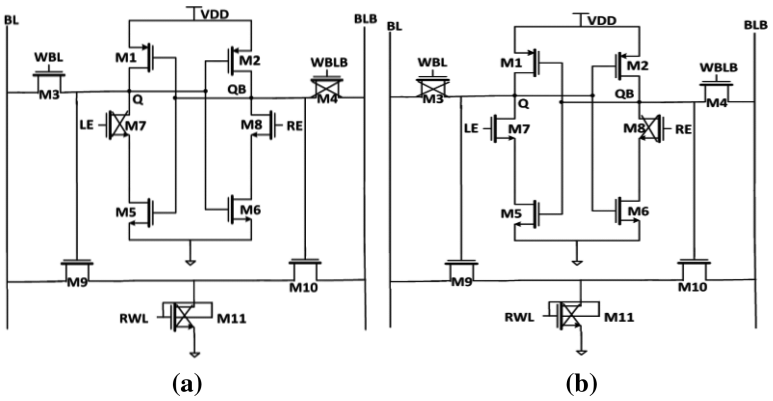

Fig. 2. (a) Write 1 operation (b) Write 0 operation

2.2 Read Operation

Read operation is performed by precharging *BL* and *BLB* and turning control signals *RWL* to logic high and *WBLB*, *WBL* to logic low. During the read operation *M7* and *M8* are *ON* by activating the *RE* and *LE* signals, leading to strong cross coupled inverter. The storage nodes *Q* and *QB* are isolated from bitlines completely which leads to disturb-free read operation. This decoupling action helps in increasing the SNM as disturbance does not reach storage nodes *Q* and *QB* as shown in Fig. 3. Body terminal of *M11* is connected to *RWL* making threshold voltage of *M11* dynamic. When *RWL* is activated for read operation it decreases the threshold voltage and discharges the bitline quickly, making read operation faster than all the compared cells with a greater margin. Due to differential signals, design of sense amplifier is simple. As the read and write access transistors are different, the sizing of the access transistors can be performed to improve the read and write margins separately. Read margin is equivalent to hold margin.

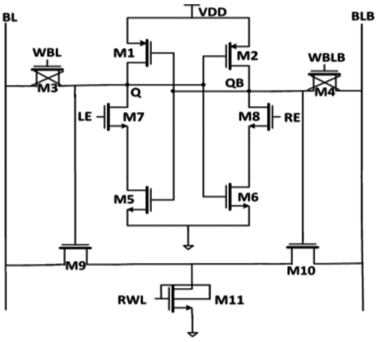

Fig. 3. Read operation

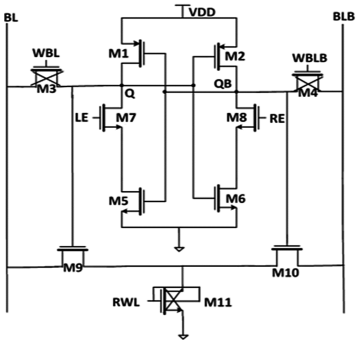

Fig. 4. Hold operation

2.3 Hold Operation

The transistors *M7* and *M8* are *ON* during hold mode. Both *WBL*, *WBLB* and *RWL* are switched *OFF* and two cross-coupled inverters form a strong feedback loop. The hold margin of proposed cell is slightly less compared to hold margin of 6T SRAM cell due to the stacking effect of pull-down NMOS transistors. On the other hand, due to stacking of transistors in pull down, leakage current is reduced in hold state (Fig. 4).

2.4 Half- Selected Cell Issue

When a write '0' ('1') operation is performed on a SRAM cell, the voltage at storage node *QB* (*Q*) for row half selected cells will increase because there will be charge transfer from bitline *BLB* (*BL*). In the proposed SRAM cell, the storage node *Q* (*QB*) does not have driving path to bitline *BL* as *M3* (*M4*) is turned *OFF*. Therefore, in the proposed design there are less chances of change in the value stored in the cell as compared to conventional techniques.

3 Simulation Results and Discussion

In this section, all the post layout simulation results are presented to confirm the functionality of proposed design. The simulations are done using 65 nm industrial technology node. The operating supply voltage and temperature for the simulations are 0.3 V and 27 °C respectively. To show effectiveness of proposed design, it is compared with 6T iso-area (6T upsized to match the layout area of proposed 10T), 9T [15], 10T [17] and ST2 [16]. Iso-area 6T is 3x upsized of its minimum required W/L ratios for 65 nm technology node. Area occupied by the layout of the proposed design is 3.216 μm^2 as shown in Fig. 1(b).

3.1 Write Ability

The WL voltage is used to assess write ability. In this case, the WL voltage is swept from zero to V_{DD} to find the minimum voltage at which the bit cell is written (Q and QB flip) and is called wordline write margin(WVWL). If the value of WVWL is less, then it is easier to write on the bit cell. The write failure criteria is defined as WVWL $\geq V_{DD}$. Write failure occurs at V_{DD}, hence margin is given by V_{DD}-WVWL and is denoted as WVWL write margin. Write ability is also assessed using Write Static Noise Margin (WSNM) calculated using butterfly curve.

In iso-area 6T and ST2, there is fight between access and pull down transistor. But in proposed 10T, during write 1 operation, we turn off *M7* that breaks the feedback loop and no direct path is now for Q node to ground. There is no fight between access and pull down transistor. There is undisturbed charging of Q node through *WBL*. The write margin is slightly lower than 9T and 10T as write operation is single ended. In 9T, write operation is differential. It is a small tradeoff for dynamic write power saved in write operation of proposed 10T. WSNM of proposed 10T is 1.71x and 1.44x as compared with that of iso-area 6T and ST2 and 0.93x as compared to 9T and 10T.

3.2 Read Static Noise Margin

RSNM is defined as the maximum amount of voltage noise that a cell can tolerate in read configuration without flipping of Q and QB. RSNM is calculated by finding the largest square which fits inside the VTCs (butterfly curves). Read noise margin are equivalent to hold noise margin as read is decoupled and disturb free as noise does not reach internal storage nodes. In 9T and 10T, the internal nodes are float during read operation and data retention time is a factor to be considered but in proposed 10T read path bypasses the storage nodes Q and QB isolating them from bitlines completely during read operation. RSNM of proposed 10T is 2x better than 6T as here no voltage divider is formed between access and pull-down transistor.

3.3 Write and Read Access Time

T_{WA} (write access time) is measured as the time required for writing '0' to the storage node *Q*. It is difference of the time when WBLB is *HIGH* and the time when *Q* falls to 10% of its initial high value (i.e., 90% change). Similarly, T_{WA} for writing '1' to *Q* is calculated as the difference of the time when WBL is turned *ON* and the time when *Q* rises to 90% of its initial low value. This ensures correct write operation. Being single ended, it requires more write time for storage nodes compared to all the compared cells as all other cells follow differential write operation.

Table 2. Comparison with different structures at 300 mV

	6T (iso-area)	9T	10T	ST2	PROPOSED 10T
WVWL (mV)	95	248.9	249.1	147	235
WSNM (mV)	127	230	230.5	145	216
RSNM (mV)	47	83	87	69	97
Write access time (ns)	5.4	9	9	8.89	18
Read access time (ns)	7.4	21	12.3	9.5	11
Read current (nA)	6.38	7.05	7.7	6.9	9.7
Write power (nW)	1.5	1.64	1.659	2.043	1.639
Read power (nW)	1.527	1.545	1.549	1.962	1.635
Write method	Differential	Differential	Differential	Differential	Single
Read method	Differential	Single	Differential	Differential	Differential

T_{RA} (read access time or read delay) is measured as the difference of the time when *RWL* (*WL*) is turned *ON* and the time when one of the bitlines is discharged by 50 mV from its initial high value [16]. The 50-mV difference in voltage between the bitlines is sufficient to be spotted by a sense amplifier, thereby avoiding incorrect read operation of the data stored. The read access time for different configurations is shown in Table 2. The read access time of proposed 10T cell is less than 10T cell. Its read current is high compared to 10T cell as result of reduced threshold voltage due to use of DTMOS technique. It is less than 9T cell as it uses single ended read.

4 Conclusion

A 10T SRAM cell is proposed to improve read and write stability for subthreshold operation. This 10T cell employs a data-aware-feedback-cutting scheme to enlarge the write margin and the read-disturb free scheme with DTMOS technique. This proposed design is an ultra-low voltage SRAM cell. Its WSNM is 1.7x of the write margin of iso-area 6T cell. The WVWL margin of proposed 10T is higher than 10T, 6T (iso-area) and ST2. Write operation is functionally single ended and write control signals are data aware. As BL and *BLB* are always high, hence activity factor of switching the bitlines

during write operation is minimal which reduces dynamic power dissipation during write operation. Design of write driver is also simple as same data is sent on both lines. RSNM is highest among all the cells under consideration. Read SNM is almost equal to hold SNM. Read access time is better than compared 9T and 10T. Due to different access transistors for read and write operation, there sizing can be done efficiently for higher margins. Proposed 10T SRAM cell in hold state has smaller leakage current due to stacking of pull down transistors. Hence the proposed cell has high read and write stability and can be operated at ultra-low voltage of 200–300 mV. The advantage of reduced dynamic power consumption enables it to be used in portable battery operated System-on-Chip (SoC) designs.

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