Low-Power Adiabatic Logic—Design and Implementation in 32-Nanometer Multigate Technology

Suresh Kumar Pittala and A. Jhansi Rani

Abstract A new FinFET-based adiabatic NAND logic circuit with Self-Adjustment of Rail Potential (SARP) is proposed. The proposed logic provides reduced power consumption when compared to conventional CMOS and adiabatic circuits. A new FinFET-based adiabatic logic is implemented based on Complementary Energy Path structure. The proposed design reduces the second-order effects, short-Channel effects occurring in Conventional CMOS circuits. The performance of the proposed SARP-FinFET-based adiabatic NAND gate is dominant when compared to the SARP-CMOS-based adiabatic NAND gate. The proposed adiabatic circuits are designed using double gate FinFET using predictive technology models (PTM) in 32 nm Technology using Synopsis HSPICE. The experimental results for the proposed adiabatic FinFET design demonstrate their effectiveness with energy consumption and power optimization.

Keywords FinFET · Adiabatic logic · Adder · NAND gate
Shorted gate · Energy efficient · Power optimization

1 Introduction

The advancements in electronics design technology led to the innovation of portable and battery-operated devices, consequently, the power consumption and speed of operation has become the primary concern. In high-performance handheld devices, the power consumption is the fundamental constraint. In the literature, several adiabatic circuits are presented and the results show their dominance in energy-saving capability. Even though the complexity in design is high when compared to the conventional circuits. Yong moon [1] presented the efficient charge

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recovery logic (ECRL) which performs precharge and evaluation phase simultaneously. An adiabatic differential cascade voltage switch with a complementary pass-transistor logic tree (ADCPL) is presented by Chun-Keung Lo and Philip C H Chan [2]. The presented work lowers the gate complexity of operating the circuit from a two-phase nonoverlapping supply clock. Matthew Morrison [3] in their chapter presented an algorithm for minimization of Boolean functions by correlating the horizontal offsets in the permutation matrix instead of library. The presented algorithm frames an adiabatic s-box structure which reduces the energy imbalance compared to previous benchmarks. The algorithm does the forward encryption and reverse decryption with minimal overhead.

F. Liu and K. T. Lau [4] presented a pass-transistor-based low-power adiabatic logic with NMOS pull-down configuration. Using the implementation of a multiplexer working at 20 MHz, a power saving of 80% is achieved when compared to 2N2N2P Multiplexer. In [5] Dragan Maksimovic presented a clocked CMOS Adiabatic Logic operating with Single-Phase Power Clock Supply. The presented low energy logic incorporates the design of the power control unit within the chip itself. In another work [6] a Pass-Transistor-based single power clock supply Adiabatic Logic is presented. The energy saving happens till 160 MHz for a 1.2 μm technology when applied to a PAL structure. A two-phase clocking dual-rail adiabatic logic known as 2PCDAL is presented in [7] which is based on 2N2N2P structure. The presented circuit uses a two-phase clocking scheme instead of a four-phase clocking scheme used in conventional 2N2N2P. A two-phase clocked adiabatic static CMOS logic (2PASCL) is presented in [8] which uses the adiabatic switching and energy recovery logic as principles. Suhwan Kim and Marios C. Papaefthymiou have presented a True Single-Phase Adiabatic logic instead of complex Dynamic logic [9] which exhibit increased energy consumption and low-performance high-speed design. The work is based on energy recovering logic operating using single-phase sinusoidal clock. Cihun-Siyong Alex Gong et al. presented [10] an irreversible energy recovery logic, which inherits the advantages of Quasi-Static Energy Recovery Logic (QSERL). When compared with QSERL, the circuit excludes the hold phase avoiding the use of feedback keeper. The work states the advantage of the circuit toward the reduction of area and power overheads. The throughput is twice when compared to the counterpart and the power clock used is similar.

In this chapter, we have presented a new adiabatic logic based on FinFET. The proposed design incorporates the best performance efficiency of FinFET and adiabatic in a single platform. The SARP-level circuit structure improves the efficiency of the design by reducing the leakage current. The rest of the chapter is organized in this manner. In the next section, the FinFET-based NAND structure is presented, followed by the proposed leakage reduction technique for adiabatic logic in Sect. 3. Section 4 presents the proposed design and implementation of the methodology. Section 5 discusses the experimental setup and results obtained followed by the conclusion and reference.

2 FinFET-Based Adiabatic NAND Structure

The improvement in technology aggressively scaled down the geometric parameters of the MOS devices to achieve the power consumption reduction, increased speed of operation and larger integration density. The scaling down of geometric parameters has limited to 45 nm due to the performance degradation of the MOSFET devices. The leakage current is the main bottleneck below submicron level scaling. The power consumption can be reduced further by reducing the power supply voltage level, but the leakage current increases exponentially. At the same time, voltage scaling reduces the energy-per-operation during switching instance due to the relation between energy and supply voltage. In multicore devices, the energy is saved using dynamic voltage scaling. The other issues in CMOS devices are the increased sensitivity to process variation and Short-Channel Effects (SCE). Previous studies show that the multigate transistor [11] reduces subthreshold and the gate tunneling leakage current. The device increases the driving current when compared to the standard single-gate MOSFETs below submicron technologies [12, 13]. The promising multigate device, which emerged to replace MOSFET device, is the FinFET. Due to its thin silicon body and dual electrically coupled gate, it suppresses the SCE which reduces the subthreshold leakage current. This device shows better parameter variations in immunity than the conventional single-gate device.

Figure 1 illustrates the FinFET-based adiabatic NAND gate structures based on Shorted Gate (SG) mode FinFETs for conventional NAND gate and 2N2N2P NAND gate.

Since FinFET being a nonplanar device and can work in different modes of operation like SG mode or independent gate mode it is efficient in logic implementation. In this chapter, the 32 nm FinFET PTM is used for HSPICE simulation. The physical characteristics of the PTM FinFET are given in the Table 1.

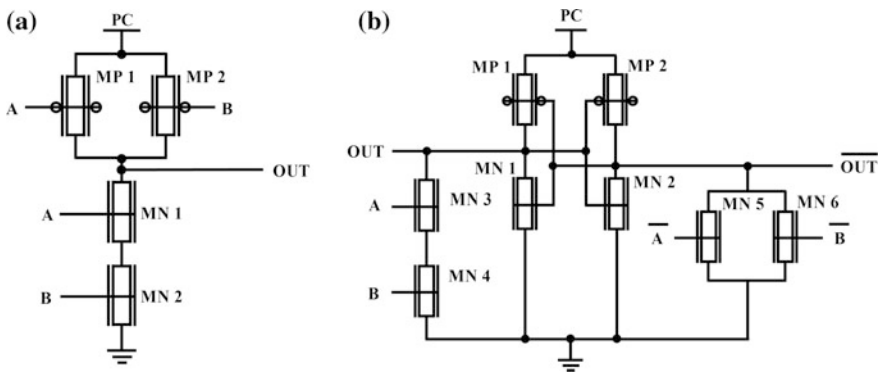

Fig. 1 FinFET-based adiabatic NAND gate structures based on Shorted Gate (SG) mode FinFETs for **a** conventional NAND gate and **b** 2N2N2P NAND gate

Table 1 Primary parameters in PTM

Parameters	Value n-type FinFET	Value p-type FinFET
Channel length (nm)	32	32
Fin height (nm)	40	50
Gate oxide thickness (nm)	1.4	1.4
Threshold voltage (V)	0.29	−0.25
Fin thickness (nm)	8.6	8.6
V_{DD} (V)	1	1

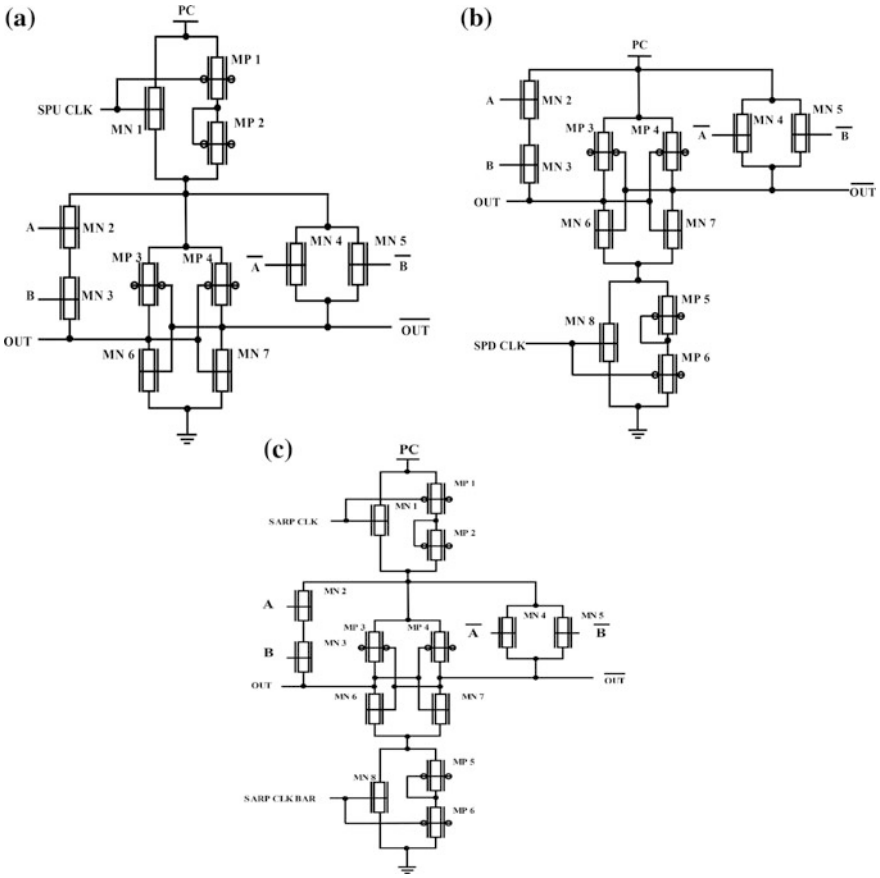

Fig. 2 Various leakage reduction technique structures **a** SPU **b** SPD **c** SARP

3 Proposed Leakage Reduction Techniques for the Adiabatic Logic

Several leakage reduction techniques are available for CMOS circuits used in memory devices [14–16] like SRAM. A leakage reduction technique SARP is designed for the proposed adiabatic circuits using FinFET. A SARP circuit supplies maximum DC voltage to an active-load circuit on request. This makes the load circuit to work quickly. When the load circuit is in active mode, the SARP circuit provides a maximum supply voltage and minimum ground voltage. The three structures of SARP technique the SARP circuit for pull-up, pull-down SARP circuit and combined SARP circuit for pull-up and pull-down is designed with the FinFET-PFAL NAND as shown in Fig. 2. The NAND gate is the load circuit with the lower SARP circuit consists of a single p-type switch while the n-type switches are connected in series.

4 Proposed Technique

A new adiabatic logic using FinFET-based Complementary Energy Path Adiabatic Logic (CEPAL) is proposed. The proposed design is been restructured by SG mode FinFET. The proposed circuits outperform the previous adiabatic logic families in terms of energy efficiency and operating speed. The proposed circuit is based on two clock signals working with four stages namely WAIT, EVALUATE, HOLD, and RECOVER. Two clock signals are used for the SARP and power supply. The phase difference between any two adjacent stages is a quarter of a period. The typical time sequence of the logic with respect to the four-stage operations are the WAIT state in which the power supply is zero, the input is valid and the pre-evaluated result is generated by the evaluation logic and the outputs keep low voltage. In EVALUATE phase, the rise time of the power supply starts from zero and increasing, the input becomes stable. The output follows the power supply and is valid. To keep the output valid (HOLD), the power supply stays in high state, providing a constant input signal to next stage. In RECOVER stage, the power supply falls to zero shutting down the current access to ground and allows the charge stored in the capacitor to recover through the cross-coupled FinFETs. The PFAL circuit eliminates the charge stored in the output through the positive feedback. The proposed CEPAL circuit inherits three advantages when compared to all the previous circuits presented earlier. The circuit operation eliminates the hold phase by which the throughput is increased. This feature is similar to QSERL where the complexity is reduced. The proposed CEPAL circuit consists of two charging transistors (MP1 and MP2), a pull-up network, two discharging transistors (MN1 and MN2), a pull-down network and the SARP block for three configurations. The CEPAL has two paths apart from the charging and discharging paths. The number of devices is more so implementation cost is higher. The adiabatic logic

Table 2 Performance analysis of different FinFET-based adiabatic circuits for PCL = 1 MHz

Switching frequency	10 kHz	20 kHz	40 kHz	80 kHz	100 kHz	250 kHz	500 kHz	1 MHz	10 MHz
Device name	Energy in fJ								
Conventional FinFET	172.4	218	1460	8150	12600	21400	10700	10600	10400
ECRL	108	135	315	1910	979	14500	41600	9810	5330
2N2N2P	134000	134010	134060	134870	984	142000	139000	72600	72600
PFAL	3240	3240	3240	3240	592	3230	3230	3240	3200

Table 3 Performance analysis of different SARP-FinFET-based adiabatic circuits for various power clock frequencies

Device name	CEPAL NAND		SARP CEPAL		SPU CEPAL		SPD CEPAL	
Power clock frequency	Iavg	E in fJ	Iavg	E in fJ	Iavg	E in fJ	Iavg	E in fJ
10 MHz	4.18E-07	418	1.74E-06	1741.76	4.03E-06	4035.36	1.08E-07	108.76
500 MHz	5.71E-07	571	1.69E-07	169.59	4.41E-06	4406.89	1.69E-07	169.59
1 GHZ	3.59E-07	359	1.99E-06	1990.11	4.48E-06	4485.31	1.33E-07	133.09
2 GHZ	4.77E-07	477	2.29E-06	2288.01	4.81E-06	4814.78	1.33E-07	133.09

operating speed depends on the pull-up transistors since the charging and discharging operation is performed through those transistors. The pull-down transistors maintain the voltage at certain nodes for operation. The leakage current and power consumption is controlled by the pull-down transistors. Therefore, in the proposed design the SARP circuit reduces the leakage current and power consumption.

5 Simulation Results

To demonstrate the effect of switching activity on the energy consumption and average current, vast experiments and simulations were conducted for different adiabatic logics designed using CMOS and FinFET. Table 2 shows the performance of different devices measured with different parameters. The switching frequency is varied from 10 kHz to 10 MHz. From Table 3, it is observed that the SPD CEPAL circuit offers reduced energy consumption when compared to the SARP and SPU circuits. The CMOS circuits show the steady-state response, but more energy dissipation while the FinFET-based design even though have peaks and trough the energy consumed is very less. Thus, the proposed designs have efficient performance when compared to the existing methods.

6 Conclusions

We have shown in this chapter the effectiveness of the proposed SARP-FinFET-based CEPAL adiabatic NAND gate. The existing CMOS-based adiabatic design is noticeably improved using our proposed SARP-FinFET-based adiabatic structures. The proposed circuits have been simulated and analyzed using HSPICE with Predictive Technology Models. The results show that the CMOS adiabatic energy

dissipation are reduced on average for PFAL and CEPAL. In future, the design will be utilized for the design of the arithmetic unit and power clock circuit.

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