Short-Range Low Data Rate Pulsed UWB Transmitter

G. Sarathy and S. Praveen Kumar

Abstract This paper presents a pulsed ultra-wideband (UWB) transmitter with high power and efficiency. It consists of a simple switched capacitor-based relaxation oscillator for sub-carrier generation which gives distortion less carrier signal with a phase noise of 106 dBc/Hz at 1 MHz frequency. Phase-locked loop circuit with ON-OFF keying (OOK) modulator to generate FM signal within the range of UWB, i.e., 3.1–10.6 GHz. And class A power amplifier is employed for signal amplification. Proposed pulsed UWB transmitter is implemented in 45-nm CMOS process technology with a power supply of 0.9 V. Experimental results prove that the presented pulsed UWB transmitter has a transmitting range of 6–8.1 GHz with a power consumption of 3.9 mW (Laha et al. 60 GHz OOK transmitter in 32-nm DG FinFET technology, [1]).

Keywords Ultra wide band (UWB) · Wireless body area network (WBAN)
Wireless personal area network (WPAN) · Voltage controlled oscillator (VCO)
ON-OFF keying (OOK) · Phase locked loop (PLL)

1 Introduction

The communication UWB performs signals in the bandwidth of 500 MHz, with the operating frequency range of 3.1–10.6 GHz. UWB communication systems play a major role in delivering short-range wireless networks such as wireless body area network (WBAN) and wireless personal area network (WPAN). The pulsed UWB transmitted at the range of 6–8.1 GHz is implemented with the help of simple switched capacitor-based relaxation oscillator, voltage-controlled oscillator (VCO) and the output amplifier [2].

G. Sarathy (✉) · S. Praveen Kumar
Department of ECE, SRM University, Kattankulatur, Chennai, India
e-mail: Sarathy_g@srmuniv.edu.in

S. Praveen Kumar
e-mail: praveenkumar.se@ktr.srmuniv.ac.in

J. Li et al. (eds.), *VLSI Design: Circuits, Systems and Applications*, Lecture Notes
in Electrical Engineering 469, https://doi.org/10.1007/978-981-10-7251-2_7

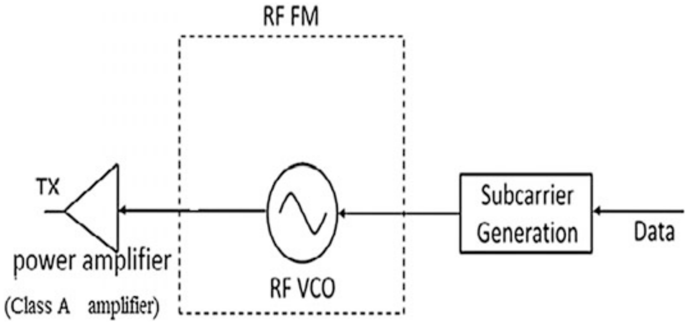

Fig. 1 Short-range low data rate pulsed UWB transmitter

UWB helps to separate the technology from narrow band and wide band. The bandwidth of UWB is defined by Federal Communication Commission (FCC) which is more than 1.5 GHz. UWB can produce impulses that are with sharp fall and rise time. There are two techniques in UWB, they are impulse radio UWB (IR-UWB) and frequency-modulated UWB (FM-UWB) (Fig. 1).

2 Sub-carrier Generation Using SC-Based Relaxation Oscillator

Generally, carrier signals are used in modulation techniques to secure the transmission data from all sources of threats. Preferred type of oscillator for pulse wave generation is relaxation oscillator comprising of charge-discharge current and a timing capacitor [3]. Figure 2 shows the schematic of simple switched capacitor (SC)-based relaxation oscillator. Switched capacitor-based fully differential relaxation oscillator with a charging-discharging timing circuit is presented. Voltage between the capacitors C_1 and C_2 remain unchanged during $-V_{ss}$. As the input X goes high the charge of the capacitor C_1 transfers to C, whereas the voltage remains same. At which point the output equals to $-C_2\ V_{ss}$. The operation keeps running until V_x reaches 0 V.

The simplified FS-embedded relaxation oscillator architecture consists of op-amp, switched capacitor, delay cell, non-overlapping clock, inverter, nand circuits. The input of the op-amp is in-n and in-p, the output is out. The comparator inputs are in-n.in-p, clk and the output is out. The two-phase non-overlapping clock consists of input clk in and the outputs clk 1 and clk 2. The supply voltage is given with V_{dc} = 1.8 V. The principles of relaxation oscillator are with V_{out} low to $-V_{ss}$ and V_x are higher than zero. The Voltage across the Un-Switched capacitor remains unchanged At $-V_{ss}$, the output will fall by an amount of

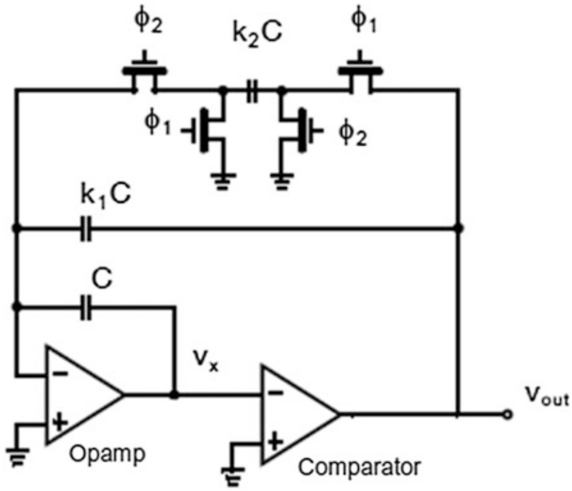

Fig. 2 Proposed sub-carried relaxation oscillator

$$\Delta v_x = \frac{\Delta Q_c}{C} = \frac{Q_{k_2c}}{C} = -k_2 V_{SS}$$

3 Proposed Transmitter with OOK Modulation

3.1 Phase-Locked Loop

The key function of phase-locked loop (PLL) is to provide synchronization clock and to maintain the integrity of time. Hence nowadays, PLL is an essential building block a major communication system. The comparison operation is performed by a phase detector. In this paper, the necessity of locking the transmitter signal on to the range of ultra-wideband (UWB) that is 3.12–10.6 GHz is achieved by using PLL. The output of the PLL block is a transmitting signal with a tuning range of 6–8.5 GHz, and the schematic of PLL is shown in Fig. 3 (Figs. 4 and 5).

3.2 OOK Modulation

The basic concept of a simple ON-OFF keying modulation is to transmit the data only during the positive transition while no data during the negative transition. The advantage of the above is power consumption that is greatly reduced as it is to operate only during the positive cycle. Also, the noise distortion scope is very less, almost negligible when compared to other conventional modulation techniques. In this paper [4], a 60 GHz, 2 Gbps OOK modulator is designed in 45-nm CMOS process technology with high ON/OFF isolation. The proposed OOK modulator is

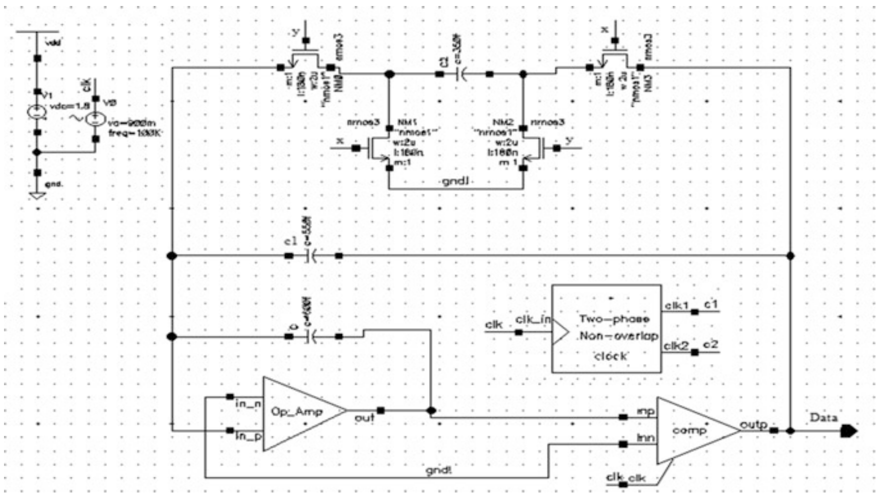

Fig. 3 Schematic of proposed sub-carried relaxation oscillator

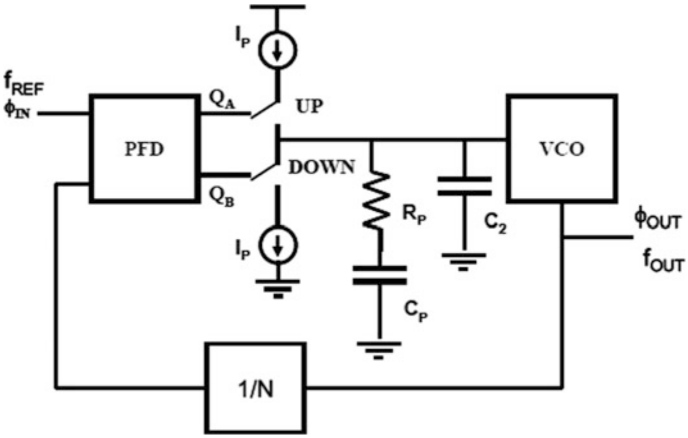

Fig. 4 Third-order phase-locked loop (PLL)

well suited for less power, short-range UWB applications [5]. From the simulated schematic, the pulsed UWB of 2.5 Gbps of data rate is transmitted (Figs. 6 and 7).

3.3 Output Amplifier

The common source (CS) configuration requires less power supply and biasing voltage compared with Darlington, cascode configuration which makes it an ideal

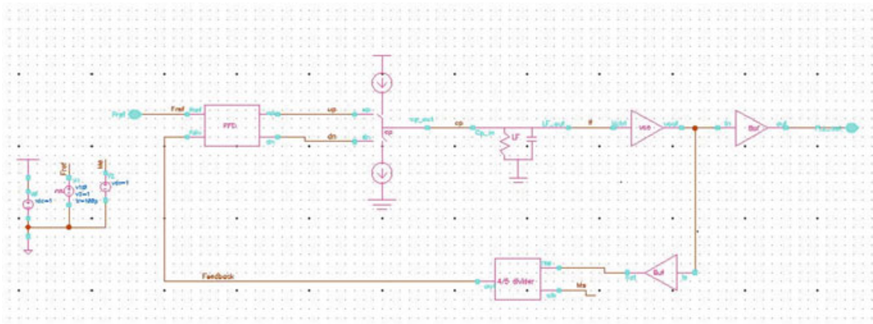

Fig. 5 Schematic of third-order phase-locked loop (PLL)

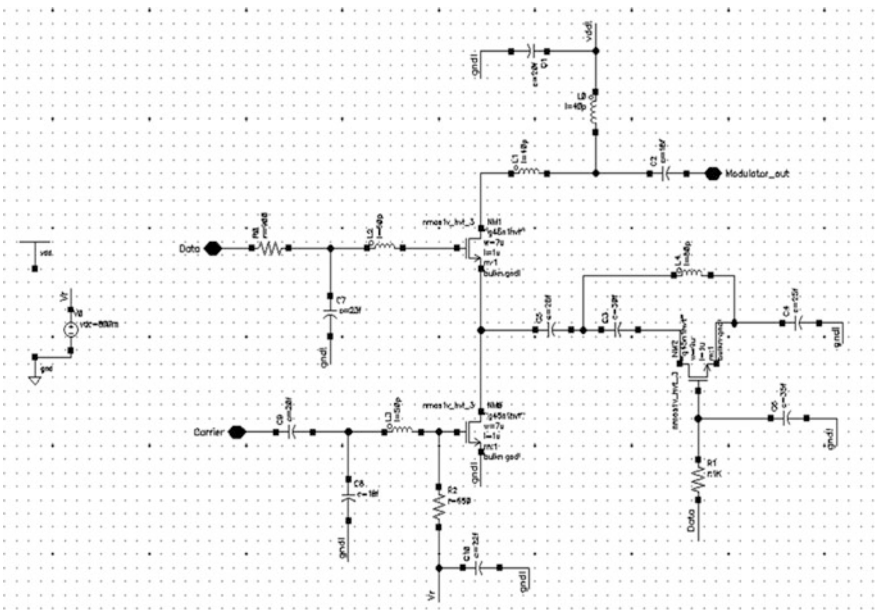

Fig. 6 Schematic of OOK modulation

option for the wireless applications employing low power, short distance. The transistor in the common source configuration operates independent eliminating the higher order distortion. In effect, the linear of the power amplifier is greatly increased. The linearity of the PA is also observed to be competitive for low power CS configurations. The output amplifier used here is class A power amplifier [1] The 1 dB compression point (P1*dB*) and the third-order input intercept point (IIP3) are found to be 5.7 and 18.7 dBm, respectively. The 13 dB difference between P1*dB* and IIP3 can be attributed to the scaling down of DG MOSFET to 32 nm [1]. The power-added efficiency (PAE) and the fractional bandwidth (FB) of this amplifier are ~ 14 and 50%, respectively (Figs. 8 and 9).

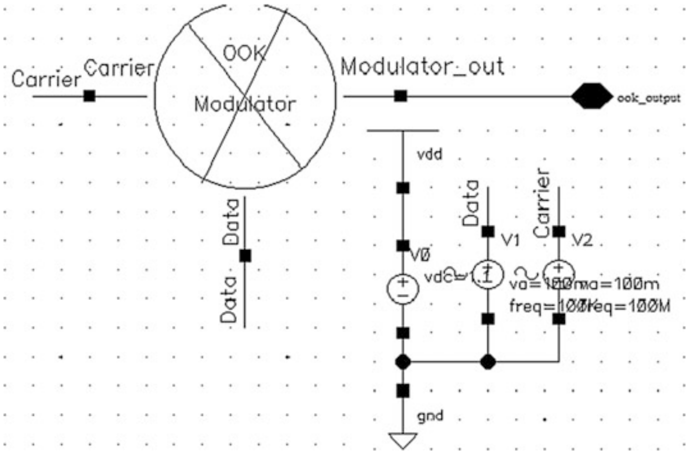

Fig. 7 Test bench of OOK modulation

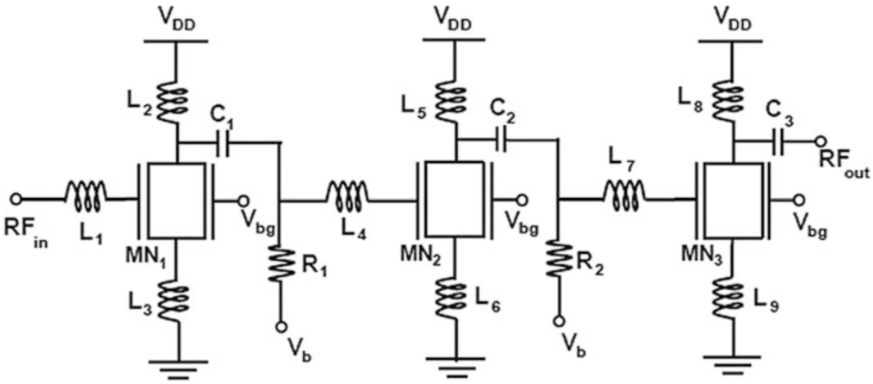

Fig. 8 Class A power amplifier

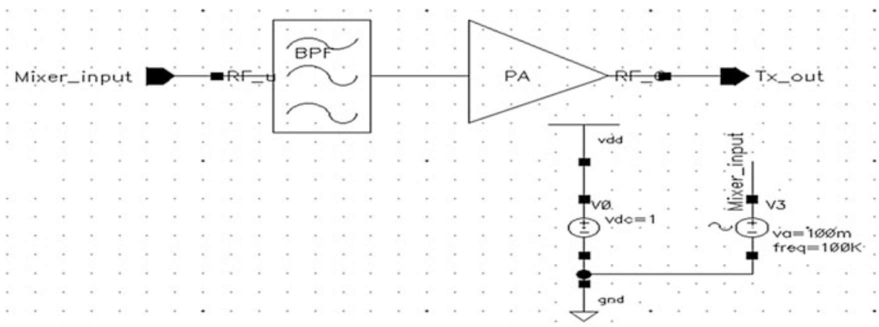

Fig. 9 Test bench of class A power amplifier with band pass filter (BPF)

4 Simulation Results

Cadence virtuoso tool was used to simulate the simulation results, and power and phase noise operation were studied under 45-nm CMOS process technology of Pulsed UWB transmitter. Output schematic of pulsed UWB transmitter shown in Fig. 10.

4.1 OOK

A 60 GHz of 2.5 Gbps OOK modulator is designed in a 0.18 m BiCMOS process (Fig. 11).

4.2 Phase Noise

It is observed in the waveform the phase noise is −105.5 dbc/Hz (Fig. 12).

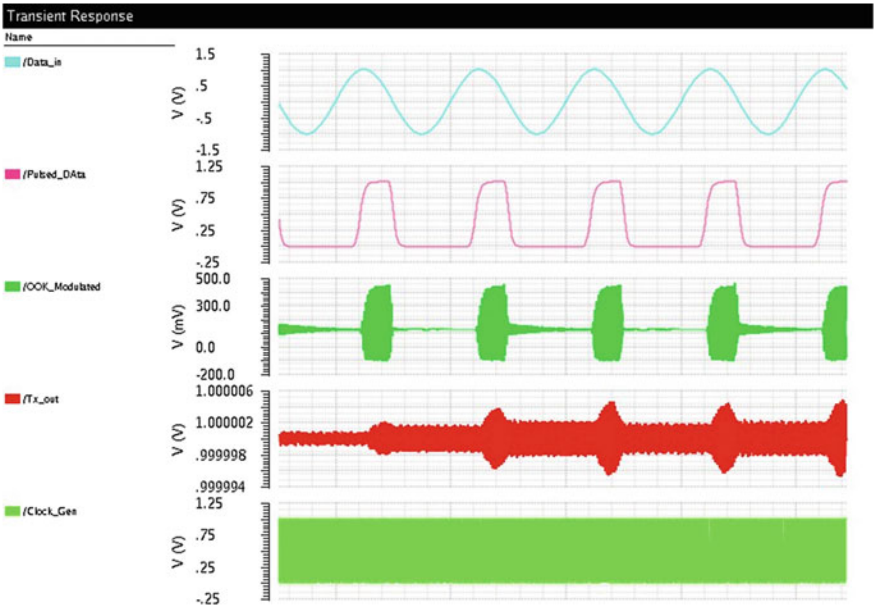

Fig. 10 Output schematic of pulsed UWB transmitter

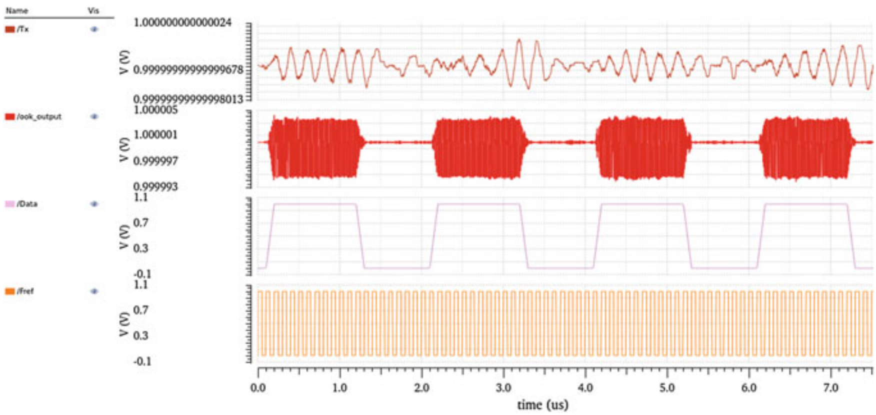

Fig. 11 Output of OOK modulator

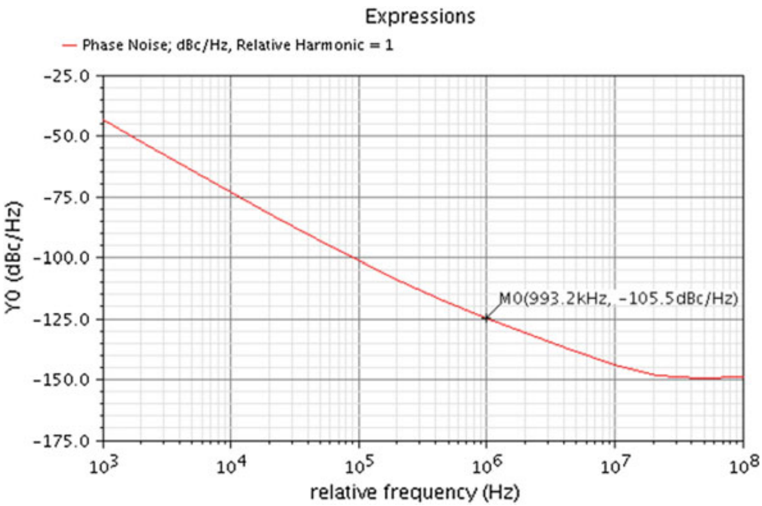

Fig. 12 Output of phase noise

4.3 Power Amplifier Power Output

The class A output amplifier is amplified and the power of 3.33 mW is obtained. The 3-dB bandwidth considered for all the cases of *Vbg* is 40 GHz (Fig. 13).

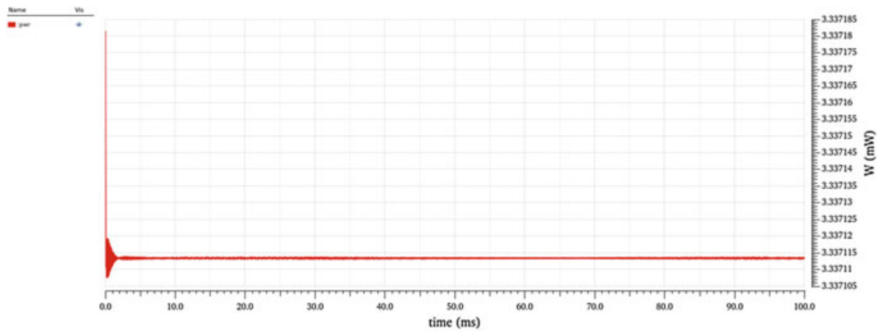

Fig. 13 Power output of class A amplifier

Table 1 Comparison of UWB transmitter

Technology	130 nm	90 nm	This work (45 nm)
VDD (V)	1.2	1	0.9
RF tuning range (GHz)	3.5–4.5	2.9–5.2	6–8.25
Sub-carrier frequency (Mhz)	1	0.8	1
Phase noise (dBc/Hz)	−107	−75	−105
Power consumption (mW)	4.6	0.8–1.1	3.9

5 Measurements Results

See Table 1.

6 Conclusion

Frequency-modulated ultra-wideband transmitter is widely used in data transmitting such as wireless personal area networks. A simplified sub-carrier generation structure has been proposed and compared with the existing architecture resulting ease of operation. The proposed architecture requires less power when compared with existing architecture for improved results modification in op-amps, biasing circuits and current-mode bandgap reference circuit should be considered as future work.

References

1. Laha S, Kaya S, Kodi A, Matolak D (2012) 60 GHz OOK transmitter in 32 nm DG FinFET technology. School of Electrical Engineering & Computer Science, Ohio University, Athens, OH, 45701, USA
2. Shawkey HA, Soliman AM (2015) A 6–10 GHz FM-UWB transmitter. Int J Eng Technol IJET-IJENS, 15(01) 39, February 2015 IJENS
3. Detratti M et al (2009) A 4.6 mW 6.25–8.25 GHz RF transmitter IC for FM-UWB applications. In Proceedings of IEEE ICUWB, Sept 2009, pp 180–184
4. Jang S, Student Member, IEEE, Nguyen C (2015) A 60 GHz 2.5 Gbps OOK modulator with data-dependent impedance cell for enhanced ON/OFF isolation in 0.18 m BiCMOS process. IEEE Microwave Wirel Compon Lett 25(4)
5. Saputra N, Long JR (2011) A fully-integrated, short-range, low data rate FM-UWB transmitter in 90 nm CMOS. IEEE J Solid-State Circuits 46:1627–1635