Adiabatic Techniques for Energy-Efficient Barrel Shifter Design

K. Anantharaman and A. V. M. Manikandan

Abstract One of the efficient ways to design a low power consumption logic style is the adiabatic logic circuits. This is far better than conventional CMOS logic in terms of power consumptions, delay, and efficiency. This paper explains the design of a 4-bit Barrel shifter using two different adiabatic logics, namely positive feedback adiabatic logic (PFAL) and pass transistor adiabatic logic (PAL). A Barrel shifter is effectively used in arithmetic and logical operations. PFAL utilizes positive feedback technique. The structure contains an adiabatic amplifier. The latch of PFAL is made by two PMOS and two NMOS transistors that avoid logic level degradation at output nodes. Energy recovery in the recovery phase of the clock supply results in a reduction in the power consumption. However, it is not suitable to the application where the delay is critical as the PFAL suffers from large switching time. PAL is a dual-rail adiabatic logic with low gate complexity. It also operates in two-phase power clock. With the use of PFAL and PAL logics, we are going to design 4-bit Barrel shifter. The circuit simulation is performed on Cadence Virtuoso using 180-nm CMOS technology. The parameters such as delay and power dissipation are calculated. From the simulation results obtained, it shows PAL adiabatic logic is more efficient than PFAL adiabatic logic because of reduction of non-adiabatic losses in PAL.

Keywords Barrel shifter · Adiabatic logic · PFAL · PAL · Multiplexer Cadence · Virtuoso

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1 Introduction

In the early days, low-power IC design techniques were not always required. But today, low-power design is necessary for all electrical design to reduce the power consumption of the devices. Minimizing of the supply voltage, circuit complexity, clocking frequencies, and many others are the common goals of low-power designer. The above parameters are reduced to an extent but, however, which is limited by other parameters such as noise margin and threshold energy.

One of the common techniques which can be used to minimize energy loss is the adiabatic logic. It can be used in analog as well as digital logic design. It can incur two types of losses. Their types are classified into adiabatic loss and non-adiabatic loss. The adiabatic loss cannot be avoided. The non-adiabatic loss can be reduced to an extent. Adiabatic logic is divided into two types [1]. They are Quasi/Partial adiabatic logic and Full adiabatic logic. Partial adiabatic logic will have a simple design and easy to implement while Full adiabatic logic has a complex design. The adiabatic loss will occur in Partial adiabatic logic when current flows through non-ideal-switch. Non-adiabatic loss can be greatly reduced in Full adiabatic logic.

Partial/Quasi adiabatic logic families include efficient charge recovery logic (ECRL), two-phase clocked adiabatic static CMOS logic (2PASCL), and positive feedback adiabatic logic (PFAL). Full adiabatic logic includes pass transistor adiabatic logic (PAL) and split-rail charge recovery logic (SCRL) [2].

Barrel shifter is used in microprocessors. They are essential for designing of the data path for DSP algorithms. They will typically shift the data in arithmetic and logical manner [3]. The main difference with the universal shifter is that Barrel shifter will shift "*n*" bit in one cycle, but universal shifter register does one-bit shift in one cycle.

In this paper, we presented two types of adiabatic logics. One is from Partial/Quasi adiabatic logic, i.e., positive feedback adiabatic logic (PFAL) and another is from Full adiabatic logic, i.e., pass transistor adiabatic logic (PAL) [4]. The basic structures of these two types are defined, and 2:1 Multiplexer is created from these logics which is the basic building block of Barrel shifter. From the implemented logics, parameters such as power and delay are calculated which show the efficient logic between these two.

2 Multiplexer

2.1 Positive Feedback Adiabatic Logic (PFAL)

It comes under the category of Partial/Quasi adiabatic logic. It is also called partial energy recovery circuit. It is a dual-rail circuit. It provides good robustness against technical variations. Two *n*-trees provide the logical function which contains NMOS transistors only. It is connected in parallel to PMOS. Totally, ten NMOS

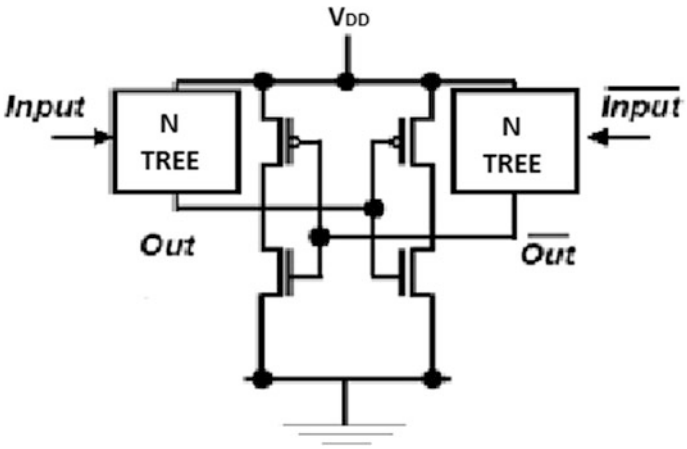

Fig. 1 Block diagram of positive feedback adiabatic logic

and two PMOS are used in the circuit. Two cross-coupled inverters and two functional blocks (*N*-Tree) form true and its complementary output of the given function [5].

In PFAL, the latch is formed by adding two PMOS and two NMOS [6]. The latch can avoid logic level degradation on the output nodes. PMOS transistor will determine the charging path resistance. Decreasing the charging path, resistance of the circuit will improve the performance of the circuit. Due to this logical style of PFAL circuit, the equivalent resistance is smaller when capacitance needs to be charged. The logical diagram of PFAL is given in Fig. 1. From this logic, Multiplexer is implemented. The designed Multiplexer is used to form Barrel shifter (Fig. 2).

2.2 Pass Transistor Adiabatic Logic (PAL)

It comes under the category of Full adiabatic logic. It is one type of dual-rail logic style which is implemented in an adiabatic logic. The complexity is somewhat less when compared to other Full adiabatic logic styles [1]. It evaluates in two phases. They are evaluation phase and recovery phase. In the evaluation phase, clock rises from zero to V_{dd} to the circuit. In the recovery phase, clock returns to zero from V_{dd}. In the recovery phase, energy is recycled back to power clock generator.

It is proposed to eliminate the precharge diodes. But it also suffers from closed recovery path. It consists of two PMOS and eight NMOS in the logical design. Two *n*-trees will produce the logical function. The logical deign will produce the true and complementary outputs of the given function [4]. The logical diagram is given in Fig. 3. From this, Multiplexer is implemented. The designed Multiplexer is used to form Barrel shifter (Fig. 4).

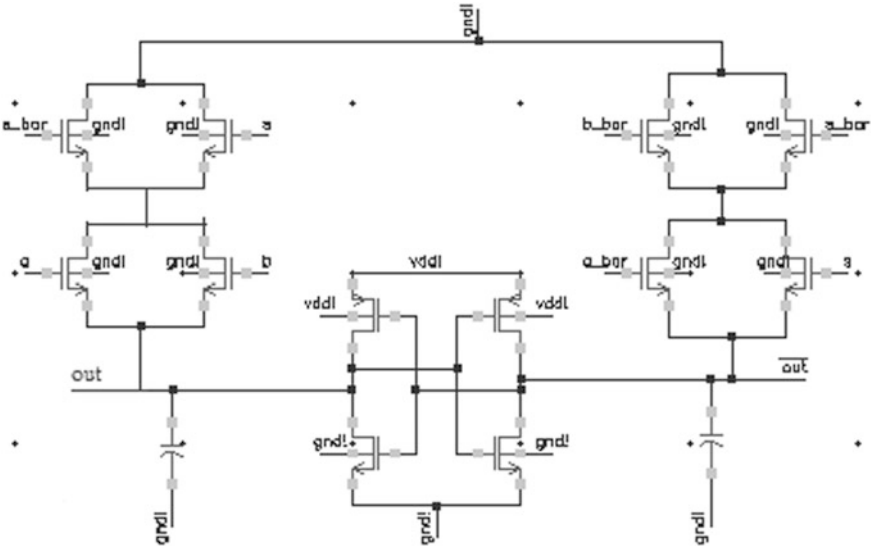

Fig. 2 Schematic of positive feedback adiabatic logic (PFAL)

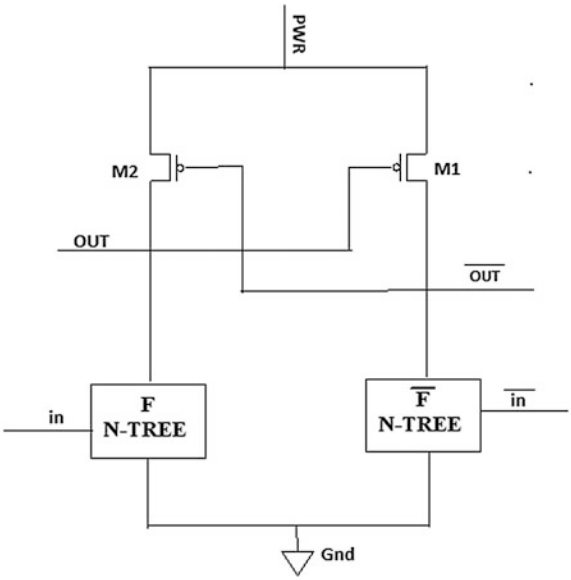

Fig. 3 Block diagram of pass transistor adiabatic logic

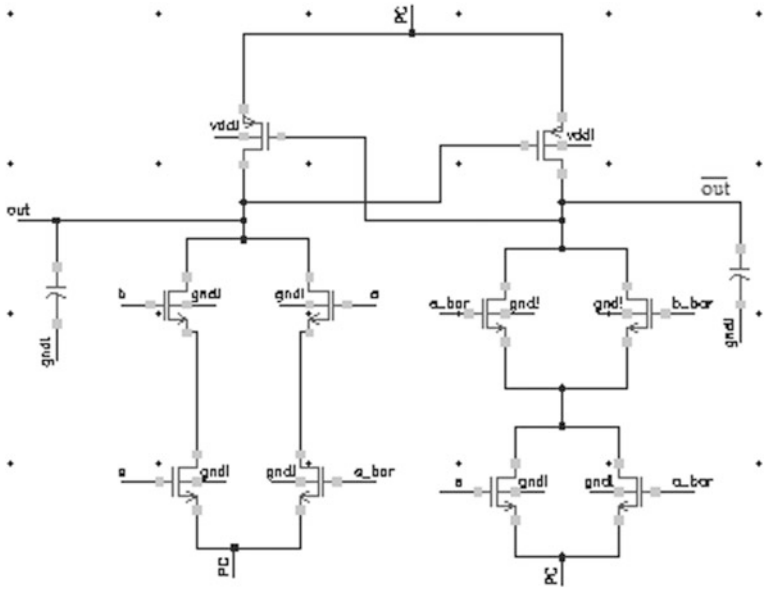

Fig. 4 Schematic of pass transistor adiabatic logic (PAL)

3 Barrel Shifter

It is a functional unit which can be used in a number of different circumstances. It is usually used to give directions of shift and rotation function operation [3]. It can also use to specify the type of shift (circular, arithmetic, or logical) and the amount of shift (typically 0 to $n - 1$ bits). The clock input will specify the number of bits which will be rotated. Even though it is complex to implement, it is always used in the design of data paths in DSP Algorithms.

It is almost symmetric. They are many ways to implement the shifter, but the most common method is to use the MUX to realize the design. The MUX design reduces the power consumption of the circuits. The basic building block of the Barrel shifter is 2:1 MUX. For 4-bit Barrel shifter, it contains 4-bit inputs & outputs and 2-bit select lines. Figure 5 represents the implementation of 4-bit Barrel shifter.

The rectangular box drawn in Fig. 3 indicates 4-bit Barrel shifter. The given circuit will perform the rotation operation. For each one-bit change in select lines, there will be a change in rotation operation; here, it will rotate up to three bits at a time for a single clock pulse. The implemented circuit will produce only left rotation (Table 1).

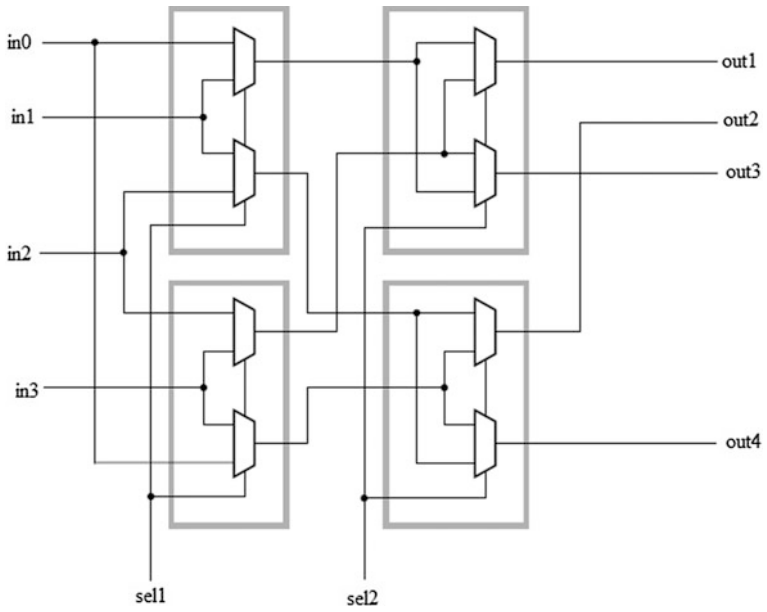

Fig. 5 4-bit Barrel shifter

Table 1 Rotation process

SEL2	SEL1	Process
0	0	No rotation
0	1	1-bit rotation (left)
1	0	2-bit rotation (left)
1	1	3-bit rotation (left)

3.1 PFAL 4-Bit Barrel Shifter

See Fig. 6.

3.2 PAL 4-Bit Barrel Shifter

See Fig 7.

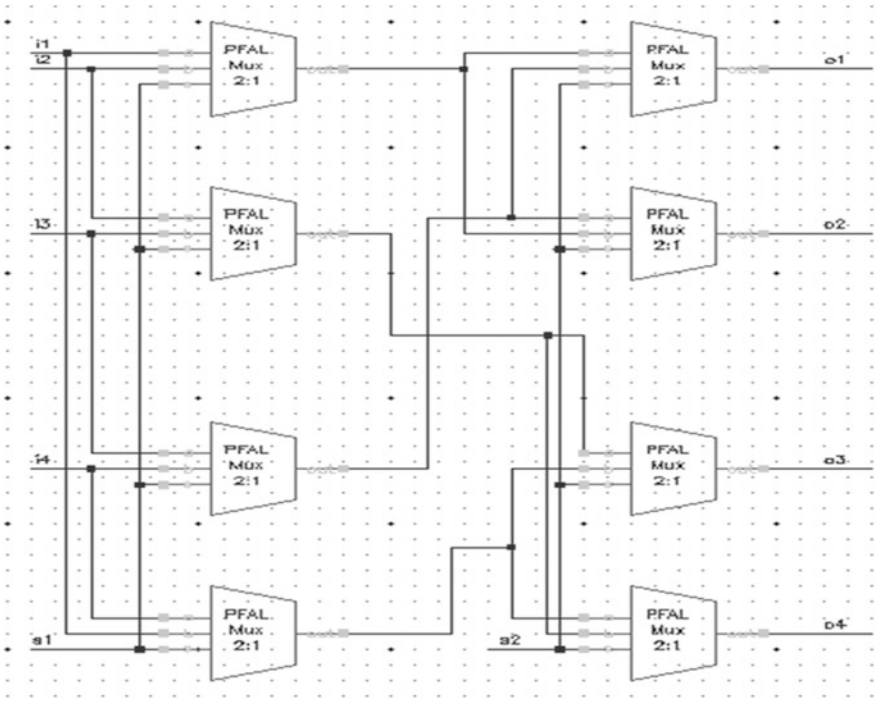

Fig. 6 4-bit Barrel shifter implemented in PFAL

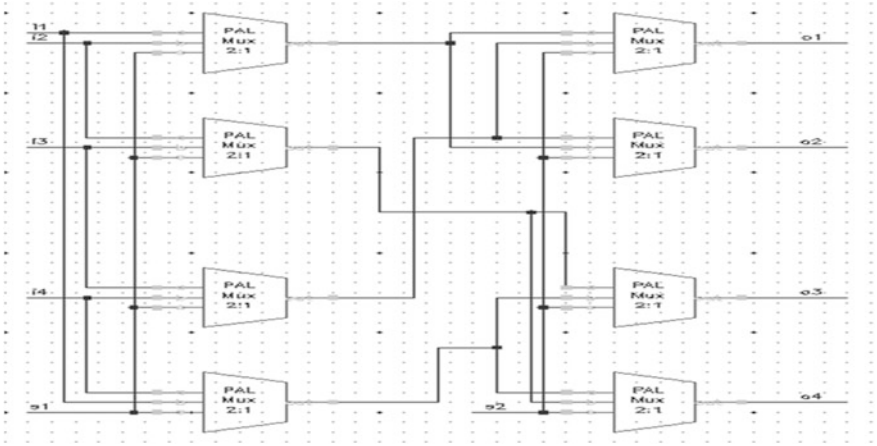

Fig. 7 4-bit Barrel shifter implemented in PAL

4 Simulation Results

4.1 PFAL 4-Bit Barrel Shifter

See Fig. 8.

4.2 PAL 4-Bit Barrel Shifter

See Fig. 9.

The simulated results show the rotation operation of the proposed work. According to the selection lines (SEL1 and SEL2), the outputs are rotated in left. The outputs will copy the inputs according to the selected line. The outputs are left rotating for every change in selection lines (SEL1 and SEL2).

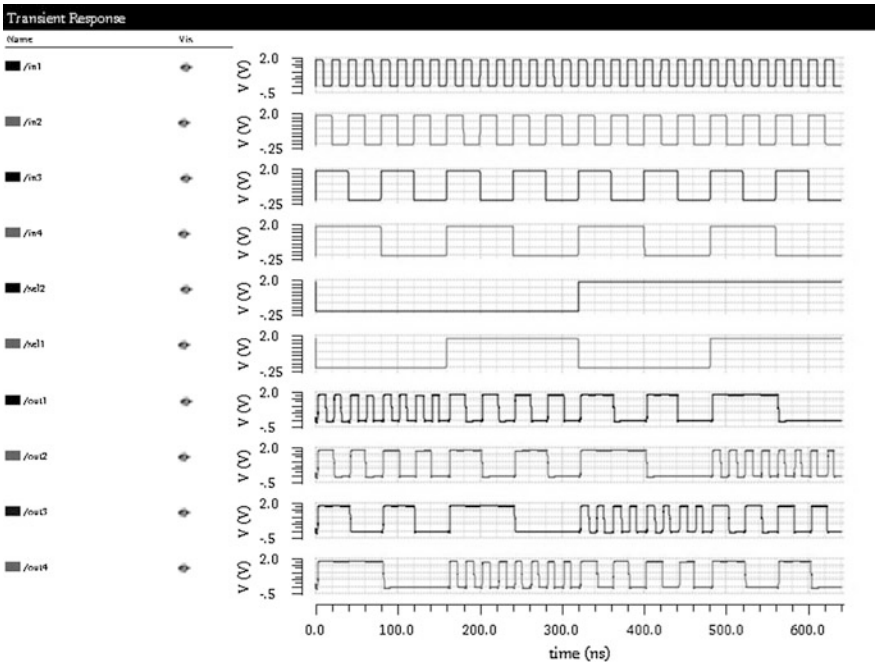

Fig. 8 4-bit Barrel shifter output in PFAL

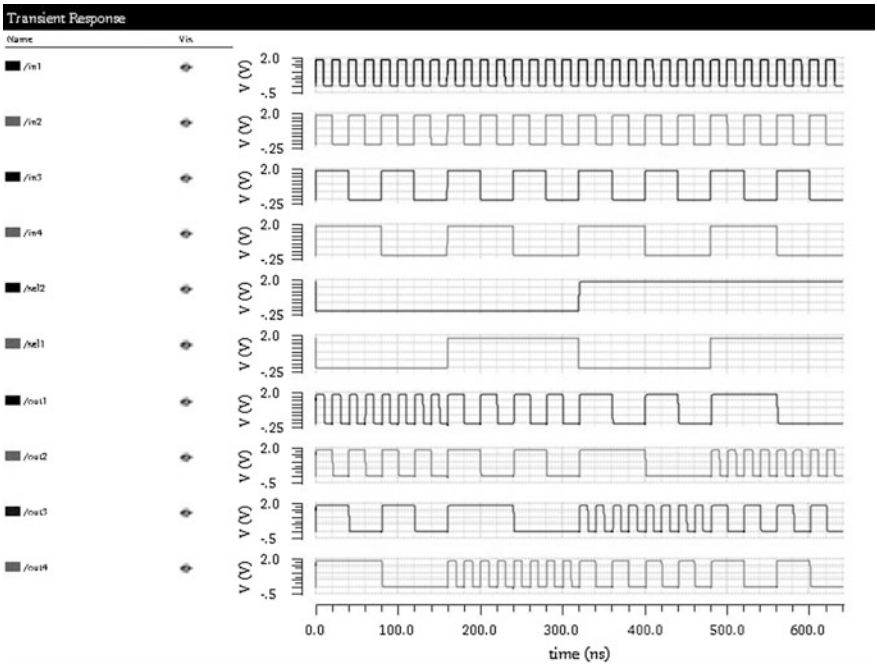

Fig. 9 4-bit Barrel shifter output in PAL

5 Specification and Comparison

The Barrel shifter is implemented using Cadence Virtuoso Analog Design Environment for TSMC 180-nm CMOS Technology process. A capacitor load is connected at the output node. The parameters which are used in the design are given in Table 2. The simulated results are given in Figs. 6 and 7 (Table 3).

Table 2 Specification table

Specifications	Values
Technology	180 nm
Power supply	1.8 V
Length of PMOS transistor	7.2 µm
Width of PMOS transistor	180 nm
Length of NMOS transistor	3.6 nm
Width of NMOS transistor	180 nm

Table 3 Comparison table

Parameters\types	PFAL	PAL
Delay	502.70 ps	90.34 ps
Power dissipation	6.51 mW	3.19 mW

6 Conclusion

In this paper, the 4-bit Barrel shifter is designed in two different adiabatic logics and different parameter variations among two different adiabatic logic families are investigated. Circuit simulation shows that PAL is more advantageous than PFAL. The parametric comparison shows that delay and power dissipation in PAL are reduced than that of PFAL. It can be used instead of conventional CMOS logic structure for smaller circuits in which it effectively reduces power consumption and delay. The higher-order Barrel shifter can be produced. It can be used in ALU operations to perform shifting operations.

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