All-Digital RF Transmitter with Highly Power-Efficient Doherty Power Amplifier

Deepa Pradeep and B. Ananda Venkatesan

Abstract In this paper, a new architecture of an all-digital RF transmitter is proposed. It makes use of delta-sigma modulators for signal synthesizing followed by a dual-input Doherty power amplifier with an efficient design approach. Delta-sigma modulator produces two out-of-phase signals, each of these signals is fed separately into the main and auxiliary power amplifiers of the dual-input Doherty power amplifier, and thereby, the transmitter overcomes the linearity issues. It demonstrates quiet comparable performances: more than 75% of power-added efficiency at a maximum output power of 48.3 dBm, with an overall efficiency greater than 80% for a frequency range from 0.9 to 1.1 GHz.

Keywords Delta-sigma modulator · Doherty power amplifier · Digital transmitter Digital to analog converter · HEMT

1 Introduction

In this digital world, it is very much necessary to have a highly power-efficient transmitter for the transmission of digital signals. This paper presents an all-digital RF transmitter with maximum power-added efficiency and better overall efficiency. It makes use of simple functional blocks and is beneficial to WLAN/WCDMA applications.

In a previous work mentioned in [1], an FPGA had been used for synthesizing signals by combining the outputs of eight DSMs and this provided an advantage of better coding efficiency. These synthesized signals were then power amplified by using a Doherty power amplifier and gained a power-added efficiency more than 40%

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with the expense of linearity. Another type of digital transmitter is proposed in [2], where adaptive phase alignment technique was used to compensate for linearity issues. This required additional hardware, and PAE reported was less than 50%. In addition to that, it required a tunable BPF to maintain high power efficiency.

Different types of digital transmitters are digital polar transmitter [3] and digital outphasing transmitter [4]. A digital-intensive polar transmitter had been proposed in [5]. It had a PAE of 35% and eliminated AM predistortion. In this paper, a new architecture of an all-digital RF transmitter with highly power-efficient power amplifier is proposed. The proposed design consists of simple functional blocks, and the basic functional blocks are discussed in Sect. 1. It makes use of dual-input Doherty power amplifier, and its design method is specified in Sect. 4.

2 Transmitter Structure

The structure of proposed all-digital RF transmitter is depicted in Fig. 1. It consists of two delta-sigma modulators (DSMs), a multiplexer acting as a digital upconverter, digital-to-analog converter (DAC), a low-pass filter (LPF), and a power amplifier (PA).

The two DSMs synthesize anti-phase signals. DSM is fed by pulse signals of frequency 25 MHz, which is then converted to almost-analog signals by the DSMs. A 2:1 multiplexer acts as a digital upconverter, it is provided with a control signal of 1 GHz, and this results in fast multiplexing and produces a signal of frequency 1 GHz. A digital-to-analog converter (DAC) is used to convert almost-analog signals to analog signals. And finally, an LPF is used to filter out the unwanted signals with a cutoff frequency of 1 GHz. These signals are further power amplified by using a dual-input Doherty power amplifier. The use of anti-phase signals eliminates linearity issues, thereby increasing the efficiency of the transmitter.

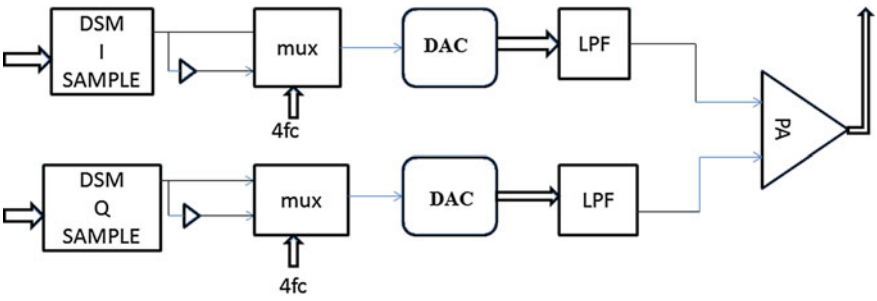


Fig. 1 Structure of the proposed transmitter

3 Signal Synthesizing

Delta-sigma modulator is derived from delta modulator. Figure 2 shows the structure of a delta-sigma modulator. It comprises an integrator, quantizer, DAC, and a D latch as the storage element. Figure 2 represents a first-order delta-sigma modulator. Vin(t) represents the input signal, and corresponding to the input signal, the delta-sigma modulator generates the output, Vout(t). The feedback signal F(t) is extracted from Vout(t) and is fed to the input terminal. The difference between input signal Vin(t) and feedback signal F(t) gives E(t), the quantization error. The errors have been accumulated by the integrator and then further send to the comparator to produce the required output signal; thus, the comparator acts as a quantizer. Thus, DAC converts high and low digital pulses into high and low voltage levels. Since delta-sigma converts an input from one domain to another, amplification is undesirable, and the feedback loop and the DAC must have a gain of 1.

The main block of a DSM is the integrator, and it decides the speed and performance of DSM. Integrator used here is a resistor–capacitor network which accumulates the received input signals; quantizer is a comparator; for this work, a 2:1 multiplexer is used as a comparator with a control signal, Fdsm, of 25 MHz. It generates one or zero based on the input. The comparator output is stored in a low power latch, which is a D flip-flop. The negative feedback path consists of a DAC and is compared with the input by using a subtractor. This results in generation of step signals, where the step size represents the information to be transmitted. The output of DSM is upconverted by using a 2:1 multiplexer, with a control signal of four times the input frequency. It results in fast multiplexing producing signals of frequency 1 GHz. The digital signal is then converted into analog signals by using a digital-to-analog converter (DAC). DAC is basically a multiplexer where the output of the digital upconverter acts as the control signal and inputs as positive and negative reference voltages. Unwanted signals are filtered out by using a low-pass filter (LPF) (Fig. 3).

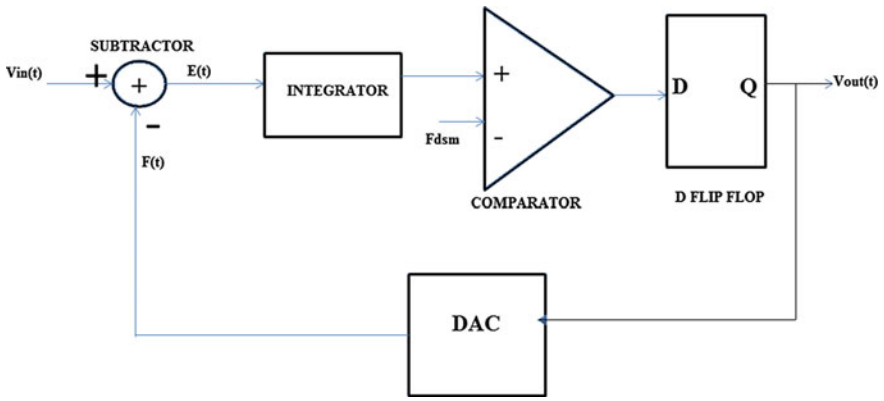


Fig. 2 Block diagram of delta-sigma modulator

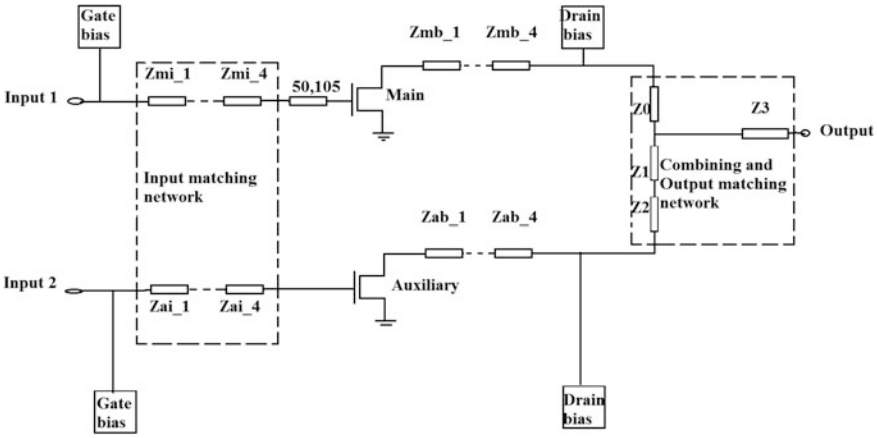


Fig. 3 Circuit diagram of the realized dual-input Doherty power amplifier. The impedances of main and auxiliary power amplifiers are Zm and Za, respectively

4 Dual-Input Doherty Power Amplifier Design

A dual-input digitally driven GaAs Doherty power amplifier is used in this work. The digital inputs to the amplifier are preprocessed as mentioned above. The main aim of using dual-input Doherty power amplifier is to compensate for linearity issues. Doherty power amplifier consists of a class AB biased main amplifier and class C biased auxiliary amplifier. The transistor used is ATF-54143 GaAs HEMT, and its biasing is done as per its datasheet. The matching networks of the main and auxiliary amplifier have been designed to maximize the efficiency and power-added efficiency at peak power. Peak power optimal load impedances are obtained by using load-pull simulations. Load-pull simulations of class AB and class C amplifiers are shown in Fig. 4. In this design, the transistors used are symmetrical and identical in size. The phase difference between the signals is established by adding a delay element. Dual-input Doherty power amplifier does not require any power-splitting network, and at the output, it makes use of combining network whose characteristic impedances are given in Tables 1 and 2.

5 Simulation Results

The proposed dual-input Doherty transmitter is built, as shown in Fig. 1, by using Advanced Design System (ADS) tool. The dual-input Doherty PA is designed by using microstrip lines instead of lumped elements, and it results in decreased size of the transmitter. The digital signal synthesizing is done by using DSM, multiplexer, DAC, and LPF. This generates a signal of frequency range 0.9–1.1 GHz. To

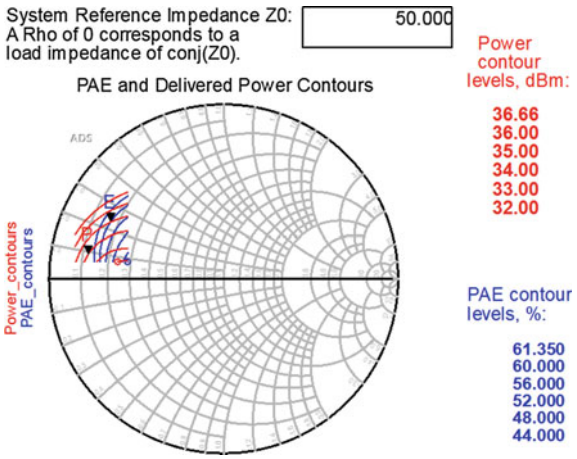


Fig. 4 One-tone load-pull simulation with input power PIN swept between −20 and 20 dBm. Output power and PAE found at each fundamental or harmonic load for the main and auxiliary amplifiers

Table 1 Determined characteristic impedances and electrical lengths of the microstrip lines in the input matching network at a frequency of 1 GHz

Zm1 (Ω)	θm	Za1 (Ω)	Θa
68.2	9.1	68.2	9.1
20.8	15.4	20.8	15.4
49.0	12.3	49.0	12.3
29.6	24.5	29.6	24.5

Table 2 Determined characteristic impedances and electrical lengths of the microstrip lines in the output matching network and combining network at a frequency of 1 GHz

Zmb (Ω)		θmb		Zab (Ω)		Θab	
33.0		16.9		8.3		20.3	
75.8		25.6		73.5		20	
20.0		12.2		6.8		23.0	
31.5		25.0		80.2		29.4	
Z0 (Ω)	θ0	Z1 (Ω)	θ1	Z2 (Ω)	θ2	Z3 (Ω)	θ3
42.0	82	42	85	35	85	20	70

demonstrate the flexibility of the proposed transmitter, the main and auxiliary PAs are excited separately by the synthesized signals and one arm of the input is provided with a delay element. This introduces a phase difference between the input signals, which eliminates linearity issues. Linearity measures are analyzed by using harmonic simulation in ADS.

Power-added efficiency (PAE) is defined as the metric for rating the efficiency of a power amplifier and is calculated and analyzed with the previous works, as given in Table 3 (Fig. 5).

The PAE measured is shown in Fig. 8 and is recorded to be 78.5% with a maximum output power, Pout, of 48.3 dBm, as shown in Fig. 6. PAE measurement is carried out by varying the input power, PIN, from −20 to 20 dBm (Fig. 7).

Table 3 Performance comparisons with the reported Doherty power amplifiers

Reference	Description	PAE (%)	Pout (dBm)
[1]	Single-input Doherty PA	73.1	17.7
[2]	Dual-input Doherty PA with advanced phase alignment technique	59.9	44.5
This work	Dual-input Doherty PA	76.45	48.3

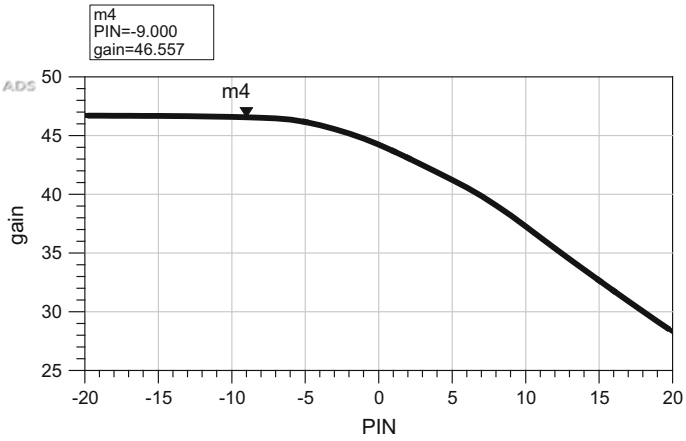


Fig. 5 Measured gain in dB

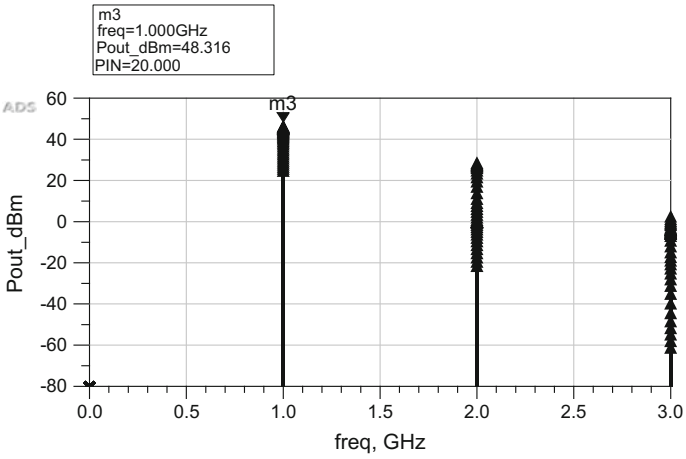


Fig. 6 Measured output power in dBm

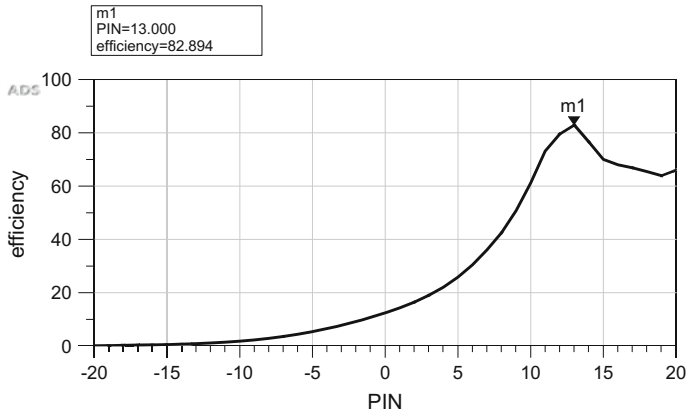
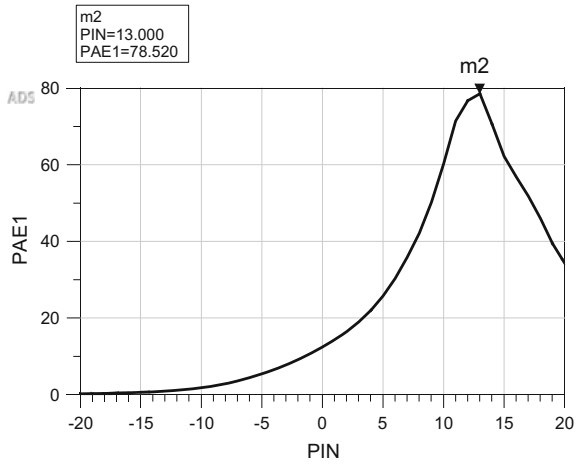


Fig. 7 Measured overall efficiency in %

Fig. 8 Measured power-added efficiency (PAE) in %



From Fig. 6, it is shown that maximum output power is obtained at a frequency of 1 GHz. In most of the previous works, maximum PAE is achieved at the expense of overall efficiency. The overall efficiency of this particular work is much greater than all previous works and is measured as 82.89%.

6 Conclusion

In this paper, a new architecture of digitally driven dual-input Doherty power amplifier is designed for the improvement of efficiency and maximum power-added efficiency of GaAs Doherty transmitters. In this architecture, direct access to the

main and auxiliary PAs' driving signals enables advanced signal processing that cannot be implemented in conventional fully analog single-input Doherty PAs. It makes use of DSMs to synthesize signals, and the step size of the signals represents the information to be transmitted. The measured PAE of the dual-input Doherty Power amplifier is higher than 74%. This represents a 3% improvement in comparison with the dual-input Doherty PA with adaptive phase alignment technique and 25% improvement over single-input standard Doherty PA. This increase is achieved without compensating the overall efficiency of the PA, which is 80%. Thus, a PAE of 76.4% is achieved at an average output power of 48.3 dBm. Better and much higher power efficiency can be achieved by replacing GaAs HEMT transistor with GaN HEMT.

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