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Jie Li
A. Ravi Sankar
P. Augusta Sophy Beulet
Editors

VLSI Design: Circuits, Systems and Applications

Select Proceedings of ICNETS2, Volume V

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Preface

This volume of the proceedings is the collation of selected papers presented in 'Symposium E' in the International Conference on NextGen Electronic Technologies—Silicon to Software—ICNETS2 conducted from March 23 to 25 at VIT, Chennai.

The development of microelectronics and VLSI design spans a time period, which is less than 50 years, but it has seen as many as four generations. Thus Symposium E—**'VLSI Design: Circuits, Systems and Applications'** provided an international platform for researchers and international speakers to present their research findings and innovative methodologies in various avenues of VLSI design.

The VLSI design symposium of ICNETS2 attracted 98 abstracts from different countries and also from within India. The full-length papers were reviewed by a panel of 40 reviewers from reputed technical institutions like Indian Institute of Technology (IIT), National Institute of Technology (NIT), Anna University; professors from abroad; and experts from industries along with the editors of this volume. After a meticulous review process, 61 papers were selected for oral presentation in the symposium. These papers were presented in nine parallel sessions conducted throughout the three-day conference. Three keynote talks were delivered in Symposium E on the following topics: radio-frequency integrated circuit design (Jie Li, University of Melbourne, Australia), an overview on memristor-based non-volatile LUT of an FPGA (T. Nandha Kumar, University of Nottingham, Malaysia), rare earth-doped semiconducting thin films for Si-based light-emitting devices (Christopher Labbé, Normandie University, France). The papers presented in each session were evaluated by two experts from academia and industries. Of the 61 papers presented in the symposium, 27 manuscripts were selected by the session chairs for this LNEE proceedings publication.

The selected papers span a wide spectrum of topics on low-power design techniques, analog and mixed-signal design, RF IC design, testing and verification of VLSI circuits, high-performance DSP architectures, architectures for hardware

security, memristor-based circuit designs, SOC designs, design of ADC, on-chip memories, etc. We the editors are happy in bringing up this volume which is a treasure for the budding VLSI researchers.

Melbourne, Australia — Jie Li
Chennai, India — A. Ravi Sankar
Chennai, India — P. Augusta Sophy Beulet

Acknowledgements

These few words of acknowledgment are too little to express our gratitude to the personnel, whose constant involvement and support made this proceedings possible.

Firstly, we would like to express our profound and heartfelt gratitude to Dr. G. Viswanathan, respected Chancellor of VIT, for bestowing his invaluable support in organizing the International Conference on NextGen Electronic Technologies—Silicon to Software—ICNETS2. We are indebted to the VIT management—Vice President, Mr. Sankar Viswanathan, and Assistant Vice President, Ms. Kadhambari, S. Viswanathan—for their encouragement and support in conducting the ICNETS2 conference in VIT Chennai, Chennai, India. This conference and associated symposia would not have been possible without the unlimited freedom extended by the management of VIT.

We are sincerely thankful to the Vice-Chancellor of VIT and the Pro-Vice-Chancellor of VIT Chennai for their constant guidance and timely input. Our special thanks are due to Chairman of ICENT2 Dr. S. R. S. Prabaharan and Co-chairwomen Dr. Nadia Magnenat Thalman and Dr. V. S. Kanchana Bhaaskaran for their help in organizing the symposium on VLSI Design: Circuits, Systems and Applications.

We would like to thank Dr. Ananiah Durai, Manager of the symposium, for his contribution in arranging the invited speakers not only for the symposium but also for the Industry-Government-Academia Forum. A special word of thanks to Dr. Nandhakumar for his technical talk on memristors and his valuable input and interaction during the technical sessions.

We owe a special gratitude to all the academic and industrial professionals who meticulously reviewed the technical manuscripts submitted to the symposium. We are thankful to the chairs of various technical sessions of the symposium for their constructive feedback and interaction with the authors of the manuscripts. We are also thankful to all the faculty members of the School of Electronics Engineering (SENSE), especially the faculty members related to VLSI and Nanotechnology group. We would also like to thank the research scholars of SENSE for their contribution to the symposium.

We sincerely thank all the committee members of ICNETS2. In particular, we would like to highlight and acknowledge the contribution of Dr. Mohanaprasad in bringing out this proceedings.

We are extremely grateful to the staff at Springer, especially Swati Meherishi and Aparajita Singh, for helping us in bringing out this volume comprising the selected manuscripts presented in the symposium of VLSI Design: Circuits, Systems and Applications, ICNETS2.

Contents

About the Editors

Dr. Jie Li received B.E. degree with first class honors and Ph.D. degree from Massey University, Auckland, New Zealand, in 2007 and 2012, respectively. He subsequently worked on mixed-signal IC designs, wireless and optical device integrations, IoT systems and applications. In April 2012, he joined the Centre for Energy-Efficient Telecommunications (CEET), a Bell Labs Research Center based on University of Melbourne as a Research Fellow, where he is developing circuits and systems for low-energy fiber access networks and wireless networks. He is currently an honorary fellow of EEE Department at University of Melbourne and the co-founder of MedRIVS Ltd, a technology company that delivers researches and solutions for medical devices and applications. He holds three international patents and has authored or co-authored more than 20 international journals and conference articles including several that were invited. He has served in the technical program committees of several international conference and journals.

A. Ravi Sankar received B.E. degree with first class in Electrical and Electronics Engineering from the University of Madras, India. He got admission to a postgraduate program through GATE 2001 examination and has obtained M.E. degree in VLSI Design from the Department of Electronics and Communication Engineering, PSG College of Technology, Bharathiar University, with a CGPA of 9.46/10 and stood first in the class. Subsequently, he joined the Department of Electronics and Electrical Communication Engineering, IIT Kharagpur, as a full-time institute research scholar and obtained Ph.D. degree in 2009. He worked as a project scientist at Advanced Technology Development Centre, IIT Kharagpur, for a period of 14 months for Indian Space Research Organization (ISRO)-sponsored projects and involved in design, fabrication, and testing of MEMS sensors. From 2009 to 2011, he worked as an Associate Professor in the Department of Electronics and Communications Engineering, Karunya University, Coimbatore. From June 2011, he is working as a Professor in the School of Electronics Engineering (SENSE), VIT, Chennai campus. His research interest includes MEMS and microsystems, silicon and glass micromachining, microelectronics and VLSI design and nanosensors. He has guided 20 M.Tech students for their postgraduate

project work and at present supervising six scholars toward their research degrees. He has published/presented around 40 papers in national and international journals and conference proceedings. He is a regular reviewer of various high-quality journals. He has served as the external expert examiner (of a doctoral thesis) at Anna University, Chennai, and also referred a couple of DST SERB project proposals. He was part of the team at IIT Kharagpur, which successfully developed country's first MEMS-based acceleration sensor for aircraft motion sensing applications.

P. Augusta Sophy Beulet received her bachelor's degree in Electronics and Communication Engineering from Government College of Engineering, Tirunelveli, Tamil Nadu, India, in 1988. After spending few years in teaching, she obtained her master's degree with specialization in 'VLSI Design' from Easwari Engineering College, affiliated to Anna University, Chennai, India, in 2006. She pursued her research in low-power VLSI architectures for DSP algorithms and received her Ph.D. degree from Anna University in 2015. With 25 years of teaching experience in various polytechnic and engineering colleges, presently she is working in VIT, Chennai. She has produced more than 15 research papers in peer-reviewed journals and guided more than 15 projects at the postgraduate level. Her research interests are high-performance VLSI architectures for signal processing algorithms and arithmetic circuits, low-power VLSI and reconfigurable architectures.

Front-End CMOS Circuit for Low Power Consumption

K. Dinesh Kumar and K. Ferents Koni Jiavana

Abstract The objective of the project is to design a CMOS circuit for a portable network. This CMOS circuit combines with instrumentation amplifier, switched capacitor, and proposed analog-to-digital converter. When the voltage is scaled to 1.8 V, the power consumption is reduced. The chopping method is introduced, and the 5 kHz is set for frequency; the frequency $1/f$ in the input transistor is less than the set frequency, and the electrode offset is suppressed by a dc servo loop. A low-pass SC filter is introduced to reduce the catches from the output of instrumentation amplifier. A successive approximation analog-to-digital converter is used to digitalize the signal. This CMOS circuit has been implemented in an 180 nm CMOS process.

Keywords Chopped capacitively coupled instrumentation amplifier (CCIA) Switched capacitor filter (SC filter) · Successive-approximation analog-to-digital converter (ADC) · Dc servo loop (DSL) · Low noise amplifier (LNA)

1 Introduction

Wireless network will monitor the patient's health without disturbing their daily activities. It will monitor the patient without a clinical environment [1]. This CMOS circuit is used for portable devices [2]. Signal quality and noise performance are determined by this circuit. This circuit achieves low power consumption, low noise, high common mode rejection ratio, and input impedance will be high [3]. Three high power efficiency modules are integrated into an analog front-end circuit to obtain these issues. The three modules are: (1) an instrumentation amplifier (IA); (2) a SC

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Fig. 1 Front-end circuit architecture

filter; (3) a proposed analog-to-digital converter, shown in Fig. 1. In instrumentation amplifier (IA), the chopper-stabilized technology is used due to its offset elimination, 1/*f* noise, power efficiency, and CMRR enhancement characteristics reduced [4]. And an implementation of the impedance boosting loop is done. For neglecting the catches, breaker, and high-frequency noise, the switched capacitor filter (SC filter) has been employed. A SAR ADC has been employed. It will reduce the static power consumption. All modules are proposed, even though there are some advantages. The power consumption is greatly reduced when the supply voltage is set. Second, a low-pass filter is used to realize a programmable gain and for the power hungry block. Third, a signal buffer is omitted when the output is given to the SAR ADC. Power consumption is greatly reduced by using these optimizations.

2 Front-End CCIA

The implemented front-end instrumentation amplifier (IA) for the acquisition is shown in Fig. 2. By the fraction of the C_{in} and the feedback capacitor C_{fb} ($A = C_{in}/C_{fb}$) the total gain is set. To obtain low noise density, the bias resistors R_{b1} and R_{b2} which are implemented in MOS transistors are operated in cut-off frequency with resistance of 100 GΩ. The noise performance of the amplifier is affected by 1/*f* noise factor. This problem is solved by chopping technique, and chopping frequency is 5 kHz.

The equivalent input resistance is 8.3 MΩ with 5 kHz frequency and capacitance of 12 pF. The implementation of positive feedback will enhance the input resistance. It comprises two capacitors C_{pf1} and C_{pf2} and a chopper CH_{fb}. To check that all

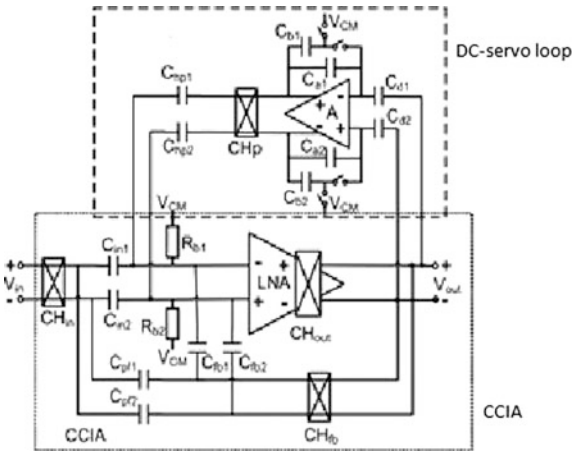


Fig. 2 Design of the chopped coupled instrumentation amplifier with DSL

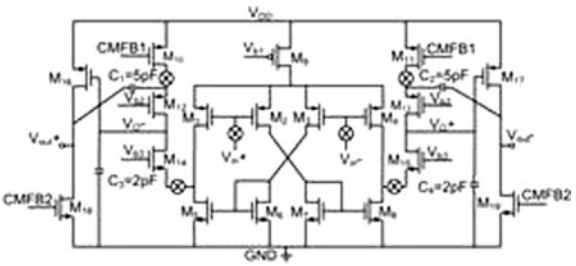


Fig. 3 Schematic of the LNA

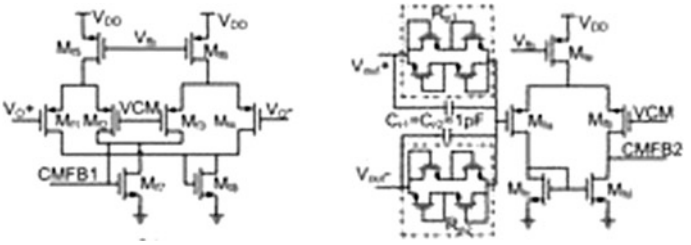


Fig. 4 Schematic of common-mode feedback circuit 1 and common-mode feedback circuit 2

switches function correctly in low voltage supply, a nonoverlapping clock generator is introduced with driver and it also increases the linearity. To neglect the electrode offset voltage DSL is needed. The bioelectrodes size and the materials are changed by input offset voltage amplitude. The power hungry block is LNA which amplifies the weak signal. To reduce the 1/*f* noise, PMOS transistors were chosen to be in input devices. A better open-loop gain is obtained with minimum current when a direct feedback loop is formed to hike the drain resistance. To ensure stability and filter, the spikes produced in the first stage is done by C_3 and C_4. IC has small value of 0.02, so gm is

$$\text{gm} \approx [\text{ID}/2\lambda\text{UT}]$$

Input transistors are tuned to small lengths and large widths to verify that they function in deep subthreshold region. ID must be large for high input gain. Noise of the CCIA is reduced by this way (Figs. 3 and 4).

3 SC Filter

To set the frequency band to reduce the noise and to neglect the spikes, low-pass filter is needed. Instead of large resistors, a low cut-off frequency can be achieved with the use of low-pass filter. Therefore, switched capacitor filter is employed in this front-end system. And the two-stage Miller-compensated amplifiers A_1 and A_2 are with large input. The amplifier must be large to achieve higher precision.

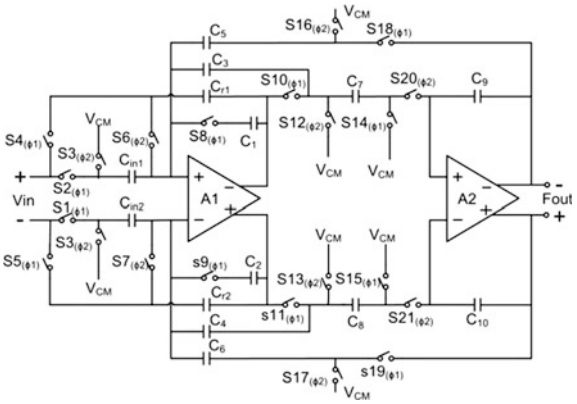


Fig. 5 Schematic of the switched capacitor filter

Two compensation capacitors C_{T1} and C_{T2} each of capacitance 200fF can be seen in the filter. The dc gain is 0 dB, and the tunable gain is realized to satisfy the variation in amplitude of biopotential signals (Fig. 5).

4 Successive Approximation ADC

The SAR ADC has lot of advantages for low-power circuit applications. Many peoples proposed their work in SAR ADC. The ADC with 10/12 bit is proposed by Harpe. The power consumption for this ADC is 97 nW. So, to reduce the power consumption, the comparator and the successive approximation logic is introduced here. The 10-bit successive approximation is performed here for low power consumption. Therefore, the sampling rate with 10 kHz is used in this ADC. The ADC consists of binary capacitor array. The proposed design is done in DAC. The function of ADC depends on control unit, capacitor array, and comparator. More energy is saved in this proposed design. The every capacitor in each array has numbers of unit capacitors (Fig. 6).

5 Table

Base paper work	Proposed work
Power = 1.3 μW	Power = 0.058 μW
Area occupies = 1 mm^2	Area occupies = 1.7 mm^2

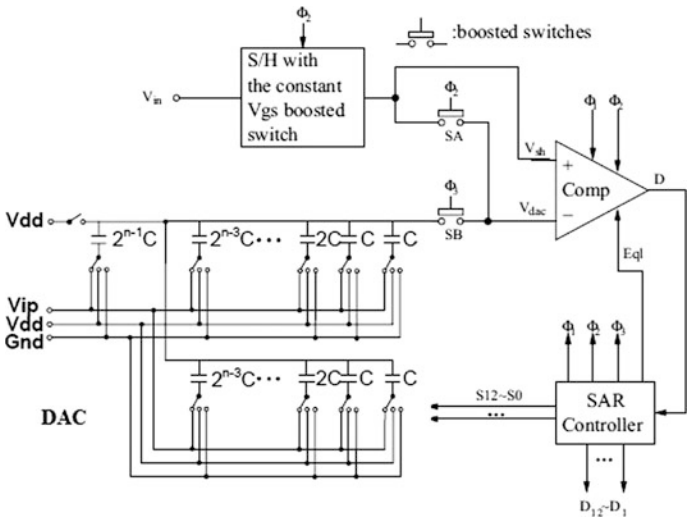
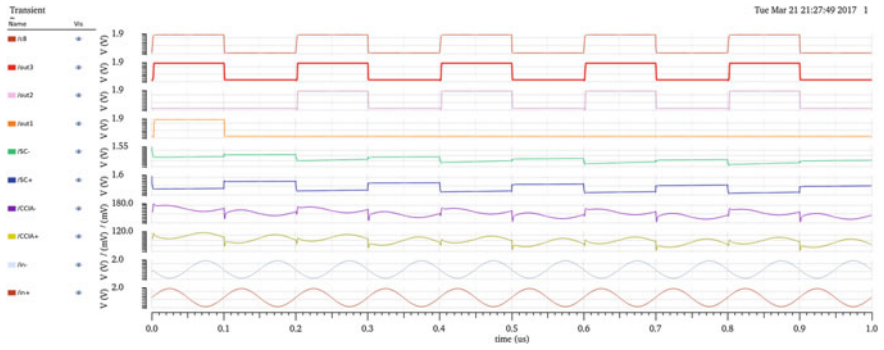


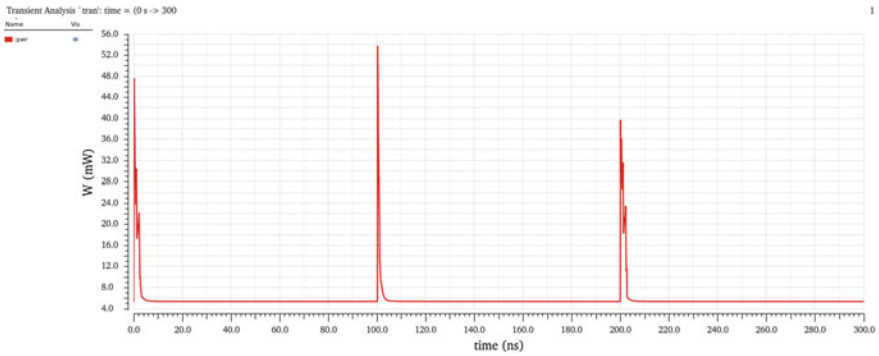
Fig. 6 Diagram of successive approximation ADC

6 Simulation Results

1. Output of front-end circuit



2. Power output



7 Measured Result

The front-end CMOS system has been designed using the 0.18 μm CMOS process; area is 1.7 mm^2, and noise is −102 dB. Clock has been set to each module to check whether the system operates properly or not. The amplifier is the major module in the system because it actuates the CMRR of the system and the noise performance. The sampling rate is 4 MHz, and the signal bandwidth is 25 kHz. The reduced power dissipation is 0.058 μW. Therefore, unity gain frequency is 24 MHz and settling time constant is 10 ns and slew rate is 14 V/ms. The switching capacitor is added that will reduce the spikes in the signal produced by CCIA. The SAR ADC is proposed in this CMOS circuit which samples the signal. And to reduce the noise, the SNR ratio of the input is merely 99 dB/95 dB, this will be the signal strength and quality.

8 Conclusion

A front-end CMOS circuit has been presented. An instrumentation amplifier (IA), a low-pass switched capacitor filter (SC filter), and SAR ADC have been designed. This Front-End CMOS circuit is designed in a 0.18-μm process. For the reduction of power, this analog CMOS circuit is suitable for portable biopotential applications.

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A Preliminary Study of Oscillators, Phase and Frequency Detector, and Charge Pump for Phase-Locked Loop (PLL) Applications

R. Prithiviraj and J. Selvakumar

Abstract The great advancement in CMOS technology, high speed and frequency, low jitter, low noise and phase noise, and less expensive phase-locked loop are very important in transceiver fields. This work aims at reviewing the performance of oscillators, phase and frequency detector (PFD), and charge pump (CP) for type-I PLL. In this work, the oscillators are reviewed as voltage-controlled oscillators (VCOs) and coherent-based phase-locked synchronous oscillator (CPSO). The phase and frequency detector is evolved as XOR gate PFD, double edge-triggered PFD, and digital pulse amplifier. The condition for stable operation and low-phase noise is established. The different types of oscillators and PFDs are reviewed. A detailed analysis of various methods to design oscillator, phase and frequency detector is provided. The best method to design phase and frequency detector is digital pulse amplifier. It minimizes the dead zone and phase error that can be easily recognized by flip-flop which is type D, and this amplifier has AND gates and is connected in series to raise the pulse width. The best method to design an efficient oscillator is the coherent phase-locked synchronous oscillator from various oscillators under study. It provides a method for improved frequency and lock-in range, capture range over the other oscillators. It retains the normal oscillator characteristics with less phase shifts across the frequency tuning and locking range.

Keywords Phase and frequency detector · Coherent phase-locked synchronous oscillator · Phase error

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1 Introduction

Phase-locked loop (PLL) is a feedback system which follows negative that compares the output frequency and phase with the input frequency and phase. It is widely used in frequency multiplier, frequency synthesizer, clock recovery, high-speed communication, clock generation, spread spectrum, clock distribution, jitter, noise reduction, deskewing, and high-speed communication systems [1]. The history of PLL goes long back to 1918 by the invention of superheterodyne. But there are high no of tuned stages as drawback. During 1930s, there were many experiments trying to compare the frequency of oscillator with input of phase detector, the results are led to the introduction of PLL by Henri de Bellesize [2]. In analog transceivers, PLL is locked to synchronized pulses in the broadcast signal. Since the PLL has been keeping on improving with lot of researches and advancement in various constraints of PLL such as lock-in range, hold in range, capture range, acquisition range, loop bandwidth, phase noise, and jitter. There are several variations of PLL. They are analog PLL (all blocks are analog), digital PLL (digital phase detector, analog VCO), all-digital PLL (ADPLL) (all blocks are digital), software PLL (all working blocks are implemented by software rather than specified hardware). This paper consists of V sections. Sect. 2 gives prior work of PLL, Sect. 3 gives overview of Digital PLL architecture, Sect. 4 gives modeling of PLL, and Sect. 5 presents conclusion.

2 Prior Work of PLL

The basic PLL has three building blocks, namely phase and frequency detector, loop filter, and voltage-controlled oscillator (VCO) [1]. The phase difference between the input signal and feedback signal is sensed by a phase and frequency detector, which changes the control voltage of VCO to make its feedback (or) output signal equal to the input signal. The operating states of PLL are unlocked, capture, and lock state. In unlocked state, PLL will be in open loop, where the VCO operates in natural frequency. In capture, PLL will be in closed loop, where the VCO frequency will be changed to make it synchronized with the input frequency. In lock state, phase noise and phase error are zero.

- In 2007, the linear capacitor is replaced by ferroelectric capacitor in VCO, which produce low cycle to cycle jitter because of its behavior of non-linear dielectric constant [3].
- By auto-correlating jittered signal, the jitter has been reduced. It is called jitter reduction technique [4].
- In 2010, the digital circuitry has been introduced to noise reduction from VCO. This was the first time, the VCO has been implemented using digital-distributed synchronous clock. But the drawback in the system is comparison of the clock

input with feedback clock is difficult due to the inaccuracy of digital to analog converter [5].

- In 2010, the charge pump has been replaced by integral path and proportional path where phase and frequency corrections are done separately. But the phase noise gets added up in both separate paths [6].
- In analog PLL, more number of algorithms has been presented and modeled [7, 8] to generate modeling of mathematical relations in order to verify the level of noise from all the blocks of PLL.

3 Overview of Digital PLL Architecture

A digital PLL consists of components, phase and frequency detector, charge pump, loop filter, and voltage-controlled oscillator. The basic component of phase detector is replaced by phase and frequency detector (PFD), and the PFD produce phase difference which is in the form of digital. The phase difference will be given to charge pump which acts as the control signal. The charge pump will generate the required VCO control voltage through loop filter. In place of voltage-controlled oscillator, the coherent phase synchronous oscillator (CPSO) has been replaced. The basic block-level architecture diagram of PLL is shown in Fig. 1. Different methods used to design these blocks are described in Fig. 1.

A. *Phase and frequency detector*

A phase detector is a component in DPLL, which produces the phase difference between the inputs, which is linear. Varieties of implementation have been seen in the literature on PFDs. The history of PFD goes long back to EXOR gate-based PFD as shown in Fig. 2. It was used for phase correction. The drawback in EXOR gate implementation is lack of sensitivity to edges.

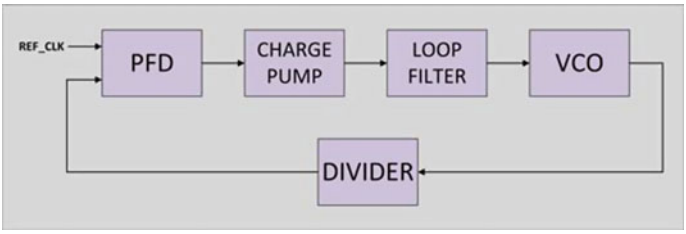

Fig. 1 Block-level architecture of PLL

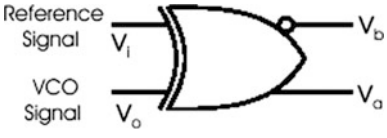

Fig. 2 EXOR implementation of phase detector

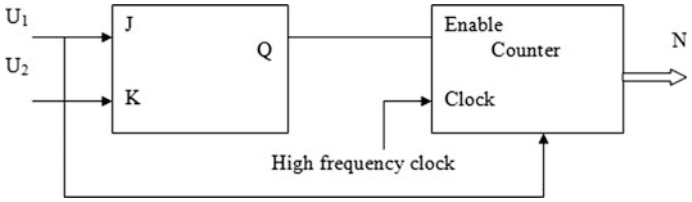

Fig. 3 Phase detector based on edge-triggered JK

This drawback can be overcome by edge-triggered JK operation. The drawback in this method is lack of sensitivity to edges as given in Fig. 3. This edge-triggered JK mechanism belongs to sequential phase detectors where EXOR PFD belongs to multiplier circuits [9].

Then it is improvised and presents the PFD with two-type D flip-flops and an AND gate. By using master slave-type flip-flop, the design specification on rise and fall time of the PLL can be achieved [10]. The phase difference, when it is very small, is very difficult to select. These phase error can get enlarged by using digital pulse amplifier (DPA) [11, 12]. DPA reduces the dead zone as well as fast detectable by D flip-flop. The DPA has AND gates connected in cascade to increase the pulse size (width) [11]. The design of DPA is shown in Fig. 4 [12]. Then after some years, PFD was designed by using Hilbert transform. In Hilbert transform, the input signal has been converted into analytic signal, by using Cartesian to polar conversion, the analytic signal has been converted into phase error.

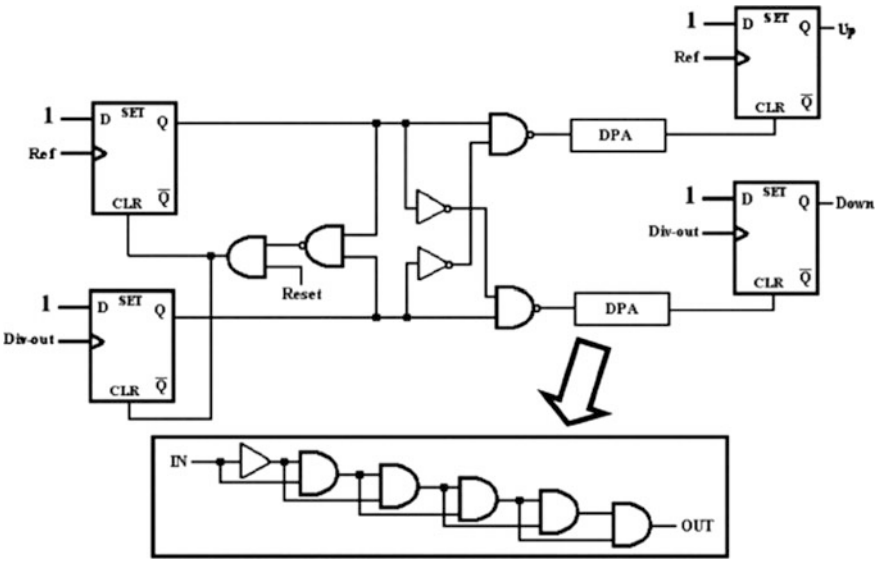

Fig. 4 Digital pulse amplifier

B. *Charge pump and loop filter*

A charge pump circuit converts digital signal to analog signal, to control the VCO. The PFD outputs, UP and DOWN signals will control the Q2 and Q3 MOSFET switch. When UP goes high, it will charge the Q3 MOSFET, when DOWN goes low, it will discharge the Q2 MOSFET. Q1 and Q4 act as current sources [13, 14]. The charge pump diagram is shown in Fig. 5. The type of loop filter which is chosen for the PLL is important property. The filter which is more suitable for lock time is type-I loop filter. It has low noise immunity [10].

Instead of charge pump, they have used the two types of deglitching filter circuit [15]. The proposed filter circuit will remove glitches from PFD, so that consumption power will be less and produces digital outputs (0, 1) according to the output of PFD [16]. The digital low-pass filter (LPF) is shown in Fig. 6.

C. *Proposed Voltage and Controlled Oscillator (VCO)*

The VCO is a main block of the PLL, which produce controllable oscillation. There are many types of VCOs. The VCO keeps on evolving with many features like low-power consumption, less area, wide tuning range, less complexity. LC VCO is one of the types of VCO. In [17] frequency-tripling technique in the VCO, with a single cross-coupled pair and dual tank topology, the wideband PLL demonstrated a wide tuning range increased with less power. However, LC-based oscillator has limitations such as high complexity, narrow tuning range, high power consumption

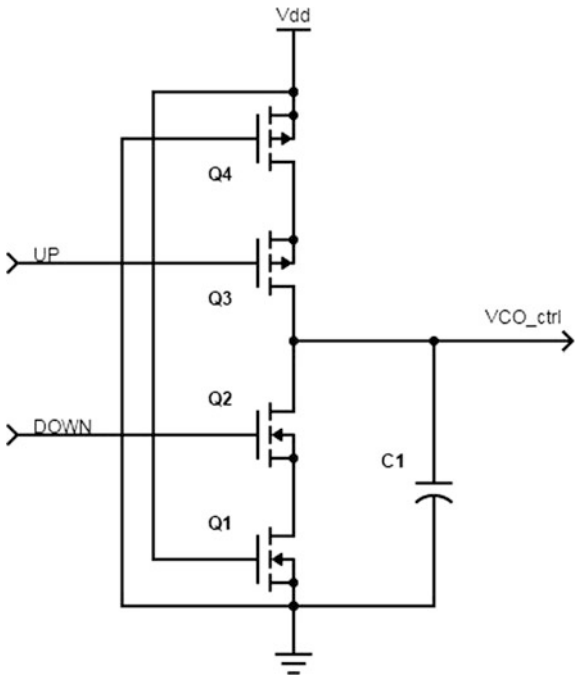

Fig. 5 Charge pump

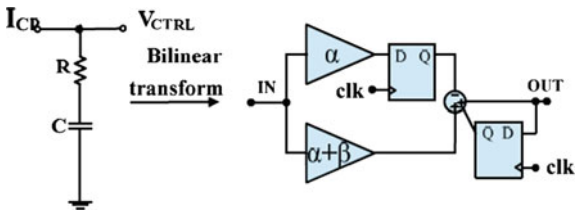

Fig. 6 Logical configuration of digital LPF

and large area [18–21]. The other type of VCO is ring oscillator. In Fig. 7, by using voltage to current converter, the supply current to the inverters is controlled based on the control voltage [22]. The capacitor will reduce the supply noise

The advanced oscillator is coherent-based phase synchronous oscillator (CPSO) [18]. It is shown in Fig. 8. The synchronous oscillator is operated by using the concept of injection locking. It has a basic circuit which consists of a parallel tank and a non-linear negative conductance shown in Fig. 8. V_i represents the signal given into the oscillator and g_m represents the transconductance of the V_i given device. At initial condition, the signal is given into the oscillator, the output is not phase locked to the given signal, which results in a frequency mismatch (Fig. 9). After many cycles, slowly the phase and frequency will be getting locked, the given oscillator is perfectly synchronized with the injected signal as shown in Fig. 10.

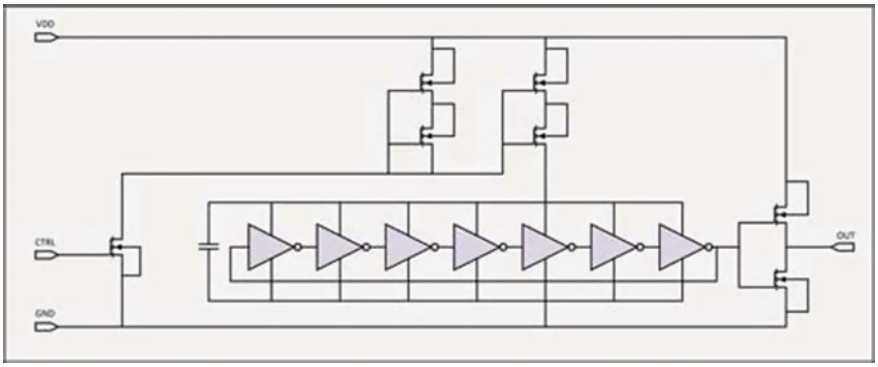

Fig. 7 Ring voltage-controlled oscillator

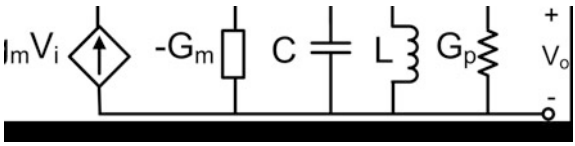

Fig. 8 Negative resistance model of synchronous oscillator

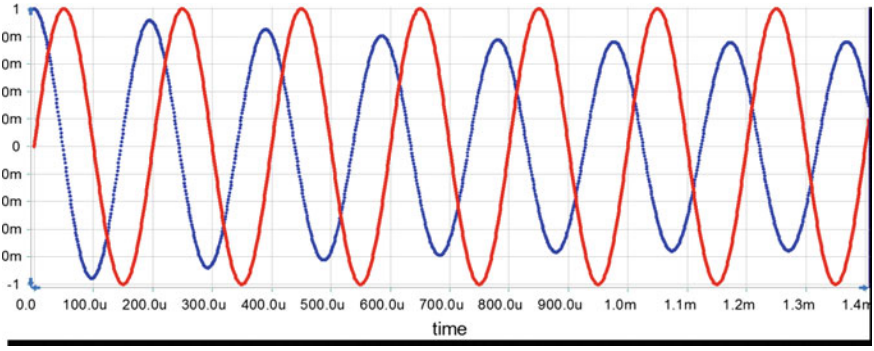

Fig. 9 Unsynchronized initially

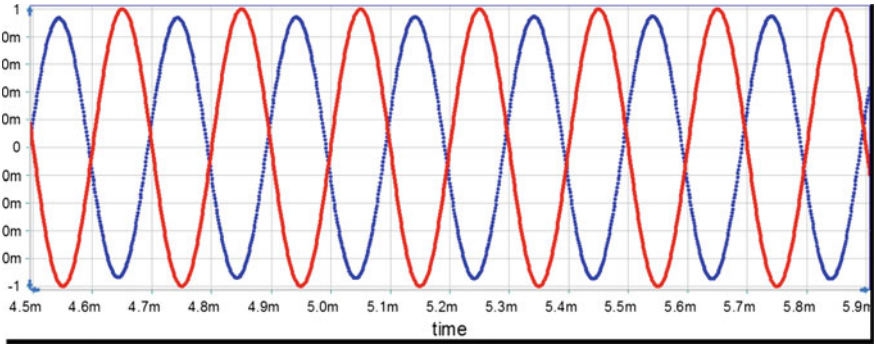

Fig. 10 Synchronized after many cycles

4 Modeling of Basic PLL

Different parameters of PLL like stability, lock-in range, loop bandwidth can be analyzed in phase domain.

D. *Phase model of PLL*

The PLL consists of three main functional blocks as shown in Fig. 1. The phase parameter and transfer function of PFD (Fig. 11), Charge pump and Loop filter (Fig. 12) and VCO are stated below.

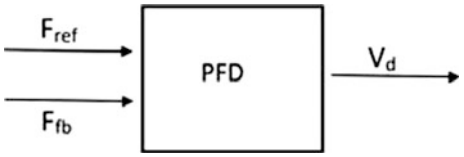

Fig. 11 Phase and frequency detector

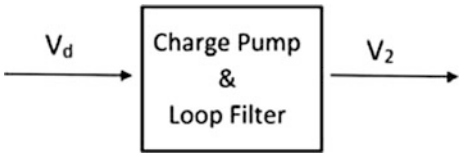

Fig. 12 Charge pump and LPF

Phase detector:

$$[F_{\text{ref}}(s) - F_{\text{fb}}(s)]K_{\text{d}} = V_{\text{d}}(s) \tag{1}$$

$$H_{\text{lpf}}(s) = \frac{v_2(s)}{v_{\text{d}}(s)} = \frac{1}{cs} \tag{2}$$

VCO:

The loop filter will produce the control voltage which is fed into VCO. The output frequency gets altered according to the control voltage, so the transfer function of VCO is given as

$$H_{\text{vco}}(s) = \frac{F_{\text{out}}(s)}{v_2(s)} = \frac{k_{\text{v}}}{s} \tag{3}$$

5 Conclusion

This paper presented a different analysis of various techniques to design the PLL blocks. From the different methods to design phase and frequency detector, digital pulse amplifier is the best method since it produces less dead zone. Charge pump and loop filter can be done by bilinear transformation of RC loop filter. The best VCO is coherent-based phase synchronous oscillator with improved coherency, lock-in range with less phase noise. If the entire best block can be put together in the DPLL with various constraints such as lock-in time, power consumption, acquisition time, tuning range can be evaluated and compared with existing DPLL.

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All-Digital RF Transmitter with Highly Power-Efficient Doherty Power Amplifier

Deepa Pradeep and B. Ananda Venkatesan

Abstract In this paper, a new architecture of an all-digital RF transmitter is proposed. It makes use of delta-sigma modulators for signal synthesizing followed by a dual-input Doherty power amplifier with an efficient design approach. Delta-sigma modulator produces two out-of-phase signals, each of these signals is fed separately into the main and auxiliary power amplifiers of the dual-input Doherty power amplifier, and thereby, the transmitter overcomes the linearity issues. It demonstrates quiet comparable performances: more than 75% of power-added efficiency at a maximum output power of 48.3 dBm, with an overall efficiency greater than 80% for a frequency range from 0.9 to 1.1 GHz.

Keywords Delta-sigma modulator · Doherty power amplifier · Digital transmitter Digital to analog converter · HEMT

1 Introduction

In this digital world, it is very much necessary to have a highly power-efficient transmitter for the transmission of digital signals. This paper presents an all-digital RF transmitter with maximum power-added efficiency and better overall efficiency. It makes use of simple functional blocks and is beneficial to WLAN/WCDMA applications.

In a previous work mentioned in [1], an FPGA had been used for synthesizing signals by combining the outputs of eight DSMs and this provided an advantage of better coding efficiency. These synthesized signals were then power amplified by using a Doherty power amplifier and gained a power-added efficiency more than 40%

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with the expense of linearity. Another type of digital transmitter is proposed in [2], where adaptive phase alignment technique was used to compensate for linearity issues. This required additional hardware, and PAE reported was less than 50%. In addition to that, it required a tunable BPF to maintain high power efficiency.

Different types of digital transmitters are digital polar transmitter [3] and digital outphasing transmitter [4]. A digital-intensive polar transmitter had been proposed in [5]. It had a PAE of 35% and eliminated AM predistortion. In this paper, a new architecture of an all-digital RF transmitter with highly power-efficient power amplifier is proposed. The proposed design consists of simple functional blocks, and the basic functional blocks are discussed in Sect. 1. It makes use of dual-input Doherty power amplifier, and its design method is specified in Sect. 4.

2 Transmitter Structure

The structure of proposed all-digital RF transmitter is depicted in Fig. 1. It consists of two delta-sigma modulators (DSMs), a multiplexer acting as a digital upconverter, digital-to-analog converter (DAC), a low-pass filter (LPF), and a power amplifier (PA).

The two DSMs synthesize anti-phase signals. DSM is fed by pulse signals of frequency 25 MHz, which is then converted to almost-analog signals by the DSMs. A 2:1 multiplexer acts as a digital upconverter, it is provided with a control signal of 1 GHz, and this results in fast multiplexing and produces a signal of frequency 1 GHz. A digital-to-analog converter (DAC) is used to convert almost-analog signals to analog signals. And finally, an LPF is used to filter out the unwanted signals with a cutoff frequency of 1 GHz. These signals are further power amplified by using a dual-input Doherty power amplifier. The use of anti-phase signals eliminates linearity issues, thereby increasing the efficiency of the transmitter.

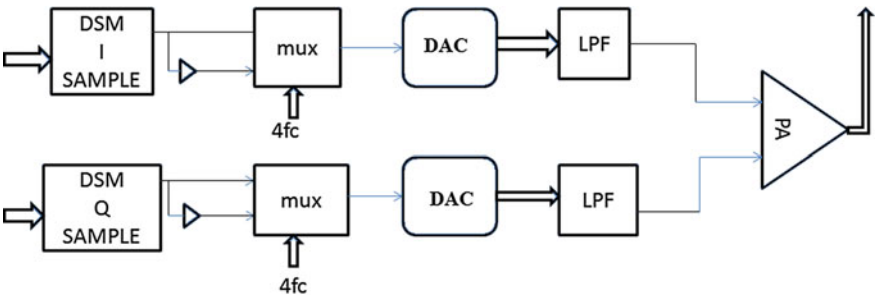


Fig. 1 Structure of the proposed transmitter

3 Signal Synthesizing

Delta-sigma modulator is derived from delta modulator. Figure 2 shows the structure of a delta-sigma modulator. It comprises an integrator, quantizer, DAC, and a D latch as the storage element. Figure 2 represents a first-order delta-sigma modulator. Vin(t) represents the input signal, and corresponding to the input signal, the delta-sigma modulator generates the output, Vout(t). The feedback signal F(t) is extracted from Vout(t) and is fed to the input terminal. The difference between input signal Vin(t) and feedback signal F(t) gives E(t), the quantization error. The errors have been accumulated by the integrator and then further send to the comparator to produce the required output signal; thus, the comparator acts as a quantizer. Thus, DAC converts high and low digital pulses into high and low voltage levels. Since delta-sigma converts an input from one domain to another, amplification is undesirable, and the feedback loop and the DAC must have a gain of 1.

The main block of a DSM is the integrator, and it decides the speed and performance of DSM. Integrator used here is a resistor–capacitor network which accumulates the received input signals; quantizer is a comparator; for this work, a 2:1 multiplexer is used as a comparator with a control signal, Fdsm, of 25 MHz. It generates one or zero based on the input. The comparator output is stored in a low power latch, which is a D flip-flop. The negative feedback path consists of a DAC and is compared with the input by using a subtractor. This results in generation of step signals, where the step size represents the information to be transmitted. The output of DSM is upconverted by using a 2:1 multiplexer, with a control signal of four times the input frequency. It results in fast multiplexing producing signals of frequency 1 GHz. The digital signal is then converted into analog signals by using a digital-to-analog converter (DAC). DAC is basically a multiplexer where the output of the digital upconverter acts as the control signal and inputs as positive and negative reference voltages. Unwanted signals are filtered out by using a low-pass filter (LPF) (Fig. 3).

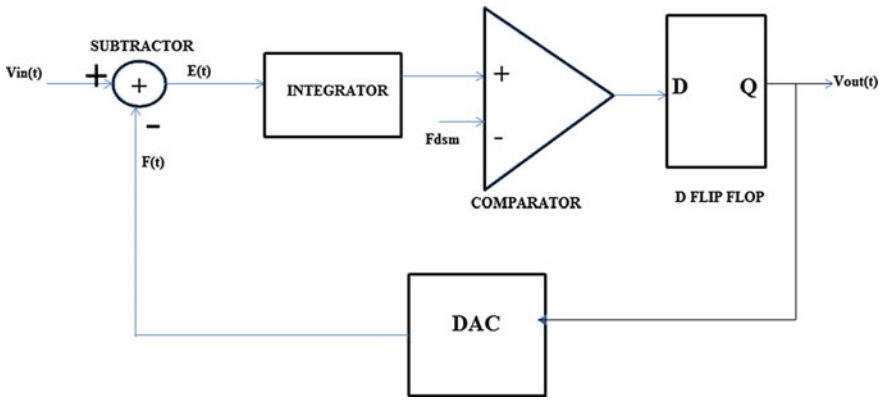


Fig. 2 Block diagram of delta-sigma modulator

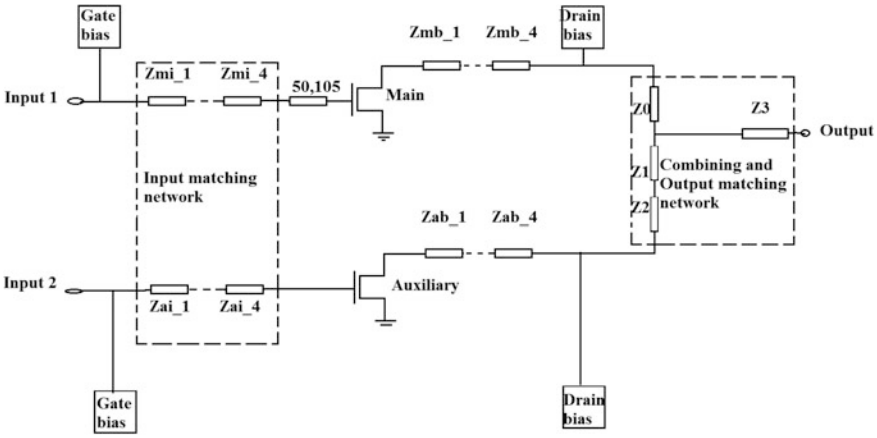


Fig. 3 Circuit diagram of the realized dual-input Doherty power amplifier. The impedances of main and auxiliary power amplifiers are Zm and Za, respectively

4 Dual-Input Doherty Power Amplifier Design

A dual-input digitally driven GaAs Doherty power amplifier is used in this work. The digital inputs to the amplifier are preprocessed as mentioned above. The main aim of using dual-input Doherty power amplifier is to compensate for linearity issues. Doherty power amplifier consists of a class AB biased main amplifier and class C biased auxiliary amplifier. The transistor used is ATF-54143 GaAs HEMT, and its biasing is done as per its datasheet. The matching networks of the main and auxiliary amplifier have been designed to maximize the efficiency and power-added efficiency at peak power. Peak power optimal load impedances are obtained by using load-pull simulations. Load-pull simulations of class AB and class C amplifiers are shown in Fig. 4. In this design, the transistors used are symmetrical and identical in size. The phase difference between the signals is established by adding a delay element. Dual-input Doherty power amplifier does not require any power-splitting network, and at the output, it makes use of combining network whose characteristic impedances are given in Tables 1 and 2.

5 Simulation Results

The proposed dual-input Doherty transmitter is built, as shown in Fig. 1, by using Advanced Design System (ADS) tool. The dual-input Doherty PA is designed by using microstrip lines instead of lumped elements, and it results in decreased size of the transmitter. The digital signal synthesizing is done by using DSM, multiplexer, DAC, and LPF. This generates a signal of frequency range 0.9–1.1 GHz. To

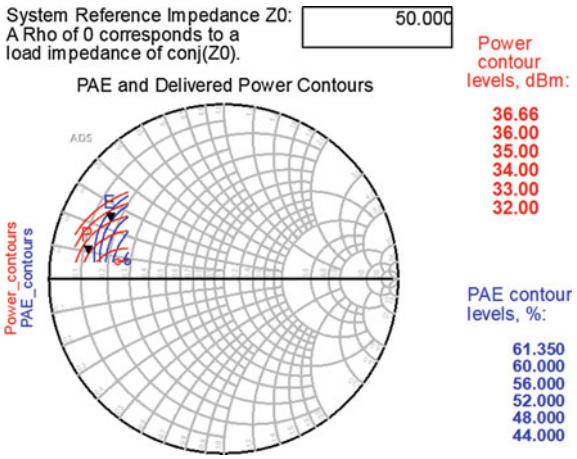


Fig. 4 One-tone load-pull simulation with input power PIN swept between −20 and 20 dBm. Output power and PAE found at each fundamental or harmonic load for the main and auxiliary amplifiers

Table 1 Determined characteristic impedances and electrical lengths of the microstrip lines in the input matching network at a frequency of 1 GHz

Zm1 (Ω)	θm	Za1 (Ω)	Θa
68.2	9.1	68.2	9.1
20.8	15.4	20.8	15.4
49.0	12.3	49.0	12.3
29.6	24.5	29.6	24.5

Table 2 Determined characteristic impedances and electrical lengths of the microstrip lines in the output matching network and combining network at a frequency of 1 GHz

Zmb (Ω)		θmb		Zab (Ω)		Θab	
33.0		16.9		8.3		20.3	
75.8		25.6		73.5		20	
20.0		12.2		6.8		23.0	
31.5		25.0		80.2		29.4	
Z0 (Ω)	θ0	Z1 (Ω)	θ1	Z2 (Ω)	θ2	Z3 (Ω)	θ3
42.0	82	42	85	35	85	20	70

demonstrate the flexibility of the proposed transmitter, the main and auxiliary PAs are excited separately by the synthesized signals and one arm of the input is provided with a delay element. This introduces a phase difference between the input signals, which eliminates linearity issues. Linearity measures are analyzed by using harmonic simulation in ADS.

Power-added efficiency (PAE) is defined as the metric for rating the efficiency of a power amplifier and is calculated and analyzed with the previous works, as given in Table 3 (Fig. 5).

The PAE measured is shown in Fig. 8 and is recorded to be 78.5% with a maximum output power, Pout, of 48.3 dBm, as shown in Fig. 6. PAE measurement is carried out by varying the input power, PIN, from −20 to 20 dBm (Fig. 7).

Table 3 Performance comparisons with the reported Doherty power amplifiers

Reference	Description	PAE (%)	Pout (dBm)
[1]	Single-input Doherty PA	73.1	17.7
[2]	Dual-input Doherty PA with advanced phase alignment technique	59.9	44.5
This work	Dual-input Doherty PA	76.45	48.3

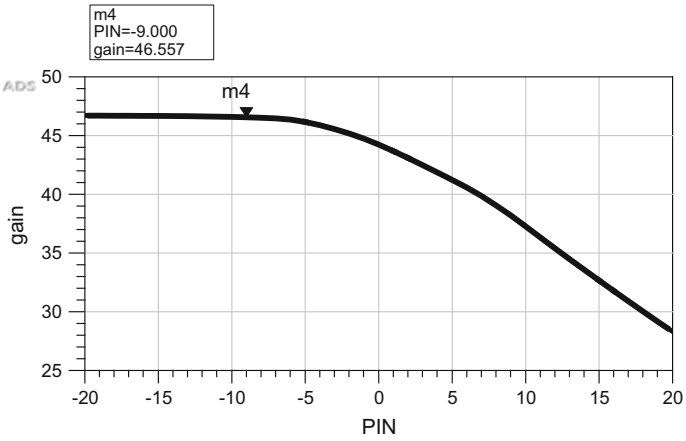


Fig. 5 Measured gain in dB

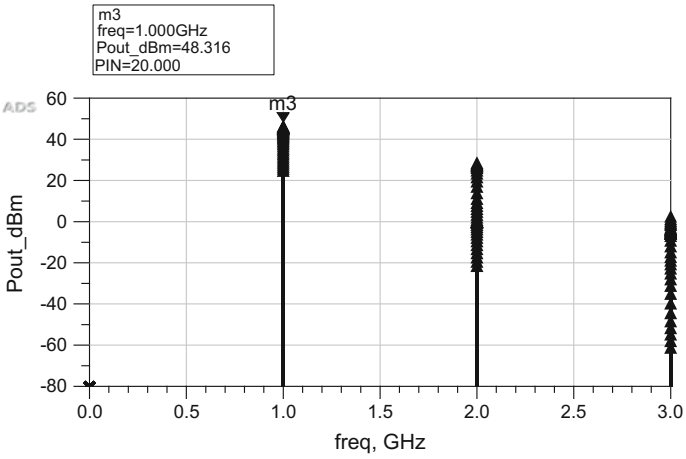


Fig. 6 Measured output power in dBm

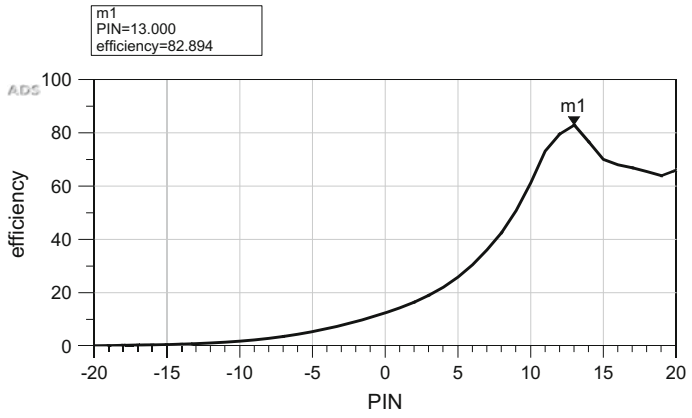
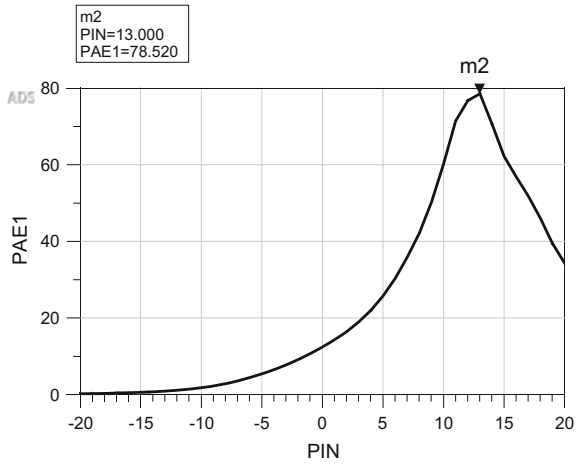


Fig. 7 Measured overall efficiency in %

Fig. 8 Measured power-added efficiency (PAE) in %



From Fig. 6, it is shown that maximum output power is obtained at a frequency of 1 GHz. In most of the previous works, maximum PAE is achieved at the expense of overall efficiency. The overall efficiency of this particular work is much greater than all previous works and is measured as 82.89%.

6 Conclusion

In this paper, a new architecture of digitally driven dual-input Doherty power amplifier is designed for the improvement of efficiency and maximum power-added efficiency of GaAs Doherty transmitters. In this architecture, direct access to the

main and auxiliary PAs' driving signals enables advanced signal processing that cannot be implemented in conventional fully analog single-input Doherty PAs. It makes use of DSMs to synthesize signals, and the step size of the signals represents the information to be transmitted. The measured PAE of the dual-input Doherty Power amplifier is higher than 74%. This represents a 3% improvement in comparison with the dual-input Doherty PA with adaptive phase alignment technique and 25% improvement over single-input standard Doherty PA. This increase is achieved without compensating the overall efficiency of the PA, which is 80%. Thus, a PAE of 76.4% is achieved at an average output power of 48.3 dBm. Better and much higher power efficiency can be achieved by replacing GaAs HEMT transistor with GaN HEMT.

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Adiabatic Techniques for Energy-Efficient Barrel Shifter Design

K. Anantharaman and A. V. M. Manikandan

Abstract One of the efficient ways to design a low power consumption logic style is the adiabatic logic circuits. This is far better than conventional CMOS logic in terms of power consumptions, delay, and efficiency. This paper explains the design of a 4-bit Barrel shifter using two different adiabatic logics, namely positive feedback adiabatic logic (PFAL) and pass transistor adiabatic logic (PAL). A Barrel shifter is effectively used in arithmetic and logical operations. PFAL utilizes positive feedback technique. The structure contains an adiabatic amplifier. The latch of PFAL is made by two PMOS and two NMOS transistors that avoid logic level degradation at output nodes. Energy recovery in the recovery phase of the clock supply results in a reduction in the power consumption. However, it is not suitable to the application where the delay is critical as the PFAL suffers from large switching time. PAL is a dual-rail adiabatic logic with low gate complexity. It also operates in two-phase power clock. With the use of PFAL and PAL logics, we are going to design 4-bit Barrel shifter. The circuit simulation is performed on Cadence Virtuoso using 180-nm CMOS technology. The parameters such as delay and power dissipation are calculated. From the simulation results obtained, it shows PAL adiabatic logic is more efficient than PFAL adiabatic logic because of reduction of non-adiabatic losses in PAL.

Keywords Barrel shifter · Adiabatic logic · PFAL · PAL · Multiplexer Cadence · Virtuoso

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1 Introduction

In the early days, low-power IC design techniques were not always required. But today, low-power design is necessary for all electrical design to reduce the power consumption of the devices. Minimizing of the supply voltage, circuit complexity, clocking frequencies, and many others are the common goals of low-power designer. The above parameters are reduced to an extent but, however, which is limited by other parameters such as noise margin and threshold energy.

One of the common techniques which can be used to minimize energy loss is the adiabatic logic. It can be used in analog as well as digital logic design. It can incur two types of losses. Their types are classified into adiabatic loss and non-adiabatic loss. The adiabatic loss cannot be avoided. The non-adiabatic loss can be reduced to an extent. Adiabatic logic is divided into two types [1]. They are Quasi/Partial adiabatic logic and Full adiabatic logic. Partial adiabatic logic will have a simple design and easy to implement while Full adiabatic logic has a complex design. The adiabatic loss will occur in Partial adiabatic logic when current flows through non-ideal-switch. Non-adiabatic loss can be greatly reduced in Full adiabatic logic.

Partial/Quasi adiabatic logic families include efficient charge recovery logic (ECRL), two-phase clocked adiabatic static CMOS logic (2PASCL), and positive feedback adiabatic logic (PFAL). Full adiabatic logic includes pass transistor adiabatic logic (PAL) and split-rail charge recovery logic (SCRL) [2].

Barrel shifter is used in microprocessors. They are essential for designing of the data path for DSP algorithms. They will typically shift the data in arithmetic and logical manner [3]. The main difference with the universal shifter is that Barrel shifter will shift "*n*" bit in one cycle, but universal shifter register does one-bit shift in one cycle.

In this paper, we presented two types of adiabatic logics. One is from Partial/Quasi adiabatic logic, i.e., positive feedback adiabatic logic (PFAL) and another is from Full adiabatic logic, i.e., pass transistor adiabatic logic (PAL) [4]. The basic structures of these two types are defined, and 2:1 Multiplexer is created from these logics which is the basic building block of Barrel shifter. From the implemented logics, parameters such as power and delay are calculated which show the efficient logic between these two.

2 Multiplexer

2.1 Positive Feedback Adiabatic Logic (PFAL)

It comes under the category of Partial/Quasi adiabatic logic. It is also called partial energy recovery circuit. It is a dual-rail circuit. It provides good robustness against technical variations. Two *n*-trees provide the logical function which contains NMOS transistors only. It is connected in parallel to PMOS. Totally, ten NMOS

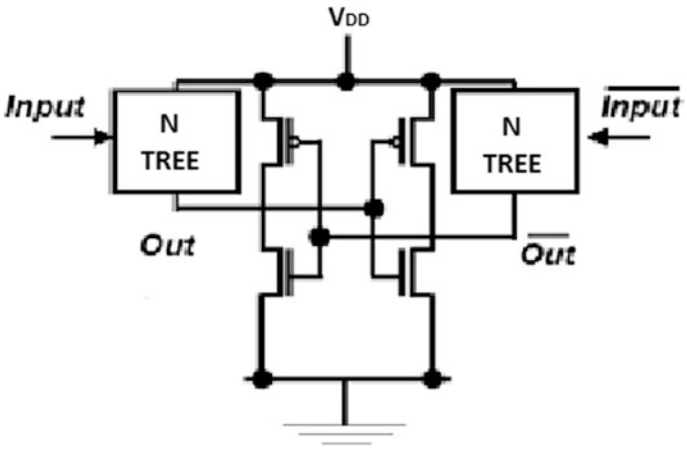

Fig. 1 Block diagram of positive feedback adiabatic logic

and two PMOS are used in the circuit. Two cross-coupled inverters and two functional blocks (*N*-Tree) form true and its complementary output of the given function [5].

In PFAL, the latch is formed by adding two PMOS and two NMOS [6]. The latch can avoid logic level degradation on the output nodes. PMOS transistor will determine the charging path resistance. Decreasing the charging path, resistance of the circuit will improve the performance of the circuit. Due to this logical style of PFAL circuit, the equivalent resistance is smaller when capacitance needs to be charged. The logical diagram of PFAL is given in Fig. 1. From this logic, Multiplexer is implemented. The designed Multiplexer is used to form Barrel shifter (Fig. 2).

2.2 Pass Transistor Adiabatic Logic (PAL)

It comes under the category of Full adiabatic logic. It is one type of dual-rail logic style which is implemented in an adiabatic logic. The complexity is somewhat less when compared to other Full adiabatic logic styles [1]. It evaluates in two phases. They are evaluation phase and recovery phase. In the evaluation phase, clock rises from zero to V_{dd} to the circuit. In the recovery phase, clock returns to zero from V_{dd}. In the recovery phase, energy is recycled back to power clock generator.

It is proposed to eliminate the precharge diodes. But it also suffers from closed recovery path. It consists of two PMOS and eight NMOS in the logical design. Two *n*-trees will produce the logical function. The logical deign will produce the true and complementary outputs of the given function [4]. The logical diagram is given in Fig. 3. From this, Multiplexer is implemented. The designed Multiplexer is used to form Barrel shifter (Fig. 4).

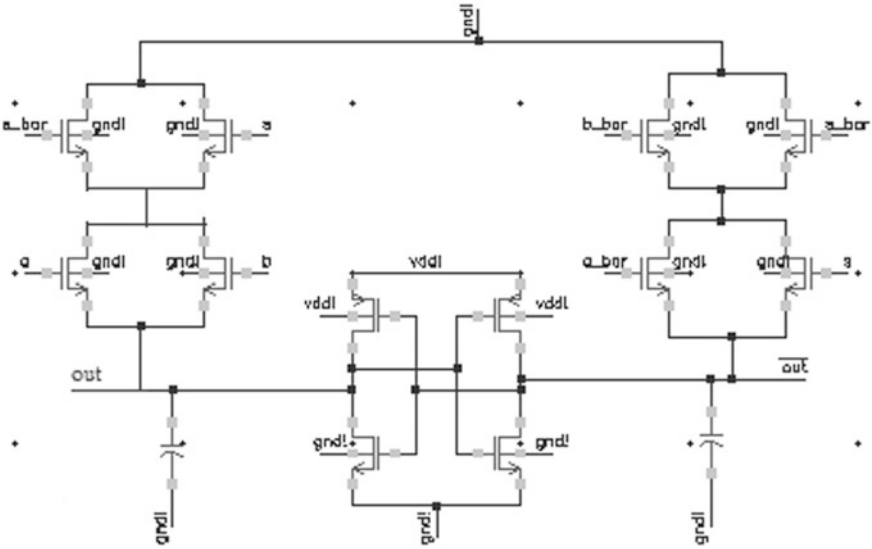

Fig. 2 Schematic of positive feedback adiabatic logic (PFAL)

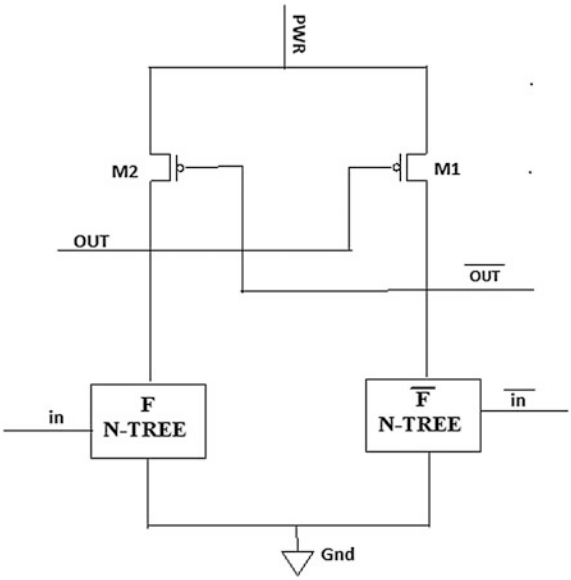

Fig. 3 Block diagram of pass transistor adiabatic logic

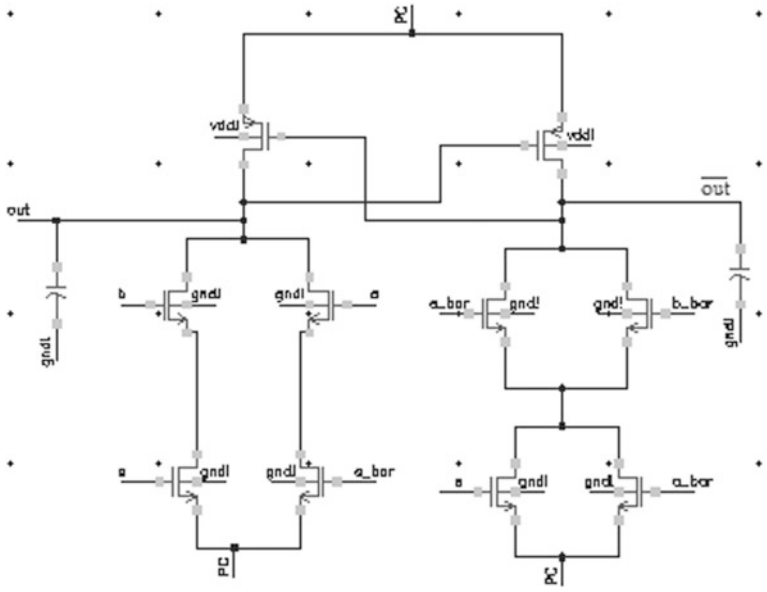

Fig. 4 Schematic of pass transistor adiabatic logic (PAL)

3 Barrel Shifter

It is a functional unit which can be used in a number of different circumstances. It is usually used to give directions of shift and rotation function operation [3]. It can also use to specify the type of shift (circular, arithmetic, or logical) and the amount of shift (typically 0 to $n - 1$ bits). The clock input will specify the number of bits which will be rotated. Even though it is complex to implement, it is always used in the design of data paths in DSP Algorithms.

It is almost symmetric. They are many ways to implement the shifter, but the most common method is to use the MUX to realize the design. The MUX design reduces the power consumption of the circuits. The basic building block of the Barrel shifter is 2:1 MUX. For 4-bit Barrel shifter, it contains 4-bit inputs & outputs and 2-bit select lines. Figure 5 represents the implementation of 4-bit Barrel shifter.

The rectangular box drawn in Fig. 3 indicates 4-bit Barrel shifter. The given circuit will perform the rotation operation. For each one-bit change in select lines, there will be a change in rotation operation; here, it will rotate up to three bits at a time for a single clock pulse. The implemented circuit will produce only left rotation (Table 1).

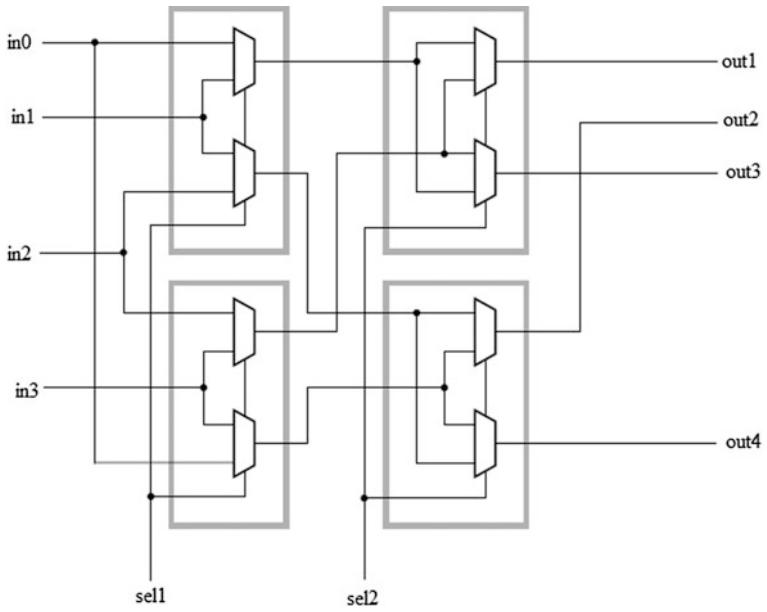

Fig. 5 4-bit Barrel shifter

Table 1 Rotation process

SEL2	SEL1	Process
0	0	No rotation
0	1	1-bit rotation (left)
1	0	2-bit rotation (left)
1	1	3-bit rotation (left)

3.1 PFAL 4-Bit Barrel Shifter

See Fig. 6.

3.2 PAL 4-Bit Barrel Shifter

See Fig 7.

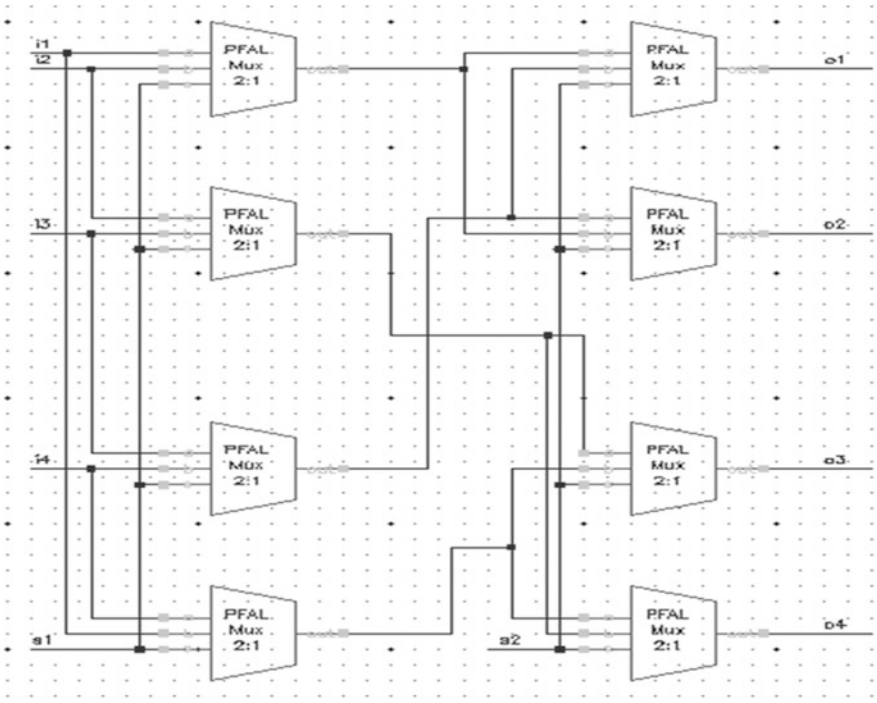

Fig. 6 4-bit Barrel shifter implemented in PFAL

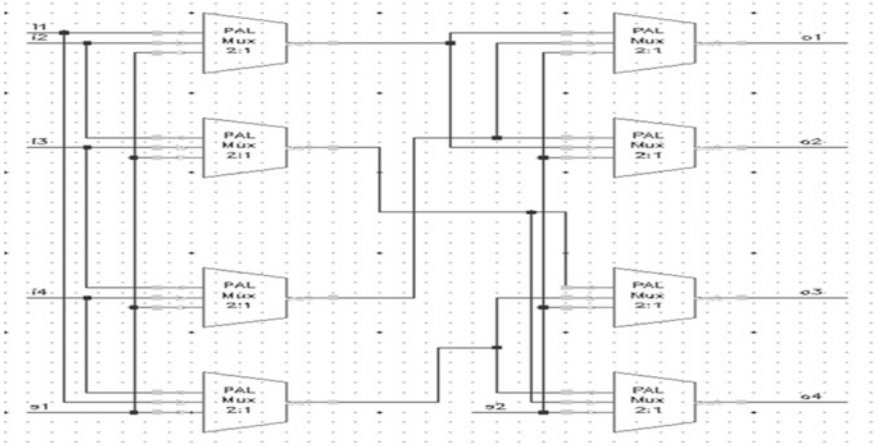

Fig. 7 4-bit Barrel shifter implemented in PAL

4 Simulation Results

4.1 PFAL 4-Bit Barrel Shifter

See Fig. 8.

4.2 PAL 4-Bit Barrel Shifter

See Fig. 9.

The simulated results show the rotation operation of the proposed work. According to the selection lines (SEL1 and SEL2), the outputs are rotated in left. The outputs will copy the inputs according to the selected line. The outputs are left rotating for every change in selection lines (SEL1 and SEL2).

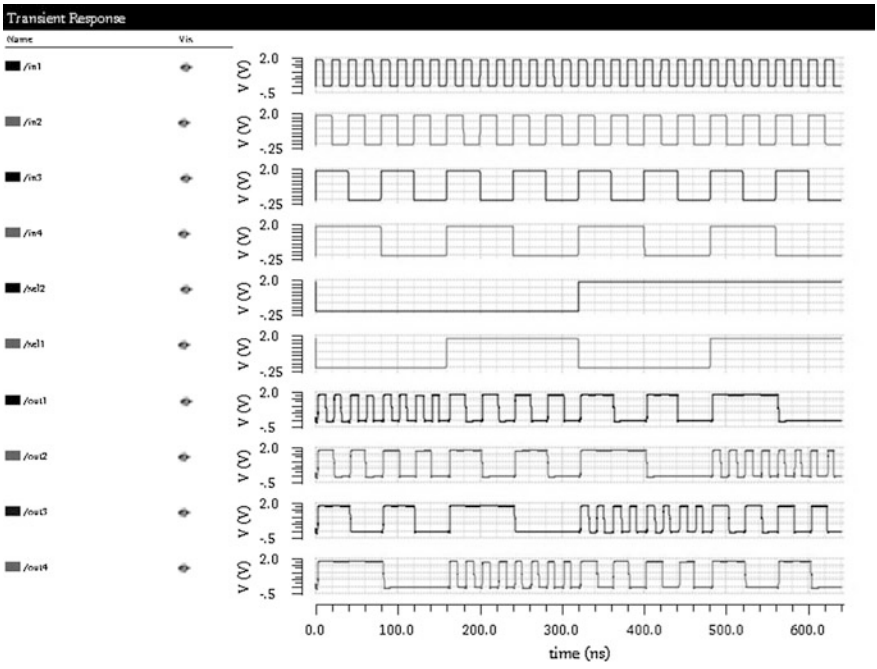

Fig. 8 4-bit Barrel shifter output in PFAL

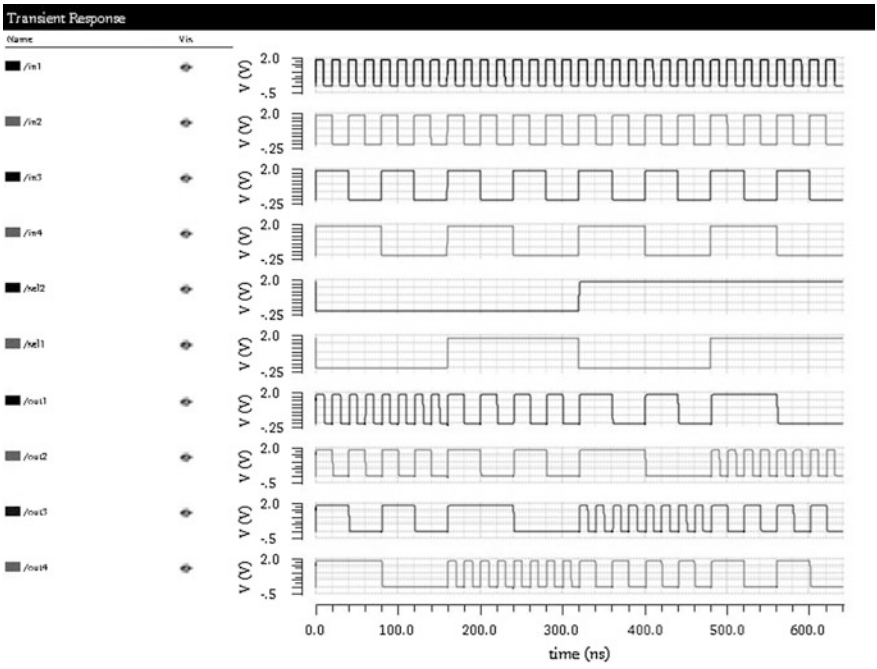

Fig. 9 4-bit Barrel shifter output in PAL

5 Specification and Comparison

The Barrel shifter is implemented using Cadence Virtuoso Analog Design Environment for TSMC 180-nm CMOS Technology process. A capacitor load is connected at the output node. The parameters which are used in the design are given in Table 2. The simulated results are given in Figs. 6 and 7 (Table 3).

Table 2 Specification table

Specifications	Values
Technology	180 nm
Power supply	1.8 V
Length of PMOS transistor	7.2 µm
Width of PMOS transistor	180 nm
Length of NMOS transistor	3.6 nm
Width of NMOS transistor	180 nm

Table 3 Comparison table

Parameters\types	PFAL	PAL
Delay	502.70 ps	90.34 ps
Power dissipation	6.51 mW	3.19 mW

6 Conclusion

In this paper, the 4-bit Barrel shifter is designed in two different adiabatic logics and different parameter variations among two different adiabatic logic families are investigated. Circuit simulation shows that PAL is more advantageous than PFAL. The parametric comparison shows that delay and power dissipation in PAL are reduced than that of PFAL. It can be used instead of conventional CMOS logic structure for smaller circuits in which it effectively reduces power consumption and delay. The higher-order Barrel shifter can be produced. It can be used in ALU operations to perform shifting operations.

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A 79 GHz CMOS LNA with Adaptive Biasing

D. Rubeena and J. Manjula

Abstract This paper proposes a high-gain and low-noise 79 GHz CMOS LNA using an adaptive biasing circuit for radar application. To achieve high gain, an LNA with a two-stage differential cascode (common source and common gate) topology is used. In the first stage, source degeneration inductors are used for both input and noise matching. Second stage of LNA consists of adaptive biasing circuit which automatically controls gain with respect to the received power. Adaptive biasing circuit is a three-stage common source amplifier to decrease output voltage as the input power increases. It provides a wide dynamic range and covers the entire detection range. The proposed design is analyzed in 180 nm CMOS technology using ADS tool. The designed LNA provides a voltage gain of more than 22 dB at 79 GHz with the input reflection coefficient (S11) of −5.7 dB, reverse isolation (S12) of −20 dB, forward transmission coefficient (S21) of −18 dB, and output reflection coefficient (S22) of −1.5 dB with the noise figure of less than 5 dB. The second stage of LNA with adaptive biasing circuit lowers the gain as the received power increases which typically gives an AC gain of 0.9 dB at 79 GHz.

Keywords Low-noise amplifier (LNA) · CMOS · Adaptive biasing (ADB) S-parameter noise figure · Linearity

1 Introduction

Short-range detection for automotive applications comes into effective usage by 79 GHz UWB radar receiver front ends. With an average effective isotropic radiated power (EIRP) of −3 dBm/MHz for unlicensed 77–81 GHz spectrum allocated by European Telecommunications Standard Institute (ETSI) makes it possible to achieve high signal-to-noise ratio at the receiver end [1]. Amplifying the received signals

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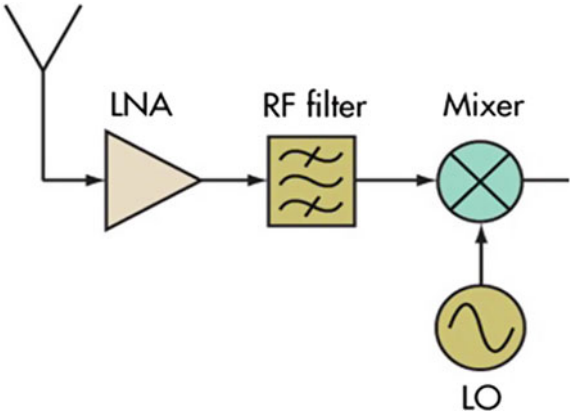

Fig. 1 Block diagram of receiver front end

without adding noise or rejecting interfering signals, optimizing the probability of detecting the signal by its bandwidth characteristics, and providing a large dynamic range to accommodate large clutter signals are design considerations of radar receiver front end [2]. Receiver front-end block diagram, as shown in Fig. 1, comprises low-noise amplifier, mixer and local oscillator that process the signal at the original incoming radio frequency, before it is converted to a lower intermediate frequency [3].

The low-noise amplifier (LNA) with low noise figure and high gain increases the sensitivity of the receiver by amplifying the weak signals without contaminating them with noise, helpful for succeeding stages. However, excessive high signal powers at 77–81 GHz will saturate the radar receiver used for short-range detection (usually 30 m) [4]. Hence, a receiver needs an adaptive biasing technique to operate the radar with a control over the gain as per the target distance with in 30 m.

This paper proposes a design of two-stage CMOS low-noise amplifier which operates at 79 GHz with adaptive biasing technique to improve performance of the radar receiver by achieving high gain and low noise figure for short-range detection. CMOS technology replaces the SiGe bipolar technology receivers in UWB range since a reasonable combination of device and bias current may provide acceptably low noise [5].

In Sect. 2, we describe the proposed low-noise amplifier with adaptive biasing technique specifying the advantages of differential cascode configuration. In Sect. 3, we describe adaptive biasing circuit and derive gain equations for the differential cascode stage. In Sect. 4, the simulation results are presented and respective discussions are made. In Sect. 5, conclusions are given.

2 Proposed Low-Noise Amplifier with Adaptive Biasing

Amongst the different LNA topologies, cascode configuration [3], shown in Fig. 2, is widely used in CMOS RF LNAs and can be considered as current-reuse configuration of a CS stage followed by a CG stage [3]. Cascode LNA ensures high

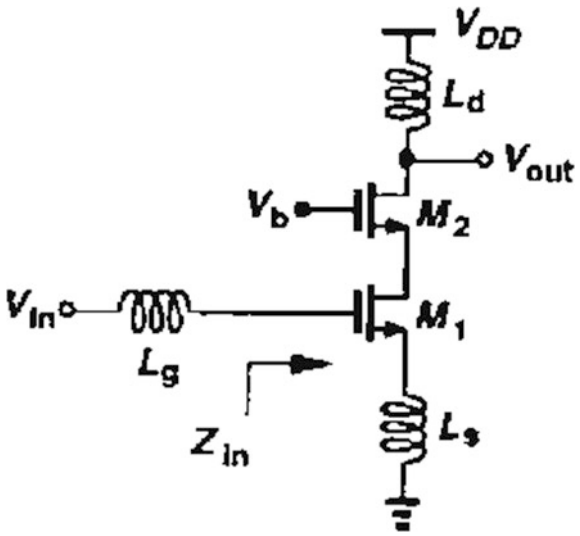

Fig. 2 Cascode configuration

power gain, good noise performance, low power consumption, and high reverse isolation [3]. However, this excellent noise and gain performance of cascode stage degrades in very high frequencies due to substrate parasitic admittance at the drain–source common node that increases as frequency increases [3]. Cascode stage is useful for wideband applications by just adding feedback techniques or any matching networks in the input. Differential cascode is preferable to obtain high gain by doubling of output voltage swing and is less susceptible to common mode disturbances [3].

The first stage of the proposed two-stage LNA is as shown in Fig. 3. It is source degeneration differential cascode configuration [6]. Minimum achievable noise figure of an LNA (NFmin) requires optimum noise matching while maximum power gain requires conjugate impedance matching. In CMOS technology, these two matching conditions are very close together, and noise and power matching becomes possible. To obtain maximum power gain matching, the input impedance of LNA must have a resistive term. Then matching network transforms this resistance to the real part of the source (generator) impedance.

3 Second Stage of LNA with Adaptive Biasing

To achieve a high gain, a two-stage differential cascode (common source and common gate) topology is proposed. Second stage of LNA, shown in Fig. 4, consists of adaptive biasing circuit (ADB), which automatically controls gain with respect to the received power [7]. Second stage is connected to first stage with the help of coupling capacitors.

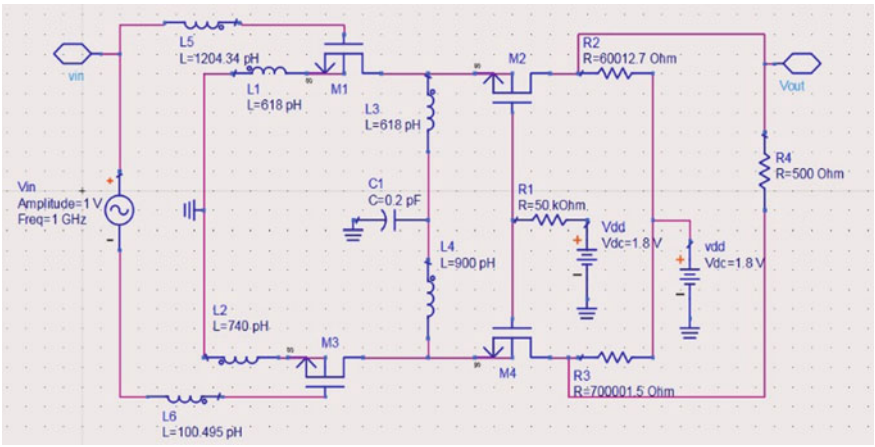

Fig. 3 First stage of LNA

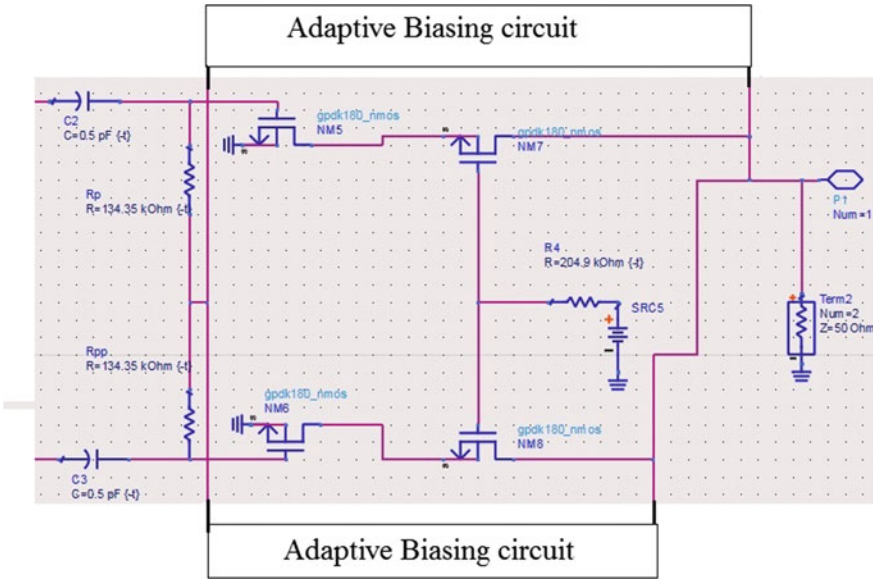

Fig. 4 Second stage of LNA

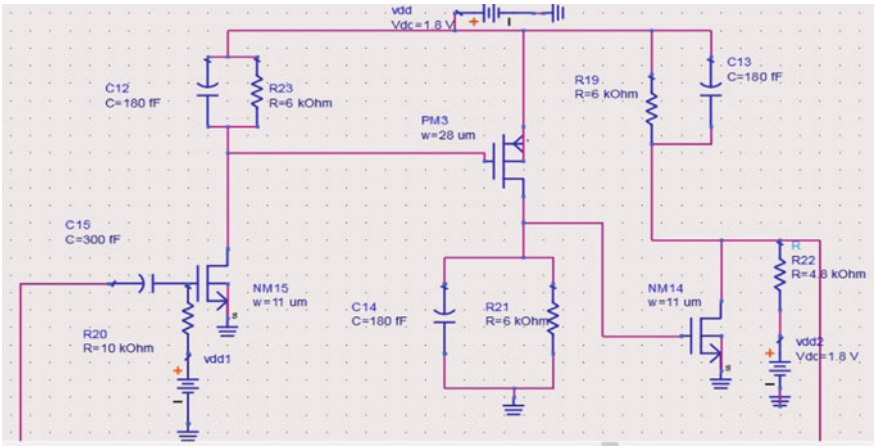

Fig. 5 Adaptive biasing circuit

As it's a differential topology, gain is doubled, shown by (1).

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = 2\left[\frac{g_{m1}r_0}{(1+g_{m1}X_{L1})r_0 + X_{L1}}\left(\frac{X_{L3}+\frac{X_{C1}}{2}-X_{L1}}{\left(X_{L3}+\frac{X_{C1}}{2}\right)(X_{L1})}\right)\right]\left[\frac{(1+g_{m2}r_0)R_2}{r_0+g_{m2}(R_S+2R_1)+R_S-R_2}\right] \tag{1}$$

where g_{m1} and g_{m2} are transconductances of MOSFETs $m1$ and $m2$. r_0 is the internal resistance of $m1$ and $m2$. R_s is source resistance. R_1 and R_2 are biasing resistors. X_{L1}, X_{L3}, and X_{C1} are reactances of input impedance matching network.

Adaptive biasing circuit is a three-stage common source amplifier as shown in Fig. 5, to decrease output voltage as the input power increases [7]. It provides a wide dynamic range and covers the entire detection range that is needed.

4 Simulations and Discussions

A. Transient Response:

The proposed design is analyzed in 180 nm CMOS technology using ADS tool. Firstly, the transient analysis is performed as shown in Fig. 6; for a Vin of 1 V, an output voltage of 1.32 V is obtained.

B. AC Gain:

The AC analysis is performed on the proposed LNA's first stage, differential cascade which provides a voltage gain of more than 22 dB at 79 GHz with gain equation as shown in Fig. 7.

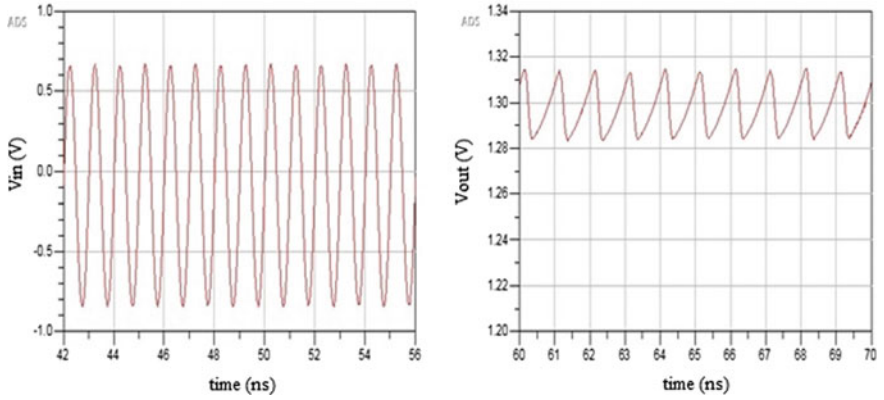

Fig. 6 Transient response

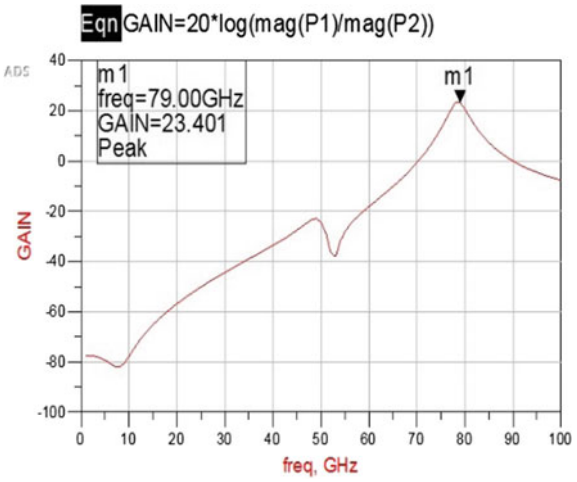

Fig. 7 AC analysis of first stage LNA

C. S-Parameters:

Input reflection coefficient (S11) defines the input matching of the LNA with source impedance of 50 Ω. The proposed LNA has S11 of −5.7 dB, as shown in Fig. 8, at the designed frequency of 79 GHz which shows it as good impedance matching. Output reflection coefficient S22 defines the output matching of LNA with output termination of 50 Ω. The proposed LNA has output reflection coefficient of −1.5 dB as shown in Fig. 9.

Reverse isolation of LNA is the measure of isolation of intermediate frequency components entering back into LNA through any feedback network. The proposed LNA has a reverse isolation of −20 dB as shown in Fig. 10. The forward

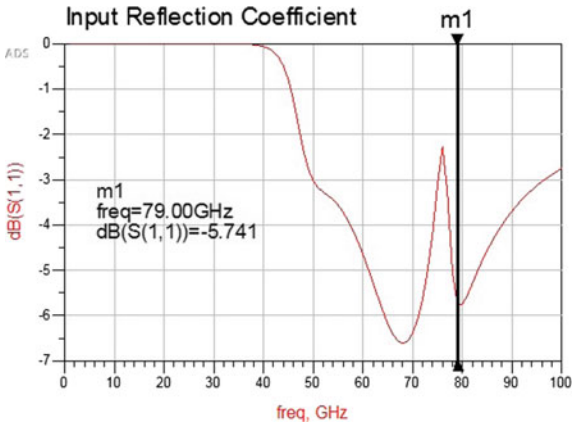

Fig. 8 Input reflection coefficient (S11)

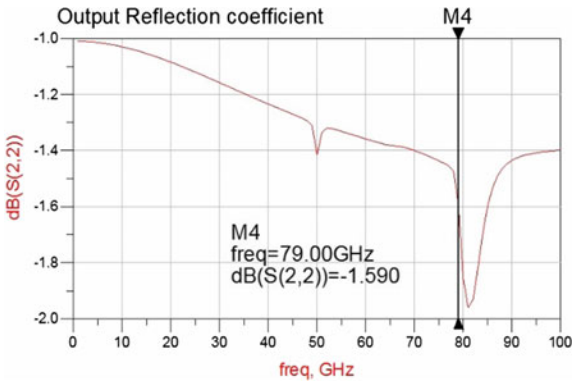

Fig. 9 Output reflection coefficient (S22)

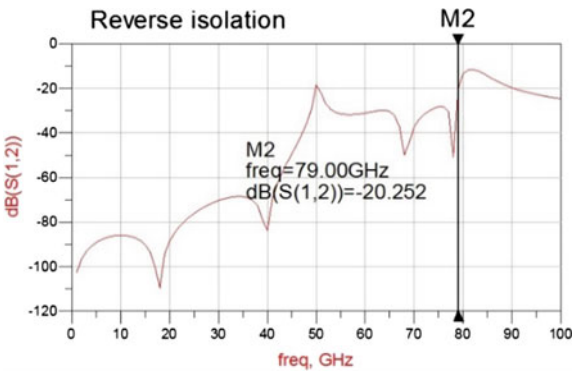

Fig. 10 Reverse isolation (S12)

transmission gain gives a measure of gain of LNA from input port to output. For the first stage, S21 is −6 dB while for second stage with ADB circuit S21 is −18 dB which specifies a considerable decrease in gain as shown in Fig. 11.

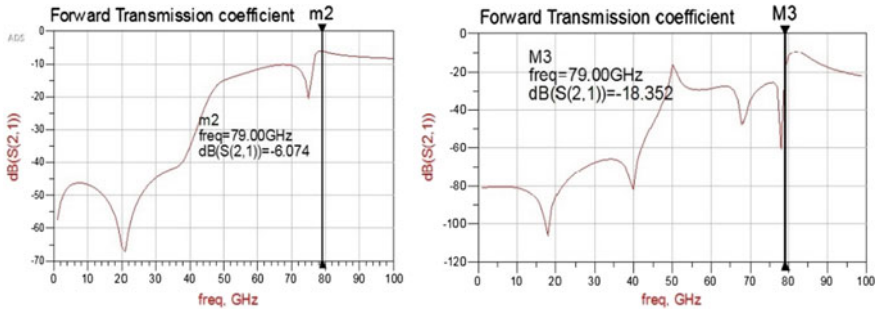

Fig. 11 Forward transmission gain of LNA

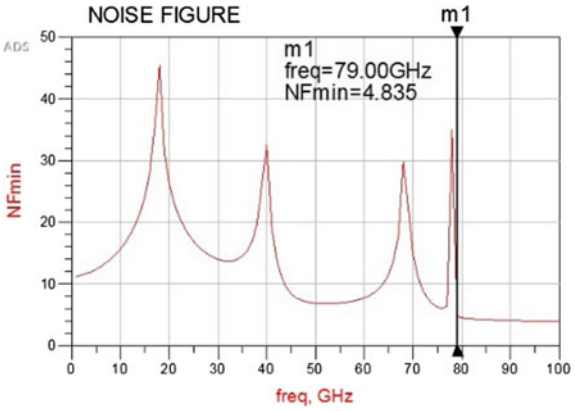

Fig. 12 Noise analysis of LNA with ADB circuit

D. Overall Noise Figure:

Noise figure (F) is the ratio of input signal-to-noise (SNR) to output signal-to-noise ratio (SNR) which gives performance measurement of an LNA, with lower values representing better performance. Hence, the overall noise figure of the proposed LNA is 4.3 dB as shown in Fig. 12.

E. Linearity:

Linearity is often affected by gain compressions and intermodulations. Gain compression (P1 dB) is the fall in the small signal gain at high input levels. Figure 13 shows the P1 dB of −21 dB of LNA which occurs at −7 dB of RF_PWR input power.

The third-order input intermodulation IIP3 is evaluated by extrapolating the curves of fundamental and third-order distortion product signal where they meet each other. The input intercept is IIP3, and output intercept is OIP3. Figure 14, shows the results of intermodulation of LNA, with IIP3 of 8 dB for OIP3 of −47 dB.

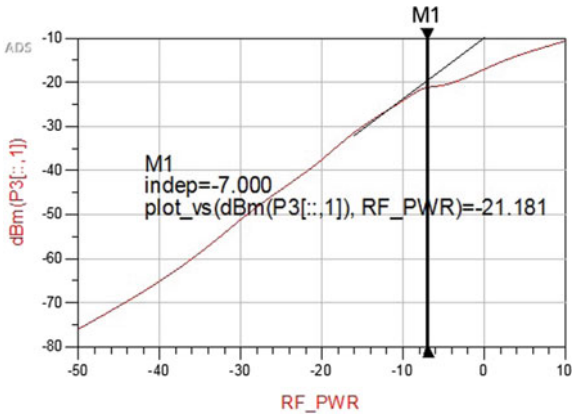

Fig. 13 P1 dB compression point of LNA

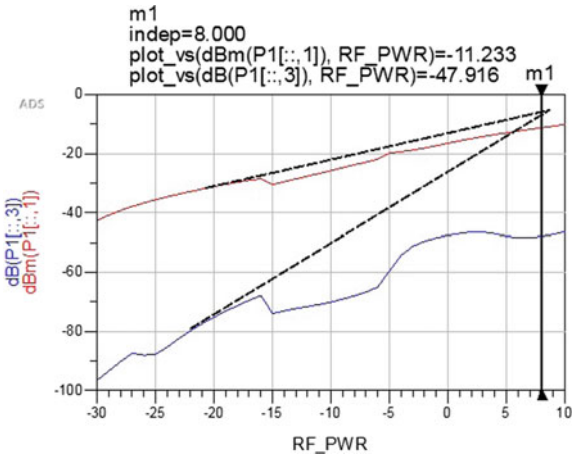

Fig. 14 IIP3 of LNA with ADB circuit

F. Gain Analysis:

The second stage of LNA with adaptive biasing circuit lowers the gain as the received power increases which typically gives an AC gain of 0.9 dB at 79 GHz as shown in Fig. 15. Overall gain decreases with increase in input power, (RF_PWR) shown in Fig. 16, which is maintaining the adaptive biasing technique.

G. Performance Comparison:

Table 1 gives a comparison of some proposed characteristics with published CMOS radar receivers in 77–80 GHz.

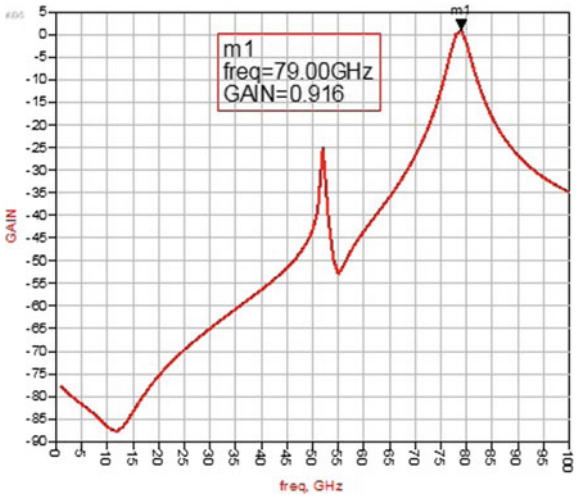

Fig. 15 AC gain of LNA with ADB circuit

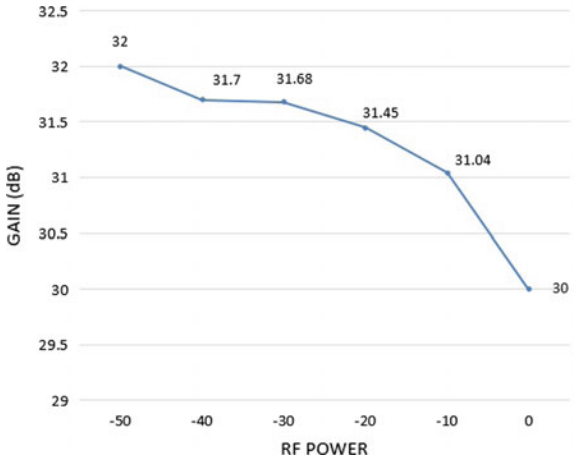

Fig. 16 Gain with respective input RF power

Table 1 Performance comparison of CMOS automotive radar receiver LNA

	Frequency (GHz)	Gain (dB)	ADB	Noise figure (dB)
[8] CMOS 65 nm	76–77	16	No	13
This work CMOS 180 nm	79	32 @ RF −50 dBm 30 @ RF 0 dBm	Yes	4.8

5 Conclusion

A CMOS LNA circuit which operates at 79 GHz was implemented using 180 nm CMOS technology. An ADB circuit was proposed to provide a wide dynamic range to a radar receiver without any additional control signals. The proposed design of LNA is implemented, and analysis over gain, reflection coefficients, and output power is performed. Our result demonstrated that the LNA with a gain of 22 dB in first stage is automatically controlled to 0.9 dB depending on input power at 79 GHz, thus, maintaining the adaptive nature of the LNA with respective to received power.

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X-band Phased-Array Transmitter in 180-nm SiGe BiCMOS Technology with Stacked Power Amplifier

Sijo Thomas and T. Saminathan

Abstract This paper briefs the design of *X*-band phased-array transmitter in SiGe BiCMOS technology using 180-nm SiGe HBTs. Power amplifier comprises a single-stage driver amplifier and a two-stage post-amplifier (PA) for better gain and output power. Driver amplifier is to boost the gain of the entire system, and it operates over a frequency range of 8–12 GHz (*X*-band). The transmitter demonstrates a gain >20 dB and a PAE greater than 15.5% over a frequency range of 7–12 GHz. Also, the PA delivers an output power of 1.34 W, with better linearity between input and output power.

Keywords Advanced design system (ADS) · Driver amplifier · Noise figure (NF) Power-added efficiency (PAE) · Stacked power amplifier

1 Introduction

Active phased arrays have been widely used in radar and wireless communication systems since they allow faster beam forming and nulling of the interferences from different directions and thereby improved signal-to-noise ratio (SNR). Traditionally, III–V technologies (InP or GaAs) are utilized to fabricate the active phased array due to their better performance on output power and noise figure (NF). However, to perform active electronic scanning, a phased-array system usually needs thousands of transmit/receive (T/R) modules, which are extremely costly. Compared with III–V technologies, silicon-based technologies can provide a higher integration level at much lower cost, although the power-handling ability, NF, and linearity cannot outperform their III–V counterparts. Therefore, it is popular to use

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III–V technologies to perform low-noise amplifying and high-power delivering and deploy low-cost silicon-based technologies to perform beam forming.

X-band phased array has been a hot research area for military radar technologies. Utilizing the system structure, the high power amplifiers (HPAs) usually need expensive III–V solutions to deliver high output power (5 W). However, with more manageable output powers, a SiGe technology, which can deliver 0.5–2 W of output power at *X*-band, is a more cost-effective solution. The previous design presents the design and fabrication of an *X*-band phased-array transceiver using SiGe BiCMOS technology. These designs achieve a decent gain, but it is having relatively higher RMS gain error to previous technologies. Also, power-added efficiency degrades due to increased power consumption. All these drawbacks are taken into consideration in the proposed design.

The critical components of the transmitter in the RF front ends are the power amplifier (PA), variable gain amplifier (VGA). The main challenge is the design of PAs which have to overcome low breakdown voltage problem with better impedance matching and large voltage swings. This paper *X*-band phase presents an array transmitter in 180-nm technology that provides a comparable gain with reduced RMS gain error and increased PAE. The increase in transistor size overcomes the lower breakdown voltage. In this paper, a stacked power amplifier is implemented with better output power and efficiency for achieving higher gain. The transmitter core chip is in 180-nm SiGe BiCMOS technology. It operates over a frequency range of 8–12 GHz with class AB amplifiers. Power amplifier circuitry comprises driving amplifier (DA) and post-amplifier (PA) with an interstage matching. Driver amplifier boosts the gain, and post-amplifier increases the output power (Fig. 1).

The transmitter design consists of power amplifier and variable gain amplifier (VGA). The relative larger RMS gain error simulations were carried out in ADS (Advanced Design System) with an input frequency range of 8–12 GHz improved by adding VGA. The overall reduced power consumption of the design improves PAE. The circuit simulations were carried out in ADS (Advanced Design System) with an input frequency range of 8–12 GHz.

This paper is organised as follows. In Sect. 2, transmitter design is highlighted. Section 3 discusses the structure of phase shifter. Section 4 shows the measurement results and comparison. Section 5 provides conclusion.

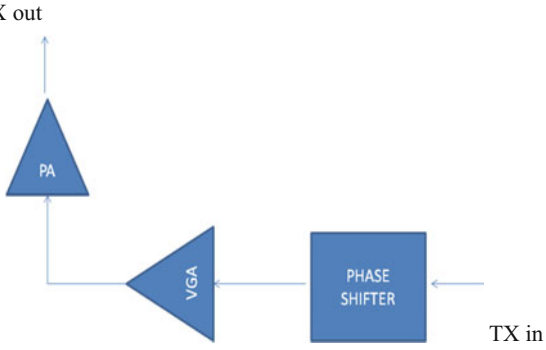


Fig. 1 Proposed design of *X*-band transmitter

2 Transmitter Design

The input reference frequency is in GHz range. A five-stacked PA to gain high output power with reduced stages of high power amplifier constitutes the major block in RF transmitter. These designs are having better anti-interference performance than the one using local oscillator. The proposed amplifier can be used in active phased-array transmitters. The design comprises a post-amplifier and a driver amplifier. The proposed design is as shown in Fig. 1. Here, power amplifier is biased in class AB in 180-nm SiGe BiCMOS technology.

2.1 Design of Stacked Power Amplifier

As the technology scales down, the design of PA is a challenging task due to the low breakdown voltage and the low output impedance. Limited by the maximum allowable voltage, many large devices have been typically connected in parallel to increase the current swing for a high output power. However, the paralleled devices have lower output impedance, which is required to be matched to 50 Ω. Thus, one possible strategy to maintain a better power performance is the transistor-stacking technique. By providing proper biasing conditions and matching networks, we can achieve uniform voltage drop across the transistors.

Stacked power amplifier consists of driver amplifier in order to boost the gain and a two-stage post-amplifier for better output power. Driver amplifier is a three stacked configuration which is cascaded with post-amplifier. Driver amplifier is shown in Fig. 4. Post-amplifier is a five stacked configuration, where two stacked ones are combined together with proper matching networks. Apart from cascade structure, the bases of the stacked configurations are not RF grounded. Ideally, the collector–emitter voltage swings are equal in phase and amplitude.

Figure 2 shows the detailed structure of post-amplifier, which plays a major role in delivering output power. Five sets of HBTs are stacked together to form post-amplifier to realize high-voltage swing. Interstage matching between transistors is done by adding inductors. Capacitors (c1, c2, c3, c4) are deployed as DC block capacitors. Also, capacitors are connected to the base of both amplifiers to make the bases of transistors experience RF swings. Transistors are biased in class AB with base-to-emitter voltage of 0.85 V and collector-to-emitter voltage of 1.5 V. Vcc of 7.5 V is supplied through an RF choke inductor, and proper biasing is done to each transistors. For better linearity, bases of bottom transistors are biased via RF choke inductors. Post-amplifiers are combined with Wilkinson power drivers. This power amplifier is matched with driver amplifier using LC impedance matching circuit, as shown in Fig. 3.

For *n*-stage *m* parallel transistors output power is given by the equation (Figs. 4 and 5).

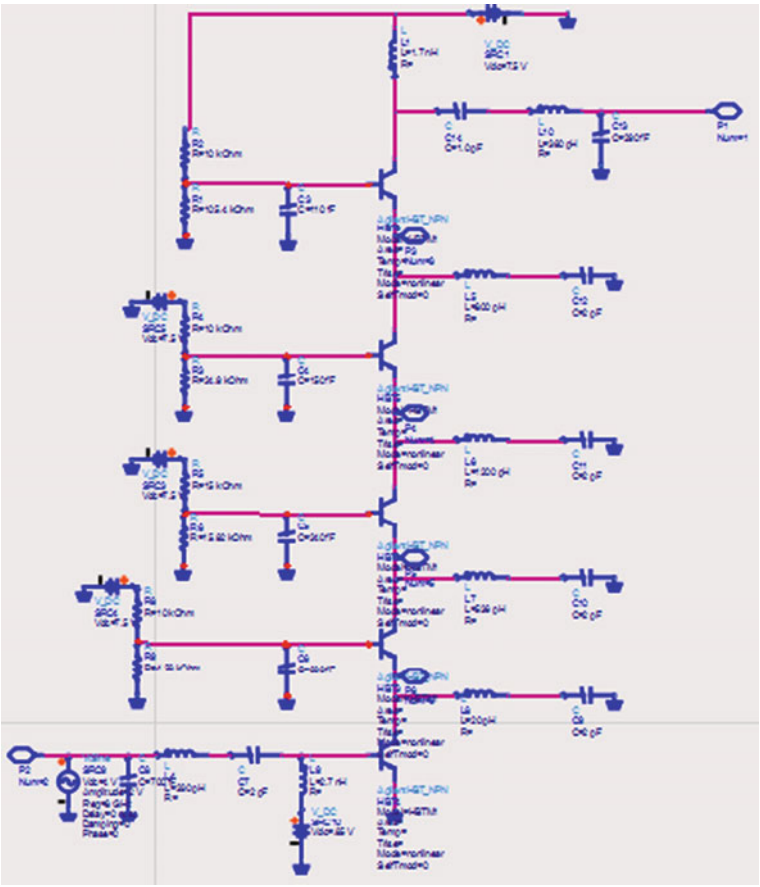


Fig. 2 Schematic of five stacked power amplifier

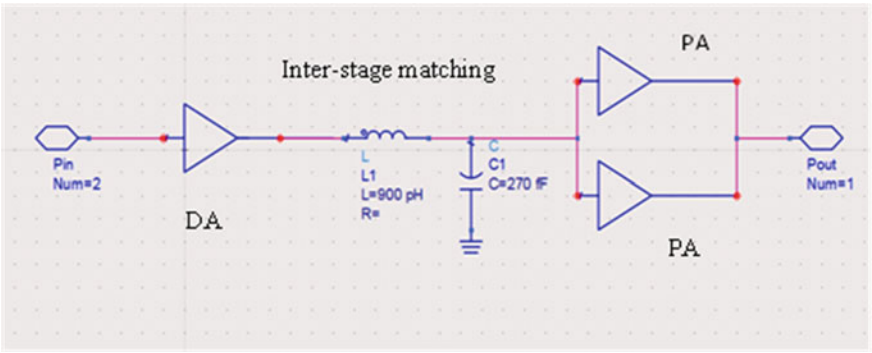


Fig. 3 Impedance matching between amplifiers

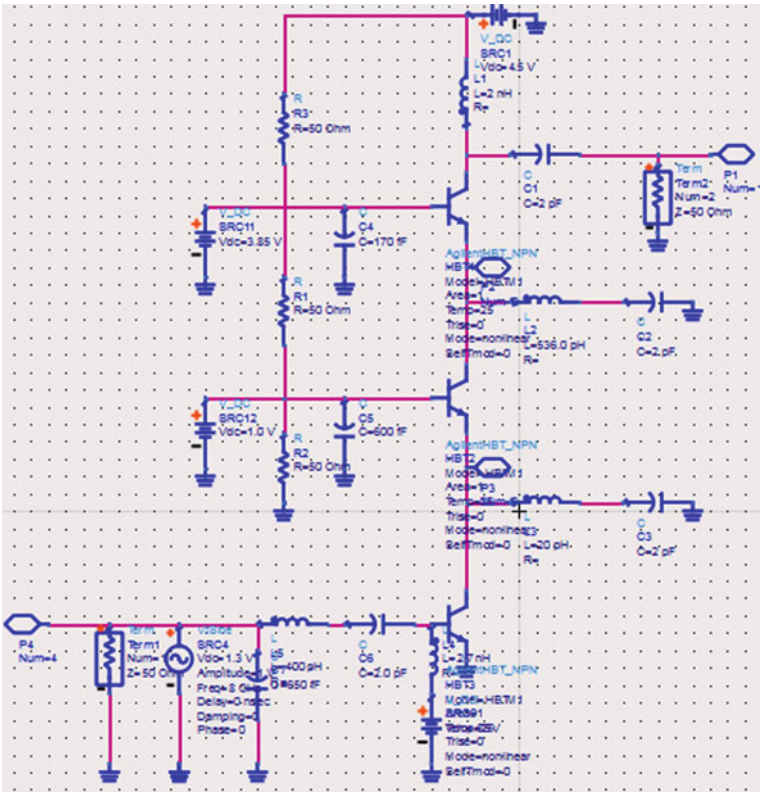


Fig. 4 Schematic of three stacked driver amplifier

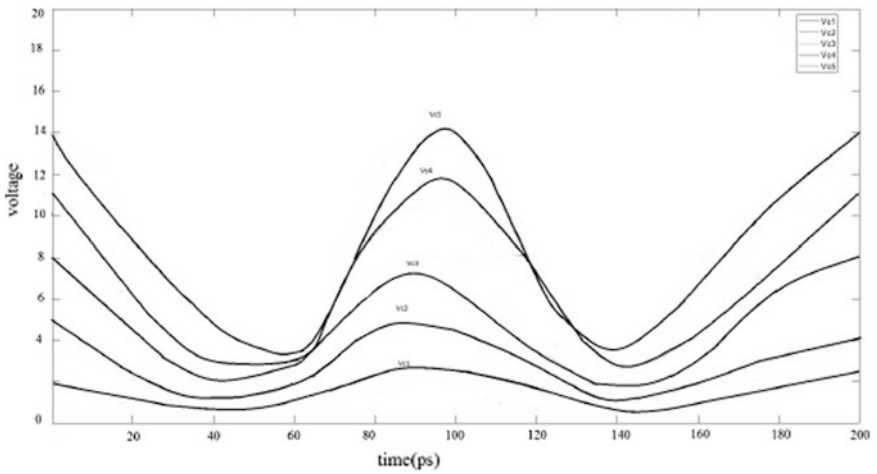


Fig. 5 Collector voltages of five stacked post-amplifier

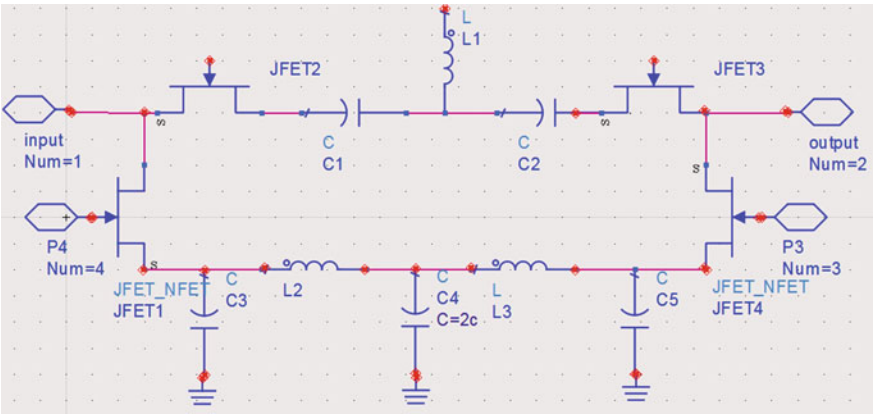


Fig. 6 Phase shifter for 90°, 180°

$$\text{output power} = \frac{V_{\text{ce,max}} \times I_{\text{ce,max}}}{2} \tag{1}$$

3 Phase Shifter

Phase shifters are used in RX as well as TX paths. They should have better linearity. Passive phase shifters may have better linearity and require greater attention in design to obtain wideband phase shift, as well as improved sensitivity to process temperature and voltage fluctuations. Here, we implement 5-bit phase shifter using MOS transistors and high-pass, low-pass filters by LC passive elements. Here, phase shift occurs at 11.25°, 22.5°, 45°, 90°, 180°. For 11.25°, 22.5°, 45°, 90°, 180°, various topologies are used which is shown in Figs. 6, 7, 8, and 9.

4 Simulation Results

The proposed transmitter is of 180-nm SiGe BiCMOS technology, and simulations are carried out in ADS. Simulated s parameter is shown in figure from 9–12 GHz. Simulated input power versus power-added efficiency is shown in Fig. 10. Here, we obtain a power-added efficiency of 16.8%. Also, a plot of measured saturated power amplifier is shown in Fig. 8 which is equal to 29.2 dBm. Here, we obtain a maximum collector voltage of 14.2 V and collector current of 0.38 A, which is shown in Fig. 5. The post-amplifier exhibits a maximum output power greater than 0.68 W, and in total, post-amplifier delivers an output power greater than 1.25 W (Fig. 9; Table 1).

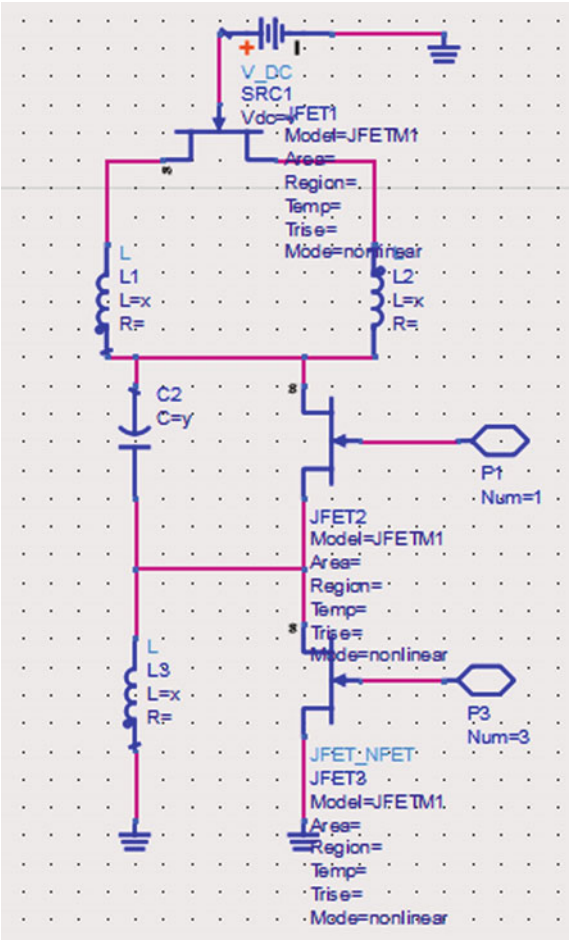


Fig. 7 Phase shifter for 25°, 22.5°, 45°

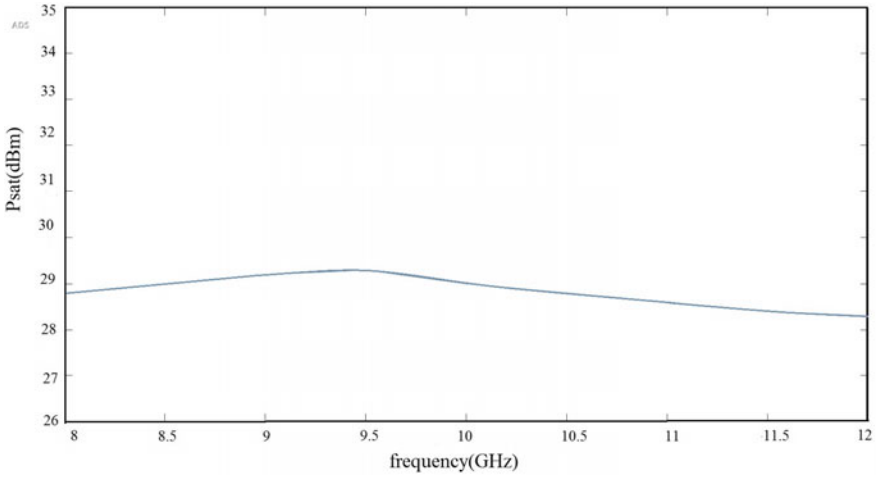
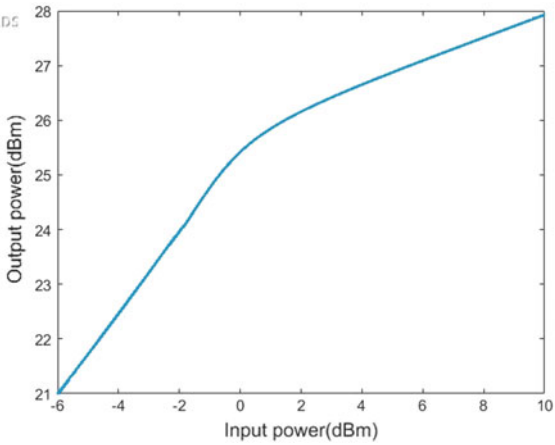


Fig. 8 Input power versus simulated Psat (dBm) of PA

Fig. 9 Input power versus output power (dBm) of PA



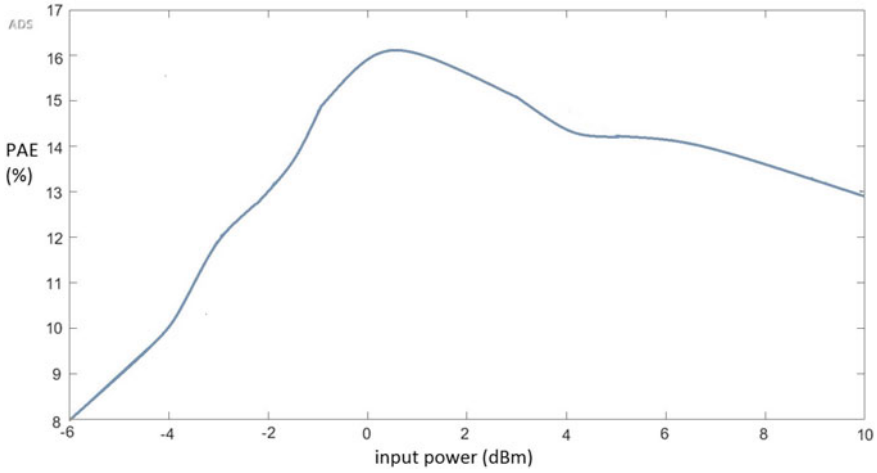


Fig. 10 PAE of power amplifier

Table 1 A comparison of *X*-band transmitters

Technology	0.25-µm SiGe BiCMOS [1]	0.18-µm SiGe BiCMOS [2]	0.18-µm SiGe CMOS [3]	0.18-µm SiGe BiCMOS (this work)
Frequency (GHz)	8–11	6–18	8.5–10	8–12
Power-added efficiency (PAE)	22%	12%	15.8%	16.2%
Function	RX/TX	RX/TX	RX/TX	TX
TX gain	17	27	11	22
TX output *p*-1 (dBm)	18	NA	11.5	27.9

5 Conclusion

An *X*-band transmitter is designed in 180-nm SiGe BiCMOS technology. Transmitter integrates a phase shifter, VGA, and power amplifier. Transmitter exhibits a maximum gain of 22 dB, output power of 27.9 dB, and an efficiency of 12.4%. Also, VGA is added to the design for better PAE.

Acknowledgements Without the help and support of many individuals, this work would not have come to fruition. The author would like to acknowledge Dr. J. Manjula, Dr. J. Selvakumar, N. Saraswathi, and all the faculties of SRM University, Kattankulathur, Tamil Nadu, India, for their technical support during this work. The author would like to acknowledge Agilent Technologies for ADS tool.

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Short-Range Low Data Rate Pulsed UWB Transmitter

G. Sarathy and S. Praveen Kumar

Abstract This paper presents a pulsed ultra-wideband (UWB) transmitter with high power and efficiency. It consists of a simple switched capacitor-based relaxation oscillator for sub-carrier generation which gives distortion less carrier signal with a phase noise of 106 dBc/Hz at 1 MHz frequency. Phase-locked loop circuit with ON-OFF keying (OOK) modulator to generate FM signal within the range of UWB, i.e., 3.1–10.6 GHz. And class A power amplifier is employed for signal amplification. Proposed pulsed UWB transmitter is implemented in 45-nm CMOS process technology with a power supply of 0.9 V. Experimental results prove that the presented pulsed UWB transmitter has a transmitting range of 6–8.1 GHz with a power consumption of 3.9 mW (Laha et al. 60 GHz OOK transmitter in 32-nm DG FinFET technology, [1]).

Keywords Ultra wide band (UWB) · Wireless body area network (WBAN) Wireless personal area network (WPAN) · Voltage controlled oscillator (VCO) ON-OFF keying (OOK) · Phase locked loop (PLL)

1 Introduction

The communication UWB performs signals in the bandwidth of 500 MHz, with the operating frequency range of 3.1–10.6 GHz. UWB communication systems play a major role in delivering short-range wireless networks such as wireless body area network (WBAN) and wireless personal area network (WPAN). The pulsed UWB transmitted at the range of 6–8.1 GHz is implemented with the help of simple switched capacitor-based relaxation oscillator, voltage-controlled oscillator (VCO) and the output amplifier [2].

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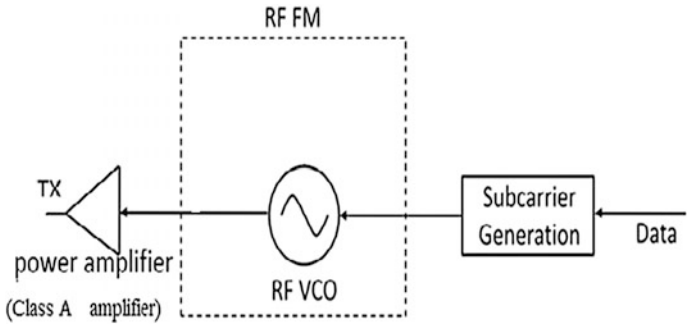

Fig. 1 Short-range low data rate pulsed UWB transmitter

UWB helps to separate the technology from narrow band and wide band. The bandwidth of UWB is defined by Federal Communication Commission (FCC) which is more than 1.5 GHz. UWB can produce impulses that are with sharp fall and rise time. There are two techniques in UWB, they are impulse radio UWB (IR-UWB) and frequency-modulated UWB (FM-UWB) (Fig. 1).

2 Sub-carrier Generation Using SC-Based Relaxation Oscillator

Generally, carrier signals are used in modulation techniques to secure the transmission data from all sources of threats. Preferred type of oscillator for pulse wave generation is relaxation oscillator comprising of charge-discharge current and a timing capacitor [3]. Figure 2 shows the schematic of simple switched capacitor (SC)-based relaxation oscillator. Switched capacitor-based fully differential relaxation oscillator with a charging-discharging timing circuit is presented. Voltage between the capacitors C_1 and C_2 remain unchanged during $-V_{ss}$. As the input X goes high the charge of the capacitor C_1 transfers to C, whereas the voltage remains same. At which point the output equals to $-C_2\ V_{ss}$. The operation keeps running until V_x reaches 0 V.

The simplified FS-embedded relaxation oscillator architecture consists of op-amp, switched capacitor, delay cell, non-overlapping clock, inverter, nand circuits. The input of the op-amp is in-n and in-p, the output is out. The comparator inputs are in-n.in-p, clk and the output is out. The two-phase non-overlapping clock consists of input clk in and the outputs clk 1 and clk 2. The supply voltage is given with V_{dc} = 1.8 V. The principles of relaxation oscillator are with V_{out} low to $-V_{ss}$ and V_x are higher than zero. The Voltage across the Un-Switched capacitor remains unchanged At $-V_{ss}$, the output will fall by an amount of

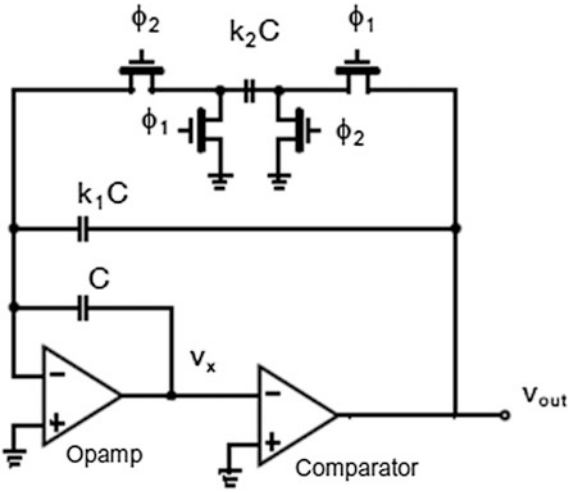

Fig. 2 Proposed sub-carried relaxation oscillator

$$\Delta v_x = \frac{\Delta Q_c}{C} = \frac{Q_{k_2 c}}{C} = -k_2 V_{SS}$$

3 Proposed Transmitter with OOK Modulation

3.1 Phase-Locked Loop

The key function of phase-locked loop (PLL) is to provide synchronization clock and to maintain the integrity of time. Hence nowadays, PLL is an essential building block a major communication system. The comparison operation is performed by a phase detector. In this paper, the necessity of locking the transmitter signal on to the range of ultra-wideband (UWB) that is 3.12–10.6 GHz is achieved by using PLL. The output of the PLL block is a transmitting signal with a tuning range of 6–8.5 GHz, and the schematic of PLL is shown in Fig. 3 (Figs. 4 and 5).

3.2 OOK Modulation

The basic concept of a simple ON-OFF keying modulation is to transmit the data only during the positive transition while no data during the negative transition. The advantage of the above is power consumption that is greatly reduced as it is to operate only during the positive cycle. Also, the noise distortion scope is very less, almost negligible when compared to other conventional modulation techniques. In this paper [4], a 60 GHz, 2 Gbps OOK modulator is designed in 45-nm CMOS process technology with high ON/OFF isolation. The proposed OOK modulator is

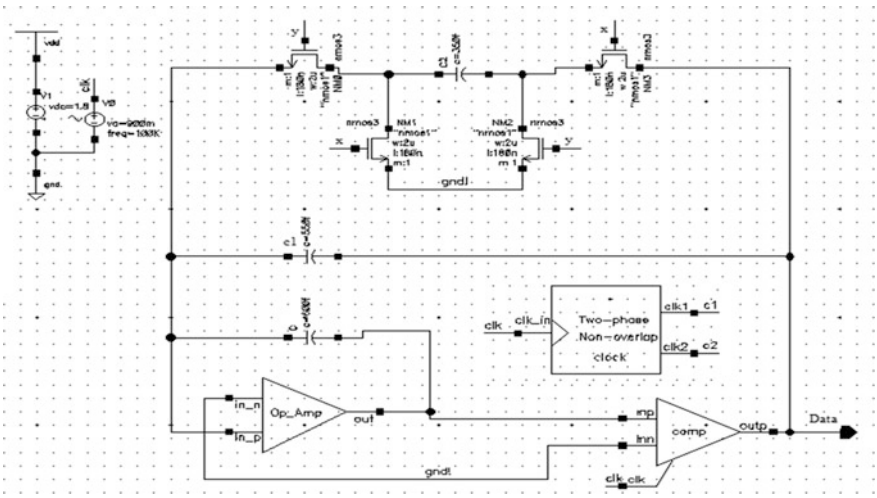

Fig. 3 Schematic of proposed sub-carried relaxation oscillator

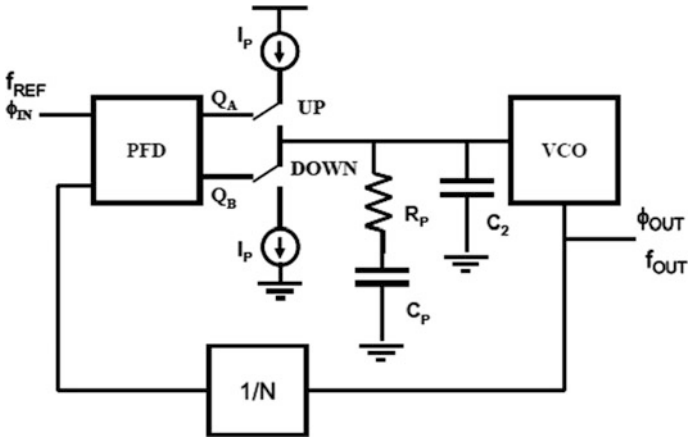

Fig. 4 Third-order phase-locked loop (PLL)

well suited for less power, short-range UWB applications [5]. From the simulated schematic, the pulsed UWB of 2.5 Gbps of data rate is transmitted (Figs. 6 and 7).

3.3 Output Amplifier

The common source (CS) configuration requires less power supply and biasing voltage compared with Darlington, cascode configuration which makes it an ideal

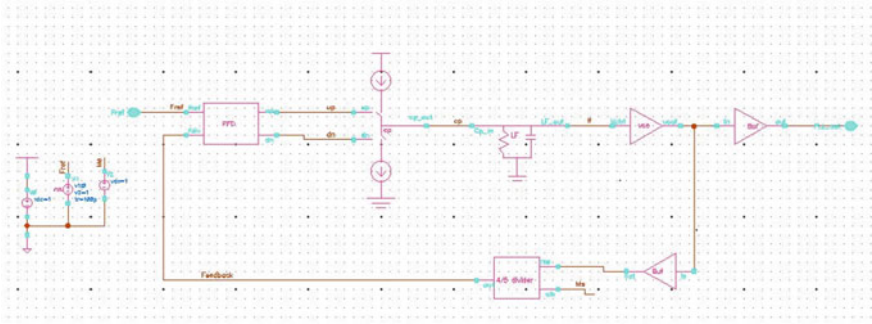

Fig. 5 Schematic of third-order phase-locked loop (PLL)

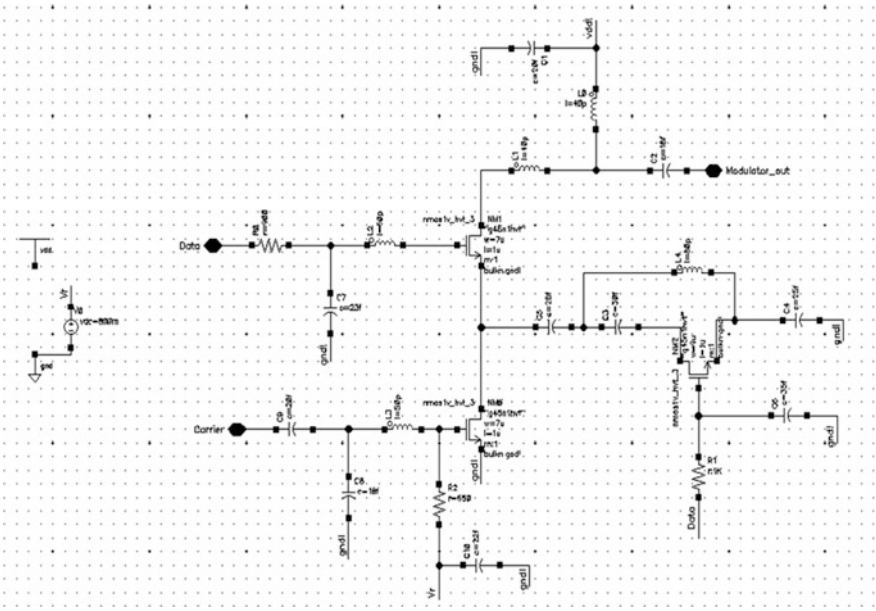

Fig. 6 Schematic of OOK modulation

option for the wireless applications employing low power, short distance. The transistor in the common source configuration operates independent eliminating the higher order distortion. In effect, the linear of the power amplifier is greatly increased. The linearity of the PA is also observed to be competitive for low power CS configurations. The output amplifier used here is class A power amplifier [1] The 1 dB compression point (P1*dB*) and the third-order input intercept point (IIP3) are found to be 5.7 and 18.7 dBm, respectively. The 13 dB difference between P1*dB* and IIP3 can be attributed to the scaling down of DG MOSFET to 32 nm [1]. The power-added efficiency (PAE) and the fractional bandwidth (FB) of this amplifier are $\sim$14 and 50%, respectively (Figs. 8 and 9).

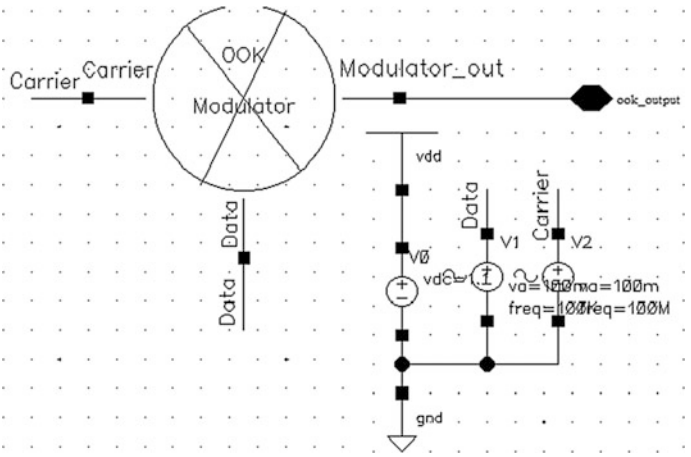

Fig. 7 Test bench of OOK modulation

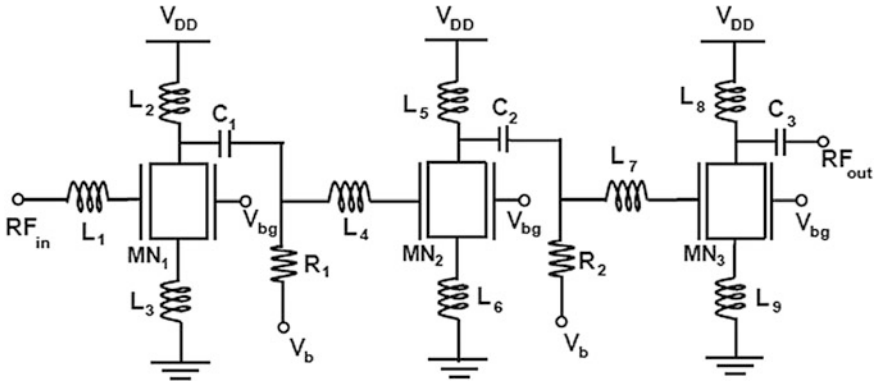

Fig. 8 Class A power amplifier

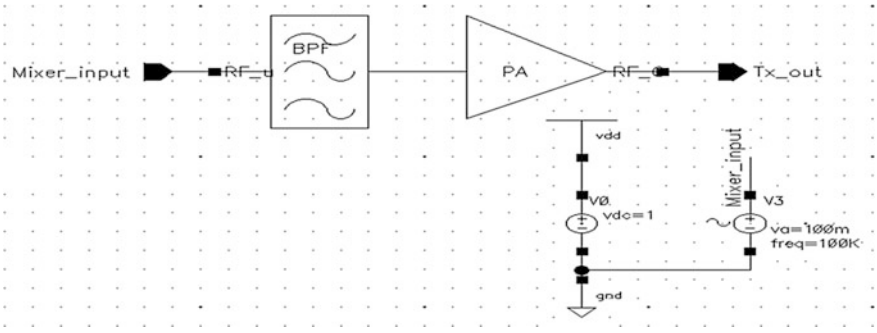

Fig. 9 Test bench of class A power amplifier with band pass filter (BPF)

4 Simulation Results

Cadence virtuoso tool was used to simulate the simulation results, and power and phase noise operation were studied under 45-nm CMOS process technology of Pulsed UWB transmitter. Output schematic of pulsed UWB transmitter shown in Fig. 10.

4.1 OOK

A 60 GHz of 2.5 Gbps OOK modulator is designed in a 0.18 m BiCMOS process (Fig. 11).

4.2 Phase Noise

It is observed in the waveform the phase noise is −105.5 dbc/Hz (Fig. 12).

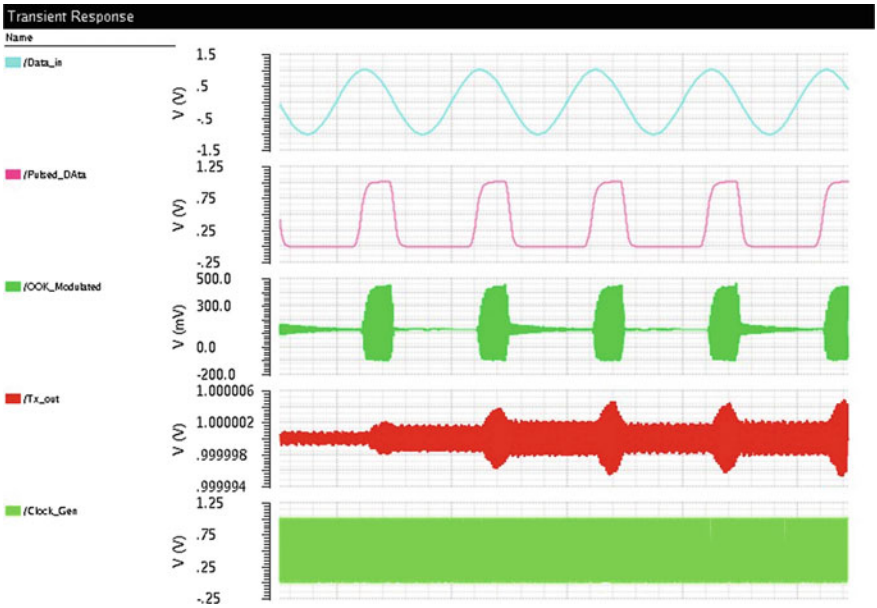

Fig. 10 Output schematic of pulsed UWB transmitter

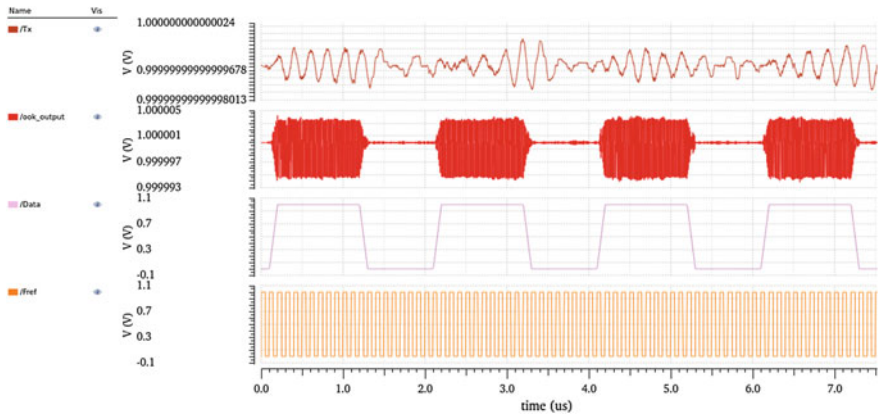

Fig. 11 Output of OOK modulator

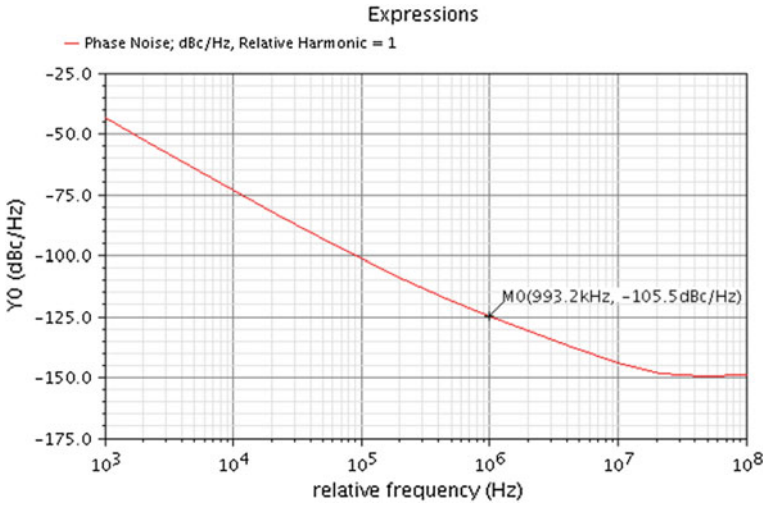

Fig. 12 Output of phase noise

4.3 Power Amplifier Power Output

The class A output amplifier is amplified and the power of 3.33 mW is obtained. The 3-dB bandwidth considered for all the cases of *Vbg* is 40 GHz (Fig. 13).

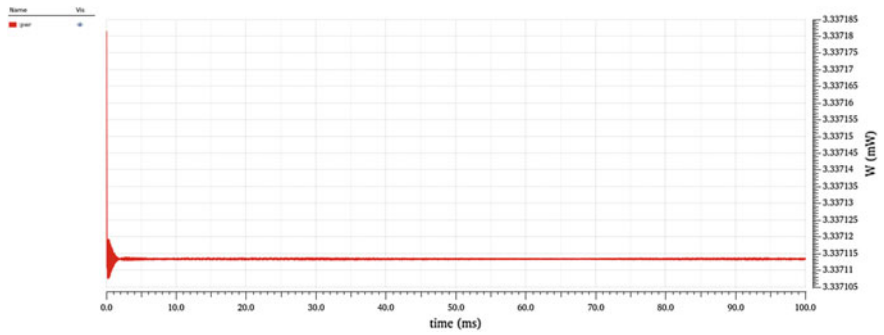

Fig. 13 Power output of class A amplifier

Table 1 Comparison of UWB transmitter

Technology	130 nm	90 nm	This work (45 nm)
VDD (V)	1.2	1	0.9
RF tuning range (GHz)	3.5–4.5	2.9–5.2	6–8.25
Sub-carrier frequency (Mhz)	1	0.8	1
Phase noise (dBc/Hz)	−107	−75	−105
Power consumption (mW)	4.6	0.8–1.1	3.9

5 Measurements Results

See Table 1.

6 Conclusion

Frequency-modulated ultra-wideband transmitter is widely used in data transmitting such as wireless personal area networks. A simplified sub-carrier generation structure has been proposed and compared with the existing architecture resulting ease of operation. The proposed architecture requires less power when compared with existing architecture for improved results modification in op-amps, biasing circuits and current-mode bandgap reference circuit should be considered as future work.

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A New High-Speed Multiplier Based on Carry-Look-Ahead Adder and Compressor

B. Jeevan and K. Sivani

Abstract This paper presents a new high-speed approximate multiplier using compressor and carry-look-ahead (CLA) adder to increase the speed of the computations. The number of full adders is reduced by introducing compressors. The CLA adder will reduce the waiting time by generating all carry at single instant. Initially, a 4 × 4 multiplier is designed using 4-2 compressor, 5-3 compressor, 5-bit CLA adder, a full adder, and a half adder. Later, the precision of multiplier is increased and designed up to 32 × 32 multiplier. All the designs are extensively simulated and synthesized in the Xilinx ISE 13.1 and targeted to Spartan-6 FPGA (XC6SLX45-CSG324C). The results of proposed approximate multipliers are better compared with exact multipliers in terms of delay. The proposed 32-bit approximate multiplier has a delay of 20.67 ns, which is approximately 5% less than exact multiplier.

Keywords Approximate computing · 4-2 compressor · Vedic multiplier Xilinx · FPGA

1 Introduction

High-speed digital circuits rely on the performance of multipliers operating with high degree of speed. However, signal processing, image and multimedia applications can tolerate imprecision and produce useful results. Approximate computing patterns are particularly interesting in these applications. Approximate models are used in the place of exact models with increase in the speed. The previous work proposed [1–6] is good but still can be improved by replacing with high-speed adder circuits to achieve high speed.

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In most of the applications, multipliers are the crucial and noticeable components dominating the overall performance of the digital circuits. The process of multiplication often consists of intermediate steps: getting partial product, summing up the partial products, and carry propagate addition to produce the final product result. Many useful techniques for multiplication are introduced in the literature to achieve faster multiplication like truncated multiplication method: making least significant bit columns of partial products as constant with an error rate, a truncated multiplier with correction constant calculating $(n + k)$ most significant columns and truncating $(n - k)$ least significant columns, and then result is rounded to n bits accumulating reduction error and rounding error, a truncated multiplier with variable correction constant [7, 8]. In recent trends, high speed is achieved by column compression multipliers. Wallace introduced the first column compression multiplier [9] using half adders (2-2) and full adders (3-2); Dadda altered the approach of Wallace by placing the half adders and full adders in the critical path.

Of the three modules of the multiplication process, second and third modules accumulate the most delay to the overall delay of the multiplier. To reduce the delay, column compression techniques [1–6] are widely used [3]. The delay of the second module is reduced using (4-2) compressors which are widely used. This paper presents a new approximate (4-2) compressors to reduce the delay of the second module used in the Vedic multiplier to achieve high performance. The delay of the third module is reduced by replacing the carry propagate adder with the CLA adder with slight increase in area [10]. The proposed approximate multiplier in the paper reduces the delay and area using carry-look-ahead concept and compressors in the intermediate steps of multiplication.

2 Proposed Multiplier

In this paper, the authors present a modification to existing multiplier architecture. Conventional multipliers consist of full adders (FAs) in first stage and ripple-carry adder (RCA) in the second stage. In the proposed method, a leaf cell i.e. 4×4 Vedic Multiplier is designed using 4:2 compressors in the first stage and carry-look-ahead adder (CLA) in the second stage. The drawback of RCA is taking more time to generate the final carry, which can be overcome by using CLA. Therefore, proposed architecture achieves high speed due to three reasons: Vedic multiplication (fast process as per literature), compressors (reduce the number of outputs), and CLA (all carries are generated simultaneously). An approximate compressor is designed in such a way that it has small error difference. The design is extended to 8×8, 16×16, and 32×32 bit multiplier using approximate compressor.

An exact multiplier consists of AND gates which generates intermediate products, ripple-carry addition tree with full adders, half adders, and compressors (5 inputs-3 outputs) [1–6] to add the intermediate products and a ripple-carry adder (RCA) to generate the end value.

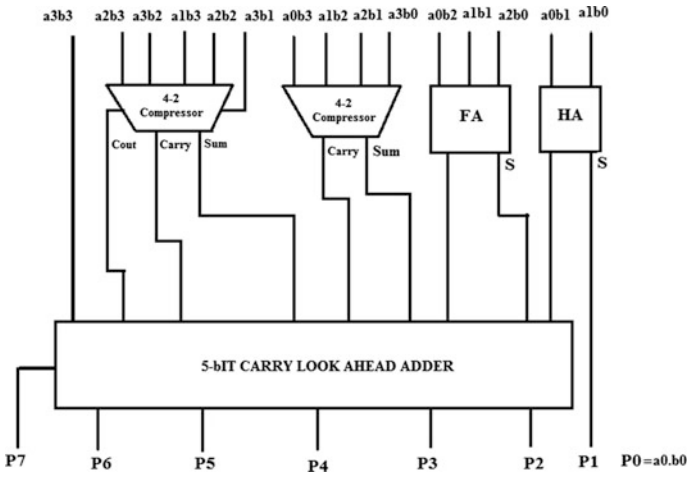

Fig. 1 Proposed 4 × 4 bit multiplier

RCA tree accumulates a larger delay of the total multiplication delay. Compressors are used in RCA tree to reduce the waiting time in the multiplication process. The concept of approximate compression is used in the multipliers, specifically in the carry-save adder tree in the place of exact compressors to decrease in delay and area.

Carry propagate adder is the second highest component accumulating larger delay to over all multiplier. To improve the speed of the multiplier, the carry propagate adder is replaced with the carry-look-ahead adder with decrease in the delay of the multiplier and slight increase in the area. Using the approximate (4-2) compressor in the second module and carry-look-ahead adder in the third module enhances the overall performance of the multiplier.

The proposed architecture is designed and analyzed for a Vedic multiplier. The techniques used in designing multipliers used in [1, 11] are good but still the speed is enhanced in proposed multiplier by replacing: RCA tree with compressors in second stage, complete RCA with CLA adder block in third stage. The proposed 4 × 4 multiplier using the approximate compressors and carry-look-ahead (CLA) adder is shown in Fig. 1.

3 Exact Compressor

Compressors can minimize multiple operand carry propagate addition and multiplication from "*n*" to 2 operands. 4-2 compressors is the most widely used structure for reducing 4 inputs to 2 outputs. The 4-2 compressor outlook is shown in Fig. 2. In the similar manner, 5-3 compressor can also be designed with less imprecision.

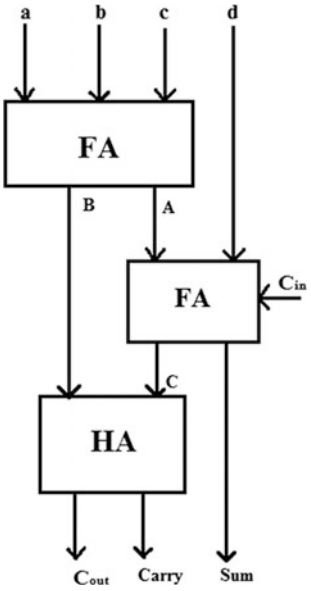

Fig. 2 Exact 4-2 compressor

An exact 4-2 compressor [2–4] has five inputs including an input carry bit from the lower significant component and three output bits including the output carry. The four inputs a, b, c, d, C_{in} and sum has the same weight. Based on the truth table shown in Table 1, the output expressions (S, Carry, and Co) of exact 4-2 compressor are extracted. The equations corresponding to this exact 4-2 compressors are as shown below.

$$\text{Sum} = a \wedge b \wedge c \wedge d \wedge C_{\text{in}} \tag{1}$$

$$B = ((a \wedge b)\&c) \big| (a\&b) \tag{2}$$

$$C = ((a \wedge b \wedge c \wedge d)\ \&\ C_{\text{in}}) \big| (a \wedge b \wedge c) \tag{3}$$

$$C_{\text{out}} = B\&C \tag{4}$$

$$\text{Carry} = B \wedge C \tag{5}$$

4 Approximate Compressors

An approximate 4-2 compressor is developed with increase in performance, decrease in number of outputs compared to the exact compressor design with a little error rate. However, the error rate is high if all the inputs of compressor are logic-1.

Table 1 Truth table of exact compressor

Input					Output		
C_{in}	a	b	c	d	C_{out}	Carry	Sum
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	0	1
0	0	0	1	1	0	1	0
0	0	1	0	0	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	0	0	1	0
0	0	1	1	1	0	1	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	0	1	1	0	1	1
0	1	1	0	0	0	1	0
0	1	1	0	1	0	1	1
0	1	1	1	0	0	1	1
0	I	1	1	1	1	0	0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	0
1	0	0	1	1	0	1	1
1	0	1	0	0	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	0	0	1	1
1	0	1	1	1	1	0	0
1	1	0	0	0	0	1	0
1	1	0	0	1	0	1	1
1	1	0	1	0	0	1	1
1	1	0	1	1	1	0	0
1	1	1	0	0	0	1	1
1	l	1	0	1	1	0	0
1	l	1	1	0	1	0	0
1	l	1	1	1	1	0	1

An approximate compressor is designed in such a way that has less error rate by eliminating output carry. Based on the observation table of exact compressor as shown in Table 1, it can be observed that C_{out} and C_{in} are same for 20 input combinations out of 32 combinations. Therefore C_{out} is approximated as C_{in} for the remaining 12 combinations so that C_{in} is directly connected to C_{out} while designing which can reduce hardware complexity. After excluding C_{in} at input side and C_{out} at output side, the number of inputs becomes 4 and the number of outputs will be 2.

By this approximation, the table consisting of 32 combinations is reduced to 16 combinations.

The error generated by considering C_{out} as C_{in} for the single combination is maximum of four, i.e., "100," and mainly for the input combination "1111." Thereafter, 4-2 compressor is modified to reduce the error rate for the specific combination, i.e., "1111." The error difference is compensated by changing the values of the carry and sum bit to one of that input combination. Changing the expected values of carry and sum bit minimizes the difference between exact outputs and the approximated outputs and also leads to ease of design. The changing of carry bit particularly reduces the delay and area. After approximating the carry and sum to one, the error difference has decreased to one which can be considered.

The block diagram representation of the new approximate compressor design is as shown in Fig. 3. The design equations corresponding to the approximate compressor is as shown below.

$$\text{Sum} = (a \wedge b \wedge c \wedge d) + (a\&b\&c\&d) \tag{6}$$

$$\text{Carry} = ((a|b)\ \&\ (c|d))|(a\&b) + (c\&d) \tag{7}$$

By making the simplifications in the approximate compressor, the speed is increased and area is decreased which can be proved by comparing the Eqs. (1)–(5) of exact compressor and Eqs. (6), (7) of approximate compressor. Based on expressions, the gate level implementation of the approximate compressor is designed as shown in Fig. 4.

The error can be exempted in certain applications such as multimedia and image processing by enhancing the processing speed and decrease in the area and can still produce useful results.

In the third stage of proposed multiplier, carry propagate adder is replaced by the CLA adder, and a 1-bit CLA adder is shown in Fig. 5.

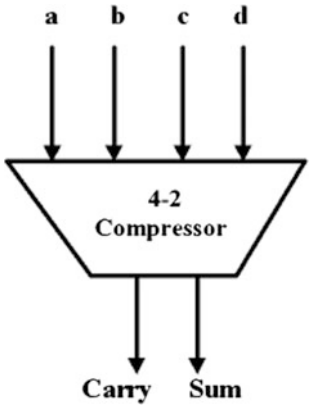

Fig. 3 Approximate 4-2 compressor

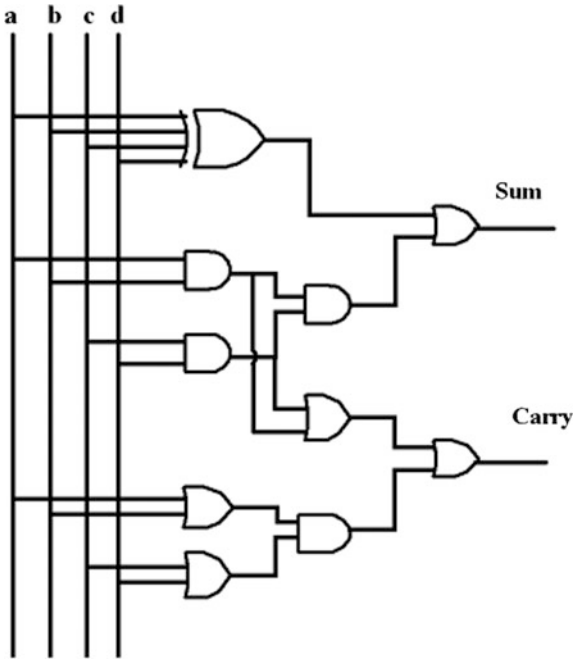

Fig. 4 Gate-level implementation of approximate 4-2 compressor

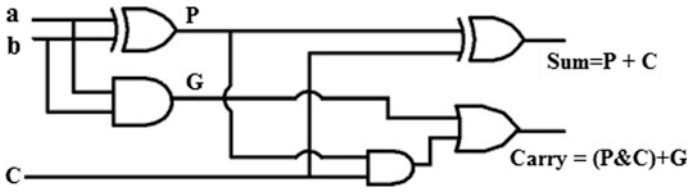

Fig. 5 Carry-look-ahead adder

The equations corresponding to the 1-bit CLA adder are as given below.

$$m = a \oplus b \tag{8}$$

$$n = a \cdot b \tag{9}$$

$$\text{Sum} = m \oplus c \tag{10}$$

$$\text{Carry} = m \cdot c + n \tag{11}$$

The equations for final product bits, i.e., $p2$–$p7$, generated by CLA adder are shown below.

$$m2 = x1 \oplus x[2] \tag{12}$$

$$m3 = m[1] \oplus c[0] \tag{13}$$

$$m4 = m[2] \oplus ((m[1] \cdot c[0]) + n[1]) \tag{14}$$

$$m5 = x[7] \oplus ((m[2] \cdot m[1] \cdot c[0]) + (m[2] \cdot g[1]) + n[2] \tag{15}$$

$$m6 = m[4] \oplus ((x[7] \cdot m[2] \cdot m[1] \cdot c[0]) + (x[7] \cdot m[2] \cdot n[1]) + (x[7] \cdot n[2])) \tag{16}$$

$$m7 = (m[4] \cdot x[7] \cdot m[2] \cdot m[1] \cdot c[0]) + (m[4] \cdot x[7] \cdot m[2] \cdot n[1]) + (m[4] \cdot x[7] \cdot n[2]) + n[4] \tag{17}$$

The CLA adder can produce result at faster rate without any waiting time compared to RCA because all sums and carries of it are generated simultaneously [10], which can be concluded by examining Eqs. (8)–(17).

The design is extended to develop 8 × 8, 16 × 16, and 32 × 32 multipliers using approximate compressors and CLA adders. The delay and area of approximate multipliers are reduced compared to exact multipliers by tolerating the error difference.

5 Results and Comparison

Every multiplier starting with 4 × 4 bit multiplier up to 32 × 32 bit multiplier is simulated and synthesized using Xilinx ISE 13.1 tool. The target device for synthesis is XC6SLX45, package CSG324 of Spartan-6 family. The simulation result of multipliers using approximate compressor and CLA adder is compared with the multipliers based on exact compressors with carry propagate adder for 4 × 4, 8 × 8, 16 × 16, and 32 × 32 bit Vedic multipliers. The comparison table of these multipliers in terms of delay is done based on synthesis report. The comparison result justifies that approximate multipliers are better than conventional multipliers in terms of speed and number of LUTs used. The sub-blocks such as approximate compressor and exact compressors are also compared by extensive simulations.

Faster multiplication is achieved using the approximate compressor with CLA adder replaces the exact compressor using carry propagate adder in the Vedic multiplier. The delay is reduced using approximate compressor compared to the exact multiplier in the Vedic multiplier; hence, the speed is enhanced. The simulation result of approximate multipliers is compared with the exact multipliers for 4 × 4, 8 × 8, 16 × 16, and 32 × 32 bit Vedic multiplier, and the parameters of them are compared in terms of delay as listed in Table 2. The simulation result of 16 × 16 and 32 × 32 bit Vedic multiplier using approximate compressor is shown in Figs. 6 and 7.

Table 2 Comparison of exact and approximate multipliers

Multiplier width	Exact compressor Vedic multiplier using carry propagate adder (ns)	Approximate compressor vedic multiplier using carry-look-ahead adder (ns)
4 × 4	9.248	8.535
8 × 8	13.266	12.432
16 × 16	17.269	16.434
32 × 32	21.501	20.666

Fig. 6 Simulation result of 16 × 16 multiplier using approximate compressor

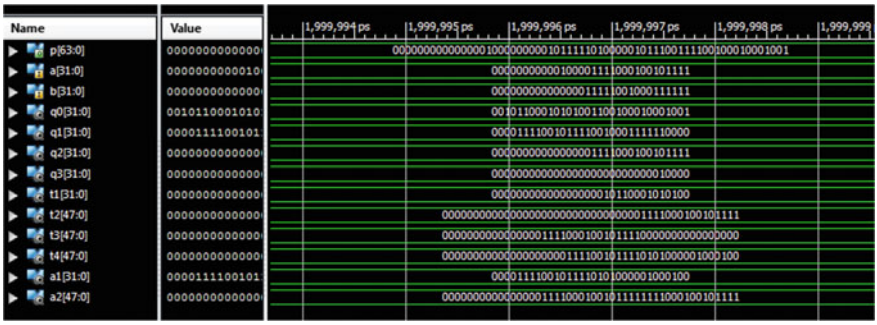

Fig. 7 Simulation result of 32 × 32 multiplier using approximate compressor

The RTL schematic view of 32 × 32 Vedic multiplier using approximate compressors is as shown below in Fig. 8.

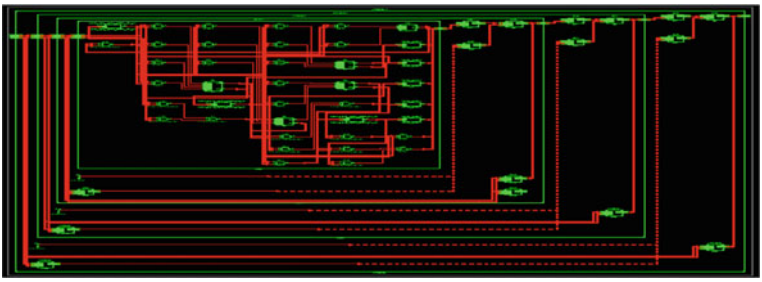

Fig. 8 Schematic view of 32 × 32 multiplier using approximate compressor

6 Conclusion

Faster multiplication is achieved using the approximate compressor and CLA adder by replacing carry propagate adder in the Vedic multiplier. The delay is reduced using approximate compressor compared to the exact multiplier in the Vedic multiplier; hence, the speed is enhanced. The work can be extended by reducing the complexity of CLA adder without affecting other performance metrics. The proposed work may be extended for a signed multiplier.

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Real-Time Automatic Peaks and Onsets Detection of Photoplethysmographic Signals

P. Madhan Mohan, V. Nagarajan and J. C. Vignesh

Abstract Photoplethysmography (PPG) is a biomedical signal which is obtained non-invasively by electro-optical sensors. Detection of peaks and onsets is required to estimate some important parameters such as heart rate (HR) and heart rate variability (HRV) using PPG signals. The robust detection of the peaks and onsets of a changing morphological wave with baseline drift and oscillations is a challenging one. This paper presents a novel real-time automated method to detect the peaks and onsets with low computational complexity. The method essentially consists of three stages. The first stage is a preprocessing stage where the PPG signal is transformed and smoothed followed by the detection stage where the peaks and onsets are detected. The last stage is the validation stage where the identified peaks and onsets are validated. The proposed method is tested with the PPG dataset, which is taken out of ten persons with duration of 10 min. The results reveal that the algorithm detects the peaks and onsets with highest average accuracy of 99.87%, average sensitivity of 99.91% and average positive predictive value (PPV) of 99.96%. The algorithm is implemented in the Cortex M4 platform using the Keil µvision 4 IDE and it requires only 12.52 kB of memory and speed of 0.5 MIPS. Since computational cost and speed is very critical for low-cost embedded platforms, the proposed method can be used to detect the peaks and onsets very effectively.

Keywords Photoplethysmography · PPG signal · Peaks · Onsets
Heart rate · Real-time

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1 Introduction

Diagnosis based on optical technology has increased in the recent years tremendously because of the availability of new optical devices and methods [1]. Even though photoplethysmography (PPG) was originally coined and used by Molitor and Kniazak [2] in the late 1930s, rapid developments are seen in the recent years to use the PPG optical sensors to estimate the vital parameters like heart rate, heart rate variability (HRV) [3], respiration rate, oxygen saturation of blood (SPO2). HRV is one of the main parameters that is estimated from the beats of the PPG signals to find the stress levels [4, 5]. The usage of PPG optical sensors and techniques is increased because of non-invasiveness [6], easy portability and cost effective than the traditional methods like an ECG.

The PPG sensors can be a transmission or reflection type which has LED (infrared, red) and photodiode pair [7]. The LED emits the light which passes through the tissue and gets transmitted or reflected after being partially absorbed by the hemoglobin of the blood. In the reflection-type PPG sensors, reflected light is captured in the photodiode which is placed next to the LED source as shown in Fig. 1a. In the transmission-type PPG sensors, transmitted light is captured in the photodiode which is placed opposite side as shown in Fig. 1b.

The PPG signal gets affected by various factors like subject's features (skin color, perfusion index) [8], sensor positioning, movement of the sensor while capturing the signal and environmental conditions which make the detection of peaks and onsets a difficult task. The accurate detection of the peaks and onsets are mandated to analyze the physiological conditions like HRV which depends upon the variation of time intervals between successive peaks. Many methods have already been suggested like Maxima and Minima [9], based on the slope sum [10] and derivative methods [11].

These methods used various preprocessing methods with different levels of computational complexity. The proposed algorithm uses a simple signal conversion and preprocessing method which would make the signal more robust than the original PPG signal and eliminates the need of baseline removal algorithms. It works in the real-time applications to detect the peaks and onsets effectively and accurately.

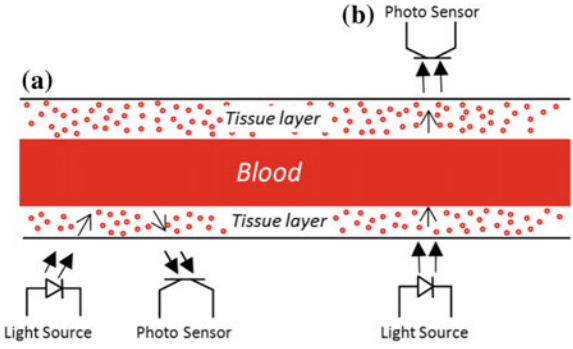

Fig. 1 **a** Reflection type. **b** Transmission type

The proposed method mainly operates on the impulse signal that can be obtained after subtracting the PPG signal from the smoothed and delayed version of the PPG signal. The first derivative of the smoothed impulse signal is used to find the peaks and onsets by using zero-crossing points. The zero-crossing point before the maximal inflection in the differential signal corresponds to onset and the point after the maximal inflection corresponds to peak. The process is automated by windowing the continuous real-time signal with optimal window size and applying the dynamic thresholding. The optimal search method is used to find the threshold in the current frame to identify the valid peaks and onsets.

This paper is organized by first exploring the Morphology of the PPG signal followed by algorithm in the Methods section. The next section is devoted to the results and discussion followed by a conclusion.

2 Methods

2.1 Morphology of PPG Signal

The PPG signal typically consists of pulsatile AC component superimposed on the DC component [12]. The pulsatile AC component is due to change in blood volume in the blood vessels [13] under the skin and it contains the valuable information. The rising part of the pulsatile component is formed due to the expansion of the artery diameter which increases the blood volume. The falling part of the pulsatile component is formed by the decrease in diameter of the artery which decreases the blood volume.

The rising part is called systolic phase and falling part is called diastolic phase. The DC component is mainly formed due to the reflected or transmitted light from the tissues. The morphological details of the PPG signal are given in Fig. 2.

2.2 Algorithm

The block diagram of the proposed method is given in Fig. 3. The algorithm basically has three blocks, namely preprocessing, detection and validation. Each block is explained in the below sections.

2.2.1 Block 1: Preprocessing

In the preprocessing block, the raw PPG signal is first windowed with the optimal window size. In the proposed method, the optimal window size of 5 s is taken after doing an analysis with different window sizes. The windowed signal is processed to

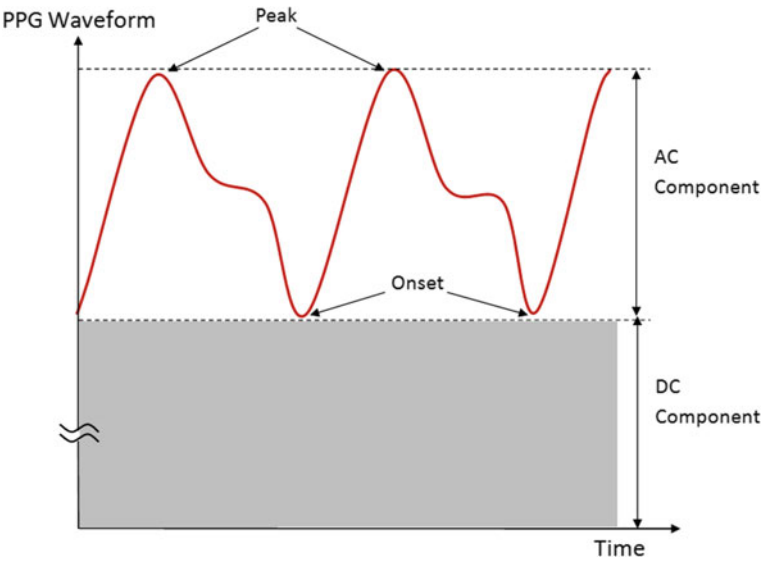

Fig. 2 Morphology of PPG signal

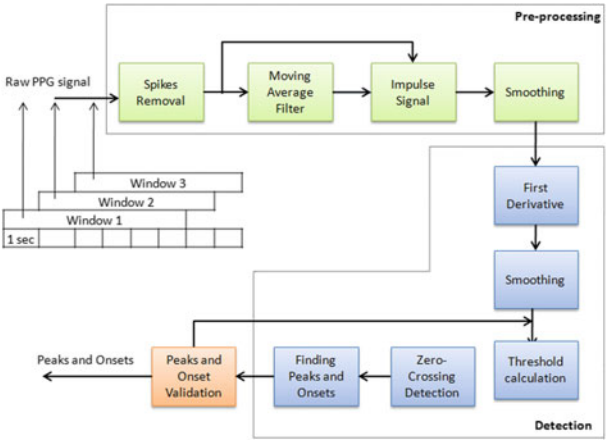

Fig. 3 Block diagram of the proposed method

remove any impulse noise like spikes if any, which would affect the performance of the algorithm. Median filter [14] is used to remove the spikes, which is mostly used method to eliminate the impulse noises.

The algorithm uses the fifth-order median after doing some preliminary analysis of the PPG signal. If the signal is distorted more at the input due to environmental conditions, then higher-order filter could be used. The spikes-removed signal (X) is

next smoothed using a simple moving average filter. The moving average filter works by averaging the K consecutive samples and it is given by

$$X_{\mathrm{sm}}(i) = \frac{1}{K} \sum_{j=-K/2}^{K/2} X(i+j)$$

The value K can be chosen based on the sampling frequency F_s. In the proposed method, the window size of ($K = F_s/2 - 1$) is taken and the window size is adjusted for the end samples on either side where it cannot accommodate the specified number of adjacent samples. The smoothed output would have a delay of ($K - 1$)/2. The delayed-smoothed signal is then transformed into an impulse signal by subtracting it from the spikes-removed PPG signal.

$$X_{\mathrm{imp}}(i) = X(i) - X_{\mathrm{sm}}(i)$$

The impulse signal is more robust than the original raw PPG signal and peaks are more visible and easier to detect. The impulse signal is further cleaned by using a smoothing filter with the window size of ($L = F_s/10 - 1$). Figure 4 shows the impulse PPG signal, impulse signal (X_{imp}) and smoothed impulse signal (X_{si}).

$$X_{\mathrm{si}}(i) = \frac{1}{L} \sum_{j=-L/2}^{L/2} X_{\mathrm{imp}}(i+j)$$

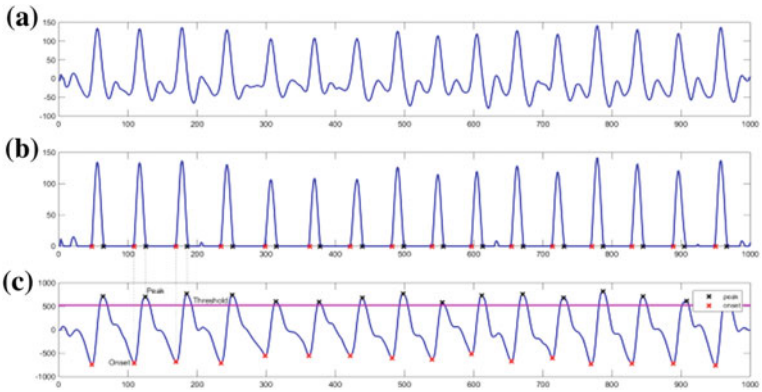

Fig. 4 **a** PPG signal. **b** Impulse signal. **c** Smoothed impulse signal

2.2.2 Block 2: Detection

In the detection block, the first derivative of the smoothed impulse signal is calculated first. The first derivative is then smoothed out to remove the noises of the derivative signal.

$$X_d(i) = X_{\mathrm{si}}(i) - X_{\mathrm{si}}(i-1)$$

$$X_{\mathrm{sd}}(i) = \frac{1}{L}\sum_{j=-L/2}^{L/2} X_d(i+j)$$

The smoothed-derivative signal is used to find the peaks and onsets. A dynamic threshold is set for each frame and it is used to reject the false peaks and onsets. The threshold is calculated based on the maximum peak to peak amplitude of the sub-windows that is formed in the sliding window based on the window length. The threshold value set would be 40–60% of the maximum peak-to-peak amplitude of the sub-windows. Then the peaks and onsets are obtained by detecting the zero-crossing points of the differential signal which crosses the threshold. In order to detect the zero-crossing points, a small window of five samples is used. If the multiplication of two adjacent samples is negative, then it is a zero-crossing point. Onsets are found by locating the zero-crossing points on the differential signal where the signal changes its direction from negative to positive (before the maximal inflection point). Similarly, peaks are found by locating the zero-crossing points, where the signal changes from positive to negative (after the maximal inflection point). Figure 5 shows smoothed-derivative signal, valid zero-crossing points and detected onsets and peaks. Figure 5c also indicates the dynamic threshold value.

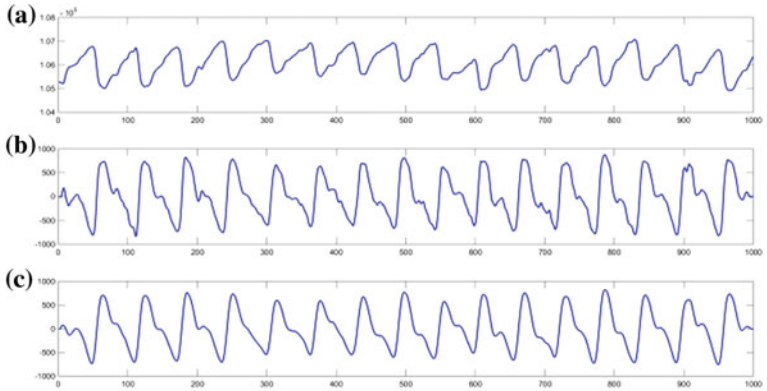

Fig. 5 **a** Smoothed-derivative signal. **b** Zero-crossing points. **c** Peaks and onsets

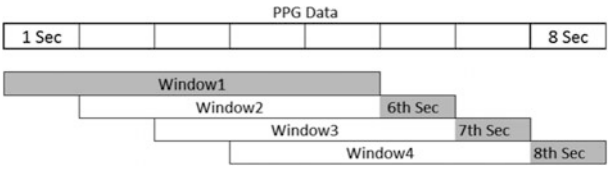

Fig. 6 Movement of the window and extraction of peaks and onsets

2.2.3 Block 3: Validation

In the validation block, the peaks and onsets estimated are validated based on certain rules. The difference between the adjacent peaks and onsets are calculated to validate it. Standard deviations of the peaks as well as onsets are calculated to identify if any peak or onset would cross the standard deviation threshold. If any outliers are identified, then it is removed. If peaks and onsets are missed, then the threshold is modified to reiterate the process to find the missed peaks and onsets. If the peaks and onsets are found to be valid, then they are stored and the window is moved to the next time frame.

2.3 Real-Time Automation

The peaks and onsets are extracted in pairs automatically in real time by moving the sliding window of 5 s for every 1 s. Figure 6 shows the movement of the sliding window in timeline. The first window "window 1" is used to extract the peaks and onsets for the first 5 s. The window is moved to the next time frame (window 2), which is from second to sixth seconds. The sixth-second peaks and onsets are extracted by comparing the window 2 and window 1 results. So every current second's onsets and peaks are extracted by removing the matching onsets and peaks in the current window with respect to the previous window. The results are stored in the buffer and used for further processing. This process is continued until the end of the stream.

3 Results and Discussion

3.1 Test Data

To verify the proposed algorithm, the dataset is collected at 100 Hz from reflective type PPG sensor for two test cases. In test case 1, data is collected for ten subjects, each subject with ten trials and each trial for 1 min. Stress analysis requires HRV data for 1 min approximately, and hence, one-minute data is taken for the testing in

case 1. In test case 2, data is collected for ten subjects, each subject with one trial of 10 min duration. This test is conducted to evaluate the robustness of the algorithm for long duration. The PPG data is collected from persons with different heart rate ranges.

3.2 Test Criteria

Three benchmark parameters as described in [15] are used to evaluate the performance of the algorithm.

Sensitivity: It gives the percentage of peaks (onsets) that are correctly identified.

$$S = \frac{\text{True Positive (TP)}}{\text{True Positve (TP)} + \text{False Negative (FN)}} * 100$$

Positive Predictive Value (PPV): It gives the percentage of peaks (Onsets) identified that are not false positives (FP).

$$\text{PPV} = \frac{\text{True Positive (TP)}}{\text{True Positve (TP)} + \text{False Positive (FP)}} * 100$$

Percentage Error:

$$E = \frac{\text{False Positive (FP)} + \text{False Negative (FN)}}{\text{True Positve (TP)} + \text{False Positive (FP)}} * 100$$

where

TP Peaks that are detected correctly,
FN Peaks that are not identified,
FP Non-peaks that are identified as peaks.

3.3 Test Results

The datasets are manually annotated for beats and compared with the proposed algorithm to evaluate the performance. Table 1 gives the performance of the proposed algorithm for peaks and onsets for case 1 (short files).

Table 2 gives the performance of the proposed algorithm for peaks and onsets for case 2 (long files).

Table 1 Performance of the algorithm for case 1

Subject	TP	FN	FP	%Sen	%PPV	%Error
S1	795	0	0	100	100	0
S2	850	0	1	100	99.88	0.12
S3	742	0	0	100	100	0
S4	670	1	0	99.85	100	0.15
S5	745	0	1	100	99.87	0.13
S6	978	1	0	99.90	100	0.10
S7	960	0	0	100	100	0
S8	850	1	0	99.88	100	0.12
S9	865	1	0	99.88	100	0.12
S10	840	0	0	100	100	0

Table 2 Performance of the algorithm for case 2

Subject	TP	FN	FP	%Sen	%PPV	%Error
S1	875	0	0	100	100	0
S2	841	1	1	99.88	99.88	0.24
S3	811	1	0	99.88	100	0.12
S4	752	1	0	99.87	100	0.13
S5	812	1	1	99.88	99.88	0.25
S6	736	1	0	99.86	100	0.14
S7	751	2	0	99.73	99.87	0.40
S8	810	1	0	99.88	100	0.12
S9	839	1	0	99.88	100	0.12
S10	795	1	1	99.87	99.87	0.25

Since the standard database is not available for PPG data, the proposed algorithm used the dataset collected from the experiments to evaluate the performance. The proposed algorithm results are compared with the other methods proposed in [15–17]. The other methods used different preprocessing filters and filter orders, threshold logic and datasets for the evaluation. Since different methods used different datasets for the evaluation, direct comparison cannot be made; however, the proposed algorithm has a very high sensitivity and PPV when compared to the other methods proposed in [15–17] and has a very lower percentage error than other methods. In case 1, out of 8295 beats, FN is only four and FP is two. In case 2, out of 8022 beats, FN is ten and FP is three only. So the average error percentage is only 0.07% in case 1 and 0.18% in case 2. Figure 7 shows the robustness of the algorithm and able to detect the beats when there is a drift and oscillations in baseline.

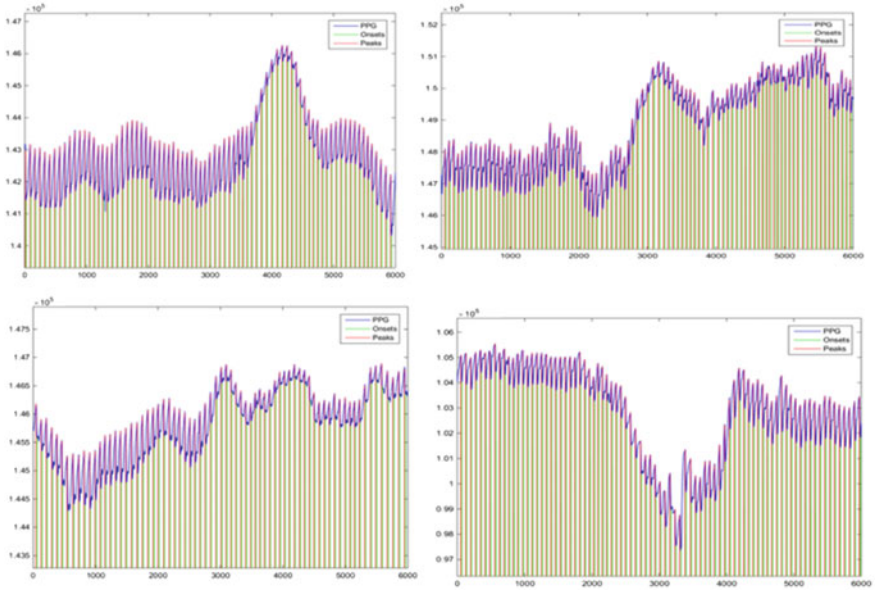

Fig. 7 Performance of the algorithm during drift and oscillations

3.4 Hardware Implementation

The proposed method is implemented in C and ported to Cortex M4 platform using the Keil µvision 4 IDE. Table 2 gives the hardware resources required for the algorithm.

RAM (kB)	ROM (kB)	Total memory (kB)
12.12	0.40	12.52

The total MIPS required to execute the algorithm is only 0.5 MIPS. So the speed of the algorithm is very high and requires only minimum hardware resources.

3.5 Simulation Testing

The MATLAB-based simulation tool is developed to analyze the PPG signals and plot the PPG and beats on the same plot. The tool is used to tune the algorithm to get the accurate results and also very useful to evaluate the performance of the algorithm. Figure 8 shows the MATLAB tool for algorithm evaluation.

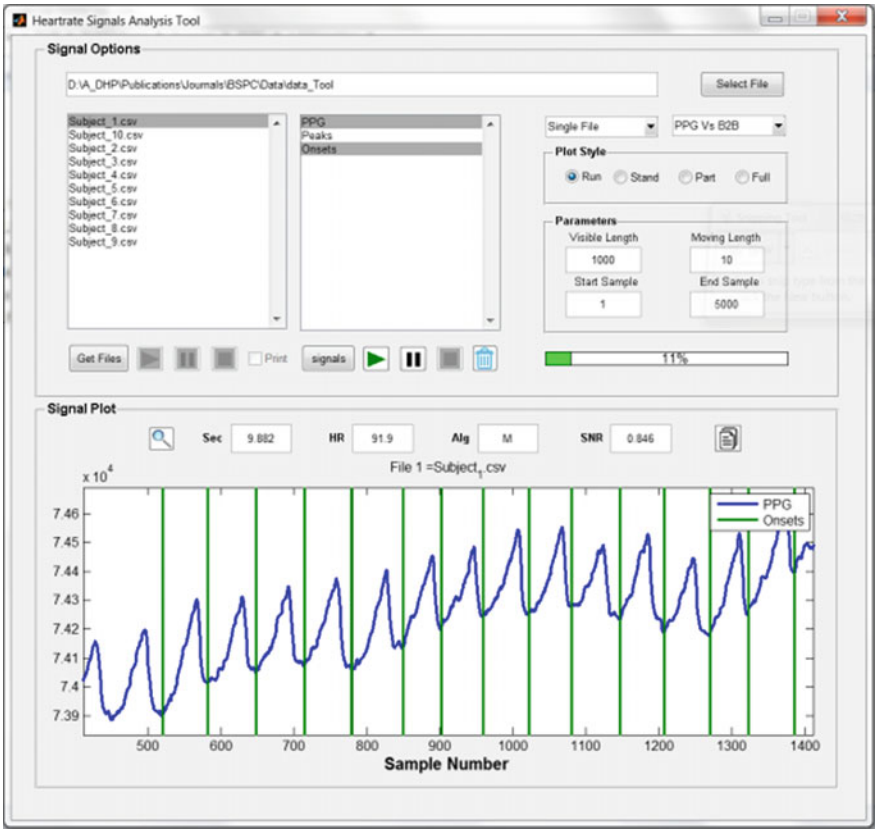

Fig. 8 MATLAB tool for algorithm evaluation

3.6 Real-Time Testing

The proposed method is tested in real-time environment using PPG sensor with M4-based evaluation board. A simple application is developed to call the algorithm to evaluate the performance. When a person put a finger on the sensor, the PPG signal is collected and fed to the application with the use of the internal drivers available in the evaluation board.

4 Conclusion

The proposed algorithm is able to detect the peaks and onsets very effectively from the morphology of the PPG signals. Though the morphology of the waveform is changing rapidly, the algorithm is able to adapt quickly to detect the beats by

employing the adaptive threshold logic. Since the algorithm works on the transformed signal rather than the original PPG signal, uses an adaptive threshold for each frame and efficient verification methods, the results are promising and comparable to the other published beat detection methods. The traditional beat detection algorithms demand high computational complexity because of using varying high-order filters, but the proposed algorithm requires minimal hardware resources because of using simple moving average smoothing filters and performs well in real-time environments. So it can be targeted to low-cost embedded platforms.

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Design of Low-Power CMOS Four-Quadrant Analog Multiplier in Nanometer Scaling

N. Sharath and S. Suhasini

Abstract A multiplier has vital impact in low power consumption and high speed. The analog multiplier constructed using current mode squarer circuits or voltage mode squarer circuits. In this review paper, analog multiplier using current squarer circuit for low power and high speed is presented because voltage mode squarer circuits consume more power and operate with less speed. High-speed multipliers can be employed in applications like neural logic, fuzzy logic, modulators, frequency doublers, and adaptive filters. New proposed design uses trans-linear loop for building compact structure analog multiplier with low supply voltage. The multiplier circuit is designed and simulated in cadence specter in nanometer scaling to achieve very low power and high speed.

Keywords Current mode squarer · Trans-linear loop · Cadence specter

1 Introduction

In recent days, design of building low power and low supply voltage design of four-quadrant analog multiplier is increasing in signal processing structures like adaptive filter, PLL, neural networks, and in fuzzy logic controllers, frequency doubler, rectifier, variable gain amplifier, and modulators [1–3]. New four-quadrant analog multiplier circuit has current mode squarer circuit operating in saturation region to reduce problems in subthreshold condition circuits, and saturation region current almost constant does not vary as supply voltage level increases. Squarer circuits operate in class AB current mode for multiplier implementation where nMOS and pMOS transistors have same trans-conductance parameters; otherwise,

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output of circuit is not correctly multiplied and this leads to total harmonic distortion. In that way, multiplier takes advantage of square root circuits or square law circuits. Squarer circuits employ square law characteristics for their operation in analog multiplier and communication system applications like peak amplitude detectors and frequency doublers. Three types of squarer circuits such as voltage mode, current mode, and mixed mode. By the way, voltage mode squarer circuits having problems like nonlinearity, more supply voltage consumption leads circuit to consume more power as well as decrease in speed of the system. The current mode squarer circuits better compare to voltage mode squarer circuits in the design of analog multipliers, i.e., low power consumption, high linearity, low distortion, high speed, and operating at higher bandwidth [4–7].

The new current mode squarer circuit proposed uses a simple current mirror circuit with four nMOS transistors with using low supply voltage technology, consuming less area and consume very low power, gives very high gain compare to previous proposed multiplier designs. However, multiplier design with trans-linear loops operates at wide range of bandwidth and high speed [8]. To reduce issues like body effect and channel length, modulation can be overcome by using cascade current mirror in the squarer circuit also to improve the gain and bandwidth of circuit. Remaining part of work is as follows: Sect. 2 tells about literature survey, Sect. 3 tells about circuit description, and conclusion as follows.

2 Literature Review

2.1 High Precision Analog Multiplier

The author [4] proposed current mode squarer circuit can design using a current squarer and one current mirror. The circuit is designed with 12 mos transistors. Results are plotted using HSPICE simulator in 350 nm standard CMOS technology. Giving power supply voltage of 2 V and input bias current of 4.6 μA getting output power dissipation is equal to 0.232 mW and 3-dB bandwidth of 485 MHz. Advantages of multiplier design have low linearity error, and improved 3-dB bandwidth improves circuit performance.

2.2 Multiplier with Device Independent Parameters

The author [5] who proposed design mos transistor device parameters does not affect output current and input resistance which has no effect on input current. The multiplier composed of current mode squarer circuit with current mode subtractor and uses 22 transistors. Input bias current signal not required in the multiplier and simulated using 2.0 μm p-well CMOS parameters (BSIM3 parameters) and giving

supply voltage of 5 V and input bias current of 80 μA getting output as power dissipation is equal to 0.93 mW and 3-dB bandwidth of 22.4 MHz. Disadvantage of this paper, which is the usage of large power supply, leads to linearity errors and decrease in speed of the design.

2.3 Low Power Multiplier

The author [1] proposed circuit composed of dual trans-linear loop is important for realization of multiplier design and can be used as multiplier or divider. Design consists of squarer circuit and composed of 12 mos transistors. Main advantages of multiplier design are high speed, low power, and less dc offset error. To guarantee biasing of transistors, bias current cannot reduce to minimum and input currents *Ix* and *Iy* constant equal to ±10 μA obtain divider circuit.

The multiplier design simulated using HSPICE simulator in 0.35 μm standard CMOS technology. By applying power supply voltage of 3.3 V and input bias current of 10 μA getting output power dissipation is equal to 0.34 mW and 3-dB bandwidth of 41.8 MHz. Disadvantage of this paper is usage of large power supply and body effect occurs.

2.4 Micro Power Multiplier/Divider

The author [2] who proposed multiplier circuit consists of trans-linear loops operating in the weak inversion mode is primary components of the design. Multiplier/divider consist 19 mos transistors, and advantage of the design is high accuracy over a wide dynamic range and low power consumption. Multiplier/divider results obtained using HSPICE simulator tool in 350 nm standard CMOS technology. Giving power supply voltage of 2 V and input bias current of 50 nA getting output as power dissipation is equal to 9 μW and 3-dB bandwidth of 19 MHz. Drawback of this circuit design is mismatch associated with circuit parameters.

2.5 Multiplier Circuit with High Speed

The author [3] who proposed circuit designed to operate in high speed using current mode squarer as building block of the circuit and dual trans-linear loop. The design composed of 20 mos transistors. The multiplier circuit outputs are plotted in HSPICE simulator by level 49 parameters in 350 nm standard CMOS technology. Giving supply voltage 3.3 V and input bias current 10 μA, results are power dissipation equal to 0.24 mW and 3-dB bandwidth of 44.9 MHz. Advantages are more speed and less power consumption. Disadvantage of this paper is the usage of high power supply.

2.6 A Novel Current-Mode Multiplier/Divider

The author [6] proposed multiplier/divider circuit very simple compare to previous designs, and the designed circuit is operating at two power supplies and comparing the output power dissipation for different power supplies. The design is composed of 10 mos transistors and hence multiplier is very simple. Multiplier results are evaluated in HSPICE simulator tool in 250 nm standard CMOS technology. Giving two different power supply voltages of 3.3, 2.5 V and input bias current of 10 μA yielding output as power dissipation are equal to 168.1 μW and 3-dB bandwidth of 278 MHz. Advantages are circuit which is very simple, high speed, linearity, and low power consumption.

2.7 Simple Low Error Multiplier

The author [9] proposed analog multiplier without input bias current I_{bias}, and squarer circuit is the modified version of [4] and circuit composed of 8 mos transistors implies requires less area. Multiplier design is very easy, requires low area, high speed low error are main advantages. The current squarer circuit suffers from body effect ($V_{SB} \neq 0$) and reduces performance of multiplier design. The multiplier is designed and simulated using HSPICE simulator in 180 nm standard CMOS technology. Giving power supply, voltage of ±0.7 V DC getting output power dissipation is equal to 41.25 μW and 3-dB bandwidth of 903 MHz.

2.8 Simple High-Speed Multiplier

The author [10] proposed circuit design is depending on geometric mean and squarer/divider circuit of three blocks imply low power, higher 3-dB bandwidth, and simpler in structure are the main advantages. Multiplier input resistance is independent of input current, and multiplier is designed by using three squarer blocks and design is composed of 12 mos transistors. The circuit is simulated using cadence specter and asura in 0.18 μm CMOS technology, power supply voltage is 1.8 V. Outputs are power dissipation of 81.2 μW and 3-dB bandwidth of 840 MHz.

2.9 Current Mode Analog Multiplier

The author [7] proposed circuit design depends on squarer law that is simple current mirror circuit operates in saturation region. The multiplier results obtained using TSPICE in 180 nm CMOS technology with a supply voltage of 2 V. Drawback of

the design is less 3-dB bandwidth is achieved, i.e., 493 MHz and circuit has low power dissipation of. 146.48 µW.

2.10 Multiplier in Weak Inversion Region

The author [8] proposed circuit design is the modified version of the current mode analog multiplier. Multiplier consists of exponential approximation circuits which are an initial building blocks operating in weak inversion region. New multiplier results are carried out in 180 nm CMOS technology by using tanner tool with a very less supply voltage of 0.5 V. Main advantage of using exponential approximation circuit is to achieve very less power dissipation of 598 nW and can be used in various analog circuits.

3 Circuit Design

3.1 Proposed Current Squarer Circuit Design

Current squarer circuits are mainly used in peak detectors, multiplier and divider circuits, and modulators. The new current squarer circuit proposed is based on [4, 5]. Figure 1 shows proposed new current squarer circuit which consists of current squarer and cascade current mirror with four nMOS transistors with input currents I_{bias} and I_{in}. Current mode squarer circuit operates in saturation region.

Compare to usage of low voltage in multiplier design [9, 10], proposed design having 20 transistors and operate over a wide range of bandwidth. Current through transistor M2 can be given as

$$Io = K_2(V_E - V_3 - V_{TN1} - V_{TN3})^2 \tag{1}$$

where K_2 is trans-conductance parameter of transistor M_2 given by K_2 = 0.5 µCox (W/L), where Cox is gate oxide capacitance per unit area and μ is electron mobility, taking µCox value as 110 µ/m, W is width, and L is length of transistor. Where V_2 and V_3 are gate–source voltages of transistor M_2 and M_4, V_{TN2}, and V_{TN4} are the threshold voltages of transistor M_2 and M_4, respectively. Voltage across the node near resistor R

$$VR_3 = R(I_{in} + I_{bias}) + V_3 \tag{2}$$

where R is resistance and I_{in} is input current and I_{bias} is constant current to the proposed squaring circuit and the voltage can be calculated using

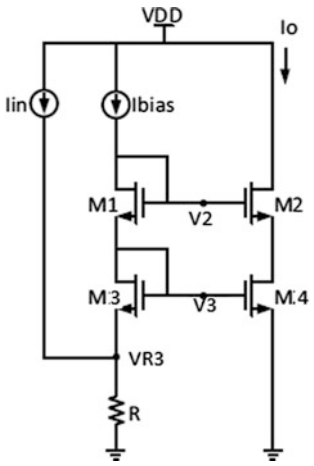

Fig. 1 Proposed current squarer circuit

$$V_3 = RI_{\text{bias}} + V_{\text{TN1}} + V_{\text{TN3}} + \sqrt{(2I_{\text{bias}}/K_1)} \tag{3}$$

$$V_2 = R(I_{\text{in}} + I_{\text{bias}}) + V_{\text{TN1}} + \sqrt{(2I_{\text{bias}}/K_1)} \tag{4}$$

And output voltage V_o is given by

$$V_o = RI_{\text{bias}} + V_{\text{TN1}} + \sqrt{(2I_{\text{bias}}/K_1)} \tag{5}$$

Equation (1) will be modified to Eq. (6)

$$I_o = K(RI_{\text{in}} + V_E)^2 \tag{6}$$

3.2 *Proposed Multiplier Circuit Design*

Four squarer cells are required to implement the four-quadrant multiplier structure by using Eq. (6) given by $[I_x + I_y]$, $-[I_x + I_y]$, $[I_x - I_y]$ and $-[I_x - I_y]$. The four different currents are applied as inputs to four squaring circuits of the multiplier and outputs of the squaring circuits are as follows

$$I_{\text{out1}} = K\left(R\left(I_x + I_y\right) + V_E\right)^2 \tag{7}$$

$$I_{\text{out2}} = K\left(-R\left(I_x + I_y\right) + V_E\right)^2 \tag{8}$$

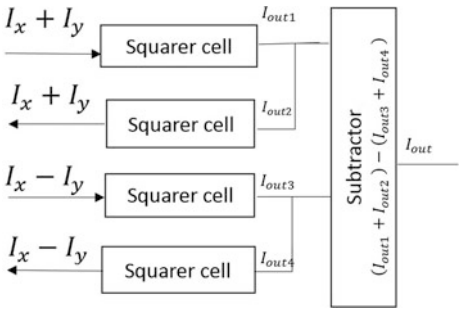

Fig. 2 Schematic of new current mode multiplier

$$I_{\text{out3}} = K\left(R\left(I_x - I_y\right) + V_E\right)^2 \tag{9}$$

$$I_{\text{out4}} = K\left(-R\left(I_x - I_y\right) + V_E\right)^2 \tag{10}$$

From above four current equations, output current of multiplier calculated by giving above four current equations into subtractor given by as follows

$$I_{\text{OUT}} = (I_{\text{out1}} + I_{\text{out2}}) - (I_{\text{out3}} + I_{\text{out4}})$$

Therefore,

$$I_{\text{OUT}} = 8KR^2 I_x I_y \tag{11}$$

Schematic for the output current I_{OUT} using four squarer circuits output currents, i.e., I_{out1} and I_{out2} subtracted from I_{out3} and I_{out4} using subtractor shown below in Fig. 2. Comparison between the parameters used in proposed work and previous works shown by Table 1.

Table 1 Comparison of new current mode multiplier and previous works

Reference No.	Technology (µm)	Supply voltage (V)	Input range (µA)	Power dissipation (µW)
[4]	0.35	2	±10	232
[5]	2	5	±20	930
[1]	0.35	3.3	±10	340
[2]	0.35	2	±10	9
[3]	0.35	3.3	±10	240
[6]	0.25	3.3, 2.5	±10	168.1
[9]	0.18	±0.7	±10	41.25
[10]	0.18	1.8	±20/10	89.2
[7]	0.18	2	±10	146.48
Proposed	0.18	1.8	±10	83.66

4 Conclusion

In this paper, analog multipliers are shortly surveyed about the basic design of building blocks of the multiplier like squarer circuits and design characteristics of the new squarer circuit depend on square law characteristics and the analysis of the performance parameters of new multiplier circuit. The new four-quadrant analog multiplier circuit can operate with low supply voltage technology and high speed. Advantages of the proposed design are low power, less area. This can be done by taking I_x and I_y as 10 μA.

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Designing 5T Embedded DRAM Cell for Ultra-Low-Power Low-Voltage Applications Based on Schmitt Trigger

V. Snigdha Chandrika and M. Maria Dominic Savio

Abstract In this proposal, we explained about 5T embedded DRAM cell which is designed based on Schmitt trigger concept. The proposed design is mainly useful for low-power, small-size applications with greatly reduced cost prize. Also, Schmitt trigger-based bit cells incorporate a built-in feedback mechanism which will be greatly useful for further nanoscaled devices. It was simulated using 45-nm CMOS process technology, and the obtained results prove that the design achieves increased read and write static noise margin (SNM) when compared with conventional 6T and 10T bit cells when powered with 0.9 V. The design also possesses lowest leakage power dissipation comparatively.

Keywords Data retention time (DRT) · Access speed · Static noise margin (SNM) Power dissipation (PD) · Refresh cycles · SRAM · DRAM

1 Introduction

As technology keeps improving the necessity of miniature devices yet with high speed and performance are increasing. But the more a transistor gets scaled, the more the power gets leaked which in turn effects the circuit performance. It is well known that 90% of the die area in system on chip (SOC) is occupied by embedded memories, say SRAM cells. All time chosen option for the purpose is 6T bit cell due to its high-speed access. However, it requires 6 transistors to store a single bit data where a DRAM cell will do the same with a single transistor and capacitor. Also, in 10T bit cell, write ability gets degraded with the series connected with write access transistors. Along with the crosscoupled inverter pair for data storage, an extra transistor is needed for decoupling. Apart from DRAM's only disadvantage, i.e. requiring continuous power pulses, it has a very attracting merits like less power consumption, occupies less space and is cheap in cost. In standby mode,

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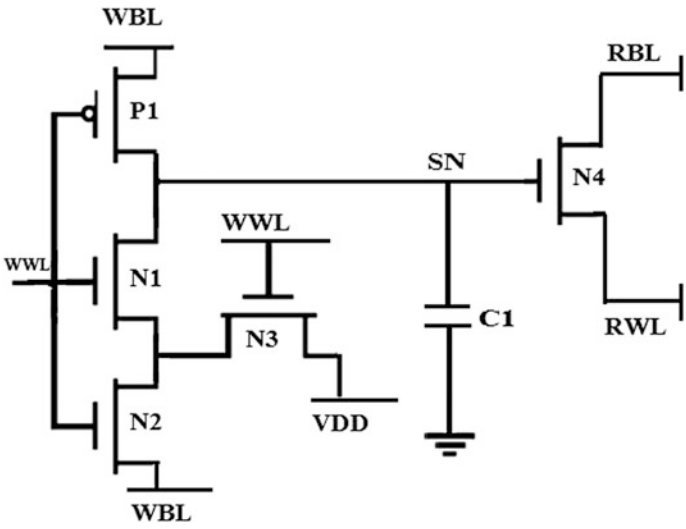

Fig. 1 Schmitt trigger-based 5T DRAM cell

DRAM's stored data get leaked unless it is provided with continuous refresh cycles at a particular time periods. Scaling the power supply voltages adversely effects the overall power dissipation, and also, the parameters sensitivity factor gets increased. This limits the circuit operation, especially the circuits comprising minimum-sized transistors. All these together may lead to memory operation failures (Fig. 1).

The demand for battery-operated devices like cell phones, implants used in medical field and wireless sensor networks in today's generation shows great interest towards DRAM cell research area. So in this paper, a Schmitt trigger-based 5T DRAM cell is proposed which gives us minimum power, minimum delay and area when compared with other conventional bit cells 6T, 8T, 10T.

2 Proposed ST_5T Gain Cell

2.1 Schmitt Trigger-Based Cell Design

For subthreshold bit cells, cells operating at voltage lower than the power supply have to face a difficulty in read and write stability. So to improve the cell stability, a Schmitt trigger concept has been introduced into memory cells [1]. A Schmitt trigger-based SRAM cells resulted in improved storage noise margin and performance when has compared with other conventional bit cells. However, it suffers from read and write operation failures. An inverter pair based on Schmitt trigger and its characteristics is shown in Fig. 2. Density architecture of SRAM cells limits their application in high-capacity, low-cost structures [2]. Built-in feedback

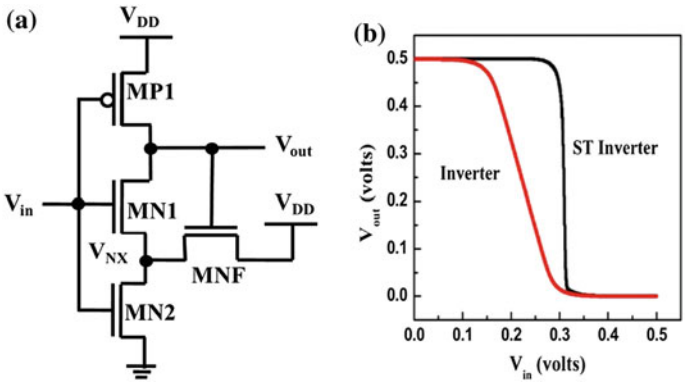

Fig. 2 **a** Schmitt trigger-based inverter, **b** output of Schmitt trigger

mechanism of Schmitt trigger-based cells is used only in the pull-down path, i.e. only during 0–1 transition. For 1–0 transition, the feedback path gets disabled which helps in effective write operation. Here, if MNF is ON and the node voltage at V_{NX} is $V_{DD} - V_{TH,}$ then V_{out} is driven high for which the minimum voltage for switching operation will be greater than V_{THN} at the input. As the inverter characteristics are improved, its also provides higher SNM. To maintain the clarity in future discussion, Schmitt trigger-based 5T DRAM cell is termed as ST-5T bit cells and the rest are termed as con-6T, con-8T, con-10T, con-5T.

2.2 Proposed ST-5T DRAM Cell

Schematic of Schmitt trigger-based 5T DRAM cell and its timing diagram is shown in Fig. 3.

Proposed ST-5T DRAM cell consists of Schmitt trigger inverter, read access transistor, a storage capacitor and control signals read bit line (RBL), read word line (RWL), two write bit lines (WBLs), two write word lines (WWLs). The inverter is controlled by storage node (SN). The proposed ST 5T DRAM cell operates with ultra-low voltage and consumes comparatively negligible power (Fig. 4).

Considering the storage capacitor is fully charged, WWL is driven high, while WBL is grounded. So the capacitor gets discharged through the short-circuit path and 0 is written at storage node (SN) [3]. During read operation, the precharged RBL is driven high and RWL is made 0. Now, since the storage node voltage is 0, no charge will pass from RBL to RWL and so 0 is read. At read and standby modes, WBL is maintained at $V_{dd}/2$ so that leakage current gets avoided which improves the data retention time (DRT) [4].

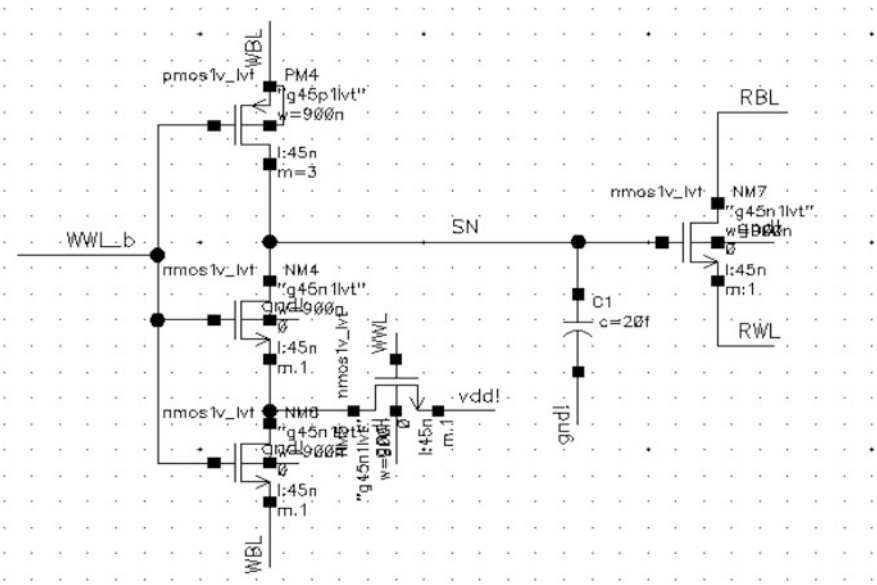

Fig. 3 Schematic of ST-5T DRAM cell

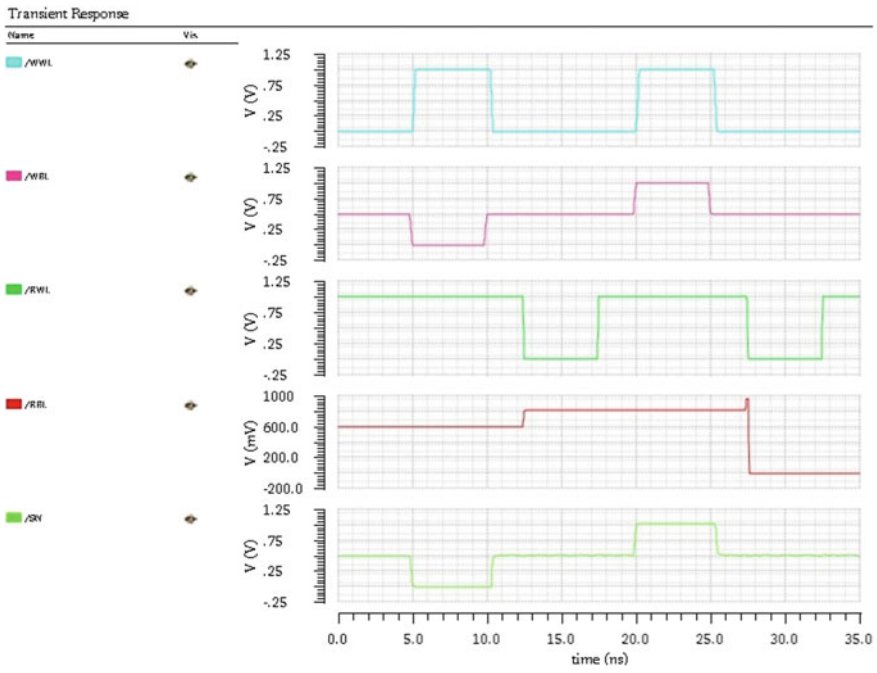

Fig. 4 Simulation of ST-5T DRAM

3 Simulation Results

Cadence virtuoso tool was used to take the simulation results, and power and low-voltage operation were studied under 45-nm CMOS process technology [5]. Having a look at the simulation results, it is clear that the proposed design consumes low power of all the other conventional bit cells (Fig. 5).

3.1 6T SRAM Cell

See Figs. 6 and 7.

3.2 8T SRAM Cell

See Figs. 8 and 9.

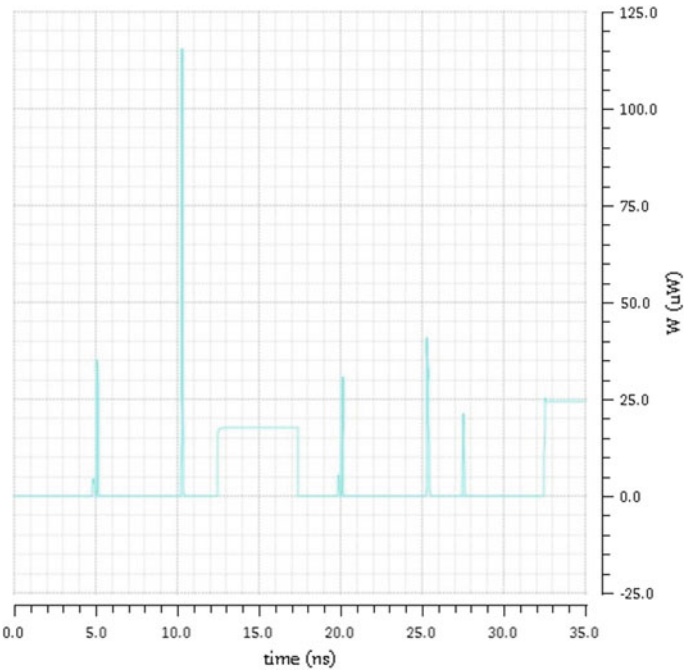

Fig. 5 Power output of ST-5T bit cell

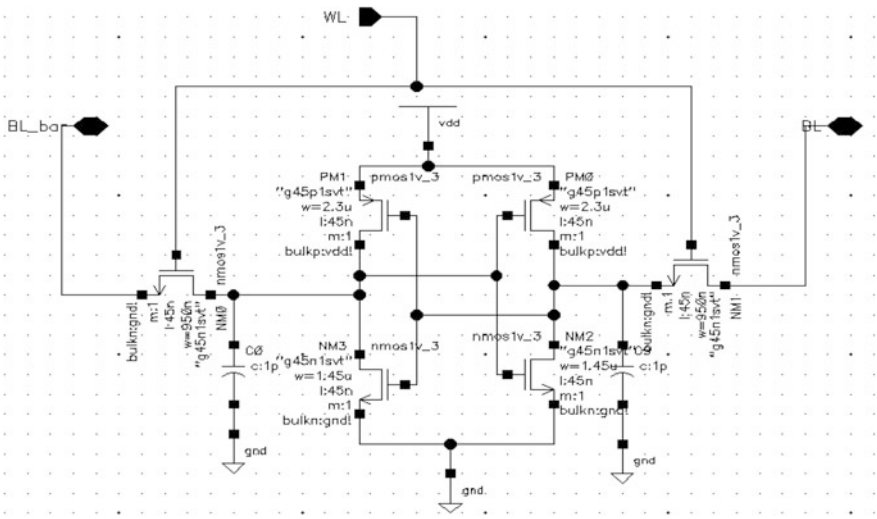

Fig. 6 Schemetic of 6T SRAM cell

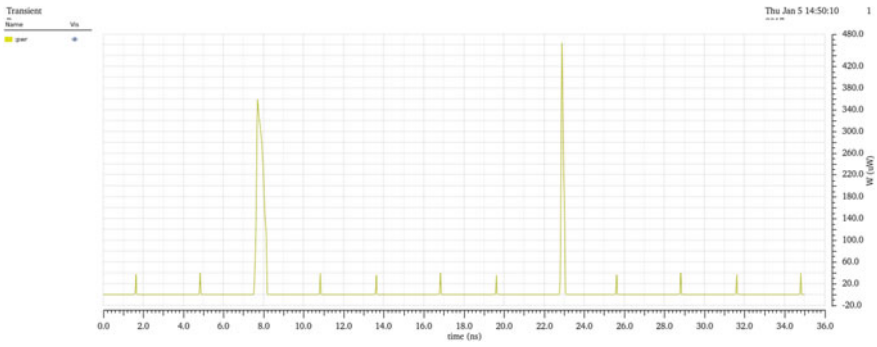

Fig. 7 Power output of 6T SRAM cell

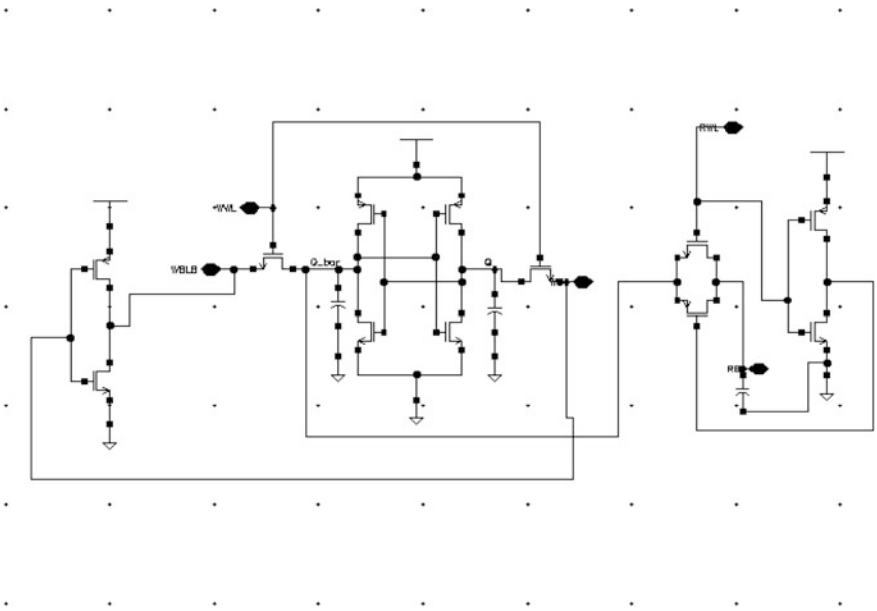

Fig. 8 Schematic of 8T SRAM cell

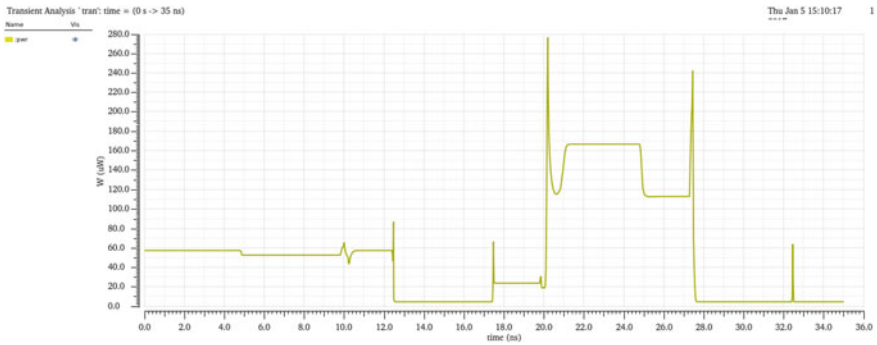

Fig. 9 Power output of 8T SRAM cell

3.3 10T SRAM Cell

See Figs. 10, 11 and Tables 1, 2.

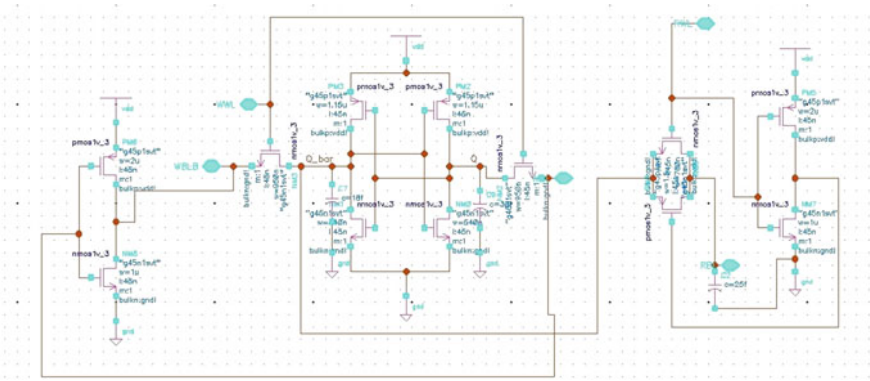

Fig. 10 Schematic of 10T SRAM cell

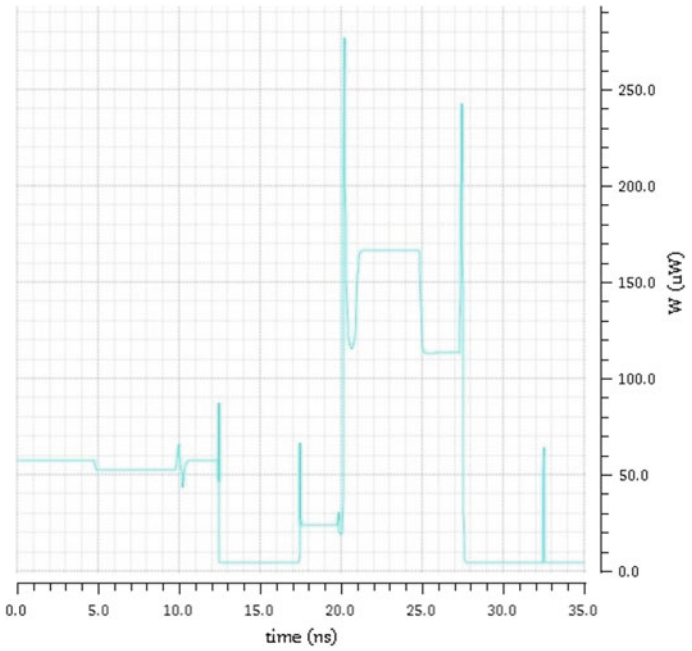

Fig. 11 Power output of 10T SRAM cell

Table 1 Specification table

Parameters	ST_5T
Process technology	45 nm
Power supply voltage	0.9 V
Pmos width	900n
Nmos width	450n
Power during reading	1.697n
Power during write	2.435u

Table 2 Comparison of bit cells

S. No.	5T	6T	8T	10T	ST_5T
Read	Single ended	Differential	Single ended	Single ended	Differential
Write	Single ended	Differential	Differential	Differential	Differential
WL	1	1	2	2	2
BL	1	1	2	2	2
Pmos	2	2	2	4	1
Nmos	3	4	6	6	4
Max power (uW)	312.6	509.24	383.12	276.42	139.98
Delay (n)	5.99n	8.84n	507.8p	1.068n	216.0p

4 Conclusion

A Schmitt trigger-based 5T DRAM cell focusing on ultra-low-power application with high device performance is proposed. It operates under very low voltage which is a prior feature in today's technology. The proposed cell exhibits less power and less area than the existing bit cells. The ability of operating under a single-supply voltage so as to eliminate the need of refresh cycles to improve the data retention time (DRT) further needs to be considered as future work.

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Design and Implementation of Multi-bit Self-checking Carry Select Adder

Shivkumar Kavitkar and A. Anita Angeline

Abstract This paper focuses on the design of self-checking carry select adder (CSTA) using FinFET devices. The CSTA adder comprises of Boolean to Excess-1 converter and D-latch. While going for multi-bit addition, it is more prone to various types of faults. Hence, the design of a self-checking CSTA is more prone to faults. This paper focuses on the design of 4-bit CSTA using FinFET and a sum bit checker design using FinFETs. The simulations are carried out using Cadence® Virtuoso platform with 32-nm FinFET technology library. The results demonstrate a device overhead of 12 and slight increase in delay and power consumption. However, the purpose of the carry checker design has a great impact on preventing the propagation of faults and ultimately ends in fault-free circuit.

Keywords Carry select adder · FinFET · Self-checking adder

1 Introduction

The adder unit plays a vital role in any digital system design. Even though many adders were contributed by the researchers, the choice of the adder for an application is based on the power consumption or speed of operation. The CSTA has a major advantage of high speed in comparison with the ripple carry adder (RCA). However, the complexity of the CSTA structure makes it necessary to have fault identification circuits. Furthermore, the incorporation of the sum checking circuit will cause an increase in the number of devices and power consumption [1].

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The gradual decrease in size of transistor over time, in accordance with Moore's Law [2], had led to a world of faster, smarter, and efficient electronic equipments. The MOSFETs have gradually scaled down from several micrometer technologies to 22-nm technology. As the technology scales down, the subthreshold leakage increases leading to more amount of static power consumption. Hence, Intel focused on the radical redesign of the transistor. This eventually led to the invention of FinFET in the year 2012. This dual-gate 3-D device, the FinFET offers a reduction in the subthreshold leakage by suppressing the short-channel effects [2]. Thus, the FinFETs offer a better replacement of the MOSFETs in domino logic circuits.

Thus, it is imperative that the usage of appropriate type of device under lower technology will lead to decrease the drawbacks which are associated with the earlier design. In this paper, the design of the adder circuit and the sum checker design are performed using FinFETs.

This paper details the design and implementation of 4-bit carry select adder with self-checking mechanism using FinFET for the carry bit. This makes the design to be more reliable and faster with minimal power dissipation. Section 2 elaborates the usage of FinFETs and the design of CSTA, and Sects. 3 and 4 elaborate the design of CSTA with sum checker for carry. Section 5 analyzes the circuit design, and Sect. 6 concludes.

This paper details the design and implementation of 4-bit carry select adder with self-checking mechanism using FinFET and proposes the self-checking mechanism for the carry bit. This makes the design to be more reliable and faster with minimal power dissipation. Section 2 elaborates the design of CSTA, followed by Sect. 3 depicting the dual-pair dual-rail checker structure. Section 4 elaborates the design of CSTA with dual-pair dual-rail checker for carry and sum. Section 5 discusses the simulation and analyzes of the circuit counterparts, and Sect. 6 concludes.

2 The FinFETs

The dual-gate 3-D FinFET device suppresses the short-channel effects in comparison with the MOSFET device. The FinFET devices are used in the following two modes [3].

- Shorted gate: In this mode, a 3-terminal device is formed which replaces the CMOS devices without any changes. Both the gates of the FinFET are tied together. The power consumption is reduced in this case.
- Independent gate: In this mode, a 4-terminal device is formed which can replace two MOSFETs with a parallel connection. Both gates are separately controlled in this case offering more design options.

3 The Carry Select Adder (CSTA)

The carry select adder (CSTA) adder compute (k + 1) bits sum of two k-bit numbers and the carry bit. The structure comprises of ripple carry adders and multiplexers. The CSTA is the fastest adder circuit owing to its circuit architecture [2].

The CSTA is a two-level structure adder. It performs addition at two different levels considering carry as '0' and '1' simultaneously. The sum bits (S_0 and S_1) are selected using a multiplexer depending on the C_{in} bit as shown in Fig. 1 [4–7].

The sum bits of two successive stages are used in identifying the fault in the sum bit. The outputs of the first-stage sum S_{00} and S_{01} are always complimentary. In order to feed the complimentary signal in the next stage, it is fed through a XNOR gate and then fed to the checker unit as shown in Fig. 2. The functionality of the checker unit is given as in Eq. 1.

$$\text{CHECK\_SUM} = (Y_0 \oplus Y_1) \odot (X_0 \oplus X_1) \tag{1}$$

The internal architecture of the sum checker using FinFETs is shown in Fig. 2 and the transistor level schematic is represented in Fig. 3.

In the CSTA design, the 2 × 1 multiplexer plays a major role in choosing the sum depending on the carry C_{in} signal. The design of a 2 × 1 multiplexer is shown in Fig. 4.

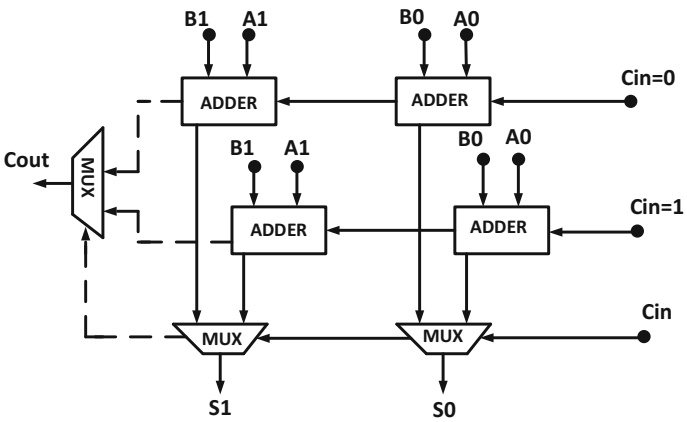

Fig. 1 Carry select adder (CSTA)

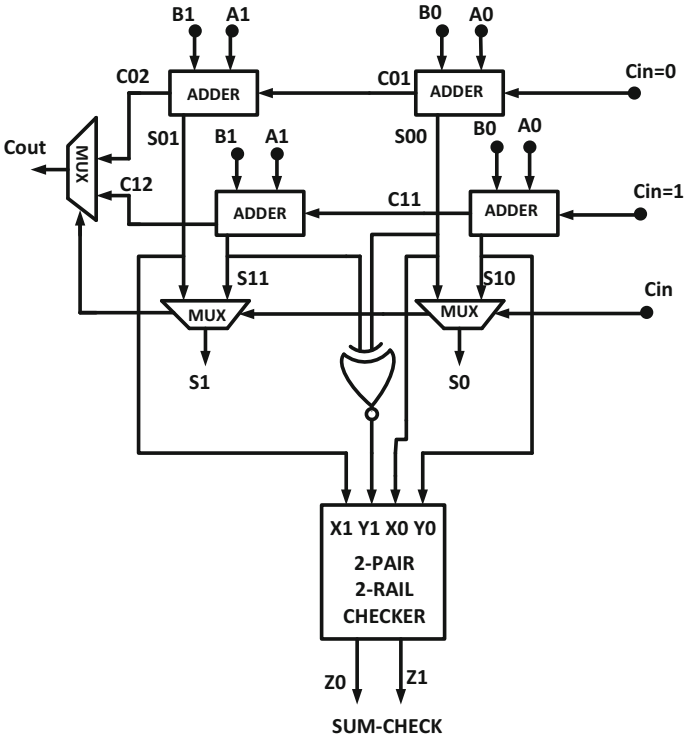

Fig. 2 Self-checking 2-bit CSTA with dual-pair dual-rail checker

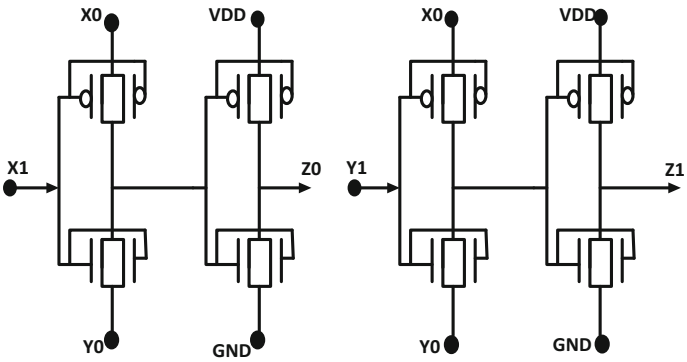

Fig. 3 Dual-pair dual-rail sum checker using FinFETs

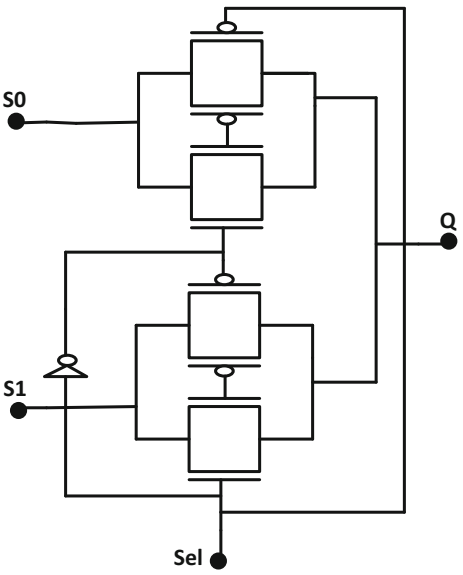

Fig. 4 2 × 1 multiplexer using FinFETs

4 Multi-bit Self-checking CSTA

In the case of multi-bit self-checking CSTA with sum checker unit as shown in Fig. 5, for all the sum bits, the checking is performed. The sum bits along with the complemented form from the other level line and the consecutive stage sum bits in the complimented form are utilized. Finally, the C_{out} bit is obtained from the multiplexer at the end M_n.

The dual-pair dual-rail checker is basically the sum checker circuit which yields Z_1 and Z_2 outputs. The Z_1 and Z_2 being complimentary indicate the presence of faults, and if not, it ensures fault-free condition.

5 Simulation Results and Analysis

Verilog-A source code of 32-nm technology FinFET provided by UC Berkeley BSIM Group is utilized for design and simulation.

A 4-bit CSTA with two rails, one for the carry in = '0' and other for carry in = '1', with sum checker is designed. The sum outputs are taken from the multiplexers and the final C_{out} from the M_n multiplexer.

The simulation results as shown in Fig. 6 demonstrate the sum and carry outputs. Furthermore, the Z_0 and Z_1 indicate the fault condition of the adder circuit. For the sake of analysis, stuck-at-1 fault is introduced at the input of XNOR and tested. The results reveal a complimentary output at Z_0 and Z_1 if fault exists and vice versa.

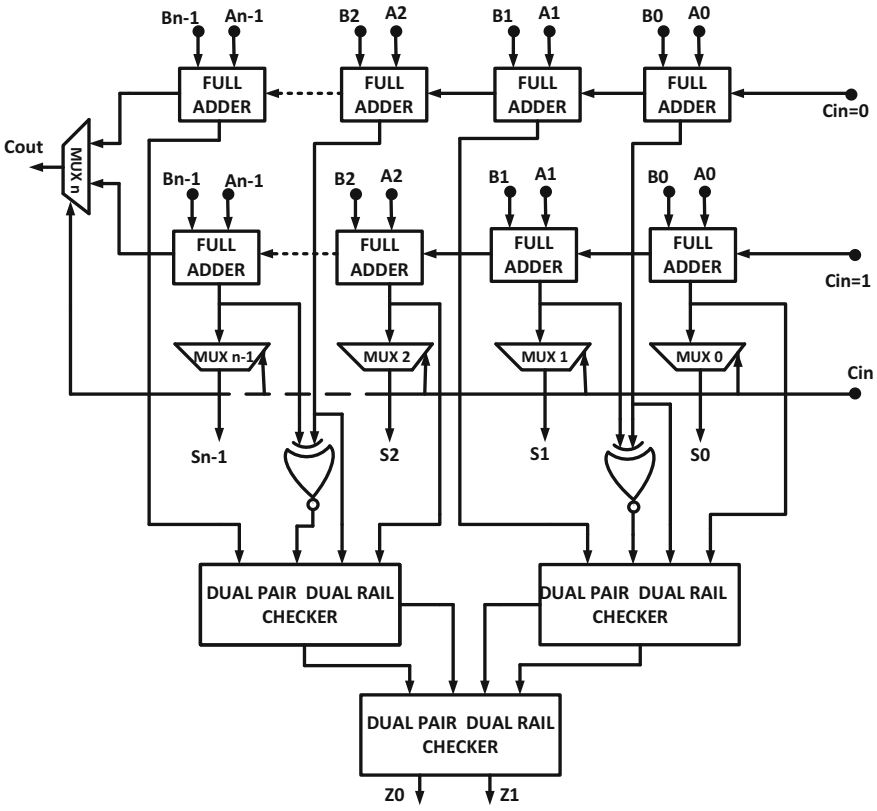

Fig. 5 Self-checking *n*-bit CSTA

In a 4-bit adder, for an input sequence of *A* (0110) and *B* (1100), the sum is obtained as *S* (1001) with a carry of $C_{out} = 0$ as shown in Fig. 6.

The design of 4-bit CSTA with sum checker demonstrates device overhead of 14 transistors and increased delay as in Table 1.

6 Conclusion

The paper presented the design of CSTA with sum checker circuits. It demonstrates that the sum checker and carry checker circuits are very efficient in fault identification process with an additional power consumption of 38 μw. This makes it a mandatory and inherent part of the adder circuit in avoiding faults at the output. The use of FinFETs has facilitated the additional advantage of lowering the power consumption.

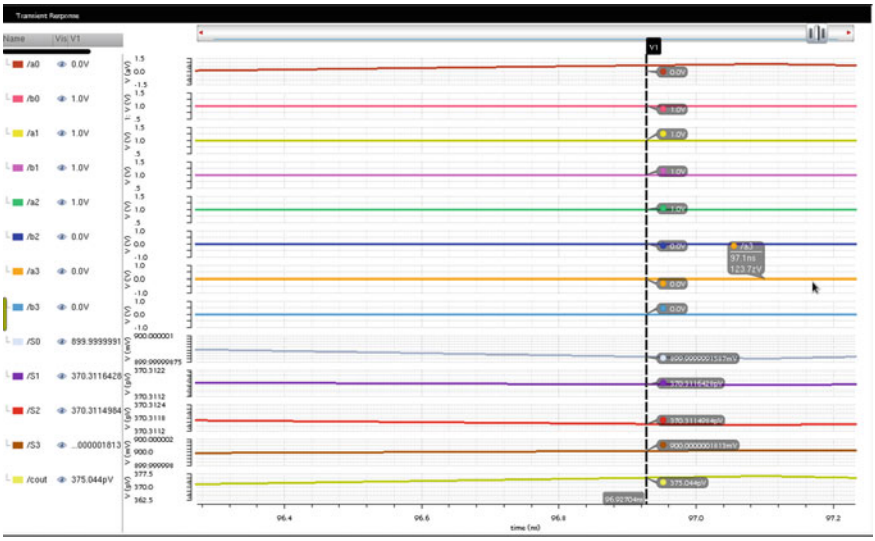

Fig. 6 Simulation result of 4-bit CSTA

Table 1 Power consumption and overall delay of different circuits

Circuit	Power (μw)	# Transistors	Delay (ns)
4-bit CSTA	24.4	222	16.04
4-bit CSTA with sum checker	62.07	236	22.4

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A Novel Adiabatic Logic for Low Power VLSI Circuit Design and Power Optimization Using FinFET

B. P. Bhuvana and V. S. Kanchana Bhaaskaran

Abstract In this article, a novel low power adiabatic circuit, namely the modified complementary pass transistor logic (MCPAL) powered by a four phase power clock supply, is proposed. The important features of the proposed logic are its low leakage power, glitch free output, and lower switching noise compared to the counterpart circuits found in the literature. Efficiency of the proposed adiabatic logic is validated by comparing with the basic inverter circuits designed using 2N2P, 2N-2N2P, PFAL, CPAL, and DCPAL type of adiabatic logic circuits. Secondly, the utilization of self-aligned double gate FinFETs in the design of MCPAL is also studied, with the use of an inverter and 512 stages of cascaded inverters implemented using 32 nm FinFET and 32 nm lower technology MOSFET by employing their corresponding BSIM model files. The circuits are designed and simulated in Cadence Virtuoso® tool environment through an operating frequency range from KHz to GHz.

Keywords Energy recovery circuits · Adiabatic circuits using FinFETs
Low power VLSI circuit design

1 Introduction

With unrelenting advancements in the electronics domain, the demand for compact devices which can operate using comparatively lower voltage values with reduced power dissipation increase. However, the high operating frequency requirements, the complex processing involved, and the continuous scaling of devices lead to increased leakage current, which in turn lead to increased power consumption.

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Many researchers focus on the optimization of power by realizing enhanced control over the gate structure with the required channel current of the MOS device, even while maintaining control over the leakage current.

Conventional CMOS circuits dissipate power in the pull-up and pull-down MOS devices during the charging and discharging operations related to the nodal capacitance. This leads toward increased power dissipation in CMOS circuits while operating at high frequencies. These disadvantages point toward a new contemporary logic called as "Adiabatic Logic" or "Energy Recovery Logic." This is accomplished by the recovery of a major portion of the energy that is expended in the nodal capacitances, and the energy so recovered is reused during the successive computations. Adiabatic logic design is categorized into two major divisions as follows: (1) Quasi-adiabatic logic circuit and (2) Fully adiabatic logic circuit. Some of the prevailing quasi-adiabatic logic circuits found in literatures are 2N2P [1], 2N-2N2P, Positive feedback adiabatic logic (PFAL) [2], Differential cascode pre-resolve adiabatic logic (DCPAL) [3], Pre-resolve and sense adiabatic logic (PSAL) [4], and Complementary pass-transistor logic (CPAL) [5].

Scaling of technology raises the leakage power dissipation. Some of the major causes of leakage power are mainly due to the sub-threshold leakage current that arises due to low threshold voltage and that due to the gate leakage current which occurs due to the thin gate-oxide material. To overcome the effect of such leakage current effects, several new devices have been suggested as an alternative to conventional MOSFFETs. Some of them are as follows: ultra-thin body devices, fully depleted silicon insulator (FDSOI), and fin-based field effect transistor (FinFET) [6].

The paper is organized as follows: Sect. 2 summarizes the operation of FinFET. Section 3 presents FinFET-based adiabatic logic circuit design. Section 4 depicts the proposed MCPAL adiabatic logic circuit. Section 5 presents the results and discussion. Section 6 concludes.

2 FinFETs

The structure of FinFET shown in Fig. 1 is derived from the folded channel MOSFET. It consists of a Fin designed using a silicon material, which acts as the body of the device. The source and drain terminals are arranged opposite to the fin in such way that it realizes efficient control over the channel, and it in reality effectively minimizes the short channel effects and leakage current, majorly felt in MOSFETs.

Various operating modes of the FinFET are as follows:

(1) Shorted Gate (SG) mode, where both the front and back gates are tied together and this mode exhibits high switching speed and better resistance to short channel effects.
(2) Reverse Bias (RB) mode, where one of the gates is kept reverse biased. Usually, the back gate is preferred as it has less V_{th} which can be varied. This approach is, however, slow and it delivers increased area overhead.

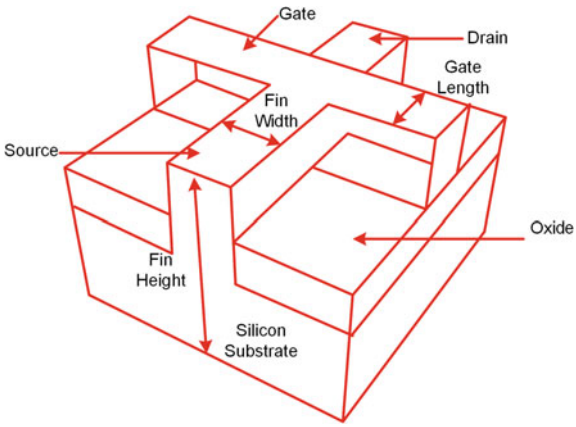

Fig. 1 Structure of FinFET

(3) Independent Gate (IG) mode, where both the gates operate individually. It consumes a lesser amount of area when compared with the other modes of operation.

3 Adiabatic Logic Circuits

Adiabatic logic circuits are capable of recovering a significant quantity of energy spent at the capacitive output nodes. Adiabatic logic circuits utilize the power clock (PC) sources as the energy source. Energy is supplied to the adiabatic logic circuits during the evaluation phase by the power clock signal and energy stored in the nodal capacitances is recovered back during the recovery phase. PC signals are so-called because they power up the adiabatic logic circuits and also these signals maintain the timing of adiabatic circuit stages [7]. The shape of PC enables operation of adiabatic circuits in four different phases, namely (1) Evaluation phase, where PC rises from 0 V to peak voltage, (2) Hold phase, when PC is constant for enabling next stage pipelining evaluates its input, (3) Recovery phase, when PC drops down from peak voltage to 0 V thus allowing charge recovery from output nodes back to PC, and (4) Wait phase, where PC is in 0 V level which aids in synchronization process across the stages.

Adiabatic logic circuits such as the 2N2P, 2N-2N2P, and PFAL operate with only one power clock signal whereas DCPAL and PSAL utilize two power clock signals with pre-resolving phase as its first phase followed by evaluation, hold and recovery phases. Each PC signal varies by 90°. This signal lags behind IN by 90°. A phase shift of 90° exists between input and output. This aids in cascading the pipelined stages. A 4-stage adiabatic inverter chain is shown in Fig. 2. Input, output, and PC waveforms are presented in Fig. 3. The 2N2P, 2N-2N2P, PFAL, DCPAL, and CPAL type of adiabatic circuits are shown in Fig. 4a–e, respectively.

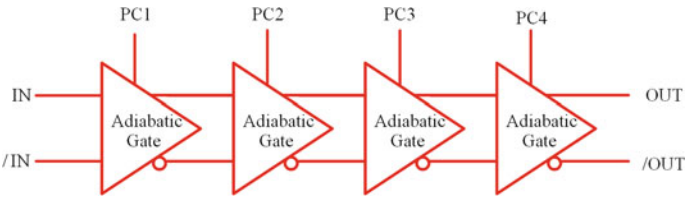

Fig. 2 Structure of a 4-stage cascaded adiabatic pipeline

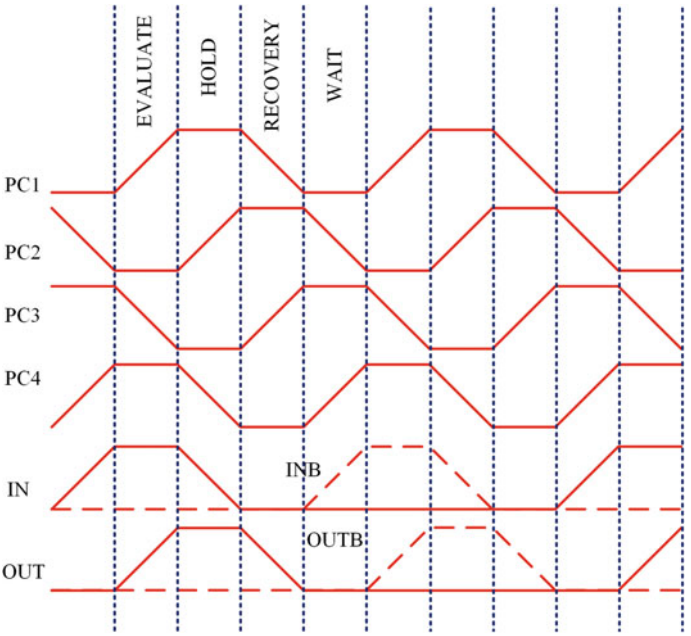

Fig. 3 Input–output, power clock transients

2N2P contains a latch formed by the cross-coupled pFinFET and nFinFET, whereas 2N-2N2P and PFAL consist of two latches formed by pFinFET and nFinFET. 2N2P suffers from the floating output node problem, when OUT node cannot find a recovery path to PC. This is eliminated in 2N-2N2P, due to the additional nFinFET present in pull-down network.

DCPAL consists of a pre-resolving phase, where it pre-resolves the input which is made to reflect on the corresponding output nodes. Also, it has a footer nFin device powered by PC3 [8]. PC3 leads PC1 by 180°. A similar conception has been used in PSAL. PSAL is very much similar to DCPAL, however, with the 2P latch replaced by 2N2P latch. The operational enhancement of PSAL is its capability to of operate at very low frequency. Leakage current in PSAL is very much reduced due to the presence of the stacking footer transistor. PFAL logic circuit has its

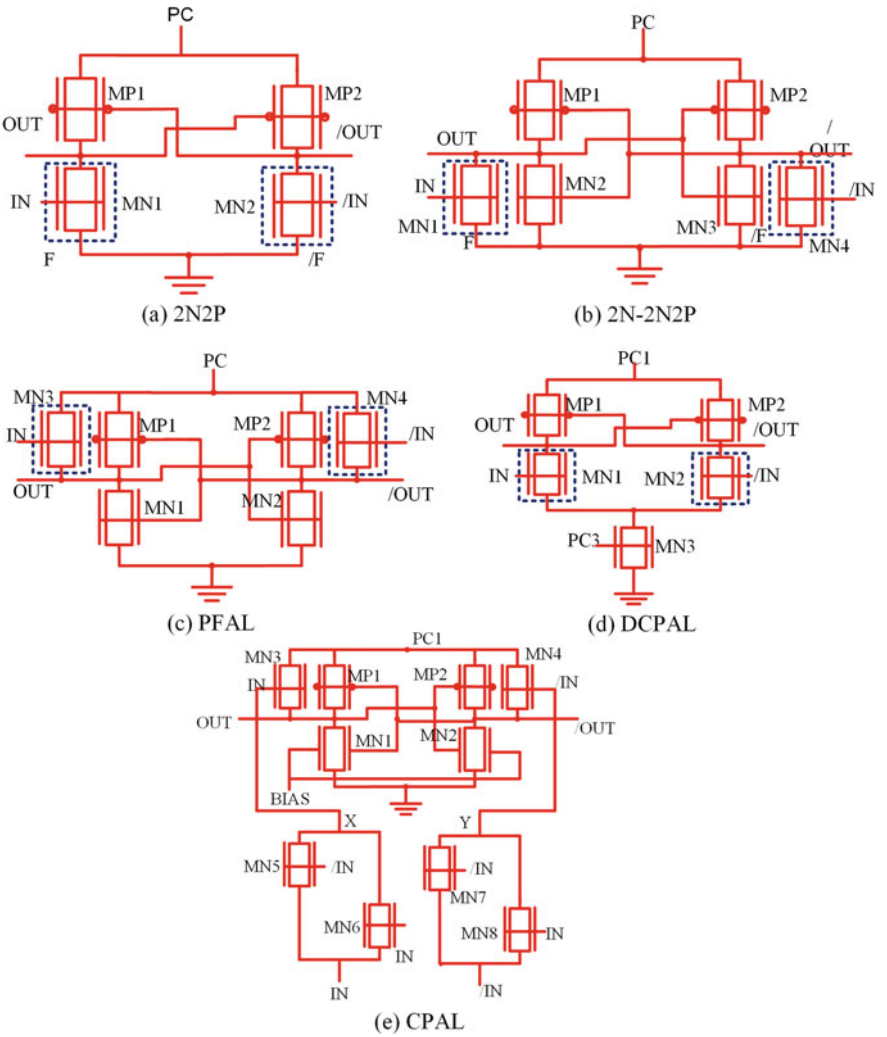

Fig. 4 Basic adiabatic logic circuit

functional block in the pull-up network. CPAL utilizes CPL (complementary pass-transistor logic) as its functional unit and consumes a smaller amount of power. To discuss its operation in brief, consider when PC ramps up in evaluation phase, IN is high. Then, node X is charged to higher level than V_{DD}-V_{th}, and OUT node is charged to V_{dd} and/OUT is pulled down to ground, and node Y is pulled down to ground. During recovery phase, PC ramps down and hence the charge in OUT node is recovered through MN3.

4 Proposed MCPAL Adiabatic Logic Circuit

This section presents the proposed MCPAL circuit, which employs complementary pass-transistor logic, which is efficient in reducing the leakage current from power supply to ground. If the common unit in the adiabatic logic circuit is designed well enough to reduce power, then the entire circuit operates in a state, where power is minimum when compared with its counterparts. The MCPAL is designed using 32 nm device operating in shorted gate mode. Major advantage of this method is the use of forced stack transistors to reduce the leakage current. MCPAL consists of a functional block formed by MN5, MN6, MN7, and MN8 shown in dotted blocks and load drive circuit formed by MN1-MN4 and MP1-MP2.

The Modified CPAL inverter of Fig. 5a with PC, input and output represented in Fig. 5b, operates as follows:

(i) Evaluation Phase: When the power clock rises from zero to peak voltage, depending upon IN and/IN either *X* or *Y* remains at HIGH voltage. Consider node *X* is stable at high voltage, which turns on MN1. MN3 and MN4 are

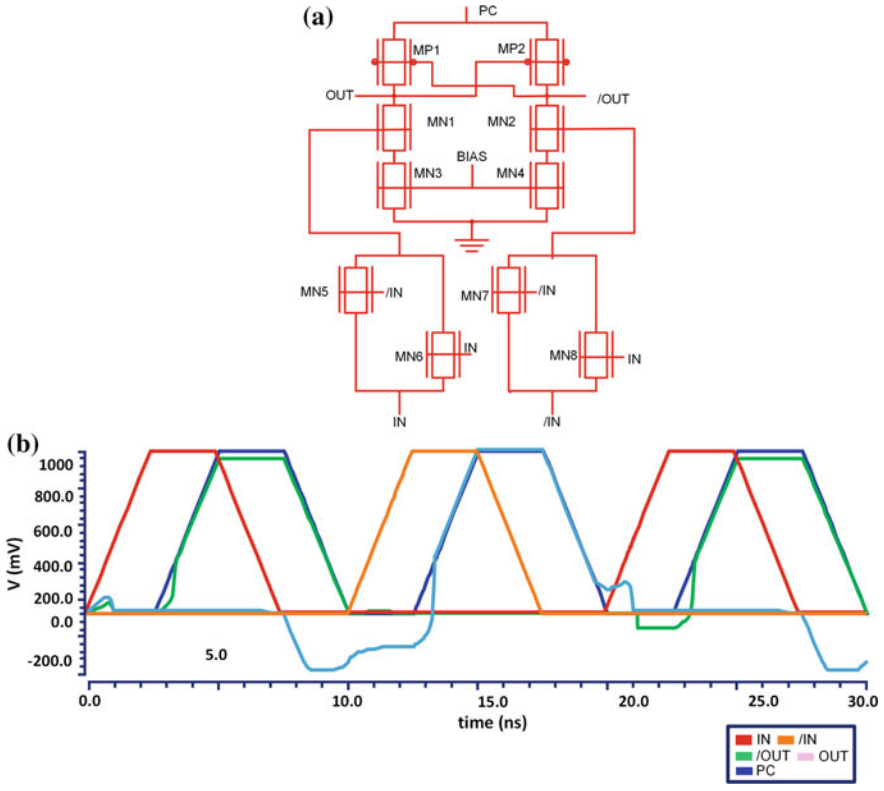

Fig. 5 **a** Proposed MCPAL inverter circuit, **b** proposed MCPAL input–output transients

biased by a high voltage and hence the OUT node is pulled down to ground. This low voltage switches ON MP2 and/OUT is pulled up to PC. Latch formations due to the cross-coupled pFin devices stabilize the outputs from the complementary pass-transistor logic. MN3 and MN4 act as stack transistors and their on/off state is similar to MN1 and MN2.

(ii) Hold phase: During this phase, PC is high which maintains the output state for evaluation by the next adiabatic stage and IN drops to 0 V. This in turn turns off MN1. Leakage current is reduced to a greater extent by the stack transistors MN3 and MN4.

(iii) Recovery phase: In this phase, when PC drops to zero, node *X* remains at zero and charge stored at the output nodal capacitances is recovered by PC through the pull-up network. Major benefit of the stacked transistor is that they recover the maximum possible charge from output nodes instead of expending it to the ground.

5 Results and Discussion

This section presents the results, and analyses are made for validating the efficiency of the proposed MCPAL. Figure 6 depicts the input–output transients along with energy recovery waveform of MCPAL-based inverter.

Figure 7 presents energy comparison of 2N2P, 2N-2N2P, PFAL, DCPAL, and CPAL inverters at 100 MHz, incurring energy of 25.55 aJ, 26.90 aJ, 37.88 aJ, 43.10 aJ, 128.0 fJ, respectively. It can be observed that MCPAL incurs 24.28 aJ, which is very less when compared with all its counterparts. Table 1 depicts the power and energy dissipation comparison among the logic families considered. The energy spent by the 2N2P, 2N-2N2P, PFAL, DCPAL, and CPAL are 657.9 aJ, 461.3 aJ, 500.8 aJ, 773.1 aJ and 718.2 aJ, respectively, at 500 MHz, with MCPAL incurring only 243.5 aJ. Figure 8a, b shows performance comparison of MCPAL inverter designed using CMOS and FinFET operating at 1 V and 500 MHz frequency.

Table 2 shows comparative energy levels of the adiabatic logic families across the frequency range. This is graphically represented in Fig. 9. It is apparent that MCPAL consumes very less energy when compared with other adiabatic logic families. Table 3 depicts the energy dissipation incurred by adiabatic logic families with 512 cascaded inverter stages operating at 500 MHz and 1 V. From the results, it is clear that MCPAL utilizes 2.44fJ which is too less when compared against other adiabatic logic families.

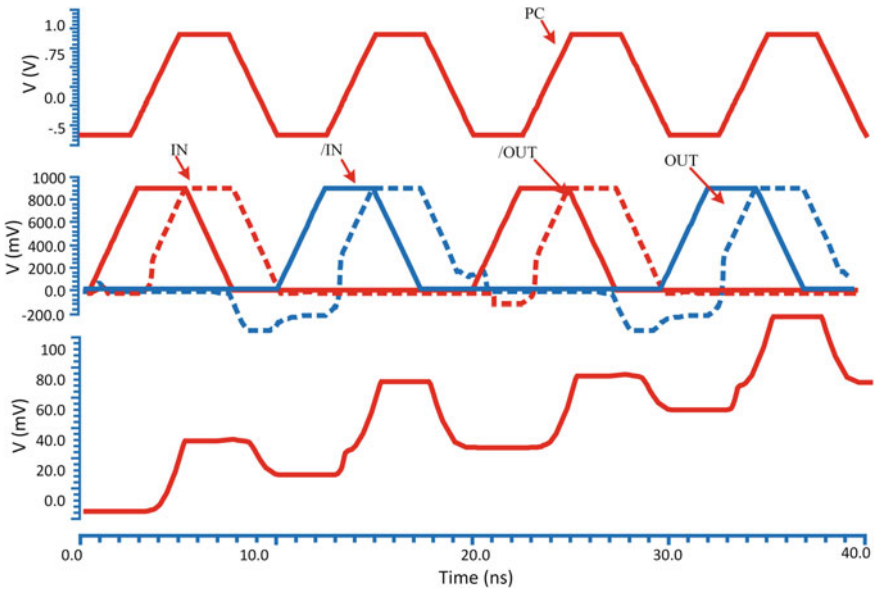

Fig. 6 Input–output transients of proposed MCPAL

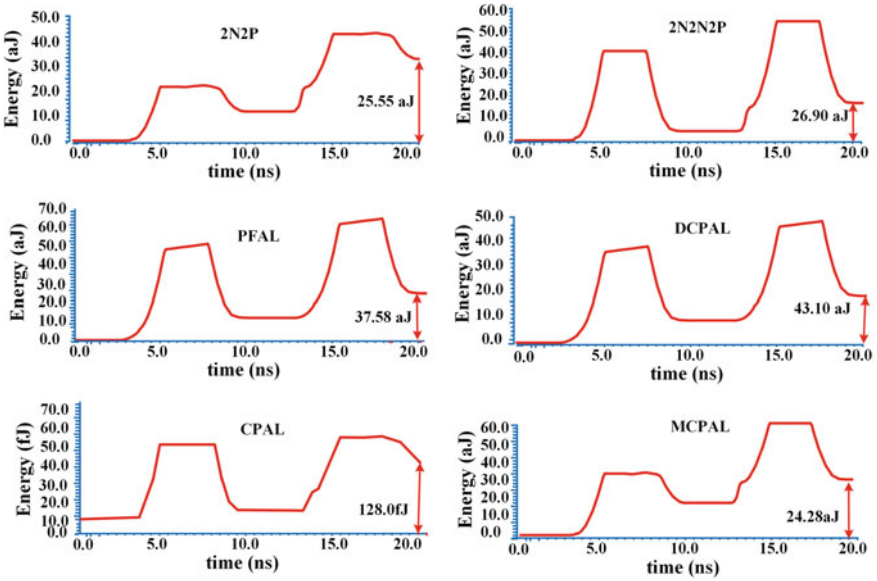

Fig. 7 Energy comparison of buffers at 100 MHz frequency

Table 1 Power and energy dissipation comparison of the adiabatic logic families

Adiabatic logic family	Power (nW)	Energy (aJ)
2N2P	13.09	657.9
2N-2N2P	8.846	461.3
PFAL	9.630	500.8
DCPAL	15.70	773.1
CPAL	14.73	718.2
MCPAL	4.729	243.5

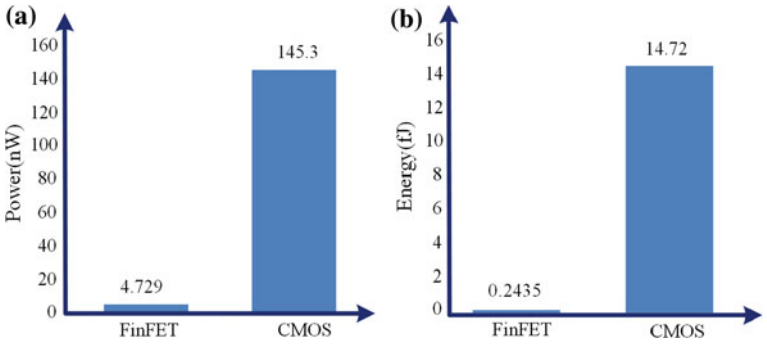

Fig. 8 **a** Power comparison of MCPAL inverters using FinFET and CMOS, **b** energy comparison of MCPAL inverters using FinFET and CMOS

Table 2 Energy dissipation of various adiabatic logic families across a range of frequency

Frequency	Energy dissipation (aJ)					
	2N2P	2N-2N2P	PFAL	DCPAL	CPAL	MCPAL
100 kHz	55.06	48.12	54.65	78.07	69.37	22.10
100 MHz	118.2	99.01	105.3	117.9	109.7	48.15
500 MHz	657.9	461.3	500.8	773.1	718.2	243.5
1 GHz	1302.4	927.4	1007.7	1002.3	1006.7	452.9

Fig. 9 Frequency versus energy for FinFET-based adiabatic logic inverter circuits

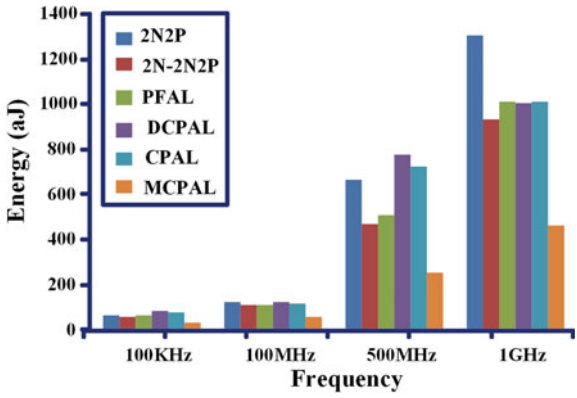

Table 3 Energy dissipation of 512 cascaded inverters designed using various adiabatic logic families

Adiabatic logic family	Energy (J)
2N2P	1.12E−14
2N-2N2P	3.77E−14
PFAL	1.38E−13
DCPAL	3.24E−14
CPAL	7.32E−13
MCPAL	2.44E−15

6 Conclusion

In this paper, the FinFET-based MCPAL adiabatic logic circuit is presented. The logic is capable of operating at a wide range of frequency from KHz to MHz. Validation of the proposed logic is carried out by comparing an inverter designed using MCPAL with 2 N2P, 2 N-2N2P, PFAL, DCPAL, and CPAL inverter circuits designed using both MOSFET and FinFET. The FinFET-based MCPAL circuit dissipates 62, 47, 51, 68, and 66% lower than 2N2P, 2N-2N2P, PFAL, DCPAL, and CPAL, respectively. Furthermore, the MCPAL realizes lower power dissipation and incurs lower energy due to lower leakage current and improved charge recovery capability.

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Test Signal Generation for Detecting Faults on Mil-Std 1553 Bus

Sowmya Madhavan and S. Sandya

Abstract Military standard 1553 is a standard data bus which is widely used in various Avionics and Aerospace systems. Mil-std 1553 bus is used to communicate between different remote terminals and bus controllers which can be placed in different sub-systems of an aerial vehicle [1]. Faults like OPENS or SHORTS can occur on the cable because of various reasons, and detecting such faults is very critical in real-time systems. There are several methods like *Time Domain, Frequency Domain, Multiple Carrier, Noise Domain, Sequence Time Domain, and Spread Spectrum Time Domain Reflectometries* to detect the faults, and spread spectrum time domain reflectometry (SSTDR) is found as the best method for real-time fault detection for a maximum distance of 23 m with a precision of a few centimeters. Hence, by inserting multiple SSTDR chip sets, complete length of the cable can be tested for its faults. The ASIC solution includes the generation of test signal and detection of faults. In this paper, the authors present a test signal generation model to detect the faults when the system is on the fly.

Keywords Mil-STD · Spread spectrum · Reflectometry · Faults
Binary phase shift signal · Spread spectrum time domain reflectometry
ASIC

1 Introduction

Mil-std is a military standard data bus, particularly used to provide highly reliable and secure data transfer between different terminals of an avionics vehicle. The architecture consists of two differential signal lines connected to different remote

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terminals and a single bus controller. The maximum number of remote terminals connected to the bus can be 31. The major function of any remote terminal is to perform the data transfer inside the sub-system.

Mil-std 1553 data bus is actually a twisted shielded pair cable, having 30.0 pF/feet wire to wire capacitance, characteristic impedance of 70–85 Ω at 1 MHz, cable attenuation of 1.5 dB/100 feet, four twists per feet minimum, and terminated by a termination resistor or load impedance, which will be same as the characteristic impedance. The physical voltage levels are 6–9 V peak to peak.

In normal conditions, the characteristic impedance Z_0 of the cable will be equal to the load impedance Z_L. In this case, the incident signal will reach the end of the cable without any reflections. But, if there are some faults like 'Opens' or 'Shorts,' there will be an impedance mismatch and the incident signal will travel in the opposite direction as a reflected wave. Electrical shorts result in high rate of current and generation of heat, which can cause sparks or a fire in the system where the cable is used. Electrical open will result in high resistance, may be infinity. Since the Mil-std 1553 buses are connected to different sub-systems, any fault on the bus can lead to non-transmission of the signal and failure of the entire system also. One of the best examples for this is the failure of the launch of STS-93 space shuttle, in which, a short was detected in the controller of the engine. The reason for this electrical short was the damage of the insulation, after getting rubbed against a screw head. This kind of a problem has become an increasing problem in aging aircrafts.

Opens or Shorts, which are the major faults in cables, occur because of two main reasons: dry arcs and wet arcs. Dry arcs occur because of vibration and may cause cracks in the cable, which causes opens in the cable. Wet arcs mainly occur because of moisture build-up, and this moisture may penetrate the cable and form a conductive path to other cables, which causes short in the cable. All these faults are intermittent in nature, that is, they do not occur always. In case of aircraft systems, these faults may occur when the aircraft is in flight. So it becomes very important to monitor and detect these faults well before they damage the system.

Mil-std 1553 supports a data rate of 1 MHz. The data could be any information for monitoring the aircraft environment, alert signals, or any other data which are sent from one Electronic Control Unit (ECU) to other.

2 Reflectometry Methods

Reflectometry methods are the standard methods for locating faults. The principle behind reflectometry methods is that an incident signal is sent on the cable which needs to be tested and the cable is observed for any reflections. If there are no impedance discontinuities on the cable, there will be no reflection and it is a 'no fault' condition. In this case, the cable is said to be normal. But, if there are 'opens' or 'shorts' in the cable, the characteristic impedance of the cable changes which causes the incident signal to reflect at impedance discontinuities. In this case, the incident signal will not reach the end of the cable. In order to locate the fault on the cable, the

time delay T_d, which is the time elapsed between the onset of the incident signal on the cable and the time at which the reflected signal is received, is measured.

There are different types of reflectometry methods, namely Time Domain, Frequency Domain, Multiple Carrier, Noise Domain, Sequence Time Domain, and Spread Spectrum Time Domain Reflectometries to detect the faults [1].

Time Domain Reflectometry can be performed by transmitting a voltage step signal on the cable and measuring the reflection. FDR sends a set of stepped frequency sine waves across the cable length which can reach the cable end. Any high noise already on the cable can be used to test the cable passively by NDR. MCR uses multi-frequency test signals [2–5].

The disadvantages of TDR, FDR, and NDR are they are effective only for short distances; directional couplers are needed for separating the incident wave from the reflected wave and implementation requires a large amount of memory [6, 7]. STDR sends a chain of pulses as an incident test signal. But the main disadvantage of STDR is that it cannot be used for cables carrying digital data [8]. SSTDR sends a modulated signal by multiplying the sine wave with a PN sequence. Out of all the reflectometry methods, through literature survey, we have found that, SSTDR is the best method because it is particularly effective at testing wires carrying digital data, and it gives higher accuracy in fault detection up to a few inches [9–11]. In SSTDR, the test signal is of higher frequency (30 MHz) than the frequency of the actual data (1 MHz), and this keeps the low-frequency region clean. Also, the bit error rate (BER) is reduced in SSTDR. The BER is about 10^{-12}. Lower the bit error rate, higher will be the chances of the actual data not getting corrupted and also not interfering with the test signal.

The SSTDR implementation block diagram is as shown in Fig. 1 [12–15].

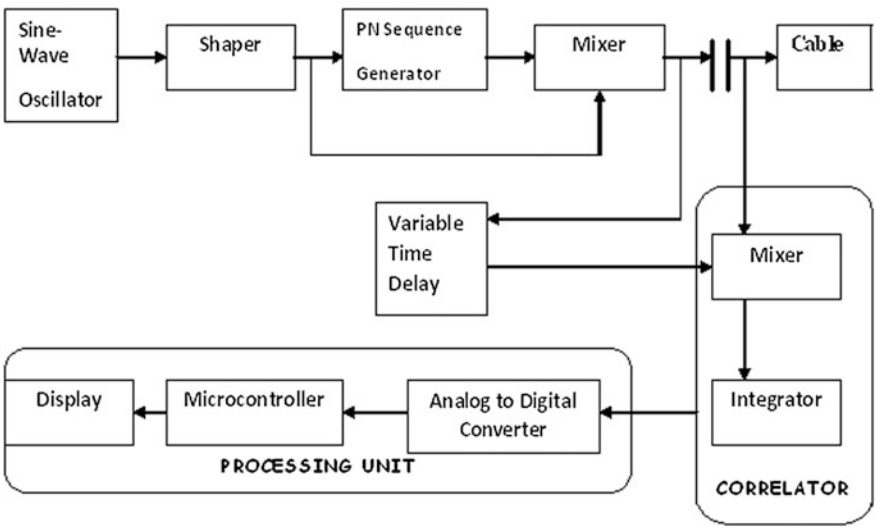

Fig. 1 System-level block diagram

The sine-wave oscillator produces a sine wave of a particular frequency. The shaper block smoothens any irregularities in the sine wave. The PN sequence generator generates a pseudo-random sequence with a known duty cycle. The mixer modulates the signal from the shaper according to the bit transitions in the PN sequence. The output of the mixer is a binary phase shift keyed (BPSK) signal [16–19]. This BPSK signal serves as the test signal which will propagate on the Mil-std 1553 bus. The same test signal is delayed by a known time delay. Any reflected signal from the cable and the signal which is time delayed are fed to the correlator unit, which will give the peak values w.r.t. the correlation amplitude [20, 21]. These values will be sent to a processing unit which will exactly calculate the location of the fault by doing mathematical correlation.

3 Simulation and Results

Simulations in MATLAB were carried out to model a general cable. The length of insertion of fault was given as 10 meters. It was simulated for two cases: OPEN and SHORT.

In order to know the location of the fault, we have to observe the *X*-axis value of the highest peak after the origin. For locating an open, there will be significant positive peaks as marked in Fig. 2, and for locating a short, there will be significant negative peaks as marked in Fig. 3.

Simulations were carried out for the sine-wave oscillator, shaper, PN sequence generator, and mixer blocks for Mil-std specifications in Cadence and Xilinx. All the simulation results are shown below.

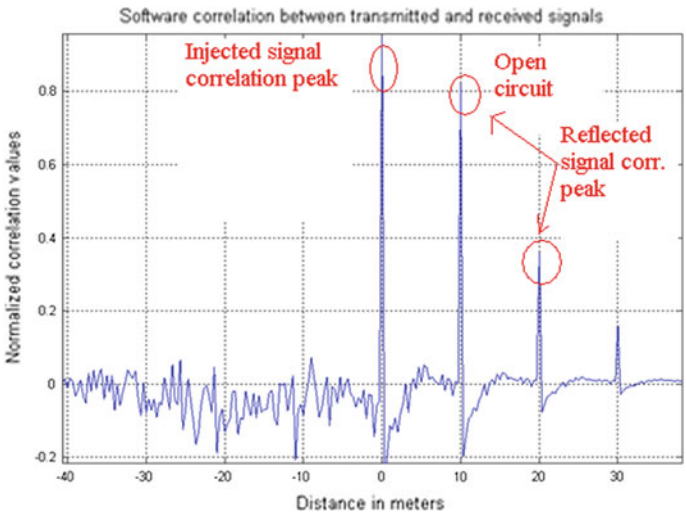

Fig. 2 MATLAB simulation for a OPEN at 10 m

Fig. 3 MATLAB simulation for a SHORT at 10 m

Figure 4 shows the output of the sine-wave oscillator. The frequency of the oscillations is 30 MHz. Thirty MHz is chosen since the data rate on Mil-std 1553 bus is 1 MHz, and there will be no interference between the actual data and the test signal.

Figure 5 shows the output of shaper block.

Figure 6 shows the output of PN sequence generator. The initial seed value is taken as decimal 1234.

Figure 7 shows the output of mixer. The inputs to the mixer are the sine wave generated and the PN sequence generated. The output is a binary phase shift keyed (BPSK) signal. Whenever there is a transition from high to low or low to high, there is a change of phase for the BPSK signal. The frequency of the BPSK signal which is the test signal is 30 MHz.

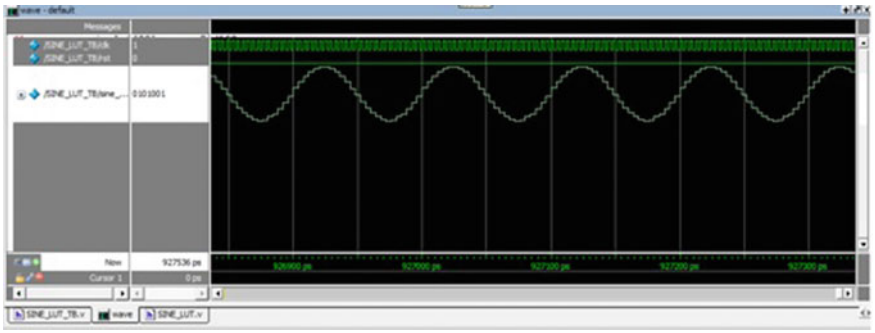

Fig. 4 Output of sine-wave oscillator

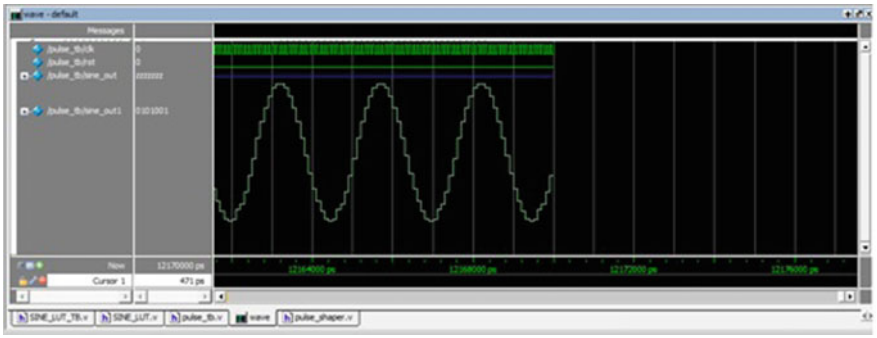

Fig. 5 Output of shaper

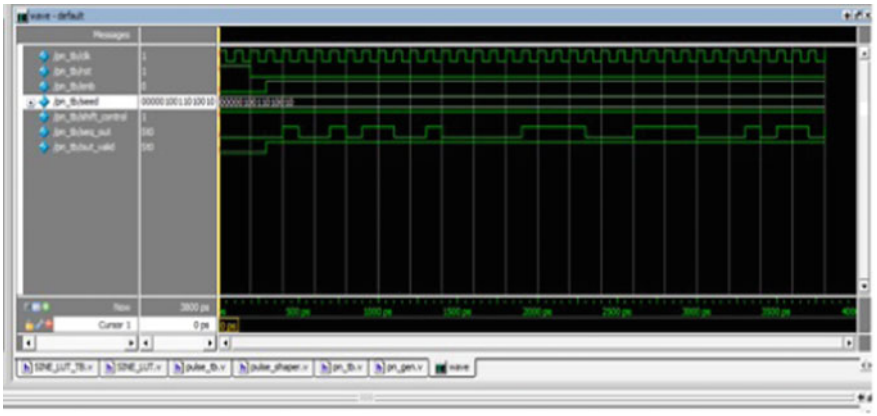

Fig. 6 PN sequence output

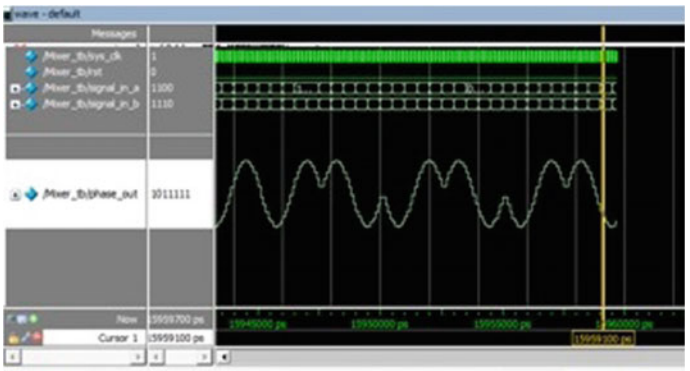

Fig. 7 Output of mixer

4 Conclusion

A fault detection model was developed in MATLAB for general cables. In the model, manually the faults can be inserted at any length, and the model is able to give accurate results as expected. This MATLAB model is very helpful in characterizing the cable and also serves as a virtual cable for implementing the entire system in Xilinx or Cadence. A test signal generation model was also developed in the paper. To validate the test signal generation model, simulations were carried out in Cadence and Xilinx. Simulations in Cadence were carried out at the transistor level. Xilinx simulations followed top-down approach, where the entire system is divided into different modules. The simulations are module-wise. The test signal chosen to be generated is a binary phase shifted signal (BPSK) of frequency 30 MHz. The first simulation presented in the paper is the generation of the carrier wave of frequency 30 MHz. This block is called as the sine-wave oscillator. The next block is the shaper which smoothens the sine wave. Then, a pseudo-noise (PN) sequence is generated. The PN sequence and sine wave form are the inputs to the mixer module, which generates the BPSK signal, which is also called as the SSTDR test signal. Modulation also increases the bandwidth of the test signal. This test signal is supposed to be sent on the Mil-std 1553 cable in developing a prototype for real-time fault detection system. The proposed system solution is also used to provide an ASIC solution for real-time fault detection system.

5 Future Scope

The results of the MATLAB model presented in this paper are for a general cable, and the same can be realized for Mil-std 1553 by adding all the given characteristics of Mil-std 1553. Work will be continued by adding these components. The same system can be realized as a prototype solution on FPGA with some minor modifications. The system-level block diagram can also be realized as an ASIC/CMOS solution for real-time fault detection. The final level would be bringing out a product using the ASIC developed.

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Design of Ultra-Low-Voltage Energy Efficient Hybrid Full Adder Circuit

M. Mahaboob Basha, K. Venkata Ramanaiah and P. Ramana Reddy

Abstract In recent years, ultra-low-voltage (ULV) operation is gaining more importance to achieve minimum energy consumption. This chapter aims at minimizing the energy consumption of the full adder circuits in the near threshold region of operation. A new hybrid full adder circuit which employs CMOS logic and transmission gate (TG) logic with dynamic threshold MOS (DTMOS) scheme is presented. The DTMOS is one of the body bias schemes used to improve the performance in ULV operation by dynamically varying the threshold voltage of the transistors. The performance metrics—energy, power, delay and EDP are calculated and compared with the conventional CMOS full adder. The simulations are performed using Cadence 90 nm technology with ultra-low-voltage of 0.2 V (sub-threshold region). The results have shown that the proposed hybrid full adder circuit with DTMOS scheme achieves more than 26% savings in delay, 15% savings in energy consumption and 38% savings in EDP in comparison with the static CMOS configuration.

Keywords CMOS · DTMOS · Energy consumption · Transmission gate ULV operation

1 Introduction

With the technology advancements and increasing demand for portable battery-operated applications such as mobile phones, laptops and energy-constrained applications like micro-sensor networks, the energy consumption of

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the digital circuits is becoming more critical [1]. It has been shown that power dissipation is directly reduced with supply voltage scaling, and the operation of digital circuits in the subthreshold region (supply voltage—V_{DD} less than the transistor threshold voltage—V_T) is considered as a most efficient solution to achieve ultra-low-power (ULP) consumption with acceptable performance [2]. The subthreshold current of the MOS transistor is given by Eq. (1) [1].

$$I_{sub} = I_0 e^{(V_{GS}-V_T)/nV_{th}} \tag{1}$$

and

$$I_0 = \mu_0 C_{ox} \frac{W}{L}(n-1)V_{th}^2 \tag{2}$$

where

V_T	threshold voltage
V_{th}	thermal voltage (KT/q)
V_{GS}	gate to source voltage
n	subthreshold slope factor ($1 + C_{dep}/C_{ox}$)
W	effective channel width
L	length of the channel
μ_0	zero bias mobility
C_{dep}	depletion capacitance
C_{ox}	oxide capacitance

Arithmetic operations play a key role in many of the VLSI applications. Addition, subtraction, multiplication and accumulation are the most commonly used arithmetic operations, where 1-bit full adder is the basic building block for all these implementations. Therefore, enhancing the 1-bit full adder cell performance is necessary to enhance the overall system performance.

This study presents a new hybrid full adder circuit designed to operate in subthreshold regime for energy efficient arithmetic applications. The rest of this chapter is organized as follows. Section 2 gives the design methodology of the proposed full adder circuit. Section 3 presents the simulation results and comparative discussions and finally, some conclusions are made in Sect. 4.

2 Proposed Hybrid Design

The proposed hybrid full adder circuit is designed by employing static CMOS logic [3] and transmission gate (TG) logic [4] with dynamic threshold (DTMOS) scheme [5] as shown in Fig. 1. The structure of the design is similar to the hybrid full adder (Hybrid-FA) proposed in [6]. It consists of two identical XNOR logic gates and transmission gates to generate the output sum and output carry (C_{out}), respectively.

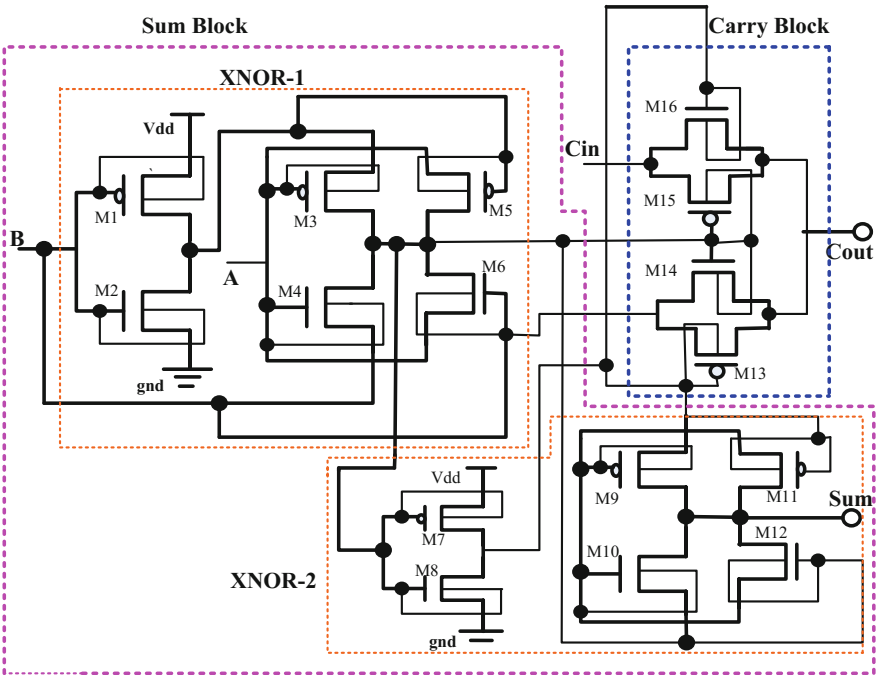

Fig. 1 Proposed subthreshold hybrid full adder circuit

As the sum block is most responsible for power consumption, the XNOR block is designed to ensure full output swing using swing restoring transistors (M_5 and M_6) and minimum transistor count which reduces the power consumption of the circuit. Use of transmission gates for generation of C_{out} ensures full logic swing. Since the carry input (C_{in}) propagates only through a single transmission gate (M_{15} and M_{16}), the propagation delay is reduced.

To further improve the energy efficiency of the hybrid adder design while operating in subthreshold region, DTMOS scheme (the transistor body terminal is tied to the gate input) is incorporated. DTMOS scheme is the ultra-low-voltage, area efficient body biasing scheme where the threshold voltage (V_T) of the device is dynamically varied with respect to the change in the gate voltage. The basic equation which models the impact of body bias on the threshold voltage is given as [7]

$$V_T = V_{T0} + \gamma(\sqrt{2\phi_B - V_{SB}} - \sqrt{2\phi_B}) \tag{3}$$

The parameter γ is the body effect coefficient, ϕ_B is the flat band voltage, V_{SB} is the source to the body bias voltage and V_{T0} is the threshold voltage with zero substrate/body bias. From Eq. (3), it is understood that by employing the DTMOS scheme there will be a reduction in the leakage (when $V_G = V_B = 0$; V_T is high) and improvement in the speed (when $V_G = V_B = 1$; V_T is low).

3 Results and Comparative Discussion

The proposed hybrid full adder circuit is simulated and the results are compared with conventional CMOS (C-CMOS) and dynamic threshold CMOS (DT-CMOS) full adder designs. All the simulations are performed using Cadence 90 nm technology with a supply voltage of 200 mV and operation frequency of 20 kHz. The comparison of the performance metrics—power, delay, energy and EDP—obtained from the simulations are shown in Table 1. From the comparisons, it is clear that the proposed design consumes less energy and EDP than the other designs.

The layout of the proposed design is shown in Fig. 2. The area of the design is found to be 28.7 μm^2 which is extremely low in comparison with the C-CMOS (30.8 μm^2) and DT-CMOS (34.6 μm^2) [with only 11% more than the Hybrid FA (25.84 μm^2) [6].

Table 1 Comparison of performance metrics for different full adder circuits

Design	Average power (pW)	Delay (ns)	Energy (aJ)	EDP (yJs)
C-CMOS	943.4	50.9	48.019	2.44
DT-CMOS	1023.4	43.22	42.379	1.827
Hybrid FA	1018.2	42.23	42.99	1.811
Proposed	1094.3	37.175	40.683	1.512

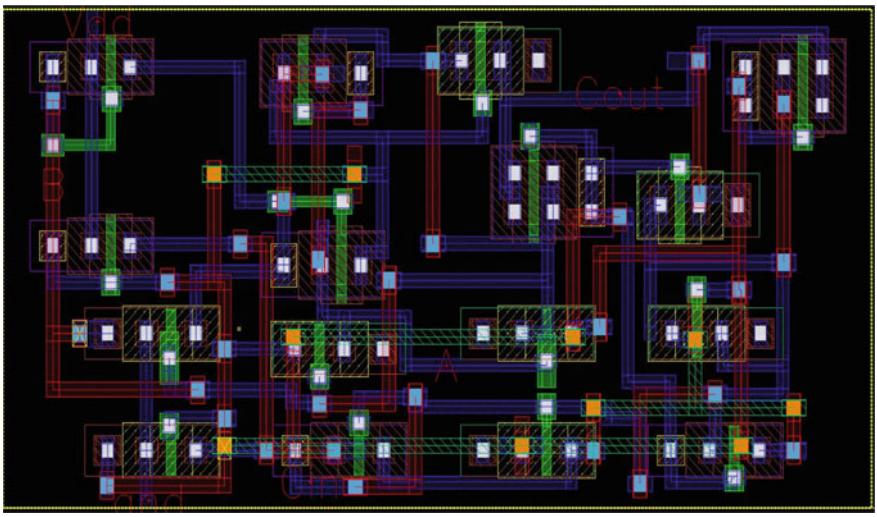

Fig. 2 Layout design of the proposed subthreshold hybrid full adder circuit

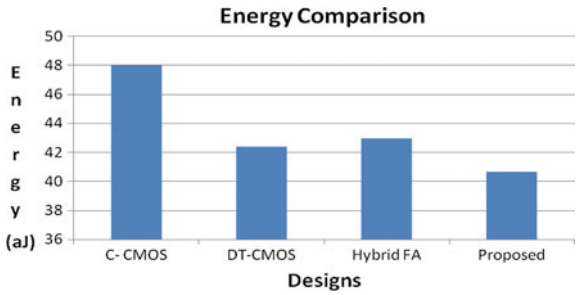

Fig. 3 Energy metric comparisons of different subthreshold full adders

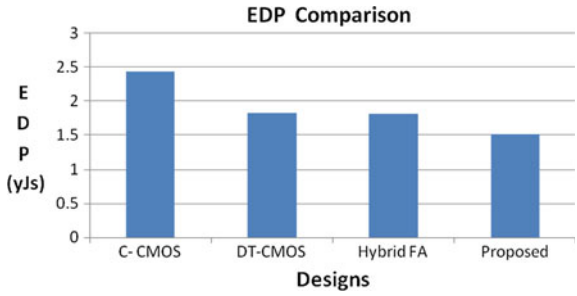

Fig. 4 EDP metric comparisons of different subthreshold full adders

The PDP and EDP comparison plots for different full adders are shown in Figs. 3 and 4, respectively. It is noticed that the proposed design achieved significant savings in terms of PDP and EDP and is more than 5 and 16% savings than the Hybrid FA, 4 and 16% savings than the DT-CMOS, 15 and 38% savings than the C-CMOS, respectively. These savings are achieved because of the less carry propagation path and the incorporation of DTMOS scheme in the proposed circuit which reduces the overall propagation delay.

4 Conclusion

In this chapter, a new hybrid full adder circuit which employs CMOS logic and transmission gate (TG) logic with dynamic threshold MOS (DTMOS) scheme is designed to operate in subthreshold regime for achieving minimum energy consumption. The simulations of the circuits have done using Cadence 90 nm technology with supply voltage of 0.2 V. The obtained simulation results have shown that the proposed design outperforms the other designs (C-CMOS, DT-CMOS and Hybrid-FA) by achieving more than 15% delay savings, 4% energy savings and 16% EDP savings with only 28.7 μm^2 of area utilization.

Hence, the proposed full adder circuit can be used as one of the substitute for many subthreshold adders designed for area and energy efficient arithmetic applications.

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A Novel MTCMOS-Based On-Chip Soft-Start Circuit for Low Leakage LED Driver with Minimum In-Rush Current

P. Magesh Kannan and G. Nagarajan

Abstract Multi-threshold complementary metal-oxide semiconductor (MTCMOS)-based on-chip soft-start circuit for low leakage LED driver with minimum in-rush current is proposed in this paper. During the start-up time of the LED driver, more in-rush current flows to the LED lights which can cause more stress and to the LED. The prolonged stress due to the in-rush current may reduce the life span of the LEDs. Hence, it is mandatory to minimize the in-rush current during the start-up time of the LED driver. The proposed method is validated through the simulations carried out in Cadence Virtuoso Analog Design Environment. The proposed circuits have been designed and implemented in CMOS 180-nm generic process design kit (GPDK). The proposed MTCMOS-based soft-start circuit reduces the in-rush current during the start-up time and minimizes the leakage power during the standby mode of the LED driver. The proposed scheme minimizes the in-rush current, and hence, the life span of the LEDs is improved; moreover, the battery backup time is also enhanced due to minimization of the leakage power. The proposed system outperforms well in terms of minimum in-rush current and low leakage current compared to the conventional LED driver. The conventional LED driver has 3.801 μA leakage current, whereas the proposed LED driver has a leakage current of 37.51 nA during 10% duty cycle for the same simulation setup.

Keywords In-rush current · Leakage power · LED driver · Low power MTCMOS · On-chip · Soft-start circuit

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1 Introduction

The existing lighting solutions like high-intensity discharge (HID) lamps and compact fluorescent light (CFL) are consuming more power and dissipate lot of heat and thereby cause global warming. Moreover, the life span of the HID and CFL is very short. LED lighting is the emerging lighting solution which consumes very less power, does not dissipate much heat, and is environment-friendly also. Due to the small size and longer life at an affordable cost, LED lighting replaced almost all other types of lighting solutions. As the LEDs are energy saving in nature, they are used in various applications like headlight and taillight in vehicles, ambient lights to create a specific mood in hotels, traffic light signals, smart street lights [1–5].

The LEDs controlled by the conventional LED driver suffer due to high in-rush current during the start-up time of the LED driver. The prolonged stress due to the heavy in-rush current will cause stress to the LEDs hence the LEDs will be damaged permanently. In addition to that, the leakage power during the minimum duty cycle or energy saving mode becomes more since the power MOSFET in the DC–DC converter goes to cut-off state for longer duration. The duty cycle of the LED drivers which are used for displaying backlight applications is kept minimum to reduce the brightness of the display as well as to extend the battery backup. More amount of power is wasted as leakage power during this scenario. Hence, it is mandatory to minimize the in-rush current during start-up and the leakage power during minimum duty cycle.

2 Related Work

An AC coupled feedback-based new alternative method to achieve fast transient response while managing the in-rush current during DC–DC converter start-up was discussed [6]. The in-rush current can be minimized by applying power gating which had been demonstrated in this paper [7]. Boost LED drivers use adaptive soft-start technique, and the in-rush current is minimized by varying the start-up time as discussed [8]. A soft-start circuit for the high power supply using pulse step modulation technique had been described [9]. A soft-start circuit which uses pulse-skipping method minimizes the in-rush current, and the overshoot in the output was described [10].

A digitally controlled soft-start circuit operating in the optimal soft-start operation and adaptive to the load was described [11]. Soft-start-based pulse current method to minimize the in-rush current had been discussed [12]. Soft-start circuit using ramp signal with compact clamp circuit and soft recovery-based buck converter was described [13]. Positive slacks of dependent path-based leakage power minimization for system-on-chip were discussed. In place, optimization of leakage was applied to minimize leakage current [14]. A sleep transistor sizing-based power gating for leakage power minimization had been discussed [15].

The circuit diagram of the conventional LED driver is depicted in Fig. 1. The power MOSET is controlled by the pulse width modulation (PWM) pulses. The load current of the DC–DC converter can be controlled by varying the duty ratio of the PWM pulses.

3 Proposed Work

A novel MTCMOS-based on-chip soft-start circuit for low leakage LED driver has been implemented in this pap. The proposed circuit minimizes leakage power during minimum duty cycle and minimizes the in-rush current during start-up of the LED driver. The proposed system outperforms well in terms of leakage current and in-rush current. The schematic diagram of the proposed LED driver is depicted in Fig. 2.

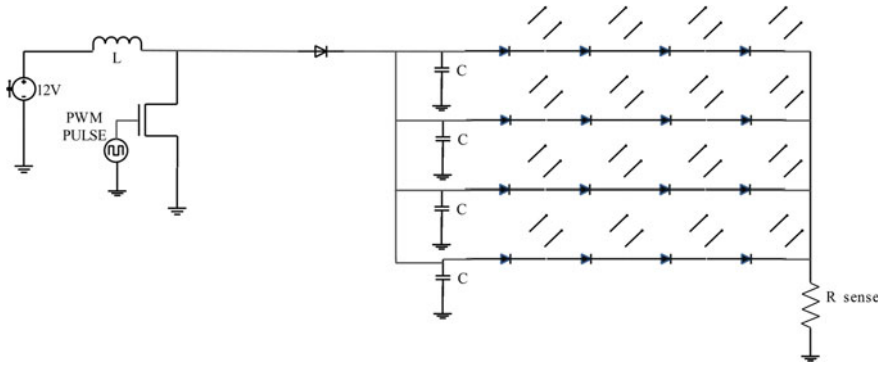


Fig. 1 Schematic diagram of the conventional LED driver

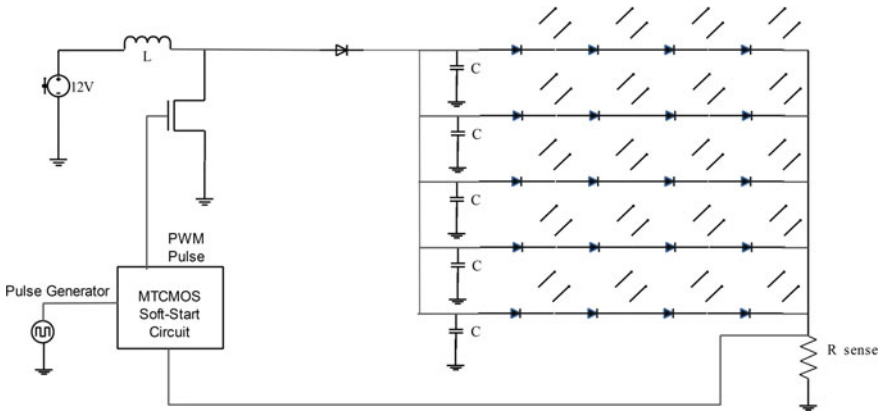


Fig. 2 Schematic diagram of the proposed LED driver

4 Simulation Results

Simulations of the conventional and proposed circuits were carried out in 180-nm CMOS process using Cadence Virtuoso Analog Design Environment. The PWM pulses of the conventional LED driver have very less rise time and fall time which is the reason for maximum in-rush current during the start-up, whereas the rise time and fall time of the PWM pulses in the proposed LED driver are increased by the MTCMOS-based on-chip soft-start circuit to minimize the in-rush current. Both PWM pulses of the conventional and the proposed LED driver are depicted in Fig. 3.

The maximum output current of both the conventional and proposed DC–DC converters with respect to the PWM amplitude is depicted in Fig. 4.

The impact of temperature on the maximum output current of both the conventional and proposed LED drivers was plotted in Fig. 5. The temperature has greater impact on the conventional circuit, whereas it has less impact on the proposed circuit.

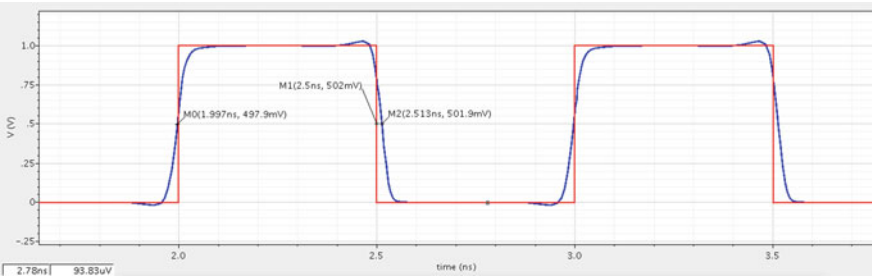
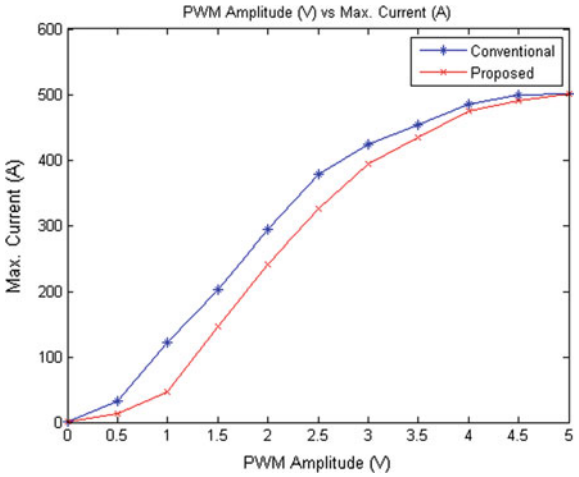


Fig. 3 PWM pulses of conventional and proposed LED drivers

Fig. 4 Load current of the proposed and conventional LED drivers with respect to PWM amplitude



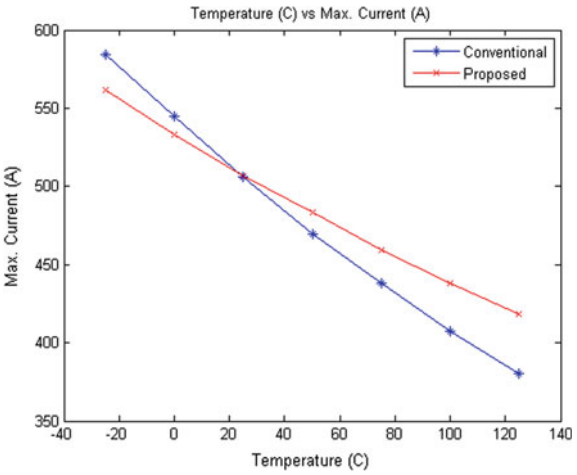


Fig. 5 Impact of temperature on the load current of the proposed and conventional LED drivers

The impact of temperature on the dynamic power consumption of the conventional and modified LED drivers is depicted in Fig. 6. The temperature has greater impact on the dynamic power of the conventional circuit, whereas it has less impact on the dynamic power of the proposed circuit.

The impact of temperature on the leakage power of the conventional and proposed LED drivers is drawn in Fig. 7. The conventional LED driver suffers from a large amount of leakage current in terms of microamperes, and the temperature has the severe effect on the leakage current, whereas the leakage current is minimum in term of nanoamperes for proposed LED driver.

Hence, the proposed LED driver outperforms well in terms of minimum leakage current, and thereby, the backup time of battery can be greatly improved which will be very much useful for battery-operated devices.

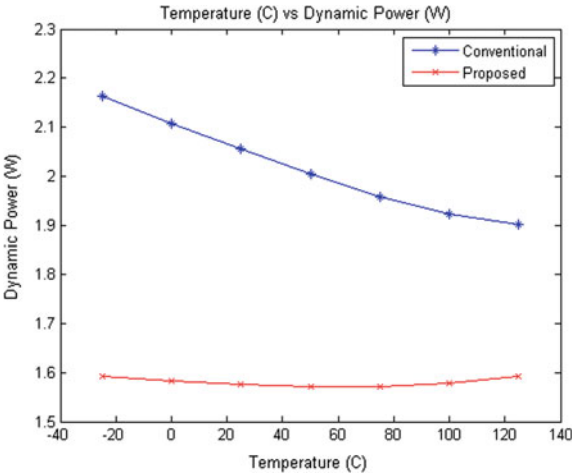


Fig. 6 Impact of temperature on dynamic power

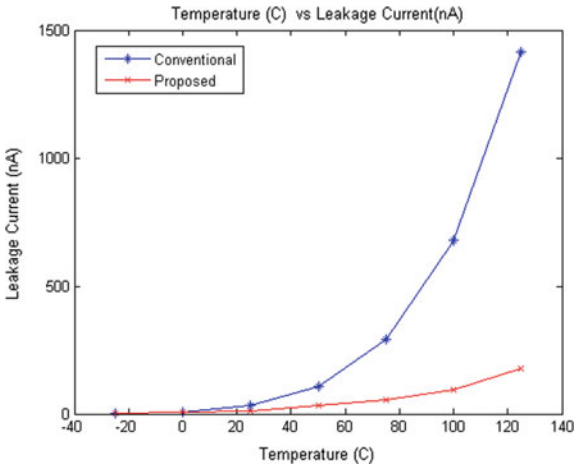


Fig. 7 Impact of temperature on leakage current

The impact of duty ratio or duty cycle on the in-rush current of the conventional and the proposed LED drivers is plotted in Fig. 8. As the duty cycle increases, the in-rush current in the conventional circuit increases drastically and reaches its maximum within a very short time, i.e., 10 ns, whereas, the in-rush current in the proposed LED driver increases gradually and reaches its maximum after 1 μs. Hence the proposed LED driver outperforms the conventional LED driver.

The impact of duty cycle on the dynamic power of the conventional and the proposed circuits is plotted in Fig. 9. The duty cycle has greater impact on the dynamic power of the conventional circuit, whereas it has less effect on the dynamic power of the proposed circuit.

The impact of duty cycle on the leakage current of the conventional and the proposed circuits is plotted in Figs. 10 and 11, respectively. The duty cycle has greater impact on the leakage current of the conventional circuit, whereas it has less

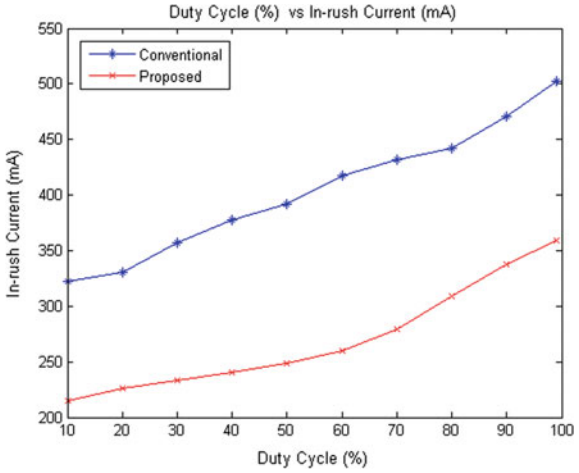


Fig. 8 Impact of duty cycle on in-rush current

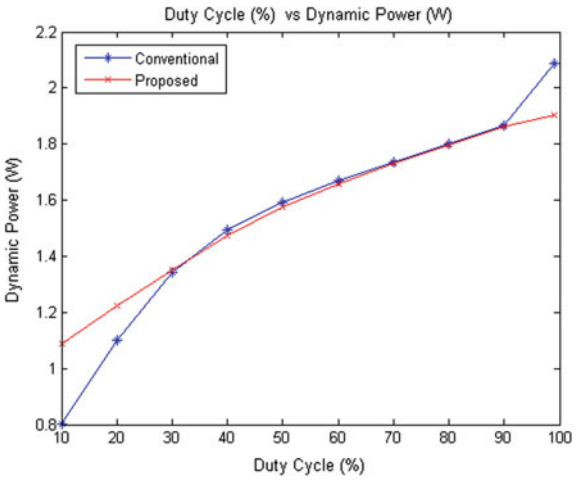


Fig. 9 Impact of duty cycle on dynamic power

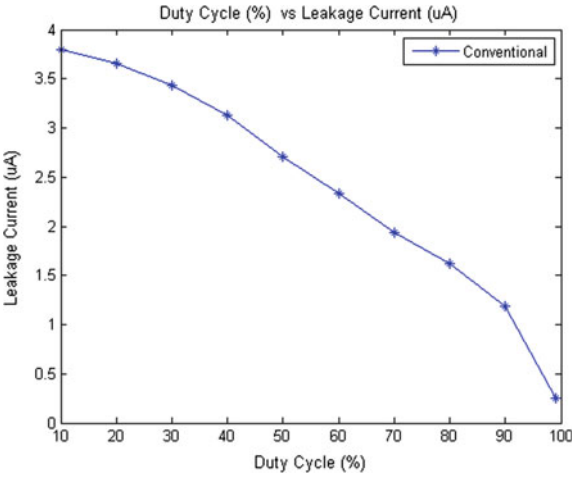


Fig. 10 Impact of duty cycle on leakage power of the conventional LED driver

effect on the leakage current of the proposed circuit. When the duty cycle is 10%, the leakage current in the conventional circuit is 3.801 µA, and leakage current is 0.248 µA when the duty cycle is 99%. When the duty cycle is 10%, the leakage current in the proposed circuit is 37.51 nA, and leakage current is 31.73 nA when the duty cycle is 99%. Conventional circuit suffers from the maximum leakage current during minimum duty cycle.

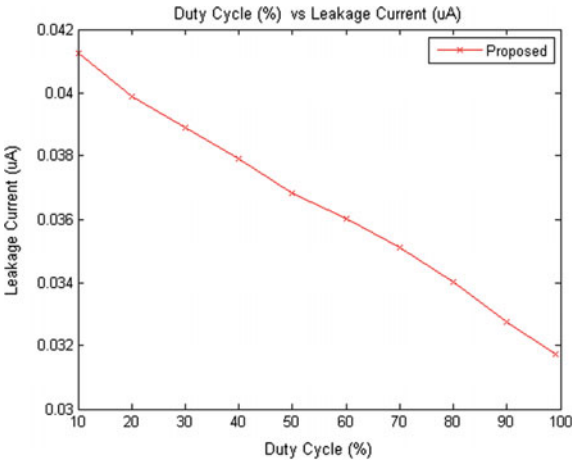


Fig. 11 Impact of duty cycle on leakage power of the proposed LED driver

5 Conclusion

A novel MTCMOS-based on-chip soft-start circuit for low leakage LED driver with minimum in-rush current is proposed. The simulation results were carried out in 180-nm CMOS process technology using Cadence Virtuoso Analog Design Environment. The conventional and the proposed LED drivers were designed to operate at 100 kHz frequency, the simulations were performed at 27 °C, and the duty cycle is varied from 10 to 99% to analyze the characteristics. When the duty cycle is 10%, the leakage current in the conventional circuit is 3.801 μA, and leakage current is 0.248 μA when the duty cycle is 99%. When the duty cycle is 10%, the leakage current in the proposed circuit is 37.51 nA, and leakage current is 31.73 nA when the duty cycle is 99%. The proposed LED driver outperforms well in terms of minimum leakage current during minimum duty cycle as well as minimum in-rush current during start-up of the LED driver. It is evident that the proposed LED driver has minimum in-rush and leakage current with the penalty of area due to MTCMOS-based on-chip soft-start circuit.

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Implementation of Dual Hysteresis Mode Flip-Flop Multivibrator Using Differential Voltage Current Conveyor

Amit Bhattacharyya

Abstract

Background/Objectives: Implementation and analysis of dual hysteresis mode flip-flop multivibrator circuit consisting of merely one differential voltage current conveyor (DVCC) as dynamic component.
Procedures/Approach: Projected dual hysteresis mode flip-flop multivibrator circuit consists of a DVCC, two resistors R_1 and R_2, and a double pole double throw dual in-line package (DPDT DIP) mechanical type switch. Top and bottom saturation levels of the flip-flop multivibrator can be set using passive components. Real structure in design of projected model describes operation of the circuit. Projected design is simulated by Spice as simulation tools. Easily accessible IC AD844AN and passive components are necessary for circuit construction.
Outcomes: Actuality of the planned model is scrutinized as measured and simulation results well agree with hypothetical result. Simulation and measurement results of V_o–V in transfer characteristic curves for clockwise and counter clockwise mode with an operating frequency of $f = 1$ kHz are shown. It is observed that edge voltages for the simulated and measured results are adjacent to the projected values $V_{TH} = 5$ V, $V_{TL} = -5$ V, and the projected flip-flop multivibrator circuit is able to fulfill the dual hysteresis action surrounded by alike design criteria. Projected model provides new presentation for the DVCC founded systems. DVCC has extensive presentations in the area of communication systems, signal processing field especially processing of electrocardiogram signal (ECG), instrumentation, and measurement systems.

Keywords Differential voltage current conveyor · Flip-flop multivibrator
Dual hysteresis mode · Current conveyor

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Table 1 Comparisons between different flip-flop multivibrator structures

Structure	Elements	Passive elements type	Electronically adjustable	Hysteresis procedure	Maximum operating frequency
Operational amplifier based	(1) Operational amplifier = 1 (2) Resistor = 2	At least one earthed	No	Single	Tens of KHz
Second generation current conveyor (CCII)	(1) CCII = 1 (2) Resistor = 3	At least one earthed	No	Single	Hundreds of KHz
Differential voltage current conveyor (DVCC)	(1) DVCC = 1 (2) Resistor = 2 (3) DPDT DIP switch = 1	At least one earthed	Yes	Dual	Hundreds of KHz

1 Introduction

Flip-flop multivibrator has wide functions in the field of processing of electrocardiogram signal (ECG), measurement systems, instrumentation, and communication schemes where typical signals like square, triangular and pulse are analyzed using flip-flop multivibrator [1–7]. In the traditional structure, flip-flop circuit consists of an operational amplifier (OPA) and two resistors but after inclusion of current conveyor, current-mode method of signal processing becomes more advantageous to fabrication of analog circuits for high presentation and useful adaptability. In OPA-based design, a major disadvantage is the variation of output levels with the change of threshold voltage. Current conveyor of second generation (CCII)-based design having one CCII together with three external resistors is also used earlier. A major drawback of previous described circuit is the absence of dual hysteresis mode within the same topology. To overcome various disadvantages of previous popular structure, the proposed model can provide dual hysteresis procedures consisting of only one DVCC, double pole double throw dual in-line package mechanical switch and two resistors as given in Table 1. Aspects of the projected models are as follows:

- Quantity of devices applied to propose design is more or less same.
- Resistors are shorted to ground to achieve benefits of integrated circuit manufacturing procedures.
- Achieved functioning frequency is greater compared to operational amplifier constructed design.
- Within the same topology the characteristics of dual hysteresis operation is obtained.
- Possibility of variation with temperature is fewer.
- Relevancy of entirely DVCC constructed design enhances.
- Higher and lower threshold voltages are electronically adjustable.

In Sect. 2, basic concept and construction of DVCC are emphasized. Then working ideology of bistable multivibrator model is described and associated expressions are given. Also non-ideality and parasitic properties of the planned

circuit are analyzed in Sect. 3. In Sect. 4, a useful fabrication technique and parametric criteria are introduced. Later, laboratory examinations are performed on the fabricated model. Operation of planned model is checked via simulation software and laboratory examination results.

Program and laboratory examined outputs match with hypothetical concepts. Last portion consists of conclusion.

2 Circuit Deliberations and Functioning Principle

2.1 Primary Concept and Implementation of DVCC

DVCC is suitable in continuous signal processing areas due to its large input resistance voltage terminals and large output resistance current terminals. Circuit symbol of DVCC with four terminals is shown in Fig. 1.

X terminal voltage drop (V_X) shows the variance of two *Y* terminals voltage drops, V_{Y1} and V_{Y2}, and *X* and *Z* terminal current propagation; I_X and I_Z occur in the same manner. DVCC has zero *X* terminal input impedance and infinite impedances at two *Y* terminals; hence, I_{Y1} and I_{Y2} both are zero. Voltage drop at *Z* terminal is denoted as V_Z. From above characteristics, *V–I* relations of DVCC are articulated in Eq. (1).

$$\begin{pmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_Z \end{pmatrix} = \begin{pmatrix} 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 \end{pmatrix} \begin{pmatrix} I_X \\ V_{Y1} \\ V_{Y2} \\ V_Z \end{pmatrix} \tag{1}$$

Figure 2 demonstrates a hands-on assembly of DVCC consuming simply available ICAD844AN. AD844AN is a special type of OPA due to virtually short inverting and non-inverting inputs. Current propagation through inverting terminal and T_Z terminal of AD844AN occurs in the same manner. Presence of very high impedance at Non-inverting I/P terminals of first two AD844ANs results I_{Y1} and I_{Y2} equivalent to zero. Connection between T_z terminal and non-inverting terminal of first and third IC AD844ANs via grounded resistor R_b provides the variance of two *Y* terminals voltage drops, V_{Y1} and V_{Y2}, and *X* and *Z* terminal current propagation; I_X and I_Z occur in the same manner. Figure 2 depicts the following relationships between voltage and current:

$$V_{Y1} = V_{1+} = V_{1-} \tag{2}$$

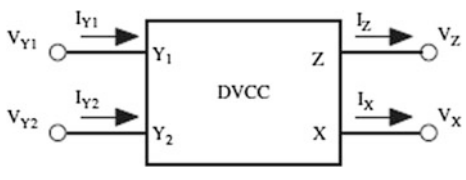

Fig. 1 Circuit symbol of DVCC

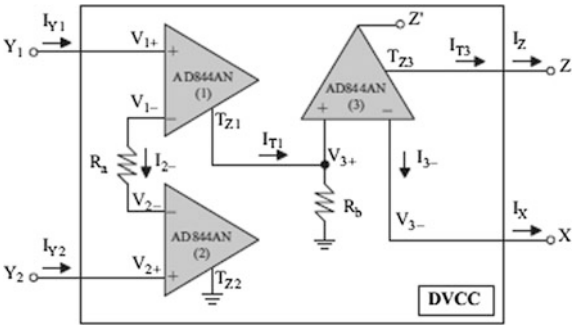

Fig. 2 Implementation of DVCC using IC844AN

$$V_{Y2} = V_{2+} = V_{2-} \tag{3}$$

$$I_{Y1} = I_{Y2} = 0 \tag{4}$$

$$I_{TI} = I_{2-} = \frac{V_{1-} - V_{2-}}{R_a} = \frac{V_{Y1} - V_{Y2}}{R_a} \tag{5}$$

$$I_X = I_{3-} = I_{T3} = I_Z \tag{6}$$

$$V_X = V_{3-} = V_{3+} = I_{T1}R_b = \frac{R_b}{R_a}(V_{Y1} - V_{Y2}) \tag{7}$$

V_{3+} and V_{3-} are non-inverting and inverting voltage drop of third ICAD844AN; I_{T1} is current flowing through T_Z terminal of first ICAD844AN. Therefore, by adjusting resistors R_a = R_b, *V–I* relationship of idyllic DVCC is achieved.

2.2 *Proposed DVCC-Based Model Discussions*

Figure 3 depicts projected DVCC-based flip-flop multivibrator consists of a DVCC, two resistors R_1 and R_2, and a DPDT DIP mechanical type switch. An oscillator [8] supplies triangular waveform as input signal V_{in}. Positive feedback [9] in projected model is obtained by connecting Y_1–Z in conjunction with shorted to ground impedance R_2. DVCC runs between upper and lower saturation levels V_{o}^{+} and V_{o}^{-}.

Figure 4a shows V_{o}–V_{in} transfer characteristics of the projected model during clockwise (CW) mode operation where terminals 1 and 3 and terminals 2 and 4 of DPDT DIP switch are shorted. For this mode, equations of current flowing through X and Z terminal I_x and I_z can be written as:

$$I_X = \frac{V_{\text{o}} - V_{\text{in}}}{R_1} \tag{8}$$

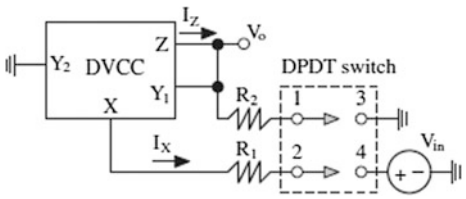

Fig. 3 DVCC-based flip-flop multivibrator controlled by switch

$$I_Z = \frac{V_o}{R_2} \tag{9}$$

At first output voltage V_o is at upper saturation level V_o^+, and input signal V_{in} is absent in the circuit, that is $V_{in} = 0$. Let R_1 is smaller than R_2. From Eqs. (8) and (9), it is clear that current I_X will be higher than I_Z. Thus, V_o remains at top saturation level V_o^+ from starting. When input signal V_{in} is applied in the circuit, current I_X diminishes gradually and V_o switches from V_o^+ to bottom saturation level V_o^- as shown in path 1 of Fig. 4a. When input signal V_{in} diminishes from zero, current I_X increases until I_X is larger than I_Z. Then, V_o switches from V_o^- to V_o^+ as shown in path 2 of Fig. 4a.

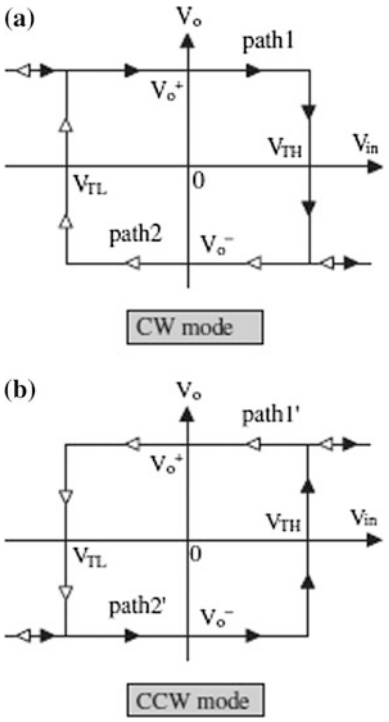

Fig. 4 **a** V_o–V_{in} transfer nature of DVCC-based flip-flop multivibrator controlled by switch for CW manner approach. **b** V_o–V_{in} transfer nature of DVCC-based flip-flop multivibrator controlled by switch for CCW manner approach

Thus, lower and higher threshold voltages, V_{TL} and V_{TH}, can be obtained for the situation when $I_X = I_Z$. Expressions of V_{TH} and V_{TL} in CW mode are given in Eqs. (10) and (11):

$$V_{TH} = V_o^+ \left(1 - \frac{R_1}{R_2}\right) \tag{10}$$

$$V_{TL} = V_o^- \left(1 - \frac{R_1}{R_2}\right) \tag{11}$$

Figure 4b shows V_o–V_{in} transfer characteristics of the projected model during counter clockwise (CCW) mode operation where terminals 1 and 4 and terminals 2 and 3 of DPDT DIP switch are shorted. For this mode, equations of I_x and I_z can be written as:

$$I_Z = \frac{V_o - V_{in}}{R_2} \tag{12}$$

$$I_X = \frac{V_o}{R_1} \tag{13}$$

Let resistor R_1 is smaller than R_2. From (12) and (13), it is clear that current I_X will be higher than I_Z. Thus, V_o remains at the top saturation level V_o^+ from starting, refer to path 1′ of Fig. 4b. When input signal V_{in} diminishes from zero, current I_Z increases. Once I_Z is larger than I_X, V_o switches from V_o^+ to V_o^-. Hence lower threshold voltage V_{TL} is obtained. In path 2′, V_{in} is lower than V_{TH} and V_o is at V_o^-. Once I_Z is more negative than I_X, output level switches from V_o^- to V_o^+. Hence, upper threshold voltage V_{TH} is obtained. Expressions of V_{TH} and V_{TL} in CCW mode derived from (12) and (13) are given in (14) and (15):

$$V_{TH} = V_o^+ \left(\frac{R_2}{R_1} - 1\right) \tag{14}$$

$$V_{TL} = V_o^- \left(\frac{R_2}{R_1} - 1\right) \tag{15}$$

3 Real and Parasitic Properties Explanations

Using IC AD844AN [10], second generation current conveyor in positive mode cascaded with buffering voltage having inbuilt parasitic impedances is obtained according to the datasheet. Several non-idealities, like parasitic impedances and real gain concepts, are emphasized here. A real structure of used DVCC-based circuit model in Fig. 5 is given where R_x, R_y, and R_z acting as terminal parasitic

resistances. Parasitic resistance R_x is approximately several tens of ohms, but R_y and R_z are approximately several mega-ohms. α is considered as non-ideal voltage gain. According to the datasheet of AD844AN, the typical data of α gain = 0.99, β gain = 0.98, R_x = 50 Ω, R_y = 10 MΩ, and R_z = 3 MΩ are considered.

4 Fabrication Criteria and Examined Outputs

4.1 Fabrication Techniques and Parametric Criteria

Minimization of the chance of parasitic and real gain effects of the proposed model, the criteria that $R_a \gg 2R_x$, $R_1 \gg R_x$, $R_b \ll (R_z//R_y)$, $R_2 \ll (R_z//R_y)$ must be maintained in the fabrication techniques. Parasitic resistance R_x is approximately several tens of ohms, but R_y and R_z are approximately several mega-ohm range.

Thus, the chosen values for resistors R_a, R_b, R_1, and R_2 range from few kilo-ohms to few hundreds of kilo-ohms. Fabrication criteria are such that R_1 must be smaller than R_2. DVCC fabricated with easily accessible ICs is able to rise above the issue of loading effect even in the absence of voltage buffer. For implementation and checking purpose, easily accessible ICs AD844AN and passive components are used to check viability of projected model.

4.2 Simulated and Examined Outputs

Laboratory examination is performed by using easily accessible AD844AN ICs, two resistors, and a DPDT DIP mechanical type switch to obtain projected design. To simulate real structure as given in Fig. 5, Spice is the simulation software.

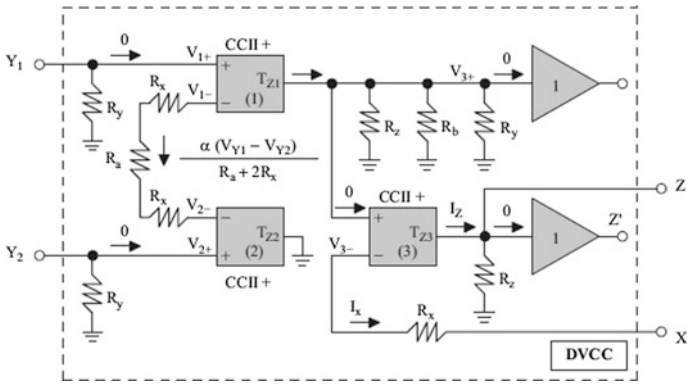

Fig. 5 Real structure of used DVCC-based circuit model

Supply voltages of ±15 V with saturation levels $\mathbf{V_o^+ = V_o^- = 14\ V}$ are maintained for circuit simulations and experiments. External function generator provides applied triggering signal V_{trg}. According to the datasheet of AD844AN, the typical data of α gain = 0.99, β gain = 0.98, R_x = 50 Ω, R_y = 10 MΩ, and R_z = 3 MΩ are considered to satisfy the conditions: $R_b = 10\ k\Omega \ll R_z/R_y = 2.3\ M\Omega$ and $R_a = 9.4\ k\Omega \ll 2R_x = 100\ \Omega$. During clockwise mode operation, the lower and higher threshold voltages are considered as $V_{TH} = 5$ V and $V_{TL} = -5$ V. Hence, a resistance ratio [11] of $R_1/R_2 = 0.64$ is achieved. Arbitrarily R_2 is considered as 20 kΩ ($R_2 = 20\ k\Omega \ll R_z \| R_y = 2.3\ M\Omega$), and hence R_1 as 12.8 kΩ ($R_1 = 12.8\ k\Omega \gg R_x = 50\ \Omega$). For counter clockwise mode operation, a resistance ratio $R_2/R_1 = 1.35$ is chosen, depending upon the said design techniques. Thus, R_2 is considered as 20 kΩ ($R_2 = 20\ k\Omega \ll R_z \| R_y = 2.3\ M\Omega$), and hence R_1 as 14.8 kΩ ($R_1 = 14.8\ k\Omega \gg R_x = 50\ \Omega$).

Figure 6a–d shows the simulation and measurement results of V_o–V_{in} transfer characteristic curves for CW and CCW mode operations with an operating frequency of f = 1 kHz. From Fig. 6a–d, it is shown that the threshold voltages for the

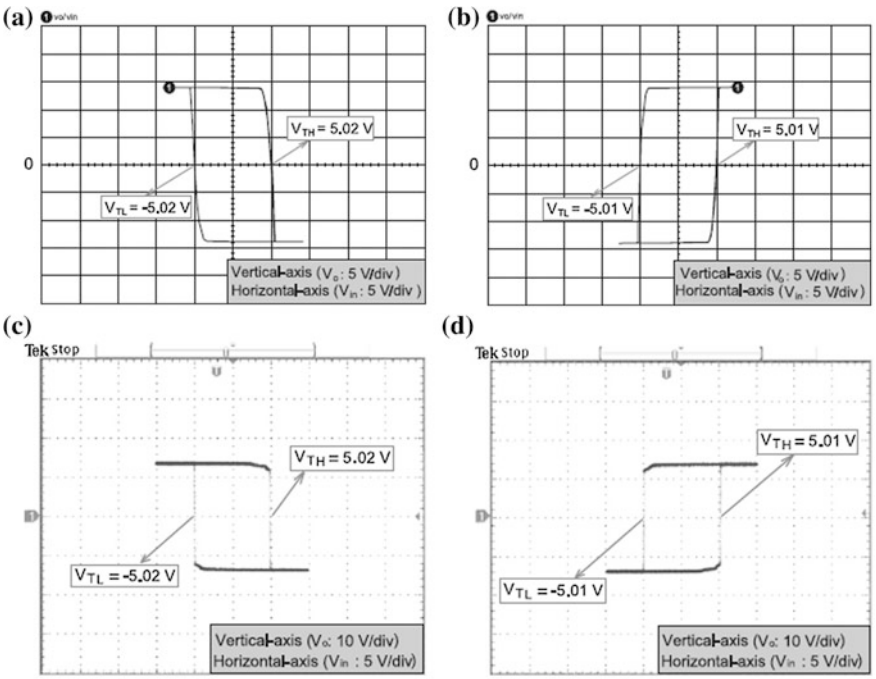

Fig. 6 **a** Simulation result of transfer characteristic for clockwise mode operation with an operating frequency of f = 1 kHz. **b** Simulation result of transfer characteristic for counter clockwise mode operation with an operating frequency of f = 1 kHz. **c** Measurement result of transfer characteristic for clockwise mode operation with an operating frequency of f = 1 kHz. **d** Measurement result of transfer characteristic for clockwise mode operation with an operating frequency of f = 1 kHz

simulation and measurement results are close to the design values $V_{TH} = 5$ V, $V_{TL} = -5$ V, and the projected flip-flop multivibrator circuit is capable of fulfilling the dual hysteresis operation within the same design criteria.

5 Conclusions

In this paper, the projected bistable multivibrator model consists of only one DVCC and three resistors and one DPDT DIP mechanical switch. The projected flip-flop multivibrator circuit is able to fulfill the dual hysteresis action surrounded by alike design criteria. Effectiveness of recommended design is scrutinized due to satisfactory results of program and experiment with theoretical results. The expected design affords new presentation for the DVCC founded systems. DVCC has extensive presentations in the area of communication systems, signal processing field especially processing of electrocardiogram signal [12, 13] (ECG), instrumentation, and measurement systems.

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High Performance Domino Logic Circuit Design by Contention Reduction

A. Anita Angeline and V. S. Kanchana Bhaaskaran

Abstract In this paper, a high-performance domino logic style with reduced delay and less delay variability under process parameter variations is presented. An improved control methodology with delayed enabling of the keeper circuit using the clock signal is proposed. This makes the keeper to be idle during the start of the evaluation phase and reduces the contention. It also helps in increasing the speed performance of the circuit. Furthermore, the reduced loop gain due to the modified keeper circuit lessens the delay variations. The proposed keeper control circuits demonstrate delay reduction of 46% compared to the conventional domino logic circuit. The statistical variations of the process parameters using Monte Carlo analysis demonstrate the reduced delay variations to the tune of 48% for 100 runs. The circuits are simulated using Cadence Virtuoso® employing 180 nm technology node libraries.

Keywords Contention current · Domino logic · Keeper transistor
Leakage current · Low power dynamic circuits · Process variations
Robustness · Reliability

1 Introduction

In high-performance applications, the domino logic circuits are widely used owing to its compactness and increased operating speed [1]. However, the leakage current and the high sensitivity to the input noise degrade the performance. To counteract this, the keeper circuit is incorporated in the dynamic node in order to replenish and retain the nodal charge. An increase in the keeper size replenishes the charge easily,

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and it can retain the logic state for a longer time, which in turn offers robustness for the circuit. However, when the pull-down network (PDN) happens to discharge depending on the input conditions being TRUE, the upsized keeper transistor tries to retain the charge inadvertently, leading to an increased contention current. It can result in deterioration of the speed performance also [2]. Hence, it is imperative to use an appropriate keeper control mechanism and suitable keeper size to offer high speed, low power operating capability and less leakage current.

In wide fan-in applications using domino logic circuits, the presence of numerous leakage current paths leads to easy discharge of the dynamic node charge and results in false evaluation. This embarks on the need for suitable leakage control mechanisms to improve the robustness of the logic. Furthermore, the drain current of the transistor is affected due to the variation in the process parameters, such as the oxide thickness (t_{ox}) and resulting gate capacitance. This results in a corresponding impact on the power and delay variability of the circuit. The loop gain due to the feedback loop, configured by the dynamic node, the inverter and the keeper circuitry also increases the delay variability in addition to the process parameter variations [3]. The necessity for leakage reduction mechanism, robustness and the tolerance to process variations has resulted in devising various keeper control mechanisms by the researchers [4–8].

This paper proposes a keeper control mechanism based on the delayed enabling of the dual keeper transistor circuit during the evaluation phase. This facilitates easy discharge of the dynamic node, when required depending on the input conditions, and the contention is reduced. Section 2 elaborates the conventional domino logic styles, and Sect. 3 details the proposed delayed enabling of the keeper control. The simulations carried out towards the comparative power measurements, delay computations and Monte Carlo simulations for validating the proposed structure are detailed in Sect. 4, and Sect. 5 concludes.

2 Domino Logic Circuit Style

The conventional domino logic style comprises of the following: (1) A single PMOS transistor acting as the pre-charge device (M_{pre}) which also acts as the pull-up network (PUN) and (2) The evaluation NMOS footer transistor, along with the pull-down network (PDN) consisting of NMOS devices connected as per the required logic function. This structure makes the domino logic a high-performance circuit style with less area and lower power consumption [1], primarily due to the reduction in the number of devices employed. While the conventional CMOS circuit requires $2N$ devices, where N is the number of logic parameters involved, the corresponding dynamic implementation requires only $N + 2$ devices. The dynamic logic is felt more advantageous due to the additional fact that N number of PMOS devices which consume more silicon area on the chip is replaced by only one PMOS device acting as the pre-charge device, with the smaller $N + 1$ number of NMOS devices in the pull-down structure. The domino logic when connected with

an NMOS transistor in series acting as a *footer* is referred tothe *footed structure* and when connected without an NMOS *footer* transistor in series is referred to the *footer-less structure*. The two structures are shown in Figs. 1 and 2, respectively. This particular feature can create a difference in the delay and the leakage current parameters of the two types of circuits [4].

During the pre-charge phase, when the clock signal is LOW, the pre-charge PMOS transistor (M_{pre}) conducts making the dynamic node to attain logic HIGH or to the voltage V_{dd} of the power supply. During the evaluation phase, when the clock signal is HIGH, the PDN either retains or discharges the charge of the dynamic node, depending on the input logic conditions. Any possible deterioration of the charge at the dynamic node during the evaluate phase gets replenished constantly using the keeper circuit consisting of a PMOS transistor connected to the inverted dynamic output node as shown in Figs. 1 and 2.

Increasing the size of the keeper transistor, M_k can enable retention of the output nodal charge for a longer time [2]. However, contention current may arise when the PDN tends to discharge in response to the input conditions, and even when the keeper transistor tries to retain the charge at the dynamic node. This leads to inadvertent delay and reduced operating speed of the circuit. Hence, various keeper control mechanisms had been put forth by researchers for reducing the delay [6–10]. Some of the widely discussed proposals are (1) Momentary delayed enabling of the keeper transistor [5]; (2) abrupt control of the keeper transistor [6–8]; (3) keeper control based on precomputation; and (4) optimal sizing of the keeper transistor [10, 11]. In addition to the focus on the charge retained at the dynamic output node, various strategies have also been presented in order to effectively control the leakage current [4].

All these various types of keeper control mechanisms offer the solution at the cost of an additional circuit overhead even while causing more power consumption

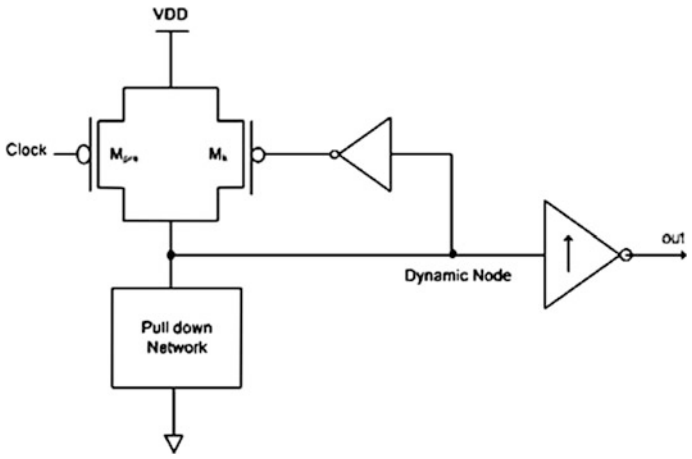

Fig. 1 Footer-less domino logic structure

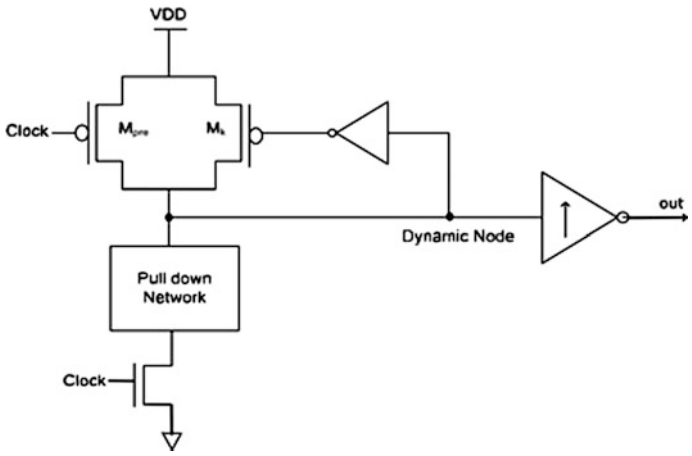

Fig. 2 Footed domino logic structure

due to the overhead. In high-speed domino logic [12], delayed enabling of the keeper circuit is deployed with an additional NMOS transistor and delayed clock control for the keeper circuit. This facilitates easy discharge of the PDN (if required) and increases the speed performance. The proposed style is an enhanced version of the high-speed domino logic style and is also based on the same principle of delayed enabling of the keeper circuit. In less fan-in circuits, power overhead is incurred due to the incorporated keeper control circuitry. However, in wide fan-in circuits, the power overhead is got rid as the leakage power is minimized and hence results in reduced power consumption. This justifies the necessity of additional keeper circuitry in wide fan-in circuits.

3 Proposed Domino Logic Circuit with Reduced Contention

The proposed domino logic circuit shown in Fig. 3 consists of the conventional keeper transistor split into two PMOS keeper transistors (M_{k1} and M_{k2}) connected in series, in addition to the conventional pre-charge transistor and the PDN with the footer transistor. The M_{k1} keeper transistor is controlled by the delayed inverted clock signal. The M_{k2} keeper transistor is controlled by the output signal as in the case of the conventional domino logic style.

During the pre-charge phase, when the clock signal is LOW, the pre-charge transistor (M_{pre}) is in the conducting mode, and the dynamic node is charged to HIGH logic voltage level. When the clock signal is HIGH, evaluation occurs, and the keeper transistor M_{k1} is initially disabled due to the delayed enabling of the keeper transistor (M_{k1}) using the delayed inverted clock signal. This facilitates the

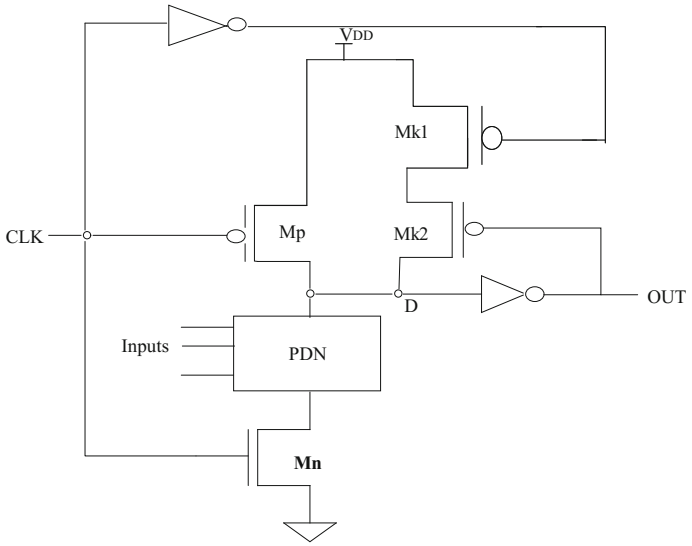

Fig. 3 Proposed clock delayed dual keeper methodology

PDN to facilitate the discharging at a faster pace, when required as determined by the input combinations. After the delay as set by the inverter, the device M_{k1} is enabled, and then, the charge retention of the dynamic node is determined by the M_{k2} keeper transistor.

The momentary delay in enabling the keeper circuit reduces the contention problem between the PDN and the keeper circuit. During the evaluation phase, if the PDN inputs are HIGH, the dynamic node discharges easily during the initial part of the delayed keeper enabling time. This enhances the operating speed of the circuit.

Furthermore, as shown in the circuit of Fig. 3, having two transistors of reduced size in effect lowers the trans-conductance (g_m) of the pull-up network, and hence, the closed loop gain of the keeper (M_{k2})—inverter circuit is also lowered [3]. This reduces the delay variability characteristics of the circuit. Furthermore, the two keeper transistor in the stack arrangement reduces the leakage current occurring in the keeper control circuit.

Comparison of the proposed structure with the conventional domino logic circuit demonstrates the fact that the proposed keeper control circuitry incurs an additional overhead of an inverter and one PMOS keeper transistor. However, the two keeper transistor sizes could be sized to half of the conventional keeper transistor with efficient laying out of the chip. This can render a solution to the problem of the area overhead due to the proposed dual keeper transistor topology.

4 Simulation and Analysis

The simulation of the proposed clock delayed dual keeper circuit is carried out for various wide fan-in gates. The industry standard Cadence® EDA tools employing 180 nm technology library have been used for simulations. A 64-bit input OR gate designed using the proposed delayed dual keeper circuit demonstrates reduced delay values of 352.4 ps compared with the conventional domino logic circuit and high-speed domino which incurs a delay of 411.98 and 405.3 ps, respectively, as marked in Table 1.

Analysing the power consumption characteristics, it can be found that for the gates with less fan-in and simple circuits, a slighter increase in the power consumption is measured for the proposed keeper domino circuits, which is mainly due to the additional keeper circuit. However, for wider fan-in gates, the total power consumption of the proposed circuit is less compared to that of a conventional domino logic circuit and the high-speed domino circuit. It is due to the extra keeper control circuit consuming very less power compared to that of the total power consumption. Figure 4 depicts the comparative analysis of the delay of various test circuits using different types of domino logic.

The leakage current values of the circuit during various phases of operation differ depending on the static leakage current of the OFF transistors. The leakage current is analysed for the three different states, namely (1) clock high input low (CHIL), (2) clock low input low (CLIL) and (3) clock high input high (CHIH). The simulation results tabulated in Table 2 signify that the CLIL state is an idle state for efficient leakage reduction at normal temperature.

The process variations and the feedback loop of the domino circuit can lead to increased delay variability conditions. The proposed circuit is simulated and validated for 100 runs using Monte Carlo simulations. The mean delay (μ) and the standard deviation (σ) of the proposed clock delayed dual keeper circuit are low which makes the delay variability (σ/μ) also to be low compared to that of the conventional domino logic style as depicted in Table 3. The reduced delay variability (σ/μ) of the proposed delayed dual keeper circuit implies less delay variability under PVT (Process, Voltage and Temperature) variations.

Table 1 Power and delay of the proposed circuit

Circuit	Conventional domino logic circuit		High-speed domino circuit		Conventional domino logic circuit	
	Power (μW)	Delay (ps)	Power (μW)	Delay (ps)	Power (μW)	Delay (ps)
8 OR	8.55	105.99	16.41	123.3	9.76	93.33
16 OR	13.844	151.8	22.61	137.1	14.6	132.21
32 OR	24.61	240.21	34.09	234.7	24.62	207.6
64 OR	48.36	411.98	56.16	405.3	44.77	352.4

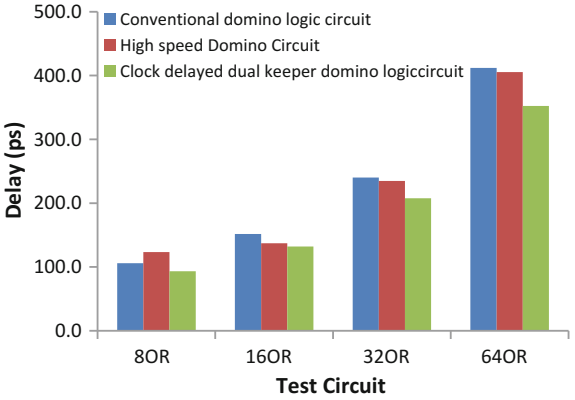

Fig. 4 Delay comparison of proposed circuit

Table 2 Leakage current at different states

Test circuit	CHIL (pA)	CLIL (pA)	CHIH (pA)
8 OR	93.2	37.33	41.02
16 OR	107.63	43.354	41.02

Table 3 Delay variability analysis using Monte Carlo simulations for 100 runs

Test circuit	Conventional domino logic circuit delay			Clock delayed dual keeper circuit delay		
	Standard deviation σ (ps)	Mean μ (ps)	σ/μ (%)	Standard deviation σ (ps)	Mean μ (ps)	σ/μ (%)
8 OR	7.5	106.35	7.1	6.49	94.31	6.9
16 OR	11.94	151.6	7.9	10.71	134.2	8.0
32 OR	20.7	240.03	8.6	17.99	206.46	8.7
64 OR	42.67	411.44	10.4	34.39	351.59	9.8

5 Conclusion

The delayed enabling of the keeper circuit in the proposed domino logic circuit style using clock and the dual keeper circuitry facilitates efficient and contention-less discharge of the PDN. This enhances the speed of the domino logic circuit. It is observed that for a 64-bit input OR gate, it is around 352.54 ps. Additionally, the delay variability of 9.8% realized by the proposed method demonstrates the fact that this proposed structure of domino logic is more robust. It is also observed that the clock low input low (CLIL) state is the optimal state for leakage reduction under idle conditions at room temperature. These analyses substantiate the claims that the proposed clocked delayed dual keeper circuit can perform the logic evaluation at higher speed with greater robustness.

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Differential Power Analysis (DPA) Resistant Cryptographic S-Box

A. Prathiba, K. M. Madhu and V. S. Kanchana Bhaaskaran

Abstract Cryptographic systems demand differential power analysis (DPA) resistant designs. The DPA resistance property of the Differential Cascode Pre-resolve Adiabatic logic (DCPAL) of quasi-adiabatic type of logic circuit is investigated in this paper. The DCPAL is an adiabatic logic, which incurs lower power consumption and earns its application in the design of low power cryptosystems. The property of power analysis resistance is demonstrated through the use of DCPAL implementation for a substitution-box (S-Box). The S-Box is implemented in both the standard CMOS and the DCPAL styles to prove the power analysis resistance and low-power operation capability. Fair comparisons have been made for validation. The advantage of using the DCPAL for DPA resistant systems is also demonstrated through the S-Box implementation. Extensive transient simulations have been carried out using the technology files from 180 nm foundry.

Keywords Side-channel attacks · DCPAL · Differential power analysis resistance S-Box · Adiabatic circuits for DPA resistance

1 Introduction

Observation of the parameters, namely the power consumption, electromagnetic radiation, and interference, along with the computation time of an operation can reveal the secret key of the cryptographic devices by side-channel analysis (SCA). This poses a major threat to the crypto chip designers. Among the major side-channel attacks, the DPA techniques are found to be more powerful, primarily due to the reason that they unveil the secret information by analyzing the intermediate power variation. Power analysis is a form of side-channel attack and is classified as simple power analysis (SPA) and differential power analysis (DPA). SPA technique leaks the power information through observation of the power

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traces, while the DPA relies upon the more involved statistical mechanisms for revealing the secret key. S-Box is the only nonlinear module in the symmetric block cipher algorithms, and its power resistant design in the circuit level of abstraction offers a greater measure of DPA resistance even at the cell-level design and further development stages.

The majority of the digital systems are designed using the conventional CMOS logic style, which during all the switching operations reflects the power activity of the circuits, such as the logic transitions, logic 0–1 and 1–0. This is due to the charging and discharging of the nodes of the conventional CMOS logic circuits, and this enables the power attacks in most of the cryptosystems. As a solution to this major issue, researchers have employed dual-rail CMOS logic design for incorporation of DPA resistance property [1]. However, the main disadvantage of the dual rail CMOS is their unity activity factor. This is due to the fact that evaluate or the pre-charge transition is guaranteed for every cycle regardless of the input activity. Hence, the dual rail CMOS suffers from increased power consumption, which in addition to the clocking power reaches intolerably higher levels. Another logic style with the DPA resistance property, which is widely discussed in the literature, is the efficient charge recovery logic (ECRL). It is one of the early quasi-adiabatic families in which the discharge circuits are asymmetric, and hence, it results in varying charging and discharging time values [2]. To solve this problem, some researchers have presented the adiabatic circuits which are symmetric in nature [3–9].

A power analysis resistant circuit is expected to belong to the logic style, which irrespective of the logic switching of the output nodes of the circuit expends uniform power dissipation even while seeking lower power consumption capability. With a uniform power trace, it becomes difficult for the hackers to extract the information through the process of DPA. The variations in power traces are found uniform, and the power per transition is also very less as compared to the CMOS circuit style. This hence can protect the cryptosystems against the DPA attacks [10, 11]. The low power operating and constant power dissipating features of the DCPAL are found to be suitable for the design of DPA resistance system. In this work, the S-Box is designed using both the standard CMOS logic and DCPAL styles and the results have been compared. The advantages of using the later have been explained with the results and power transient waveforms.

The structure of the paper is organized as follows. The DPA resistance property of the DCPAL S-Box is highlighted in Sect. 2. The design methodology of the standard CMOS S-Box is explained in Sect. 3, and the DCPAL implementation methodology has been explained in Sect. 4. The power analysis is carried out in Sect. 5, and conclusion is presented in Sect. 6.

2 Adiabatic Logic for DPA Resistance

The DPA countermeasure for an efficient cryptographic hardware necessitates constant power consumption irrespective of the data variations. It must prevent the dependencies between the power consumption values and the input data. Normally, the counter mechanisms employed in the circuit level aim at uniform power dissipation irrespective of the input variations [12–14]. The DCPAL is a quasi-adiabatic logic suitable for such light-weight devices, and hence, it can be a suitable choice for implementation of the light-weight crypto hardware. In addition to the low-power operating capability, the cryptographic circuits demand less vulnerability to side-channel DPA power analysis. The power analysis resistance capability of the DCPAL is validated in this section through the implementation of the DCPAL XOR gate as shown in Fig. 1. Here, PC1 and PC3 are the power clocks which are 180° out of phase with each other, and the power clocks serve as the power supply and timing clock signal for the DCPAL circuitry. It has four phases of operation, namely the Pre-resolve, Evaluate, Hold, and Recover. The input and output transient waveforms for the XOR operation are shown in Fig. 2. Figure 3 presents the supply current variations as observed for the certain set of input transitions, and it is also observed to be constant as shown in the figure, irrespective of the input transitions. The power trace for the input transitions 00-11-10-01-00 in Fig. 4 shows the uniform power variations. This, thus, proves the suitability of DCPAL for the design of DPA resistant Cryptographic systems. The work is further extended with the S-Box implemented in both the standard CMOS circuit style and the DCPAL circuit style. The following sections detail the S-Box implementation in both the standard CMOS and the DCPAL, respectively.

3 Methodology of the Standard CMOS Logic S-Box Implementation

The S-Box implementation methodology incorporates mechanisms to eliminate the unnecessary transitions. The combinational logic modules, namely logic 1 to logic 3 shown in Fig. 5 are the submodules of the S-Box implemented using the standard CMOS logic. Buffers are used to match the delays in the feed-forward path. This avoids the unwanted glitches. The CMOS_FFP 1 and CMOS_FFP 2 are the feed-forward paths. Int_in1 to int_in6 are the intermediate inputs. The feed-forward paths (FFP) in the circuit balance the timing at the input port of the logic blocks. I1 is feed-forwarded to one stage ahead, and hence, the buffer in the CMOS_FFP 1 path should offer the delay as that of the propagation delay incurred by the logic 1 module. In other words, the signal Int_in1 must reach the input of the logic 2 module at the same time as the signal Int_in2. Similarly, the feed-forward path CMOS_FFP 2 caters to the timing balance of the input Int_in5 at the logic 3 module. Meeting these timing constraints will avoid any glitches in the output and eliminates any possible unnecessary power consumption.

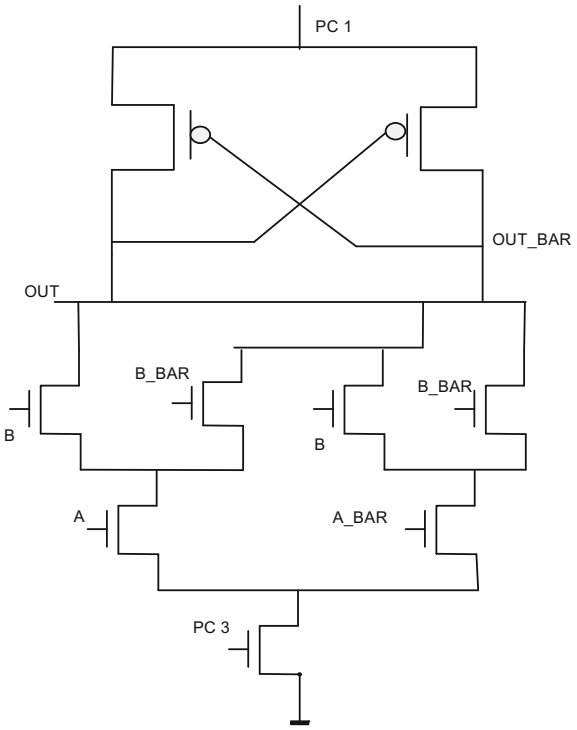

Fig. 1 DCPAL XOR/XNOR gate

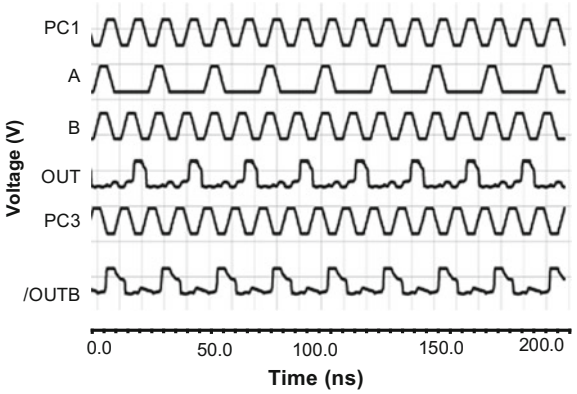

Fig. 2 Input/output waveforms of the DCPAL XOR/XNOR gate

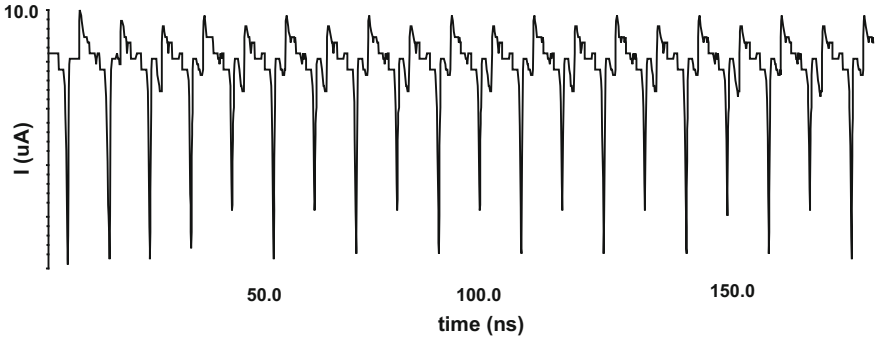

Fig. 3 Supply current variations of the DCPAL XOR gate

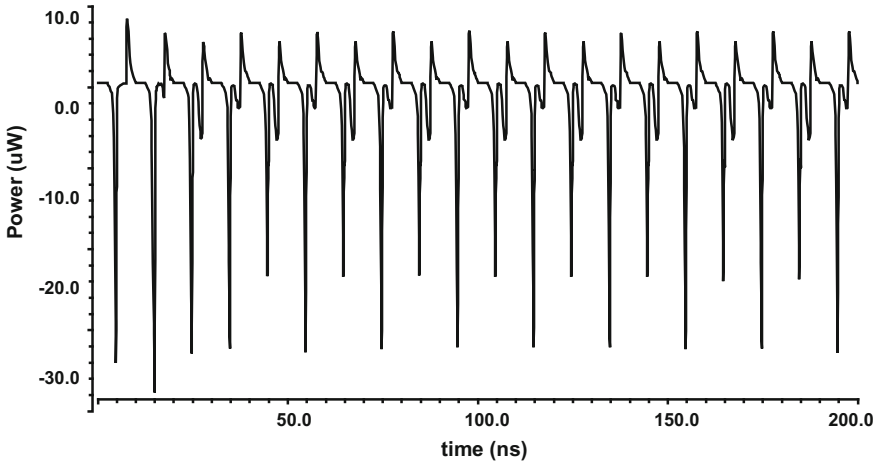

Fig. 4 Power consumed by the DCPAL XOR gate

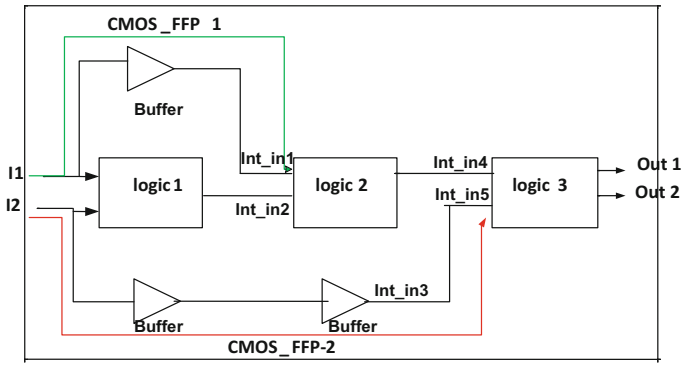

Fig. 5 Standard CMOS logic S-Box

4 Implementation Methodology of the DCPAL-Based S-Box

The primary challenge in the system implementation using the DCPAL is meeting the timing constraints. The adiabatic logic circuits use power clocks as the supply voltage and the synchronizing clock signal. The DCPAL_FFP 1 and DCPAL_FFP 2 mentioned in Fig. 6 are the two feed-forward paths (FFPs). The delay of the path from I1 to the input port of logic 2 as denoted by the path DCPAL_FFP 1 in the schematic should offer the same delay as the propagation delay incurred by the logic 1 module for the Int_in1 and Int_in2 to be valid at the logic 2 block input. In addition, the power clock phases of the buffer and logic 1 should be in phase as shown by PC1 and PC3 in Fig. 6. In the path DCPAL_FFP 2, the intermediate inputs Int_in1, Int_in2, and Int_in3 are maintained in the same phase. In order to match the phase conditions at the logic 3 input port, the successive power clock, namely PC3 and PC1 are applied to buffer 3. This operating requirement is the main consideration to be taken care in the implementation of DCPAL circuits. The methodology has 17 inner-pipelining stages employed to implement the S-Box, and the output latency hence will be 17 $\times$ T_p s, where T_p is the propagation delay of a single stage of the pipeline. If T_p is 1 ns, then the output would be observed after 17 ns since the input is applied.

Figure 7 shows the inputs X0–X3 applied to the S-Box, and the signals PC1–PC4 are the power clocks, and S0–S3 are the outputs of the S-Box. The period of each pipelining stage is 0.25 ns, and the output will be available after 17 $\times$ 0.25 ns = 4.25 ns, where 17 is the number of pipeline stages.

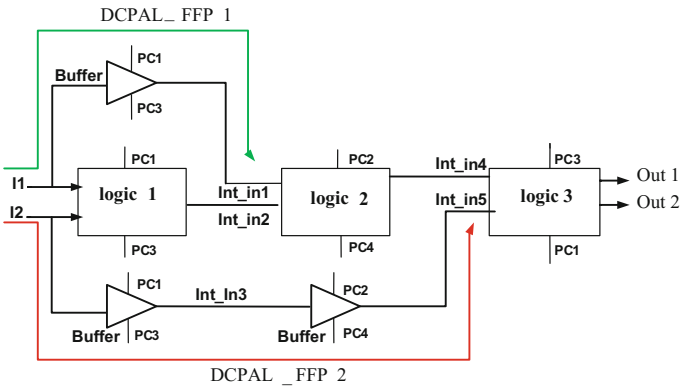

Fig. 6 DCPAL S-Box

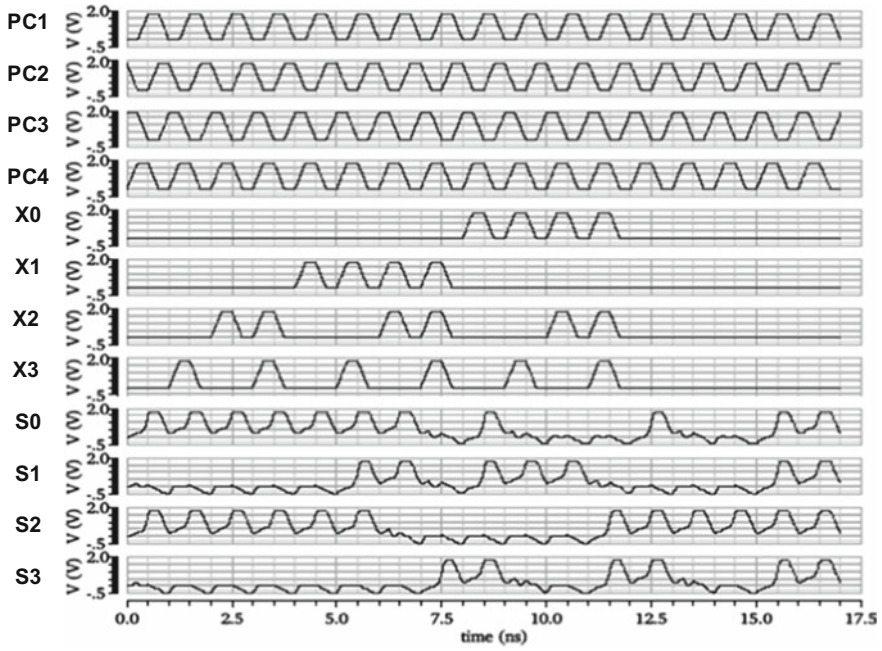

Fig. 7 Output of the DCPAL S-Box

5 Power Analysis

The power variations of the S-Box implemented in both the standard CMOS and DCPAL are analyzed with the input clock period of 1 ns. The average power of standard CMOS logic-based S-Box is 1.73 mW, and for the DCPAL, it is found to be 949.3 μW. The results validate the claim that the DCPAL adiabatic logic-based S-Box circuits consume lower power. In standard CMOS logic style, the power spikes of 0–1 transition are clearly visible as shown by the power traces in Fig. 8 with values ranging from 5 to 21 mW. On the other hand, the DCPAL systems incur uniform power variation around 950 μW irrespective of the circuit switching. This makes the cryptosystems DPA resistant, since the power of DCPAL is so low of the order of μW, and it becomes difficult for the SPA systems to identify the variations from the power traces so obtained.

With all the outputs of S-Box high at 9 ns, the highest spike in the power trace (marked area) of 20.23 mW is observed in Fig 8. This non-uniform power variation will help the hackers to guess the pattern of outputs. This is a threat for the chip designers.

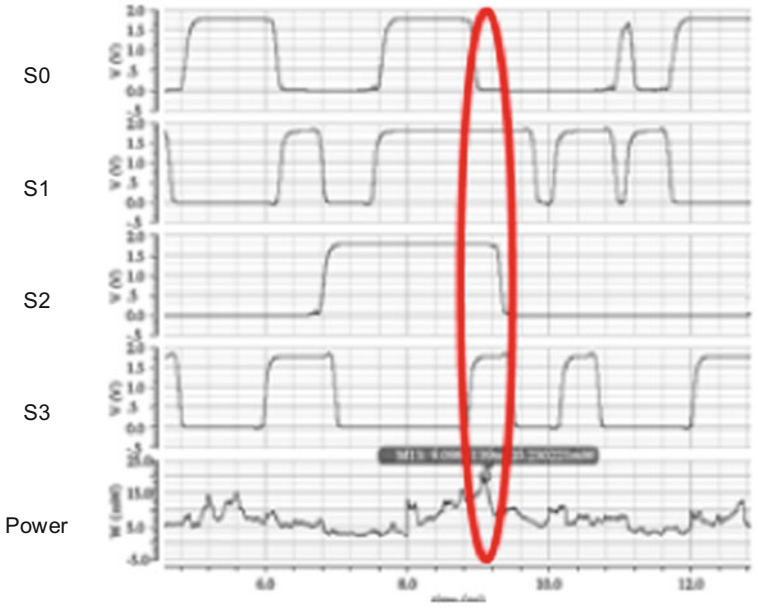

Fig. 8 Power trace of the standard CMOS S-Box

The uniform power variation incurred by the DCPAL-based system is shown in Fig. 9, and its power consumption is very less as compared to the standard CMOS counterpart. In the standard CMOS style, the highest peak current is found to be 20.23 mW. On the other hand, it is measured to be 6.98 mW for the DCPAL-based design. This validates the claim of low power consumption in the DCPAL implementation.

6 Conclusion

The use of DCPAL-based adiabatic circuits for the implementation of cryptosystems to prevent the DPA attacks on chips has been presented. The claims are validated through the power trace results of the CMOS and DCPAL-based S-Boxes. The implementation of elementary XOR gate is to prove the principle of DCPAL adiabatic operation. The average power of standard CMOS logic is found to be 1.73 mW and that of the DCPAL is measured to be 949.3 μW. The peak power dissipation is found to be 20.23 and 6.98 mW for the standard CMOS and DCPAL-based circuits, respectively. The future work is to improve the S-Box design for area optimization and implementing the S-Box with the combination of different logic styles, aiming at further reduction in the number of spikes.

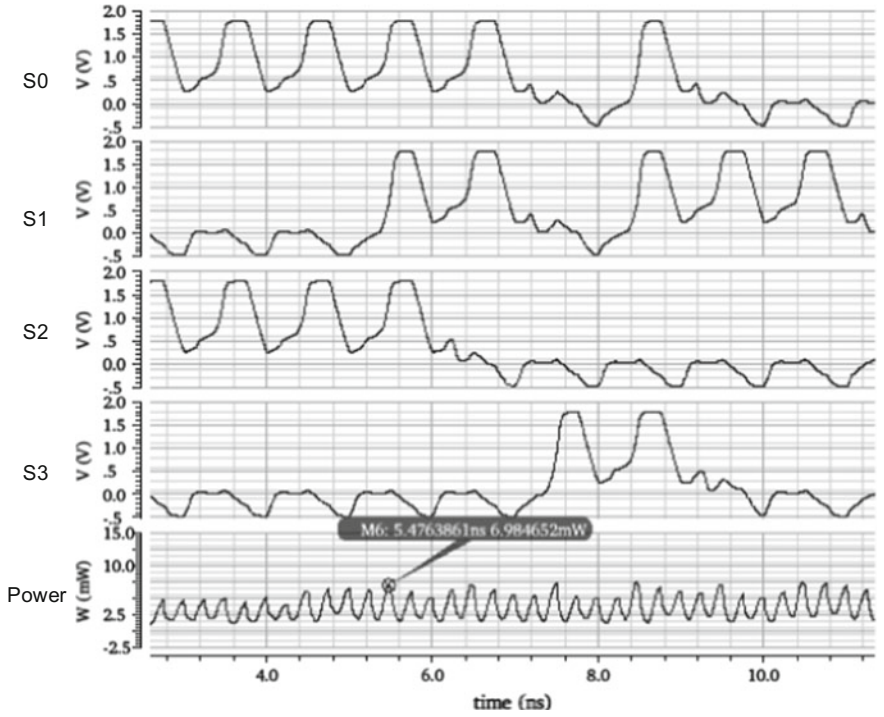

Fig. 9 Power trace of the DCPAL S-Box

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Implementation of Radix-2 Butterfly Using Distributed Arithmetic Algorithm (DAA)

Ketan Tarkas, Chetan Sharma, Oshin Mehta and P. Augusta Sophy Beulet

Abstract

Background/Objectives: The FFT computation is a widely used building block in signal processing. In this work, radix-2 butterfly is implemented by distributed arithmetic algorithm (DAA).
Methods/Statistical Analysis: The distributed arithmetic distributes the calculations in a bit-serial manner, thereby the lumped multiplications are eliminated.
Findings: Designing of butterfly is done using Verilog HDL, simulation is done in Cadence NC Sim tool, and synthesis is done in Cadence RTL compiler. The proposed architecture provides high speed and less area compared with existing architecture. The proposed structure requires less power compared to existing structure.
Improvements/Applications: The DA is used in many applications of DSP functions like filtering, FFT, DCT.

Keywords FFT · Radix-2 butterfly · Distributed arithmetic · Look-up table (LUT)

1 Introduction

Fast Fourier transform (FFT) is very commonly used in many DSP and communication applications. Design of radix-2 decimation in time (DIT) butterfly, based on look-up tables (LUTs) [1, 2] is used as a methodology in this work. Distributed

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Arithmetic (DA) has been selected to perform the multiplication by the twiddle factors. This arithmetic uses look-up tables (LUTs) to store the pre-calculated values which are the combinations of the coefficient to get the required multiplier output. It is used in a large number of DSP applications (filtering, transforms, etc.). The distributed algorithm (DA) is used to perform multiplication in radix-2 butterfly. This algorithm results in area reduction while large size FFTs are designed.

Multiplication is a strong operation because it needs a repeated addition. Hence it occupies large chip area and also consumes more power. Implementing butterfly of FFT algorithm using distributed arithmetic is a different approach. In DA, all multiplications and additions are replaced by a look-up table (LUT) and a shifter-accumulator [3]. Distributed arithmetic technique leads to a multiplier-less architecture for digital signal processing applications. Distributed arithmetic-based computations are cost-effective and area-efficient.

Butterflies are the essential building block of FFT implementation of digital signal processing (DSP). Distributed arithmetic efficiently computes the sum of products called the vector product. This is otherwise known as inner product or multiply and accumulate (MAC) operation. MAC operation is very common in all digital signal processing algorithms [4]. The benefits of DA can be best exploited in the design of data path circuits like multipliers. DA efficiently implements the MAC using look-up tables. In this work, DAA is used for designing a radix-2 butterfly.

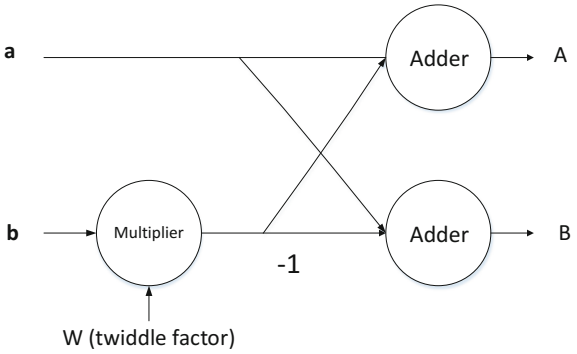
2 Decimation in Time (DIT) Radix-2 Butterfly

In fast Fourier transform algorithm (FFT), the butterfly devices a mechanism that combines the results of smaller discrete Fourier transforms (DFTs) into a larger DFT, or vice versa. The name butterfly is given because the shape of radix-2 signal flow diagram looks like a butterfly. In Cooley–Tukey FFT algorithm, the term "butterfly" appears to break down a DFT of size $n = r^m$ into "r" number of smaller transforms of size "m" where r is the "radix" of the transform. These smaller DFTs are then combined by a bigger butterfly of size r to obtain the DFTs of size r. There are two types of algorithm, the "decimation in time" (DIT) and "decimation in frequency" (DIF). DIF is similar to DIT but few steps are reversed, where the butterflies are post-multiplied by root of unity known as twiddle factors [5]. In radix-2 Cooley–Tukey (CT) algorithm, a DIT size-2 butterfly takes two inputs (x_0, x_1) and gives two outputs (y_0, y_1). A radix-2, DIT algorithm of $n = 2^p$ inputs needs the primitive nth root of unity $\omega_n^k = e^{-\frac{2\pi ik}{n}}$ and relies on $O(n \log n)$ butterflies. The outputs of a butterfly are obtained from Eqs. (1) and (2) as shown in Fig. 1.

$$y_0 = x_0 + x_1\omega_n^k \tag{1}$$

$$y_1 = x_0 - x_1\omega_n^k \tag{2}$$

Fig. 1 Radix-2 butterfly



3 Distributed Arithmetic Algorithm

Distributed arithmetic (DA) technique is basically a bit-serial operation. Efficient computation of weighted sum of product or dot product can be computed by using the basic DA algorithm [6]. Computation of the inner product of an input vector and constant coefficient vector as given in Eq. (3) can be done by DA technique and is explained as follows.

$$Y = \sum_{k=1}^{K} A_k X_k \tag{3}$$

Where,

Y Output response
A_k Constant filter coefficients
X_k Input data.

Let X_k be represented in a N-bit format and expressed in scaled two's complement number as in (4)

$$X_k = -b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \tag{4}$$

Substituting X_k into the Eq. (3), we get Eq. (5)

$$Y = \sum_{k=1}^{K} A_k \left[-b_{k0} + \sum_{n=1}^{N-1} b_{kn} 2^{-n} \right] \tag{5}$$

On rearranging the computed terms and grouping the sum of products together, the final Eq. (6) formed is,

$$Y = -\sum_{k=1}^{K} A_k.b_{k0} + \sum_{n=1}^{N-1}\left[\sum_{k=1}^{K} A_k.b_{kn}\right]2^{-n} \tag{6}$$

The DA contains look-up table (LUT), accumulator and shifter. Look-up table (LUT) contains all the partial products that are pre-computed [7]. LUTs are addressed by the inputs given to the multiplier and its coefficients decide the values to be stored in LUT [4]. Only the addition and subtraction of coefficients and the coefficient itself are the part of LUTs.

In the above equation, AND operation is performed between the bits of input given and the constant coefficient known as twiddle factor. The plus signs are there to perform arithmetic addition operations. By this, a look-up table is made that contains all the partial product values that are pre-computed. These LUTs are addressed by the inputs given to the multiplier. The term given as 2^{-n} is to shift bits pattern [8].

4 Butterfly Using DAA

Using distributed arithmetic algorithm, the multiplication in butterfly can be done without using multiplier. Using look-up table (LUT), the multiplications are pre-computed and stored in LUT, and thus the use of LUT reduces the area, latency and also the power consumption [3]. Using the concept of DA, a butterfly can be made and this butterfly can be instantiated many times in the FFT algorithm.

Block diagram is given in Fig. 2. It contains the following units, namely bitwise concatenation, LUT, shifter, and accumulator. The first unit is bitwise concatenation, which does the concatenation from least significant bit (LSB) to most significant bit (MSB) of the two inputs given to it. Next unit is LUT, it contains the values of partial products and gives the value stored at the desired address as shown in Tables 1 and 2. The output of LUT is given to shift unit which shifts it in the left direction. This shifted value is accumulated in ACC unit and finally the output is generated.

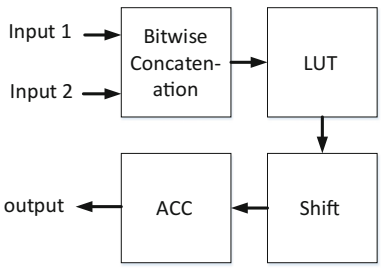


Fig. 2 Block diagram of distributed arithmetic algorithm

Table 1 LUT for DA real part

Address	Output
00	00000000
01	00011001
10	00100110
11	01000000

Table 2 LUT for DA imaginary part

Address	Output
00	00000000
01	00100110
10	11100111
11	00001100

Table 3 Comparison between ordinary and DA butterfly

Parameter	Ordinary butterfly	DA butterfly
Power (nw)	7411464	4418998
Cells	2919	874

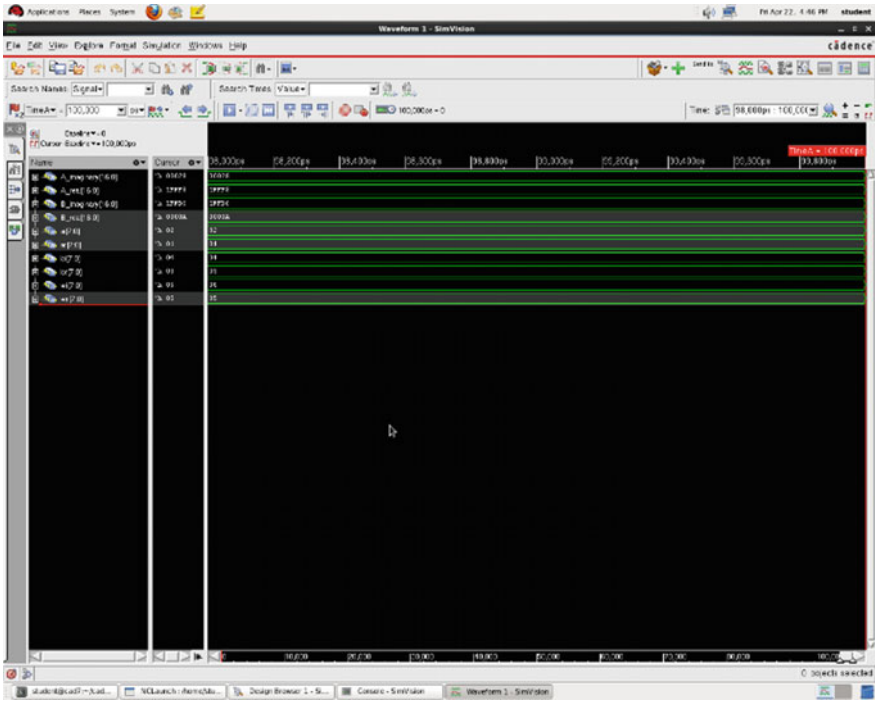


Fig. 3 Simulation of ordinary butterfly

5 Results

From Table 3, it can be seen that the power utilized by DA butterfly is very less compared to ordinary butterfly and also the cells used for ordinary butterfly is three times that of DA butterfly.

Figure 3 shows the simulation of conventional butterfly, where the values of input and twiddle factor are given in the test bench. Figure 4 shows the outputs for some random values. Simulation in Figs. 5 and 6 are the intermediate values of final DA-based butterfly where the simulation of imaginary part and real part is shown separately. And in Fig. 7, the schematic of distributed arithmetic algorithm (DA)-based butterfly is shown.

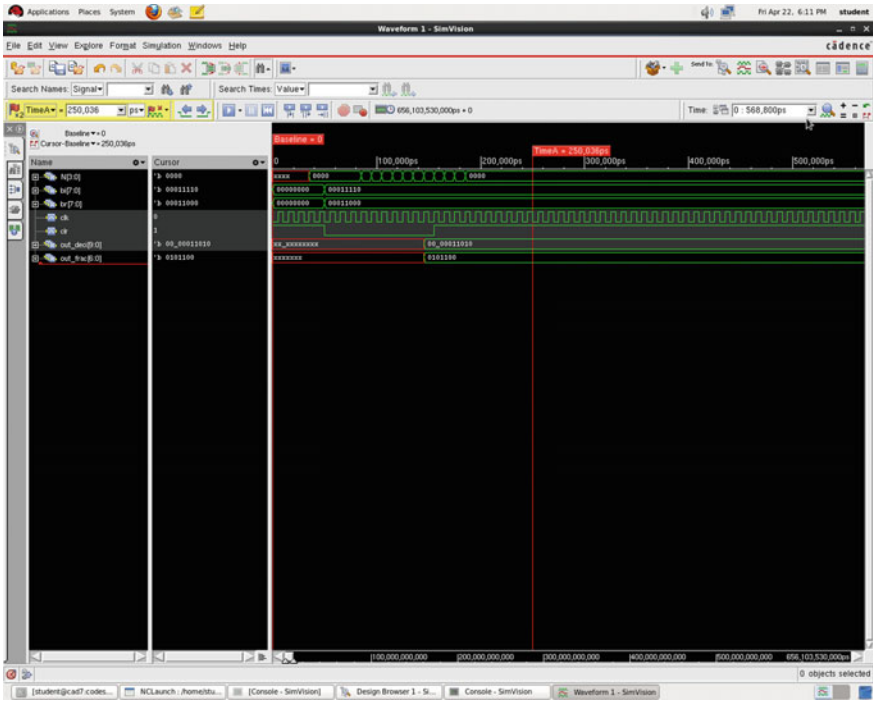


Fig. 4 Simulation of DA real part

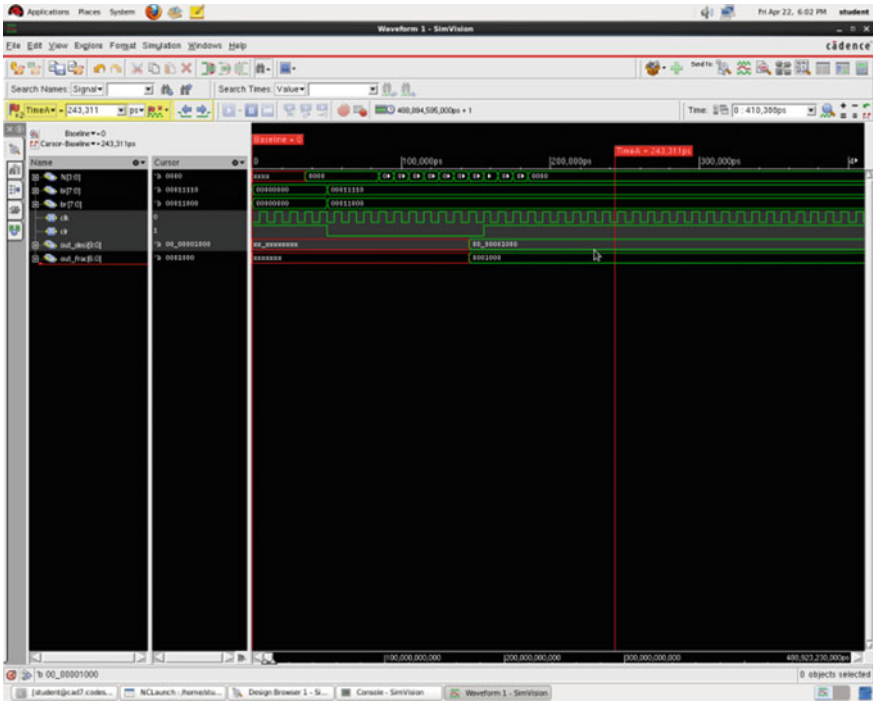


Fig. 5 Simulation of DA imaginary part

6 Conclusion

DA has been applied significantly in various digital signal processing (DSP) applications. In this method, the implementation of multiplier-less butterfly using distributed arithmetic algorithm is done. This is having bitwise concatenation, look-up table (LUT), shifter, and accumulator. LUT partition reduces memory requirements. This technique reduces the delay, area, and power consumption. By

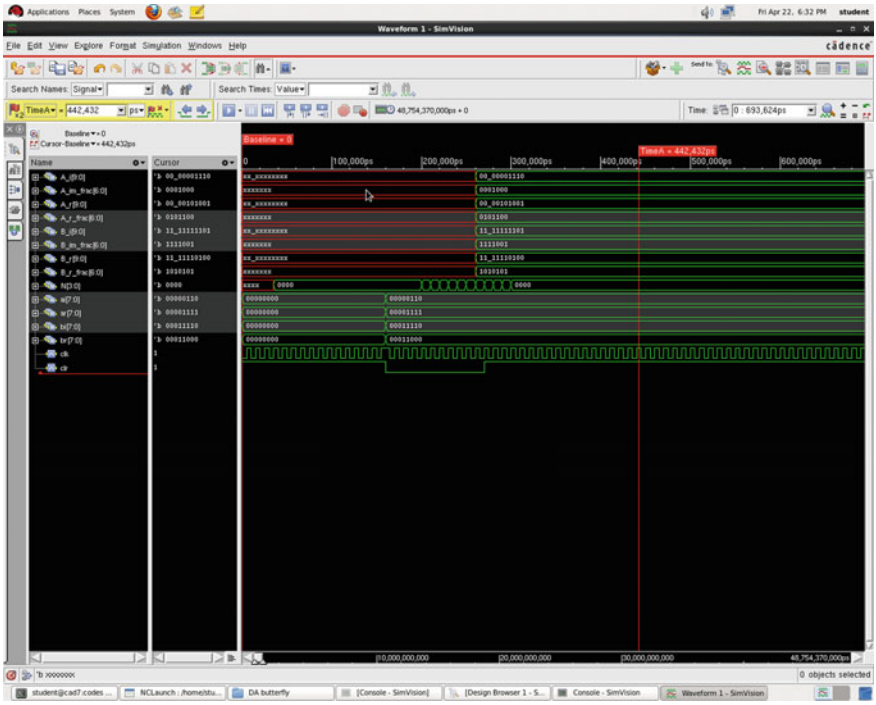


Fig. 6 Simulation of DA-based butterfly

pipelining of all partial products, further improvement in performance can be seen. Area and timing are improved by basic DA structure, which involves significantly less latency and less area-delay complexity when compared with conventional butterfly structure.

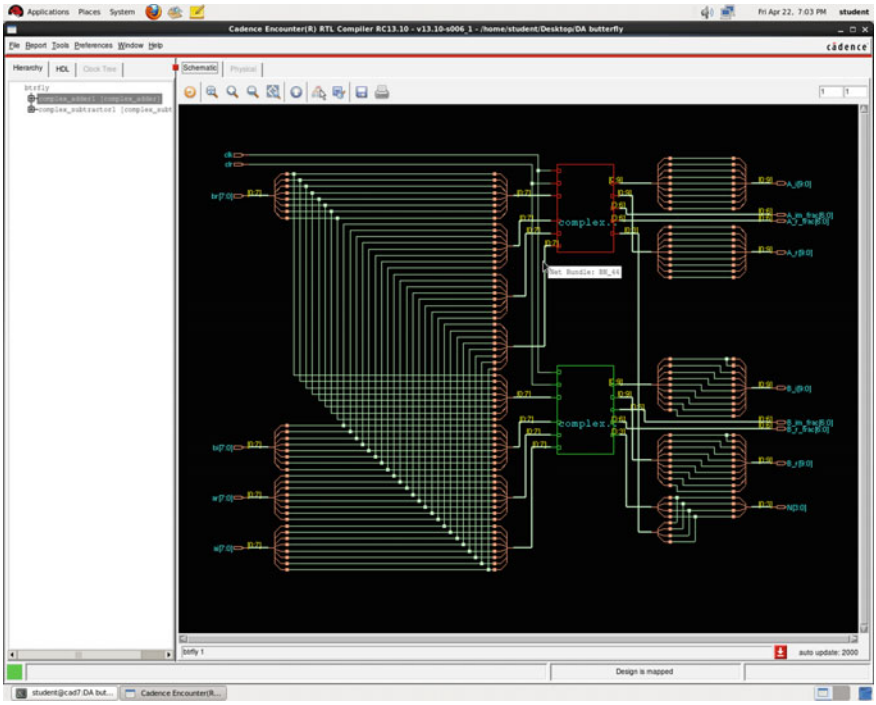


Fig. 7 Schematic of DA butterfly

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An Area Efficient Design of Warped Filters

Kruttika Golwelker, Ritu Kumari and T. Vigneswaran

Abstract An area efficient implementation of the warped filter using variable high-pass, low-pass, band-stop and band-pass responses is proposed in this research work. A warped filter is achieved by placing an all-pass filter in the place of unit delay in the configuration of the digital filter. A variable high-pass or low-pass configuration is obtained using first-order transformation of the all-pass filter. However, the band-stop and band-pass variable filters are achieved by all-pass configuration of second order. A technique of coefficient decimation is used in the warped filter to overcome this issue. In order to make this design area efficient, a comparative analysis among the various adders and multipliers is performed. The most efficient adder and multiplier are incorporated in the filter design. The comparative analysis for the different adder and multiplier disposition is performed in the Cadence environment using the RC tool. The coding style used for this implementation is Verilog Hardware Description Language (HDL). The area utilization is reduced by 22% by implementing the new design of the warped filter.

Keywords Warped filter · Variable digital filter · Low pass · High pass
Band pass · Band stop · Coefficient decimation

1 Introduction

The variable digital filter is one which produces different responses by varying parameters such as cut-off frequencies. A warped filter is an example of a Variable Digital Filter (VDF) [1]. The delay element of a filter is replaced by an all-pass

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single-stage filter structure. Warped filters have a wide range of applications ranging from audio applications like loudspeaker equalization, linear prediction, and detection of band-pass signals [1], echo cancellation, spectral modification of audio signals. The warped filter can be used as high-pass, low-pass, band-stop or band-pass filter based on the application desired. In some applications such as audio equalization [2], warped filters show better results than the Finite Impulse Response (FIR) filters. Another example for use of warped filter technique is in broadband signals for detecting band-pass signals [3]. A second-order filter transformation is used for designing the adaptive warped filter, resulting in band-pass responses of fixed bandwidth. However, filter coefficients require to be updated whenever the bandwidth has to be modified. This will demand a large memory for the read operation and the write operation. A design of filter bank using the warped technique for digital hearing aid [4] is proposed with the help of high-pass and low-pass filters in a parallel configuration. The design uses all-pass configuration of the second order. Various numbers of approaches for the VDF implementation are available. The linear phase characteristics [1] of this filter make it suitable for communication applications. However, it is not preferred for audio applications due to a small range of band-pass frequency and has higher complexity when compared to the warped filter. Drawbacks of this design are that only a finite set of cut-off frequencies can be adopted. Also, the filter structure or the filter coefficients require to be updated to procure the band-stop or band-pass responses.

The major drawback in this design is that it works only for a particular application by setting a particular cut-off frequency required for the desired application. For an audio application, it works as a high-pass filter; for another application, it works as a band-pass filter. Another drawback is that it requires second-order transformations for some of the applications.

In this paper, the Sect. 2 elaborates on the currently existing filter systems and their advantages and disadvantages. In Sect. 3, we discuss the modified proposed design for the warped filter. Section 4 discusses the results obtained on implementing the modified design. Section 5 deals with conclusion of the research work.

2 Background Study

2.1 Warped Filter

A FIR filter is considered as the prototype filter. The warped filter is a modified version of the FIR filter wherein the delay element is replaced by a single-stage all-pass transformation. The warping coefficient, α, is used in the transformation. When $-1 < \alpha < 0$, a backward transformation is observed. While $0 < \alpha < 1$, the transformation is forward. A warped filter is designed by first implementing an Nth order FIR filter having cut-off frequency of $fc0$ and having coefficients $h0$, $h1$, $h2\ldots$, hN [1]. The delay element in the FIR filter is then changed to the architecture shown

in Fig. 1. This is termed as $A(z)$. The cut-off frequency is varied, by varying α. If $\alpha = 0$, then the warped filter works as the ordinary FIR filter.

When band-stop or band-pass responses are to be achieved, the single-stage all-pass transformation [1] is unable to do so as a single parameter α is not sufficient. Another issue is that for varying the responses for different applications the coefficient needs to be updated in every trial, which in turn increases the memory occupancy for the write and the read operations. In order to incorporate the transformations from one type of the filter to another, both first-order transformation and second-order transformation will be required, which in turn will make the overall filter design very complex.

To overcome these issues, an efficient warped filter is to be designed, which does not require the updating of the filter coefficients for every high-pass to band-pass transformation or vice versa.

The block diagram of the single-stage all-pass filter is illustrated in Fig. 1. This is the structure to be placed instead of the delay element in the FIR filter.

2.2 *Coefficient Decimation Technique*

In the CDM technique, a constant coefficient method is used. A decimated version [5] of the frequency response is originally used. In this technique, an integer decimation factor M is used, such that every Mth coefficient is grouped and the remaining coefficients in between are discarded.

Figure 2 illustrates the VDF design for a fourth-order warped filter, where the new replaced delay element is incorporated in the design. In this design, α is the warping coefficient and select lines *sel_m*1, *sel_m*2 are the enabled signals to the multiplexers which help decide the type of filter to be used, i.e. low-pass filter, high-pass filter, band-pass filter or the band-stop filter.

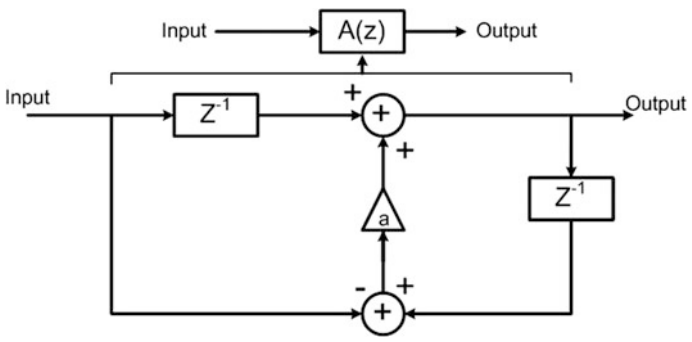

Fig. 1 Single-stage all-pass filter

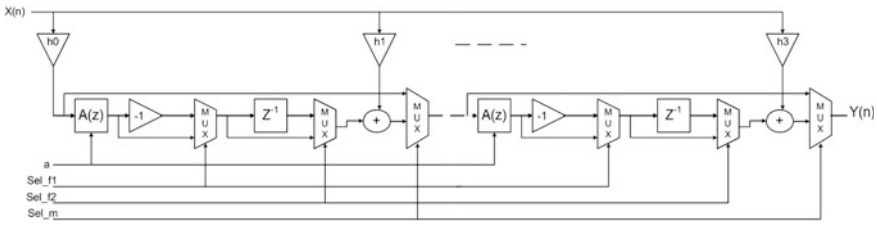

Fig. 2 Proposed warped filter design

3 Proposed Work

In this research work, we designed different types of adders to identify the most efficient adder in terms of area and power. An efficient multiplier is also implemented and incorporated in the VDF design, in order to get a performance efficient warped filter.

3.1 Ripple Carry Adder (RCA)

An RCA is implemented by using full adders cascaded in series [6]. A sum and a carry are generated from each of the full adders, and the carry generated from each stage is carried over to the next full adder stage. Thus, the carry bit is propagated serially.

Figure 3 illustrates the ripple carry adder with serially propagated carry.

3.2 Carry Skip Adder (CSkA)

In this adder, the carry is skipped as suggested in the name of the architecture. This results in speeded up addition. The carry bit is propagated around the portion of the

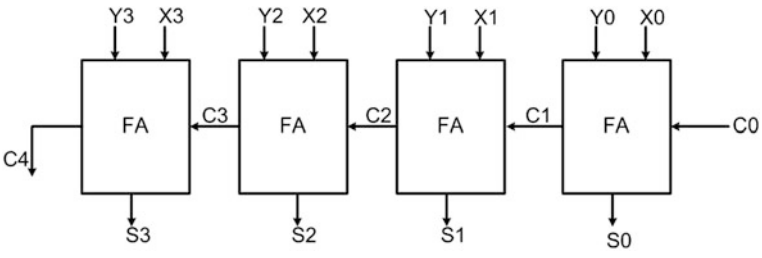

Fig. 3 Ripple carry adder

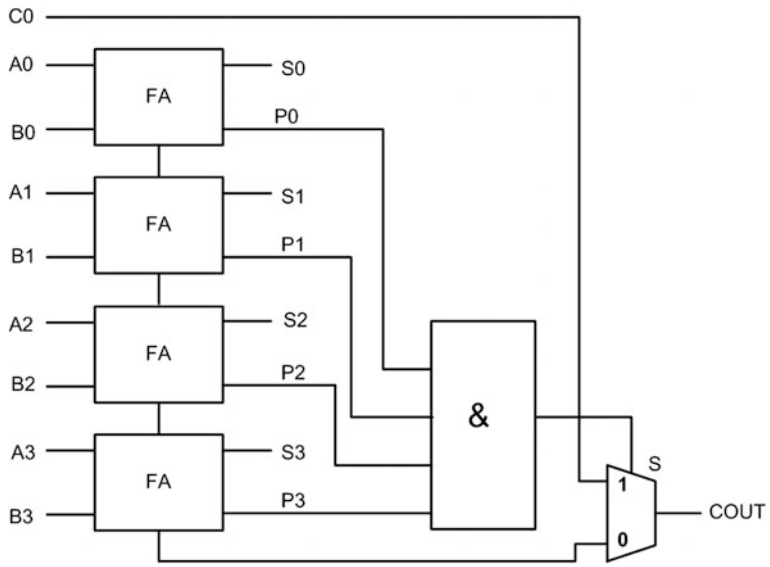

Fig. 4 Carry skip adder

entire adder [7]. This circuitry uses two gates. The AND gate compares the carry bit with the propagated signal.

Figure 4 demonstrates the carry skip adder with the carry skip logic.

3.3 Carry Increment Adder (CIA)

The CIA architecture uses a RCA block cascaded an incremental circuit. The incremental block is designed using series of half adders sequentially. Since four-bit addition is required for this application, one four-bit ripple carry adder along with the incremental circuitry is sufficient for generating the four-bit sum and a carry.

Figure 5 illustrates the block diagram of the CIA using the incremental circuitry. The RCA block in the figure represents a four-bit ripple carry adder, with the carry in bit assumed to be zero initially.

Figure 6 shows the internal circuitry of the incremental circuit consisting of sequentially connected series of half adders.

3.4 Carry Look Ahead Adder (CLA)

The Carry Look Ahead (CLA) adder is designed based on a concept of looking at lower adder bits of argument [8] and checking if higher order carry gets generated.

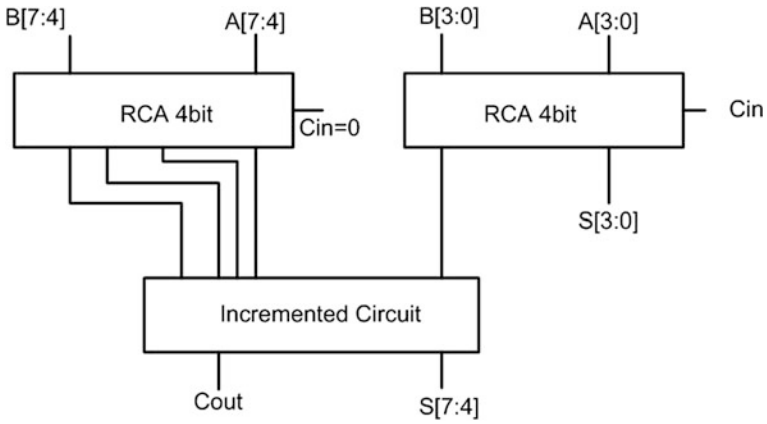

Fig. 5 Carry increment adder

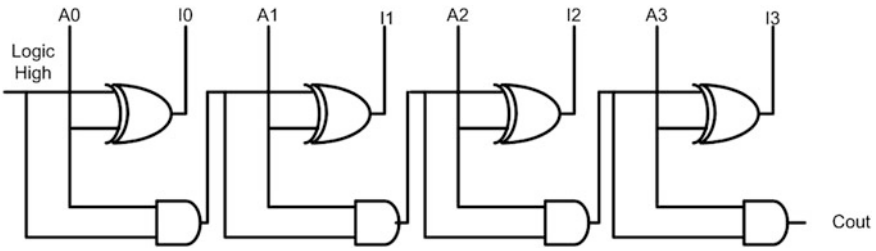

Fig. 6 Incremental circuit

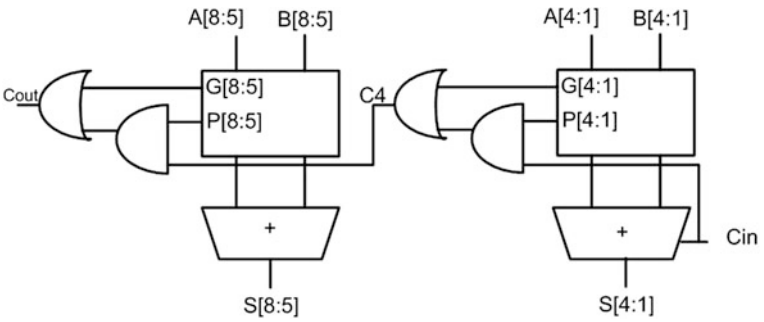

Fig. 7 Carry look ahead adder

The generation and propagation values are computed separately, and the internal carry is calculated in the following stage. The sum is calculated in the final stage.

Figure 7 illustrates the CLA along with its generated and propagated bits.

3.5 Carry Save Adder (CSA)

In this architecture, three input bits are parallelly added. The carry bit is not propagated in the following stages, and instead it is stored in the present stage [7]. In the next stage, the addend value is updated.

Figure 8 shows a detailed block diagram of the CSA, with the carry saving architecture.

3.6 Carry Select Adder (CSlA)

This architecture utilizes independent carry and sum generation units. The carry bit is propagated as $C_{in} = 0$ in one block and $C_{in} = 1$ in another block. A multiplexer is used to choose the required block and pass the output to the consecutive stage.

Figure 9 illustrates the structure of the carry select adder with the use of a multiplexer for choosing the block with the corresponding C_{in} bit.

A multiplier for speeded multiplication is also designed in order to make the filter more efficient.

3.7 Baugh-Wooley Multiplier

The Baugh-Wooley multiplier is a signed multiplier. It uses the concept of 2's complement addition. The Baugh-Wooley algorithm is widely used because of the ability to maximize the multipliers regularity, and it allows positive signed partial products [9]. In order to avoid negative weighted partial product bits, the matrix is entered with extra bits, and this in turn increases the efficiency of the multiplication to be performed. The architecture makes use of two basic blocks named the white cell and grey cell.

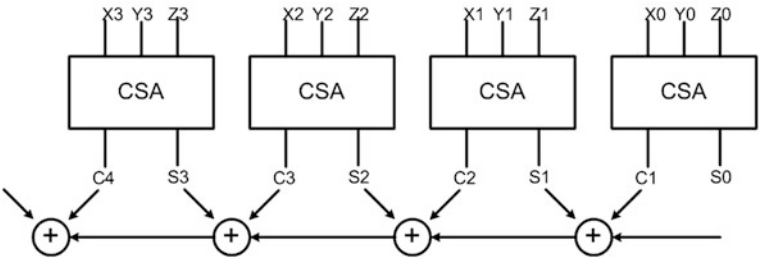

Fig. 8 Carry save adder

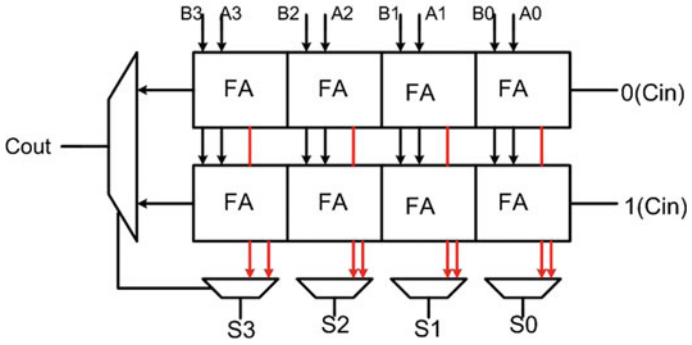

Fig. 9 Carry select adder

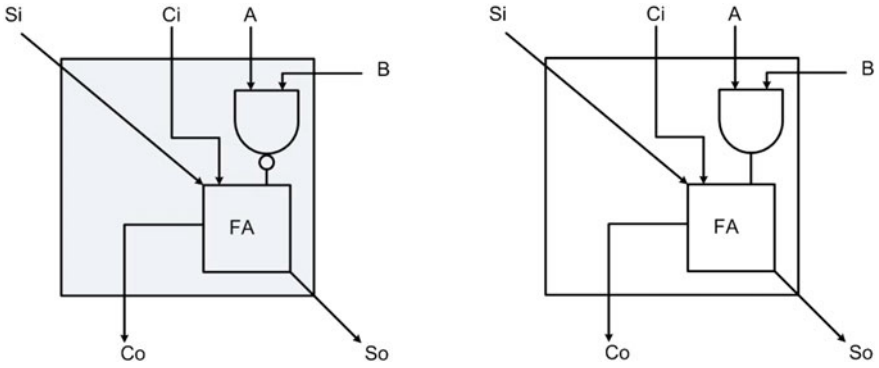

Fig. 10 Grey cell and white cell

There is a minor difference in the two architectures of the cells: the grey cell uses a NAND logic gate to feed in the inputs to the full adders, while the white cell uses AND logic gate output as the input to the full adder in the next stage.

Figure 10 gives the detailed internal diagram of the grey cell and white cell used in the Baugh-Wooley multiplier.

Figure 11 shows the basic structure of the Baugh-Wooley multiplier. A series of cascaded serial fall adders are used in the final stage of the multiplier.

3.8 Proposed Filter

The proposed warped filter is designed by replacing the adder with a Carry Look Ahead adder and the multiplier by the signed Baugh-Wooley multiplier. The adder used in this design is as illustrated in Fig. 7, and the multiplier block is illustrated

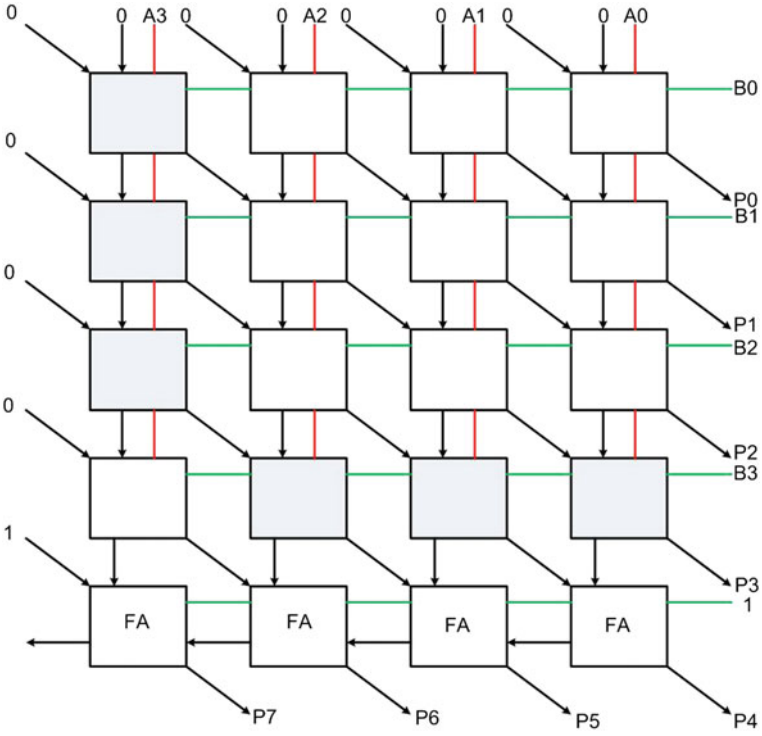

Fig. 11 Baugh-Wooley multiplier

in Fig. 11. Since the design is replaced by blocks using less area, the proposed filter is expected to use comparatively less area and also less time to be executed. The block diagram for the proposed filter is the same as shown in Fig. 2, with replaced adder and multiplier.

4 Results and Discussion

4.1 Simulation Tool

The coding style used for implementing this filter is Verilog Hardware Description Language. The tool used for simulation is Xilinx ISE. Cadence tool, RC Compiler is used to calculate the power, area and delay of the circuits. The simulation output of the different adders is illustrated below.

4.2 Performance Analysis of Adders

The different adder designs are simulated in the Cadence environment to verify their functionality. The performance analysis is performed in the RC compiler. Synthesis of the designs gives a detailed report of the area, power, timing and gates report. A comparison of the performance of adders is tabulated.

Table 1 analyses the performance of the different configurations of the adders based on the power consumed, area utilized and the delay incurred during the implementation of each of the adder architectures. From the report, it is evident that the ripple carry adder requires least number of cells. However, when considering optimization of both area and delay, the Carry Look Ahead adder is the most feasible adder. Hence, the proposed design of the warped filter is designed using the Carry Look Ahead adder.

It is deduced from the table that the CLA consumes less area when compared to the carry select adder by approximately 35%. When comparing the carry increment adder with the CLA, the latter performs better by 47% in terms of area utilization. The Carry Save Adder requires 31% more time than the Carry Look Ahead adder. The Carry Look Ahead adder is 25% faster than the ripple carry adder. Considering area utilization and the delay in performance, the Carry look Ahead adder is more efficient than the other adders. Therefore, CLA is preferred for the proposed filter.

4.3 Performance Analysis of Baugh-Wooley Multiplier

The Baugh-Wooley multiplier is proven to be among the fastest and most efficient multipliers in date.

This multiplier is most widely used in signed bit multiplication.

Table 2 discusses the amount of power consumed by the multiplier, the delay observed during simulation and the area required or the number of gates utilized.

Table 1 Performance analysis of various adders

Adder type	Power (nW)	Delay (ps)	Area (cells)	No. of gates
Ripple carry adder	24532.472	1103	652	28
Carry select adder	62427.884	1269	1711	76
Carry increment adder	42155.906	1564	838	36
Carry look ahead adder	30201.191	822	838	34
Carry skip adder	28583.007	1269	780	33
Carry save adder	45182.122	1197	1071	46

Table 2 Performance analysis of the multiplier

Multiplier type	Power (nW)	Delay (ps)	No. of gates
Baugh-Wooley	5172.522	172	16

Table 3 Performance analysis of conventional and modified filter

	Area (cells)	Delay (ps)	Power (nW)	Gates
Conventional filter	5252	4539	1541488.49	178
Modified filter	4072	4222	1168394.41	200

4.4 Performance of Filter

The conventional filter is compared with the modified design and the results are tabulated.

Table 3 shows the performance results of both the conventional and the modified filter designs. It is observed that the power of the modified filter is reduced by 24%. However, the number of gates required for implementing the modified design is increasing by 12%. The area utilization in the modified filter is less than the area utilized in the conventional design. The delay observed in the conventional filter is more than the delay observed in the modified filter.

5 Conclusion

The VDF proposed in this paper is a more efficient one in terms of performance with respect to the area and power. The adder selected in order to make the warped filter area efficient is the Carry Look Ahead adder. The signed Baugh-Wooley multiplier is used to speed up the multiplications inside the filter. The final filter is designed such that the entire design works with a single-stage all-pass transformation allowing the user to transform from one type of the filter to another based on the application desired. The area utilization has reduced by 22%, and the delay has reduced by 9%.

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Design of Arithmetic and Logic Unit (ALU) Using Subthreshold Adiabatic Logic for Low-Power Application

Anagh Deshpande and T. Vigneswaran

Abstract As density and size of VLSI chips still increase, the power consumption has become an important concern. The CMOS circuit with nominal supply voltage operating in high frequency consumes more power. The fashionable applications like mobile systems, sensing element networks need low power consumptions. In subthreshold logic, the circuit operates with voltage which is below transistor threshold voltage and it utilizes the subthreshold current as operating current. Adiabatic logic can even enforce in subthreshold regime to cut back dynamic power consumption considerably. ALU is one in all basic block within the low-cost electronic equipment. It consumes heap of power by continuous computation. So, it's important to cut back power consumption for higher performance. During this work, Arithmetic and Logic Unit is designed by subthreshold adiabatic logic and standard CMOS logic. The performance of ALU designed by subthreshold adiabatic logic is compared with standard CMOS logic. In order to simulate the circuits, Cadence virtuoso environment is used for 180 nm technology.

Keywords Subthreshold adiabatic logic (SAL) · Arithmetic and Logic unit (ALU)

1 Introduction

According to Moore's Law, due to increase in density, there is also increase in chip area as well as in the power dissipation of it. Hence, it has been turned into requirement for degrading the power dissipation with high-speed performance.

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The static CMOS logic is the previously known popular robust one, but it has a major debit of leakage current and slow performance. Here, dynamic logic style is the high-performance circuit with low power dissipation, but that compromises with its robustness.

In subthreshold logic, circuit works with a supply V_{DD} which is lesser than threshold of transistor. In saturation region, CMOS logic consumes more power as compared to same logic operating in subthreshold region.

In order to cut down dynamic power expenditure, the adiabatic logic can be used which has strong inversion without affecting noise immunity. These circuits attain ultralow energy consumption maneuvering by reprocessing the energy which is stored in their capacitive loads, particularly at low-frequency area.

In this paper, Sect. 2 covers background details of this research work and deals about understanding of subthreshold adiabatic logic and analysis of power dissipation of different gates. Section 3 describes power analysis and explanation of Arithmetic and Logic unit. The conclusion is offered in Sect. 4.

2 Background Study

2.1 Adiabatic Logic

The reversible logic effectuation in CMOS technology in order to denigrate the current guide for lesser energy diminishing is known as adiabatic Logic. This is attained by reprocessing circuit energy instead of diminishing its nearby area. This is good for CMOS, as input in addition with output charges are kept distinguished, in order to denigrate leakage power and current. In comparison with pass transistor logic, adiabatic logic effectuations of CMOS can be used for amelioration in power consumption. The adiabatic logic wants the use of ramp signal rather than faster varying signal to attain the required function.

There are two problems that have got to be self-addressed in any CMOS adiabatic logic. The use of energy efficient style and clock source which reduces the united power of the circuit. Next, in order to fulfill bijective demand, reversible logic needs more logic overhead. Hence, energy diminished by change of circuit should be checked and reprocessed rather than denigrated in the surroundings. The energy waste is decremented via employment of ramp function rather than quicker shift accomplished in step function.

Hence, transistors could also be employed in adiabatic operation, in spite of being incontestable as lossy devices, and is accomplished via effectuation of two rules. The transistor should usually turns on when there is a current flow through it. Next, once there is a big distinction supply and drain voltages, transistor should be off.

2.2 Subthreshold Adiabatic Logic (SAL)

In this logic, ramp signal is supplied instead of V_{DD} at source end (PMOS) and drain end (NMOS) in order to work as adiabatic logic. The PMOS and NMOS are kept at subthreshold region to achieve subthreshold adiabatic logic.

When the output of any gate is 1, the output follows the ramp signal [1] which is shown in Figs. 1, 2, and 3.

2.2.1 MOSFET Model in Subthreshold Region

At subthreshold region, V_{gs} is very very low than V_{th} which results in reducing the power consumption of the devices and having leakage current as drain source current of MOSFET transistors.

The I–V characteristics of the subthreshold PMOS device can be expressed by

$$I_S = I_o \exp\left(V_{GS} - |V_T|/n_p V_T\right)\left(1 - \exp(-V_{DS}/V_T)\right) \quad (1)$$

where $I_o = 2n_p\, u_p\, C_{ox}(W/L)V_T 2$. V_{GS}, $V_{DS,}$ and V_T are source to gate and drain and threshold voltage of PMOS, respectively. V_T is thermal voltage, n_p is subthreshold slope factor, and u_p is mobility of PMOS device. At subthreshold region, via body effect and drain-induced barrier lowering, V_T depends on V_{DS}.

So, for expressing threshold voltage following expression can be used:

$$V_T = V_{OT} - \gamma V_{BS} - \eta V_{DS} \quad (2)$$

where V_{OT} is the threshold voltage at zero bias, c is body effect coefficient and η is the drain-induced barrier lowering coefficient. Drain current varying exponentially with V_{GS} [2, 3].

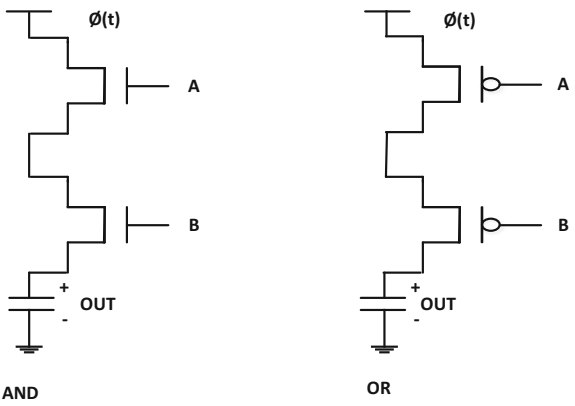


Fig. 1 AND and OR gate implementation in SAL logic

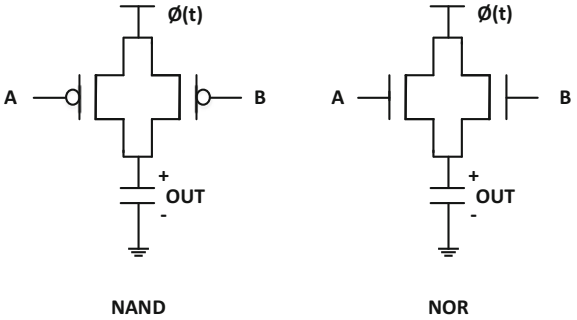


Fig. 2 NAND and NOR gate implementation in SAL logic

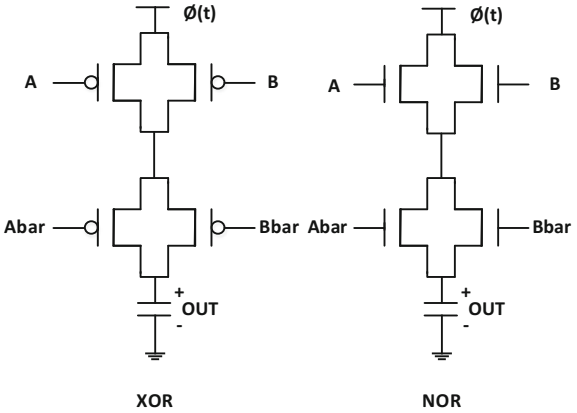


Fig. 3 XOR and XNOR gate implementation in SAL logic

This importantly less current induces a significant amount of reduction in power consumption as compared with saturation region operation. But, this delay in the circuit increases when this technique is implemented. As a consequence, speed of the circuit gets slower. Also, this technique is best operational at low-frequency range as in order to reduce the power consumption.

2.2.2 Effect of Parasitic Gate Capacitances on Varying Supply Voltage

The CMOS circuit operating in subthreshold region, the gate capacitance of MOSFET varies if the supply voltage increases or decreases [4, 5]. Owing to this, a very less number of energy is channelized from varying supply voltage to the inputs, inducing a non-adiabatic decay. At this stage, noise can be introduced due to non-adiabatic loss of energy. As MOSFETs are maintained below V_{DS}, throughout adiabatic switching, the best way to express (C_G) of PMOS device is as follows

Table 1 Power comparison

Gates	Power consumption	
	CMOS (μW)	SAL (nW)
XOR	1.667	463.1
XNOR	1.141	447.1
OR	1.081	18.41
AND	1.09	26.39
NAND	1.799	368.8
NOR	0.6	91.63
INVERTER	0.89	298.3

$$C_G = C_{GD} + C_{GS} \tag{3}$$

where C_{GD} and C_{GS} are the gate-to-drain and gate-to-source capacitances, respectively.

This can be presumed that the initial value of V_G and supply voltages maintained at zero. When the supplying voltage rages up, in very less time period, the gate voltage climbs up step by step from 0 to V_{DD}. So, in consequence, total C_G V_{DD} measure of charge runs to the gate node, making a 0.5 $C_G(V_{DD})^2$ J of energy dissipation.

Now, the power consumption of both CMOS and SAL logics are tabulated as follows.

As shown in Table 1, it is seen that power consumption in CMOS gates is much higher than in SAL gates.

3 Arithmetic and Logic unit (8 Bit)

ALU is an integral part of processor in modern integrated chips. ALU comprises of different functions such as addition, subtraction, multiplication, modulo, right and left shift as arithmetic functions while for logical function, it contains different gates circuits [6]. This paper implements the gates using SAL logic for arithmetic as well as logical operation. For logical operation, previously explained gates are used.

Now, to show the workability of SAL logic, 4-bit equality comparator is implemented as shown in Fig. 4.

In this circuit, if all bits of input signal are equal then only output will be validated [7, 8]. The power consumption comparison of above circuit in CMOS as well as SAL logic is tabulated as in Table 2.

Power dissipation in the comparator designed by CMOS gates is 579.4 μW while comparator designed by SAL gates consumes 8.93 μW average power.

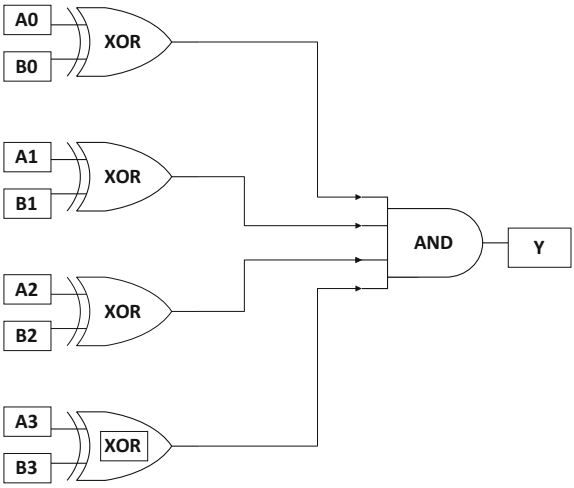


Fig. 4 4-bit magnitude equality comparator

Table 2 Power comparison

Module	Power consumption	
	CMOS (μW)	SAL (μW)
4-bit equality comparator	589.4	8.931

3.1 Schmitt Trigger

Schmitt trigger is a circuit useful in generating clean pulses from a noisy input signal or in the design of oscillator circuits. As explained in previous section, ramp signal is supplied instead of V_{DD} at source end (PMOS) and drain end (NMOS) in order to work as adiabatic logic. The PMOS and NMOS are kept at subthreshold region to achieve subthreshold adiabatic logic [9, 10].

When the output of any gate is 1, then in this logic output follows the supplied ramp signal. But in order to work, any transistor requires steady pulse input and that's where Schmitt trigger is required. As Schmitt trigger converts output ramp signal from any gate output and feeds to next gate, the desired output is achieved (Figs. 5 and 6).

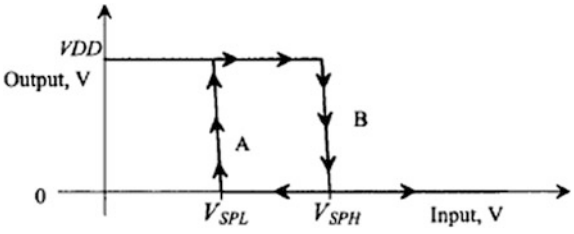
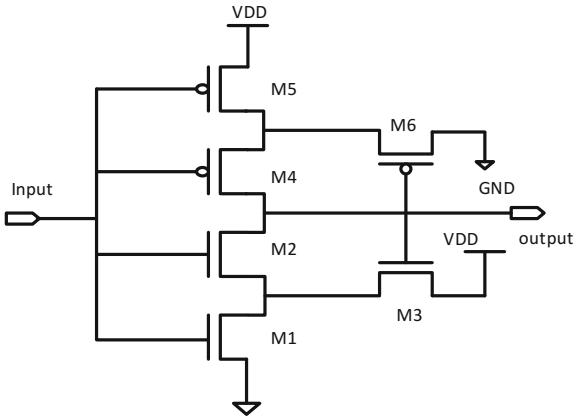


Fig. 5 Transfer characteristics of Schmitt trigger

Fig. 6 Schmitt trigger



In order to design Schmitt Trigger, the upper and lower switching points need to find out from the ramp signal. The equation for upper switching point is

$$W_1L_3/L_1W_3 = (V_{DD} - V_{SPH}/V_{SPH} - V_{TH})^2 \tag{4}$$

Similarly, for lower switching point,

$$W_5L_6/L_5W_6 = (V_{SPH}/V_{DD} - V_{SPL} - V_{TH})^2 \tag{5}$$

3.2 8-Bit Arithmetic and Logic unit (ALU)

8-Bit ALU is shown in Fig. 7.

Here, for logical operation, AND and OR gates are used. For arithmetic operation, adder circuit is devised. After each gate, one Schmitt trigger and one inverter are added in order to convert ramp signal into constant pulse signal. Inverter is necessary because the Schmitt trigger provides inverted pulse.

Finally, 4:1 MUX is applied to choose which function is wanted at the end of the output.

3.3 Power Dissipation Analysis

Module	Power consumption (average)	
	CMOS (mW)	SAL (mW)
8-bit ALU	11.67	4.508

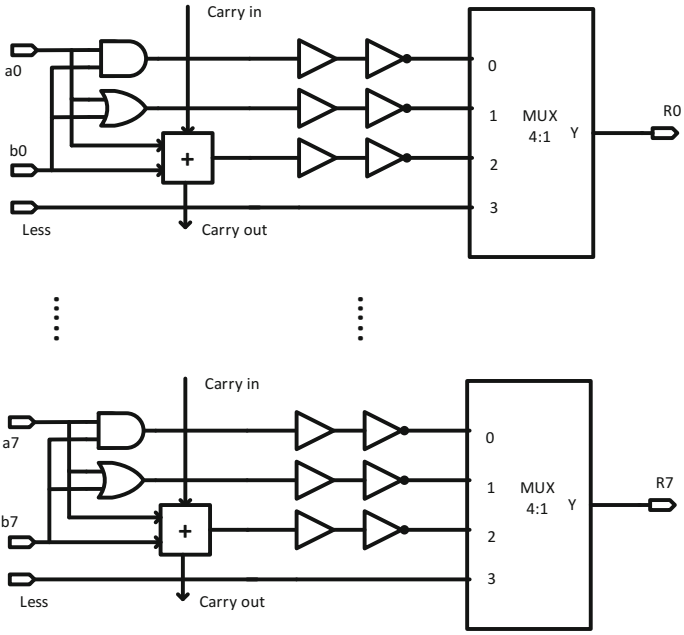


Fig. 7 8-bit ALU

From above table, it is concluded that Arithmetic and Logic unit designed by CMOS logic consumes 61.37% more power as Arithmetic and Logic unit designed by subthreshold adiabatic logic.

4 Conclusion

As number of transistors decreases in SAL, power consumption reduces. As compared with static CMOS, subthreshold adiabatic logic saves considerable amount of energy. In particular, the effect of parasitic gate capacitances on varying supply voltage has been discussed thoroughly in this paper. For applications which require low power consumption at lower operating frequency, subthreshold adiabatic logic (SAL) is very useful. Simulations using CADENCE SPICE Spectra and virtuoso at 180 nm technology are done in order to explain the workability of subthreshold adiabatic logic.

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Design of Sample and Hold for High-Speed Analog to Digital Converter

D. Patel Konarkkumar and P. Augusta Sophy Beulet

Abstract In remote sensing applications which mostly process graphic and video streams, data acquisition needs high speed and accurate ADC. ASIC implementation of ADC gives higher performance compared to discrete component. This report discusses the design of sample and hold for high-speed ADC with sampling speed of 250 MSPS. Report comprises implementation of Op-Amp and sample hold design. Op-Amp implemented using fully differential folded cascode topology gives more than 55 dB gain, unity-gain bandwidth of 500 MHz and phase margin of 50°. Sample and hold circuit is implemented using switched capacitor logic with dummy transistor. Design is tested against all the specification. Design has been carried out in cadence®. The designs are simulated in Cadence Virtuoso 6.1.5 with HSPICE simulator.

Keywords ADC · Op-Amp · Slew rate · Offset voltage · SH

1 Introduction

Most of the environmental signal in the world is in the analog form and is converted to analog voltage or current. There should be need of converting such a measurement into digital form so that all data can be processed or stored for further processing. Many digital signal processing circuits consist of high-speed ADC for such kind of conversation.

Mixed signal ASIC design reduces the overall power and area requirement as compared to discrete component. ADC is the main analog block in space application such as video processing, data acquisition system, bias generator. Sample and hold circuit is crucial component of high-speed ADC. It is very important to design CMOS implementation of ADC with reduced size and cost for space application. In sample and hold design, Op-Amp is the key component. In this

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report, various Op-Amp design configurations are compared and appropriate design is selected for implementation of various blocks of ADC.

2 Op-Amp Configurations

Op-Amps designed for high-speed data converter must satisfy the accuracy and fast settling specification. To achieve this design, Op-Amp needs high gain and high unity-gain bandwidth [1].

2.1 Telescopic Op-Amp

As technology scales down, further design of Op-Amp with high gain along with large unity-gain bandwidth is a challenging task. Telescopic Op-Amp gives high gain, and it takes less power compared to other Op-Amp configurations [1]. Figure 1 shows implementation of telescopic Op-Amp.

It gives high performance in terms of DC gain due to fact that the second pole depends on voltage at n-channel. This voltage is decided by p-channel device [2]. Telescopic Op-Amp output voltage swing is very less as the bottom transistor cuts the output swing from both sides of the Op-Amp.

2.2 Gain-Boosted Op-Amp

Gain-boosted Op-Amp configuration gives very high gain at the cost of lesser phase margin. Gain boosting does not affect output voltage swing. It comprises a gain-boosted amplifier [3]. P-stage- and N-stage-boosted amplifiers make the gate voltage and the drain voltage equal. To make gain bandwidth product constant, output resistance must be small. At larger frequency, output resistance is decreasing. The decrease in output resistance leads to increase in bandwidth. The increase in bandwidth alters gain bandwidth product.

Gain-boosted amplifier adds doublet pole and zero. This seriously affects the slew rate. For high-resolution ADC, slew rate limits the use with lower slew rate [4]. The basic configuration of gain-boosted Op-Amp is shown in Fig. 2.

2.3 Two-Stage Op-Amp

Two-stage Op-Amp comprises a differential amplifier with common source amplifier. First stage is used to get high gain, and second stage provides high output voltage swing [5].

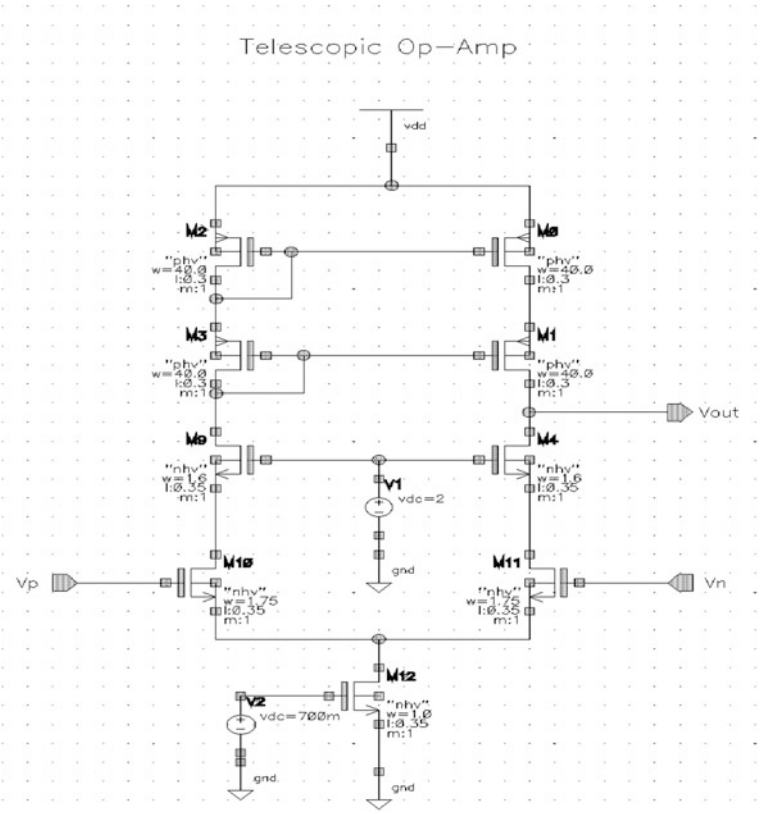

Fig. 1 Schematic of telescopic Op-Amp

First stage and second stage gain equations for gain-boosted Op-Amp can be written respectively as,

$$A_v = g_{m2} r_o \tag{1}$$

$$A_v = g_{m0}(r_{o13} \| r_{o3}) \tag{2}$$

Figure 3 shows the schematic of two-stage Op-Amp. Compensation technique is used to maintain stability when Op-Amp is used as a negative feedback. Two-stage Op-Amp configurations give two poles that are very close to each other.

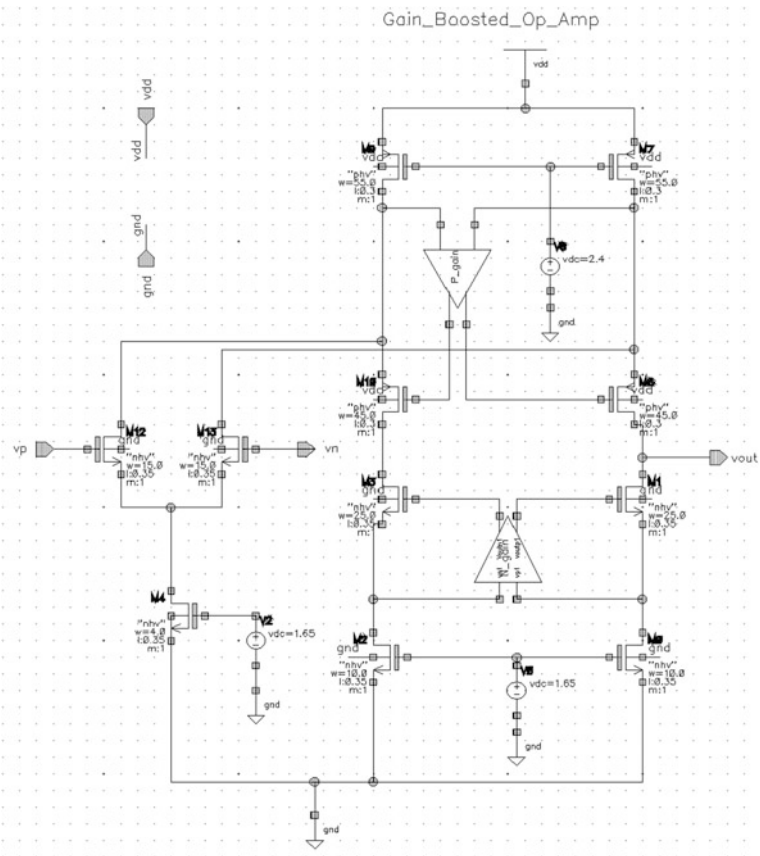

Fig. 2 Schematic of gain-boosted Op-Amp

2.4 Folded Cascode Op-Amp

Folded cascode Op-Amp offers high gain, high output resistance, and self-compensation. It consists of differential amplifier biased using current sink to provide constant current source [6]. Figure 4 shows the schematic of folded cascode Op-Amp. Here, load resistance is replaced with MOSFET device.

For 8-Bit ADC, we require a gain of 16 dB and to amplify this signal with 8-bit accuracy, open-loop gain of the amplifier is given as,

$$|V_{OL}| \geq 32 \cdot 16 = 512 \text{ V} = 54.18 \text{ dB}$$

Unity-gain frequency of folded cascode Op-Amp is calculated as,

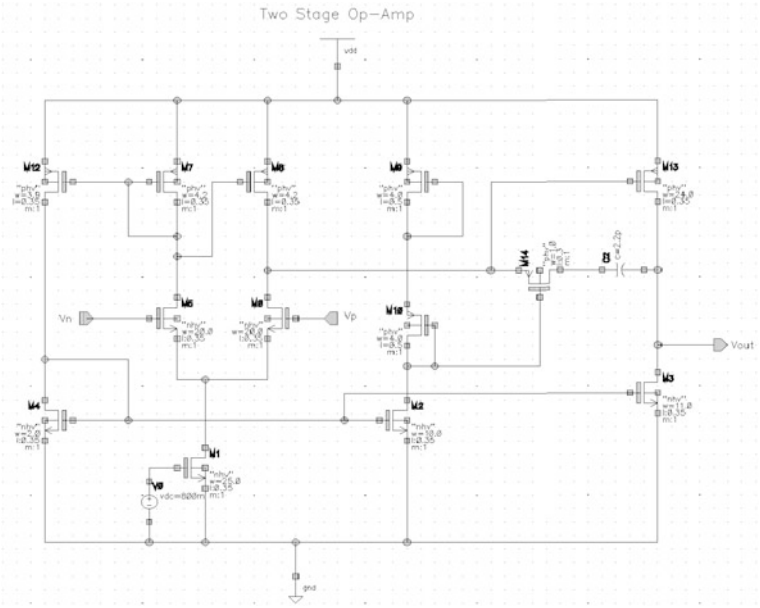

Fig. 3 Schematic of two-stage Op-Amp

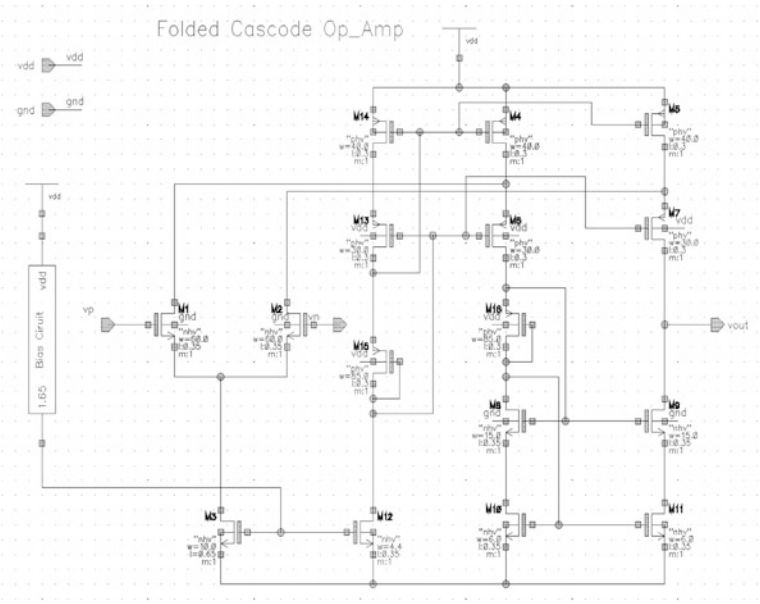

Fig. 4 Schematic of folded cascode Op-Amp

$$f_{\text{un}} \geq \frac{f_{\text{clk}} \times \ln 2^{N+1}}{2\pi \times \beta}$$

For $N = 8$ and $f_{\text{clk}} = 250$ MHz, $f_{\text{un}} \geq 500$ MHz.

Slew rate of an Op-Amp must be larger than 250 V/μs to chive 8-bit accuracy in ADC. Slew rate of an Op-Amp is given as,

$$I_3 = SR \times C_L \tag{4}$$

To avoid zero bias current in the cascode OPAMP, current at the drain terminal of M_4 and M_5 must be equal to,

$$I_4 = 1.2I_3 \text{ and } I_5 = 1.5I_3$$

The value of resister can be calculated as,

$$R_1 = \frac{V_{DS13(\text{sat})}}{I_{12}} \text{ and } R_2 = \frac{V_{DS8(\text{sat})}}{I_6} \tag{5}$$

Increasing the width of the driving transistor M_3, leads to more current. Larger current results increases the transconductance 'gm', there by increasing the gain. However increasing the width of M_3 so as to increase the current, limits the output voltage swing after a certain value.

3 Sample and Hold Design

In data acquisition system, sample hold is critical component. It samples the analog input during sample phase and holds the sampled value during hold phase. The hold value is used to convert the analog input to digital input [7]. Figure 5 shows the sample and hold architecture.

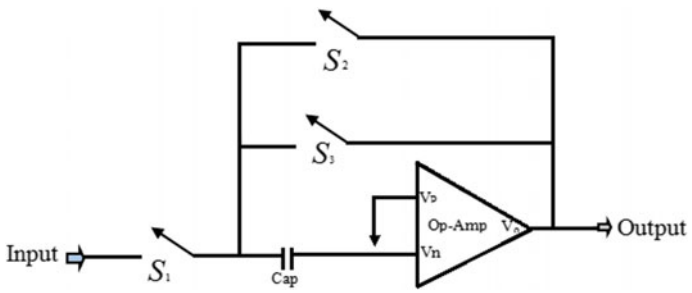

Fig. 5 Sample hold architecture

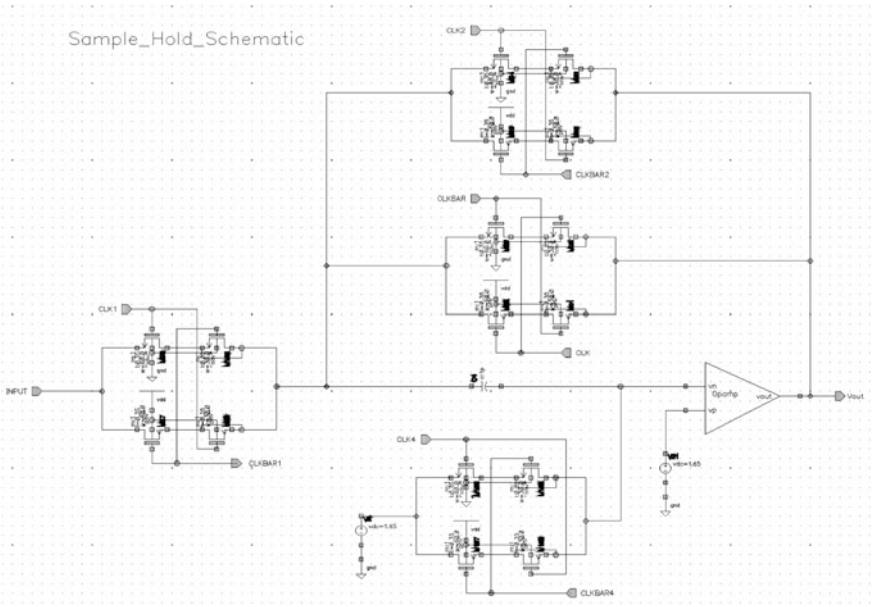

Fig. 6 Sample hold schematic

During rising edge of clock signal, switches S_1 and S_3 are closed . In this instant, data are latched from input to output so this instance is referred as sampled instance. When switch S_1 is closed capacitor charges towards the value of the input voltage. When inverted clock is applied, switches S_1 and S_3 are detached from the circuit. At the same time, S_2 starts conducting. The charge stored in the capacitor is applied to the Op-Amp through feedback. At this instance, 'data out' can be obtained from the sample hold circuit which is equivalent to the charge stored during sample phase. Figure 6 shows the schematic of sample hold. Switch of sample and hold is designed using transmission gate. Generated output may suffer from clock feed through effect and charge injection effect due to direct path between clock and output. It should be noted that during sampling phase finite amount of charge is stored in the transistor.

This charge requires finite amount of time to discharge. To eliminate these effects, dummy transistor with inverted clock is connected at each switch.

4 Simulation Result and PVT Analysis

For high-speed ADC, Op-Amp needs large gain, high phase margin, and less offset voltage. Telescopic Op-Amp gives high gain but the unity-gain bandwidth is very less. The gain-boosted stage of the differential amplifier improves the gain, but slew

Table 1 Op-Amp achieved specification

Parameter	Telescopic Op-Amp	Gain-boosted Op-Amp	Two-stage Op-Amp	Folded cascode Op-Amp
Gain (dB)	68.4	104.48	34.17 dB	57.877
3 dB bandwidth	9.57 kHz	350.9 kHz	138.5 kHz	1.3175 MHz
UGB	12.17 MHz	45 MHz	3.17 GHz	633 MHz
Phase margin	51.8°	49.1º	62.4º	60º
Slew rate (V/μs)	58.7	94	335.8	352.4
Settling time	3.4 ns	1.8 ns	768 ps	750 ps
CMRR (dB)	53.3	41.4	61.26	76
PSRR (dB)	45.7	35.25	54.25	54.27

rate of the gain-boosted Op-Amp limits its use for high-speed ADC. Two-stage Op-Amp accommodates advantage of high gain and high output voltage swing. Still its gain is not sufficient for high-speed design. Table 1 shows the achieved specification using different topology.

Folded cascode Op-Amp combines all the specification The balance of currents to the differential amplifier does not need exact balance as same excess current flow in and out of the current mirror sink.

For 8-Bit ADC with 250 MSPS speed, some specifications of Op-Amp against the achieved specification are listed in Table 2. Figure 7 shows the AC response of an Op-Amp. All parameters of Op-Amp are calculated by considering 1 Pf load at the output terminal of Op-Amp. The performance of the Op-Amp may vary with parameter variation during front-end and back end design.

In high-resolution ADC, design must be less sensitive to process, voltage, and temperature variation. PVT analysis is carried out to verify the design. Figure 8 shows the PVT analysis of Op-Amp with temperature range varying from −20° to 70°.

Table 2 Op-Amp specification for high-speed ADC

S. No.	Parameter	Required value	Achieved value
1	Gain (dB)	≥ 55	57.877
2	UGB (MHz)	≥ 400	633
3	Phase margin	≥ 50º	60º
4	Slew rate (v/μs)	≥ 250	299.3
5	CMRR (dB)	≥ 50	76
6	PSRR (dB)	≥ 45	54.27

Fig. 7 AC simulation of two-stage Op-Amp

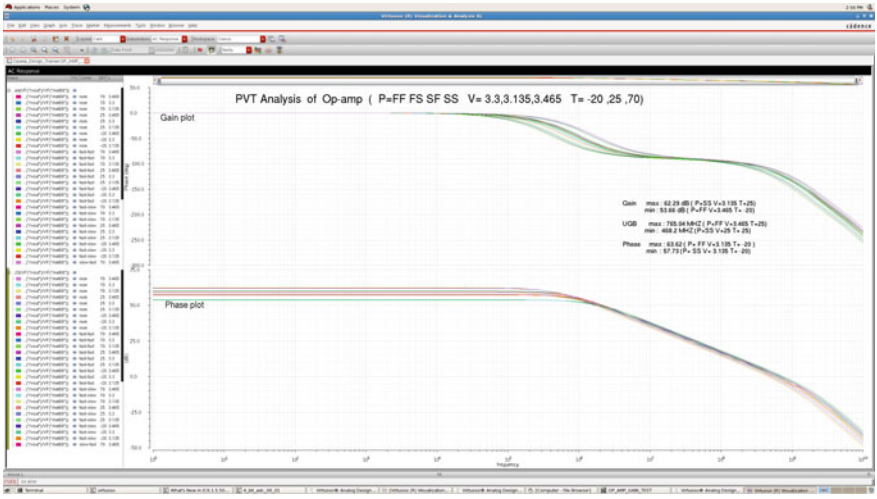

Fig. 8 PVT analysis of two-stage Op-Amp

Designed Op-Amp having lowest offset voltage gives high gain for all corners. The highest gain is 62.29 dB in slow-slow corner and the lowest gain is 53.66 dB in the fast-fast corner.

Figure 9 shows the simulation result of sample hold designed using folded cascode topology. High-speed ADC needs high-resolution sample and hold. For

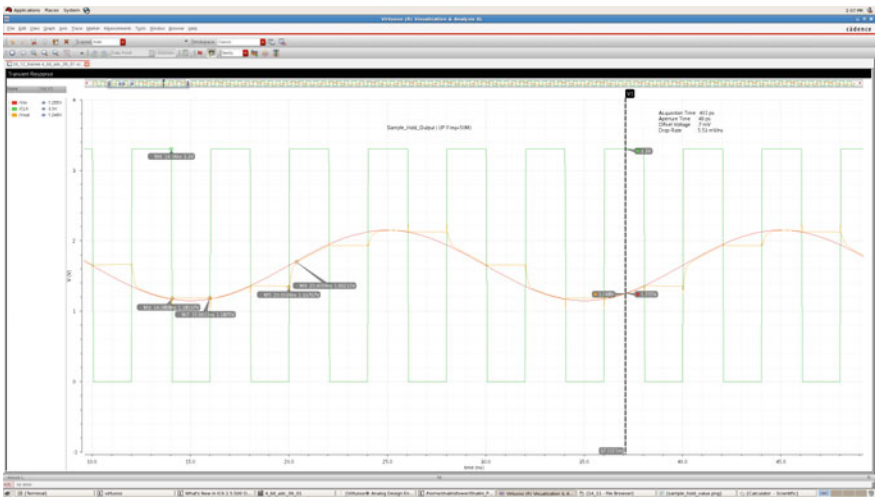

Fig. 9 Sample and hold output specification result

Table 3 Sample and hold specification

Parameter	Required specification	Achieved specification
Acquisition time	<2 ns	401 ps
Aperture time (ps)	<100	49
Droop rate (mV)	<10	7
Offset voltage (mV)	<25	5.53

this reason, sample and hold must meet certain specification such as aperture time, acquisition time, offset, and droop rate.

Acquisition time is the time required for the output of sample and hold to reach sampling value after initiation of sampling instance. Droop rate is the ratio of change in the output voltage with respect to change in time during hold phase. Table 3 shows the achieved specification against the 8-bit ADC specification.

PVT analysis of sample and hold with temperature range varying from −15° to 80° is shown in Fig. 10. The design is tested with load of 1 pF load and 40 MHz input frequency. The design is started with goal of designing high-speed ADC with 250 MSPS speed. So the clock period of 4 ns is given at the input of the sample and hold.

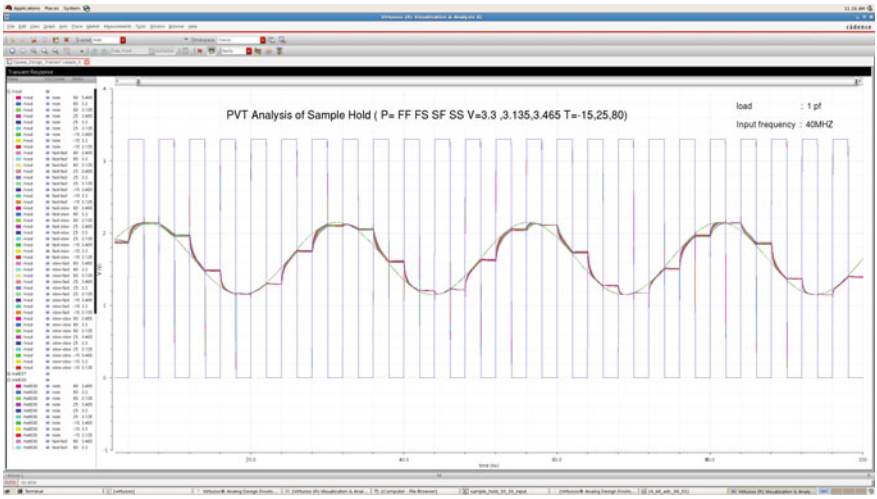

Fig. 10 PVT analysis of sample and hold

5 Conclusion

Designed folded cascode Op-Amp with special current sink improves the gain and offset voltage. Sample and hold designed using this topology of Op-Amp gives satisfactory result against the 8-bit ADC specification. The simulation result of sample and hold shows that the designed Op-Amp can be used for high-speed 250 MSPS ADC. Further PVT analysis shows that the design can be able to sustain with parameter variation such as temperature voltage and process. All designs are verified using cadence® 180 nm technology.

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FPGA-Masked S-Box Implementation for AES Engine

Maneesha Jayakumar

Abstract

Objective: The paper proposes a high-throughput masked AES engine which helps to avoid differential power analysis attacks on data without compromising the performance. It also optimizes the area for AES. Methods: The AES implemented includes mapping operations from GF(2^8) to GF(2^4). The masking is implemented using Boolean masking which provides masking at the algorithmic level and assures secret sharing property. Boolean masking uses XOR operations on plain text or intermediate values which masks these original data. The work includes implementation of AES and masked AES using Verilog in FPGA.
Findings: The Boolean masking using XOR operations masks the original values making output independent of the input which in turn avoids correlation between power and input values. This enables weakening of DPA attack. Use of XOR operations does not bring any noticeable variation in performance, area and timing requirements.
Applications: The masking technique randomizes the output of the AES for every execution using different mask values. This randomization improves reduction of relation between power consumption of output and input data. Thus, the leakage of data using differential power analysis reduces. Hence, the encryption process becomes DPA attack resistant.

Keyword Differential power analysis

1 Introduction

Every modern application requires a large amount of data storage. This data in storage network may get transparent leading to leakage of information. The leakage is possible using some properties such as power consumption, timing and fault

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detection. Several masking methods are developed to remove DPA attacks for the AES implementation. The paper presents S-box masking of AES using Boolean masking which prevents DPA and glitch attacks. Masking is the process of randomizing the values of the data to be stored. This brings uncorrelation between power consumption and intermediate data which is made possible by removing relationship between output and input of AES. The paper explains the implementation of AES followed by implementation of the masked AES. The implementation of masked AES is explained towards the ending of the paper.

2 S-Box Implementation

In AES algorithm [1], the elements undergo four transformations—AddRound Key, SubByte, ShiftRow and MixColumn. Among the four transformations, SubByte is the only nonlinear byte substitution. The work includes the mapping of the S-box of AES algorithm. S-box architecture is constructed using first multiplicative inverse [2] computation and then the affine transformation. The general block diagram for the path of the data in multiplicative inverse operation is given in Fig. 1.

2.1 Isomorphic and Inverse Isomorphic Mapping

The operation isomorphic δ includes mapping [3, 4] of elements based on GF(2^8) to GF(2^4). Inverse isomorphic mapping δ^{-1} is used to map the result of multiplicative inverse which is in GF(2^4) to its equivalent GF(2^8). Both functions can be represented as an 8×8 matrix. Let q be the element in GF(2^8) where $q7$ is the MSB and $q0$ is the LSB and k output. The equations for isomorphic mapping are given in Table 1. Inverse isomorphic mapping equations are given in Table 2 where input is denoted by q and output with k.

2.2 Addition

Addition operation in the multiplicative inverse is performed using bitwise XOR operation between the two elements.

2.3 Squaring (X^2)

Let the input be q and output of the squaring function be k, which are of 4 bits and $k = q^2$. The equations for squaring are given in Table 3.

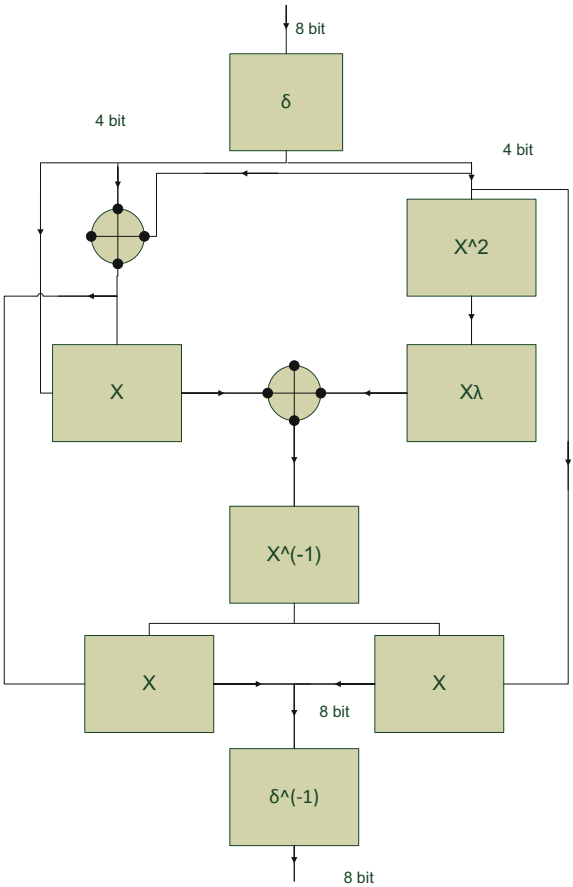

Fig. 1 Multiplicative inversion module

Table 1 Equations for isomorphic mapping

$k0 = q6 \hat{} q1 \hat{} q0;$
$k1 = q6 \hat{} q4 \hat{} q1;$
$k2 = q7 \hat{} q4 \hat{} q3 \hat{} q2 \hat{} q1;$
$k3 = q7 \hat{} q6 \hat{} q2 \hat{} q1;$
$k4 = q7 \hat{} q5 \hat{} q3 \hat{} q2 \hat{} q1;$
$k5 = q7 \hat{} q5 \hat{} q3 \hat{} q2;$
$k6 = q7 \hat{} q6 \hat{} q4 \hat{} q3 \hat{} q2 \hat{} q1;$
$k7 = q7 \hat{} q5;$

2.4 Multiplication with Constant λ (Xλ)

Let the input be q and output of the multiplication with the constant be k, which are of size 4 bits and $k = q\lambda$. The equations for this operation are given in Table 4.

Table 2 Equations for inverse isomorphic mapping

$k0 = q6\hat{}q5\hat{}q4\hat{}q2\hat{}q0;$
$k1 = q5\hat{}q4;$
$k2 = q7\hat{}q4\hat{}q3\hat{}q2\hat{}q1;$
$k3 = q5\hat{}q4\hat{}q3\hat{}q2\hat{}q1;$
$k4 = q6\hat{}q5\hat{}q4\hat{}q2\hat{}q1;$
$k5 = q6\hat{}q5\hat{}q1;$
$k6 = q6\hat{}q2;$
$k7 = q7\hat{}q6\hat{}q5\hat{}q1;$

Table 3 Equations for squaring

$k0 = q3\hat{}q1\hat{}q0;$
$k1 = q2\hat{}q1;$
$k2 = q3\hat{}q2;$
$k3 = q3;$

Table 4 Equations for multiplication with constant

$k0 = q2;$
$k1 = q3;$
$k2 = q3\hat{}q2\hat{}q1\hat{}q0;$
$k3 = q2\hat{}q0;$

2.5 *GF(2^4) Multiplication* (X)

GF(2^4) consists of hardware which includes GF(2^2) multiplication. The hardware implementation is shown in Fig. 2 which acts on two four-bit inputs to GF(2^4) multiplication. Let the inputs for GF(2^2) be 2-bit q and w and the output 2-bit k. The equations for GF(2^2) are given in Table 5.

The equations for multiplicative inversion (X^{-1}) are given in Table 6.

3 AES Implementation

The AES algorithm consists of fixed block size of 128 bits. The plain text which is given as the input to AES is represented as a 4×4 matrix called state. Each byte in the state denoted by $S_{i,j}$ ($0 \leq i, j < 4$) is represented as an element of GF(2^8). Each operation of encryption algorithm of AES can be explained as follows.

3.1 *AddRound Key*

The AddRound key performs bitwise XOR operations.

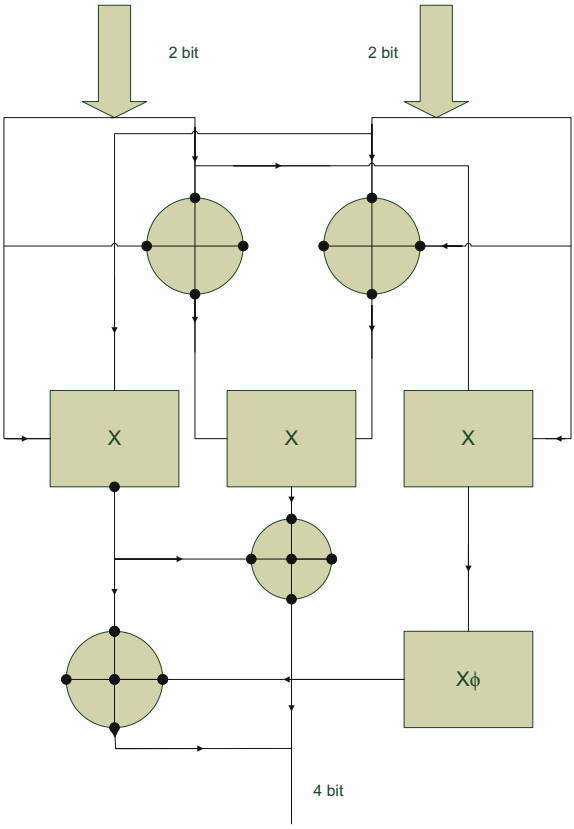

Fig. 2 Hardware implementation of GF(2^4) multiplication

Table 5 Equations for GF(2^2)

$k0 = q1w1 \hat{} q0w0;$
$k1 = q1w1 \hat{} q0w1 \hat{} q1w0;$

Table 6 Equations for multiplicative inverse

$q^{-1}0 = q3q2q1 \hat{} q3q2q0 \hat{} q3q1 \hat{} q3q1q0 \hat{} q3q0 \hat{} q2 \hat{} q2q1 \hat{} q2q1q0 \hat{} q1 \hat{} q0;$
$q^{-1}1 = q3 \hat{} q3q2q1 \hat{} q3q1q0 \hat{} q2 \hat{} q2q0 \hat{} q1;$
$q^{-1}2 = q3q2q1 \hat{} q3q2q0 \hat{} q3q0 \hat{} q2 \hat{} q2q1;$
$q^{-1}3 = q3 \hat{} q3q2q1 \hat{} q3q0 \hat{} q2;$

3.2 ShiftRows

ShiftRows perform shifting operation where except the first row other rows of the state are cyclically shifted one byte, two bytes, and three bytes to the left, respectively.

3.3 *MixColumn*

The computation performed on the state in MixColumn [1, 5, 6] operation can be expressed by the equations shown in Table 7.

The paper presents implementation of one round of AES which has the steps included as shown in the AES algorithmic structure shown in Fig. 3.

4 Masked AES Implementation

Masking is the methodology adopted to improve the DPA resistance of a cryptographic device. Side channel attacks relate the leakage of information hidden, using some physical implementation features such as power, time. The masking preferred for nonlinear operations like S-box is arithmetic masking. As the arithmetic type may lead to faults in masking 0's, Boolean masking is implemented in both linear and non-linear operations of AES. Boolean masking uses simple Boolean operations like XOR operations which enable easy masking by bringing change only in the algorithmic level of the encryption system [7, 8]. The objective of masking is to make outputs independent of input which indirectly leads to lack of correlation between power and inputs. This procedure helps to avoid DPA attack. The masking turns the original data v into masked value v_m using 8-bit mask value r. This ensures secret sharing where there is a need of knowing both the v_m and m which will be unknown to the attacker to decode v.

The masking implementation is performed using a random number r. The steps used for masking can be explained as follows:

(i) Each byte of the input M is xored with the mask value r. The respective output undergoes multiplication with r.
(ii) The output of first step is xored with the multiplication output of r with itself.
(iii) This output becomes input for multiplicative inverse module of SubByte transformation which generates an output that gets xored with value 1.
(iv) The output of third step is xored with r and becomes input for the affine transformation. This operation generates output $M1$.

Table 7 Equations for MixColumns

$$\begin{bmatrix} S'0,c \\ S'1,c \\ S'2,c \\ S'3,c \end{bmatrix} = \begin{bmatrix} 02 & 03 & 01 & 01 \\ 01 & 02 & 03 & 01 \\ 01 & 01 & 02 & 03 \\ 03 & 01 & 01 & 02 \end{bmatrix}_{Hex} \begin{bmatrix} S0,c \\ S1,c \\ S2,c \\ S3,c \end{bmatrix}$$

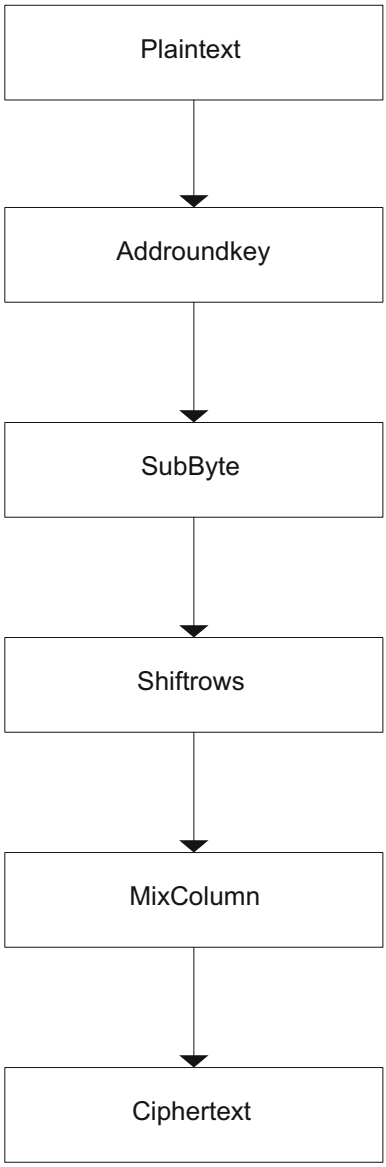

Fig. 3 AES encryption structure for one round

(v) $M1$ is xored with the affine transformation of r, i.e. ra.
(vi) The output of the xor operation mentioned in step-v, undergoes operations such as ShiftRows and MixColumns to generate $M3$ which is again xored with ra.

As SubByte is the only nonlinear transformation, the masking done in this stage is with a complex arithmetic which has the flow of the operations as shown in Fig. 4. The one round of AES encryption algorithm is masked as shown in Fig. 5.

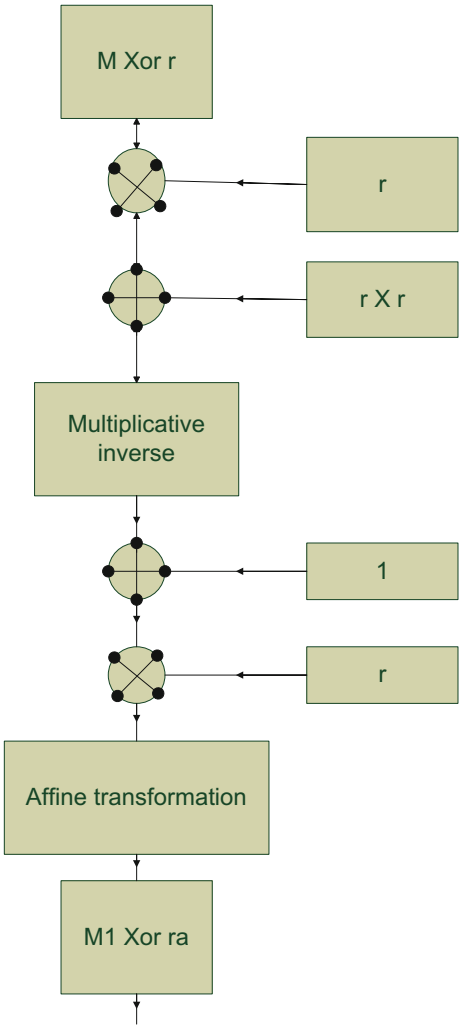

Fig. 4 SubByte transformation with masking

5 Implementation Result

The algorithm for the encryption is implemented using FPGA which enables parallel efficient execution of algorithms rather than serial fashion of computing. The programs for the algorithms of both AES and masked AES are simulated for certain test vectors which successfully provided the ciphertext as shown in Figs. 6, 7 and 8. The implementation of the AES and the masked AES was performed with same plain text and key. Masking implementation was performed using two sets of mask value which provided different ciphertext for each mask which are also entirely different from ciphertext of unmasked AES. The implementation result is shown in Table 8.

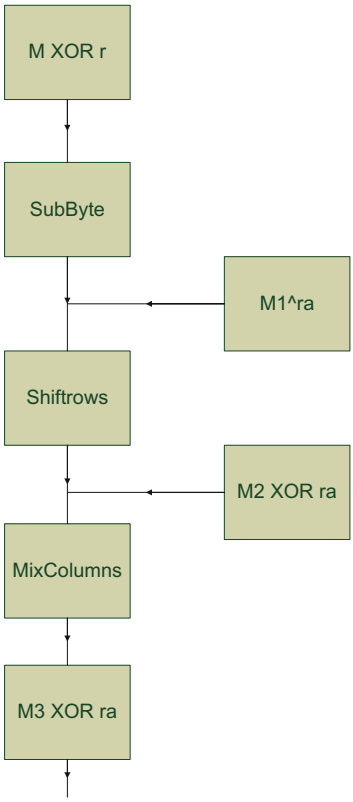

Fig. 5 AES transformation with masking

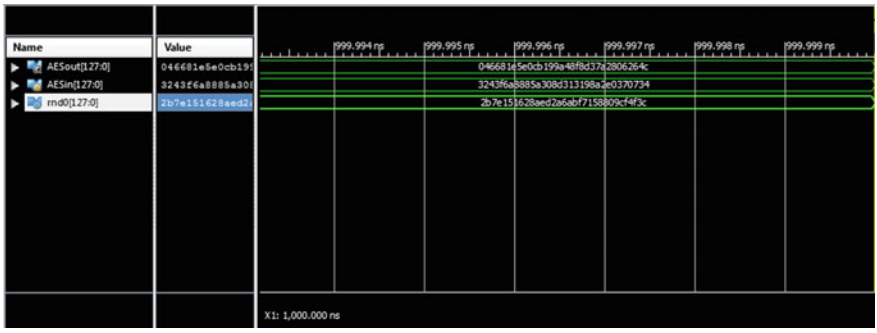

Fig. 6 Simulation result of AES (without mask)

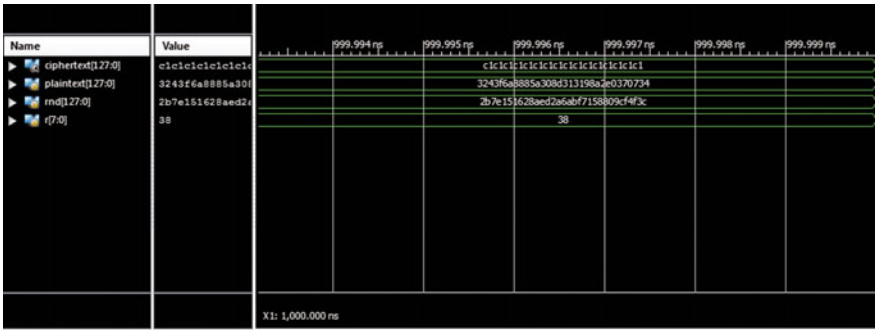

Fig. 7 Simulation result of masking with mask 8′b38

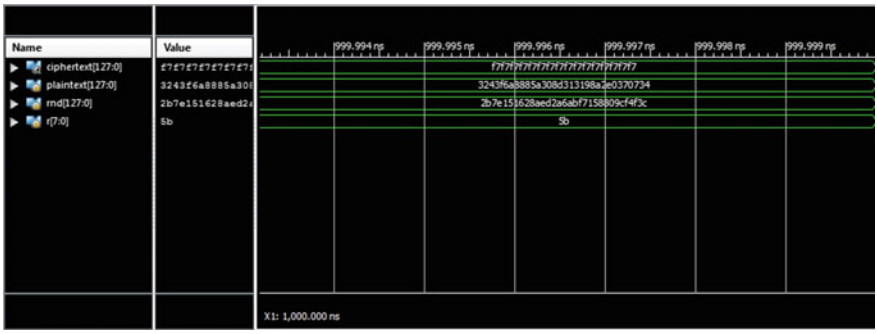

Fig. 8 Simulation result of masking with mask 8′b5b

Table 8 Implementation result

Cipher	AES	Masked	Masked
Plain text	3243f6a8	3243f6a8	3243f6a8
	885a308d	885a308d	885a308d
	313198a2	313198a2	313198a2
	e0370734	e0370734	e0370734
Key	2b7e1516	2b7e1516	2b7e1516
	28aed2a6	28aed2a6	28aed2a6
	abf71588	abf71588	abf71588
	09cf4f3c	09cf4f3c	09cf4f3c
Mask	No mask	38	5b
Ciphertext	046681e5	c1c1c1c1	f7f7f7f7
	e0db199a	c1c1c1c1	f7f7f7f7
	48f8d37a	c1c1c1c1	f7f7f7f7
	2806264c	c1c1c1c1	f7f7f7f7
Max. path delay (ns)	36.886	36.886	36.886
Memory usage (Kbytes)	342,532	342,532	342,532

6 Conclusion

Masking is the process of converting the real element into a random value to make power consumption of each process in AES implementation independent of data. This helps to prevent DPA. The paper includes implementation of the architecture for normal S-Box and other linear structures of AES. Masking technique is implemented on AES encryption structure using Boolean operations like XOR. Masking operation has generated different outputs for same input or plain text using a mask value. The technique used removes relation between outputs and inputs without affecting the performance of AES implementation. The synthesis of the AES and masked AES shows no variation in area, time and memory utilization. More than one mask for single intermediate value can be used to ensure high masking, but as the number of masks increases, cost of implementation, storage area and computation time increases. Number of masks used should not degrade the performance of cryptography device. Masking helps to bring DPA resistance in a device without making change in its power consumption characteristics.

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Pipelined and Parallel Architecture of Reversible Watermarking for Greyscale Images

M. Murali, A. Ravi Sankar and S. M. Sakthivel

Abstract

Background: The rapid advancement of multimedia technology has made the data communication and data sharing so comfortable through wireless network and Internet. During this multimedia communication, the piracy of the multimedia content is a primary concern (i.e. anyone can duplicate or alter the originality). One of the most efficient techniques to protect the multimedia data is watermarking. It is the process of adding a secret digital signature to the host content in a visible or invisible form. The process of watermarking will be of reversible or irreversible nature.
Method: In this paper, a reversible watermarking strategy using prediction technique with its hardware architecture is proposed. In the VLSI implementation aspect three different architectural structures are proposed as pipelined, parallel and dataflow architecture with embedding concept.
Findings: Finally, all the three architectural designs are modelled and implemented using Verilog HDL. The entire process is integrated in a specific chip.
Application: It can be used as a separate co-processor for carrying out the watermarking in real time with any multimedia devices.

Keywords VLSI architecture for data hiding · Reversible watermarking
Prediction technique · Bits per pixel (bpp) · Greyscale images

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1 Introduction

Effective communication in digital media is possible as digital image has many advantages in its storage and manipulation. Each and every minute vast amount of multimedia data is embedded and also disperses through Internet [1]. The copyright protection and content integrity is not possible because digital data can be easily duplicated or even it can be altered [2]. Digital watermarking is the good technique for providing content protection. It is the process of embedding secret content into the payload content (image, audio and video).

Image watermarking is carried out either in spatial domain as pixel modification or transform domain as frequency medications [3]. Based on the characteristics, watermarks are classified as robust, fragile and semi-fragile watermarks [4]. Similarly based on visibility, watermarks are classified as visible and invisible watermarks.

Steganography is the technique in which the message is hidden under other source of data without knowing the encoding scheme; it is very difficult to detect [5]. Figure 1 explains the classification of watermarking from the steganography.

Hosinger et al. [6] proposed a watermarking technique in which the payload is embedded in the host and reconstructed from the watermark image by simple subtraction operation. Similarly Kamstra and Heijmans [7] developed a technique to improve the embedding capacity by considering group of pixels and its location.

Following the Kamstara and Heijmans [7], Tian developed a embedding technique [8] based on the high difference between the pixel values. Later Alatter [9] has expanded the pair of pixels into triplet or quadruplet for each cell and then embedded two or three bits per cell according to the pixel values. Alatter's technique covers the triplet [10] or quadruplet [11] of pixels compared to Tian's technique, and it embeds more bits per pixel. Sachnev et al. [12] have used the sorting technique followed by histogram shifting methodology, and finally the embedding is based on the prediction error for increasing embedding capacity. Most of the watermarking algorithms use software approach. In real time, there is a

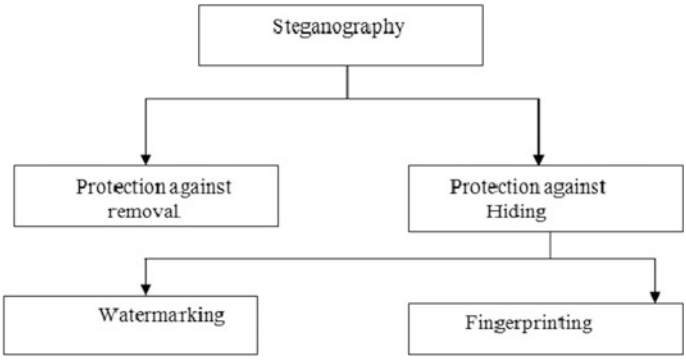

Fig. 1 Types of steganography

greater chance of optimizing area, speed and power using custom circuit design [13–17].

Hardware-based data hiding (watermarking) happens in real time with greater chance of optimizing speed. When image size is too high, software approach is not an ideal one because it needs specific processor to carry out watermarking technique written in high-level language [13–19]. The proposed watermarking approach is the reversible data embedding using sorting and prediction by Sachnev et al. [2] in real time with its VLSI architecture modelled using Verilog HDL language. In this work, different architecture proposed are data flow, pipeline and parallel combination and also evaluated using various metrics

2 Prediction Algorithm

In the entire reversible watermarking process, the average value and the difference value are calculated by considering the four base pixels. Then based on the difference, centre pixel is modified accordingly using the prediction algorithm in the watermarking process. Finally, in the payload embedded data is accomplished with a modified pixel value as shown in Fig. 2. The entire watermarking principle using prediction process is explained in detail in the following subsections.

2.1 Watermarking Process

Here, the four pixel values are taken in diamond pattern and average of four pixel values are calculated. The predicted pixel value is written as in Eq. 1

$$m'_{i,j} = \left[n_{i,j-1} + n_{i+1,j} + n_{i,j+1} + n_{i-1,j}\right]/4 \tag{1}$$

The difference between the actual pixel value and predicted pixel value can be calculated by using histogram shift technique.

The prediction error can be calculated based on Eq. 2

$$S_{i,j} = m_{i,j} - m'_{i,j} \tag{2}$$

Histogram shift encoder technique is used to expand the prediction error depends on where the pixels are located and threshold values. New pixel value is calculated by adding modified prediction error with actual pixel value. The mathematical equation can be written as in Eq. 3

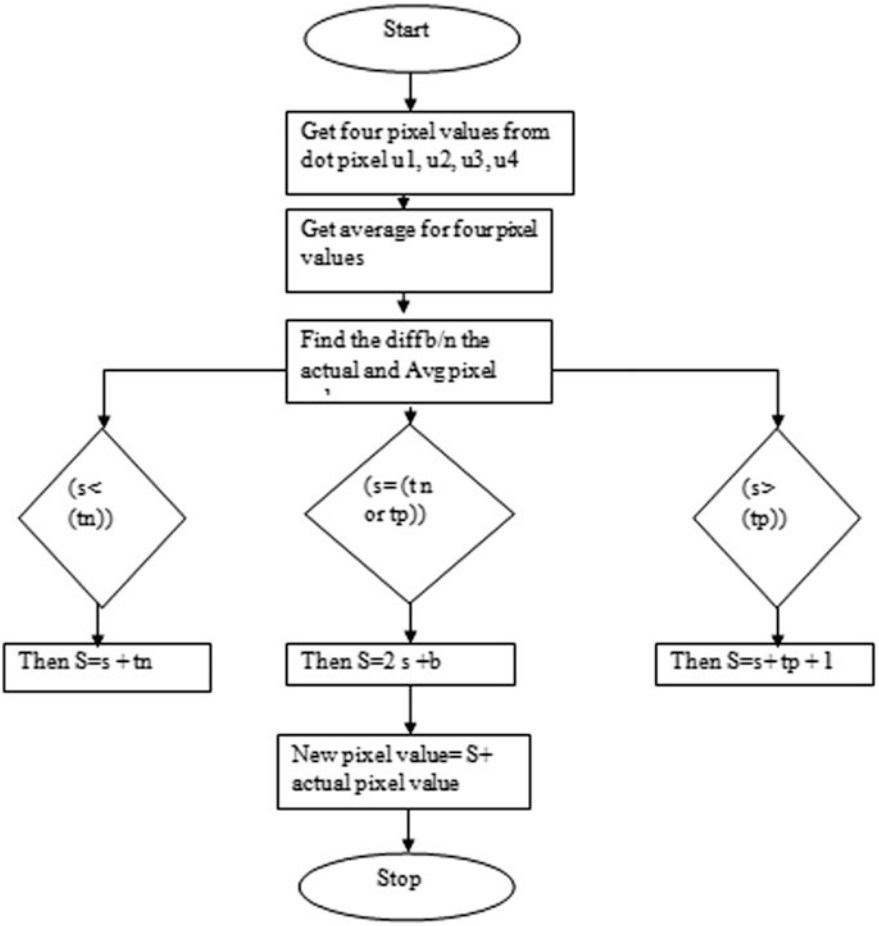

Fig. 2 Encoder of prediction technique

$$M_{i,j} = S_{i,j} + m'_{i,j} \tag{3}$$

Watermarking process is performed at the encoder side by adding digital data (0, 1) to the host signal (image) at the encoder side.

2.2 Extraction Process

In the extraction process, the reverse operation of the prediction algorithm is incorporated for payload extraction. In this once again difference is calculated for the new embedded image, and then by comparing with the original difference, the

payload is extracted. The entire process of the watermarking extraction is explained in details in the following subsections as below and as in Fig. 3.

Modified predicted pixel value is calculated from the new pixel value and actual pixel value. Mathematical expression is written as in Eq. 4

$$S_{i,j} = M_{i,j} - m'_{i,j} \tag{4}$$

Histogram decoder technique is used to calculate the original predicted value. The embedded bit can be recovered from Eq. 5

$$b_i = S_{i,j} \bmod 2 \tag{5}$$

The original pixel value is recovered by adding predicted pixel value with prediction error. The mathematical expression can be written as in Eq. 6

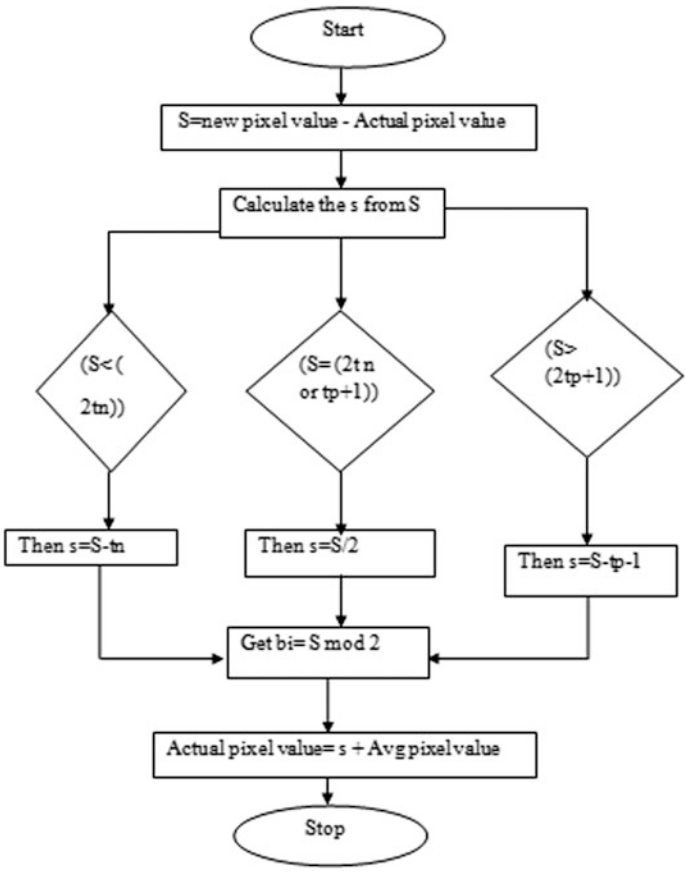

Fig. 3 Decoder of prediction technique

$$m_{i,j} = m'_{i,j} - s_{i,j} \tag{6}$$

Extraction of digital value (0, 1) from the host signal (greyscale image) is performed at the decoder side.

3 Data Path Architecture

The entire reversible watermarking and extraction principle is implemented in three data path architectural mode as dataflow architecture, pipelined architecture and parallel architecture. The rest of the paper is organized with the explanations of the three architectural description and functionalities with its corresponding structures.

3.1 Dataflow Architecture

In this architecture, the algorithm is explained with the help of encoder and decoder blocks.

3.1.1 Encoder

First, two pixel values $n1$, $n2$ are send to adder and $n3$, $n4$ are send to another adder. Outputs of first and second adder are sent to another adder. It is followed by shifter block to calculate the average pixel value. Subtractor block is used to calculate prediction error(s'). It is then followed by histogram shifter and then adder to get modified pixel value (M). The entire process is given as a block diagram in Fig. 4.

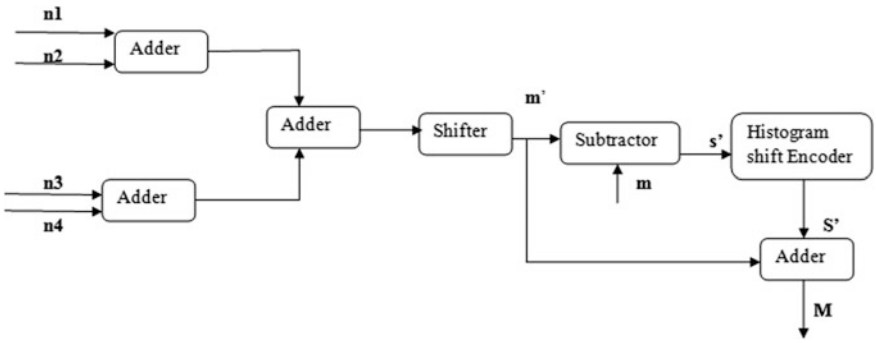

Fig. 4 Encoder of dataflow architecture

3.1.2 Decoder

Modified pixel value and predicted pixel value is sent through subtractor to get modified prediction error. It is then followed by histogram shifter and adder to get the actual pixel value. The entire process is given as a block diagram in Fig. 5.

3.2 Pipelined Architecture

In this architecture, the throughput is constant after specific period of time. For increasing the speed of operation, the operation addition, subtraction and shifting are overlapped in the consecutive clock cycles. The entire scenario is explained in detail using an encoder and decoder data path.

3.2.1 Encoder

The flow is similar to dataflow architecture but in between each operation *D* flip-flop is inserted. Because of using the FF, the delay is reduced between each block. The block diagram of encoder is given in Fig. 6.

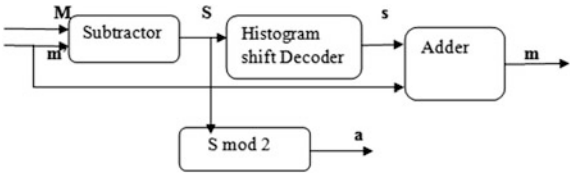

Fig. 5 Decoder of dataflow architecture

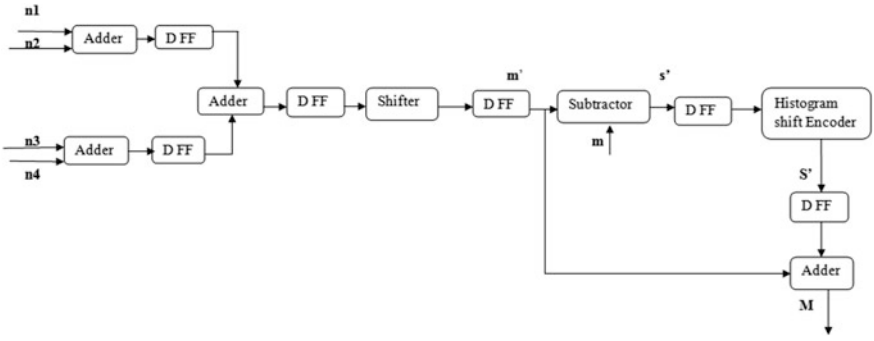

Fig. 6 Encoder of pipelined architecture

3.2.2 Decoder

The operation is alike the decoder of dataflow architecture but in between each operation *D* flip-flops are inserted. The block diagram is given in Fig. 7.

3.3 Parallel Architecture

In this architecture, throughputs are more. Speed of operation is almost similar to dataflow architecture, where two or more consecutive structures are simultaneously utilized for the watermark embedding and extraction.

3.3.1 Encoder

Once again the operation is similar to dataflow with a difference of more than one output as the blocks are simultaneously carrying the process. The block diagram is given in Fig. 8.

3.3.2 Decoder

The flow is similar to decoder of dataflow, but it generates more than one output at the decoder. The entire process is given as a block diagram in Fig. 9.

4 Experimental Results and Discussion

This section explains about the simulation results using MATLAB R2013b© and Xilinx ISE 14.3. Boat image is taken as a host image with a size 256 × 256 as in Fig. 10. The watermarking content can be considered as a random binary data. By using MATLAB, the entire strategy is evaluated using the image quality metrics

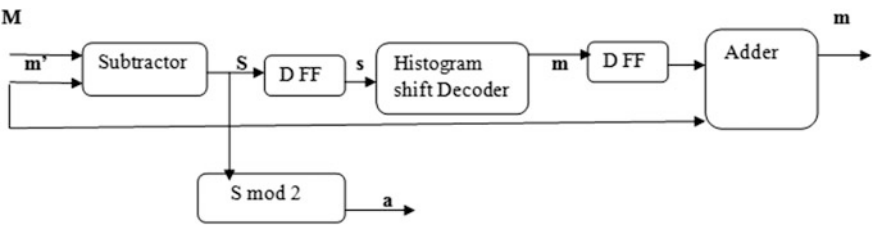

Fig. 7 Decoder of pipelined architecture

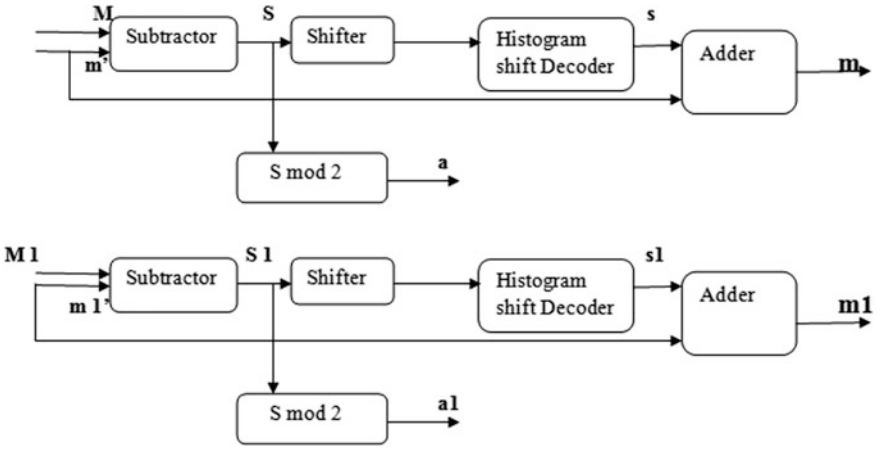

Fig. 8 Encoder of parallel architecture

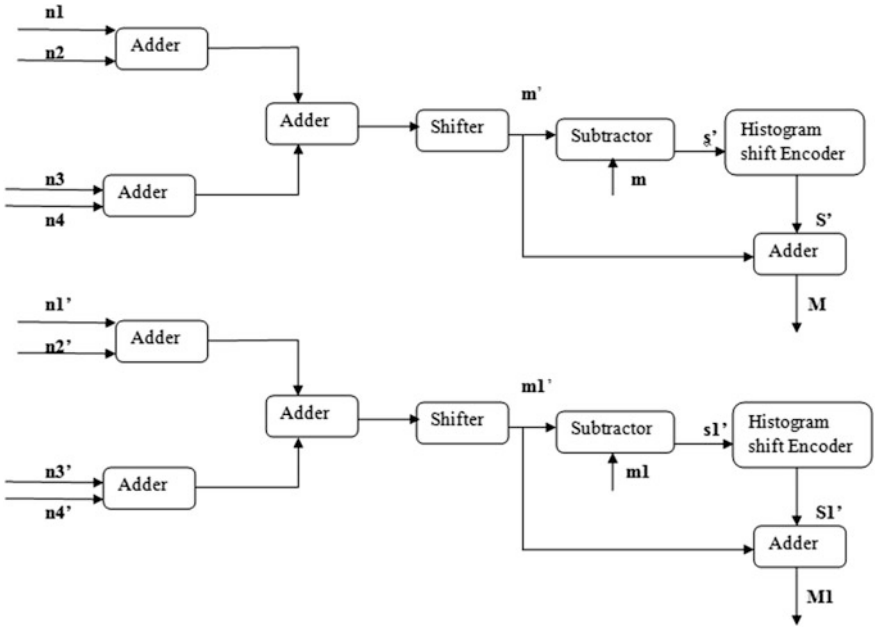

Fig. 9 Decoder of parallel architecture

payload size (Bits per pixel bpp) and signal-to-noise ratio (PSNR). For a 256 × 256 image after performing the prediction technique the total number of bits embedded are 55,076. Hence the bpp (bits per pixel) is 0.84 compared to the original pixels of embedded image. Table 1 shows PSNR and bpp for the corresponding boat image.

Fig. 10 Reversibly embedded 256 × 256 image

Table 1 Quality metrics

Technique	Prediction technique
Image pixel value	65,536
Payload size	55,076
Bit rate (bpp)	0.84
PSNR (dB)	31.50

The same concept is implemented in Xilinx ISE using Verilog HDL for different architectures. The simulation result for the prediction technique for different architectures is taken. For Verilog HDL implementation, the image values are converted into hexadecimal values using MATLAB. Simulation is executed. From the simulated output of MATLAB and Verilog implementation, it is found that there is no deviation in the pixel values, hence the algorithm working good on both HDL and MATLAB. Entire three different architectures for same watermarking and extraction are synthesized. Run time efficiency of proposed hardware implementation is performed for 256 × 256 image size over software simulation. Simulation using MATLAB R2013b© platform running on a Intel® core TM i3-3110 M CPU with 4 GB internal RAM and operating frequency of 2.40 GHz takes 1.123 s to process entire algorithm, but the hardware implementation using pipeline architecture requires 139.106 μs, and pipeline with pipeline adder architecture requires

Table 2 Delay of different architecture

Architecture	Delay for each rhombus pattern (ns)	Delay for entire image (μs)
Dataflow	8.821	162.558
Parallel	8.905	164.136
Pipeline	7.547	139.106
Pipeline with pipeline adder	2.051	37.804

only 37.804 μs to process 256 × 256 image. Delay is calculated for dataflow, pipelined parallel architecture and pipeline architecture with pipeline adder results are calculated and results are tabulated in Table 2.

5 Conclusion

In this paper, a simple reversible data embedding method using MATLAB and its hardware realization in three architectural mode using Verilog HDL is carried out in an effective way. Finally, the comparison has been made with software approach and hardware approach. Redundancy in the digital content is explored using prediction technique and compared with different architectures. It can be enhanced for RGB images. It can be improved further by considering the pixels as a group and pipeline with different hardware. The proposed algorithm provides real time high-speed hardware processing by resolving the privacy and piracy issues.

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Design and Verification of AMBA AXI3 Protocol

Shweta Sharma and S. M. Sakthivel

Abstract

Objective: In this paper, the design and verification of AMBA AXI3 protocol are carried out in a coverage mode analysis using Verilog HDL language.
Method: The design of AXI protocol is made according to its architecture specifications, and its functionality is verified using QuestaSim tool. In the AXI protocol analysis, the burst-based transactions, i.e. writing and reading of increment burst have been implemented.
Findings: In addition to that the AMBA AXI efficiency is evaluated by calculating performance metrics bus utilization, busy count and valid count. In the entire paper, a verification environment is created for the verification of AXI protocol as a verification IP for modern SOC architectures.
Applications: High percentage of bus utilization ensures that the SOC on chip bus is functioning well and makes this protocol as one of the widely used protocols in today's SOC implementation.

Keywords AMBA AXI3 · AMBA AXI3 master · AMBA AXI3 slave
Handshaking process · Coverage mode analysis · Verification IP

1 Introduction

Today's digital world is converging towards data with the evolving of not only entire 3G network but also the 4G network and all this is benefiting data market. The modern SOC architecture consists of many intellectual IP cores inbuilt on it, and hence, establishing a proper synchronization between each IP cores is a crucial task

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[1]. Nowadays, majority of the SOC chips using an inbuilt bus architecture like AXI to establish an error free and synchronized data communication [2] between the IP cores. In the recent years, the design of Modern SOC with inbuilt architectures involves major percentage of time in the verification only (i.e. up to 70%) [3]. Hence, the design engineer has adopted a verification strategy as inbuilt verification IP for the modern SOCs in a coverage-driven mode [4]. Due to the availability of inbuilt verification IP, a major span of time spend in the verification process is reduced. Among all the BUS protocols like AHB and APB, AXI consumes moderate power with a better performance which leads to the usage of AMBA AXI bus in all modern SOC architectures [5, 6]. Here to connect IP core to the surrounding interface, the AMBA bus is used (one of the SOC buses) [6–12]. The width of the AMBA data bus can be 32, 64, 128 or 256 byte and that of the address bus is 32 bits. AMBA protocol enables IP reuse which is essential component in reducing the time scale and development cost. The AMBA AXI is a standard bus protocol. Interconnects which supports AXI bus interface are designed by most of the companies.

2 Amba Axi3 Architecture

AMBA AXI is a burst-based protocol. The AMBA AXI3 consists of master, slave and AMBA AXI3 interface. Using an interface, slave and master are connected. Master M1 can access one slave at same time as master M2 access another slave, this is due to the parallel capability of interconnect [6–12]. This is shown in Fig. 1.

AXI protocol key features are:

- Separate control/address and data phases
- Using byte strobes support for unaligned data transfers
- To enable low-cost *direct memory access* (DMA) separate read and write data channels.
- Issue of multiple outstanding addresses
- Out-of-order transaction completion

To provide timing closure easy addition of register stages.

Nature of data to be transferred is determined by address and control information present on address channel.

Using a write data channel or a read data channel, data are transferred between the master and slave.

The AXI protocol supports:

- Issuing of address information ahead of actual data transfer.
- Multiple outstanding transactions.
- Out-of-order completion of transactions.

AXI protocol consists of five channels:

- Write address channel
- Read address channel

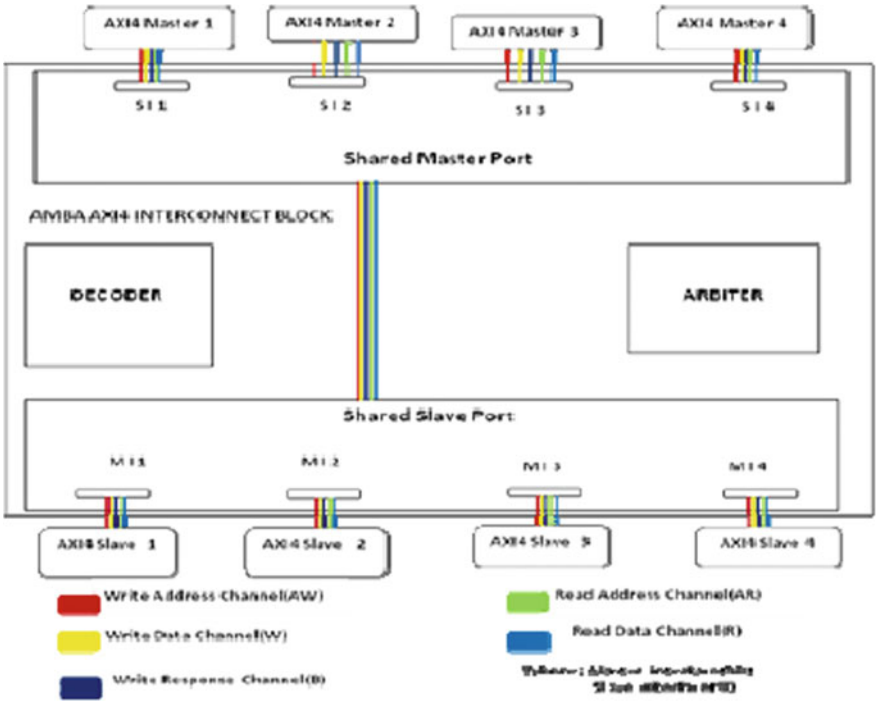

Fig. 1 AMBA AXI3 bus interconnect block diagram [7, 9]

- Write data channel
- Read data channel
- Write response channel.

Burst is of three types:

- Fixed burst
- Incrementing burst
- Wrapping burst.

In this paper, incrementing burst is used.
The AXI protocol responses are:

- OKAY
- EXOKAY
- SLVERR
- DECERR.

In this paper, OKAY response is showcased and described.
AXI3 support maximum up to 16 beats for a single burst.

In write transaction, address and data are sent from master and accepted by slave as shown in Fig. 2. When whole data are received on slave side, the slave sends response signal to master as acknowledgement.

Read transaction includes transferring of address from master to slave and data from slave to master as shown in Fig. 3.

3 Proposed Work

The proposed work includes designing of AXI master and AXI slave with operating frequency of 100 MHz, i.e. clock duration of 10 ns. Communication between master and slave is established at the prescribed frequency stated and well maintained during the entire design process. Master initiates each and every transaction, and thus, slave characteristics are studied. Burst signals are sending from master to slave or from slave to master.

Function of two components of AXI is:

3.1 AMBA AXI3 Master

Master sends write address and write data signals, i.e. it sends signal like AWADDR, WDATA, AWBURST to slave through an interface in case of write

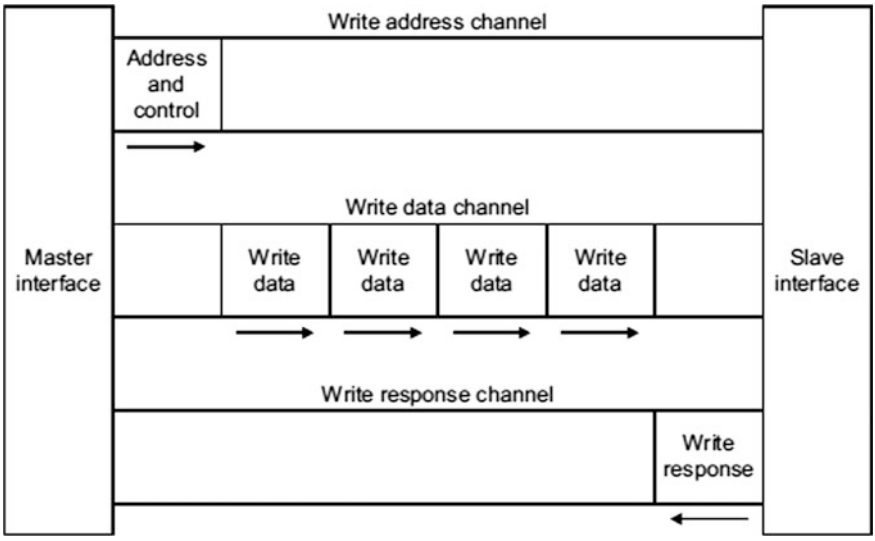

Fig. 2 Channel architecture of write

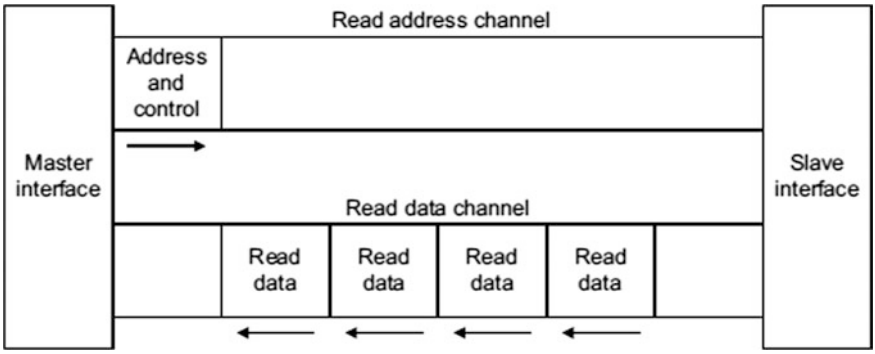

Fig. 3 Channel architecture of read

operation. Similarly, signals like ARADDR, ARBURST are sent from master to slave in case of read operation. Handshaking operation is carried out between master and slave in which address and data are validated.

3.2 AMBA AXI3 Slave

It receives all the signals coming from master side. It sends signal like RDATA from slave to master in case of read data. Handshaking signals are sending from slave side to master.

Signals involved in AMBA AXI3 protocol has been shown in Fig. 4 in detail.

3.3 Handshaking Process

3.3.1 Write Transaction

In write transaction, as shown in Fig. 5, address from master, i.e. AWADDR is sent. Correspondingly WDATA is sent from master side. AWVALID rises to one as soon as address information and control information are available on lines. On availability of WDATA, the WVALID signal goes one. On reception of AWVAID and WVALID, AWREADY and WREADY go to one after one clock cycle. WLAST signal goes to high when last WDATA of a particular burst is sent. In response, BRESP signal is sent as OKAY if everything is proper otherwise other relevant statuses are sent. If BRESP signal is sent as OKAY, then BVALID is raised to one and then on the master side the reception of BVALID BREADY is raised to one. In this paper, the increment operation is carried out in the burst mode.

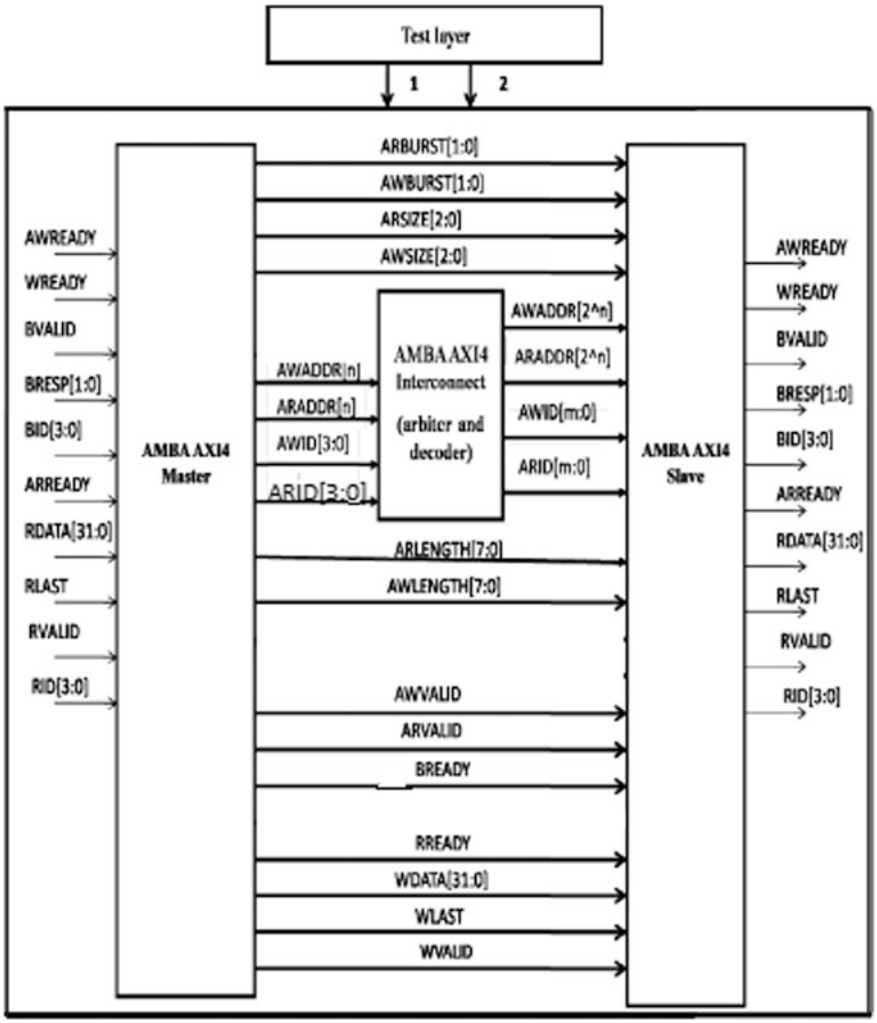

Fig. 4 Signals used to design AMBA AXI3 protocol

3.3.2 Read Transaction

In read transaction, as shown in Fig. 6, ARADDR is sent from the master to slave. ARVALID goes high when ARADDR is available. On reception of ARVALID on slave side, ARREADY gets high after one clock cycle.

RDATA is sent from slave side, and correspondingly RVALID is set high. On master side, RREADY is high when master side is ready to accept the data, i.e. when RVALID is high. When RLAST is high (on sending of last beat of burst), then RRESP sends OKAY as response if burst transaction is fine.

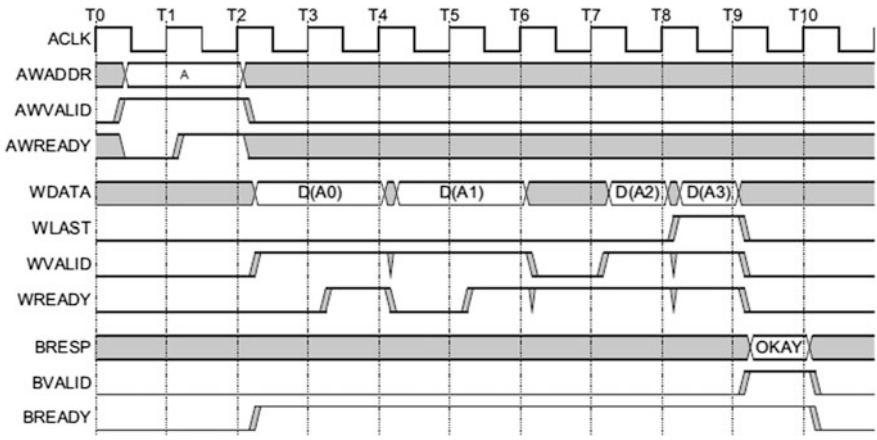

Fig. 5 Write burst cycle

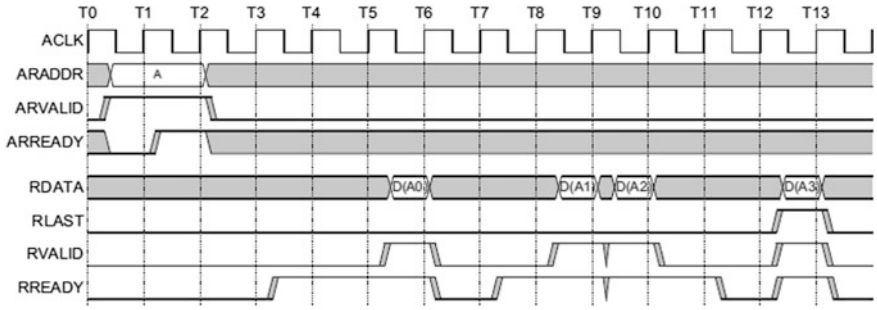

Fig. 6 Read burst cycle

4 Simulation Results

Simulation of the code written in Verilog is done using the Mentor Graphics Questasim.

One case simulation has been shown in this paper, i.e. firstly writing of data in the memory and then reading of same data from memory and sending it to master.

4.1 Write Transaction

In write transaction, WDATA corresponding to AWADDR has been sent. Correspondingly, for address 1, data sent are five in hexadecimal, for address 2, data sent are six and for address 3 data sent are seven. Here AWLEN is two and

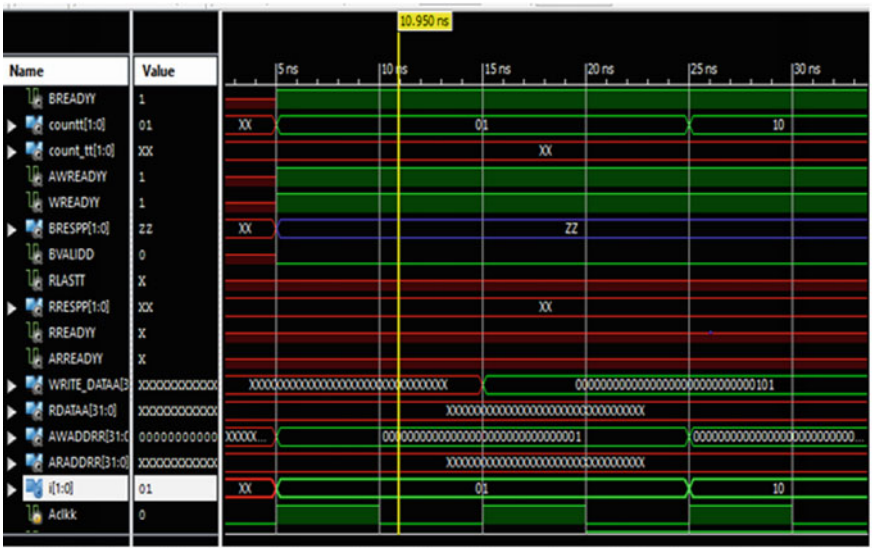

Fig. 7 Initial step of write phase

AWSIZE is one. Figure 7 shows sending of write address and date. Figure 8 shows sending of last data and generation of response as 2′b00 from slave side which indicates OKAY.

VALID COUNT for write phase = 4

BUSY COUNT for write phase = 5

BUS UTILIZATION = (4/5) * 100 = 80%

4.2 Read Transaction

In read transaction, written data are read from the memory and sent to master. Five corresponding to address 1 in hexadecimal have been sent from slave to master. Similarly, six corresponding to address 2 and 7 corresponding to address 3. Figure 9 shows sending of five as data corresponding to address 1.

Figure 10 shows generation of response as 2′b00 from slave side, i.e. OKAY from slave side when RLAST is high.

VALID COUNT for read phase = 3

BUSY COUNT for read phase = 4

BUS UTILIZATION = (3/4) * 100 = 75%

The corresponding read and write transaction with their respective metrics are shown in the below diagrams in the following manner.

Initial phase shown in Fig. 7 denotes transfer of data 5, 6 and 7 corresponding to write address 1, 2 and 4 in case of write operation.

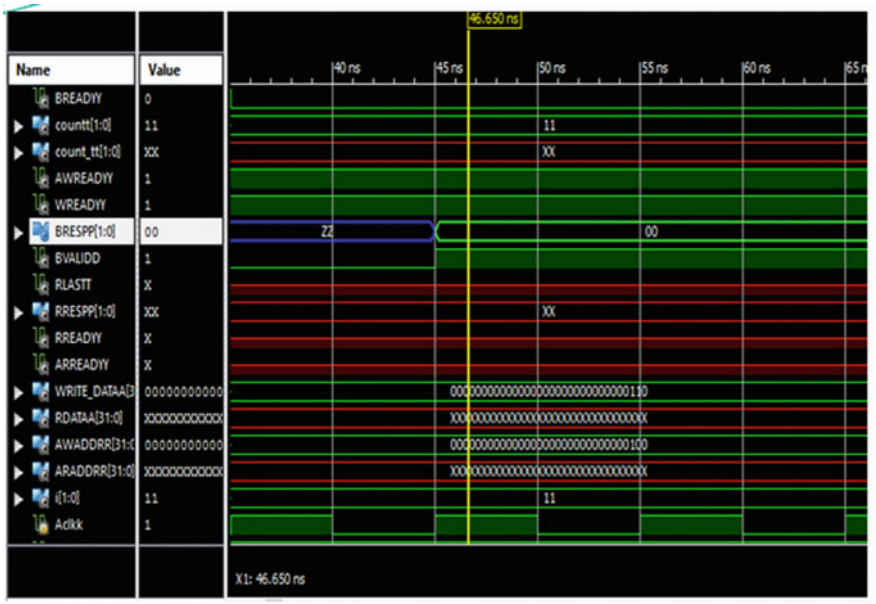

Fig. 8 Final step of write phase

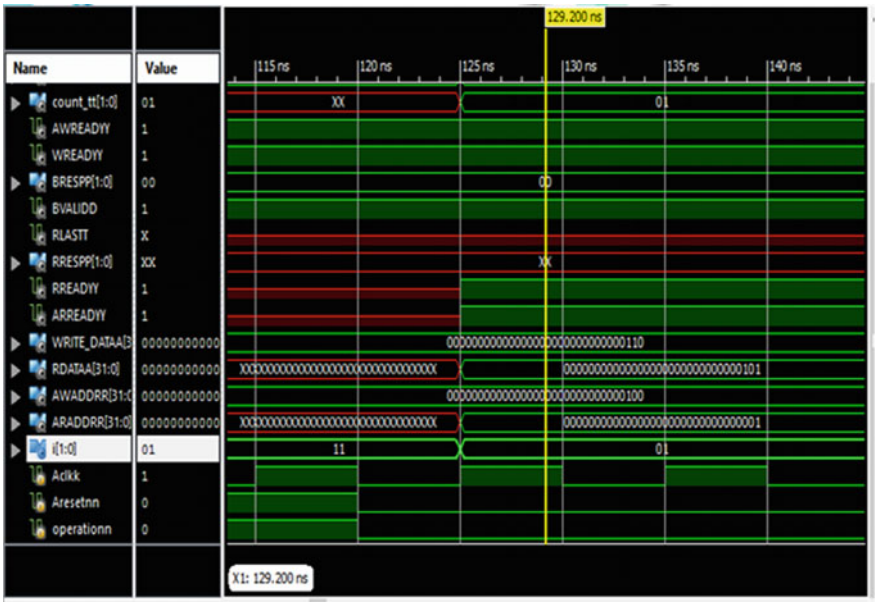

Fig. 9 Initial step of read phase

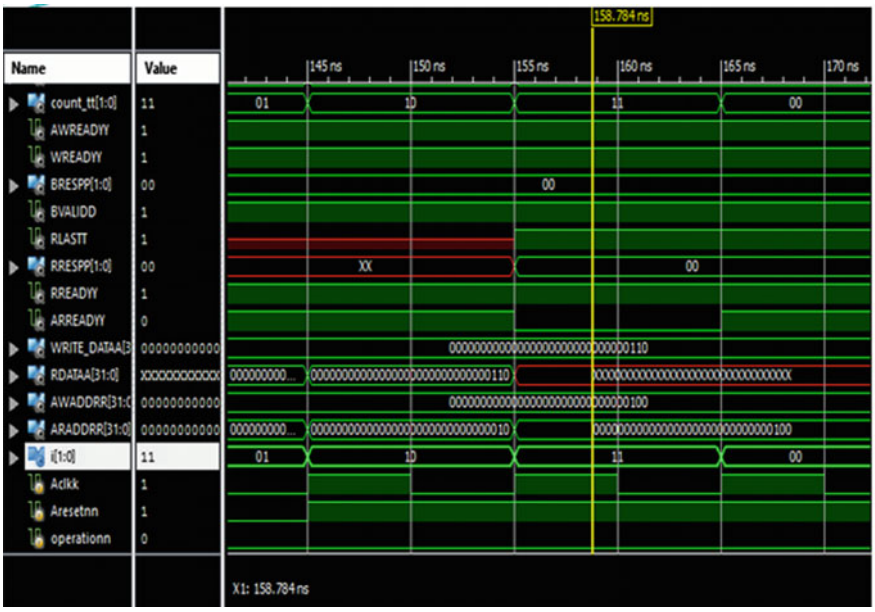

Fig. 10 Final step of read phase

Figure 8 denotes sending of BRESP as okay from slave to master on reception of seven as data on slave side. Figure 8 is final step of write phase.

Initial step of read phase as shown in Fig. 9 shows reception of data 5, 6 and 7 corresponding to read address 1, 2 and 4. Final step of read phase shows sending of RRESP as okay from slave to master when last transfer is being send.

Functional verification is performed here by checking address and data sent and by checking handshaking signals with the help of waveforms. Fine handshaking process shown in Figs. 7, 8, 9 and 10 verifies the design. Result of the code coverage using QUESTA SIM is shown in Figs. 11a, b and 12. These two figures show total coverage, i.e. how many statements, branches, states, toggle bins have been covered. Here in test bench, there are no states, branches to be covered. So, all statements and toggles have been covered. Here tb_axi is showing whole code coverage of the design.

Statements coverage is 100% in tb_axi. In Fig. 11, it is shown 10 statements 10 hits, 360 toggles 357 hits and 3 misses. In Fig. 12, 100% coverage coverage of tb_axi is shown.

(a)

Coverage Report Summary Data by file

File: axi_master.v

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	26	0	26	0.0
Branches	13	0	13	0.0
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	0	0	0	100.0
Transitions	0	0	0	100.0
Toggle Bins	208	0	208	0.0

File: axi_slave.v

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	29	0	29	0.0
Branches	15	0	15	0.0
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	0	0	0	100.0
Transitions	0	0	0	100.0
Toggle Bins	156	0	156	0.0

(b)

File: master_slave.v

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	0	0	0	100.0
Branches	0	0	0	100.0
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	0	0	0	100.0
Transitions	0	0	0	100.0
Toggle Bins	74	0	74	0.0

File: tb_axi.v

Enabled Coverage	Active	Hits	Misses	% Covered
Stmts	10	10	0	100.0
Branches	0	0	0	100.0
FEC Condition Terms	0	0	0	100.0
FEC Expression Terms	0	0	0	100.0
States	0	0	0	100.0
Transitions	0	0	0	100.0
Toggle Bins	360	3	357	0.8

Fig. 11 **a, b** Code coverage results

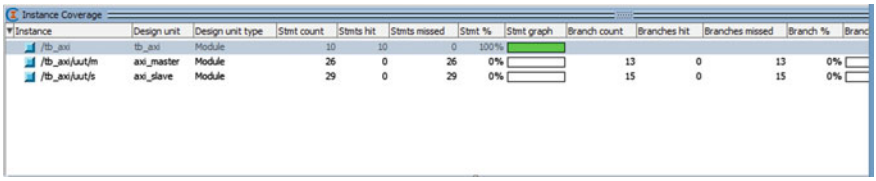

Fig. 12 Percentage of code coverage

5 Conclusion

AMBA AXI3 is designed using Mentor Graphics QuestaSim tool in Verilog and functionally verified. Corresponding code coverage is also calculated and measured. Performance metrics is calculated which includes calculation of valid and busy count and bus utilization [5]. Bus utilization is 80% in case of write case and 75% in case of read case.

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Design of Multi-stage CMOS OTA for Low-Power and High Driving Capability

Rama Krishna Murthy Paturi and P. Manikandan

Abstract

Objective/Background: Multi-stage CMOS OTAs have been used in vast areas like micro-sensor nodes, Bio-medical applications. In this paper, a three-stage CMOS OTA has been designed in 180 nm technology, which is suitable for low-power applications requiring high driving capability.
Methods/Analysis: When both low-power and low-voltage operation are the goals, MOS transistors operating in subthreshold regions are used. So, in this work, all the transistors of the amplifier operate in subthreshold region. Reversed Nested Miller Compensation (RNMC) technique is used for stabilizing the amplifier. A slew-rate enhancer (SRE) is used to enhance the slew-rate of the amplifier after compensation.
Findings: Powered with 1-V supply, the proposed OTA can drive loads up to 450 pF with phasemargin for this maximum load as 45°. The maximum gain achieved is 120 dB for low frequencies. Power dissipation is obtained as 275.39 nW for low capacitive loads (200 pF). Cadence Virtuoso-64 tool is used for simulations.
Conclusion/Improvements: The problem with slew-rate at higher frequencies has been found to be not at the final stage but at the first stage and is resolved using the SRE circuit for a stabilized three-stage OTA. The stabilized and slew enhanced amplifier can drive up to 450 pF load with around 4 μW power dissipation.

Keywords Low-power · Low-voltage operation · Subthreshold regions
High driving capability · Cadence Virtuoso-64

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1 Introduction

These days are meant for devices which consume less power while meeting all the design goals. So, reducing power from the scratch is needed. Driving high capacitive loads is the current issue on which the semiconductor industry focused. Operational amplifiers have been very important circuit components giving high gains. A buffered operational amplifier can not drive capacitive loads, whereas an unbuffered operational amplifier with high output resistance can drive capacitive loads. Operational transconductance amplifier (OTA) is an unbuffered operational amplifier. So, with proper designing, it can drive high capacitive loads. Single stage is not sufficient to achieve higher gains. Adopting multiple stages has been a new industrial trend. The multi-stage high-gain amplifiers face stability problem. So, proper compensation technique should be adopted for stabilizing the amplifier. With compensation, the amplifier faces bandwidth constraints. So, this design is useful for low-frequency applications such as micro-sensor nodes, bio-medical applications. In three-stage CMOS OTAs, there is slew-rate problem that is arising due to compensating capacitors [1]. So, additional circuitry is needed to resolve this issue which should not consume additional power when added to the amplifier.

2 Literature Review

The demand for low power and ultra-low power made the devices to adopt sub-threshold region as operating domain [1]. Nested Miller compensation (NMC) technique [2] faces bandwidth problems. Reversed nested Miller compensation (RNMC) gives better results [3, 4]. A slew-rate enhancer is needed for the stabilized amplifier to resolve slew-related problems with high capacitive loads. CMOS OTA with rail-to-rail output swing is demonstrated [5].

3 Proposed Work

The amplifier that is designed in this paper consists of three stages. The gain of folded-cascode OTA as a single stage is larger than the normal OTA. But, in subthreshold region, single-stage OTA gain is not sufficient. So, in this work, a three-stage OTA [1] has been used in 180 nm CMOS technology which can drive high capacitive loads. Because, in the same proportion of the supply voltage reduction, the threshold voltages do not decrease. So, operating the circuit in the subthreshold region is a better choice for low-voltage operations.

3.1 Design of Stable Three-Stage OTA

The three-stage OTA [1] is as shown in Fig. 1. It consists of a folded-cascode CMOS OTA as the first stage (M0–M8) which increases the input common-mode range. This is a non-inverting stage. Second stage is a common source stage (M9–M10) and this is an inverting stage. This boosts the gain observed in the first stage. Third stage (M11–M14) is a class AB output stage. This is designed using common source transistors to increase the allowable output voltage swing. Two capacitors C_{c1} and C_{c2} are used in reversed nested Miller compensation (RNMC) technique. In the circuit diagram, 200 pF load is shown. Capacitive load can range up to 450 pF using slew-rate enhancer (SRE). In the following subsections, Sect. 3.2 describes the I_D–V_{GS} relation of NMOS transistors operating in subthreshold region, Sect. 3.3 describes the RNMC frequency compensation technique and Sect. 3.4 describes the amplifier's slew-rate dependence on compensation capacitors.

3.2 Subthreshold Region Analysis

For an *n*-channel metal oxide semiconductor (MOS) transistor operating in subthreshold region, the I_D–V_{GS} relation is given by,

$$I_D = I_o e^{(V_{GS}-V_{TH}/nV_T)}\left(1 - e^{-V_{DS}/nV_T}\right)$$
$$\approx I_o(W/L)\, e^{(V_{GS}-V_{TH}/nV_T)} \quad (1)$$

where I_o is a technology-dependent parameter.

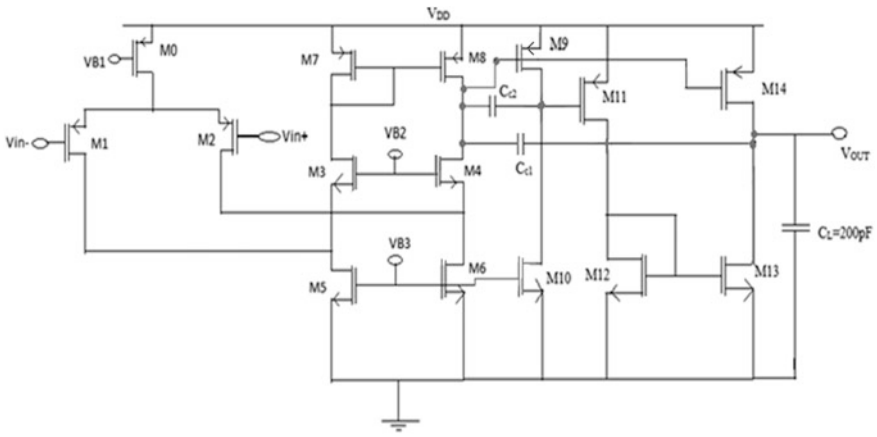

Fig. 1 Three-stage OTA with 200 pF capacitive load

When the $V_{GS} < V_T$, and $V_{DS} \geq 0.1$ V, a weak inversion condition exists and so V_{DS} drops almost entirely across the reverse-biased substrate-drain p–n junction. As a result, variation in electrostatic potential along the channel at the semiconductor interface is small. So, the longitudinal electric field is small. With this and small number of mobile carriers, the drift component of drain to source current I_{DST} is negligible. But as we know, the minority carrier concentration is exponentially dependent on surface potential; this carrier concentration gradient is relatively large, which is enough to produce a significant I_{DST} through diffusion current.

3.3 RNMC Frequency Compensation Technique

When the amplifier is made up of three gain stages and the inner stage is inverting one, reversed nested Miller compensation is used [3]. This technique considers the phasemargin as the main design parameter. And also, this method has proven to be giving better bandwidth compared to NMC technique [2]. The transfer function of the compensated amplifier consists of one dominant pole, two higher poles and two zeros. The constraint to be followed to make the positions of two zeros to be higher than gain–bandwidth product is [1]

$$C_{c2} < \left(I_2 I_3 / I_1^2\right) C_{c1} \tag{2}$$

Assuming the two zeros have been cancelled, a specified phasemargin is [1]

$$\tan\Phi = \left(C_{c1}^2\right)(I_3/I_1)/(C_{c2}C_L) \tag{3}$$

So, the phasemargin is in proportion with C_{c1} and inversely proportion with C_{c2} and C_L. These equations are applicable only when the zeros are assumed to be constant. But, for low-voltage operations, it can not be like that. So, RHP-zero cancellation techniques [4] should be used. But in this paper, no such proposals are needed as zeros can be neglected for this amplifier.

3.4 Slew-Rate Analysis for the Amplifier

Slew-rate determines the rate at which the output changes. It depends on the current flowing through the load capacitor at the output stage. In multi-stage amplifiers, the slowest stage limits the slew-rate. The slew-rate for the designed amplifier is limited by the first stage because of the compensation capacitor C_{c1} including high capacitive load such as 450 pF. The relation can be given as,

$$\text{Slew-Rate, SR} = I_1/C_{c1} \tag{4}$$

So, a slew-rate enhancer (SRE) circuit is needed at the first stage output. The SRE that is used to adjust the slew-rate at the first stage is as shown in Fig. 2.

The MBH (shown in box) adds extra current to the first stage output. After adding the SRE, when the inverting terminal is high, the MB transistor draws more current which makes the PMOS transistor MBH to add current at the output of first stage eliminating the slew-rate problem. The next stages have to be designed based on gain and bandwidth requirements.

4 Simulation Results

4.1 Implementation

When C_L = 200 pF, with 1 $V_{P\text{-}P}$ input step voltage with 10 ms period, transient analysis is done for the uncompensated amplifier in Cadence Virtuoso-64 tool and the results are shown in the Fig. 3.

Slew-rate is calculated by using the relation, slew-rate = dV/dt. All the results are shown in the subsection Sect. 4.2.

$$\text{Power dissipation} = 275.539\ \text{nW}$$

$$\text{Slew-Rate} = 0.56324\ \text{mV}/\mu\text{s}$$

Now, when the amplifier is compensated, the circuit is showing the slew-rate problem as shown in Fig. 4b.

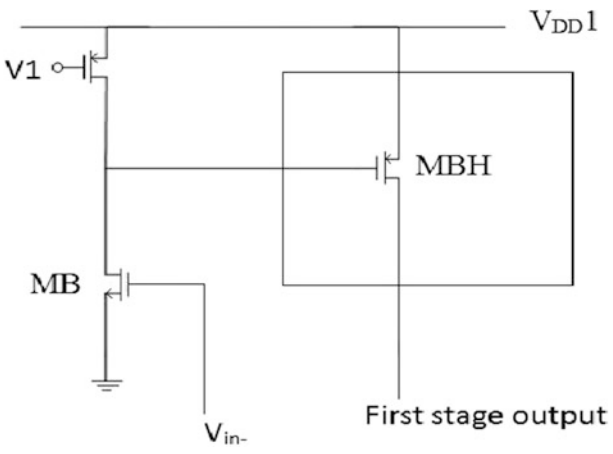

Fig. 2 Slew-rate enhancer circuit

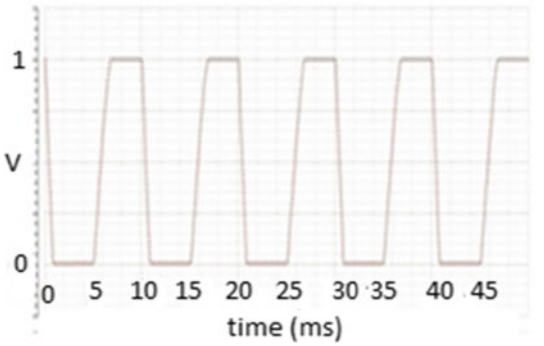

Fig. 3 Transient analysis at output of the three-stage OTA with C_L = 200 pF

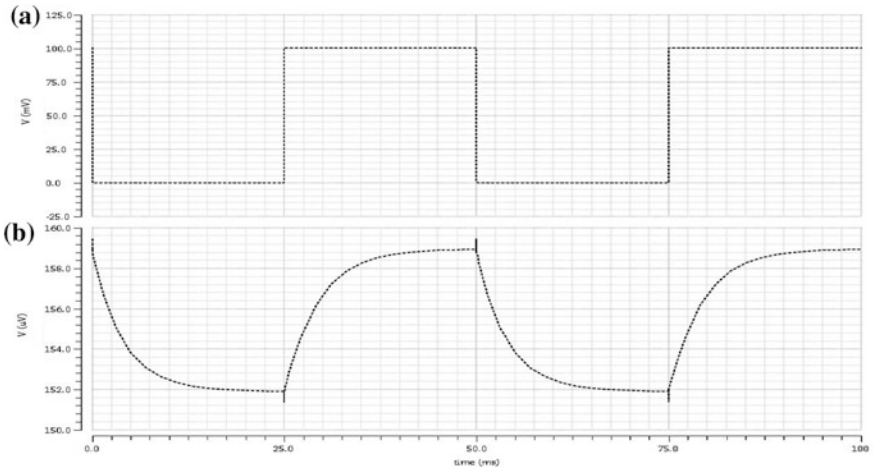

Fig. 4 **a** Input waveform at inverting terminal, **b** output of compensated amplifier without slew-rate enhancer

After adding the SRE, the output is as shown in Fig. 5.

Here, the power consumption and gain–bandwidth product are increasing which is shown in Table 2 in next section.

4.2 Comparison of Results

Table 1 shows the parameters that are extracted from the compensated circuit with slew-rate problem. The maximum gain obtained is 91 dB, and unity gain frequency is around 30 kHz. The static power dissipation is 275.539 nW. C_{c1} = 150 pF, C_{c2} = 1 pF.

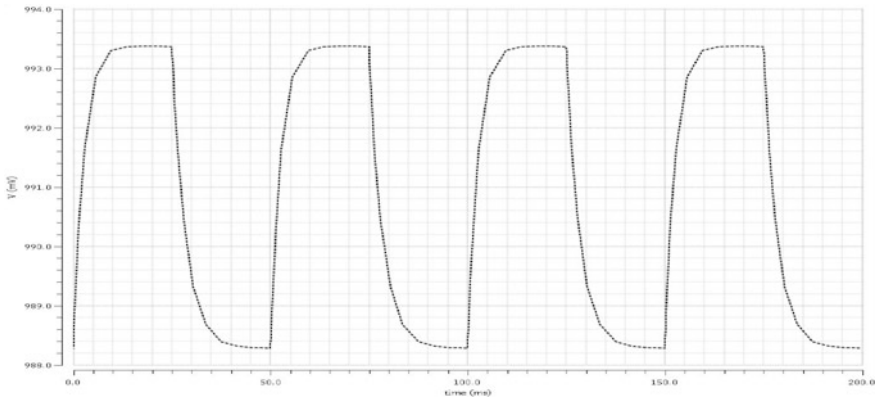

Fig. 5 Output after adding SRE circuit

Table 1 Amplifier parameters without slew-rate enhancer

Parameter	Value
Gain (dB)	91
Unity gain frequency (kHz)	30.596
Power (nW)	275.539
Phasemargin	75.8484°

Table 2 shows the parameters for the slew-rate adjusted circuit using SRE circuit. The gain for the designed circuit is around 100 dB, and the static power dissipation for the slew-rate enhancer circuit is around 6 nW which is negligible. The unity gain frequency is 153.897 kHz which is larger than the previous design as shown in Table 1. The phasemargin is 62.765°. C_{c1} = 150 pF, C_{c2} = 1 pF.

The system can be used for a load up to 450 pF with a phasemargin of 45°. This is much larger than the design in [1]. The maximum gain obtained for the entire system is 100.3 dB. The circuit can be designed for lower gain with less power consumption. With the gain mentioned above, the amplifier can drive loads up to 450 pF.

Table 2 Amplifier parameters with slew-rate enhancer

Parameter	Value
Gain (dB)	100.3
Unity gain frequency (kHz)	153.145
Power (μW)	4.93785
Phasemargin	62.765°

5 Conclusion

In this design, a low-power three-stage OTA is analysed and the problems involved in the design are resolved. The problem with slew-rate at higher frequencies is adjusted using slew-rate enhancer (SRE) circuit. The maximum gain that is obtained for low-frequency operation is around 100 dB for a stable circuit. Compared to the previous designs, this design can drive loads up to 450 pF. The static power dissipation is 275.539 nW making the design useful for ultra-low-power applications operating at low frequencies. The unity gain frequency is 153.897 kHz for 100.3 dB gain.

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