

Novel Robust Design for Reversible Code Converters and Binary Incrementer with Quantum-Dot Cellular Automata

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Abstract This work, we employ computing around quantum-dot automata to construct the architecture of the reversible code converters and binary incrementer. The code converter and binary incrementer are made up of Feynman gate and Peres gate, respectively. We have presented the robust design of Ex-OR in QCA, which is used for the construction of code converters and binary incrementer. The layouts of proposed circuits were made using the primary elements such as majority gate, inverter, and binary wire. A novel binary-to-gray converter design offers 59% cell count reduction and 36% area reduction in primitives improvement from the benchmark designs. Being pipeline of PG gate to construct the 1-bit, 2-bit, and 3-bit binary incrementer, we can use this robust layout in the QCA implementation of binary incrementer. By the comparative result, it is visualized that the binary incrementer such as 1-bit, 2-bit, and 3-bit achieved 60.82, 60.72, and 64.79% improvement regarding cell count from the counterpart.

Keywords Reversible logic · Quantum-dot cellular automata · Nanotechnology
Code converter, binary incrementer

1 Introduction

The current microelectronics has grown for the past years, but it faces problems in miniature, power, and design cost. Nanoelectronics have an alternative to tackle these problems [1]. The challenges task today is the construction of robust design.

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QCA computing is suitable for the efficient computing around nanometer scale [2]. This paper introduces the robust design with emerging QCA technology which has a potential to the difficulty of conventional CMOS technology [3].

The essence of reversible circuits is accessible to the new generation designer regarding no loss of information. Landauer [4] proved that conventional irreversible logic gates have information loss, i.e., energy dissipate. Bennett [5] proved that for a digital circuit construct from reversible logic gates no information loss also negligible energy dissipation. Moreover, the quantum circuit is to be developed by reversible gates [6].

This paper proposes a robust design of Ex-OR which uses the QCA technology are presented to be used in the construction of reversible code converter and binary incrementer. The design was driven toward less latency, less cell count, minimum clock zones, and no crossover. QCADesigner tool was adapted toward achieving these QCA primitives' results. However, more cell complexity means more power dissipation similarly low complexity increase the computation speed [7]. The complete quantitative analysis of converters and binary incrementer are explored to less complexity means faster computational speed. The results show reduction of QCA primitives when compared with previous work reported herewith. The reversible binary incrementer introduced in this paper will be useful in various fields, including digital signal processing and ALU. Whereas, reversible code converter will be applicable in a change of information from one format to another. Moreover, reversible code converter and binary incrementer will be useful in digital electronics computing where dedicated code converter and binary incrementer modules are demanded. The proposed idea of this article is described as follows.

- A novel two-input Exclusive-OR (Ex-OR) gate is proposed which is used to design an efficient Feynman gate (FG) in QCA.
- The efficient Feynman gates are used to construct the basic designs of a code converter and incrementer.
- Using proposed two-input Ex-OR design of QCA, the 1-bit, 2-bit, and 3-bit binary incrementers have been constructed and reported better QCA primitives as compared to previous designs.
- Half adder and n-bit binary incremental are designed using the proposed Peres gate.

The rest of the article is organized as follows: Sect. 2 discusses previous work. Section 3 presents novel design architecture and the results are discussed and in Sect. 4 comparative statistics is presented. In Sect. 5, conclusion is presented.

2 Previous Work

The architecture of reversible code converter and binary incremental in QCA framework are drawing attention in the previous works. Many works of these designs have been proposed. In 2016, Das et al. [8] proposed binary incrementer in

QCA. The 1-bit design consists of 97 cells, $0.075 \mu\text{m}^2$ area, seven majority voter, four inverter, and four clocking zones. The 2-bit incrementer design consists of 14 majority voter, 8 inverters, 196 cell count, $0.272 \mu\text{m}^2$ area, and 4 clocking zones. Several reversible code converters in QCA have been proposed in [9, 10]. Das et al. [9] present the code converters in QCA. In these designs, multilayer design is used for layout, with suffers from high latency and complexity. Misra et al. [10] presents the 3-bit reversible binary-to-gray and gray-to-binary code converter in QCA. The design consists of 118 and 112 cell count in binary-to-gray and gray-to-binary code converter, respectively. Several efforts have been made in optimizing the code converter and binary incrementer in QCA technology for efficient reversible logic computing. In this work, the robust QCA design of the proposed reversible circuits is introduced first by using Ex-OR. Such a proposed QCA design shows the robust in the reliability as a whole.

3 Building Blocks of Code Converter and Binary Incremental

This section introduces robust architecture of reversible code converter and binary incrementer. Toward the QCA design of code converter and binary incrementer, one robust design of Ex-OR is presented which incurs zero latency.

3.1 Ex-OR Gate in QCA

Ex-OR operation is commonly used in many digital logic applications such as designing arithmetic circuits, pseudorandom number generation, correlation, and sequence detection. In this work, we are presenting a new two-input Ex-OR gate. Figure 1a, b illustrates the gate symbol and QCA layout of this gate respectively. Figure 2c illustrates the simulation result which indicates that there is a zero latency.

Our proposed QCA layout of two-input Ex-OR gate requires 13 cell count with an overall area of $0.02 \mu\text{m}^2$. This gate will be highly cost efficient in designing complex digital circuits. The comparison result is presented in Table 1. This is the first Ex-OR gate that utilizes less cell count and zero latency as compared to previous.

3.2 Reversible Code Converter Implementation in QCA

To design a code converter, we used the two-input Ex-OR gate in logic output construction. In the first type, code converter is binary-to-gray. In this design, three

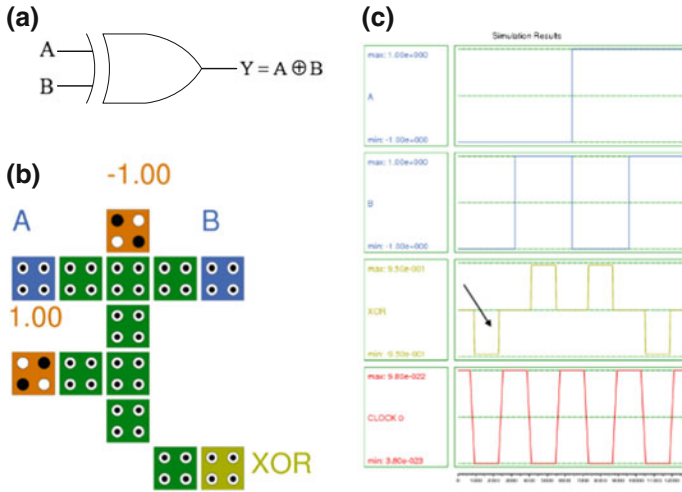


Fig. 1 Ex-OR gate a functional diagram b quantum-dot cell layout c timing waveform

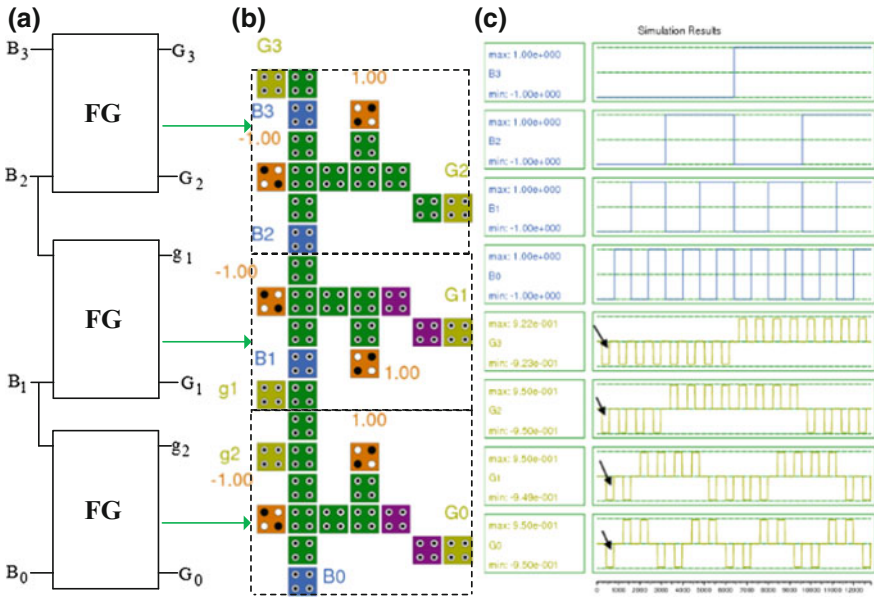


Fig. 2 Reversible four-input binary-to-gray code converter a functional diagram b quantum-dot cell layout c timing waveform

Table 1 Comparison of two-input Ex-OR gate QCA layouts

Design	Cell count	Latency	Area (μm^2)
[11]	67	1.25	0.06
[12]	29	0.75	–
[13]	18	0.75	0.01
[14]	14	0.5	0.02
New	13	0.5	0.02

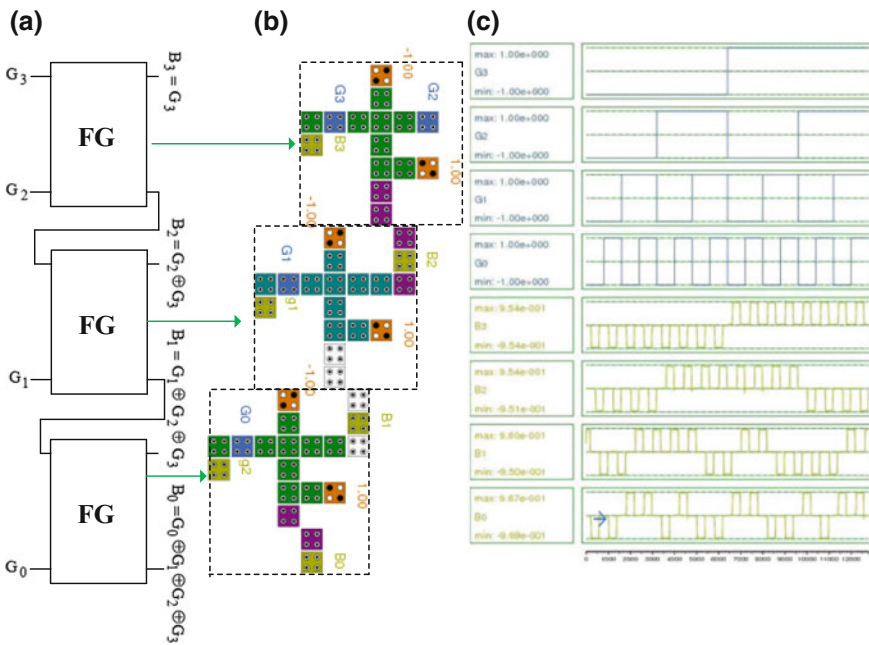


Fig. 3 Reversible four-input gray-to-binary code converter **a** Functional diagram **b** quantum-dot cell layout **c** timing waveform

Ex-OR gates were settled in the specified logic manner. The function diagram and cell layout of binary-to-gray are exhibited in Fig. 2a, b. Figure 2c presents the result of binary-to-gray converter. In this result, settled outputs are correctly with zero latency. The second code converter is gray-to-binary, which was drawn in Fig. 3a. The gray-to-binary design in QCA is presented in Fig. 3b, which was utilized by the less cell count, latency, and two clock zones. Figure 3c presents simulation result of proposed gray-to-binary. In this result attained correctly logic signal, zero latency is achieved in output B₃, B₂, and B₁, whereas B₀ after one clock cycle delay.

3.3 Reversible Binary Incrementer in QCA

In the proposed scheme, we have shown pipeline design of binary incrementer in size of 1-bit, 2-bit, and 3-bit in QCA. With a pipeline design in QCA of binary incrementer, we utilize Peres gate as a building block. Implementation of Peres gate in QCA has been presented in Fig. 4b. It is noted that the latency of the design in large size order of binary incrementer has been diminished. Peres gate design in QCA has been achieved by use of Ex-OR. Peres gate is a reversible gate having three inputs and three outputs as shown in Fig. 4a. Here, the input to output mapping is $P = A$, $Q = A \oplus B$, $R = AB \oplus C$ and the quantum cost of this gate is four. The simulation result of the Peres gate is shown in Fig. 4c. In simulation result, it is shown that P and Q outputs have zero latency, whereas R output has one latency (clock delay). This quantum-dot cell of PG is achieved by taking three majority gates and two inverters.

3.4 Reversible 1-Bit Binary Incrementer

In the quantum-cell design of reversible binary incrementer only by normal cell, and fix polarization cell are utilized. Most of the existing binary incrementers are based on coplanar or multilayer [8]. In this work, we are targeting the normal and fix cells based design. Figure 5a shows the binary incrementer block for one bit. The proposed Peres gate implemented reversible binary incrementer circuit is shown in Fig. 5b. Figure 5c, d shows the cell layout and simulation results related to binary incrementer, respectively.

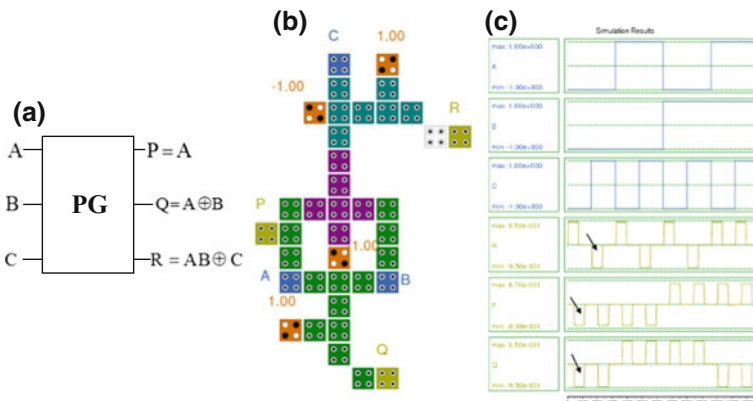


Fig. 4 Reversible PG **a** functional diagram **b** quantum-dot cell layout **c** timing waveform

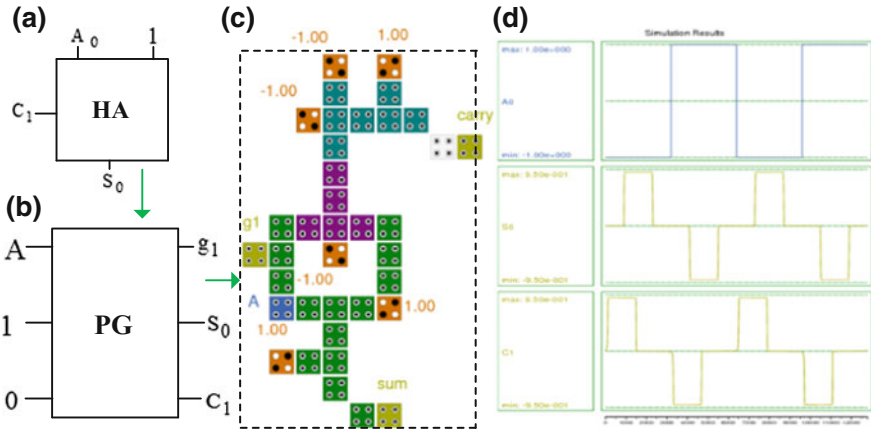


Fig. 5 Binary incrementer **a** Half adder as Binary incremental **b** Peres gate as an incremental **c** quantum-dot cell of PG as half adder **d** timing waveform

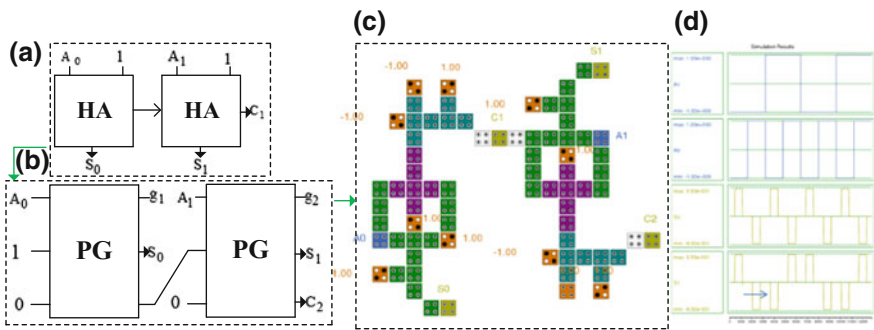


Fig. 6 2-bit reversible binary incrementer **a** functional diagram **b** quantum-dot cell **c** timing waveform

3.5 2-Bit Reversible Binary Incrementer

A 2-bit binary incrementer is implemented with cascading two half adders as shown in Fig. 6a. Here A_1, A_0 is 2-bit input binary number and S_1, S_0 represents incremented output. A structure of 2-bit binary incrementer using Peres gates is shown in Fig. 6b. QCA schematic and simulation results of the proposed 2-bit binary incrementer are drawn in Fig. 6c and Fig. 6d respectively. In timing waveform result, arrow sign indicates the output signal that has arrived at that point after two latency.

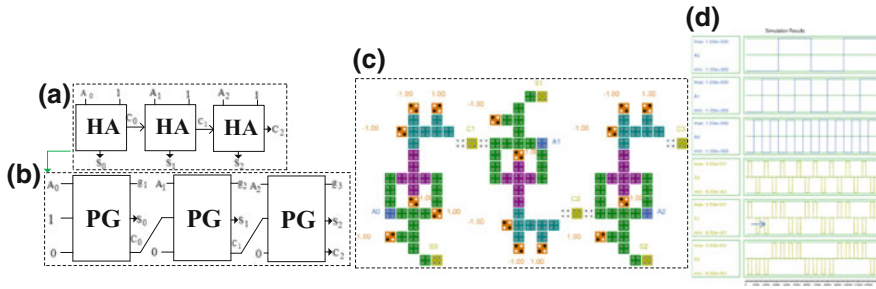


Fig. 7 Reversible 3-bit binary incrementer **a** functional diagram **b** quantum-dot cell **c** timing waveform

3.6 3-Bit Reversible Binary Incrementer

The 3-bit binary incrementer is implemented using three number of cascaded HA as shown in Fig. 7a. Here, $A_2A_1A_0$ represents 3-bit input number and $S_2S_1S_0$ represents 3-bit output number. The 3-bit reversible binary incrementer with the PG's is shown in Fig. 7b. Its proposed QCA layout and simulation results are drawn in Fig. 7c, d, respectively. The QCADesigner has two type of engines that are available for simulation. Coherence vector and the bistable approximation are two engines [15, 16]. In this work, we use a bistable engine which is a default set of parameters.

3.7 Reversible n -Bit Binary Incrementer

The structure of 1-bit reversible binary incrementer requires one Peres gate as shown in Fig. 5 and it has one garbage output. Two numbers of Peres gates are used in designing 2-bit binary incrementer having two garbage outputs as shown in Fig. 6. Figure 7 shows that three Peres gates are used in the design of 3-bit reversible binary incrementer, and it has three garbage outputs. Similarly to design n -bit reversible binary incrementer n -number of Peres gates are used with n -number of garbage outputs. The structure of n -bit binary incrementer using PG's is shown in Fig. 8.

4 Comparative Statistics

Table 1 explores the comparison of the quantum-dot cell circuits of reversible binary-to-gray and gray-to-binary converters. Table 2 shows that the new binary-to-gray converter has an improvement of 59% in cell count and 36%

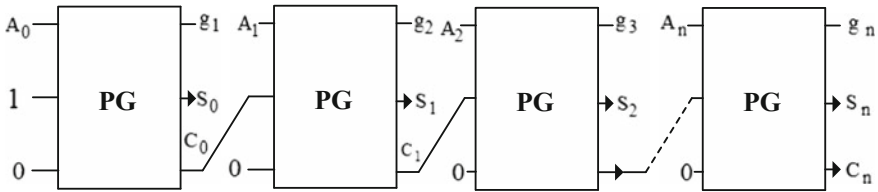


Fig. 8 Functional diagram of n-bit reversible binary incrementer

Table 2 Comparison of QCA layouts of reversible binary-to-gray code converters

	Design	Capability	Cell count	Area	Crossover	Latency
Binary-to-gray	[10]	3-bit	90	0.95	0	2
	[17]	4-bit	192	0.34	0	2
	[9]	3-bit	118	0.38	1	0.75
	[13]	4-bit	108	0.11	1	0.75
	New	4-bit	44	0.07	0	0.5
Gray-to-binary	[10]	3-bit	194	0.28	0	4
	[17]	4-bit	269	0.69	0	6
	[9]	3-bit	99	–	0	0.75
	[13]	4-bit	69	0.10	0	0.75
	New	4-bit	50	0.09	0	1

improvement in the total area over the previous design [9]. This circuit also has no crossover and 33% improvement in latency [9]. The proposed reversible gray-to-binary code converter has 27% improvement in cell count and 10% improvement in the area over the previous work [9].

The proposed quantum-dot cell of PG and 1-bit binary incrementer have 60 and 6% improvement in terms of cell count and area over [8], respectively. Our proposed reversible 2-bit binary incrementer has 60 and 52% improvement in cell count and area over existing QCA layout [8], respectively. Similarly, the proposed reversible 3-bit binary incrementer has 64 and 34% improvement in cell count and area compared to existing designs [8], respectively. The overall evaluation is drawn in Table 3. It is realized that there is a significant enhancement of results in the proposed QCA layout designs.

Table 3 Comparison of Peres gate and reversible binary incrementer QCA layouts

		MV No	INV No.	CC	Area (μm^2)	Crossover	Latency
Peres gate	[8]	7	4	97	0.075	1	1
	New	3	2	38	0.070	0	1
1-bit reversible incrementer	[8]	7	4	97	0.075	1	1
	New	3	2	38	0.070	0	1
2-bit reversible incrementer	[8]	14	8	196	0.272	2	2
	New	6	4	77	0.130	0	2
3-bit reversible incrementer	[8]	21	12	321	0.274	3	3
	New	9	6	113	0.18	0	2

5 Conclusion

This paper has reported the novel designs of reversible code converters and binary incrementer using QCA technology. All layouts are implemented in QCADesigner tool. The simulation results of all the QCA layouts have confirmed the functionality of the designs. All these designs have achieved a higher efficiency compared to previous works available in the literature. We also presented optimized designs of Feynman gate and the Peres gate in QCA. These two are basic gates having a low quantum cost which can be used for designing reversible circuits in QCA technology. Therefore, all our proposed QCA layouts can be used as an effective architecture for designing efficient digital circuits with the power of reversibility and QCA technology.

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