Optical Quadruple Toffoli and Fredkin Gate Using SLM and Savart Plate

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Abstract. Reversible computing not only reflects a fundamental law of physics, but also offers potential to achieve zero dissipation by preventing entropy loss during computation. With the demand of time, reversible logic is becoming more and more prominent to deal with modern technology. In optical computation the multi-valued logic system is the most important area where trinary and quadruple valued logic systems are demanding their uniqueness in handling big data. In this paper we have proposed the optical quadruple Toffoli and Fredkin gate using Spatial Light Modulator (SLM) and Savart Plate for realization. SLM and Savart Plate can play a significant role in the field of ultra fast optical signal processing.

Keywords: Di-bit · Fredkin Gate · Quadruple · Savart Plate · SLM · Toffoli Gate

1 Introduction

In recent years, the multi-valued logic (MVL) system is becoming highly praised by the scientific community for its' inherent property of handling huge volume of data. The several inherent potential opportunities of MVL circuits may be explored further in the improvement of present VLSI circuit designs. V. Patel and K.S. Gurumurthy demonstrated the arithmetic operations like addition, subtraction and multiplications in modulo-4 arithmetic in Galois field using MVL [1]. Quaternary to binary and binary to quaternary converters [2] are also designed. The two input logic operations, half-adder, full-adder, full sub-tractor, one-bit data comparator, etc. are can be implemented optically using this architecture.

With the demand of tremendous operational speed and data processing, computing field is evolved with many new ideas. These include optical processor for switches and the logical development of MVL from binary. The parallel operation is advantageous for optical processor. MVL can also be implemented in optical system using the polarization states of light along with it's presence or absence [3]. The signed digit number system was introduced by the pioneering works of Avizienis [4]. The modified signed digit [5–7] or modified trinary [8] system also suggests the carry free operation. However, Lukasiewicz [9] initiated the use of ternary logic based on three states.

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The modified trinary system to a quadruple-valued logic system using SLM and Savart Plate is already implemented [10, 11].

In many applications for lossless data processing the design of reversible logic is highly demanding [12, 13]. Optical and quantum computing is revolutionary computing paradigms with the help of Conservative and reversible logic gates. With this aim, we have presented optical Quadruple Toffoli Gate and optical Quadruple Fredkin Gate using SLM and Savart Plate in this paper. The simulation results confirm the described method.

The proposed paper is arranged as follows: The quadruple valued logic systems are reported in Sect. 2. Section 3 is for representation of Truth Tables in Di-bit Format. Section 4 presents the working principle of basic building block using SLM and Savart Plate. The working principle and design of Quadruple Toffoli and Fredkin Gate are presented in Sects. 5 and 6. Logical simulation results are shown in Sect. 7 and concluding remarks are given in Sect. 8.

2 Quadruple Valued Logic System

The quadruple valued logic system consists of four states. The states may be classified as the true, partly true, partly false and the false. Here we are considering four states explicitly as {0, 1, 2, 3} and their corresponding di-bit representations as {00, 01, 10, 11}. The logical states, their representations and corresponding di-bit representations and the state of polarization are given in Table 1.

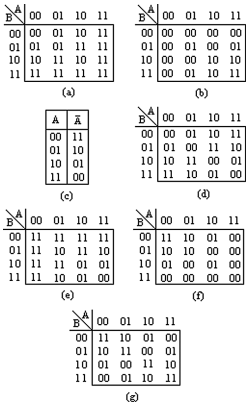
Table 1. Quadruple valued logic system

Logical state	Represented by	Di-bit representation	State of polarization
False/Wrong information	0	00	No light
Partial information	1	01	Vertical polarization
Partial information (Complement of 1)	2	10	Horizontal polarization
True/Complete information	3	11	Presence of both the Horizontal & Vertical polarization

3 Representation of Truth Tables in Di-bit Format

In the present system the normal logical gates e.g., OR, AND, NOT, XOR, NAND, NOR and XNOR are represented in di-bit format and the corresponding truth table is given in Table 2.

Table 2. Truth tables for (a) OR, (b) AND, (c) NOT (d) XOR, (e) NAND, (f) NOR and (g) XNOR Gates



4 The Basic Building Block

Figure 1 represents the basic building block to implement the logical operations in quadruple valued logic system and Fig. 2 represents the operation in flow chart format. The Light that is coming out from a laser source L is incident on the polarizer P. After passing through the polarizer P it is incident on the Savart Plate S_1 as shown in Figs. 1 and 2. S_1 is used to split the light into two orthogonal components (horizontal polarization and vertical polarization). The two components of input beam are controlled by the electrically addressable negative SLMs, P_1 and P_2. The negative SLM is transparent when no electric voltage is applied on it and it becomes opaque when an electric voltage is applied on it. The property of positive SLM is just opposite. The inputs are considered as in the form of di-bit format. The Savart Plate S_2 combines the outputs from SLMs and provides the final output.

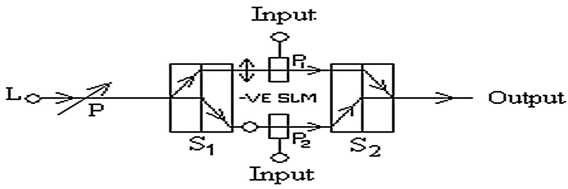


Fig. 1. The basic building block

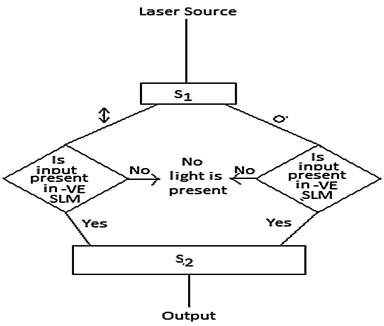


Fig. 2. The flow chart of basic building block

5 Quadruple Toffoli Gate: Principle and Design

Toffoli Gate is a universal reversible logic gate [14, 15]. A, B, C and X, Y, Z are the three inputs and outputs, respectively. The Boolean expression of the Toffoli Gate is given below.

$$\begin{aligned} X &= A \\ Y &= B \\ Z &= A \cdot B \oplus C \end{aligned} \tag{1}$$

Table 3 represents the truth table of Toffoli Gate.

Table 3. Binary truth table of Toffoli Gate.

Input			Output		
A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Here we are going to discuss about Quadruple Toffoli Gate with di-bit representation which is in Table 4.

Table 4. Truth table of Quadruple Toffoli Gate

A	A_1	A_2	B	B_1	B_2	C	C_1	C_2	X	X_1	X_2	Y	Y_1	Y2	Z	Z_1	Z_2
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	2	1	0	0	0	0	0	0	0	2	1	0
0	0	0	0	0	0	3	1	1	0	0	0	0	0	0	3	1	1
0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	1	0	1	1	0	1	0	0	0	1	0	1	1	0	1
0	0	0	1	0	1	2	1	0	0	0	0	1	0	1	2	1	0
0	0	0	1	0	1	3	1	1	0	0	0	1	0	1	3	1	1
0	0	0	2	1	0	0	0	0	0	0	0	2	1	0	0	0	0
0	0	0	2	1	0	1	0	1	0	0	0	2	1	0	1	0	1
0	0	0	2	1	0	2	1	0	0	0	0	2	1	0	2	1	0
0	0	0	2	1	0	3	1	1	0	0	0	2	1	0	3	1	1
0	0	0	3	1	1	0	0	0	0	0	0	3	1	1	0	0	0
0	0	0	3	1	1	1	0	1	0	0	0	3	1	1	1	0	1
0	0	0	3	1	1	2	1	0	0	0	0	3	1	1	2	1	0
0	0	0	3	1	1	3	1	1	0	0	0	3	1	1	3	1	1
1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	1	1	0	1	0	0	0	1	0	1
1	0	1	0	0	0	2	1	0	1	0	1	0	0	0	2	1	0
1	0	1	0	0	0	3	1	1	1	0	1	0	0	0	3	1	1
1	0	1	1	0	1	0	0	0	1	0	1	1	0	1	1	0	1
1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	0	0	0
1	0	1	1	0	1	2	1	0	1	0	1	1	0	1	3	1	1
1	0	1	1	0	1	3	1	1	1	0	1	1	0	1	2	1	0
1	0	1	2	1	0	0	0	0	1	0	1	2	1	0	0	0	0
1	0	1	2	1	0	1	0	1	1	0	1	2	1	0	1	0	1
1	0	1	2	1	0	2	1	0	1	0	1	2	1	0	2	1	0
1	0	1	2	1	0	3	1	1	1	0	1	2	1	0	3	1	1
1	0	1	3	1	1	0	0	0	1	0	1	3	1	1	1	0	1
1	0	1	3	1	1	1	0	1	1	0	1	3	1	1	0	0	0
1	0	1	3	1	1	2	1	0	1	0	1	3	1	1	3	1	1
1	0	1	3	1	1	3	1	1	1	0	1	3	1	1	2	1	0
2	1	0	0	0	0	0	0	0	2	1	0	0	0	0	0	0	0
2	1	0	0	0	0	1	0	1	2	1	0	0	0	0	1	0	1
2	1	0	0	0	0	2	1	0	2	1	0	0	0	0	2	1	0
2	1	0	0	0	0	3	1	1	2	1	0	0	0	0	3	1	1
2	1	0	1	0	1	0	0	0	2	1	0	1	0	1	0	0	0
2	1	0	1	0	1	1	0	1	2	1	0	1	0	1	1	0	1
2	1	0	1	0	1	2	1	0	2	1	0	1	0	1	2	1	0
2	1	0	1	0	1	3	1	1	2	1	0	1	0	1	3	1	1

(*continued*)

Table 4. (*continued*)

A	A_1	A_2	B	B_1	B_2	C	C_1	C_2	X	X_1	X_2	Y	Y_1	Y2	Z	Z_1	Z_2
2	1	0	2	1	0	0	0	0	2	1	0	2	1	0	2	1	0
2	1	0	2	1	0	1	0	1	2	1	0	2	1	0	3	1	1
2	1	0	2	1	0	2	1	0	2	1	0	2	1	0	0	0	0
2	1	0	2	1	0	3	1	1	2	1	0	2	1	0	1	0	1
2	1	0	3	1	1	0	0	0	2	1	0	3	1	1	2	1	0
2	1	0	3	1	1	1	0	1	2	1	0	3	1	1	2	1	0
2	1	0	3	1	1	2	1	0	2	1	0	3	1	1	0	0	0
2	1	0	3	1	1	3	1	1	2	1	0	3	1	1	1	0	1
3	1	1	0	0	0	0	0	0	3	1	1	0	0	0	0	0	0
3	1	1	0	0	0	1	0	1	3	1	1	0	0	0	1	0	1
3	1	1	0	0	0	2	1	0	3	1	1	0	0	0	2	1	0
3	1	1	0	0	0	3	1	1	3	1	1	0	0	0	3	1	1
3	1	1	1	0	1	0	0	0	3	1	1	1	0	1	1	0	1
3	1	1	1	0	1	1	0	1	3	1	1	1	0	1	1	0	1
3	1	1	1	0	1	2	1	0	3	1	1	1	0	1	3	1	1
3	1	1	1	0	1	3	1	1	3	1	1	1	0	1	2	1	0
3	1	1	2	1	0	0	0	0	3	1	1	2	1	0	2	1	0
3	1	1	2	1	0	1	0	1	3	1	1	2	1	0	3	1	1
3	1	1	2	1	0	2	1	0	3	1	1	2	1	0	0	0	0
3	1	1	2	1	0	3	1	1	3	1	1	2	1	0	1	0	1
3	1	1	3	1	1	0	0	0	3	1	1	3	1	1	3	1	1
3	1	1	3	1	1	1	0	1	3	1	1	3	1	1	2	1	0
3	1	1	3	1	1	2	1	0	3	1	1	3	1	1	1	0	1
3	1	1	3	1	1	3	1	1	3	1	1	3	1	1	0	0	0

The SLM and Savart Plate based circuit for Quadruple Toffoli Gate is given in Fig. 3.

The polarized parallel beam coming from the Laser source L through polarizer P is incident on the beam splitter BS_7. The beam is splitted into two directions by BS_7 as shown Fig. 3. From the Fig. 3 it can also be seen that the output of S_{16} gives the output X, the output of S_{21} provides the output Y and the output of S_7 and S_{14} combines by the beam splitter BS_5 and produce the another output Z. The functions of SLM and Savart Plate are already described in Sect. 4. From Table 4 it can be seen that total 64 cases are considered. Some cases are discussed as follows:

- When A = 0 (A_1 = 0, A_2 = 0), B = 0 (B_1 = 0, B_2 = 0) and C = 0 (C_1 = 0, C_2 = 0) then no light is present at the output of S_{16} and $S_{21,}$ hence X = 0 (X_1 = 0, X_2 = 0) and Y = 0 (Y_1 = 0, Y_2 = 0). As the input C = 0 so there will be no light at the output of S_7 and S_{14}, so the output, Z = 0 (Z_1 = 0, Z_2 = 0).
- As A = 0 (A_1 = 0, A_2 = 0), B = 3 (B_1 = 1, B_2 = 1) and C = 0 (C_1 = 0, C_2 = 0) then no light is present at the output of S_{16}, hence X = 0 (X_1 = 0, X_2 = 0). The output of S_{21} consists of both vertical and horizontal polarized light, hence

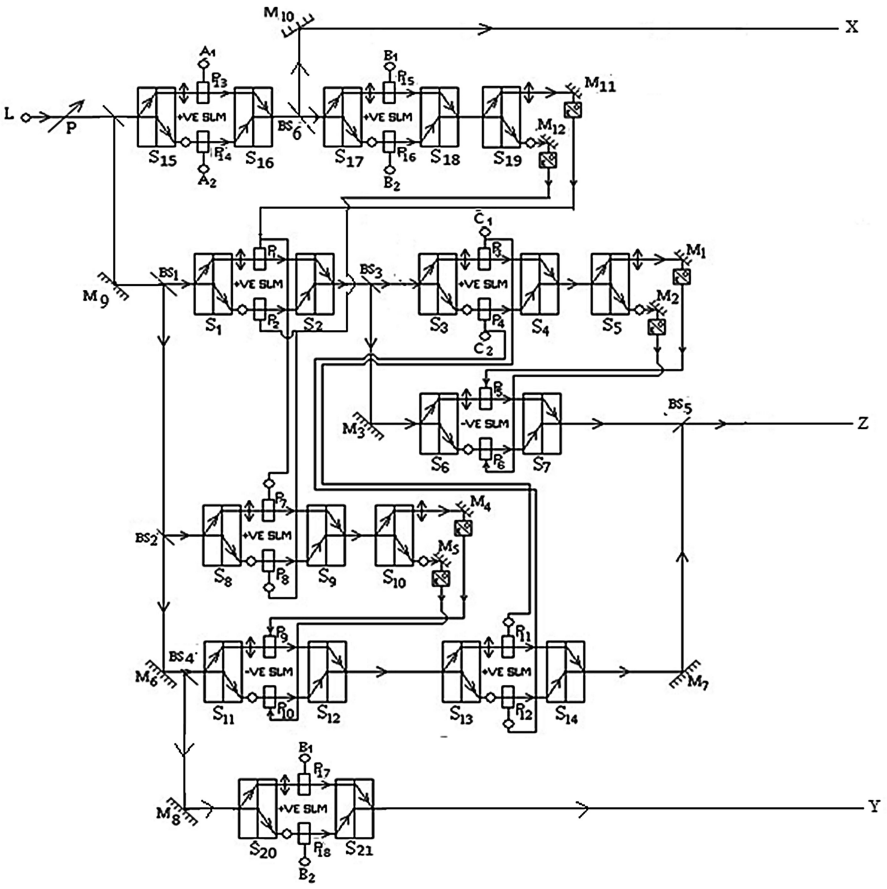


Fig. 3. SLM and Savart Plate based Quadruple Toffoli Gate

Y = 3 ($Y_1 = 1$, $Y_2 = 1$). As AB = 0 ($A_1B_1 = 0$, $A_2B_2 = 0$) and C = 0 so there will be no light at the output of S_7 and S_{14} i.e. Z = 0 ($Z_1 = 0$, $Z_2 = 0$).

- When A = 1 ($A_1 = 0$, $A_2 = 1$), B = 1 ($B_1 = 0$, $B_2 = 1$) and C = 1 ($C_1 = 0$, $C_2 = 1$) then X = 1 ($X_1 = 0$, $X_2 = 1$) as X = A. The output of S_{21} consists of only vertically polarized light, hence Y = 1 ($Y_1 = 0$, $Y_2 = 1$). As AB = 1 ($A_1B_1 = 0$, $A_2B_2 = 1$) and C = 1 so there will be no light at the output of S_7 and S_{14} i.e. Z = 0 ($Z_1 = 0$, $Z_2 = 0$).
- When A = 1 ($A_1 = 0$, $A_2 = 1$), B = 2 ($B_1 = 1$, $B_2 = 0$) and C = 1 ($C_1 = 0$, $C_2 = 1$) then X = 1 ($X_1 = 0$, $X_2 = 1$) as X = A. Only horizontally polarized light is present at the output of S_{21} i.e. Y = 2 ($Y_1 = 1$, $Y_2 = 0$). As AB = 0 ($A_1B_1 = 0$, $A_2B_2 = 0$) and C = 1 so there is no light at the output of S_7 and the output of S_{14} consists of vertically polarized light i.e. Z = 1 ($Z_1 = 0$, $Z_2 = 1$).
- When A = 2 ($A_1 = 1$, $A_2 = 0$), B = 2 ($B_1 = 1$, $B_2 = 0$) and C = 2 ($C_1 = 1$, $C_2 = 0$) then X = 2 ($X_1 = 1$, $X_2 = 0$) as X = A. Only horizontally polarized light is present

at the output of S_{21} i.e. Y = 2 ($Y_1 = 1$, $Y_2 = 0$). As AB = 2 ($A_1B_1 = 1$, $A_2B_2 = 0$) and C = 2 so there is no light at the output of S_7 and S_{14}. The output is Z = 0 ($Z_1 = 0$, $Z_2 = 0$).

- When A = 2 ($A_1 = 1$, $A_2 = 0$), B = 3 ($B_1 = 1$, $B_2 = 1$) and C = 2 ($C_1 = 1$, $C_2 = 0$) then X = 2 ($X_1 = 1$, $X_2 = 0$) as X = A. The vertical and horizontal polarized lights are present at the output of S_{21}, hence Y = 3 ($Y_1 = 1$, $Y_2 = 1$). As AB = 2 ($A_1B_1 = 1$, $A_2B_2 = 0$) and C = 2 so there is no light at the output of S_7 and S_{14}. The output is Z = 0 ($Z_1 = 0$, $Z_2 = 0$).
- When A = 2 ($A_1 = 1$, $A_2 = 0$), B = 3 ($B_1 = 1$, $B_2 = 1$) and C = 3 ($C_1 = 1$, $C_2 = 1$) then X = 2 ($X_1 = 1$, $X_2 = 0$) as X = A. The output of S_{21} consists of both vertical and horizontal polarized light, hence Y = 3 ($Y_1 = 1$, $Y_2 = 1$). As AB = 2 ($A_1B_1 = 1$, $A_2B_2 = 0$) and C = 3 so there is no light at the output of S_7 and the output of S_{14} consists of vertically polarized light. The output consists of only vertically polarized light i.e. Z = 1 ($Z_1 = 0$, $Z_2 = 1$).
- When A = 3 ($A_1 = 1$, $A_2 = 1$), B = 0 ($B_1 = 0$, $B_2 = 0$) and C = 3 ($C_1 = 1$, $C_2 = 1$) then X = 3 ($X_1 = 1$, $X_2 = 1$) as X = A. No light is present at the output of S_{21} i.e. Y = 0 ($Y_1 = 0$, $Y_2 = 0$). As AB = 0 ($A_1B_1 = 0$, $A_2B_2 = 0$) and C = 3, the output of S_{14} consists of both vertical and horizontal polarized light. There is no light at the output of S_7. The final output is Z = 3 ($Z_1 = 1$, $Z_2 = 1$).
- When A = 3 ($A_1 = 1$, $A_2 = 1$), B = 3 ($B_1 = 1$, $B_2 = 1$) and C = 3 ($C_1 = 1$, $C_2 = 1$) then X = 3 ($X_1 = 1$, $X_2 = 1$) as X = A. The vertical and horizontal polarized lights are present at the output of S_{21}, hence Y = 3 ($Y_1 = 1$, $Y_2 = 1$). As AB = 3 ($A_1B_1 = 1$, $A_2B_2 = 1$) and C = 3 so no light is present at the output of S_{26} and S_{33}. No light is present at the output of Z i.e. Z = 0 ($Z_1 = 0$, $Z_2 = 0$).

In the same way the other cases can be described according to the Table 4.

6 Quadruple Fredkin Gate: Principle and Design

The Fredkin gate is a computational circuit suitable for reversible computing [14]. A, B, C and X, Y, Z are the three inputs and outputs, respectively. The Boolean expression of the Fredkin Gate is given below.

$$\left.\begin{aligned} X &= A \\ Y &= \overline{A} \cdot B + A \cdot C \\ Z &= A \cdot B + \overline{A} \cdot C \end{aligned}\right\} \tag{2}$$

Figure 4 represents the block diagram and Table 5 shows the truth table of Fredkin Gate.

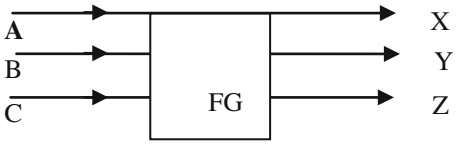


Fig. 4. Block diagram of Fredkin Gate

Table 5. Binary truth table of Fredkin Gate

Inputs			Outputs		
A	B	C	X	Y	Z
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Here we are going discuss about Quadruple Fredkin Gate and the corresponding truth table is given in Table 6.

Table 6. Truth table of Quadruple Fredkin Gate

A	A_1	A_2	B	B_1	B_2	C	C_1	C_2	X	X_1	X_2	Y	Y_1	Y2	Z	Z_1	Z_2
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	0	1	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	2	1	0	0	0	0	0	0	0	2	1	0
0	0	0	0	0	0	3	1	1	0	0	0	0	0	0	3	1	1
0	0	0	1	0	1	0	0	0	0	0	0	1	0	1	0	0	0
0	0	0	1	0	1	1	0	1	0	0	0	1	0	1	1	0	1
0	0	0	1	0	1	2	1	0	0	0	0	1	0	1	2	1	0
0	0	0	1	0	1	3	1	1	0	0	0	1	0	1	3	1	1
0	0	0	2	1	0	0	0	0	0	0	0	2	1	0	0	0	0
0	0	0	2	1	0	1	0	1	0	0	0	2	1	0	1	0	1
0	0	0	2	1	0	2	1	0	0	0	0	2	1	0	2	1	0
0	0	0	2	1	0	3	1	1	0	0	0	2	1	0	3	1	1
0	0	0	3	1	1	0	0	0	0	0	0	3	1	1	0	0	0
0	0	0	3	1	1	1	0	1	0	0	0	3	1	1	1	0	1
0	0	0	3	1	1	2	1	0	0	0	0	3	1	1	2	1	0
0	0	0	3	1	1	3	1	1	0	0	0	3	1	1	3	1	1
1	0	1	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0
1	0	1	0	0	0	1	0	1	1	0	1	1	0	1	0	0	0
1	0	1	0	0	0	2	1	0	1	0	1	0	0	0	2	1	0
1	0	1	0	0	0	3	1	1	1	0	1	1	0	1	2	1	0
1	0	1	1	0	1	0	0	0	1	0	1	0	0	0	1	0	1
1	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1
1	0	1	1	0	1	2	1	0	1	0	1	0	0	0	3	1	1
1	0	1	1	0	1	3	1	1	1	0	1	1	0	1	3	1	1

(*continued*)

Table 6. (*continued*)

A	A_1	A_2	B	B_1	B_2	C	C_1	C_2	X	X_1	X_2	Y	Y_1	Y2	Z	Z_1	Z_2
1	0	1	2	1	0	0	0	0	1	0	1	2	1	0	0	0	0
1	0	1	2	1	0	1	0	1	1	0	1	3	1	1	0	0	0
1	0	1	2	1	0	2	1	0	1	0	1	2	1	0	2	1	0
1	0	1	2	1	0	3	1	1	1	0	1	3	1	1	2	1	0
1	0	1	3	1	1	0	0	0	1	0	1	2	1	0	1	0	1
1	0	1	3	1	1	1	0	1	1	0	1	3	1	1	1	0	1
1	0	1	3	1	1	2	1	0	1	0	1	2	1	0	3	1	1
1	0	1	3	1	1	3	1	1	1	0	1	3	1	1	3	1	1
2	1	0	0	0	0	0	0	0	2	1	0	0	0	0	0	0	0
2	1	0	0	0	0	1	0	1	2	1	0	0	0	0	1	0	1
2	1	0	0	0	0	2	1	0	2	1	0	2	1	0	0	0	0
2	1	0	0	0	0	3	1	1	2	1	0	2	1	0	1	0	1
2	1	0	1	0	1	0	0	0	2	1	0	1	0	1	0	0	0
2	1	0	1	0	1	1	0	1	2	1	0	1	0	1	1	1	1
2	1	0	1	0	1	2	1	0	2	1	0	3	1	1	0	0	0
2	1	0	1	0	1	3	1	1	2	1	0	3	1	1	1	1	1
2	1	0	2	1	0	0	0	0	2	1	0	0	0	0	2	1	0
2	1	0	2	1	0	1	0	1	2	1	0	0	0	0	3	1	1
2	1	0	2	1	0	2	1	0	2	1	0	2	1	0	2	1	0
2	1	0	2	1	0	3	1	1	2	1	0	2	1	0	3	1	1
2	1	0	3	1	1	0	0	0	2	1	0	2	1	0	3	1	1
2	1	0	3	1	1	1	0	1	2	1	0	2	1	0	3	1	1
2	1	0	3	1	1	2	1	0	2	1	0	2	1	0	2	1	0
2	1	0	3	1	1	3	1	1	2	1	0	2	1	0	3	1	1
3	1	1	0	0	0	0	0	0	3	1	1	0	0	0	0	0	0
3	1	1	0	0	0	1	0	1	3	1	1	1	0	1	0	0	0
3	1	1	0	0	0	2	1	0	3	1	1	2	1	0	0	0	0
3	1	1	0	0	0	3	1	1	3	1	1	3	1	1	0	0	0
3	1	1	1	0	1	0	0	0	3	1	1	0	0	0	1	0	1
3	1	1	1	0	1	1	0	1	3	1	1	1	0	1	1	0	1
3	1	1	1	0	1	2	1	0	3	1	1	2	1	0	1	0	1
3	1	1	1	0	1	3	1	1	3	1	1	3	1	1	1	0	1
3	1	1	2	1	0	0	0	0	3	1	1	0	0	0	2	1	0
3	1	1	2	1	0	1	0	1	3	1	1	1	0	1	2	1	0
3	1	1	2	1	0	2	1	0	3	1	1	2	1	0	2	1	0
3	1	1	2	1	0	3	1	1	3	1	1	3	1	1	2	1	0
3	1	1	3	1	1	0	0	0	3	1	1	0	0	0	3	1	1
3	1	1	3	1	1	1	0	1	3	1	1	1	0	1	3	1	1
3	1	1	3	1	1	2	1	0	3	1	1	2	1	0	3	1	1
3	1	1	3	1	1	3	1	1	3	1	1	3	1	1	3	1	1

The SLM and Savart Plate based circuit for Quadruple Fredkin Gate is given in Fig. 5. The polarized parallel beam coming from the Laser source L through polarizer P is incident on the beam splitter BS_1. The beam is splitted into two directions by BS_1 as shown Fig. 5. Two parts of light from the output of BS_1 are incident on the Savart Plate S_1 and beam splitter BS_3 respectively. The incident beam is splitted into two orthogonal components - the p-polarization (horizontal polarization) and the s-polarization (vertical polarization) by the Savart Plate S_1. The input A (combination of A_1 and A_2) is used to control the positive SLMs P_1 and P_2. The outputs form P_1 and P_2 are recombined by the Savart Plate S_2 and incident on the beam splitter BS_2. From the Fig. 5 it can also be seen that we get output X = A from the output of S_2. $(A \cdot C)$ is the output of S_4, which is incident on S_5. The opto-electrical converters (O/E) are used in the path of the rays to convert the light signal into electric voltage. The output of S_5 is incident on the opto-electrical converters (O/E). The output from opto-electrical converter (O/E) will act as control input terminals for P_7 and P_8. $\bar{A}$ is the output of S_{12}, which one after passing through S_{13} and opto-electrical converters (O/E) will act as control input terminals for P_{13} and P_{14}. $(\bar{A} \cdot B)$ is the output of S_{19} and it is incident on S_{20}. The SLMs P_{11} and P_{12} are controlled by the output of S_{20} which is again converted into electrical signal by the use of opto-electrical converters (O/E). Finally BS_5 is used to combine the outputs of S_{10} and S_{15} and produce the output $Y = \bar{A} \cdot B + A \cdot C$ $(\bar{A} \cdot C)$ is the output of S_{24} and $(A \cdot B)$ is the output of S_{29}. By the same procedure, finally BS_{12} is used to combine the outputs of S_{32} and S_{34} and produce the output $Z = A \cdot B + \bar{A} \cdot C$. From Table 6 it can be seen that total 64 cases are there. Some cases are explained as follows:

- When A = 0 ($A_1 = 0$, $A_2 = 0$), B = 0 ($B_1 = 0$, $B_2 = 0$) and C = 1 ($C_1 = 0$, $C_2 = 1$) then no light at the output of S_2, hence X = 0 ($X_1 = 0$, $X_2 = 0$). There is no light at the output of S_4, S_{19}, S_{10} and S_{15} i.e. Y = 0 ($Y_1 = 0$, $Y_2 = 0$). As the input C = 1 so there is no light at the output of S_{29} and S_{34} but the outputs of S_{24} and S_{32} consist of vertically polarized light. The vertically polarized light is present at the output of Z i.e. Z = 1 ($Z_1 = 0$, $Z_2 = 1$).
- When A = 0 ($A_1 = 0$, $A_2 = 0$), B = 0 ($B_1 = 0$, $B_2 = 0$) and C = 2 ($C_1 = 1$, $C_2 = 0$) then X = 0 ($X_1 = 0$, $X_2 = 0$) as X = A. No light is present at the output of S_4, S_{19}, S_{10} and S_{15} i.e. Y = 0 ($Y_1 = 0$, $Y_2 = 0$). The output of S_{24} and S_{32} consist of horizontally polarized light and no light is present at the output of S_{29} and S_{34}. Hence the output is Z = 2 ($Z_1 = 1$, $Z_2 = 0$).
- When A = 0 ($A_1 = 0$, $A_2 = 0$), B = 0 ($B_1 = 0$, $B_2 = 0$) and C = 3 ($C_1 = 1$, $C_2 = 1$) then X = 0 ($X_1 = 0$, $X_2 = 0$) as X = A. No light is present at the output of S_4, S_{19}, S_{10} and S_{15} i.e. Y = 0 ($Y_1 = 0$, $Y_2 = 0$). As the input C = 3 so no light is present at the output of S_{29} and S_{34} but both vertically and horizontally polarized lights are present at the outputs of S_{24} and S_{32}. Hence the output is Z = 3 ($Z_1 = 1$, $Z_2 = 1$).
- When A = 0 ($A_1 = 0$, $A_2 = 0$), B = 1 ($B_1 = 0$, $B_2 = 1$) and C = 0 ($C_1 = 0$, $C_2 = 0$) then X = 0 ($X_1 = 0$, $X_2 = 0$) as X = A. No light is present at the output of S_4 and S_{10} but vertically polarized light is present at the output of S_{19} and S_{15} i.e. Y = 1 ($Y_1 = 0$, $Y_2 = 1$). As the input C = 0 so no light is present at the output of S_{24}, S_{29}, S_{32} and S_{34}, hence the output is Z = 0 ($Z_1 = 0$, $Z_2 = 0$).

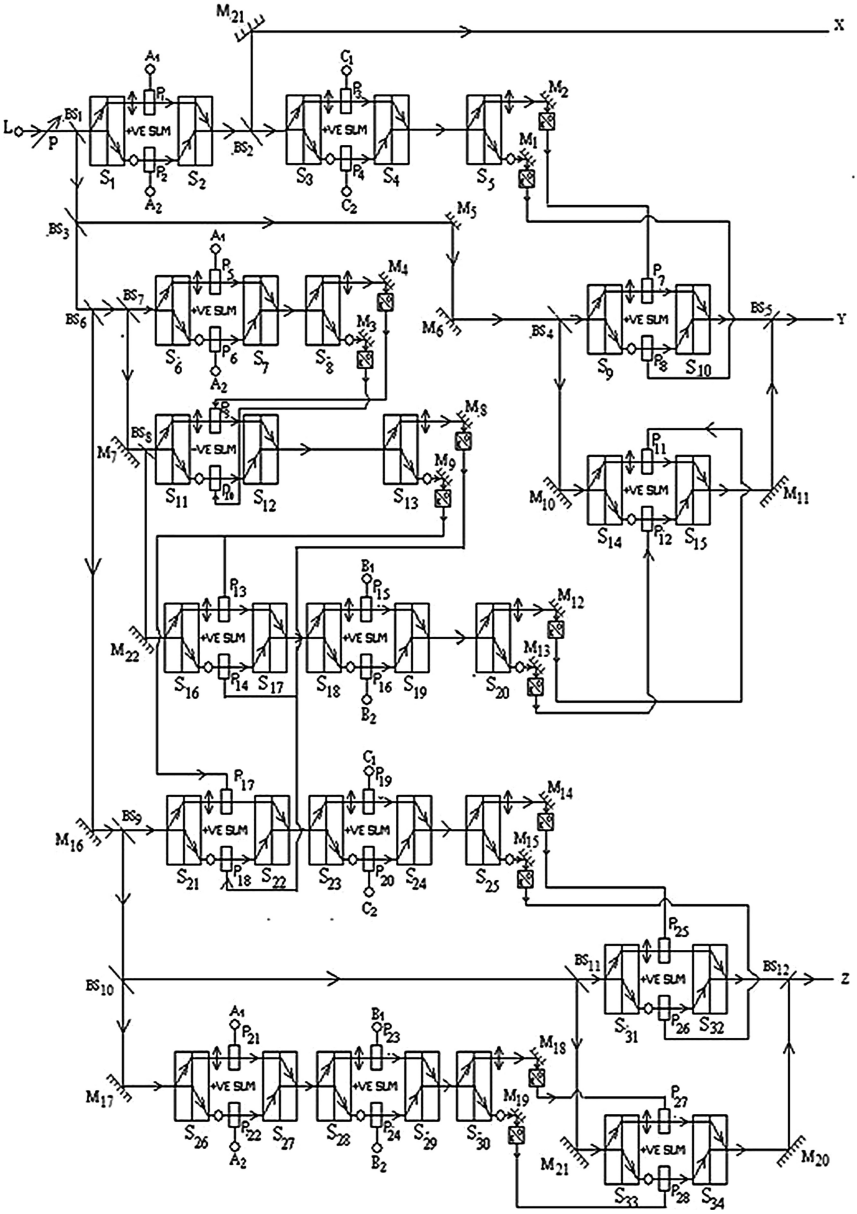


Fig. 5. SLM and Savart Plate based Quadruple Fredkin Gate

- When A = 1 ($A_1 = 0$, $A_2 = 1$), B = 1 ($B_1 = 0$, $B_2 = 1$) and C = 0 ($C_1 = 0$, $C_2 = 0$) then X = 1 ($X_1 = 0$, $X_2 = 1$) as X = A. No light is present at the output of S_4, S_{19}, S_{10} and S_{15} i.e. Y = 0 ($Y_1 = 0$, $Y_2 = 0$). As the input C = 0 so no light is present at the output of S_{24} and S_{32} but only vertically polarized light is present at the output

of S_{29} and S_{34}. The output of Z consists of only vertically polarized light i.e. Z = 1 ($Z_1 = 0$, $Z_2 = 1$).

- When A = 2 ($A_1 = 1$, $A_2 = 0$), B = 2 ($B_1 = 1$, $B_2 = 0$) and C = 0 ($C_1 = 0$, $C_2 = 0$) then X = 2 ($X_1 = 1$, $X_2 = 0$) as X = A. No light is present at the output of S_4, S_{19}, S_{10} and S_{15} i.e. Y = 0 ($Y_1 = 0$, $Y_2 = 0$). As the input C = 0 so no light is present at the output of S_{24} and S_{32} but only horizontally polarized light is present the output of S_{29} and S_{34}. The output of Z consists of only horizontally polarized light i.e. Z = 2 ($Z_1 = 1$, $Z_2 = 0$).
- When A = 3 ($A_1 = 1$, $A_2 = 0$), B = 3 ($B_1 = 1$, $B_2 = 1$) and C = 0 ($C_1 = 0$, $C_2 = 0$) then both polarized lights are present the output of S_2, hence X = 3 ($X_1 = 1$, $X_2 = 1$). No light is present at the output of S_4, S_{19}, S_{10} and S_{15} i.e. Y = 0 ($Y_1 = 0$, $Y_2 = 0$). As the input C = 0 so no light is present at the output of S_{24} and S_{32} but both polarized lights are present at the output of S_{29} and S_{34}. The horizontally and vertically polarized light is present at the output of Z i.e. Z = 3 ($Z_1 = 1$, $Z_2 = 1$).

In the similar way the other cases can be explained according to the Table 6.

7 Performance Evaluation Through Simulation and Discussion: Toffoli Gate and Fredkin Gate

The Boolean function of Toffoli gate and Fredkin Gate are verified by the simulation results using Mathcad-7. The simulated wave forms are shown in Fig. 6(a) and (b) of Toffili and Fredkin Gates respectively. The power of the input pulse is taken A = 2.26 dBm, B = C = 1.13 dBm.

In Fig. 6(a) upper three set waveforms of the timing instant for the occurrence of bit patterns at 0, 5, 10, 15, 20, 25, 30, 35 ps, indicate the input bit sequences, 00001111, 00110011, 01010101 for the input variables A, B, C, respectively. Whereas, the lower three waveforms denote bit sequences 00001111, 00110011, 01010110 for the output variables X, Y, Z respectively.

Now we are going to check the reversible operation from the simulation results for time instant at 15 ps of Fig. 6(a), the output signals are Z = 1, Y = 1, X = 0. From Eq. (1), we get A = 0, B = 1 and C = 1 using these specific outputs.

In Fig. 6(b), upper three set waveforms of the timing instant for the occurrence of bit patterns at 0, 5, 10, 15, 20, 25, 30, 35 ps, indicate the input bit sequences 00001111, 00110011, 01010101 for the input variables A, B, C respectively. Similarly, the lower three waveforms denote bit sequences 00001111, 00110101, 01010011, for the output variables X, Y, Z, respectively.

Now the output signals of reversible operation from the simulation results at 10 ps of Fig. 6(b) are Z = 0, Y = 1, X = 0. From Eq. (2), we have A = 0, B = 1 and C = 0 using these specific outputs.

By the same procedure the reversibility condition can be verified for different bit patterns.

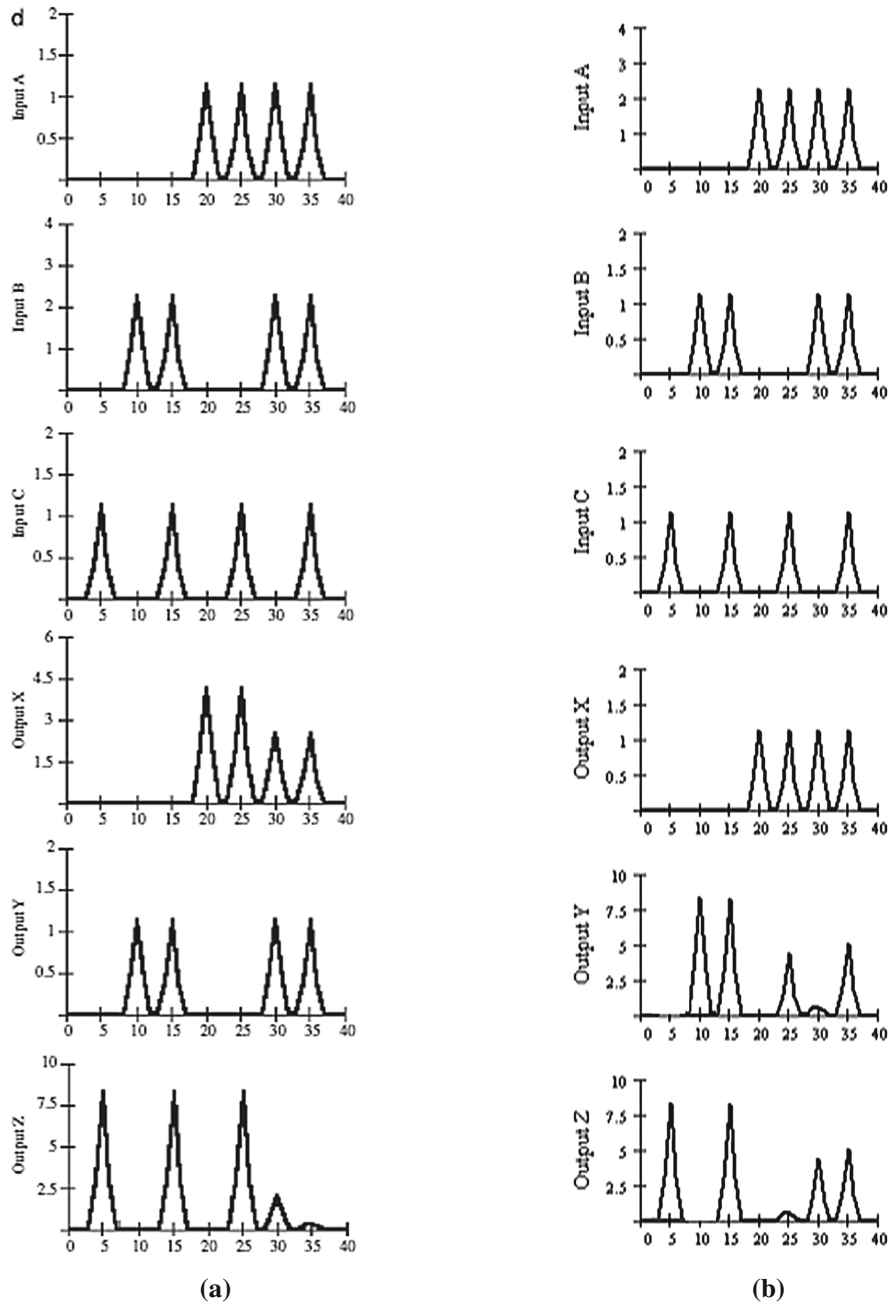


Fig. 6. Simulation result of (a) Toffoli Gate (b) Fredkin Gate: [x-axis: time (ps) and y-axis: power dBm)]

8 Conclusions and Future Work

In this paper we have proposed and described SLM and Savart Plate based reversible Quadruple Toffoli Gate and Quadruple Fredkin Gate. These have wide applications in reversible logic based digital signal processing systems and optical communication systems. The theoretical models developed and the results obtained numerically are useful to future optical reversible logic computing system in four-state implementation which is possible to handle more information at a time. Future work would concentrate realization of various Boolean expressions in the form of system implementation, arithmetic and logical operations in reversible system.

References

1. Patel, K.S.V., Gurumurthy, K.S.: Arithmetic operation in multi valued logic. Int. J. VLSI Des. Commun. Syst. (VLSICS) **1**(1), 13–23 (2010)
2. Chattopadhyay, T., Roy, J.N.: All-optical conversion scheme: binary to quaternary and quaternary to binary number. Opt. Laser Technol. **41**(3), 289–294 (2009)
3. Lohmann, A.W.: Polarization and optical logic. Appl. Opt. **25**, 1594–1597 (1986)
4. Avizienis, A.: Signed-digit number representation for fast parallel arithmetic. IRE Trans. Electron. Comput. **10**, 389–400 (1961)
5. Drake, B.L., Bocker, R.P., Lasher, M.E., Patterson, R.H., Miceli, W.J.: Photonic computing using the modified-signed-digit number representation. Opt. Eng. **25**, 38–43 (1986)
6. Drake, B.L., Bocker, R.P., Lasher, M.E., Henderson, T.B.: Modified signed-digit addition and subtraction using optical symbolic substitution. Appl. Opt. **25**(15), 2456–2457 (1986)
7. Cherri, A.K., Karim, M.A.: Modified signed digit arithmetic using an efficient symbolic substitution. Appl. Opt. **27**(18), 3824–3827 (1988)
8. Datta, A.K., Basuray, A., Mukhopadhyay, S.: Arithmetic operations in optical computations using a modified trinary number system. Opt. Lett. **14**, 426–428 (1989)
9. Lukasiewicz, J.: O logice trojwartosciowej. Ruch Filozoficny, vol. 5, pp. 169–171 (1920)
10. Ghosh, A.K., Bhattacharya, A., Raul, M., Basuray, A.: Trinary Arithmetic and Logic unit (TALU) using Savart Plate and Spatial Light Modulator (SLM) suitable for optical computation in multivalued logic. Opt. Laser Technol. **44**(5), 1583–1592 (2012)
11. Ghosh, A.K., Bhattacharya, A., Basuray, A.: Quadruple - valued logic system using Savart Plate and Spatial Light Modulator (SLM) and it's applications. J. Comput. Electron. **11**(4), 405–413 (2012)
12. Maity, G.K., Maity, S.P., Roy, J.N.: Design of all-optical reversible TOAD-based Feynman and Toffoli Gate. In: International Conference on Advanced Computing & Communication Technologies (ACCT12), Rohtak (India) (2012)
13. Taraphdar, C., Chattopadhyay, T., Roy, J.N.: Mach-Zehnder interferometer-based all-optical reversible logic gate. Opt. Laser Technol. **42**(2), 249–259 (2010)
14. Fredkin, E., Toffoli, T.: Conservative logic. Int. J. Theoret. Phys. **21**, 219–253 (1982)
15. Toffoli, T.: Reversible computing. In: Automata, Languages and Programming, pp. 632–644 (1980)