Chapter 8
Electronic Behavior of Nanocrystalline Silicon Thin Film Transistor

Prachi Sharma and Navneet Gupta

Abstract Thin film transistor (TFT) plays an important role for the fabrication of highly functional active matrix backplanes for large area display applications such as organic light emitting diodes (OLEDs). Nanocrystalline silicon (nc-Si) has recently achieved lot of interest over existing hydrogenated amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si) due to its superior properties which makes it suitable channel material for the fabrication of TFTs. In present work, the physical insight into the nc-Si TFT device characteristics and device non idealities is reported which can provide important step for the production of high performance large area display devices.

8.1 Introduction

Thin film transistor (TFT) is commonly used as a pixel addressing element and is the heart of large area electronic devices over the past few decades [1–3]. Large area electronics involves various display applications such as liquid crystal displays (LCDs) and organic light emitting diodes (OLEDs). The aim of these applications is to spread electronic components over large area substrate at low fabrication cost.

For the production of new generation large displays, an active matrix addressing scheme is required for display panels where pixels are located at row and column interactions in order to minimize capacitive losses in column and row lines. This addressing scheme basically consists of two TFTs per pixel, of which one is operated under continuous gate bias and hence requires a high electrical stability.

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For fabricating TFTs, various materials can be used as an active channel layer. The commonly used materials are hydrogenated amorphous silicon (a-Si:H) and polycrystalline silicon (poly-Si).

Nanocrystalline silicon (nc-Si) has been proven as the best alternative material over a-Si:H and poly-Si as shown in Table 8.1. The TFTs consist of three electrodes (i.e., source, drain, and gate), gate insulator, and thin semiconductor layer. Based on the level of the gate electrode, the TFTs are divided into two types, top-gate TFT and bottom-gate TFT. In top-gate TFT, the gate electrode is located above the semiconductor layer whereas in bottom-gate TFT, the gate electrode is located below the semiconductor layer.

When the nc-Si film is deposited over the amorphous substrate like glass then its crystallinity is not very high in the initial growth phases because the nc-Si is usually grown up in the form of cone-shape that is from bottom to top. The grain size and therefore the crystallinity increase with the increase in nc-Si film thickness [6]. This structural difference in top and bottom layers of nc-Si film plays crucial role in nc-Si TFT designing.

In case of bottom-gate structure, the device performance depends on the bottom layer of nc-Si film where the channel is formed as compared to top-gate TFT, where the channel is located in highly crystalline part at the top of nc-Si film [7]. Owing to this, the top-gate nc-Si TFT provides high mobility and also the better performance as compared to bottom-gate TFT. For this reason, top-gate structure of nc-Si TFT is considered in the present work. The schematic view of top-gate nc-Si TFT shown in Fig. 8.1 consists of a glass substrate, above which a nc-Si layer is used to form the channel followed gate dielectric.

The advancement in performance of flat panel display has been realized by reducing the size of top-gate nc-Si TFT and thus of gate dielectric. However, scaling down the size of gate dielectric causes two main problems that are reliability and leakage current. To avoid the leakage current problem, the selection of gate dielectric material is necessary which must have high-k value. However, possible high-k materials impose some practical challenges and have conflicting material properties. Therefore, some material selection approaches are required to recognize the trade-offs between conflicting properties and also to select the optimal material for better device performance. Material selection approaches also help us to provide ranking to the alternatives from best to worst. Therefore, these approaches provide a platform to select and prioritize the possible materials and also provide support to perform rigorous evaluation of the possible alternatives. Sharma and Gupta [8]

Table 8.1 Comparison between different materials used for the TFT fabrication [4, 5]

Parameters	a-Si:H	nc-Si	Poly-Si
Mobility	Low	Much higher than a-Si:H	High
Circuit type	NMOS	NMOS/PMOS	NMOS/PMOS
Stability	Less stable	More stable than a-Si:H	Stable
Uniformity	High	Potentially high	Poor
Cost	Low	Low	High

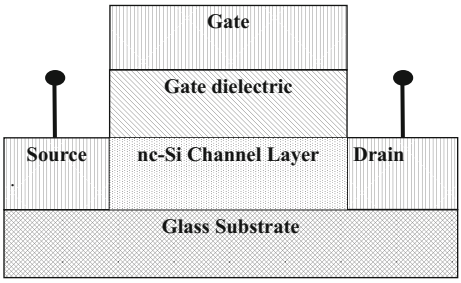

Fig. 8.1 Schematic view of top-gate nc-Si TFTs

investigated Si_3N_4, Al_2O_3, ZrO_2, Ta_2O_5, and HfO_2 materials for the gate insulator of top-gate nc-Si TFT by mean of three most popular material selection approaches i.e., Ashby's approach [9], VIKOR (VlseKriterijumska Optimizacija I Kompromisno Resenje in Serbian) [10], and TOPSIS (Technique for order preference by similarity to ideal solution) [11]. For this analysis, two performance indices (i.e., drain current and leakage current) based on four material indices (i.e., dielectric constant, band gap, conduction band offset and interface trap density) have been considered. The results (Tables 8.2 and 8.3) show that Si_3N_4 is the best suitable material and can provide high drain current and less leakage current when used as gate dielectric in top-gate nc-Si TFT.

The performance of top-gate nc-Si TFT also depends upon the various process parameters used during its fabrication and also on the conduction and instability mechanisms that occurs under electrical stress. So it is important to look into all these aspects.

The first section of this chapter explains the important outcomes and the research carried till date in the area of top-gate nc-Si TFT. In the second section, models for conduction in nc-Si TFT given by various researchers are reviewed. In third section, the mechanisms which cause the electrical instability in TFT are explained in detail.

8.2 Fabrication of nc-Si Based TFTs

The key findings of published research in the area of top-gate nc-Si TFT are as follows.

Min et al. [12] discussed that the nc-Si film in ideal condition grows quickly, provide highest mobility in minimum thickness and provide lowest conductivity under electrical stress. The lowest conductivity at room temperature in nc-Si film is achieved as low as conductivity of crystalline silicon which is around 10^{-7} S/cm. They proposed that as the film thickness increases from 50 to 350 nm, the magnitude of film conductivity increased by the order of five. This is due to the increase in magnitude of electron field-effect mobility by order of two and also increase in carrier density. The increase of electron mobility with the increase in film thickness is the key point behind the use of top-gate structure of nc-Si TFT to avail benefit of

carrier mobility which is premier at the top level of the nc-Si film. However, authors didn't present any information regarding hole mobility. Authors also discussed that in case of TFT, the leakage current is basically the conduction current which is related to channel layer under flat band situation. Therefore, it is necessary to reduce the electron carrier density present in channel in neutral condition. In TFT, the leakage current must be lowest for its possible application as switch, to provide voltage stability or in CMOS circuits to provide minimal power consumption. They have used PECVD technique for the fabrication of top-gate coplanar TFT and proposed that the compensation doping getting of water and oxygen content from mixture of base gases, or addition of chlorine content during film deposition can help in reducing the electron carrier density.

Cheng et al. [13] presented top-gate staggered nc-Si TFT deposited using PECVD at low temperature of about 150 °C. They proposed that the quality of the nc-Si material can be measured by the mobility of carriers present in the nc-Si channel in saturation condition as it directly reveals the capability of nc-Si material because saturation current is not influenced by the trapping and detrapping of charge carriers in gate dielectric. In addition to this, there is insufficient activity of doped layer under saturation condition and therefore saturation mobility reflects the lower limit of nc-Si channel capability.

In later research [14], they proposed that the structural formation of nc-Si film is based on various parameters like hydrogen dilution, temperature during deposition, nc-Si film thickness, and type of the substrate. They used both glass and plastic (Kapton E polymide) substrates for their study and fabricated both p-type and n-type staggered top-gate TFT devices on a single substrate using PECVD. They have achieved sufficient mobilities for realizing CMOS circuit on plastic but fail to achieve low off current and less threshold voltage shift due to poor quality of dielectric and the interface between gate dielectric and channel. They reported that for the better performance of the device, the substrate must have low thermal expansion coefficient, high thermal stability, low surface roughness, high chemical stability and transition temperature of glass, low permeability by oxygen and water, and low shrinkage capability to avoid misalignment during photolithography.

Lee et al. [15] proposed ambipolar transistor which worked alternatively as p-type and n-type transistor by the application of negative and positive gate voltages, respectively. The fabrication of ambipolar transistor is not reported earlier as it is difficult to realize high-quality contact between metal and semiconductor and also to deposit high-quality nc-Si film. They have used nc-Si/Cr stack as source-drain contacts in place of n^+ nc-Si for the fabrication of top-gate TFT. They proposed that hydrogen atoms clean the surface of Cr electrodes, during the initial phase of nc-Si film formation and this leads to highly crystalline nc-Si film and therefore Cr silicidation provides lower electron as well as hole injection barrier. They reported that at higher gate voltages, leakage current increases exponentially for both p- and n-type TFTs, which validates ambipolar operation. This behavior is due to accumulation of holes and electrons in n-channel and p-channel under reverse gate voltages through injection from Cr drain, this discriminates TFT with Cr silicide contacts from TFT with n^+ nc-Si contacts.

Lee et al. [16] presented the low temperature (i.e., 260 °C) fabrication of top-gate nc-Si TFT through 13.56 MHz PECVD by the use of silane diluted with hydrogen. They propose that the hydrogen dilution of silane controls the crystallinity of nc-Si layer [17], however, this increases the level of oxygen impurity in nc-Si film and at the grain boundaries. The high concentration of hydrogen atoms in the silane plasma is the main requirement for the deposition of low temperature highly crystalline nc-Si film. They reported that low dark conductivity can be achieved by providing hydrogen chemical cleaning during the deposition of nc-Si film.

In later research, Lee et al. [18] proposed that the field-effect mobility (μ_{FE}) is the ratio of free charge carriers in extended energy states, n_{band}, to the total number of induced charge carriers (which comprises of trapped carriers, n_{trap} and free carriers) times the band mobility μ_{band}, and is expressed as:

$$\mu_{FE} = \left[\frac{n_{band}}{n_{band} + n_{trap}}\right] \mu_{band} \tag{8.1}$$

The grains of nc-Si are enclosed by amorphous grain boundaries. Low temperature process provides low oxygen content in nc-Si film and thereby reduces probability of defect state creation at grain boundaries. This avoids band bending and thereby offers high mobility. This validates that low temperature is necessary for the deposition of highly crystalline nc-Si film.

Park et al. [6] presented the fabrication of top-gate nc-Si TFT using inductively coupled plasma (ICP) CVD with different channel thicknesses at the temperature of 180 °C. They proposed that ICP-CVD reduces the surface damage usually caused by ion bombardment by generating the remote plasma without causing the bombardment of ions. This reduction in surface damage provides highly crystalline growth of nc-Si film and avoids amorphization in Si deposition surface. They proposed that grain size increases with increase in film thickness because of the growth of nc-Si layer in form of cone shape i.e., from bottom to top. In addition to this, the surface roughness also increases with increase in nc-Si thickness. Lee et al. [19] proposed that the top-gate nc-Si TFT provides better stability and high on/off ratio as compared to bottom-gate nc-Si TFT. The high stability of top-gate nc-Si TFT makes it highly suitable device for display application like pixel driver in OLED to maintain low line voltages. They have used silicon nitride as the gate dielectric for the fabrication of both top-gate and bottom-gate n-channel nc-Si TFT because silicon nitride provides high reliability, high breakdown field and also allow processing at low temperature.

Kang et al. [20] also presented the effect of film thickness on the nc-Si TFT performance. They proposed that as thickness of nc-Si film increases, the field-effect mobility also increases due to increase in grain size. However, this causes the increase in leakage current. According to them, this increase in leakage current is due to the reduction in total resistance present in TFT.

Lee et al. [21] reported the mechanisms that are responsible for gate leakage current. They proposed that at high gate and low drain bias, thermal emission of charge carriers that are trapped in grain boundary regions is responsible for leakage

current whereas Poole–Frenkel emission mechanism in drain depletion state is responsible for high gate bias and high drain bias. Under low gate bias, ohmic conduction via bulk channel layer is responsible mechanism for leakage current. They presented that high leakage current causes loss of signal in pixels and also increases the power consumption of the driving circuitry. They proposed that reduction in leakage current can be attained either by using offset-gated configuration or by employing lightly doped drain regions.

Cheng et al. [22] reported the effect of contact resistance on the performance of staggered top-gate nc-Si TFT and for this study they have fabricated both n^+ and p^+ nc-Si TFT at various channel lengths. The total resistance of nc-Si TFT comprises of channel resistance R_{CH} and the contact resistance R_o. They reported that $R_o \times W$ decreases with increase in gate overdrive voltages. They also proposed that if the channel length of n-type TFT is below 10 μm and of p-type TFT is below 25 μm, then the drain current at $V_{DS} = 10$ V is restricted by the contact resistance.

Djeridane et al. [23] proposed that during the growth of nc-Si film over the amorphous like substrate, a residual amorphous phase called as incubation layer is formed at the interface between the substrate and the film. This incubation layer can be avoided by controlling the deposition plasma parameters. They also reported that silicon nitride provides better stability when used as gate dielectric for the fabrication of n-type nc-Si TFT. However, for fabrication of p-type TFT they have used SiO_2 as a gate dielectric due to its wide band gap, large conduction and valence band offset.

Subramaniam et al. [24] reported that ambipolar operation can be achieved by reducing the oxygen concentration in the nc-Si channel. The ambipolar transistor allows the production of complementary inverter using single type device. They

Table 8.2 Ranking of alternatives by VIKOR approach [8]

Gate dielectric materials	Maximum group utility, G	Ranking based on G values	Minimum regret of opponent, R	Ranking based on R values	Q ($v = 0.5$)	VIKOR ranking
Si_3N_4	0.2079	1	0.1590	1	0	A1
Al_2O_3	0.4880	4	0.4	4	0.8521	A5
ZrO_2	0.4734	2	0.1778	2	0.3730	A2
HfO_2	0.4856	3	0.1778	2	0.3880	A3
Ta_2O_5	0.6056	5	0.3	3	0.7925	A4

Table 8.3 Ranking of alternatives by TOPSIS approach [8]

Gate dielectric materials	S^*	S^-	Z	TOPSIS ranking
Si_3N_4	0.0714	0.2143	0.7501	1
Al_2O_3	0.1615	0.1848	0.5336	2
ZrO_2	0.1229	0.1280	0.5101	3
HfO_2	0.1287	0.1236	0.4898	4
Ta_2O_5	0.1881	0.1270	0.4030	5

Table 8.4 Experimental published data for top-gate nc-Si TFT

Reference	Esmaeili et al. [7]	Cheng et al. [13]	Min et al. [12]	Lee et al. [15]
Gate contact	Al 300 nm	Al 200 nm	Al 200 nm	Al 300 nm
Source/drain contact layer	–	Cr 50 nm	Cr 50 nm	Cr 50 nm
Doped layer	n^+ nc-Si 80 nm	n^+ nc-Si 60 nm	n^+ nc-Si 60 nm	n^+ a-Si:H 50 nm
Process nc-Si	PECVD 50 nm	VHF PECVD 50 nm	VHFPECVD 300 nm	PECVD 100 nm
Dielectric	SiO_2 270 nm	SiO_2 300 nm	SiO_2 370 nm	a-SiO_x
Temperature (°C)	350	150	150	260
Width to length ratio (W/L)	180 μm/45 μm	200 μm/30 μm	240 μm/40 μm	W = 200 μm L = 20, 50, 100, 200 μm
Structure type	Top-gate coplanar	Top-gate staggered	Top-gate staggered	Top-gate staggered
Substrate	Glass	Glass, Kapton	Glass	Glass
Mobility	11 cm^2/Vs (at V_{ds} = 10 V)	Glass 30 cm^2/Vs Kapton 23 cm^2/Vs	40 cm^2/Vs	100-150 cm^2/Vs
Leakage current	1×10^{-12}A	–	–	–
Sub-threshold Slope	2.5 V/dec	–	–	0.22-0.25 V/dec
On/off ratio	10^8 at V_{DS} = 10 V	–	–	10^6
Threshold voltage	2.5 V (at V_{DS} = 0.1 V)	–	–	1.5–2 V
Threshold voltage shift	–	–	–	–
Year	2002	2002	2002	2005

(continued)

Table 8.4 (continued)

Reference	Fonrodona et al. [25]	Cheng et al. [14]	Kamei et al. [17]	Fonrodona et al. [26]
Gate contact	Al Thermally evaporated	Al 300 nm	Sputtered Al 300 nm	Al Thermally evaporated
Source/Drain contact layer	–	–	–	–
Doped layer	n + or p + a-Si:H 150 nm	Cr 100 nm	Cr 100 nm	n + nc-Si 150 nm
Process nc-Si	HWCVD 200 nm	PECVD 100 nm	RF PECVD 300 nm	HWCVD 200 nm
Dielectric	SiO_2 100 nm	a- SiO_x 300 nm	SiO_2 300 nm	SiO_2 100 nm
Temperature	200 ºC	260 ºC	150 ºC	200 ºC
Width to Length ratio (W/L)	20 µm/60 µm	200 µm/50 µm	200 µm/50 µm	100 µm/20 µm
Structure	Top-gate Coplanar	Top-gate Staggered	Top-gate staggered	Top-gate coplanar
Substrate	Glass covered with 200 nm APCVD deposited SiO_2	Glass	Glass	Glass covered with APCVD deposited SiO_2
Mobility	22 cm^2/Vs	150 cm^2/Vs	450 cm^2/Vs	11.5 cm^2/Vs
Leakage current	–	–	–	–
Sub-threshold Slope	0.5 V/dec	0.3 V/dec	0.6 V/dec	0.34 V/dec
On/off Ratio	$>10^6$	10^7	10^6	–
Threshold voltage	6.3 V	2 V	2 V	5.70 V
Threshold voltage shift	–	–	–	0.5 V at $V_{GS} = -10$ V
Year	2005	2005	2006	2006

(continued)

Table 8.4 (continued)

Reference	Lee et al. [19]	Lee et al. [18]	Kang et al. [20]	Subramaniam et al. [24]
Gate contact	Al	Al 300 nm	Al 300 nm	Al Liftoff
Source/Drain contact layer	Cr	n + nc-Si	n + nc-Si	Cr or Ti
Doped layer	n + nc-Si 60 nm	–	–	n^+ nc-Si 100 nm
Process nc-Si	PECVD 80 nm	ICP-CVD 60, 90, 130 nm	ICP-CVD 60, 90, 130 nm	PECVD 250 nm
Dielectric	a-SiN_x:H 300 nm	SiO_2 150 nm	SiO_2 150 nm	SiO_2
Temperature	240 ºC	180ºC	–	250˚C
Width to Length ratio (W/L)	200 µm/50 µm	20 µm/10 µm	20 µm/10 µm	20 µm/10 µm
Structure type	Top-gate	Top-gate	Top-gate Staggered	Top-gate Staggered
Substrate	Glass	Glass	Glass	p-type silicon
Mobility Resistivity	0.5 cm^2/Vs at V_{DS} = 1 V 0.6 cm^2/Vs at V_{DS} = 10 V	69 cm^2/Vs with 60 nm film 99 cm^2/Vs with 90 nm film	26 cm^2/Vs with 60 nm film 77 cm^2/Vs with 90 nm film 119 cm^2/Vswith 130 nm film	–
Leakage current	6.75×10^{-14}Aat V_{DS} = 0.1 V 2×10^{-11}A at V_{DS} = 10 V	At V_{GS} = −4.4 V 8.4×10^{-11} A with 60 nm film 3.6×10^{-10}A with 90 nm film	7.2×10^{-10} to 1.9×10^{-8}A at V_{GS} = −4.4 V	–
Sub-threshold Slope	0.82 V/dec at V_{DS} = 1 V 0.93 V/dec at V_{DS} = 10 V	217mv/dec with 60 nm film 230 mv/dec with 90 nm film	–	–

(continued)

Table 8.4 (continued)

Reference	Lee et al. [19]		Lee et al. [18]	Kang et al. [20]	Subramaniam et al. [24]
On/off Ratio	10^6 at V_{DS} = 1 V 2 × 10^5 at V_{DS} = 10 V		10^7 at V_{DS} = 0.1 V	10^4 at V_{DS} = 0.1 V	–
Threshold Voltage	2.4 V at V_{DS} = 1 V 2.7 V at V_{DS} = 10 V		2.2 V with 60 nm film 2.3 V with 90 nm film	–	–
Threshold voltage shift	V_{DS} = 1 V	V_{DS} = 10 V	V_{GS}	–	–
	0.35 0.77 1.52	0.34 0.57 1.23	20 V 30 V 40 V		
Year	2007		2007	2008	2012

fabricated both n-type and p-type top-gate staggered nc-Si TFT at submicron dimensions with no short channel effects.

Table 8.4 summarized nc-Si top-gate TFT device dimensions and performance parameters of the published experimental works. So based on the literature review, it is clear that n-channel nc-Si TFT provides higher mobility compared to p-channel TFT and staggered top-gate structure of TFT provides better stability and high on-off current ratio. So in this chapter, staggered top-gate n-channel nc-Si TFT is considered and investigated for its electrical behavior.

8.3 Conduction Models

Various device models have been presented in past for explaining the electrical behavior of nc-Si TFTs. This section presents the key assumptions, their conditions of validity and range of applicability of important analytical models of nc-Si TFTs.

Dosev et al. [27] reported the physical phenomenon accountable for different operation regimes and presented an analytical model for nc-Si TFTs associated with this phenomenon. This model is based on existing models for a-Si:H TFTs, which have been extended to account for observed physical phenomena in nc-Si TFT. They proposed that the density of the defect states (i.e., DOS) is lesser in nc-Si than in a-Si:H due to higher internal order of atoms in nc-Si.

$$I_{\mathrm{Dsat}} = \mu_{\mathrm{fet}} C_{\mathrm{i}} \frac{W}{L} V_{\mathrm{DSe}} (1 + \lambda V_{\mathrm{DS}}) V_{\mathrm{GTe}} \quad (\text{for above threshold regime}) \tag{8.2}$$

where μ_{fet} is the field-effect carrier mobility, C_{i} is the capacitance of gate insulator, V_{DS} is drain to source voltage, λ is parameter relating to the effect of gate-length modulation, V_{DSe} is effective voltage from drain to source, and V_{GTe} is the effective gate overdrive voltage.

Dosev et al. [28] presented the numerical simulation results of nc-Si TFTs, using ATLAS device simulator. They examined that acceptor-like defect states in nc-Si TFTs are filled at lower gate voltages as compared to a-Si:H having similar threshold voltages. The transconductance shape of nc-Si TFTs is same as of a-Si:H TFTs before the acceptor-like states are occupied. When acceptor-like states are filled by electrons then transconductance shape of nc-Si TFTs becomes typical as of poly-Si TFTs. Due to this behavior of acceptor-like states, the nc-Si TFTs properties typically lie between a-Si:H and the poly-Si transistors. However, authors considered a gap of 1.91 eV which is not a usual value for a-Si:H as well as for nc-Si TFT devices. For nc-Si TFT devices with an optical gap of 1.72 eV, Estrada et al. [29] demonstrated that the anomalous effect of transconductance is due to trapped charge concentration and if some conditions are fulfilled related to the trapped charges concentration in defect states and concentration of free charges in the material then this effect can also observe for a-Si:H devices with acceptor tail states activation energy similar to normal values of 0.035 eV. Therefore, the behavior of nc-Si is not

necessarily suggested between a-Si:H and poly-Si. The mobility and drain current models for nc-Si TFT devices are presented by Cerdeira et al. [30] including a second region examined in above-threshold regime, which are not exist in a-Si:H TFTs.

Hatzopoulos et al. [31] proposed the model for drain current in regime of above threshold, on the basis of exponential distribution of tail states energy. Under linear region, this proposed model explained the observed super linear rise of drain current with gate voltage by the value of characteristic thermal energy of band tails being higher than 1.5 times the lattice thermal energy. When the characteristic temperature distribution of tails states is equal to 1.5 times the lattice temperature, then the derived current analytical model leads to the general quadratic metal-oxide-semiconductor (MOS) expression which is reported by Pappas et al. [32]

$$I_{\mathrm{D}} = \frac{W}{L}\mu B\left[(V_{\mathrm{G}} - V_{\mathrm{T}})^{2AkT_{\mathrm{t}}} - (V_{\mathrm{G}} - V_{\mathrm{T}} - V_{\mathrm{D}})^{2AKT_{\mathrm{t}}}\right] \quad (\text{for above threshold regime}) \tag{8.3}$$

$$I_{\mathrm{Dsat}} = \frac{W}{L}\mu B(V_{\mathrm{G}} - V_{\mathrm{T}})^{2AkT_{\mathrm{t}}} \quad (\text{for saturation regime}) \tag{8.4}$$

where

$$B = \frac{n_i}{qA^2\sqrt{2kT_{\mathrm{t}}N_{\mathrm{t}}/\varepsilon_{\mathrm{s}}}}\left(\frac{C_{ox}^2}{4\varepsilon_{\mathrm{s}}kT_{\mathrm{t}}N_{\mathrm{t}}}\right)^{AkT_{\mathrm{t}}} \tag{8.5}$$

and

$$A = \frac{1}{kT} - \frac{1}{2kT_{\mathrm{t}}} \tag{8.6}$$

$$\mu_{\mathrm{FE}} = \frac{\mu B}{C_{\mathrm{in}}}2AkT_{\mathrm{t}}(2AkT_{\mathrm{t}} - 1)(V_{\mathrm{G}} - V_{\mathrm{T}} - V_{\mathrm{D}})^{2(AKT_t - 1)} \tag{8.7}$$

where I_{D} is drained current, μ_{FE} is field-effect mobility, k is Boltzmann constant, μ is low electric field mobility of electron, T_{t} is characteristic temperature of tail state distribution, N_{t} is tail states volume density at intrinsic level, n_{i} is intrinsic carrier concentration, C_{ox} is gate dielectric capacitance, ε_{s} is silicon permittivity, kT is thermal energy at room temperature, V_{G}, V_{D} and V_{T} are gates, drain and threshold voltage respectively, W is channel width, and L is channel length.

When μ_{FE} is constant and is independent of gate voltage then from Eq. (8.6), $AkT_{\mathrm{t}} = 1$ and $T_t > 3T/2$. Under this condition Eq. (8.3), (8.4), and (8.7) becomes,

$$I_{\mathrm{D}} = \frac{W}{L} C_{\mathrm{in}} \mu_{\mathrm{FE}} \left[(V_{\mathrm{G}} - V_{\mathrm{T}}) V_{\mathrm{D}} - \frac{V_{\mathrm{D}}^2}{2} \right] \quad (\text{for } V_{\mathrm{D}} < V_{\mathrm{G}} - V_{\mathrm{T}}) \tag{8.8}$$

$$I_{\mathrm{Dsat}} = \frac{W}{2L} C_{\mathrm{in}} \mu'_{\mathrm{FE}} \left[(V_{\mathrm{G}} - V_{\mathrm{T}})^2 \right] \quad (\text{for } V_{\mathrm{D}} \geq V_{\mathrm{G}} - V_{\mathrm{T}}) \tag{8.9}$$

$$\mu'_{\mathrm{FE}} = \frac{3\mu k T n_{\mathrm{i}}}{2q\sqrt{3\varepsilon_{\mathrm{s}} k T N_{\mathrm{t}}}} \frac{C_{\mathrm{in}}}{N_{\mathrm{t}}} \tag{8.10}$$

The off current in nc-Si TFT is examined by Esmaeili-Rad et al. [33] and analyzed that the presence of fixed charges at the nc-Si/passivation nitride interface serves to increase the band bending, leading to an increase in off current by about two orders of magnitude. The reduction in leakage current can be achieved by using a-Si:H/nc-Si bilayer as the channel of nc-Si TFT device. When the nc-Si channel layer is capped with a-Si:H, the reduction in leakage current can be determined by the bulk conductivity of nc-Si because a-Si:H layer typically makes less defective interface with the nitride layer which is used for the passivation.

Ahnood et al. [34] presented a general analytical technique capable of removing contact resistance effects, both ohmic and non-ohmic based solely on *I–V* measurements, enabling the extraction of an accurate and physically meaningful mobility. They proposed that the omission of contact resistance effects can results in an incorrect extraction of the maximum μ_{FET} by a factor of 2. Mao [35] demonstrated the impact of the grain size of nc-Si on the surface potential of doped nc-Si TFTs. During the calculation of the surface potential of nc-Si, authors examined that the change in the dielectric constant of nc-Si should be considered when its diameter is smaller than 10 nm and the change in the band gap of nc-Si should be considered when its diameter is larger than 6 nm. They proposed a simplified surface potential equation for nc-Si TFTs under strong inversion conditions.

$$E(\varphi_{\mathrm{s}}) = \sqrt{\frac{2q}{\left(1 + \frac{10.4}{1 + \left(\frac{1.38}{d \times 10^9}\right)^{1.37}}\right)\varepsilon_0} \left[\frac{N_{\mathrm{ST}}}{d}\varphi_{\mathrm{s}} + \frac{1}{N_{\mathrm{Aa}}^-} \frac{4kT(2\pi kT)^3 (m_{\mathrm{e}} m_{\mathrm{h}})^{\frac{3}{2}}}{h^6} \exp\left(- \frac{E_{\mathrm{g}}(\infty) + q\left(\frac{3.4382}{d \times 10^9} + \frac{1.1483}{(d \times 10^9)^2}\right)}{kT} \right) kT \exp\left(\frac{q\varphi_{\mathrm{s}}}{kT}\right) \right]} \tag{8.11}$$

where N_{Aa}^- is active dopant concentration, d is average grain size, q is electronic charge, N_{ST} is grain boundary surface state density, $E_{\mathrm{g}}(\infty)$ is bulk band gap, k is Boltzmann constant, T is temperature, φ_{s} is surface potential, ε_o is dielectric constant of free space, m_{e} and m_{h} are effective electron and hole masses respectively, and h is Planck's constant.

Anutgan et al. [36] performed the capacitance analyzes of nc-Si TFT. They found that the conducting thin layer in nc-Si film enlarges the effective area of capacitor beyond the electrode in nc-Si TFT structure. This increase of the effective area can be related to bulk capacitance-resistance branches and also with channel resistance where the earlier is governing at higher frequencies and the latter is

accountable for the further increase in effective area at lower frequencies. Thus, they proposed that the hole conductivity along the nc-Si TFT interface is less as compared to electron conductivity.

Steinke et al. [37] presented a model for determining the threshold voltage of nc-Si TFTs by examining the multiple boundaries between neighboring crystalline grains limit the charge-carrier transport. They have calculated the macroscopic densities of free and trapped carriers and then relate these densities with the site and bond occupation probabilities of a two-dimensional percolation problem in which sites correspond to grains and bonds to grain boundaries. In the site-bond percolation problem, they determined the threshold by using Monte-Carlo simulations. However, the model only describes transistor behavior near-threshold and could not explain the linear behavior soon after the transistor is turned on at low drain bias.

Sharma et al. [38] presented an analytical model for calculating the threshold voltage using one-dimensional Poisson's equation. They have analyzed the effect of various physical parameters i.e., trapping state density, doping density, temperature, and gate insulator thickness on the threshold voltage. They proposed that the decrease in gate insulator thickness and increase in temperature causes the decrease in the threshold voltage as shown in Fig. 8.2. They also demonstrate that the

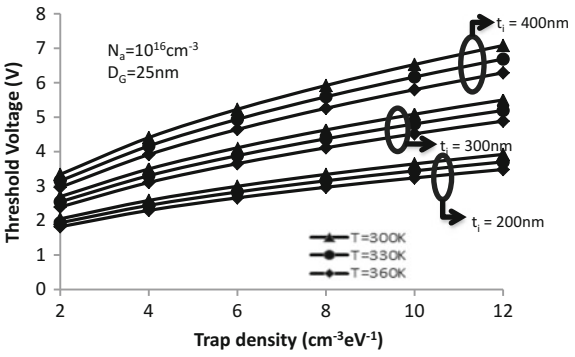

Fig. 8.2 Variation of threshold voltage as a function of trap density for different values of gate insulator thickness at different temperatures [38]

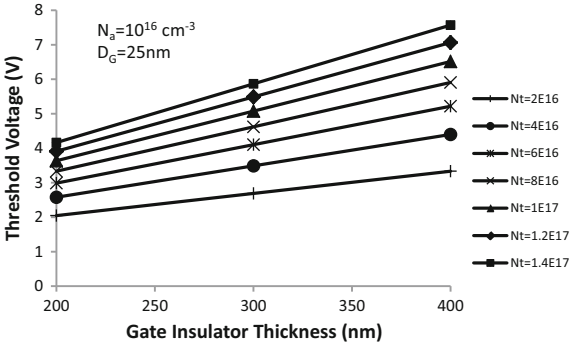

Fig. 8.3 Variation of threshold voltage as a function of gate insulator thickness for different values of trap density [38]

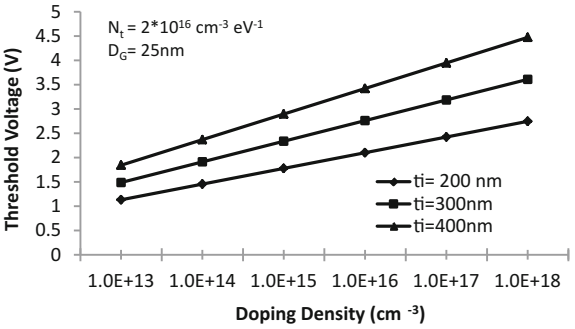

Fig. 8.4 Variation of threshold voltage as a function of doping density for different values of gate insulator thickness [38]

threshold voltage increases with increase in trap density and doping concentration for a particular value of gate insulator thickness as shown in Figs. 8.3 and 8.4.

8.4 Electrical Instability

In general, the silicon (Si) based TFT suffers from electrical instability due to two possible instability mechanisms: (a) Charge trapping in gate insulator and/or in the interface between the gate insulator and channel (b) Defect state creation in active layer. These instability mechanisms cause the shift in threshold voltage and thereby change the drain current of TFT. Esmaeili-Rad et al. [39] found that the nc-Si TFT shows less threshold voltage shift as compared to a-Si:H TFTs. In addition, Kim et al. [40] examined that in case of top-gated nc-Si TFT, the defect state creation is much lower due to the presence of well-crystallize region of the nc-Si film. Sharma and Gupta [41] further analyze the instability mechanism in top-gate nc-Si TFT and proposed the model for threshold voltage shift including the effect of various physical parameters like grain size, gate insulator thickness, doping density, and grain boundary trapping state. They provided the expression for threshold voltage as-

$$|\Delta V_T| = \left(V_{gs} - \varphi_s \left[1 + \frac{q t_i \sqrt{N_t}}{\varepsilon_i} \sqrt{1 + \frac{10.4}{1 + \left(\frac{1.38}{D_G \times 10^7} \right)^{1.37}}} \right] \right) \left\{ 1 - \exp\left[-\left(\frac{t}{\tau} \right)^{\beta} \right] \right\} \tag{8.12}$$

where V_{gs} is gate to source voltage, φ_s is surface potential, q is electronic charge, t_i is insulator thickness, ε_i is dielectric constant, N_t is density of trapping states (cm^{-3} eV^{-1}), D_G is grain size, τ is characteristic trapping time, and β is stretched-exponential exponent.

Based on the analysis, they proposed that the higher trap density, larger gate insulator thickness, and greater doping concentration provide lesser threshold

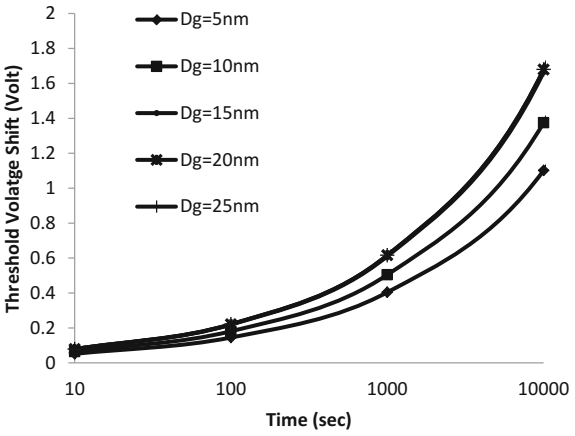

Fig. 8.5 Computed variations of threshold voltage shift in the top-gated nc-Si TFTs as a function of time for different grain sizes [41]

voltage shift. They also investigated that for smaller grain size, threshold voltage shift reduces with the reduction in grain size. But, if grain size is larger i.e., greater that 20 nm then device become shows minimal threshold voltage shift as shown in Fig. 8.5. Now, in the following section, we discuss about the attributes of instability mechanisms which are presented by the various researchers.

8.4.1 Powell's Model

Powell [42] analyzed that the electrical instability mechanism in amorphous silicon-silicon nitride TFTs, operate with low electric fields ($\sim 3 \times 10^5$ V cm^{-1}) in the dielectric, is basically the charge trapping that occurs in silicon nitride layer that causes the threshold voltage shift and thus causes drain current degradation for a given biasing condition. Since silicon nitride as a gate dielectric has a high density of trap states thus causes charge trapping instabilities in TFT. Author proposed that the rate limiting process involved in the charge transfer at low electric field is basically the conduction in the nitride by variable range hopping at Fermi level and not the supply function from the semiconductor. Since the space charge in the nitride and the variable hopping conduction both depends on density of states in silicon nitride thus the threshold voltage shift is determined by the density of states at the Fermi level.

However, author [43] further proposed that the nitride dependency of the hopping rates was due to variation in wave function rather than the trap density. The magnitude of threshold voltage shift is strongly temperature dependent with activation energy of 0.3 eV. This activation energy is determined by the mean hop energy required for charge injection deep into the silicon nitride at the low applied electric fields. The strong temperature dependency of charge trapping is due to charge redistribution in the silicon nitride by thermally activated variable hopping from occupied states.

The logarithmic time dependence of threshold voltage shift is given as-

$$\Delta V_{\mathrm{T}} = r_{\mathrm{d}} \log\left(1 + \frac{t}{t_{\mathrm{o}}}\right) \tag{8.13}$$

where r_{d} is constant and contains the density of traps and tunneling constant.

Later, Powell and his research group [44] analyzed that in addition to the existing process of charge trapping near the interface, following mechanisms are also possible: (1) tunneling into the dielectric, (2) trapping into states at semiconductor-dielectric boundary, and (3) localization in deep states within the amorphous silicon layer.

They proposed that the new mechanism responsible for instability of a-Si:H TFTs is the creation of metastable dangling bond states within the a-Si:H layer near to dielectric interface as a result of the field-effect-induced changes in electron density.

If phosphorus doping is used in order to move the Fermi level into the conduction band tail, then this makes the unstable configuration of silicon atom with five electrons. This silicon atom located just below the fermi level and thus causes the breaking of weak Si–Si bond and hence the formation of dangling bond defects:

$$2\mathrm{Si_4}^{0} + \mathrm{e}^{-} \rightarrow \mathrm{Si_3}^{-} + \mathrm{Si_3}^{0}$$

The main difference [45] between the two instability mechanisms is that, in case of charge trapping mechanism [42], the charge carriers are slowly trapped into electron states (also known as slow states) which are in poor communication with the a-Si conduction band. This trapping process produces a fixed shift in the transfer characteristic of a-Si TFTs. However, in case of defect state creation mechanism [44], there is a slow increase of extra states (also known as fast states) which are in good communication with the a-Si conduction band.

Berkel et al. [45] analyzed the bias dependence of threshold voltage shift in amorphous silicon-silicon nitride ambipolar TFTs and reported the coexistence of both instability mechanisms. They proposed that the state creation is dominated at low positive bias whereas charge trapping is dominated at higher positive as well as negative bias. An ambipolar TFT possess electron as well as hole accumulation layers under positive and negative gate biases, respectively. In this case, the number of created dangling bonds is given as [45]

$$\Delta N_{\mathrm{dh}} = C\frac{V_{\mathrm{e}} - V_{\mathrm{h}}}{2}\left(\mathrm{cm}^{-2}\right) \tag{8.14}$$

where V_{e} is the shift of threshold voltage for electron conduction and V_{h} is the shift for hole conduction, while the density of slow states is given by

$$\Delta n_t = C\frac{V_e + V_h}{2}\left(\mathrm{cm}^{-2}\right) \tag{8.15}$$

where C in Eqs. (8.14) and (8.15) is the geometrical capacitance.

Author concludes that the extra states are created due to the absence of bonding electrons and these reactions will separately proceed whenever conduction band states or valence band states are populated and thus for bond breaking, recombination events are not required which is considered essential by Stutzmann et al. [46]. Berkel et al. [45] provide clear evidence for the charge trapping in the nitride and thus for the presence of slow states at the a-Si:H/a-SiN:H interface. Charge exchange with the nitride layer causes the net positive charge after negative bias stress and also net negative charge after positive bias stress. Under positive bias, the charge trapping mechanism is strongly field dependent.

Powell and his group [47] provide further refinement in bias dependency of the threshold voltage shift by including the effect of nitride composition. They reported that state creation is independent of the nitride composition and dominant at lower biases whereas the charge trapping is dependent on the nitride composition and dominant at higher biases. This indicates that the state creation process occurs in the a-Si:H layer whereas the charge trapping occurs in a-SiN_x:H layer. The defect states can be directly created by populating the conduction band tail states in the undoped material which moves the Fermi level up to the energy similar to these states. They also proposed that the charge trapping process is strongly field dependent which is associated with the field enhanced hopping at the Fermi level.

They also measured the time and temperature dependence of two instability mechanisms [48] and found that at the bias above which the charge trapping in the nitride dominates, the threshold voltage shift shows the logarithmic time dependence whereas at the bias below which state creation in the a-Si:H dominates, the threshold voltage shift shows the power law dependence, $\Delta V_T = \alpha(t/t_o)^{\beta}$ where β is about 0.5. They also found that the state creation is thermally activated but the charge trapping is weakly temperature dependent. The charge trapping shows logarithmic time dependence and the small temperature dependence because the rate limiting step is basically the charge injection from the a-Si:H to the silicon nitride with charge trapping close to the semiconductor interface and no charge redistribution occurs due to the conduction in the nitride. The threshold voltage shift due to the state creation is small and is given as

$$\Delta V_T = (V_G - V_T)(t/t_o)^{\beta} \tag{8.16}$$

Thus, the rate of state creation is proportional to the band tail electrons and t_o is independent of density of band tail electrons. The magnitude of $E_a \sim 0.9$ eV (i.e., activation energy of t_o) and temperature dependent β ($\sim$0.45–0.65) is uniform with dispersive hydrogen diffusion. Thus, they proposed that the state creation process is similar to that of dangling bond creation process which occurs due to the breaking of weak Si–Si bonds sustained by dispersive diffusion of hydrogen [49, 50].

Powell et al. [51] also reported that the charge trapping mechanism causes a shift of the electron and hole threshold voltages in the same direction whereas the state creation mechanism causes a shift in opposite direction. The electron threshold voltage is shifted in positive direction while hole threshold voltage is shifted in negative direction. For the transistor which uses silicon nitride as a gate dielectric, state creation in the lower part of the band gap is the dominant process at the low positive bias whereas the removal of states from the lower part of the gap dominates at the low negative bias. However, for the transistor that uses oxide as the gate dielectric, state creation is the dominant process for both positive and negative bias. For positive bias, states creation occurred in the lower portion of the band gap whereas for negative bias, it occurred in the upper portion of the band gap. In addition to this, for oxide transistor, the positive and negative bias annealing causes overall increase in the density of states whereas for nitride transistor negative bias annealing causes a decrease in the density of states due to the annealing of defect states presents below the midgap. This difference between nitride and oxide transistor is because of the different zero-bias Fermi energy position at the interface due to the existence of an electron accumulation layer in the nitride transistor.

For nitride transistor, the dominant mechanism for threshold voltage shift under the higher biases stress is the charge trapping which occurs for both high positive as well as high negative bias. The magnitude of the threshold voltage shift for state reduction is smaller than for the state creation. Authors also found that threshold voltage shows the power law time dependence for both the polarities and in addition to this the activation energy is same ($\sim$0.9 eV) for both positive and negative bias. This concludes that the state creation process for positive bias is similar to that of state removal process for negative bias.

Powell and his group [52] further proposed that the parameter β is not appropriate for measuring the TFT instability and thus a new concept known as thermalization energy concept has been proposed. According to them, defect creation during bias stress exhibits a thermal barrier for defect removal with the maximum energy around 1.1–1.4 eV based on the time and temperature at which defects were created. This barrier is not important under thermal equilibrium ($\sim$500 K) because the defect creation and removal are balanced by the formation energy of defects, however, under non-equilibrium condition, this energy barrier is important in order to identify the specific intermediate step.

They reported the expression for thermalization energy as [52]

$$E = (k_B T)\ln(\nu t) \tag{8.17}$$

It means that after time t, all defect-creation sites with energy $E_a \leq E$ would have converted into defects. Deane et al. [52] plotted threshold voltage shift as a function of stress time at various temperatures and then applied the thermalization concept to the bias stress data by plotting threshold voltage shift as a function of thermalization energy and found a unique curve at a single fitting parameter i.e., attempt-to-escape frequency $\upsilon(=10^{10}\ \mathrm{Hz})$. They also plotted stretched exponential as a function of thermalization energy and found that the stretched exponential curve matched well

with the experimental data for the $E < 0.95$ eV but curves show mismatched for $E > 0.95$ eV and thus they proposed that to obtain a stretched exponential, the defect state creation has to be proportional to the number of excess band tail carriers $(\Delta N_{BT})^{\alpha}$ with α between 1.5 and 1.7. For $\alpha = 1.5$, threshold voltage shift is given as equation

$$\Delta V_t \propto \left[\left(\frac{t}{t_0}\right)^{\beta} + 1\right]^{-2} \tag{8.18}$$

They provide the following comparison between defect state creation and defect removal

1. Defect state creation possesses $E_a = 0.975$ eV with $\upsilon_o = 10^{10}$ Hz whereas defect removal shows activation energy between 01.1 and 1.5 eV with υ_o of 10^{13} Hz.
2. Defect creation mechanism occurs due to the breaking of weak Si–Si bond and which results into the thermalization of SiHD complex in the H-DOS (hydrogen density of states) whereas the defect removal occurs due to the release of hydrogen from the SiHD complex. The following equation shows that thermalization of SiHD complex.

$$\mathrm{Si} - \mathrm{Si}_{\mathrm{weak}} + \mathrm{SiHD} \rightarrow \mathrm{SiHD} + \mathrm{Si} - \mathrm{Si}_{\mathrm{strong}}$$

8.4.2 Libsch's Model

Libsch et al. [53] proposed that the charge injection from the a-Si:H channel into the traps presented in the a-Si:H/a-SiN$_X$:H interface and in the nitride layer close to the interface causes the threshold voltage shift (ΔV_T) in the transfer characteristic of TFT. They proposed the stretched-exponential equation given as-

$$|\Delta V_T| = |\Delta V_0|\left\{1 - \exp\left[-\left(\frac{t}{\tau}\right)^{\beta}\right]\right\} \tag{8.19}$$

where ΔV_0 is the effective voltage drop across the insulator, $\tau = \tau_0 \exp(E_T/kT)$ is the characteristic trapping time of the carriers with τ_o being the thermal prefactor for emission over the energy barrier, $E_a = E_T\beta$ represent the thermal activation energy with β as the stretched-exponential exponent and E_T being the average effective energy barrier for the carriers enter into the insulator from the a-Si:H channel. When the shorter stress times, lower stress electric fields or lower stress temperatures are applied on the nitride gate dielectric a-Si:H TFT then the carriers inject directly into the bottom energy states of a-Si:H/a-SiN$_X$:H interface and in the a-SiN$_X$:H transitional layer near the a-Si:H/a-SiN$_X$:H interface. However, when longer stress times,

higher stress electric fields or higher stress temperatures are applied then large concentration of states in the insulator near the a-Si:H/a-SiN_X:H interface will get filled and as a result probability of emission from these states increases.

Staebler et al. [54] reported that β and τ are independent of gate bias while ΔV_0 is dependent on gate bias and is given as $\Delta V_0 \approx V_g - V_{ti}$ with no power dependence (i.e., $\alpha = 1.0$). β is given as $\beta = \left(T_{ST}/T_0^*\right) - \beta_0$ with $T_0^* \approx 229$ K and $\beta_0 \approx 1.04$ for $T_{ST} \leq 80$ °C while for $T_{ST} \geq 80$ °C, β becomes temperature independent with $\beta \approx 0.5$. A nonzero value of β_0 shows that ΔV_T is independent of gate dielectric which differs from the conclusion given by previous researchers [55].

8.4.3 Nathan's Model

Nathan and his group [56] proposed that when a bias is applied on the gate terminal with the drain and source grounded then the threshold voltage shift shows the power law dependence on gate bias stress and can be given by defect pool model [57]. According to defect pool model, the rate of defect state creation is dependent on barrier to defect state formation, number of band tail electrons and density of week Si–Si bonds. Thus, the threshold voltage shift is given as

$$\Delta V_T = A(V_{ST} - V_{Ti})(t)^{\beta} \tag{8.20}$$

where V_{ST} is the gate bias stress voltage, V_{Ti} is the threshold voltage of TFT before gate bias is applied, A and β (~ 0.3) are temperature dependent parameters, and t is the gate bias stress time. However, when both gate and drain terminals of the nitrogen rich gate dielectric TFTs are subjected to bias voltage then for small gate stress biases (≤ 15 V), where the defect state creation is the dominant instability mechanism, TFT shows less threshold voltage shift as compared to the presence of only gate bias stress. Authors reported that the increase in drain bias stress results in the increase of lateral electric field which in turn decreases the channel carrier concentration (n_{BT}) close to drain. However, in the saturation mode ($V_{DS} = V_{GS} - V_T$), the channel carrier concentration remains constant and thus causes negligible threshold voltage shift. Similarly, TFTs subjected into deeper saturation ($V_{DS} > V_{GS} - V_T$) shows less threshold voltage shift. Thus, the charge stored on the gate when TFT is subjected to both gate and drain bias stresses is given as [56]:

$$Q_G = \frac{2}{3} C_G WL \frac{(V_{GS} - V_T)^3 - (V_{GD} - V_T)^3}{(V_{GS} - V_T)^2 - (V_{GD} - V_T)^2} \tag{8.21}$$

$$\text{In linear region, } V_{GD} = V_{GS}\, Q_{G0} = C_G \cdot W \cdot L(V_{GS} - V_T) \tag{8.22}$$

$$\text{In saturation region, } V_{GD} \rightarrow V_T \quad Q_G = \frac{2}{3} C_G \cdot W \cdot L(V_{GS} - V_T) \tag{8.23}$$

Now threshold voltage shift is given as,

$$\Delta V_T = \left(\frac{Q_G}{Q_{G0}}\right) A(V_{GS} - V_{Ti})(t)^{\beta} \tag{8.24}$$

where Q_G is given by Eq. (8.21) and Q_{G0} is given by Eq. (8.22)

In constant current stressing, the drain and gate terminals of the TFTs are shorted in the diode connected configuration with the source terminal grounded. The constant drain current is maintained by the progressive adjustment of the gate bias for the compensation of threshold voltage shift. Such compensation thus maintained the constant band tail carrier density (n_{BT}) and hence threshold voltage shift shows no trend of saturation.

Nathan and his group [58] further modified the power law dependency of ΔV_T which is given as

$$\Delta V_T(t) = [V_{GS}(t) - V_T(t)]^{\gamma} \left(\frac{t}{t_0}\right)^{\beta} \tag{8.25}$$

where

$$t_0 = \left(\frac{\beta w N_{BT}}{A N_{WB} D_{00} w^{\beta}}\right)^{\frac{1}{\beta}} \tag{8.26}$$

Here, A is proportionality constant, N_{BT} is the band tail states density, w is the attempt-to-escape frequency of hydrogen, D_{00} is the microscopic diffusion coefficient, β is power law index, and γ is a power parameter having values between 1.5 and 1.9. The power law parameters β, γ, and t_0 are dependent on temperature and stress history of the TFT.

8.5 Conclusion

The purpose of this chapter is to provide a detailed progress in the area of top-gate nc-Si TFT. The performance of top-gate nc-Si TFT depends upon the various process parameters used during its fabrication and also on the conduction and instability mechanisms that occurs under electrical stress. So an extensive review is provided by covering the fabrication techniques, conduction models and electrical instability mechanisms of top-gate nc-Si TFT which can be useful for its effective application in new generation displays.

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