Effect of Skin Impedance on Delay and Crosstalk in Lossy and Non-uniform On-Chip Interconnects

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Abstract An efficient finite-difference time-domain (FDTD) model is presented to analyse time delay and the crosstalk noise in lossy non-uniform interconnects. The complementary metal oxide semiconductor (CMOS) is used as driver for non-uniform interconnects and terminated with capacitive loads. Further, the resistive losses at high frequency due to skin effect and shrinking of interconnects are inculcated in the proposed model and analysed the high frequency effects. The improved alpha power law model represents the nonlinear behaviour of CMOS drivers, and the non-uniform interconnect is modelled including skin effect by FDTD technique. Hence, the proposed algorithm accurately estimates the crosstalk noise and delay in non-uniform interconnects at high frequencies and the results of FDTD are validated using HSPICE simulations.

Keywords Skin effect · FDTD · VLSI interconnects · CMOS

1 Introduction

In recent trends, faster and compact devices need smaller interconnect length and result in performance degradation in terms of delay, noise, and crosstalk. High-speed interconnects are normally modelled with an equivalent circuit having distributed RLGC parameters. Transmission lines with frequency-dependent variables are the best suit to describe electrical characteristics of on-chip interconnect. At earlier stages of VLSI design, it is necessary that CMOS technology needs keen

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modelling of CMOS gate-driven interconnect structures [1]. Driving of interconnects with the CMOS driver rises frequency/time conversion problem.

Recently, the authors in [2] proposed a model to analyse crosstalk accurately but it depends on even mode and odd mode and is suitable for loss less uniform interconnects. In [3], the authors proposed FDTD algorithm for analysing transients in CMOS gate-driven lossy uniform interconnects with frequency-dependent parameters. However, it is restricted to uniform interconnects, whereas for non-uniform interconnects it is unreported. In this work, the extension of frequency-dependent parameters is incorporated for non-uniform on-chip VLSI interconnects. In high-speed interconnects, due to skin effect, the current flows near the surface of the conductors and leads to increase in effective resistance [3]. In [4, 5], the authors proposed a method to explain propagation delay for non-uniform lossy transmission lines in time (t) domain using FDTD. In this work, parameters depending on frequency are also included. However, in this model a resistive driver is connected to transmission lines and terminates using resistive loads, so this analysis is not a practical one for on-chip interconnects which are having nonlinear drivers.

In this work, an efficient method is proposed for analyzing the crosstalk of CMOS gate driven loss non uniform interconnect system. Signal integrity issues are reported due to coupling in between the interconnect lines and nonlinear behaviour of CMOS driver. Further, CMOS driver's nonlinear behaviour is best described using improved alpha power law model and interconnects are modelled based on finite-difference time-domain (FDTD) model including frequency-dependence parameters.

2 Modelling of FDTD Algorithm for Non-uniform Lossy Interconnect System

In this section, the expressions for copper (Cu) interconnect line are developed using frequency-based skin impedance in (1) and the same is incorporated in FDTD model to find delay time and crosstalk at far end of the interconnect. The modelling part is represented below.

$$Z(z) = A_1(z) + B_1(z)\sqrt{s}. \tag{1}$$

2.1 Modelling of Non-uniform Lossy Interconnects with Frequency Dependency

Generally, transmission line model is best suit to analyse coupled interconnect lines because both have similar RLCG distributed elements [1]. The transmission line

(TL) expression with space and time dependency is modelled [7, 8] as in (2a) and (2b), and the equivalent two-coupled non-uniform lossy line is shown in Fig. 1.

$$\frac{\partial}{\partial z}v(z,t)+Z(t)i(z,t)=-l(z)\frac{\partial}{\partial z}i(z,t) \tag{2a}$$

$$\frac{\partial}{\partial z}i(z,t)+g(z)v(z,t)=-c(y)\frac{\partial}{\partial z}v(z,t) \tag{2b}$$

The internal impedance and current of the transmission line Eq. (2a) and (2b) are transformed to Laplacian domain as

$$Z(z,s)*i(z,s)=Z(z,t)i(z,t). \tag{3}$$

From Eq. (1) in Eq. (3),

$$L^{-1}\{Z(z,s)i(z,s)\}=A_1(z)i(z,t)+L^{-1}\left\{\frac{B_1(z)}{\sqrt{s}}\right\}*\frac{\partial}{\partial t}i(z,t). \tag{4}$$

The term $(1/\sqrt{s})$ in (4) having inverse transform as from [6] is

$$\frac{1}{\sqrt{\pi t}}=\frac{1}{\sqrt{s}}. \tag{5}$$

By substituting Eq. (5) in (4) gives

$$Z(z,t)*i(z,t)=\left\{A_1(z)i(z,t)+\left(\frac{1}{\sqrt{\pi}}\right)B_1(z)\int_0^t\frac{1}{\sqrt{p}}\frac{\partial}{\partial(t-p)}i(z,t-p)\mathrm{d}p\right\}. \tag{6}$$

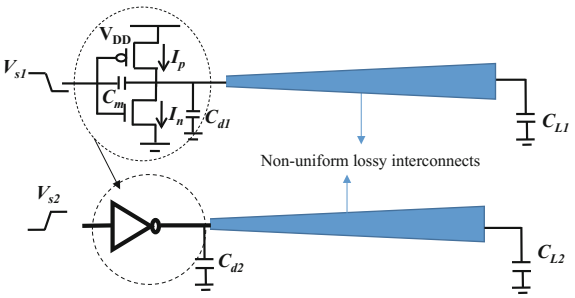

Fig. 1 Non-uniform lossy interconnect line existed by CMOS nonlinear gate

To solve lossy transmission line equations, FDTD is the most appropriate and widely used technique. By using this technique, the space position axis z is divided into equal subsections. Every adjacent V and I points are $\Delta z/2$ apart. Similarly, adjacent voltage and current time points are $\Delta t/2$ apart.

On applying finite-difference algorithm to Eq. (6) gives:

$$\int_0^t \frac{1}{\sqrt{p}} \frac{\partial}{\partial(t-p)} i(z,t-p)\mathrm{d}p = \int_0^t \frac{L(z,t-p)}{\sqrt{p}}\mathrm{d}p \tag{7}$$

where the function $L(z,t)$ is treated as constant over the time segment Δt. Thus, Eq. (7) becomes

$$\sum_{x=0}^{n} \int_{\Delta t(x)}^{\Delta t(x+1)} \frac{L(z,(n+1)(\Delta t-p))}{\sqrt{p}}\mathrm{d}p = \sqrt{\Delta t}\sum_{x=0}^{n} L(z,(x+1)\Delta t-p)P_0(x). \tag{8}$$

On applying finite-difference approximation to TL equations in (2a), (2b) and substituting (8) in (2a), results in (9a) and (9b) [9–11]

$$\begin{aligned} l(k)\frac{-i_k^{n+1/2}+i_k^{n+3/2}}{\Delta t} + \frac{v_{k+1}^{n+1}}{\Delta z} + A_1(k)\frac{i_k^{n+1/2}+i_k^{n+3/2}}{2} \\ + \frac{B_1(k)}{\sqrt{\pi\Delta t}}\sum_{x=0}^{n} P_0(x)\left\{i_k^{n+3/2-x} - i_k^{n+1/2-x}\right\} = 0 \end{aligned} \tag{9a}$$

$$c(k)\frac{v_k^{n+1}-v_k^n}{\Delta t} + g(k)\frac{v_k^n+v_k^{n+1}}{\Delta t} = -\frac{i_k^{n+1/2}-i_{k-1}^{n+1/2}}{\Delta z} \tag{9b}$$

where k = 1, 2,…., N_z. $v_k^n = v(\Delta z(k-1), \Delta t\, n)$; $i_k^n = (\Delta z\left(k-\frac{1}{2}\right), \Delta t n)$.

By solving (9a) and (9b)

$$\begin{aligned} \left[\frac{l(k)}{\Delta t}+\frac{A_1(k)}{2}+\frac{B_1(k)P_0(0)}{\Delta t}\right] i_k^{n+3/2} = \left[\frac{l(k)}{\Delta t}-\frac{A_1(k)}{2}+\frac{B_1(k)P_0(0)}{\Delta t}\right] i_k^{n+1/2} - \frac{v_k^{n+1}-v_k^{n+1}}{\Delta z} \\ - \frac{B_1(k)P_0(0)}{\Delta t}\sum_{x=1}^{n} P_0(x)\left(i_k^{n-x+3/2} - i_k^{n-x+1/2}\right) \end{aligned} \tag{10}$$

$$\left[\frac{C(k)}{\Delta t}+\frac{G(k)}{2}\right] V_k^{n+1} = \left[\frac{C(k)}{\Delta t}-\frac{G(k)}{2}\right] V_k^n - \frac{I_k^{n+1/2}-I_{k-1}^{n+1/2}}{\Delta z}. \tag{11}$$

A bootstrapping method is used to solve the Eqs. (10) and (11). The interconnect line voltage and current values are assigned as zero. After applying input to the line, from Eq. (11) the voltages are evaluated based on previous voltage and current

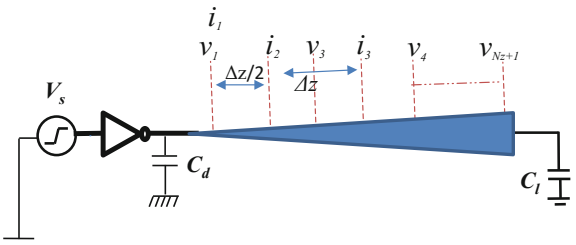

Fig. 2 Interconnect line with space discretization along its length for implementing FDTD model

solutions; later using Eq (10), currents are evaluated in terms of present current and past voltages. The space discretization for performing the bootstrapping mechanism along the line is shown in Fig. 2.

Putting $k = 1$ and $N_Z + 1$ in Eq. (11) results (12) and (13) for near- and far-end equations, respectively.

$$\left[\frac{c(1)}{\Delta t}+\frac{g(1)}{2}\right]v_1^{n+1}=\left[\frac{c(1)}{\Delta t}-\frac{g(1)}{2}\right]v_1^{n}-\frac{i_1^{n+1/2}-i_0^{n+1/2}}{\Delta z/2} \tag{12}$$

$$\left[\frac{c(N_z+1)}{\Delta t}+\frac{g(N_z+1)}{2}\right]v_{N_z}^{n+1}=\left[\frac{c(N_z+1)}{\Delta t}-\frac{g(N_z+1)}{2}\right]-\frac{i_{N_z+1}^{n+1/2}-i_{N_z}^{n+1/2}}{\Delta z/2}. \tag{13}$$

The line current at near end $z = 0$ is i_0 and at far end $z = l$ as i_{N_z+1}. Then, KCL expression is represented in (14) and (15), respectively.

$$i_0 = i_p - i_n + c_m\left(\frac{\mathrm{d}(v_s^n - v_1^{n+1})}{\mathrm{d}t}\right) - C_d\frac{\mathrm{d}v_1}{\mathrm{d}t} \tag{14}$$

$$i_{N_z+1} = C_l\frac{\partial v_{N_z+1}}{\partial t}. \tag{15}$$

By substituting Eq. (14) and Eq. (15) in (12) and (13) yields (16) and (17), respectively. These are the expressions for line voltage and currents at any point along the interconnect lines and for $k = N_a + 1$.

$$v_1^{n+1}=\left[\frac{c(N_a+1)}{\Delta t}+\frac{g(N_a+1)}{2}\right]^{-1}\left\{\begin{array}{l}\left[\frac{c(N_a+1)}{\Delta t}-\frac{g(N_a+1)}{2}\right]v_1^n-\frac{2}{\Delta z}i_1^{n+1/2}\\+\frac{2}{\Delta z}\left(i_p^{n+1/2}-i_n^{n+1/2}-c_m\left(\frac{d(v_{in}^n-v_1^n)}{dt}\right)+C_d\left(\frac{dv_1^{n+1/2}}{dt}\right)\right)\end{array}\right\} \tag{16}$$

$$i_k^{n+3/2} = \left[\frac{l(k)}{\Delta t} + \frac{A_1(k)}{2} + \frac{B_1(k)P_0(0)}{\Delta t}\right]^{-1} \left\{ \begin{array}{l} \left[\frac{l(k)}{\Delta t} - \frac{A_1(k)}{2} + \frac{B_1(k)P_0(0)}{\Delta t}\right] i_k^{n+1/2} - \frac{v_k^{n+1} - v_k^{n+1}}{\Delta z} \\ - \frac{B_1(k)P_0(0)}{\Delta t} \sum_{x=1}^{n} P_0(x)\left(I_k^{n-x+3/2} - I_k^{n-x+1/2}\right) \end{array} \right\}. \quad (17)$$

3 Results and Discussions

In this section, the proposed FDTD model for interconnect lines is validated using HSPICE simulations for different input conditions. Consider a two-coupled non-uniform interconnects shown Fig. 1. The input excitation given as 0.9 V pulse with duty cycle of 50% and rise/fall times is 50 ps and pulse width of 300 ps.

The load capacitance (C_L) is 1fF. The interconnect line length is 1 mm, the spatial discretization of the non-uniform lines chosen to be 10 segments, and the time discretization is $\Delta t = 100\Delta$tmax.

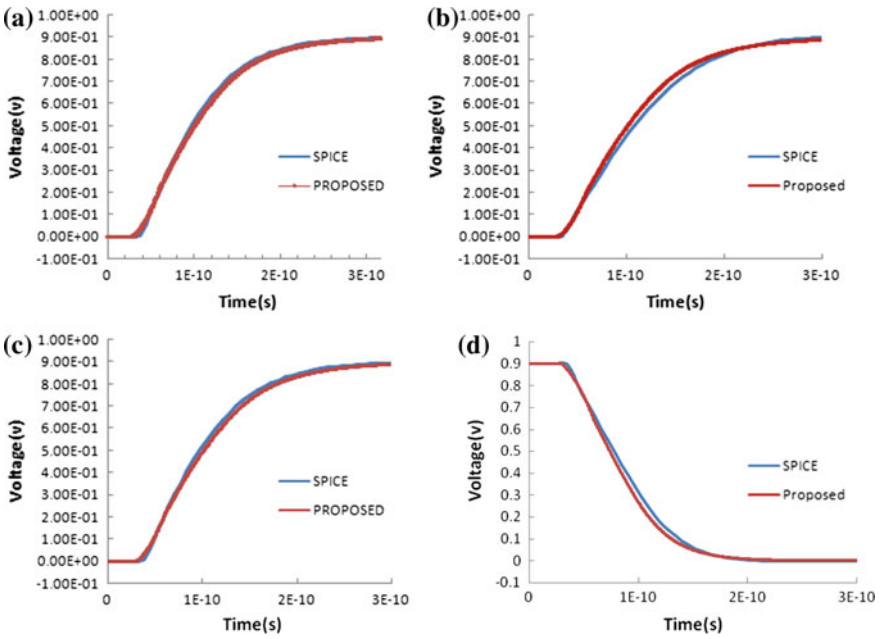

Fig. 3 Time-domain response at **a** port 3 in-phase, **b** port 4 in-phase, **c** port 3 out-phase, and **d** port 4 out-phase

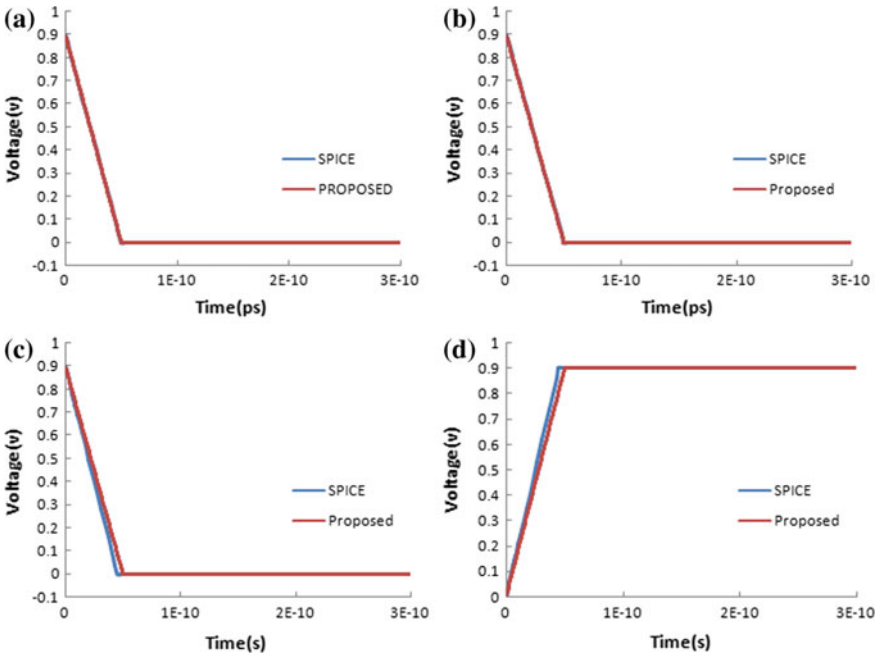

Fig. 4 Time-domain response at **a** port 1 in-phase, **b** port 2 in-phase, **c** port 1 out-phase, and **d** port 2 out-phase

The p.u.l parameters are represented as follows:

$$l = \begin{bmatrix} L_1 & L_{12} \\ L_{12} & L_2 \end{bmatrix} \text{nH/m} \quad c = \begin{bmatrix} C_1 & C_{12} \\ C_{12} & C_2 \end{bmatrix} \text{pF/m}$$

$$g = \begin{bmatrix} G_1 & 0 \\ 0 & G_2 \end{bmatrix} \text{S/m} \quad R = \begin{bmatrix} R_1 & 0 \\ 0 & R_2 \end{bmatrix} \Omega/\text{m}$$

where $L_1 = L_2 = L(y) = 387/1 + \lambda(y)$; $L_{m12}(y) = \lambda(y)L(y)$; $C(y) = 104.3/(1 + \lambda(y))$; $C_{12}(y) = -\lambda(y)C(y)\,\mathrm{R}_1 = \mathrm{R}_2 = 60\,\Omega/\mathrm{m}$

$$G_1 = G_2 = G(y) = 0.001/[1 - \lambda(y)]$$
$$\lambda(y) = 0.25\left[1 + \sin\left(6.25\pi y + \tfrac{\pi}{4}\right)\right]$$

At far end of interconnect, the transient response is observed and shown in Fig. 3a–d. At near end, the transient response is shown in Fig. 4a–d. The results are validated with HSPICE simulations.

4 Conclusion

An efficient frequency-dependent FDTD model is developed for non-uniform lossy interconnect lines to analyse near- and far-end transient analyses for interconnects. Further, the proposed algorithm is validated using HSPICE simulation results in very good accuracy in predicting the response. The time delay analysis is done by comparing the near- and far-end interconnect time delays using FDTD, and the same is validated using HSPICE. Hence, the model is verified accurately both in predicting the timing response and delay of the on-chip interconnect lines.

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