Implementation of Adder Circuit Using Quantum-Dot Cellular Automata-Based Logic Gates

Priyanka Kumari, Abhay Sharma and Arpita Singh

Abstract Quantum-dot Cellular automata (QCA) is nanotechnology that can be acquired to replace transistor-based design. The approach of transistor is based on charge transport; the primitive element in QCA is a cell; the communication between cells is solely Columbic hence there is no physical transport of charge. The major feature includes higher packaging density and lower power consumption. QCA cell-based structures can implement the logic gates, wires, memory units, combinational and sequential logic circuits. Digital logic design employing QCA cell is the main focus of this paper. In this paper, structure for Exclusive OR operation is proposed with primary goal of application in adder circuit to reduce the area. QCA designer is the EDA tool used for implementation and functional verification of the proposed structures.

Keywords Quantum-dot cellular automata (QCA) · EXOR gate
Half adder · Full adder

1 Introduction

As VLSI technology has made striking development which is continuously waning in future. The fundamental limit of MOSFET technology is its dimensional scaling which suffers from short channel and narrow channel effect which reduces

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performance. Other limitation deals with it is interconnects problem and power dissipation of the devices. In the trend of minimization of device size, researchers are trying to find other alternatives supplement to conventional transistors [1]. And QCA technology is one of its representatives.

In this paper, a QCA EX-OR circuit is proposed which is further being used in a half adder circuit as reposing the severe clocking scheme. There are three majority gates, and one inverter is being used in the proposed circuit. In QCA, the device can be used as an interconnect [2].

The QCA approach is firstly introduced in [3] as an effective ultra dense devices with higher performance. Basically a QCA cell is quadratic in shape that exhibits 3D quantum confinement. There are four quantum dots in a single cell oriented at the corner sides of the square which are coupled capacitively and tunnel barrier [4]. A quantum dot is a region of low potential encompasses by higher potential region which is able to detain electron of lower energies known as potential well [5]. These quantum dots comprise by the constitute of group II-VI, III-V, and IV-V Ex-CdSe, PbSe, and InP [1, 6].

These QCA cell can contain two electrons, which are free to move between adjacent dots known as tunneling. In a QCA cell, transfer of information does not depend on the transport of electron as in conventional transistor, while on the location and adjustment of electron in a small area. And when feature size approaches to nanometer size, then quantum effect tunneling take place [3] by which electrons changes their position as depicted in Fig. 1.

There exist two charged electrons in a cell which always try to achieve the opposite corners due to repulsive electrostatic force. According to electron position in a cell, these two kinds of cell polarization or binary values take place and the values of these polarizations are defined by following equation:

$$P = \frac{(P_2 + P_4) - (P_1 + P_3)}{P_1 + P_2 + P_3 + P_4},$$

where P_j is the columbic charge at dot j. This equation shows that location of electrons at site 2 and 3 yield $P = +1$ polarization and location at site 1 and 4 will give $P = -1$ polarization. The fundamental idea of QCA cell is generic and can be

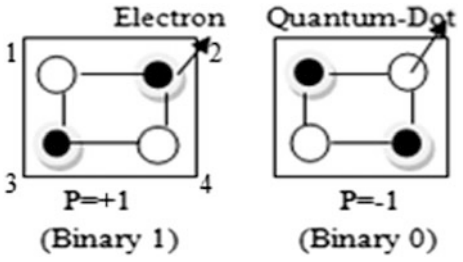

Fig. 1 QCA cells with electrons indicating logic level

implemented by various methods: molecular implementation, semiconductor implementation, and magnetic implementations [5, 7, 8]. Arrangement of these cells in an array is used to perform all logical functions like wires, memories, logic gates, all combinational and sequential circuits.

QCA designer tool is being used for an extant work of layout for quantum-dot cellular automata (QCA) by the Walus Group of B. Columbia University produces a fast and accurate simulation [9] by providing the powerful CAD features. QCA designer can simulate more complex computational circuits for general purpose.

2 Clock Zone

To attain the controllable data direction, cells are set into the four clock zones. For the synchronization of QCA circuit, clock plays a very crucial role [5]. A QCA array is categorized into four clock zones which are 90 degree in phase shift from one clock zone to another (Fig. 2).

These clock zones have four states: low-to-high, high, high-to-low, and low which are correspondingly referred as relax, switch, hold, and release [10]. These cells start computing during the high-to-low and hold the value during the low state [5]. Switch phase occurs when cells being unpolarized and having low potential barrier in increasing order. High potential barriers are achieved in the hold phase and lower potential barriers attained in release phase [11]. In relax phase, barriers cells are kept in unpolarized state at low level [12, 13].

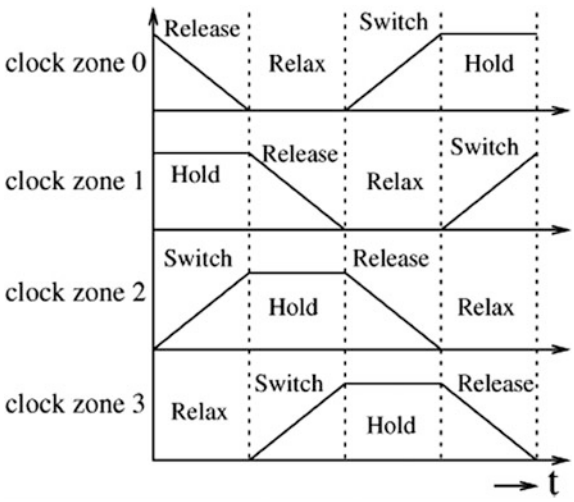

Fig. 2 QCA clocks zones [2]

3 QCA Wire

A series of Quantum cell driven by the fixed polarization work as a wire and flow of signal is controlled with clock. The binary signals propagate from one end to another end by the electrostatic interaction between cells [14]. The state of the first polarized drive cell induces the same polarization in the complete series of the cells [15]. By this method, information propagated from first cell to last cell. There are two kinds of configuration of wire (Fig. 3).

4 Logic Gates Based on QCA Logic

4.1 Majority Gate

It is the fundamental logic function being used in QCA which uses odd number of input more than one. In Fig. 4, majority gate has been shown. It is denoted as $M(A, B, C) = AB + BC + CA$. By using these majority gates, two input AND gate and OR gate can be implemented by fixing one of its input at polarization−1 (binary 0) and polarization+1 (binary 1), respectively.

For AND operation: $-M(a, b, 0) = a \cdot b$,
For OR operation: $-M(a, b, 1) = a + b$.

4.2 Inverter

It is another basic logic gate used in QCA. On applying 1 at input, output 0 is attained and vice versa. It is denoted in (Fig. 5).

To implement the circuit of an inverter cell should be arranged at overlapping condition at input side and at other ends corner of the cells should be matched to invert the value at output.

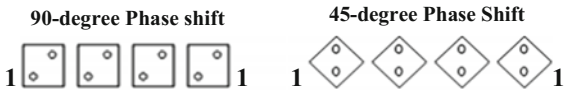

Fig. 3 QCA wires configurations

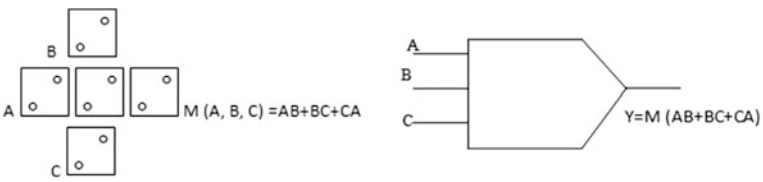

Fig. 4 QCA majority gate

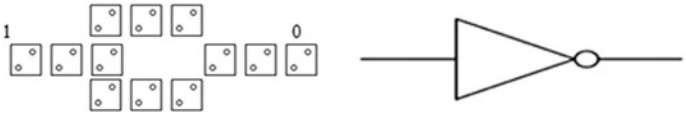

Fig. 5 QCA inverter circuit

5 QCA Cell Placement Technique: Crossover Technique

The printing area is 122 mm; crossover techniques introduce the concept of building QCA devices which are able to execute computation as a function of synchronization. QCA follows two kinds of crossover or can say interconnection technique known as coplanar and multilayer techniques. A coplanar technique is one layer technique either regular or rotated or simultaneous cell configuration technique. While multilayer technique uses bridge kind of structure, i.e., one layer deposited over another layer. It is complex in nature due to deposition of one layer over another and it is fiddle to implement [10, 11, 16, 17] (Fig. 6).

6 Conventional Circuit Using Multilayer Architecture

6.1 EX-OR Gate

It is a universal gate and used in various adder circuits and comparator and so many. EX-OR gate gives high at different level input and low at same level input.

$$Y_{\text{out}} = PQ' + P'Q.$$

This Boolean expression has been implemented in the circuit designing depicted in Fig. 7, using the multilayer crossover technique and can be realized more than one way. This technique uses the three majority gates and two inverters.

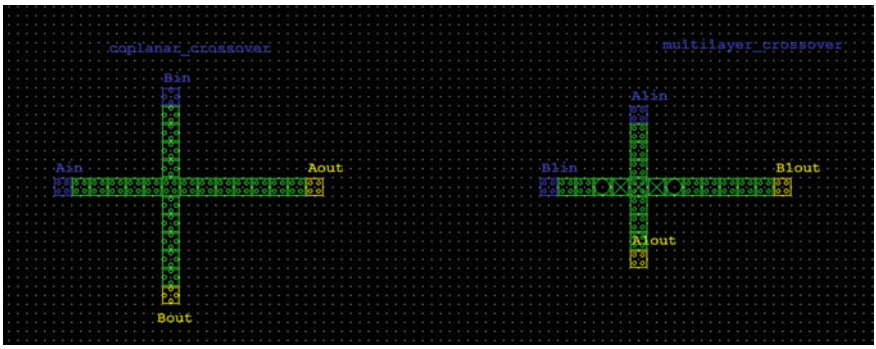

Fig. 6 Crossovers technique

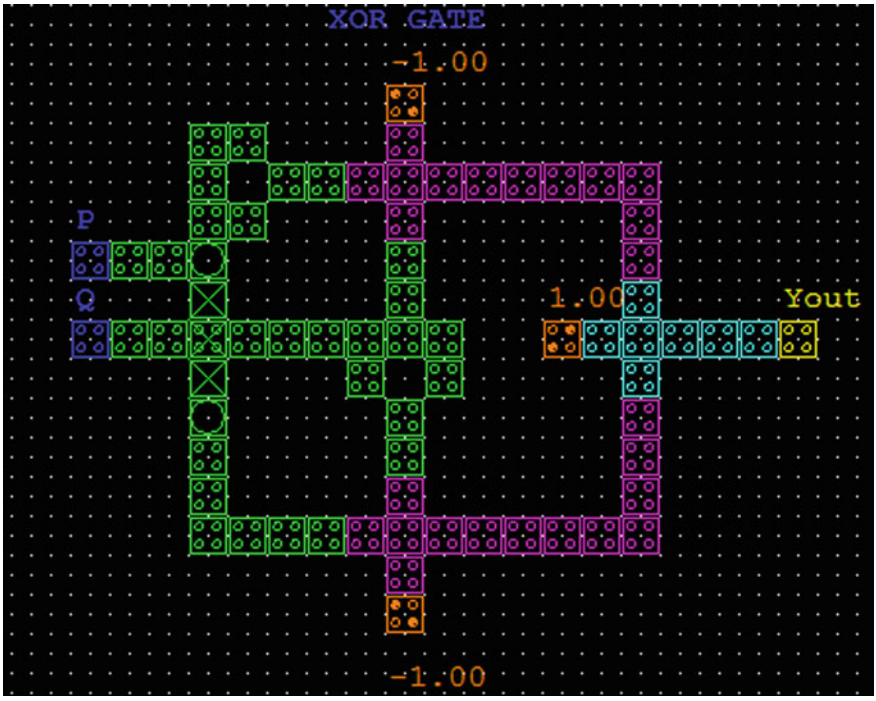

Fig. 7 Conventional EX-OR gate

6.2 *Half Adder*

Half adder is an arithmetic circuit which is used for addition of two numbers and produces a sum and carries as the output, e.g., if P and Q are the inputs then the sum will be the EX-OR of P and Q and the carry will be the AND of P and Q [6] (Figs. 8 and 9; Tables 1 and 2).

6.3 *Full Adder*

A one-bit full adder used to add three one-bit numbers and generate a carry. If P, Q, and R three input bits then the sum will be the EX-OR of P, Q, and R and the carry will be $PQ + QR + PR$. Layout and simulation of full adder have been shown in Figs. 14 and 15, respectively, (Table 3).

$$\text{SUM} = P \,\text{XOR}\, Q \,\text{XOR}\, R,\ \text{CARRY} = PQ + QR + PR.$$

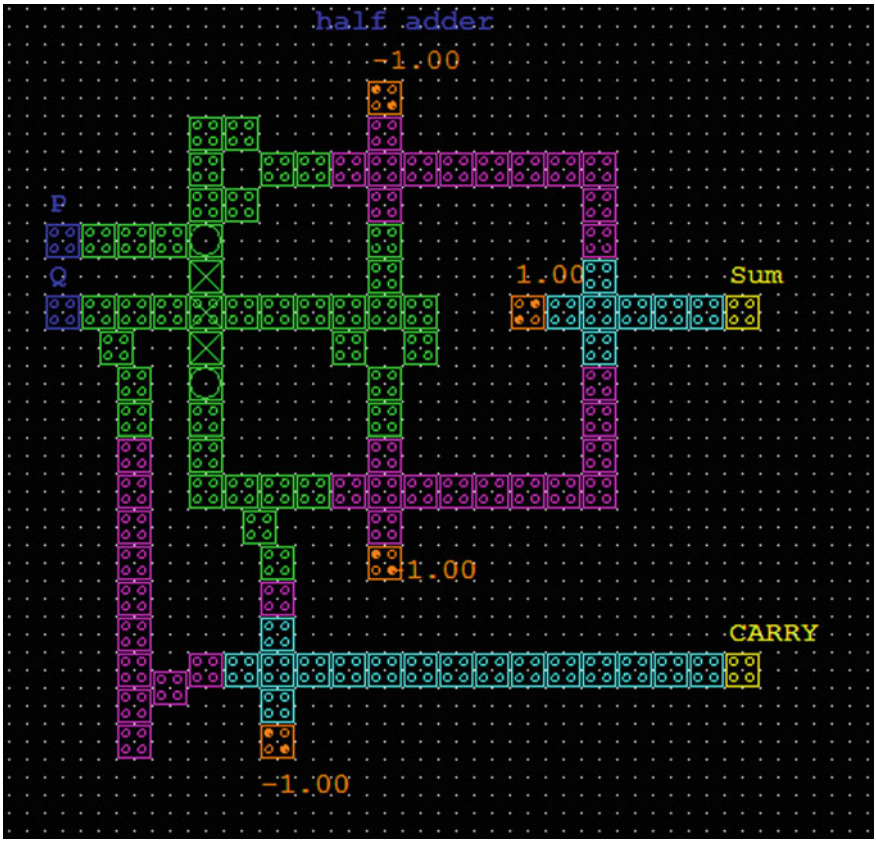

Fig. 8 Half adder circuit

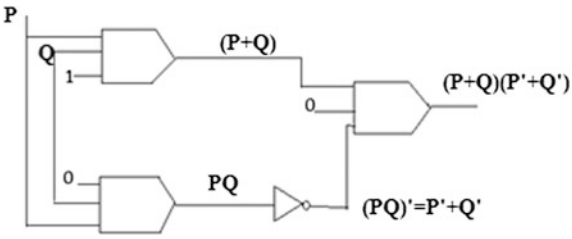

Fig. 9 Logical implementation of EX-OR gate

Table 1 EX-OR gates truth table

P	Q	Y_{out}
0	0	0
0	1	1
1	0	1
1	1	0

Table 2 Half-adder gates truth table

P	*Q*	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

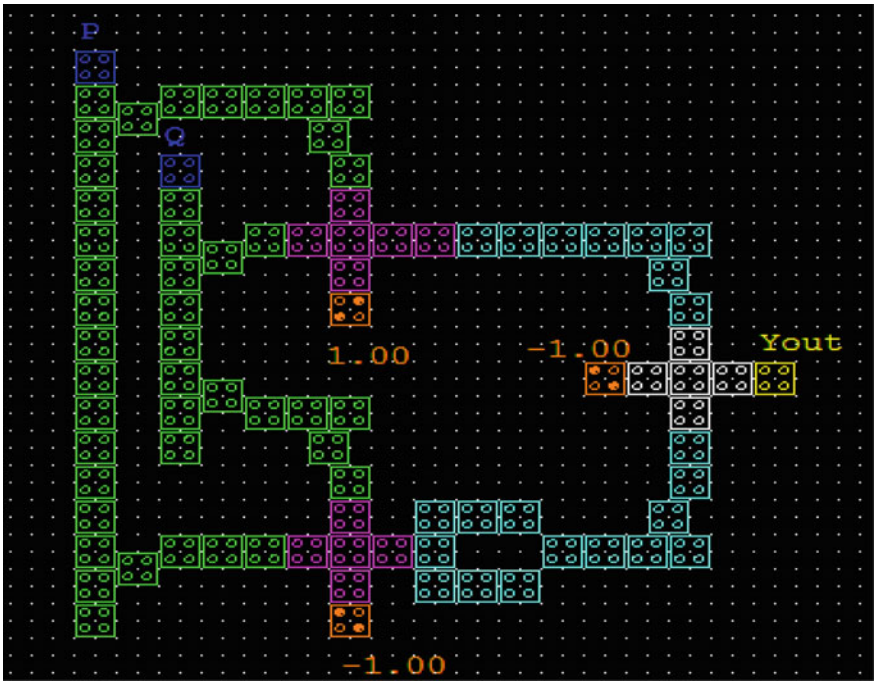

Fig. 10 Layout of EX-OR gate

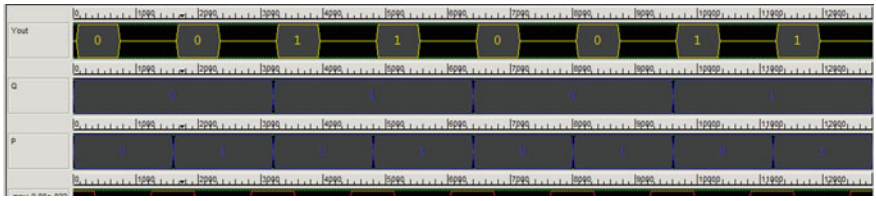

Fig. 11 Simulation of EX-OR gate

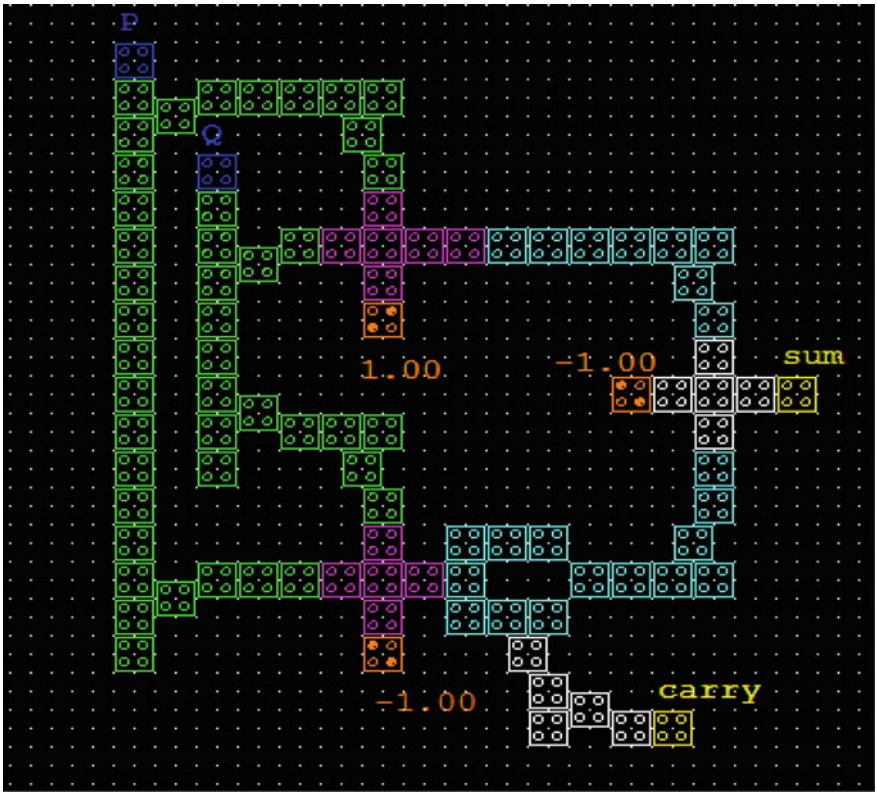

Fig. 12 Layout of half-adder using coplanar EX-OR gate

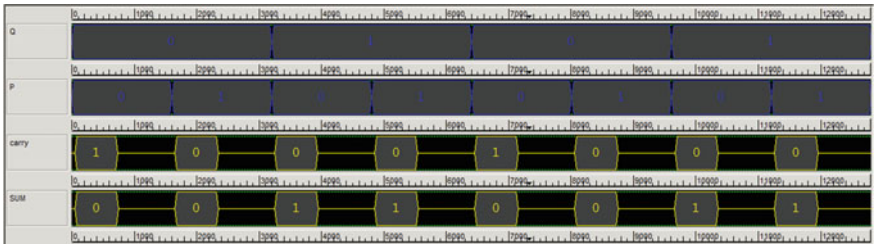

Fig. 13 Simulation of half adder

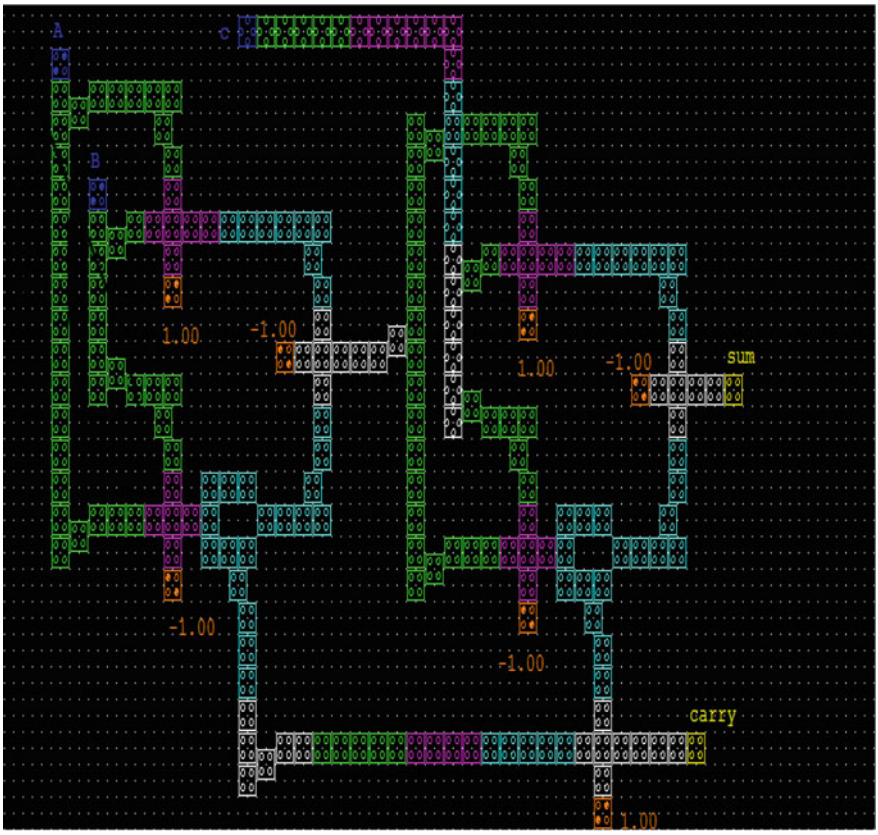

Fig. 14 Layout of full adder using coplanar half adder

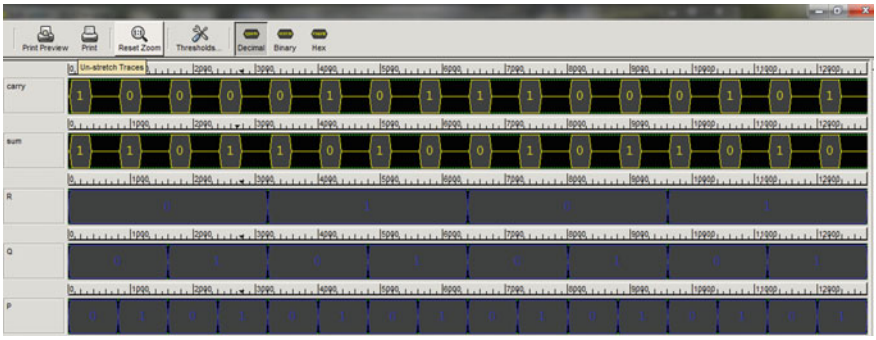

Fig. 15 Simulation of full adder using half adder

Table 3 Full adder truth table

P	Q	R	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

7 Proposed Circuit of EX-OR Gate, Half Adder, and Full Adder Using Coplanar Technique

In the proposed circuits, three majority gates and one inverter are being used [14].

$$\text{Sum} = (P+Q).(PQ)' = (P+Q).(P'+Q') = P'Q + PQ',$$

$$\text{Carry} = PQ.$$

The layout of the above Boolean expression has been shown in Figs. 10 and 12 along with the simulation result in Fig. 11 and in Figs. 13, 14 and 15.

8 Comparison

See Table 4.

Table 4 Area comparison between different structures

Crossover structure	Cell count	Area (nm^2)
Multilayer XOR	**77**	12,663
Multilayer half adder	114	185,318
Coplanar XOR	88	137,706
Coplanar half adder	94	141,954
Coplanar full adder	221	370,670

9 Conclusion

QCA is the answer for transistor-less design. In this paper, it is demonstrated how QCA cells can be arranged to obtain exclusive or operation. Further, it was proposed that half adder and full adder operation can be implemented employing the QCA cell-based structure. It was also observed that coplanar crossover architecture for EX-OR gate was less complex in terms of implementation when compared to multilayer crossover structure. Area was significantly reduced in half adder and full adder designs when the proposed architecture for EX-OR operation was used. This fact is illustrated in Table 4 where comparison of various adder structures has been provided. All the QCA cell-based structures were implemented on QCA designer tool with multi-phase clock propagation.

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