Lecture Notes in Electrical Engineering 436

Amik Garg
Akash Kumar Bhoi
Padmanaban Sanjeevikumar
K.K. Kamani
Editors

Advances in Power Systems and Energy Management

ETAEERE-2016

Springer

Lecture Notes in Electrical Engineering

Volume 436

About this Series

"Lecture Notes in Electrical Engineering (LNEE)" is a book series which reports the latest research and developments in Electrical Engineering, namely:

- Communication, Networks, and Information Theory
- Computer Engineering
- Signal, Image, Speech and Information Processing
- Circuits and Systems
- Bioengineering

LNEE publishes authored monographs and contributed volumes which present cutting edge research information as well as new perspectives on classical fields, while maintaining Springer's high standards of academic excellence. Also considered for publication are lecture materials, proceedings, and other related materials of exceptionally high quality and interest. The subject matter should be original and timely, reporting the latest research and developments in all areas of electrical engineering.

The audience for the books in LNEE consists of advanced level students, researchers, and industry professionals working at the forefront of their fields. Much like Springer's other Lecture Notes series, LNEE will be distributed through Springer's print and electronic publishing channels.

More information about this series at http://www.springer.com/series/7818

Amik Garg · Akash Kumar Bhoi
Padmanaban Sanjeevikumar
K.K. Kamani
Editors

Advances in Power Systems and Energy Management

ETAEERE-2016

Springer

Editors
Amik Garg
Sikkim Manipal Institute of Technology (SMIT)
Rangpo, Sikkim
India

Akash Kumar Bhoi
Department of Electrical and Electronics Engineering
Sikkim Manipal Institute of Technology (SMIT)
Rangpo, Sikkim
India

Padmanaban Sanjeevikumar
Department of Electrical and Electronics Engineering Science
University of Johannesburg
Johannesburg
South Africa

K.K. Kamani
Government of Karnataka
Chitradurga, Karnataka
India

ISSN 1876-1100 ISSN 1876-1119 (electronic)
Lecture Notes in Electrical Engineering
ISBN 978-981-10-4393-2 ISBN 978-981-10-4394-9 (eBook)
https://doi.org/10.1007/978-981-10-4394-9

Library of Congress Control Number: 2017937707

Printed on acid-free paper

This Springer imprint is published by Springer Nature
The registered company is Springer Nature Singapore Pte Ltd.
The registered company address is: 152 Beach Road, #21-01/04 Gateway East, Singapore 189721, Singapore

Preface

Advances in Electronics, Communication and Computing is a collection of research articles and critical review articles presented at the International Conference on 'Emerging Trends and Advances in Electrical Engineering and Renewable Energy—ETAEERE-2016', organized by the Department of Electrical and Electronics Engineering (EEE) of Sikkim Manipal Institute of Technology (SMIT), Majhitar, Sikkim, India during December 17–18, 2016. This was a unique conference which combined renewable energy, electronics, computing, communication, systems, controls and automations under one roof. Moreover, it is a matter of honour for SMIT to learn that Springer was associated with ETAEERE-2016 as a major publication sponsor for the event. The proceedings of this conference came out with four different book volume titles under Lecture Notes in Electrical Engineering (LNEE). This book is a compilation of research work in the interdisciplinary areas of electronics, communication and computing. The chapters of this book cover the different approaches and techniques for specific applications, such as particle swarm optimization, Otsu's function and harmony search optimization algorithm, triple-gatesilicon-on-insulator (SOI) MOSFET, micro-Raman and Fourier Transform Infrared Spectroscopy (FTIR) analysis, high-k dielectric gate oxide, spectrum sensing in cognitive radio, microstrip antenna, ground-penetrating radar (GPR) with conducting surfaces and digital image forgery detection.

Eminent speakers like Prof. A Chakrabarti, former vice-chancellor of Jadavpur University; Prof. A Rajaraman of IIT, Chennai; Prof. Gyoo-Shee Chae of Baekseok University, South Korea; Prof. Avinash Konkani of University of Virginia, USA; Prof. Kamani KK, the global economic advisor of Karnataka; Prof. Manjesh of Bangalore University and Dr. Amitanshu Patnaik of DRDO Delhi shared their knowledge and experience. The conference attended and presented by participants from institutes such as IISc, IITs, NITs, NEHU, BIT, VIT, MIT Manipal, IIEST Kolkata, and abroad deliberated on their research works. In addition, the paper presentations were accompanied by six keynote addresses from leading academic and industry researchers around the globe. The paper presentations took place in three different tracks with 18 parallel sessions. Through the platform of

ETAEERE-2016, we got the opportunity to promote the national campaign ‘Make In India’.

The review committee has done an excellent job in reviewing the articles and approving the high-quality research articles to be published in the conference proceedings. The editors are thankful to all of the faculty and students of these various committees for their dedication in making this a very successful conference and also to the editing and printing support staff of Springer for making the compilation possible. We sincerely hope that this volume will inspire researchers.

Majhitar, Sikkim, India

Karma Sonam Sherpa
Akash Kumar Bhoi
Mohammed Nasir Ansari
Amit Kumar Singh

Editorial Board

Chief Patron

Prof.(Dr.) Somnath Mishra, Vice-Chancellor, Sikkim Manipal University

Patron

Prof.(Dr.) Ashis Sharma, Registrar, SMU
Prof.(Dr.) Amik Garg, Director, SMIT
Prof.(Dr.) Sadasivan Thekkey Veetil, Joint Director, SMIT

Programme Chair

Dr. Rabindranath Bera, SMIT
Dr. Karma Sonam Sherpa, SMIT
Dr. Kalpana Sharma, SMIT
Dr. H.K.D Sarma, SMIT
Dr. Tejbanta Singh Chingtham, SMIT
Dr. Utpal Deka, Physics, SMIT
Dr. B.B Pradhan, SMIT
Dr. Samarjeet Borah, Dept. of CA, SMIT
Dr. Gobinda Chandra Mishra, SMIT
Prof. Om Prakash Singh, SMIT

Special Session Chairs

Dr. Sabyasachi Sen Gupta, IIT Kharagpur
Dr. Samrat Paul, NEHU, Shillong
Dr. Swagatam Das, ISI, Kolkata
Dr. Abhijit Chakrabarti, IIEST, Shibpur
Prof. Kamani K.K, Dept. of Higher Education, Govt. of Karnataka (Global Economic Adviser)
Dr. GS Chae, Baekseok University, South Korea
Prof. Natarajan Gajendran, Editor IJST, President (iSee)
Dr. Manjesh, Dept. of Electronic Science, Bangalore University
Dr. Amitanshu Patnaik, DTRL, DRDO

International Advisory Committee

Dr. Avinash Konkani, AHFP, Clinical Engineer, University of Virginia Health System, USA
Dr. P. Sanjeevikumar, Dept. of EEE, University of Johannesburg, South Africa
Dr. Ahmed Faheem Zobaa, BU, UK
Dr. Akhtar Kalam, VU, Australia
Dr. David YU, UWM, USA
Dr. Atilla Elci, Chairman, Dept. of EEE, Aksaray University, Turkey
Dr. Dmitri Vinnikov, TUT, Estonia
Dr. Hussain Shareef, UKM, Malaysia
Dr. Seshadev Sahoo, Purdue University, USA
Dr. Anil Kavala, Sr. Engineer, Samsung Electronics, Seoul, South Korea
Dr. Kamran Morovati, University of New Brunswick, Canada
Dr. Joseph Olorunfemi Ojo, TTU, USA
Dr. Mohamed A. Zohdy, OU, MI
Dr. Murad Al-Shibli, Head, EMET, Abu Dhabi
Dr. Nesimi Ertugrul, UA, Australia
Dr. Omar Abdel-Baqi, UWM, USA
Dr. Richard Blanchard, LBU, UK
Dr. Shashi Paul, DM, UK

National Advisory Committee

Dr. Sabyasachi Sen Gupta, IIT Kharagpur
Prof. Kamani K.K, Dept. of Higher Education, Govt. of Karnataka (Global Economic Adviser)

Reviewer Committee

Organizing Committee

(Sikkim Manipal Institute of Technology)

Overall Incharge
Prof. Karma Sonam Sherpa—Convenor
Prof. Akash Kumar Bhoi—Secretary
Prof. Mohammed Nasir Ansari—Convenor
Prof. Amit Kumar Singh—Convenor

Publicity
Prof. Pradeep Kumar Mallick
Prof. Himangshu Pal

Hall and Stage Arrangements
Prof. Shabbiruddin
Prof. Sandip Kumar Gupta

Caterings and Refreshment
Prof. Sunam Saha
Prof. Roshan Pradhan

Transport
Prof. Arunava Tikader
Prof. Arijit Ghosh

Help Desk and Registration
Prof. Chitrangada Roy
Prof. Dibyadeep Bhattacharya

Sponsorship
Prof. Saikat Chatterjee
Prof. Anirban Sengupta

Guest Hospitality
Prof. Moumi Pandit
Prof. Bijay Rai
Prof. Rahul Kumar

Printing
Prof. Pratik Pradhan
Prof. Rajiv Pradhan

Student Organizing Committee

(Sikkim Manipal Institute of Technology)

Yupphung Keimba Limbu
Kunglho Lepcha
Sagar Pradhan
Avinash Gupta
Avinash Pradhan
Tshering Sangmo Sherpa
Sisir Chettri
Deepika Chettri
Suyog Pradhan
Shristi Shresta
Pankaj Kumar
Biswas Pradhan
Ritika Pradhan
Aruna Chettri
Ashish Lamichaney
Neeta Lamichaney
Ashutosh Mukherjee
Amit KR. Singh
Gyan Shree
Dheeraj Kumar
Raval Parth Pradip
Srihari K
Saurabh Bhowmik
Madhura Pardhe

Contents

Non-isolated Sextuple Output Hybrid Triad Converter Configurations for High Step-Up Renewable Energy Applications 1
Padmanaban Sanjeevikumar, Mahajan Sagar Bhaskar, Pranav Dhond, Frede Blaabjerg and Michael Pecht

Dual-Band Wearable Rectenna for Low-Power RF Energy Harvesting 13
B. Naresh, Vinod Kumar Singh, V. Bhargavi, Amik Garg and Akash Kumar Bhoi

Reduction of THD in Nine-Phase Induction Motor Drive with CLC Filter 23
Manjesh, Nilima Siddhartha Dabhade, Amik Garg and Akash Kumar Bhoi

Comparative Study of Harmonics and Total Harmonic Distortion of Five-Phase Inverter Drive with Five-Phase Multilevel Inverter Drive Using Simulink/MATLAB 33
Manjesh, K. Hasitha, Akash Kumar Bhoi and Amik Garg

Design and Implementation of Two Level and Multilevel Inverter 39
Amruta Pattnaik, Shawet Mittal, Vinay Gupta, Basudev Prasad and Akash Kumar Bhoi

Raman Characterization of Gallium Nitride Nanowires Deposited by Chemical Vapor Deposition 47
Umesh Rizal and Bibhu P. Swain

Selection of an Electric Motor for an Equivalent Internal Combustion Engine by TOPSIS Method 63
K. Srihari, Parth Raval and Shabbiruddin

Analysis of Medium Voltage BTB System by Using Half Bridge Modular Multilevel Converter Topology 71
Yasmeena and G. Tulasi Ram Das

The Need for Uncertainty-Based Analysis in Power System Networks 87
Yoseph Mekonnen Abebe, P. Mallikarjuna Rao and M. Gopichand Naik

Impact of DC Bias on the Magnetic Loading of Three Phase Three Limb Transformer Based on Finite Element Method 97
Saurabh Kohli, S.B. Mahajan, Padmanaban Sanjeevikumar, Viliam Fedák and Valentin Oleschuk

Cost Optimization of a Ring Frame Unit 107
Rathinadurai Louis Helen Catherine, A. Soundarrajan and Josephine Rathinadurai Louis

Analysis of Power System Harmonics Using PSNR Metric 119
Srihari Mandava and Ramesh Varadarajan

Low Power Circularly Polarized Wearable Rectenna for RF Energy Harvesting 131
B. Naresh, Vinod Kumar Singh and V. Bhargavi

Performance Analysis of Series-Passive Filter in 5-Phase PWM Inverter Drive and Harmonic Study Using Simulink/Matlab 139
A.S. Ananda and Manjesh

Finding the Initial Variables for Affine Arithmetic-Based Power Flow Analysis 147
Yoseph Mekonnen Abebe, P. Mallikarjuna Rao and M. Gopichand Naik

Ecology and Energy Dimension in Infrastructural Designs 157
A. Rajaraman

Energy-Aware Data Aggregation Techniques in Wireless Sensor Network 165
M. Ambigavathi and D. Sridharan

Design and Performance Analysis of Noise Equivalent Model for Optical Fiber Link 175
Manoj Kumar Dutta

Improvement of Efficiency of a Three-Phase Induction Motor Using Robust Control 183
Anirban Sengupta

Improvement of Electrical Power Quality with Distributed Power Flow Controller with Fuzzy PWM Technique 193
Jyoti Saraswat and Jaydeep Chakravorty

New Sliding Mode Control of a Five-Phase Permanent Magnet Synchronous Motor Drive in Wide Speed Range 205
Anissa Hosseyni, Ramzi Trabelsi, Med Faouzi Mimouni, Atif Iqbal and Padmanaban Sanjeevikumar

Novel Sensorless Sliding Mode Observer of a Five-Phase Permanent Magnet Synchronous Motor Drive in Wide Speed Range 213
Anissa Hosseyni, Ramzi Trabelsi, Med Faouzi Mimouni, Atif Iqbal and Padmanaban Sanjeevikumar

Thermal Analysis of Inverter-Fed Induction Motor 221
Sunam Saha and Mohammed Nasir Ansari

Contingency Analysis Reliability Evaluation of Small-Signal Stability Analysis 229
A. Murugan, S. Jayaprakash and R. Raghavan

Finite Element Method Based Determination of Magnetic Loading of Three-Phase Five-Limb Transformer with Impact of DC Offset 241
Saurabh Kohli, S.B. Mahajan, S.M. Badave, Padmanaban Sanjeevikumar and Atif Iqbal

Sensorless Back Stepping Control for a Five-Phase Permanent Magnet Synchronous Motor Drive Based on Sliding Mode Observer 251
Anissa Hosseyni, Ramzi Trabelsi, Padmanaban Sanjeevikumar, Atif Iqbal and Med Faouzi Mimouni

A Compact Dual-Band N-Way Wilkinson Power Divider for GSM 263
Aijaz M. Zaidi, Syed A. Imam and Binod K. Kanaujia

Comparative Analysis of DC/DC Converters with MPPT Techniques Based PV System 275
S. Saravanan, N. Ramesh Babu and Padmanaban Sanjeevikumar

Single Phase Asymmetric Switched-Inductor Quasi-Z-Source CHB Multilevel Inverter 285
G. Prem Sunder, B. Shanthi, Alamelu Nachiappan, S.P. Natarajan and Padmanaban Sanjeevikumar

Buck–Boost LED Driver with Dimming Characteristics 295
R. Gunabalan, D.R. Binu Ben Jose and Padmanaban Sanjeevikumar

S-Parameter Based Evaluation of Cable Losses for Precise Low Frequency Voltage and Current Calibration 307
Swati Kumari, Sunidhi Luthra, Jyoti Chauhan, Bijendra Pal, Saood Ahmad, Ravinder Kumar, P.S. Negi and V.N. Ojha

Buck–Boost Current Converter Using Duality Concept and Its DC Transformer Modelling 315
S.B. Mahajan, Padmanaban Sanjeevikumar, K.M. Pandav, R.M. Kulkarni and V.A. Sherke

2.4 kW Three-Phase Inverter for Aircraft Application-Hardware Implementation 325
K.M. Pandav, S.B. Mahajan, Padmanaban Sanjeevikumar, S.M. Badave and R.M. Pachagade

Control Algorithm Concept for AC Voltage Stabilizer Based on Hybrid Transformer with a Matrix Converter 337
Paweł Szcześniak, Jacek Kaniewski and Padmanaban Sanjeevikumar

Design and Analysis of Ultra-Low Power QCA Parity Generator Circuit 347
Trailokya Nath Sasamal, Ashutosh Kumar Singh and Umesh Ghanekar

Modeling of the State Space Vector PWM (SVPWM) Based STATCOM for Voltage Improvement in the Transmission Line 355
Rubi Kumari and Chitrangada Roy

Common-Mode Voltage Regulation of Three-Phase SVPWM-Based three-Level NPC Inverter 367
Subramaniam Umashankar, Vishnu Kalaiselvan Arun Shankar, Padmanaban Sanjeevikumar and K. Harini

Survey of Power Quality Discrete Disturbances in an Educational Institution 377
Subramaniam Umashankar, Vishnu Kalaiselvan Arun Shankar, Shanmugam Paramasivam, Padmanaban Sanjeevikumar and K. Anil Kumar

Study of AGC in Two-Area Hydro-thermal Power System 393
Bibhu Prasad Ganthia, Anita Pritam, Krishna Rout, Siddhartha Singhsamant and Jayashree Nayak

Wavelet Technique-Based Fault Classification in Transmission Lines 403
Avagaddi Prasad and J. Belwin Edward

Comparative Analysis of Feed-Forward and Synchronous Reference Frame Control-Based Dynamic Voltage Restorer 411
A. Rini Ann Jerin, K. Palanisamy, S. Umashankar and Padmanaban Sanjeevikumar

Performance Comparison of Two Real-Time Power System Frequency Estimation Methods 421
R.B. Sharma, G.M. Dhole and M.B. Tasare

Brushless DC Electric Motor Speed Control and Power Factor Correction Using Single-Ended Primary Inductor Converter 431
Shaw Bikash, Sengupta Anwesha, S.B. Mahajan, Padmanaban Sanjeevikumar and Shaikh Aamer

Naturally Clamped, Isolated, High-Gain DC–DC Converter with Voltage Doubler for Battery Charging of EVs and PHEVs 439
Abhinav Bhattacharjee, Sangit Saha, D. Elangovan and G. Arunkumar

An Energy-Efficient and Reliable Depth-Based Routing Protocol for Underwater Wireless Sensor Network (ER-DBR) 451
S. Neelavathy Pari, M. Sathish and K. Arumugam

Adaptive PI Control of STATCOM for Stability Improvement of Power System 465
Rubi Kumari and Chitrangada Roy

Defect Detection in Power Electronic Circuits by Artificial Neural Network Using Discrete Wavelet Analysis 477
Dibyendu Khan, Sankhadip Saha, Shiladitya Saha and Subhrodipto Basu Choudhury

Stability of Two-Dimensional Systems Using Single Square Matrix 487
P. Ramesh and K. Vasudevan

Multidimensional Linear Discrete System Stability Analysis Using Single Square Matrix 499
P. Ramesh and K. Vasudevan

Detection of Static Air-Gap Eccentricity in Three-Phase Squirrel Cage Induction Motor Through Stator Current and Vibration Analysis 511
S. Bindu and Vinod V. Thomas

Analysis of Three Phase Inverter Using Different PWM Techniques . . . 519
Ayesha Firdous, Mohammed Imran and Mahboob Shaik

A State-of-the-Art Review on Synchrophasor Applications to Power Network Protection 531
M.S. Prabhu and Paresh Kumar Nayak

Performance Analysis of Current-Mode Interconnect System in Presence of Process, Voltage, and Temperature Variations 543
Yash Agrawal, Rutu Parekh and Rajeevan Chandel

LMP Difference Approach for Management of Transmission Congestion 553
Divya Asija, K.M. Soni, S.K. Sinha and Vinod Kumar Yadav

Optimal Allocation of DG in the Radial Distribution Network Using Bat Optimization Algorithm 563
T. Yuvaraj, K.R. Devabalaji and K. Ravi

Smart Controlling of Appliances in Power-Line Communication Using LabVIEW 571
Deepthi P. Kulkarni, H.B. Bhuvaneswari and B. Kalyan Ram

Modelling and Analytical Study of Linear Induction Motor and Its Air Gap Flux Measurement at Different Slip 585
Prasenjit D. Wakode, Mohd Tariq, T.K. Bhattacharya and C. Bharatiraja

Model Predictive Current Control of Single-Phase 13-Level Transistor-Clamped H-Bridge Based Cascaded Multilevel Inverter 597
K. Rameshkumar, V. Indragandhi, Geetha Mani and Padmanaban Sanjeevikumar

3-to-8 Decoder Implementation Using Single Electron Threshold Logic (SE-TL) for Low Power Computing 609
Arpita Ghosh and S.K. Sarkar

Parallel Investigation of Different Task Schedulers at Greencloud for Energy Consumption in Datacenters 617
S. Aarthee and R. Prabakaran

Distributed Energy Generation—Is It the Way of the Future? 627
Mujahid Tabassum, Saad Bin Abul Kashem and Kuruvilla Mathew

Impact of Distance on the Harmonic Active Power and Energy Metering at the Load 637
K.S.V. Phani Kumar and S. Venkateshwarlu

Generation System Reliability Assessment Incorporating Photovoltaic Energy 647
K. Shivarama Krishna and K. Sathish Kumar

Design Study for a 5 GW Base Load Power Drawn from Satellite Solar Power Station 655
Deepak Kumar and Kalpana Chaudhary

Reduction of Fault Detection Time by Using Fast S-Transform (FST) 665
P. Mahalakshmi, Ritwik Dhawan, Archit Srivastava and A. Sharmila

Low-Voltage Low-Power FGMOS-Based Current Conveyor III 673
Charu Rana, Neelofer Afzal, Dinesh Prasad and Anu

Single-Precision Floating Point Matrix Multiplier Using Low-Power Arithmetic Circuits 683
Soumya Gargave, Yash Agrawal and Rutu Parekh

Monitoring Real and Reactive Power in a Transmission Network Using Generalized Unified Power Flow Controller 693
Raja Reddy Duvvuru, B. Venkata Prasanth and V. Ganesh

Improvement of Power System Security Under Single Line Critical Contingency Condition by Optimal Placement of Multiple TCSCs 701
Pallavi Choudekar, Sanjay Sinha and Anwar Siddiqui

DXCCII-Based First Order Voltage-Mode All-Pass Filter 709
Ashok Kumar, Ajay Kumar Kushwaha and Sajal K. Paul

Performance Analysis of High Power Brushless DC Motor Drive 719
R. Babu Ashok and B. Mahesh Kumar

Design and Fabrication of Scale-Down Model of 620 MVA, 275 kV Transmission Line 729
Akash Deep Mukhia, Anwesh Gautam, Suyog Pradhan and Sandip Kumar Gupta

About the Editors

Prof. (Dr.) Amik Garg received his B.E. (Mechanical) in 1986 from Delhi College of Engineering (DCE) (now known as Delhi Technological University), M.Tech. in Industrial Tribology and Maintenance Engineering from Indian Institute of Technology Delhi (IIT Delhi) in 1996 and subsequently completed his Ph.D. in the area of multi-echelon repair inventory systems from the Department of Mechanical Engineering, IIT Delhi in 2010. He is currently the Director of Sikkim Manipal Institute of Technology (SMIT), Sikkim. He has the practical experience of serving the defence industry as maintenance engineer at various levels of over thirty years and has vast exposure in the field of supply chain management, performance measurements, maintenance management, industrial engineering, etc.

Akash Kumar Bhoi has completed his B.Tech. (Biomedical Engineering) from the Trident Academy of Technology (TAT), Bhubaneswar and M.Tech. (Biomedical Instrumentation) from Karunya University, Coimbatore in the years 2009 and 2011, respectively. He is pursuing his Ph.D. (Biomedical Signal Processing) from Sikkim Manipal University, India. He is currently working as a research and development (R&D) Faculty Associate in the R&D Section of Sikkim Manipal Institute of Technology (SMIT) and Assistant Professor in the Department of Electrical and Electronics Engineering (EEE), Sikkim Manipal Institute of Technology (SMIT). He has published book chapters and several papers in national and international journals and conferences.

Dr. Padmanaban Sanjeevikumar received his B.E. (Electrical and Electronics), M.Tech. (Electrical Drives and Control), and Ph.D. degrees, respectively, from Madras University, Pondicherry University, India, and Alma Mater Studiorum 1088AD, University of Bologna, Italy in 2002, 2006, and 2012. He pursued his doctoral degree with full comprehensive grant successfully obtained from the Ministry of University Research (MIUR), from the government of Italy (January 2009–December 2011). Professor Sanjeevikumar's biography is listed along with the list of professional achievers' biographies @ MarquisWho'sWho, United States of America (33rd Edition, 2016).

Prof. K.K. Kamani received his B.Sc. and M.Sc. degrees in Physics from the Karnatak University Dharwar in 1987 and 1989. With a Bachelor of Education (B. Ed.) degree in 1992 he joined the service in 1989 as a lecturer and served for 20 years in various institutions of the Karnataka Government. Currently he is working as Professor in the Physics postgraduate Department, NAAC Reaccredited A grade Government Science College Chitradurga, Government of Karnataka. He received the FESE in 2008. He is presently working as a Global Economic Advisor, Asia-Pacific CEO Association (APCEO) Senior Expert authorized by the Asia-Pacific CEO Association [Worldwide].

Non-isolated Sextuple Output Hybrid Triad Converter Configurations for High Step-Up Renewable Energy Applications

Padmanaban Sanjeevikumar, Mahajan Sagar Bhaskar, Pranav Dhond, Frede Blaabjerg and Michael Pecht

Abstract This article presents a new non-isolated DC-DC sextuple output hybrid triad converter configurations for high step-up renewable energy applications. Total 8 (eight) converters configurations are obtained by combining SEPIC/SI-SEPIC, Cuk/SI-Cuk, and Boost/SI-Boost which is highly suitable for step-up renewable applications where DC-DC multi-output converters/choppers are needed; such as a solar multilevel DC-AC converter (MLI), HVDC, hybrid/electric and electric vehicles. The most important characteristics of the proposed converter configurations are (i) only one power control semiconductor switch, (ii) offer six different DC outputs with different conversion ratio, (iii) non-isolated (without transformers) Converter topologies, (iv) high voltage at the output side without using large duty cycle and (v) modular DC-DC converter structure. The simulation results are presented and it validates the practicability, functionality, and the idea of suggested sextuple output hybrid triad converter configuration.

P. Sanjeevikumar (✉)
Department of Electrical and Electronics Engineering, University of South Africa, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

P. Sanjeevikumar
Research and Development (R & D), Ohm Technologies, Chennai, India

M.S. Bhaskar · P. Dhond
Department of Electrical and Electronics (EE) Engineeering, Marathwada Institute of Technology (MIT), Aurangabad, India
e-mail: sagar25.mahajan@gmail.com

P. Dhond
e-mail: dhondpranav11@gmail.com

F. Blaabjerg
Center for Reliable Power Electronics (CORPE), Department of Energy Technology, Aalborg University, Aalborg, Denmark
e-mail: fbl@et.aau.dk

M. Pecht
Center for Advanced Life Cycle Engineering (CALCE), University of Maryland, College Park, MD, USA
e-mail: pecht@umd.edu

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_1

Keywords Sextuple output · Triad converter configurations · Non-isolated Single control switch · High step-up · Renewable applications

1 Introduction

In recent years, development of low-cost multiport DC-DC power converter attracted much attention for renewable energy application due to its capability of interfacing with diverse sources, battery systems, and loads with different voltage levels [1, 2]. In renewable energy conversion equipment production, DC-DC power converters represent the largest percentage and are becoming the most important sector of power electronics. The market of DC-DC converters comprise three sub-fragments (i) low-power DC-DC converter, (ii) medium-power converter and (iii) high-power converter [3, 4]. Most of the renewable energy application such as solar multilevel DC-AC converter, HVDC, hybrid/electric and electric vehicles requires multiple DC outputs at different voltage levels [4–17]. Multiport DC-DC converters are a breed of DC-DC converters and are classified into three major categories: (i) SIMO (Single-Input Multiple-Output) [8–12], (ii) MIMO (Multiple-Input-Multiple-Output) [13–15] and (iii) MISO (multiple-input single-output) [18–20]. To design multi-output to a different output voltage level, several techniques are adopted and developed by using DC-DC isolated (using transformer) converter/choppers configurations such as Forward Converter, Flyback Converter, Push–Pull Converter/chopper, DC-DC Half Bridge, and Full Bridge converter as well as non-isolated (without transformer) DC-DC converter [8–20]. In flyback and forward converter, only one transformer primary (Input Side) winding is used, other than in order to obtain multiple outputs separate secondary windings are employed. This input side (Primary) winding reduces count of the reactive element in the converter/chopper whereas several secondary winding raise the size, cost, circuit complexity, and weight of the converter. Non-isolated converters are one of the cost-effective and viable solutions to overcome the drawback of the flyback and forward converter. In [8–12], SIMO converter is proposed by using numerous power controller and semiconductor power devices, thus raises the system cost and complexity. In [23] a new family of Switched DC-DC resonant converter/chopper had been proposed in which resonance tank is periodically supplied from the power supply and sequentially releases the energy into the output. But, continuous regulation of load is difficult because discrete manner of load power. In [7, 24] Single-Inductor Multi-Output voltage sharing DC-DC power converters for transformerless grid connection systems are proposed. These converter configurations are suitable for renewable energy applications, but require several control switches which increases the number of gate driver, cost and losses in the converter. In this article new non-isolated sextupling output hybrid triad converter configurations are proposed to overcome the above-mentioned drawbacks of recent proposed converters. Figure 1a–j shows (a) traditional Boost (Non-inverting step-up converter with single inductor), (b) SI-Boost (switched inductor boost converter) [25],

(c) traditional SEPIC (Single-Ended Primary-Inductor Converter), (d) SI-SEPIC-I (Single-Ended Primary-Inductor Converter with switched inductor at input side), (e) SI-SEPIC-II (Single-Ended Primary-Inductor Converter with switched inductor at output side), (f) SI-SEPIC-III (Single-Ended Primary-Inductor Converter with switched inductor at input and output side) [26], (g) traditional Cuk (Inverting output DC-DC converter derived from the combination of boost and buck converter), (h) SI-Cuk-I (Cuk converter with switched inductor at input side), (i) SI-Cuk-II (Cuk converter with switched inductor at output side), (j) SI-Cuk-III (Cuk converter with switched inductor at input and output side).

Table 1 shows the conversion ratio, voltage across switch in off mode and output type of converter mentioned in Fig. 1. To achieve high gain, several recent converters with minimum switch voltage stress are proposed [27–33]. In this article total 8 (eight) converters configurations are obtained from combining SEPIC/SI-SEPIC, Cuk/SI-Cuk and Boost/SI-Boost which are highly suitable for step-up renewable applications where sextuple output DC-DC converters are needed, such as a solar multilevel DC-AC Converter (MLI), HVDC, hybrid/electric and electric vehicles.

The most important characteristics of the proposed converter configurations are (i) only one power control semiconductor switch, (ii) sextuple output: Provide six different outputs with different conversion ratio, (iii) Non-isolated topologies (no use of transformer and coupled inductor), (iv) High voltage at the output side without using large duty cycle and (v) modular DC-DC converter structure.

The proposed sextuple converters configurations are described in the next section. Simulation results are presented in Sect. 2.2 and it validates the practicability, functionality of suggested sextuple output hybrid triad converter configuration.

2 Sextuple Output Hybrid Triad Converter Configurations

In Fig. 1a–j shows the various configurations of Boost, SEPIC and Cuk converters. It is observed that the converters depicted in Fig. 1a, c, e, g, i and in Fig. 1b, d, f, h, j have an identical front-end structure. The front-end structure consists of supply voltage, reactive circuit, and single switch. This allows us to combine front-end structure of three converters (triad configuration) to derive new configurations for sextuple output, therefore obtains new 8 (eight) topologies which are highly suitable for step-up renewable applications.

Figure 2 shows the generalized structure of sextuple output triad converter configurations. The other main features of the new proposed configurations are (i) simple structure since converters are designed with only one control power switch and allows to connect a sextuple load to the converter. (ii) Single driver circuit and switch also simplifies the control strategies for proposed converter.

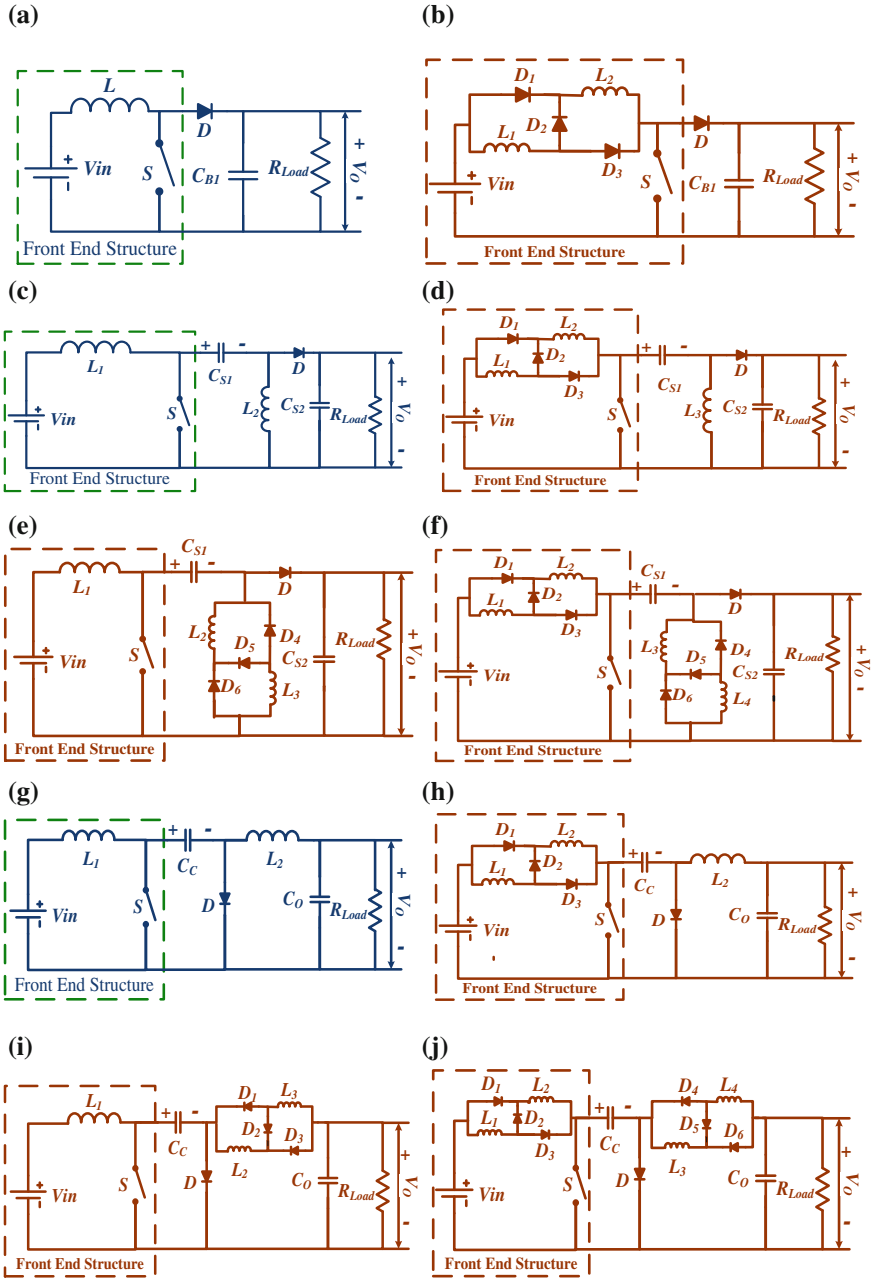


Fig. 1 **a** Traditional boost. **b** SI-Boost. **c** Traditional SEPIC, **d** SI-SEPIC-I (SI-SE). **e** SI-SEPIC-II (SISE). **f** SI-SEPIC-III (SI-SISE), **g** Traditional Cuk, **h** SI-Cuk-I (SI-CU), **i** SI-Cuk-II (SICU). **j** SI-Cuk-III (SI-SICU)

Table 1 Conversion ratio, voltage across switch in off state and output type of converters depicted in Fig. 1

Type of converter	Voltage conversion ratio	Switch voltage (OFF state)	Output type
Traditional boost	$1/(1-D)$	$V_{in}/(1-D)$	Non inverting boost
SI-Boost	$(1+D)/(1-D)$	$(1+D)V_{in}/(1-D)$	Non inverting boost
Traditional SEPIC	$D/(1-D)$	$V_{in}/(1-D)$	Non inverting buck or boost
SI-SEPIC-I	$(D+D^2)/(1-D)$	$V_{in}(1+D)/(1-D)$	Non inverting buck or boost
SI-SEPIC-II	$2D/1-D^2$	$V_{in}/(1-D)$	Non inverting buck or boost
SI-SEPIC-III	$2D/(1-D)$	$V_{in}(1+D)/(1-D)$	Non inverting buck or boost
Traditional Cuk	$-D/(1-D)$	$V_{in}/(1-D)$	Inverting buck or boost
SI-Cuk-I	$-(D+D^2)/(1-D)$	$(1+D)V_{in}/(1-D)$	Inverting buck or boost
SI-Cuk-II	$-2D/1-D^2$	$V_{in}/(1-D)$	Inverting buck or boost
SI-Cuk-III	$-2D/(1-D)$	$(1+D)V_{in}/(1-D)$	Inverting buck or boost

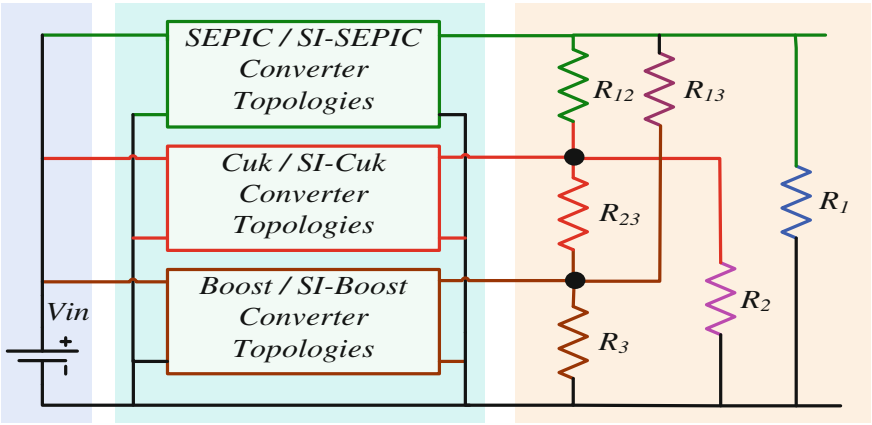


Fig. 2 Generalized structure of sextuple output triad converter configuration

(iii) High efficiency and reduced size, since the high-frequency transformer is not required to design proposed converter.

Total 8 (eight) sextuple output triad converter structure are derived by combining identical front-end structure of converters as mentioned in Fig. 1.

Figure 3 shows the various sextuple output triad converters configurations. Figure 3a–d configurations have identical front end structure with single inductor at the input side. Figure 3e–h configurations have an identical front structure with

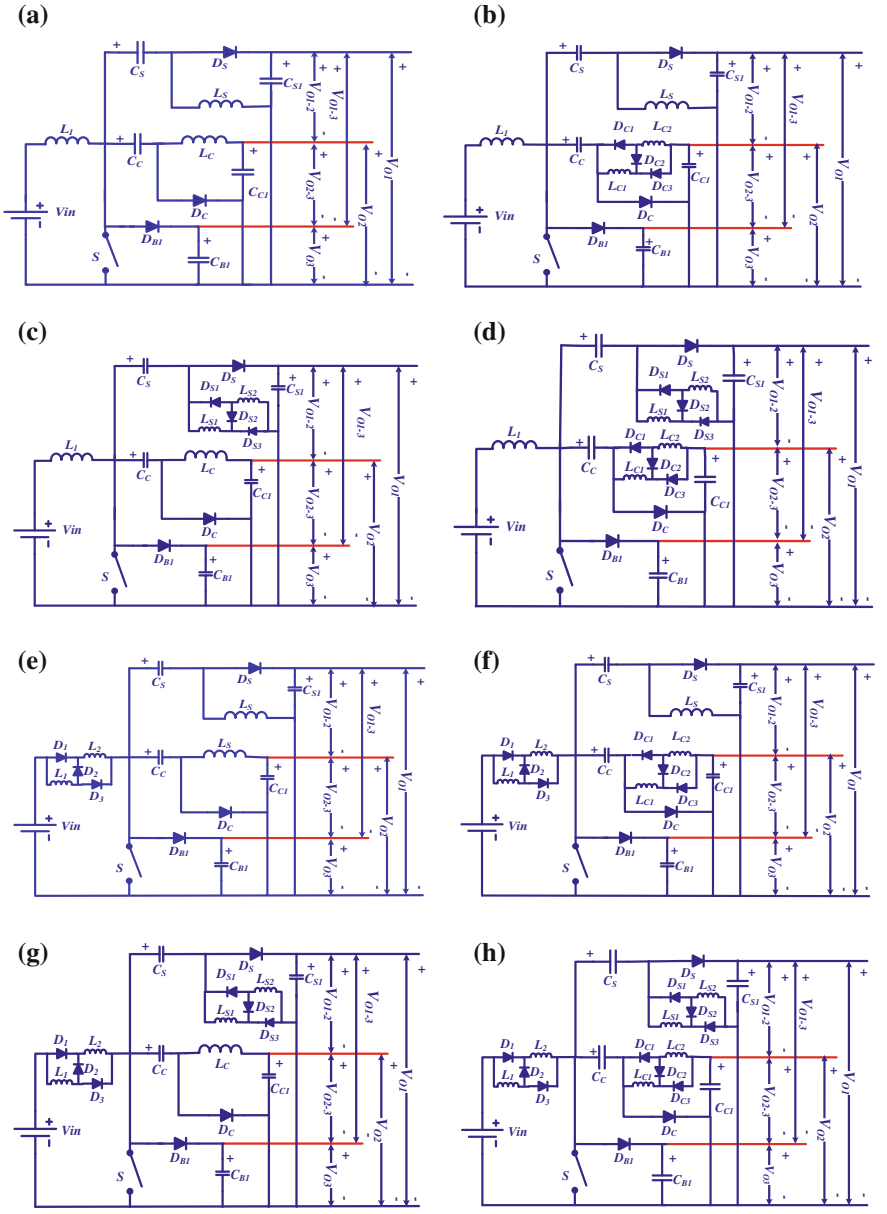


Fig. 3 Sextuple output triad converter configurations. **a** SE-CU-BO converter. **b** SE-SICU-BO converter. **c** SISE-CU-BO converter. **d** SISE-SICU-BO converter. **e** SI-SE-CU-BO converter. **f** SI-SE-SICU-BO converter. **g** SI-SISE-CU-BO converter. **h** SI- SISE-SICU-BO converter

switch inductor at the input side. All the sextuple proposed converters are continuous input current type converters. The voltage gain (Conversion Ratio) of all the presented converters configurations are analyzed for sextuple load and are given in Table 2. To explain the mode of operation the proposed converter configurations, SI-SISE-SICU-BO converter operation modes are discussed in detail in Sect. 2.1.

2.1 SI-SISE-SICU-BO Converter (Switched Inductor SISE-SICU-BO Converter)

Figure 2h shows the power circuit of switched inductor SISE-SICU-BO converter (SI-SISE-SICU-BO Converter). It is designed by combining SI-SISE (switched Inductor SISE), SI-SICU (switched Inductor SICU) and SIBO (switched inductor boost) converters. The operation of SI-SISE-SICU-BO is divided into two separate modes: one when power switch is ON and other when power switch is OFF. When the control switch is ON, the energy fed by the input supply is stored in inductor L_1 and L_2; inductors L_{C1}, L_{C2} (output side inductors of Cuk converter) and L_{S1}, L_{S2} (output side inductors of SEPIC) also stores energy due to the discharge of C_C and C_S. Throughout this interval, the power diodes D_2, D_{B1}, D_C, D_S, D_{C2}, and D_{S2} are not conducting and the output capacitor (C_{B1}, C_{C1}, and C_{S1}) provides the supply energy to sextuple loads. Figure 4 shows the equivalent circuit of SI-SISE-SICU-BO converter in ON state. When the control switch is OFF, all the capacitors are recharged by inductors through freewheeling diodes and also provides supply to sextuple load with different output voltage. During the OFF state, power diode D_1, D_3, D_{C1}, D_{C3}, D_{S1}, and D_{S3} are not conducting. Figure 4 shows the equivalent circuit of SI-SISE-SICU-BO converter in OFF state.

2.2 Simulation Results of SI-SISE-SICU-BO Converter

Sextuple SI-SISE-SICU-BO triad converter configuration (see Fig. 3h) is simulated in MATLAB with 24 V input supply, 150 W input power and 0.60 Turn ON Time (duty ratio) and switching frequency 50 kHz provided to switch. Figure 5a–b shows the sextuple output voltage waveforms of SI-SISE-SICU-BO converter. It is observed that the SEPIC and Cuk structure of the proposed SI-SISE-SICU-BO converter provides positive and negative output voltage (V_{01} = 72 V and V_{02} = −72 V) respectively. Boost structure of the proposed converter provides voltage V_{03} = 96 V. It is also observed that the voltage across load connected between Cuk and Boost structure (V_{02-3}) is −168 V. The voltage across load connected between SEPIC and Cuk Structure (V_{01-2}) is 144. The DC voltage across load connected between SEPIC and Boost structure (V_{01-3}) is −24 V. The voltage across power semiconductor switch is shown in Fig. 6a. It is investigated that the

Table 2 Conversion ratio of proposed triad converter configuration for sextuple load

Sextuple converter	Voltage conversion ratio					
	V_{01}/V_{in}	V_{02}/V_{in}	V_{03}/V_{in}	V_{01-2}/V_{in}	V_{02-3}/V_{in}	V_{01-3}/V_{in}
SE-CU-BO	$D/(1-D)$	$-D/(1-D)$	$1/(1-D)$	$2D/(1-D)$	$-(1+D)/(1-D)$	-1
SE-SICU-BO	$D/(1-D)$	$-2D/1-D^2$	$1/(1-D)$	$(3D+D^2)/(1-D^2)$	$-(1+3D)/(1-D^2)$	-1
SISE-CU-BO	$2D/1-D^2$	$-D/(1-D)$	$1/(1-D)$	$(3D+D^2)/(1-D^2)$	$-(1+D)/(1-D)$	$-1/(1+D)$
SISE-SICU-BO	$2D/1-D^2$	$-2D/1-D^2$	$1/(1-D)$	$4/(1-D^2)$	$-(1+3D)/(1-D^2)$	$-1/(1+D)$
SI-SE-CU-BO	$(D+D^{2)}/(1-D)$	$-(D+D^{2)}/(1-D)$	$(1+D)/(1-D)$	$2D(1+D)/(1-D)$	$-(1+D)^2/(1-D)$	$-(1+D)$
SI-SE-SICU-BO	$(D+D^{2)}/(1-D)$	$-2D/(1-D)$	$(1+D)/(1-D)$	$(3D+D^2)/(1-D)$	$-(1+3D)/(1-D)$	$-(1+D)$
SI-SISE-CU-BO	$2D/(1-D)$	$-(D+D^{2)}/(1-D)$	$(1+D)/(1-D)$	$(3D+D^2)/(1-D)$	$-(1+D)^{2/}(1-D)$	-1
SI-SISE-SICU-BO	$2D/(1-D)$	$-2D/(1-D)$	$(1+D)/(1-D)$	$4/(1-D^2)$	$-(1+3D)/(1-D)$	-1

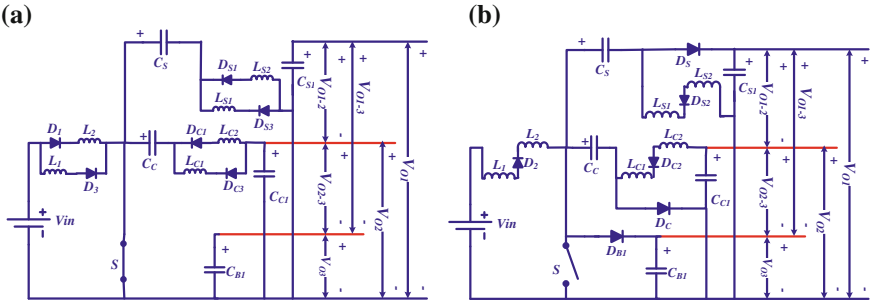


Fig. 4 Equivalent circuit of SI-SISE-SICU-BO configurations **a** ON start. **b** OFF state

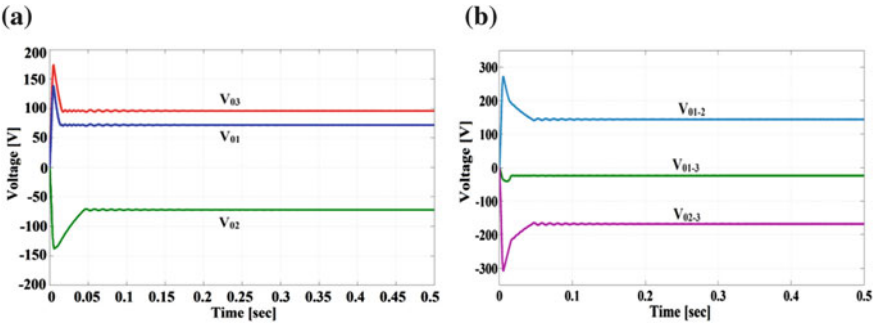


Fig. 5 Sextuple output voltage waveforms of SI-SISE-SICU-BO converter. **a** V_{01}, V_{02} and V_{03}. **b** $V_{01–2}$, $V_{02–3}$ and $V_{01–3}$

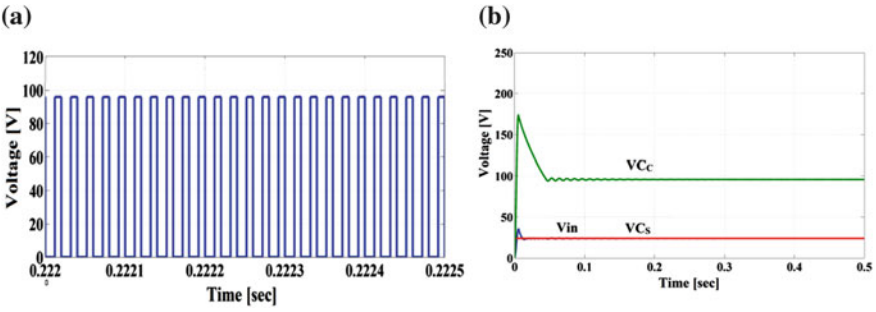


Fig. 6 Voltage waveform across **a** switch **b** intermediate capacitors (C_C and C_S)

voltage across power switch in OFF mode is equal to the output DC voltage of boost structure ($V_S = V_{03} = 96$ V). The voltage across intermediate capacitors of SEPIC (C_S) and Cuk (C_C) structure converter present in the proposed converter is shown in Fig. 6b. It is noted that the voltage of across capacitor C_C and C_S is 96 and 24 V.

3 Conclusions

A new non-isolated sextuple output triad converter hybrid configurations are presented for high step-up renewable applications. The proposed converters have a sextuple output with high conversion ratio and also suited for applications where DC-DC multi-output converters/chopper are needed; such as a solar DC-AC converter (MLI), HVDC, hybrid/electric and electric vehicles. Total 8 (eight) converters configurations are obtained by combining SEPIC/SI-SEPIC, Cuk/SI-Cuk and Boost/SI-Boost. The voltage conversion ratio of all configurations is also presented. The most important characteristics of the proposed converter configurations are (i) only one power control semiconductor switch, (ii) Sextuple output: provide six different outputs with different conversion ratio, (iii) Non-isolated topologies (no use of transformer and coupled inductor), (iv) High voltage at the output side without using large duty cycle and (v) modular DC-DC converter structure. Out of 8 configurations, SI-SISE-SICU-BO converter is the best configuration and its simulation results are presented and it validates the practicability, functionality and the idea of the suggested sextuple output hybrid triad converter configuration.

References

1. Patra, P., Patra, A., Misra, N.: A single inductor multiple output switcher with simultaneous Buck, Boost and inverter outputs. IEEE Trans. Power Electron. **27**(4), 1936–1951 (2012)
2. Wai, R.J., Jheng, K.H.: High-efficiency single-input multiple-output DC-DC converter. IEEE Trans. Power Electron. **28**(2), 886–898 (2013)
3. IHS Technology: The world market for semiconductors in AC-DC & DC-DC merchant power supplies. (2014)
4. Darnell Group: Worldwide DC-DC converter modules and ICs forecasts; application, amperage, wattage, isolation, input voltages, output voltages and converters IC trends, 11th edition (2011)
5. Ferrera, M.B., Litran, S.P., Duran, E., Andujar, J.M.: A converter for bipolar dc link based on SEPIC-Cuk combination. IEEE Trans. Power Electron. **30**(12), 6483–6487 (2015)
6. Ferrera, M.B., Litran, S.P., Duran, E., Andujar, J.M.: A SEPIC-Cuk converter combination for bipolar dc microgrid applications. In: Proceedings of the IEEE International Conference on Industrial Technology (2015)
7. Nami, A., Zare, F., Ghosh, A, Blaabjerg, F.: Multi-output DC-DC converters based on diode-clamped converts configuration: topology and control strategy. IET Power Electron. **3**(2), 197–208 (2010)
8. Dietrich, S., Strache, S., Wunderlich, R., Heinen, S.: Get the LED out: experimental validation of a capacitors-free single-inductor, multiple-output LED driver topology. IEEE Ind. Electron. Mag. **9**(2), 24–35 (2015)
9. Ma, D., Ki, W.H., Tsui, C.Y., Mok, P.K.: Single inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode. IEEE J. Solid State Circuits **38**(1), 89–100 (2003)

10. Huang, M.H., Chen, K.H.: Single-inductor multi-output (SIMO) DC-DC converter with highlighted-load efficiency and minimized cross regulation for portable devices. IEEE J. Solid-State Circuits **44**(4), 1099–1111 (2009)
11. Kwon, D., Rincon-Mora, G.A.: Single-inductor-multiple-output switching DC-DC converters. IEEE Trans. Circuits Syst. II Exp. Briefs **56**(8), 614–618 (2009)
12. Wai, R.J., Jheng, K.H.: High-efficiency single-input multiple-output DC-DC converter. IEEE Trans. Power Electron. **28**(2), 886–898 (2013)
13. Qian, Z., Abdel-Rahman, O., Al-Atrash, H., Bataresh, I.: Modeling and control of three-port DC/DC converter interface for satellite applications. IEEE Trans. Power Electron. **25**(3), 637–649 (2010)
14. Behjati, H., Davoudi, A.: A Multiple-input multiple output DC-DC converter. IEEE Trans. Ind. Appl. **49**(3), 1464–1479 (2013)
15. Tong, Y., Shan, Z., Jatskevich, J., Davoudi, A.: A non-isolated multiple-input multiple-output DC-DC converter for DC distribution of future energy efficient homes. In: Proceedings of IEEE 40th Annual Conference on Industrial Electronics Society (2014)
16. Mahajan, S.B., Sreeramula Reddy, N., Pavan Kumar, R.K.: A novel single phase advanced multilevel inverter with adjustable amplitude of voltage levels. In: IEEE International Conference on Circuit, Power and Computing Technologies (IEEE-ICCPCT), Nagarcoil (2014)
17. Mahajan, S.B., Kiran, P., Revathi, B: A novel single phase multilevel inverter with single photovoltaic source and less number of switches. In: IEEE International Conference on Devices, Circuits and Systems (IEEE-ICDCS), Coimbatore (2014)
18. Khaligh, A., Cao, J., Lee, Y.J.: A multiple-input DC-DC converter topology. IEEE Trans. Power Electron. **24**(3), 862–868 (2009)
19. Li, Y., Ruan, X., Yang, D., Liu, F., Tse, C.K.: Synthesis of multiple-input DC/DC converters. IEEE Trans. Power Electron. **25**, 2372–2385 (2010)
20. Wu, H., Xu, P., Hu, H., Zhou, Z., Xing, Y.: Multiport converters based on integration of full bridge and bidirectional DC-DC topologies for renewable generation systems. IEEE Trans. Ind. Electron. **61**(2), 856–859 (2014)
21. Kim, H.-S., Jung, J.-H., J.-W. B, Kim, H.-J.: Analysis and design of a multioutput converter using asymmetrical PWM half-bridge flyback converter employing a parallel-series transformer. IEEE Trans. Ind. Electron. **60**(8), 3115–3125 (2013)
22. Mullett, C., Cathell, F.: Improving the regulation of multi output flyback converters. In: Proceedings of IEEE APEC, pp. 1923–1926. Washington, USA (2009)
23. Jabbari, M., Farzanehfard, H.: Family of soft-switching resonant DC-DC converters. IET Power Electron. **2**(2), 113–124 (2009)
24. Boora, A.A., Zare, F., Ledwich, G., Ghosh, A.: A new DC-DC converter with multi output: topology and control strategies. EPEPEMC (2008)
25. Mahajan, S.B., Sreeramula Reddy, N., Pavan Kumar, R.K.: A novel non isolated switched inductor floating output DC-DC multilevel boost converter for fuelcell applications. In: IEEE Students' Conference on Electrical, Electronics and Computer Sciences (IEEE-SCEECS), Bhopal (2014)
26. Mahajan S.B., Rishi, K., Anita, K., Pooja, C.: Non isolated switched inductor SEPIC converter topologies for photovoltaic boost applications. In: IEEE International Conference on Circuit, Power and Computing Technologies (IEEE-ICCPCT), Nagarcoil (2016)
27. Mahajan, S.B., Rishi, K., Sanjeevikumar, P., Siano, P., Blaabjerg, F.: Hybrid non-isolated and non inverting Nx interleaved DC-DC multilevel boost converter for renewable energy applications. In: The 16th IEEE International Conference on Environment and Electrical Engineering, (IEEE-EEEIC'16), Florence, Italy (2016)
28. Mahajan, S.B., Rishi, K., Sanjeevikumar, P., Blaabjerg, F., Viliam, F., Mihai, C.: Non isolated and non-inverting cockcroft walton multiplier based hybrid 2Nx interleaved boost converter for renewable energy applications. In: IEEE Conference on 17th the Power Electronics and Motion Control, (IEEE-PEMC'16), Europe (2016)

29. Sanjeevikumar, P., Kabalci, E., Iqbal, A., Abu-Rub, H., Ojo, O.: Control strategy and hardware implementation for DC-DC boost power conversion based on proportional-integral compensator for high voltage application. Engg. Sci. Tech. Intl. J. (JESTECH). Elsevier J. **18** (2), 163–170 25 (2014)
30. Sanjeevikumar, P., Iqbal, A., Abu-Rub, H.: Implementation and control of extra high voltage DC-DC boost converter. In: The 7th IET International Conference on Sustainable Energy and Intelligent System, IET-SEISCON '14, Chennai (India) (2013)
31. Mahajan, S.B., Sanjeevikumar, P., Ojo, O., Rivera, M., Kulkarani, R.: Non-isolated and inverting Nx multilevel boost converter for photovoltaic DC link applications. IEEE ICA/ACCA, Chile (2016)
32. Mahajan, S.B., Sanjeevikumar, P., Blaabjerg, F., Ojo, O., Seshagiri, S., Kulkarni, R.: Inverting Nx and 2Nx non-isolated multilevel boost converter for renewable energy applications. 4th IET, CEAT, Kuala Lumpur, Malaysia (2016)
33. Mahajan, S.B., Sanjeevikumar, P., Wheeler, P., Blaabjerg, F., Rivera, M., Kulkarni, R.: XY converter family: a new breed of buck boost converter for high step-up renewable energy applications. In: IEEE-ICA/ACCA, Chile (2016)

Dual-Band Wearable Rectenna for Low-Power RF Energy Harvesting

B. Naresh, Vinod Kumar Singh, V. Bhargavi, Amik Garg and Akash Kumar Bhoi

Abstract In this paper, a dual-band textile rectenna is fabricated and tested to power the wireless and wearable sensor systems at 2.45 and 5.8 GHz. The wearable rectenna substrate is designed with a textile material and conductive element is a copper tap. Fabricated antenna has a size of 50 × 50 mm^2 and it is effortlessly bent on human body. The rectenna element is also fabricated on the same textile material and RF to DC conversation is investigated for power levels −20 to 15 dBm. The wearable antenna has experimentally measured impedance bandwidth of 40% for primary band and 51% for second band. The rectenna has maximum efficiency of 60% at −3 dBm (5.8 GHz) and 0 dBm (2.45 GHz).

Keywords Dual band · Rectenna · RF to DC · Wearable antenna
Wireless sensor system

B. Naresh
Department of Electrical Engineering, Bhagwant University, Ajmer, Rajasthan, India
e-mail: nareshbangari@gmail.com

V.K. Singh (✉)
Department of Electrical Engineering, SR Group of Institutions, Jhansi, UP, India
e-mail: singhvinod34@gmail.com

V. Bhargavi
Government of India, Jhansi, UP, India
e-mail: bhargavivanga1990@gmail.com

A. Garg
Department of EEE, Research & Development Section, Sikkim Manipal Institute of Technology, Sikkim Manipal University, Rangpo, India
e-mail: amikkgarg@gmail.com

A.K. Bhoi
Research & Development Section, Sikkim Manipal Institute of Technology, Sikkim Manipal University, Rangpo, India
e-mail: akash730@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_2

1 Introduction

Solid dielectric substrate antennas are more common in use, they made with a printed copper on a dielectric substrate such as FR4 for low gain antennas, Duroid, Benzocyclo butane, Roger 4350, FR4-epoxy, Bakelite [1, 2]. These days researcher brings in new kind of dielectric materials are called textile materials. A coaxial feed textile antenna with wash cotton, curtain cotton, and jean cotton substrate materials are investigated in [3] with the help of HSFF software. E-shaped antenna with fleece fabric as a substrate is designed and manufactured for 2.25–2.75 GHz band in [4]. The main advantages of textile material are light in weight, easily foldable, and the most important one is it is wearable. The proposed textile antenna is designed with jeans as dielectric substrate and the radiating patch is designed with a copper tap. The development of textile-based antennas introduces a new type of communication system that is body-centric wireless communication [5, 6]. In this technology sensors or monitoring electronic devices are integrated into the clothing. Wearable antenna for military applications and the performance of the wearable antenna on the human body is presented in [7]. How this wearable antenna can improve the safety of the firefighters is introduce in [8]. A short range personal area network and body wireless communication design based on the textile antenna is in [9]. The power required to drive the electronic devices is supplied by a battery or a super capacitor. While using battery system as a power source there are some problems like recharging and also it required maintenance. So to overcome the problem energy harvesting is the best alternative.

Semiconductor design technology is at freezing pace in the twenty-first century. Consequently, devices are miniaturized; power levels have come down to micro- and nanowatts. So that energy harvesting from the surrounding environment is an active research area. Radio frequency (RF) is one of such energy harvesting method from the ambient. Harvested energy is used to drive the micropower devices which are integrated into the wearable system. RF harvesting mainly requires an antenna which receives RF energy and the rectifier which converts RF energy into DC voltage. Rectifying antenna for low-power applications at 2.45 GHz and rectenna circuit topologies for different power levels are also explained in [10]. The author in [11] fabricated the multi-energy harvesting system which scavenged through solar, RF, heat energy sources.

In this paper ultrawide dual-band textile antenna is designed and fabricated, the jeans cotton fabric is used to design textile antenna [12–15]. RF to DC rectification is investigated at 2.45 and 5.80 GHz; the rectifier circuit is intended for low power level ($E < 2$ V).

2 Antenna Configuration

The dielectric material has an important role in microstrip antenna when it comes to wearable antenna it must be flexible and lightweight so that the substrate material chosen is a cotton jeans. Textile antenna conducting path is designed by a foil tap of

Table 1 Antenna specification used in CST microwave studio

S. No.	Parameter	Value
1	Dielectric permittivity (ε_r)	1.7
2	Loss tangent	0.025
3	Textile thickness (mm)	1.0
4	Textile dimension (mm)	50 × 50
5	Partial ground plane (mm)	46 × 16
6	Circle 1 radius	8.0
7	Circle 2 radius	6.4
8	Microstrip feed line	20 × 4

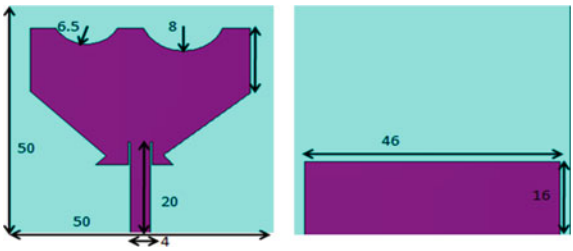


Fig. 1 Geometry of a compact circularly polarized rectangular microstrip antenna with a pair of truncated corners (all dimension in mm)

copper. The properties of the textile material are determined by conduction experiment and are reported in Table 1. Patch antenna patch dimensions are calculated by using Eqs. (1) and (2). The most significant future of the wearable antenna is, they can integrate into clothing to drive the smart electronic devices or the sensors. Before fabrication, the textile antenna was simulated in CST microwave studio 2010 environment. The designed antenna snapshot is depicted in Fig. 1 with front and back view.

$$W = \frac{C}{2f_0\sqrt{\frac{\varepsilon_r+1}{2}}};\ \varepsilon_{\text{reff}} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left(\frac{1}{\sqrt{1+12\left(\frac{h}{w}\right)}}\right) \tag{1}$$

$$L = \frac{C}{2f_0\sqrt{\varepsilon_{\text{reff}}}} - 0.824h\left(\frac{(\varepsilon_{\text{reff}}+0.3)\left(\frac{W}{h}+0.264\right)}{(\varepsilon_{\text{reff}}-0.258)\left(\frac{W}{h}+0.8\right)}\right). \tag{2}$$

3 Rectenna Design

The rectifying circuit design is initiated with a second-order low-pass filter which takes the form of impedance matching in between the textile antenna and diode. Matching is essential while working with low power levels; else harvesting efficiency will reduce by reflected power. The Schottky diode used in the RF to DC

Table 2 HSMS-285x PSPICE parameters

S. No.	Parameter	Units	HSMS-285x
1	B_V	V	3.8
2	C_{J0}	pF	0.18
3	E_G	eV	0.69
4	I_{BV}	A	3 E^{-4}
5	I_S	A	3 E^{-6}
6	N		1.06
7	R_s	Ω	25
8	$P_B(V_J)$	V	0.35
9	P_T (XTI)		2
10	M		0.5

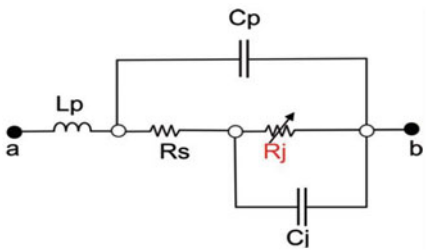


Fig. 2 Equivalent diode model with Spice parameters

conversion is HSMS2850 with a low threshold voltage of 150 mV [12]. The input impedance of the diode is a dynamic variable dependent on input RF power, in order to understand that diode performance a mathematical model of the diode undergoes detail analysis with spice parameters given in Table 2.

The diode input impedance is calculated from the zero-biased equivalent circuit of the diode as shown in Fig. 2, where L_p is the parasitic inductance, C_p—parasitic capacitance, and R_s series parasitic resistance. Junction capacitance C_j and R_j junction resistance, the junction resistance is a function of the applied bias current given by Eqs. (3) and (4). I_T is the sum of the diode saturation current (I_S) and diode bias current (I_B). The input impedance between terminals a and b in Fig. 2 is calculated for dual-band operating frequencies. The input impedance at 2.45 and 5.8 GHz are 219.4 and 41 Ω respectively.

$$R_J = \left(\frac{0.026}{I_T}\right) \tag{3}$$

$$I_T = I_B + I_S \tag{4}$$

LC filter elements are calculated separately for dual-band frequencies. While using this rectenna circuits for sensor applications, ripples in the output may cause failure or malfunction of the circuit because they are the most sensitive devices. Pass the smooth DC current to load after the rectification filters are necessary, they

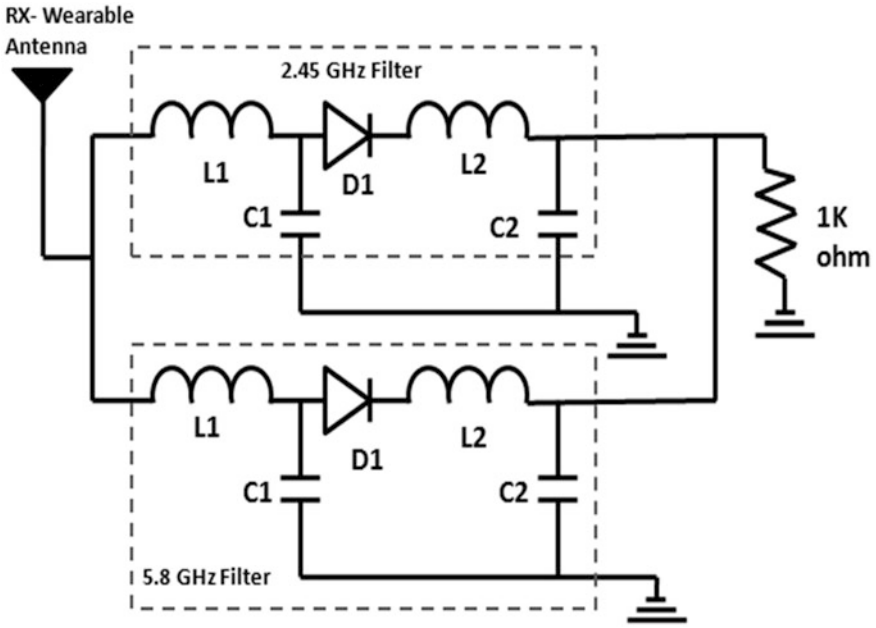


Fig. 3 Electrical circuit of rectenna

eliminate the ripples in the rectified direct current or voltage. The proposed rectenna has the output filter is a LC filter, aimed to diminish the AC frequency components. The proposed low-power rectenna electrical circuit is shown in Fig. 3. The circuit elements for 2.45 GHz are L_1 = 1.42 nH, C_1 = 2.1 pF, L_2 = 4 nH, and C_2 = 45 pF. The circuit elements for 5.8 GHz are L_1 = 1.54 nH, C_1 = 0.27 pF, L_2 = 1.06 nH, and C_2 = 45 pF.

4 Results and Discussions

The proposed antenna measurement is done in an anechoic chamber to find the parameters of the antenna in both bent and unbent conditions using vector analyzer (Agilent E5071C ENA). Figure 4 presents the comparative return loss measured in bent and flat condition along with simulated return loss of the antenna. Measured dual-bandwidths are 2.2–3.30 GHz (40%) and 4.0–6.73 GHz (51%). The primary band resonance frequency is 2.45 GHz with return loss magnitude of −17 and −21 dB is the return loss magnitude at 5.8 GHz. When antenna bent the bandwidths are reduced by a small amount due to fabrication tolerance and drapability of the textile material. In the bent condition, the resonance frequencies along with magnitudes are shifted. Resonance frequencies are shifted to words the lower frequency side in both the bands.

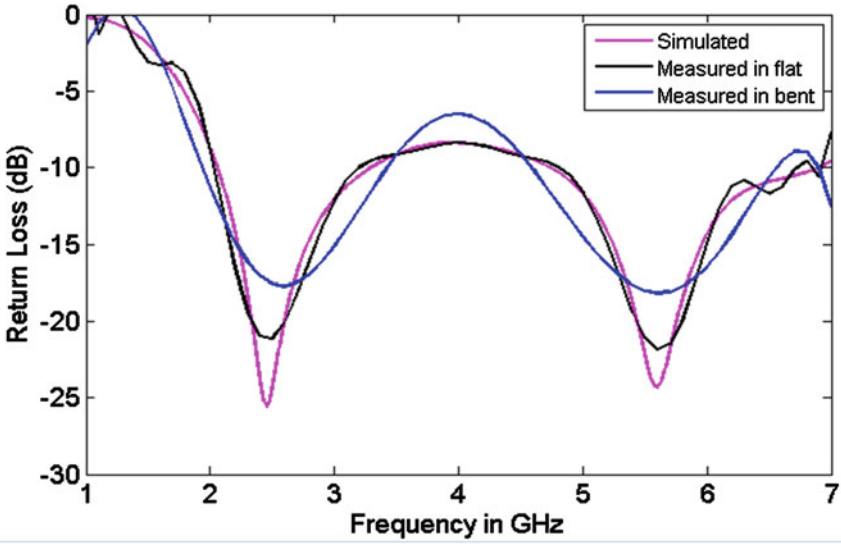


Fig. 4 Comparative return loss of the proposed antenna

The distance (D_r) between the transmitting horn antenna with the gain of G_{tX} = 11 dBi and the rectenna is 1 m. The Friis transmission Eq. (5) is used to find out the micro power available at rectenna terminals.

$$P_{rX} = P_{tX} G_{tX} G_{rX} \left(\frac{C}{4\pi D_r f_0} \right)^2, \tag{5}$$

where P_{tX} is the transmitting power at a given field strength E (mV/m); G_{rX} is the receiving antenna gain (3.5 dBi).

The constant C and f_0 are the velocity of light and frequency of the microwave. The output DC voltage (V_{outDC}) and overall efficiency (η_{EH}) of the rectenna against power density are calculated by Eq. (6).

$$\eta_{EH} = \frac{P_{outDC}}{P_{rX}} = \frac{V_{outDC}^2 / R_L}{P_{rX}} \tag{6}$$

Finally the simulated and measured overall efficiency of the rectenna is depicted in Fig. 5a, b. The measured maximum efficiency for flat rectenna is 60% is obtained at −3 dBm input power for a load of 1 kΩ at 5.8 GHz. The measured RF to DC conversion at 2.45 GHz is 54%. The rectenna efficiency is measured in bent condition too. From the measured return loss plot it is witness that in the bent condition the magnitude of S_{11} is reduced with effect the gain of the antenna and so efficiency is affected. The efficiency obtained in bent condition is 41.34% at 5.8 GHz and 45 for an input of −5 dBm.

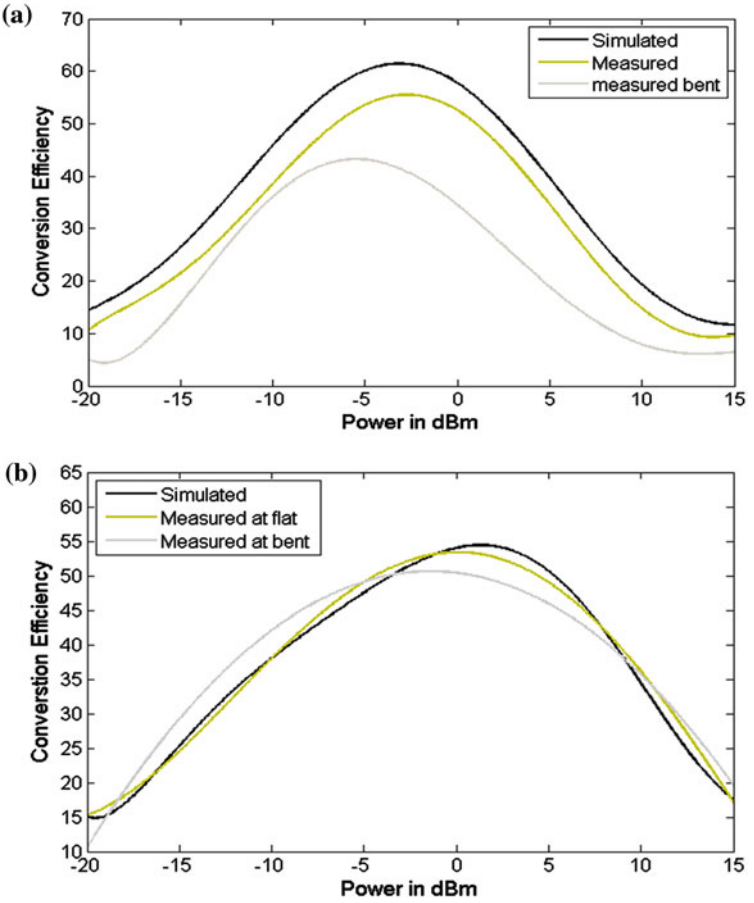


Fig. 5 **a** Measured and simulated overall efficiency versus input power levels at 5.8 GHz. **b** Measured and simulated overall efficiency versus input power levels at 2.45 GHz

From Eq. (6) DC power output is directly proportional to the square of the DC voltage and the effect of load resistance on power conversion efficiency is studied at dual bands. The harmonics at the output DC voltages has to be limited by connecting an LC filter at load side. The inductor in the filter controls the load current variations and output voltage variations are dampens by the capacitor. The capacitance value is chosen in such a way to limit maximum ripple in the output voltage is 10 mV at −5 dBm power level. The DC output voltages at the flat and bent position are 0.82 V (2.45 GHz) and 1 V (5.8 GHz) are shown in Fig. 6a. Finally, the low-power microwave energy harvester is fabricated on textile is depicted in Fig. 6b.

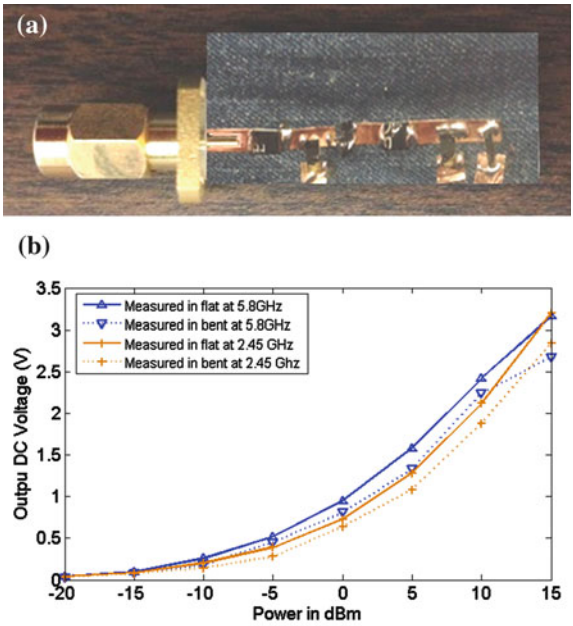


Fig. 6 **a** Fabricated 2.45 GHz rectenna on textile material. **b** Output DC voltages from rectifier

5 Summary

This paper works explain the design and manufacturing of the antenna with the textile materials and also its potential application in wearable wireless system. The textile antenna is made with jeans cotton as the substrate and copper tap as a radiating element. From the measured results the fabricated antenna has dual band in that first band covers the ISM bans 2.45 and 5.8 GHz. Proposed textile rectenna is tested for different micropower levels as −20 to 15 dBm. The wearable antenna has experimentally measured impedance bandwidth of 40% for primary band and 51% for second band. The rectenna has maximum efficiency of 60% at −3 dBm (5.8 GHz) and 0 dBm (2.45 GHz).

References

1. Shukla, S.S., Verma, R.K., Gohir, G.S.: Investigation of the effect of Substrate material on the performance of Microstrip antenna. In: IEEE Conference, pp. 1–3 (2015)
2. Mane, P., Patil, S.A., Dhanawade, P.C.: Comparative study of microstrip antenna for different subsrtate material at different frequencies. Int. J. Emerg. Eng. Res. Technol. **2**(9), 18–23 (2014)
3. Daya Murali, S., Narada Maha Muni, B., Dilip Verma, Y., Chaitanya, S.V.S.K.: Development of wearable antennas with different cotton textiles. Int. J. Eng. Res. Appl. **4**(7), 08–14 (2014) ISSN: 2248-9622

4. Zhang, H.S., Chai, S.L., Xiao, K., Ye, L.F.: Numerical and experimental analysis of Wideband e-shaped patch textile antenna. Prog. Electromagnet. Res. C, **45**, 163–178 (2013)
5. Hall, P.S., Hao, Y.: Antennas and propagation for body-centric wireless communications. Artech House (2006)
6. Kennedy, T.F., Fink, P.W., Chu, A.W., Champagne, N.J., Lin, G.Y., Khayat, M.A.: Body-worn e-textile antenna: the good, the low-mass, and the conformal. IEEE Trans. Antennas Propag. **57**(4), 910–918 (2009)
7. Chahat, N., Zhadobov, M., Sauleau, R.: Antennas for body centric wireless communications at millimeter wave frequencies. Progress in compact antennas, Chapter 2 (2014)
8. Van Torre, P., Vallozzi, L., Rogier, H., Verhaevert, J.: Diversity textile antenna systems for fire fighters. In: 2010 Proceedings of the Fourth European Conference on Antennas and Propagation (EuCAP) (2010)
9. Lui, K.W., Murphy, O.H., Toumazou, C.: Wearable wideband circularly polarized textile antenna for effective power transmission on a wirelessly-powered sensor platform. IEEE Trans. Antennas Propag. **61**(7), 3873–3876 (2013)
10. Roundy, S.J.: Energy scavenging for wireless sensor nodes with a focus on vibration to electricity conversion, Ph.D. Thesis, University of California, Berkeley, USA (2003)
11. Lemey, S., Declercq, F., Rogier, H.: Textile antennas as hybrid energy-harvesting platforms. Proc. IEEE **102**(11), 1833–1857 (2014)
12. Agilent HSMS 285x Series Surface Mount Zero Bias Schottky Detector Diodes-Data Sheets 5898-4022 EN, Agilent Technologies, Inc. (2005)
13. Singh, N., Singh, A.K., Singh, V.K.: Design & performance of wearable ultra wide band textile antenna for medical applications. Microw. Opt. Technol. Lett. **57**(7), 1553–1557 (2015)
14. Singh, V.K., Dhupkariya, S., Bangari, N.: Wearable ultra wide dual band flexible textile antenna for WiMax/WLAN application. Int. J. Wireless Personal Commun. **90**(4), Springer (2016) (ISSN 0929-6212)
15. Singh, N.K., Singh, V.K., Naresh, B.: Textile antenna for microwave wireless power transmission. In: International Conference on Computational Modelling and Security (CMS 2016), Procedia Computer Science, vol. 85, pp. 856–861 (2016)

Reduction of THD in Nine-Phase Induction Motor Drive with CLC Filter

Manjesh, Nilima Siddhartha Dabhade, Amik Garg and Akash Kumar Bhoi

Abstract Most of the applications 60% of loads are motor driven loads, more than 90% of these loads are used for industrial applications. Many applications use three phase motor drive which limits the torque density. Multiphase motor drives are better solutions for high torque density and heavy loads. In this work a Nine-Phase Inverter is designed to drive nine-phase load along with fundamental frequency, the output of the inverter generates harmonics. These harmonics are higher than fundamental frequencies and cause total harmonic distortion (THD) which enhances the current harmonics and generates more heat in the load. Many techniques are used to suppress the harmonics to minimize the heat in the load. A common technique is employed in this paper to minimize THD by constructing CLC filter in the PWM inverter and simulated using Simulink/MATLAB, the results are compared with the normal nine-phase inverter.

Keywords Harmonics · Nine-phase inverter · CLC filter
Nine-phase induction motor · MATLAB/Simulink

Manjesh (✉) · N.S. Dabhade
Bangalore University, Bengaluru, India
e-mail: manjesh1972@gmail.com

N.S. Dabhade
e-mail: dabhade_nilima@yahoo.com

A. Garg
Research & Development Section, Sikkim Manipal Institute of Technology,
Sikkim Manipal University, Rangpo, India
e-mail: amikkgarg@gmail.com

A.K. Bhoi
Department of Electrical & Electronics Engineering, Research & Development Section,
Sikkim Manipal Institute of Technology, Sikkim Manipal University, Rangpo, India
e-mail: akash730@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_3

1 Introduction

The three-phase drives are generally used for heavy torque loads, if the phases are increased beyond three phase then it is more advantageous. The main advantages of constructing a multiphase motor in place of a three-phase motor is due to density of high torque, minimization of ripples, better noise suppression, smoother torque and reduction of the torque ripple magnitude [1]. To drive the multiphase motor multi phase inverters are used, multiphase drives are best examples for high torque motor drives like aviation, hybrid electric cars, traction and battery-operated electric vehicles.

2 Nine-Phase Induction Motor Drive

The N Phase Asynchronous machines have "n" number of stator windings obtained by "360°/n" phase. Therefore nine-phase synchronous motor has nine-stator windings with 40° phase shift. Rotor windings use squirrel cage rotor, the nine-phase synchronous motor is fed by nine-phase inverter presented in Fig. 1. There are nine-push pull drives, each drive is triggered by PWM signal, thus there are nine-PWM signals which are 40° out of phase with each other. The PWM trigger signals used to drive IGBT (Insulated-Gate Bipolar Transistor) switches, all the switches operated for a period of 180° conduction mode is as shown in Figs. 2 and 3.

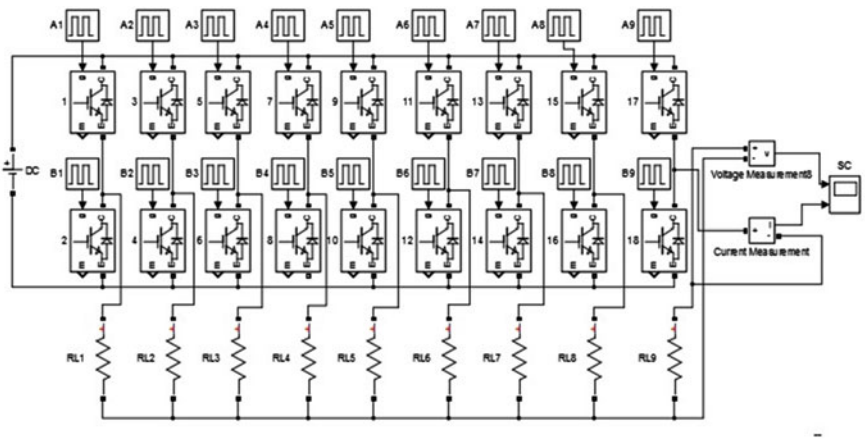


Fig. 1 Schematic diagram of nine-phase inverter drive

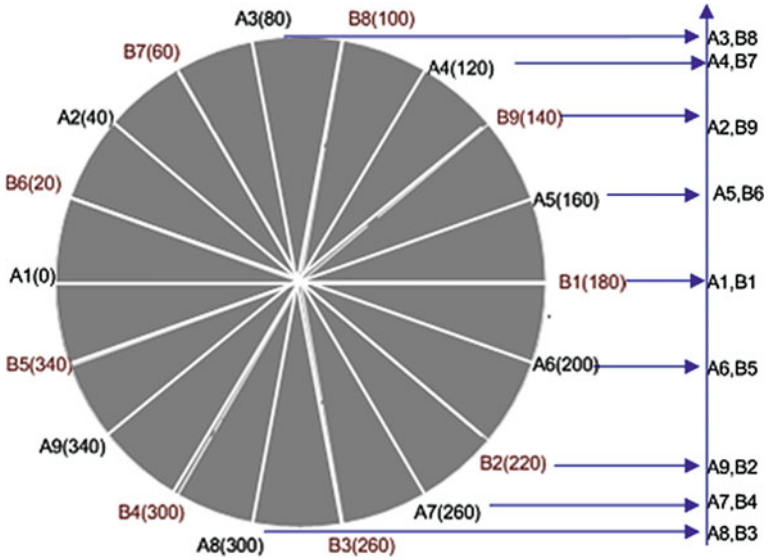


Fig. 2 Switching cycle of inverter legs with 180° conduction mode

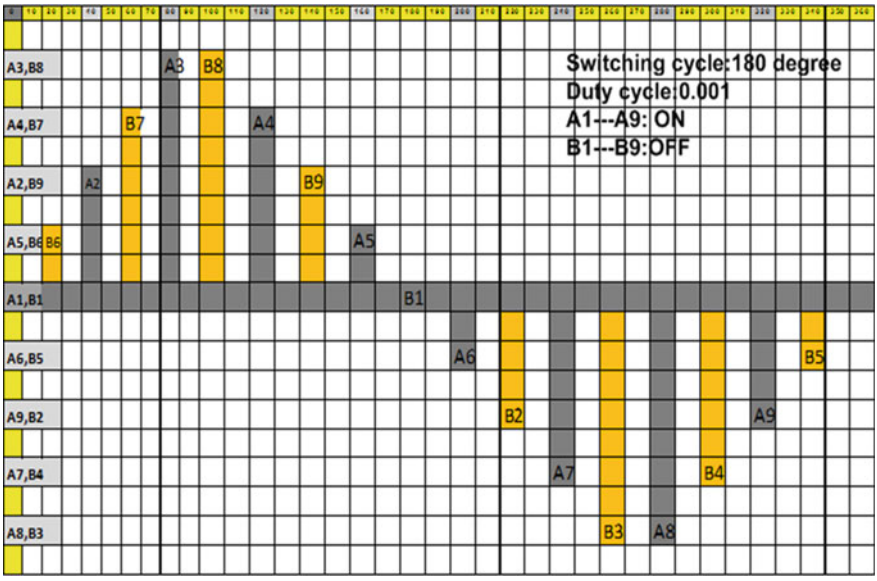


Fig. 3 Switching sequence of inverter legs with 180° conduction mode

3 Nine-Phase Inverters

The inverter is most commonly used unit for motor drive applications in industries, speed of the asynchronous motor can be varied by pulse width modulation method. Most of the inverters use power MOSFETs or IGBTs as semiconductor switching devices. The PWM inverter topology use semiconductor switches, each leg is constructed with two semiconductor switches connected in series, in each PWM inverter leg the ON and the other is OFF, the operation will be performed with upper and lower switches alternatively. The arms of PWM inverter design is depending on linear and nonlinear phase load applications [1–10]. The nine-phase inverter is constructed with nine legs and 18 switches as shown in Fig. 4.

The control signals to the inverter switches are pulse width modulated (PWM) signals which are generated through pulse generators. The magnitude of generated pulse depending on modulation index, as the modulation index approaches unity, the harmonic content can be minimized. Reducing a THD is very important factor in power electronics systems, harmonics are the sinusoidal frequencies of voltage and current that is whole multiples of fundamental power supply frequency 50 Hz. The main reason for the presence of harmonics in the power electronic converter system is the use of nonlinear loads, the additional power harmonics associated with fundamental frequency will not provide any additional energy nor influences any mechanical torque at the output of inverter, but this frequency of harmonics dissipated as heat in the load, which affects the power factor and switching losses.

THD is the percentage of harmonic magnitudes at the output of the inverter which affects the efficiency of an inverter. Third-order harmonic is the most prominent harmonic content which belongs to 3rd order of 50 Hz, i.e. 150 Hz, also amplitude of harmonic is 34.70% of the input power, the suppression of third harmonic can improve the efficiency of an inverter.

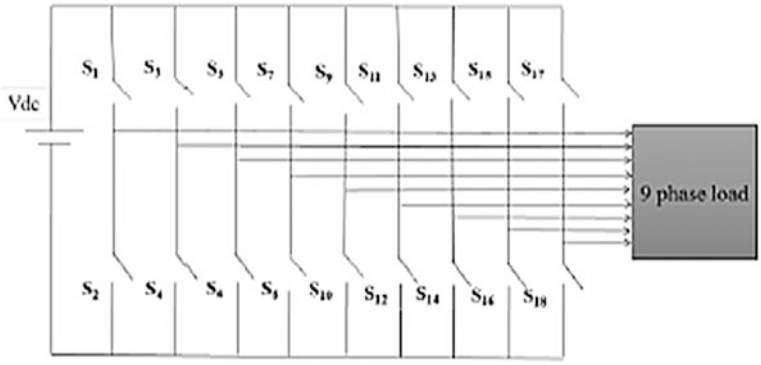


Fig. 4 Topology of nine-phase inverter

Nonlinear loads are the major challenge in the field of power electronics, the gradual impact of nonlinear parameters on load generates additional harmonic frequencies, which affect the power factor. The power rectifiers and PWM inverters are employed to operate the nonlinear loads and 'Filters' are the best option to overcome this distortion.

Filters are the circuits which block the unwanted frequency components of different harmonics, passive filters are easy to construct but at lower frequencies the values of the components are complex. In the nine-phase PWM inverter drive, the even harmonics are absent and only odd harmonics are present at the output of the nine-phase inverter, as third harmonic is most dominant harmonic, this dominant harmonic can be reduced by using passive filters [11–13].

3.1 Nine-Phase Inverters with Passive Filter

Block diagram of PWM 9-phase inverter using CLC filter and R-load in each phase is as shown in Fig. 5.

The schematic designed with the CLC filters arranged with the combination of two capacitors and an inductor. It provides better minimization of harmonics in the nine-phase inverter compare to other filter techniques. Main significance of using the CLC scheme at the inverter output is to reduce unwanted harmonics with ripples at the output of the converter.

Resonant frequency of the circuit with CLC filter scheme can be obtained by

$$f_0 = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

where f_0 is the 'frequency' of resonance, L is an 'Inductor' and C is a 'capacitor'. The filter scheme has been constructed using Eq. (1), resonance frequency has been taken

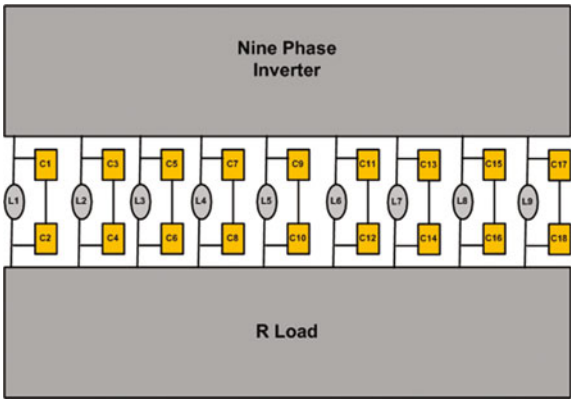


Fig. 5 Block diagram of nine-phase inverter with CLC filter and *R* load

as 150 Hz to eliminate three harmonic (3 × 50 Hz). The values of inductor and capacitor has been designed accordingly, L = 1.12 µH and $C_1 = C_2$ = 1000 mF.

The complete circuit diagram with CLC filter is as shown in Fig. 6 the CLC filter is connected at the output of the inverter with nine-phase star load, where C_1 to C_{18} = 1000 mF and L_1 to L_8 = 1.12 µH.

4 Simulation Results

The results obtained using 9-phase inverter with and without filter are presented in Figs. 7 and 8. The waveforms are generated for line voltage and line current, simulation work has been carried out for nine-phase inverter by connecting CLC filter at the output of the inverter and obtained the THD, also the same circuit is used to obtain the parameters without using the filter scheme. The inverter drives studied and simulated for rated frequency 50 Hz, the results obtained are analyzed for harmonics and (THD).

Figures 9 and 10 shows the FFT analysis of normal nine-phase inverter for 50 Hz using CLC filter scheme respectively. The comparison of percentage of reduction in THD of traditional inverter drive without filter and with CLC filter scheme is presented in Table 1. The drastic change is observed in presence of odd harmonics with and without CLC filter for f = 50 Hz is shown as in Table 2.

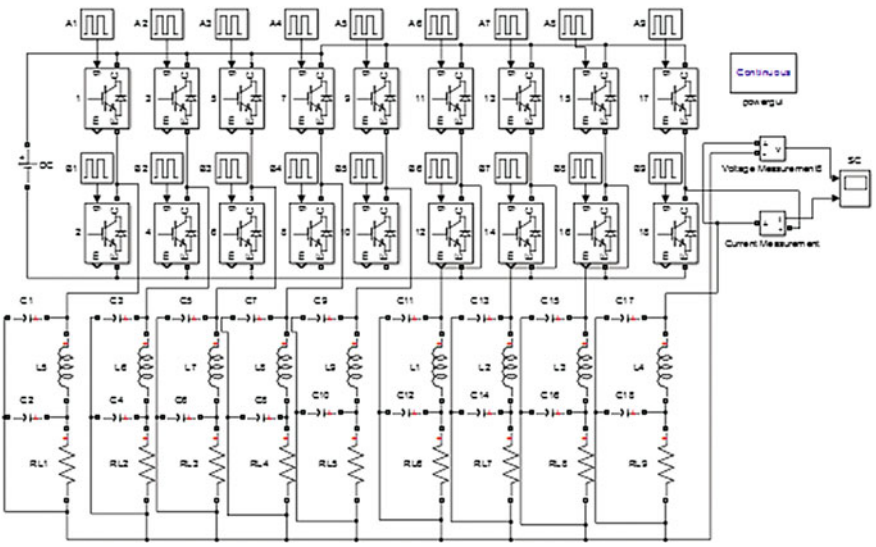


Fig. 6 Schematic of nine-phase inverter drive with CLC filter

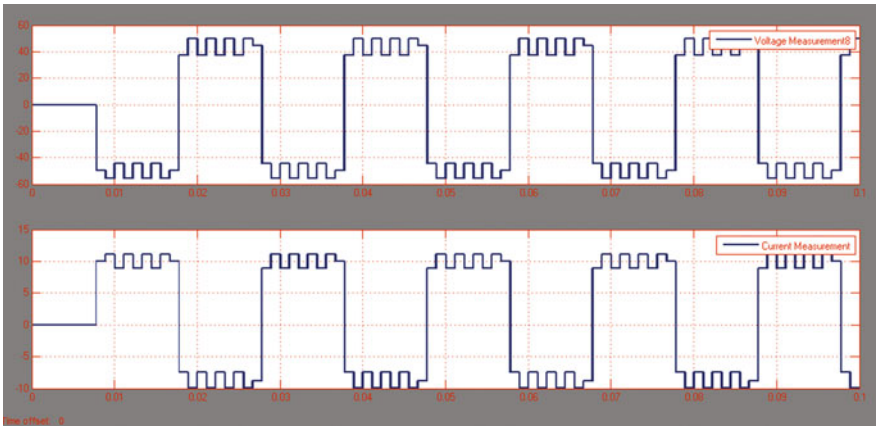


Fig. 7 Individual line voltage/current waveforms without filters

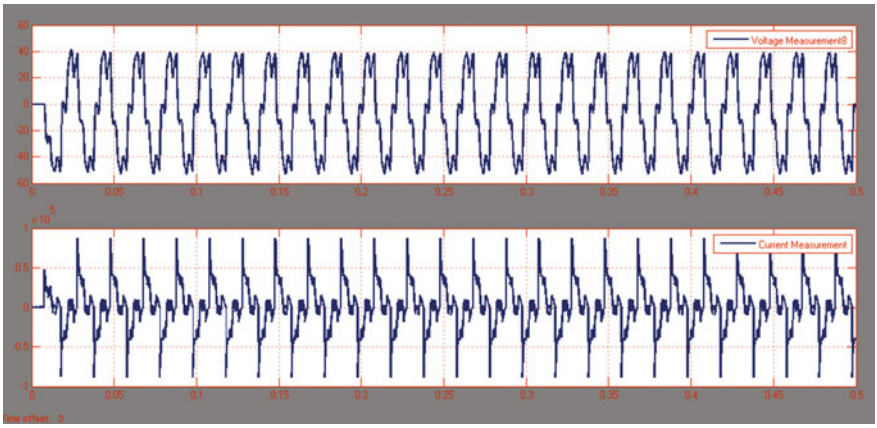


Fig. 8 Individual voltage/current waveforms with CLC filter

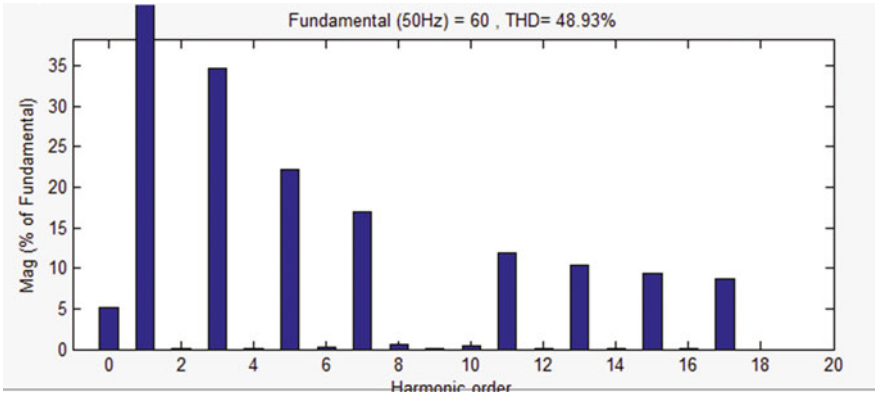


Fig. 9 FFT analysis of normal nine-phase inverter for 50 Hz

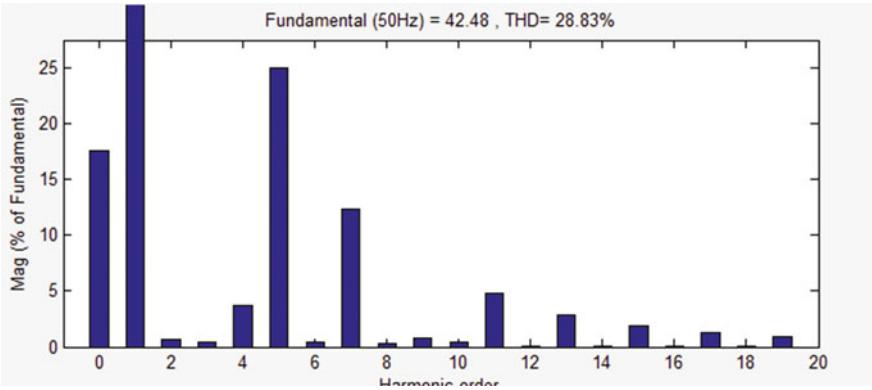


Fig. 10 FFT analysis of nine-inverter with CLC filter for 50 Hz

Table 1 Comparison of THD without filters and with CLC filter for fundamental frequency 50 Hz, V_{dc} = 100 V

Modes	THD (%)
Without CLC filter	48.93
With CLC filter	28.83

Table 2 THD profile without and with CLC filter for frequency 50 Hz

Harmonics	Without filter THD (%)	With filter THD (%)
3rd	34.70	0.38
7th	16.92	12.56
9th	0.00	0.77
11th	11.85	4.78
13th	10.34	2.85
17th	8.05	1.20
19th	0.00	0.96

The parameters used for simulation work with frequency f = 50 Hz, V_{dc} = 100 V, the THD obtained at the output of the 9-phase inverter is presented in Table 1.

The THD analysis for nth harmonics is as shown in Table 2, at fundamental frequency f = 50 Hz, V_{dc} = 100 V.

5 Conclusion

A nine-phase Inerter drive is constructed using Simulink/MATLAB to study the harmonics and THD of the nine-phase inverter and compared the results obtained using Nine Phase Inverter and CLC filter. It is observed that the harmonics and percentage of Total Harmonics Distortion (THD) at the output nine-phase inverter is found to be less using CLC filter. This work extended to study the nine-phase asynchronous motor for stator winding temperature analysis.

References

1. Singh, G.K.: Multi phase Induction Machine Drive research survey. Elect Power Syst. Res. **62**, 139–147 (2002)
2. Bose, B.: Power Electronics and AC Drives. Prentice Hall, Englewood Cliffs (1986)
3. Levi, E., Jones, M., Vukosavic, S.N., Toliyat, H.A.: A five-phase two-machine vector controlled induction motor drive supplied from a single inverter. EPE J. **14**(3), 38–48 (2004)
4. Jones, M., Levi, E.: A literature survey of state-of-the-art in multiphase ac drives. In: Proceedings of 37th International UPEC, Stafford, UK, pp. 505–510 (2002)
5. Levi, E., Bojoi, R., Profumo, F., Toliyat, H.A., Williamson, S.: Multiphase induction motor drives—a technology status review. IET Elect. Power Appl. **1**(4), 489–516 (2007)
6. Levi, E.: Multi-phase machines for variable speed applications. EEE Trans. Ind. Electron. **55** (5), 1893–1909 (2008)
7. Prasad Rao, K.P., Krishna Veni, B., Ravithej, D.: Five-leg inverter for five-phase supply. Int. J. Eng. Trends Technol. **3**(2), 144–152 (2012)
8. Moinoddin, S., Iqbal, A., Elsherif, E.M.: Five-phase induction motor drive for weak and remote grid system. Int. J. Eng. Sci. Technol. **2**(2), 136–154 (2010)
9. Dabour, S.M., Hassan, A.E.-W., Rashad, E.M.: Five-phase induction motor drive system fed from five-phase matrix-converter. In: Proceedings of the IEEE 15th International Middle East Power Systems Conference (MEPCON'12), Alexandria University, Egypt, December 23–25, Paper ID 302, pp. 898–903 (2012)
10. Reznik, A., Godoy Simões, M., Al-Durra, A., Muyeen, S.M.: LCL filter design and performance analysis for grid interconnected systems. In: IEEE Trans. Ind. Appl. **50**(2), 1225–1232 (2014)
11. Parikshith B.C., John, V.: Higher order output filter design for grid connected power converters. In: Fifteenth National Power Systems Conference (NPSC), IIT Bombay, (2008)
12. Ahmed, K.H., Finney, S.J., Williams, B.W.: Passive filter design for three-phase inverter interfacing in distributed generation. Electr. Power Q. Utilisation J. **XIII**(2) (2007)
13. Srivastava, K.K., Shakil, S., Pandey, A.V.: Harmonics & its mitigation technique by passive shunt filter. Int. J. Soft Comput. Engineering (IJSCE) **3**(2) (2013) ISSN: 2231-2307

Comparative Study of Harmonics and Total Harmonic Distortion of Five-Phase Inverter Drive with Five-Phase Multilevel Inverter Drive Using Simulink/MATLAB

Manjesh, K. Hasitha, Akash Kumar Bhoi and Amik Garg

Abstract Harmonics are created in the output of the Inverters due to nonlinear loads. These harmonics not only causes excessive heat in the devices or appliances used in the daily life of human being, but also reduces the life period of the appliances. This reduction of harmonics in such system has become great concern for the engineers. Multilevel inverter technology has proved to give improved harmonic performance. This paper presents simulation of harmonic analysis in five-phase two-level inverter and five-phase multilevel (three level). It has been found that the total harmonic distortion (THD) is less in case of five-phase three-level inverter.

Keywords Five phase · Multilevel · Diode clamped · Harmonics
FFT analysis · Total harmonic distortion

Manjesh (✉)
Department of Electronic Science, Bangalore University, Bengaluru, India
e-mail: manjesh1972@gmail.com

K. Hasitha
Department of Electronics, Mount Carmel College, Bengaluru, India
e-mail: hasitha.koka@gmail.com

A.K. Bhoi
Department of Electrical & Electronics Engineering, Research & Development Section, Sikkim Manipal Institute of Technology, Sikkim Manipal University, Rangpo, India
e-mail: akash730@gmail.com

A. Garg
Research & Development Section, Sikkim Manipal Institute of Technology, Sikkim Manipal University, Rangpo, India
e-mail: amikkgarg@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_4

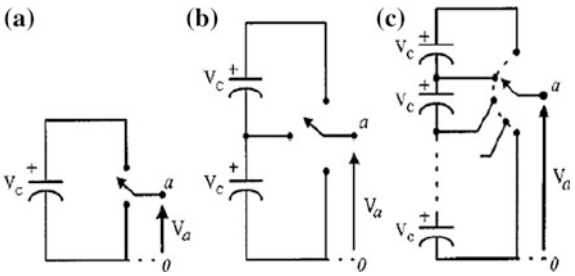


Fig. 1 Individual phase arm with **a** two-level **b** three-level and **c** *n*-level

1 Introduction

Present technology in power electronic system especially industrial applications work with high power. Some linear loads in the industries, however, require medium or low power for their operation [1]. Multilevel inverters are used to reduce the content of the harmonics at the inverter, harmonics major problems for the linear loads, these harmonics are generated from inverters and converters, it is required to minimize for the loads, the harmonics cause heat in the loads this is the main drawback of the loads. Figure 1 shows the inverters with different voltage levels. Multilevel inverters have many applications due to high power system relevant to lower output voltage harmonics and lower power switching losses [2, 3]. Multilevel are classified into three types, diode clamped multilevel inverter, flying capacitors multilevel inverter and cascaded H-bridge multilevel inverter. Multilevel inverters are added advantages on reduction of harmonics at the output of the inverter, also has high-power applications in industries.

2 Five-Phase Inverters

Five-phase inverter is constructed with five harms consist of 10 IGBTs are as shown in Fig. 2 the switching operation of the inverter can be implemented with pulse generators with phase shift of 72° with each phase arm of the inverter. The switching conductions sequence can be analyzed, two switches from upper group and three from lower group are turned on to synthesize five-phase output voltage shown in Fig. 3.

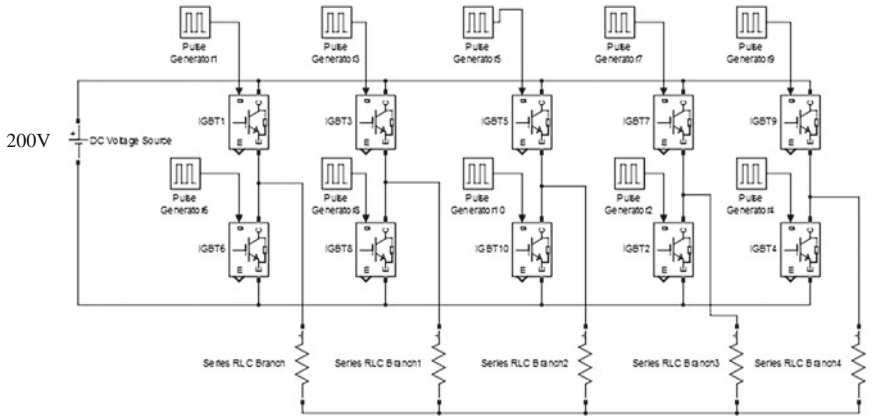


Fig. 2 Five-phase two-level inverter

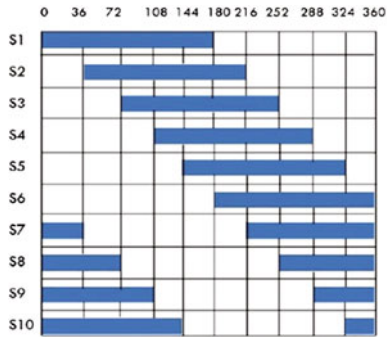


Fig. 3 Switching sequence for 180° conduction angle

3 Five-Phase Multilevel Inverters

The diode clamped multilevel inverter constructed with two capacitors inserted in series at the input side of the inverter and assigned as DC neutral point. These capacitors scheme synthesize three level output DC voltage of $V_{dc}/2$, 0, $-V_{dc}/2$. To increase the number of levels at the output of the inverter series connected capacitors should be increased. Therefore to synthesize an n-level output voltage $(n - 1)$ capacitors are used. This work presents a three level inverter with diode clamped scheme is employed. The circuit is constructed with two input capacitors with DC neutral point presented in Fig. 4.

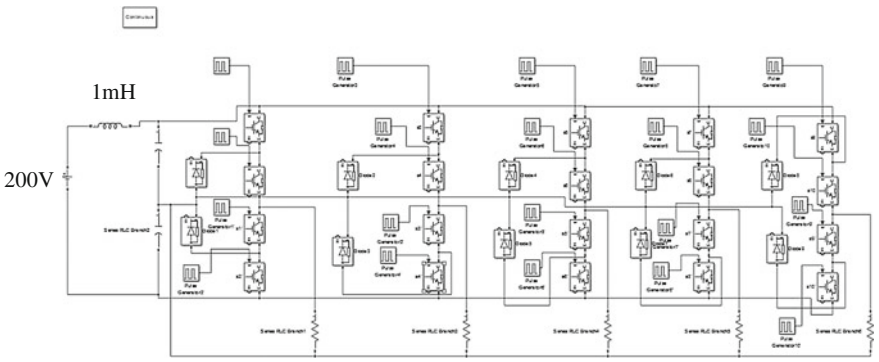


Fig. 4 Five-phase three-level inverter

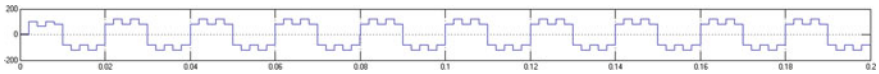


Fig. 5 Output voltage (125.9 V) of an individual five-phase two-level inverter

4 Simulation Results

The output voltages of both types of inverters are simulated by using "Matlab/Simulink" software [4]. The IGBT's are used to construct 5-phase inverter and multilevel inverter. The gate pulses are generated using pulse generators and the simulation is done for both the inverters.

Parameters used for simulation:

$$\text{Input voltage} = 200\,\text{V}$$
$$R = 1.7\,\Omega.$$

Figures 5 and 6 shows the output voltage and FFT analysis of five-phase two-level inverter. Total harmonic distortion of output voltage is found to be 43.05%.

Figures 7 and 8 shows the output voltage and FFT analysis of five-phase three-level inverter. Total harmonic distortion of output voltage is found to be 38.38%.

The overall THD for both inverters is shown in Table 1.

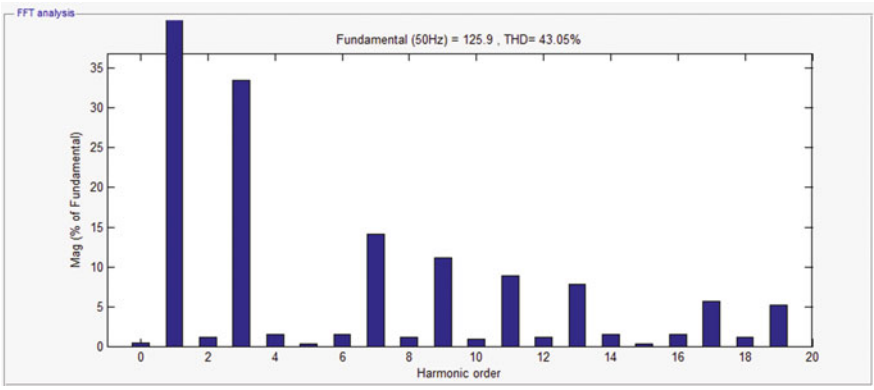


Fig. 6 FFT analysis of five-phase two-level inverter

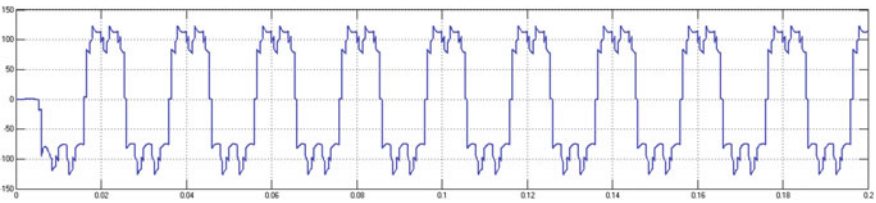


Fig. 7 Output voltage (123.7 V) of an individual five-phase three-level inverter

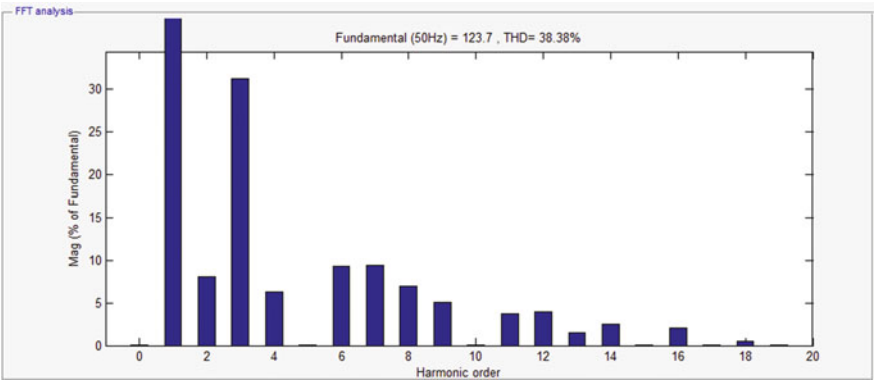


Fig. 8 FFT analysis of five-phase three-level inverter

Table 1 Total harmonic distortion of five-phase two- and three-level inverter (THD)

Inverter	THD (%)
Five-phase two level inverter	43.05
Five-phase three level inverter	38.38

5 Conclusion

A comparison of total harmonic distortion of five phase two-level and five-phase three-level multilevel inverter is constructed and analyzed using Simulink/Matlab. The results obtained with FFT analysis and presented in this work. From the results it is concluded that the content of harmonics and total harmonic distortion is found to be less in case of Five Phase three-level multilevel inverter. The results obtained can be used to study temperature analysis of five-phase induction motor in future work.

References

1. Patomaki, L., Forsti, J., Nokso-Koivisto, V.-M., Jokinen, Y., Lansimies, E.: On line recording and analysis of the ECG in ambulatory patients. Comput. Cardiol. 173–175 (1981)
2. Thakor, N.V., Webster, J.G., Tompkins, W.J.: Design, implementation, and evaluation of a microcomputer-based portable arrhythmia monitor. Med. Biol. Eng. Comput. **22**, 151–159 (1984)
3. Mark, R.G., Moody, G.B., Olson, W.H., Peterson, P.S., Schulter, S.K., Walters, J.B., Jr.: Real-time ambulatory arrhythmia analysis with a microcomputer. Comput. Ardiol. 57–62 (1979)
4. Pahlm, O., Sornmo, L.: Software QRS detection in ambulatory monitoring—a review. Med. Biol. Eng. Comput. **22**, 289–297 (1984)

Design and Implementation of Two Level and Multilevel Inverter

Amruta Pattnaik, Shawet Mittal, Vinay Gupta, Basudev Prasad and Akash Kumar Bhoi

Abstract This paper deals with the comparative study of two-level inverter and three level inverter (Multilevel Converter) topologies. The multilevel term defines more than two level whose performance is better than the two-level inverter because of lesser harmonics, electromagnetic interference and higher dc link voltages. In this paper, three levels Diode Clamped Multilevel inverter with PWM technique is recommended to improve the performance of inverter. This topology requires fewer apparatuses and therefore the cost and complexity is lesser as compared to other topologies of multilevel inverter.

Keywords Multilevel inverter · Voltage Source Inverter (VSI)
Harmonic reduction · MATLAB/Simulink

1 Introduction

The average voltage and megawatt power are basically required for specified motor drives. The alternative concept of multilevel inverters is introduced for high power and medium voltage situations since there is difficulty in connecting the power electronic devices directly with a specified voltage grid. A multilevel inverter can

A. Pattnaik (✉) · B. Prasad
Department of Energy & Environment, TERI University, Vasant Kunj 110070, Delhi, India
e-mail: amruta.pattnaik@students.teriuniversity.ac.in

V. Gupta
Department of Physics & Astro-Physics, University of Delhi, Delhi 110007, India

S. Mittal
Department of Electrical & Electronics Engineering, Northern India Engineering College, Shastri Park 110053, New Delhi, India

A.K. Bhoi
Department of Electrical & Electronics Engineering, Research & Development Section, Sikkim Manipal Institute of Technology, Sikkim Manipal University, Rangpo, India
e-mail: akash730@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_5

be straight forwardly interfaced to nonconventional energy resources like solar cells, wind energy conversion system (WCES), fuel cell [1–3].

The multilevel inverter was introduced in 1975 [4, 5]. The multilevel inverter comprises number of capacitor-voltage sources and semiconductor devices generating staircase waveform output voltage which is being used in industrial applications. This is being done because of usage of higher power rated equipment in industrial applications.

The series arrangement of switches which are controlled by switching angle or frequency in the multilevel inverter arranged in such a way that it provides the sinusoidal output voltage and current with less harmonic distortion [6].

In this paper, a three-level inverter topology is compared with two-level VSI based inverter. The analysis and simulation of the suggested topologies is verified for checking the viability of the topology.

2 Two-Level Inverter and Multilevel Inverter

The advantages of multilevel inverter over conventional inverter are as follows: lower THD value, less switching losses due to allow range of switching frequency, good electromagnetic compatibility and lower voltage stress on switches resulting in high voltage capability [7]. One of the biggest disadvantages is that it needs more power modules. The driver isolations are complicated because of the requirement of the extra level (each level requires an additional power source), making it costly compared to conventional inverters. The attractive features of multilevel inverter have inspired the researchers to go through the studies on these [8, 9]. Recently, in order to reduce the demerits, the researchers are developing some multilevel inverter with decreased number of power semiconductor devices [10–12].

The purpose of inverter is changing the supply from DC to AC, wherever essential. Voltage Source Inverter is fed with Direct Current source (having negligible impedance), whereas a Current Source Inverter is fed with variable current from a DC source (having high impedance). Various converter applications are ASDs, UPS, active filters, static VAR compensators, Flexible AC transmissions (FACT), voltage compensators, etc. The normally required source is the voltage source with controllable magnitude, frequency, and phase should be of the output ac voltage. The topologies of the VSIs are considered on the basis of the output AC waveform, as required by many industrial applications.

A conventional two-level VSI is illustrated in Fig. 1 [13]. It is consisting of a DC link capacitor and six power semiconductor devices. In order to produce 3-Φ supply, the energy of the DC link capacitor is released. The switching of the power electronic devices is done using the PWM switching scheme.

A three-level converter comes under the category of multilevel converters. Medium voltage semiconductors devices can be used for applications using both high voltage and power [12, 14]. In this paper, the diode clamped multilevel inverter is used with PWM technique as shown in Fig. 2 [12, 14].

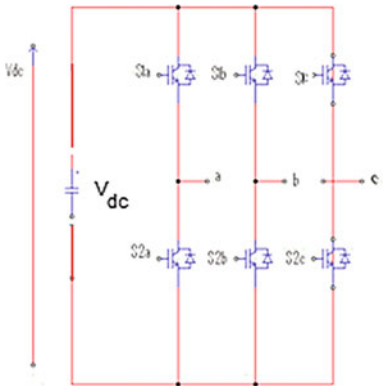


Fig. 1 Two-level six-pulse VSI

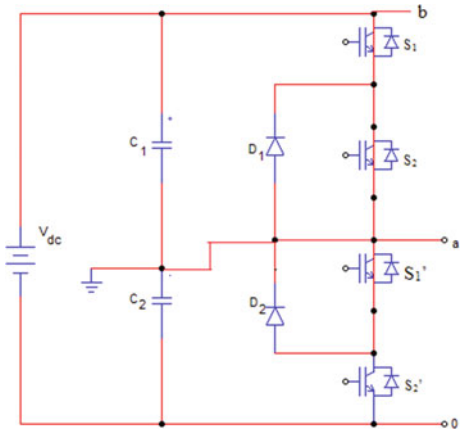


Fig. 2 Diode clamped three-level VSI

3 Sinusoidal Pulse-Width Modulation Technique

The pulse-width modulation technique used by a converter is one of the methods of controlling the output voltage. In PWM technique, the input is fixed dc source and the output is controlled by ac source, which is obtained by controlling the on and off periods of the semiconductor switching devices used in the inverter. The merits of this technique are as follows: (i) No additional component for controlling the output voltage (ii) The lower order harmonics can be eliminated using this technique and higher order harmonics can be filtered using the suitable filtering technique [15]. Different PWM techniques categorized on the basis of current and voltage control are as follows: (i) Sigma-Delta modulation, (ii) Delta Modulation, (iii) space vector PWM, (iv) SPWM (Sinusoidal pulse-width modulation), (v) SHE (selected harmonic elimination) PWM [16], (vi) Minimum, ripple current PWM, (vii) Hysteresis band current control PWM, (viii) SPWM with current control [13]. Out of all these, the SPWM technique is used here.

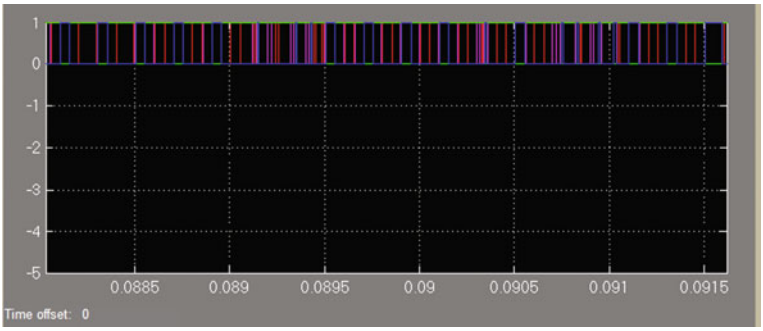


Fig. 3 SPWM gate pulse for inverter

SPWM is used for suppressing the harmonics because of its following features: (i) having a constant amplitude and variable time period of the pulses which are modulated for voltage control and for harmonic reduction. (ii) Reduces switching losses by incorporating soft switching at voltage zero and current zero. (iii) The comparison between the sinusoidal wave and the triangular wave in order to produce the pulses. Figure 3 shows the SPWM gate pulse for both inverters [16].

4 Simulink Model and Results of a Two-Level Inverter

Two-Level Inverter is the electrical device used for converting DC supply to an AC supply. Multilevel inverter has advantages over two-level inverter such as multilevel inverter is applicable for high voltage applications whereas two level are not applicable.

The MATLAB/SIMULINK technical software is used to simulate the inverter with the R-L load. Here the Simulink model for two-level VSI has been given in Fig. 4 while the simulation results of line current, line voltage, and FFT have given below in Figs. 5, 6 and 7 respectively.

Current and voltage waveforms are shown above figures along with the FFT analysis of a current waveform in a two-level inverter which shows that THD value is 6.30% (Fig. 8).

5 Simulink Model and Results of a Three-Level Inverter

AMATLAB/SIMULINK model for three-level diode clamped inverter is presented below in which twelve IGBT and six gate pulses are required to operate the switches. The simulation results like line current, line voltage and FFT of three-level diode clamped multilevel converter are shown in Figs. 9, 10 and 11

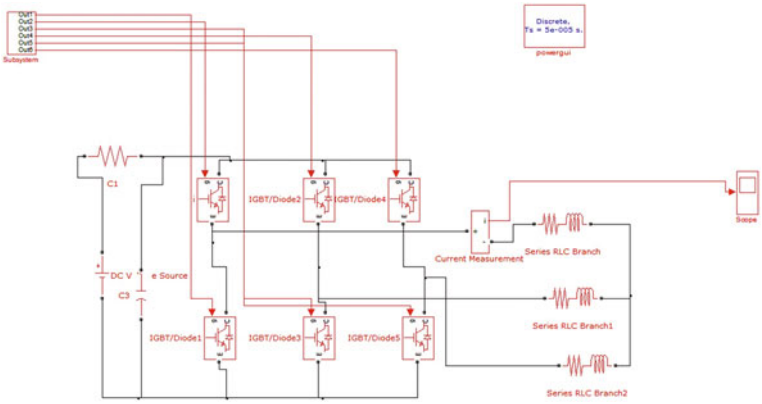


Fig. 4 MATLAB/SIMULINK model of two-level VSI

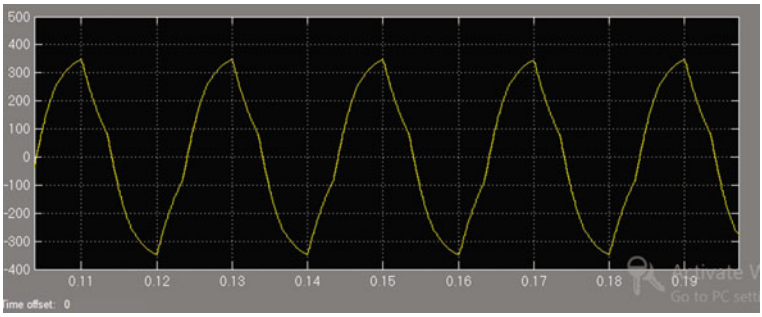


Fig. 5 Line current waveform of a two-level inverter

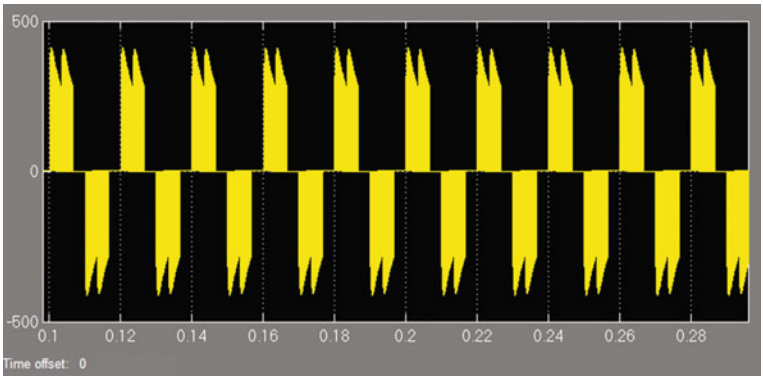


Fig. 6 Line voltage waveform of a two-level inverter

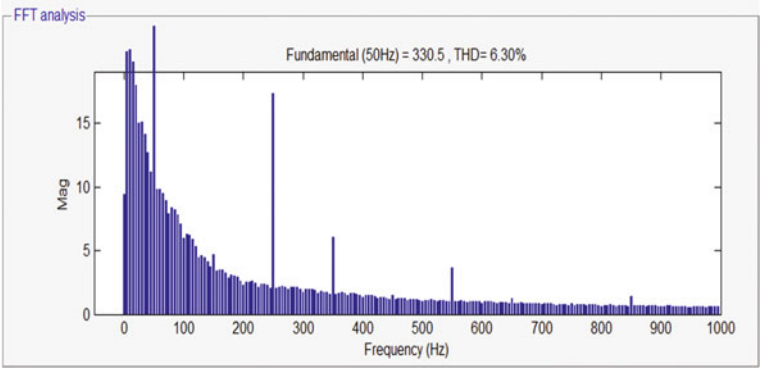


Fig. 7 FFT analysis of line current waveform in a two-level VSI

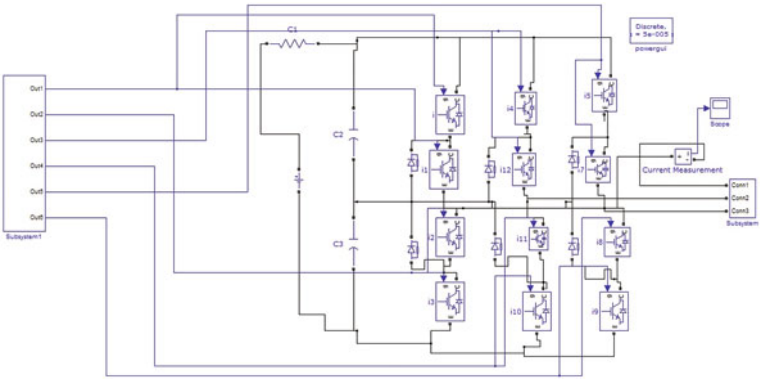


Fig. 8 MATLAB/SIMULINK model of three-level diode clamped inverter

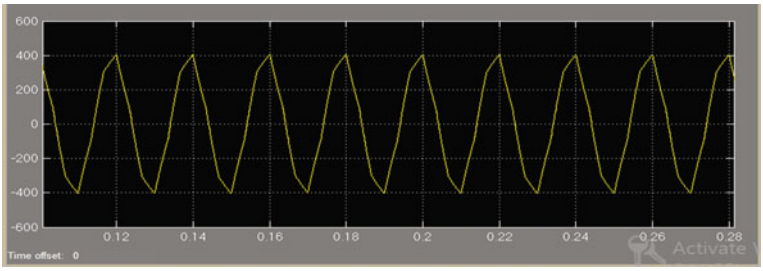


Fig. 9 Line current waveform of three-level diode clamped Inverter

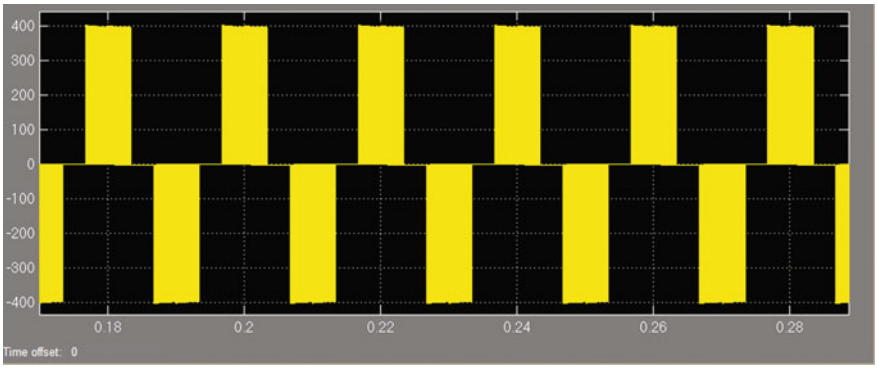


Fig. 10 Line voltage wave form of three-level diode clamped multilevel inverter

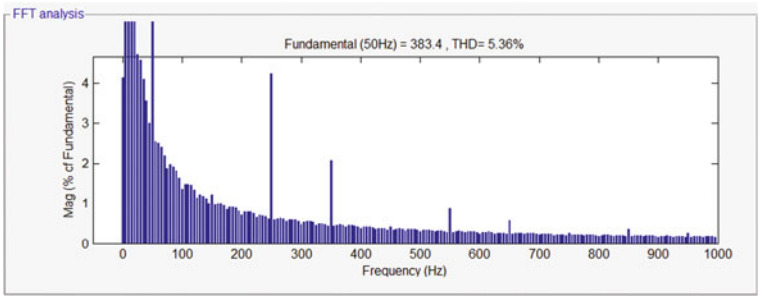


Fig. 11 FFT analysis of line current waveform in a three-level diode clamped VSI

Table 1 Comparison between the current THD values of two level and Multilevel inverter

Parameter	Two-level inverter (%)	Three-level inverter (%)
THD value	6.30	5.56

respectively and the FFT analysis of current to analyze the harmonics and the resultant spectrum is shown in Fig. 11 which shows that THD value is 5.36% (Table 1).

6 Conclusion

A comparative study and analysis of two- level and three-level inverter have discussed in the paper. It discussed regarding the different techniques used in the two-level and three-level diode clamped inverter with new multilevel topology.

According to this report, it is concluded that three level multilevel inverter is better than the other methods due to reduced harmonics. The applications of diode clamped multilevel inverters are such as Electrical Drives for an induction motor, STATCOM, aerospace and solar energy applications of SPWM technique.

References

1. Rodriguez, J., Lai, J.S., Peng, F.Z.: Multilevel inverters: survey of topologies, controls, and applications. IEEE Trans. Ind. Appl. **49**(4), 724–738 (2002)
2. Lai, J.S., Peng, F.Z.: Multilevel converters—a new breed of power converters. IEEE Trans. Ind. Appl. **32**, 509–517 (1996)
3. Tolbert, L.M., Peng, F.Z., Habetler, T.: Multilevel converters for large electric drives. IEEE Trans. Ind. Appl. **35**, 36–44 (1999)
4. Baker, R.H., Bannister, L.H.: Electric Power Converter, U.S. Patent 3 867 643, February (1975)
5. Tahri, A., Draou, A., Ermis, M.: A comparative study of PWM control techniques for multilevel cascaded inverters. Applied Power Electronics Laboratory, Department of Electro technics, University of Sciences and Technology of Oran, BP 1505 El Mnaouar (31000 Oran), ALGERIA (2010)
6. Filho F.J.T.: Real-time selective harmonic minimization for multilevel inverters using genetic algorithm and artificial neural network angle generation, Ph.D. dissertation, University of Tennessee (2012)
7. Rahim, N.A., Mahrous, E.A., Sor, K.M.: Modeling and Simulation of Linear Generator PWM Multilevel Inverter. In: National Power and Energy Conference (PECon) 2003 Proceedings, Malaysia (2003)
8. Beser, E., Arifoglu, B., Camur, S., Beser, E.K.: Design and application of a single phase multilevel inverter suitable for using as a voltage harmonic source. J. Power Electron. **10–2**, 138–145 (2010)
9. Babaei, E., Hosseini, S.H.: New cascaded multilevel inverter topology with minimum number of switches. Energy Convers. Manag. **50**, 2761–2767 (2009)
10. Ahmed, R.A., Mekhilef, S., Ping, H.W.: New multilevel inverter topology with reduced number of switches. Proceedings of 14th International Middle East Power Systems Conference, pp. 565–570 (2010)
11. Nabae, A., Takahashi, I., Akagi, H.: A new neutral-point clamped PWM inverter. IEEE Trans. Ind. Appl. **IA-17**, 518–523 (1981)
12. Padiyaar, K.R.: FACTS controllers in power transmission and distribution (2007)
13. Bose, B.K.: Modern power electronics and AC drives. Prentice Hall India Edition (2005)
14. Tolbert L.M., Habetler, T.G.: Novel Multilevel Inverter Carrier Based PWM Method (2008)
15. Li, L., Crazkowski, D., Pillay, P., Liu, Y.: Multilevel selective harmonic elimination PWM technique in series connected voltage inverters, NY (1999)
16. Sinha, G., Lipo, T.: A four level rectifier inverter system for drive applications. IEEE IAS Annual Meeting, pp. 980–987 (1996)

Raman Characterization of Gallium Nitride Nanowires Deposited by Chemical Vapor Deposition

Umesh Rizal and Bibhu P. Swain

Abstract Gallium Nitride Nanowires (GaN-NWs) were synthesized on p-type c-Si (100) by thermal chemical vapor deposition (CVD) using Ag, Fe, In, Ni as catalysts. These NWs were synthesized with variation of H_2 flow rate from 40 to 120 standard cubic per centimeter (sccm) while maintaining constant flow of N_2 gas at 120 sccm. FESEM, FTIR, Raman and photoluminescence spectroscopy were used to characterize the GaN-NWs for microstructure, vibrational and optical properties. The microstructure of GaN-NWs reveals thin and hairy nanowires for Ag and In catalysts while long and thick NWs were observed for Fe and Ni catalyst. Raman spectra reveal that the peak position of A_1(LO), A_1(TO) phonon shifted to higher frequency from 705.37 to 716.58 and 520.94 to 528.71 cm^{-1}, whereas E_1(TO) phonon shows pronounced red shift from 544.36 to 540.60 cm^{-1}. In a similar sideline, fwhm of A_1(LO), A_1(TO) phonon increases from 13.11 to 21.01 cm^{-1} and 16.99 to 20.78 cm^{-1}, whereas fwhm decreases for E_1(LO) and E_1(TO) phonon. We have found Surface Optic (SO) phonon of GaN-NWs at 610 cm^{-1} in FTIR spectra. Room temperature photoluminescence (PL) spectra show a prominent blue luminescence from GaN-NWs.

Keywords GaN-NWs · Thermal CVD · Raman spectroscopy · FTIR Room temperature PL

U. Rizal · B.P. Swain (✉)
Nano-Processing Laboratory, Centre for Material Science and Nanotechnology, Sikkim Manipal Institute of Technology, Majitar, Rangpo, East Sikkim, India
e-mail: bibhu.s@smit.smu.edu.in

U. Rizal
e-mail: umeshrizal680@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_6

1 Introduction

From the past decade, research in Gallium Nitride Nanowires (GaN-NWs) is ever-increasing owing to its superior material properties such as high electrical conductivity [1], high carrier mobility [2], high break down voltage [3], and tailorable band gap [4]. GaN-NWs is an emerging wideband gap with a band gap 3.4 eV, used efficiently in optoelectronic, and sensors [5]. GaN-NWs synthesized various techniques such as laser ablation [6], MBE [7], and chemical vapourdeposition methods [8]. Zhang et al. investigated catalyst effect on microstructure and structural property of GaN-NWs using In, Fe, Ni, Au catalysts [9]. Wang et al. synthesized wurtzite GaN-NWs on silicon substrate using GaN powder, Nitrogen and Hydrogen as a reactive gas by PE-HFCVD [10]. Biswas et al. investigated the effect of Au catalyst on morphology of thermal CVD deposited GaN-NWs [8]. Samanta et al. reveals that the length of nanowires strongly depends on the size and diameter of catalyst nanoparticle [11]. Since catalyst plays an important role in the nucleation of semiconductor nanowires. However, H_2 dilution further modulate the inherent material properties of CVD processed GaN-NWs thin films [12]. However, catalyst effect on phonon modes of GaN-NWs has been rarely studied. To realize the importance of the catalyst and H_2 gas during GaN-NWs growth, herein we have synthesized GaN-NWs via reaction of gallium nitride vapor with flowing N_2, H_2 gas using Ag, Fe, Ni and In catalyst respectively. In this article, catalyst effect and H_2 dilution on microstructural, optical and phononic properties of GaN-NWs are discussed.

2 Experimental Details

GaN-NWs were grown by using GaN powder as a GaN source and N_2, H_2 mixture as precursor gases in a horizontal thermal CVD reactor. The p-type Si (100) (resistivity 3–10 Ω cm) substrate is placed on the downstream to the Ga source with the distance of 4 cm. The metallic coating of silver (Ag), iron (Fe), indium (In), and nickel (Ni) on c-Si were used as substrate. The growth temperature was 1050 °C at a rate of at 5 °C/min. The N_2 and H_2 flow rate of 120 sccm and 40 to 120 sccm, respectively. The deposition time was for 4 h. The microstructure of GaN NWs was observed by a FE-SEM, JEOL-JEM-3000F. The Raman spectrum was carried out by Horiba JobinYvon at room temperature using the 488 nm line of an Ar^+ laser as excitation source. Perkin Elmer spectrometer (Model: Spectrum 2) operated to take in transmission mode between 450 and 1500 cm^{-1} with a resolution of 1 cm^{-1}. Perkin Elmer LS-45 fluorescence spectrometer with Xe discharge lamp is operated at room temperature. The excitation wavelength was varied from 290 to 350 nm. The deconvolution of Raman spectra were carried out by an Origin 6.0 computer program.

3 Results and Discussion

3.1 Microstructure Overview

Figure 1 shows the microstructure of GaN-NWs synthesized using different catalysts. With In and Ag catalyst the NWs were thin and broken into pieces at many places. However, Fe and Ni catalyzed GaN-NWs were mostly straight, long, and entangled each other. The eutectic temperature of Ag–Ga, Ni–Ga, Fe–Ga, and In–Ga system were found as 301.85 °C [13], 895 °C [14], 770 °C [15], 153 °C [16], respectively. The following important factors decides the formation of nanowires (i) eutectic temperature of alloys, (ii) surface energy of catalysts, (ii) adatom vapor pressure inside the reactor, (iii) adatom vapor pressure inside catalyst particles [17]. In the past, GaN-NWs were synthesized successfully by using various catalysts such as Ag [18], Fe [18], Ni [19], and In [20]. Figure 1a–d shows FESEM of GaN-NWs using Ag, Fe, In and Ni catalysts with H_2 80 sccm flow rate. Figure 1a shows very thin GaN-NWs grown in presence of Ag catalyst. Comparatively thin NWs were observed with millimeter in length after 4 h of deposition. Figure 1b reveals the nodules like microstructure of GaN-NWs synthesized by using Fe catalyst. In addition, lots of twisted NWs were observed and randomly distributed on the substrates. Figure 1c shows the microstructure of In catalyzed GaN-NWs.

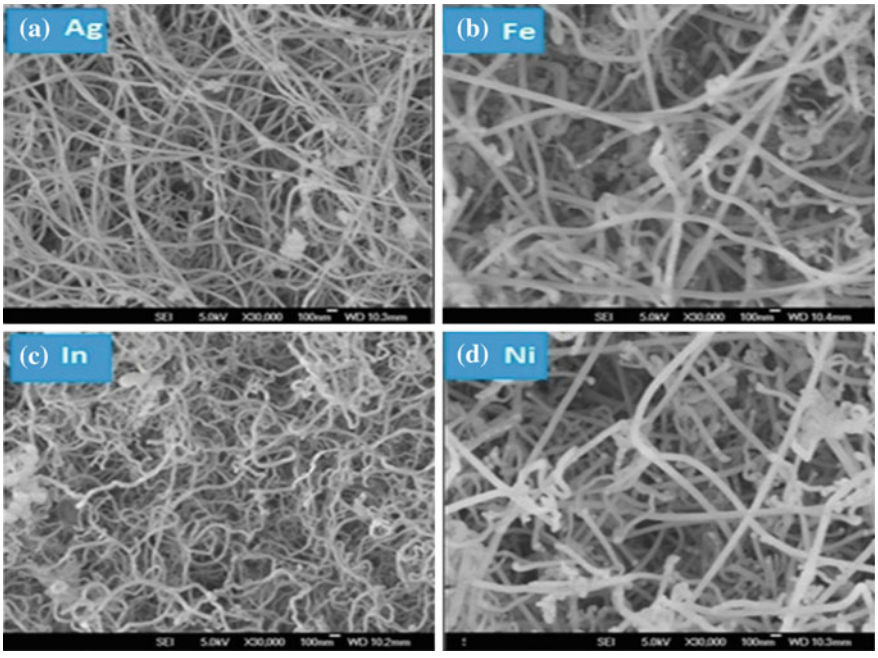


Fig. 1 FESEM images of GaN-NWs synthesized at 1050 °C with 80 sccm H_2 flow rate in the presence of different catalyst **a** Ag, **b** Fe, **c** In, **d** Ni

The NWs were broken into pieces and coiled. However, the density and distribution of NWs was much better than the other catalyzed GaN-NWs. Figure 1d shows a FESEM of GaN-NWs grown using Ni catalyst. The NWs are straight, long and entangled in a dense microstructural network of GaN. As seen from the SEM images, NWs grown with nickel and iron catalyst are mostly larger in diameter and long. It may due to more diffusion of nickel and Fe catalyst causes increased length of NWs. The limited surface diffusion is responsible for the saturated length of the NWs for the four different catalysts. Diffusion of adatom in liquid droplets of metal catalyst will be reduced the Gibbs free energy or chemical potential of system [21]. The diameter, density, and length of GaN-NWs synthesized in presence of Ag and In catalyst was quite different than Fe and Ni catalyzed GaN-NWs. These visible changes in the microstructure of GaN-NWs could be assigned to eutectic temperature of various metal catalysts.

We have further investigated the morphology of GaN-NWs by optical microscope. Figure 2a–d shows optical image (×200) of GaN-NWs thin films synthesized using different catalyst with variation of H_2 flow rates. Optical images reveal that the thin films were smooth and homogeneous. As it is evident from these figures, the color of thin film varies accordingly with each catalyst and H_2 flow rate. We believed that, emission of different colors by thin film might have strong correlation with size and diameter of catalyst nanoparticles.

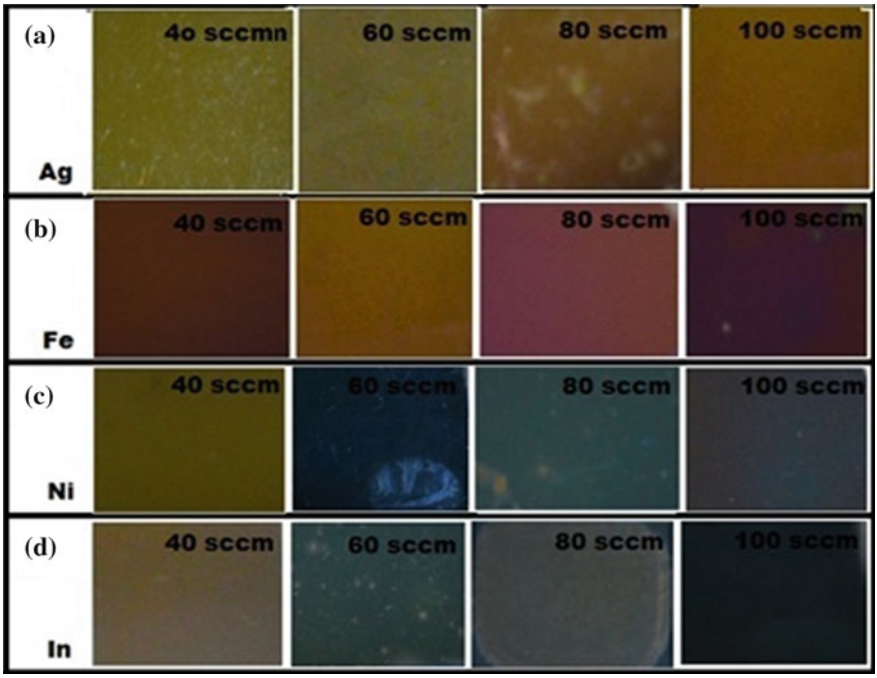


Fig. 2 Optical image of GaN-NWs synthesized using different catalysts with different H_2 flow rates **a** Ag catalyst, **b** Fe catalyst, **c** Ni catalyst, **d** In catalyst

3.2 Raman Spectroscopy

Figure 3 shows Raman spectra of GaN-NWs synthesized using Ag, Fe, In and Ni catalysts. As seen in figure, five well-defined phonon signatures were located at 421, 505, 539, 564 and 727 cm^{-1} correspond Zone boundary (ZB) phonon, A_1(TO), E_1(TO), E_2(high), A_1(LO) respectively [22]. The observed Raman bands were broad and asymmetrical, which often indicated size of nanowires, surface disorder, strains and surrounding chemical environment.

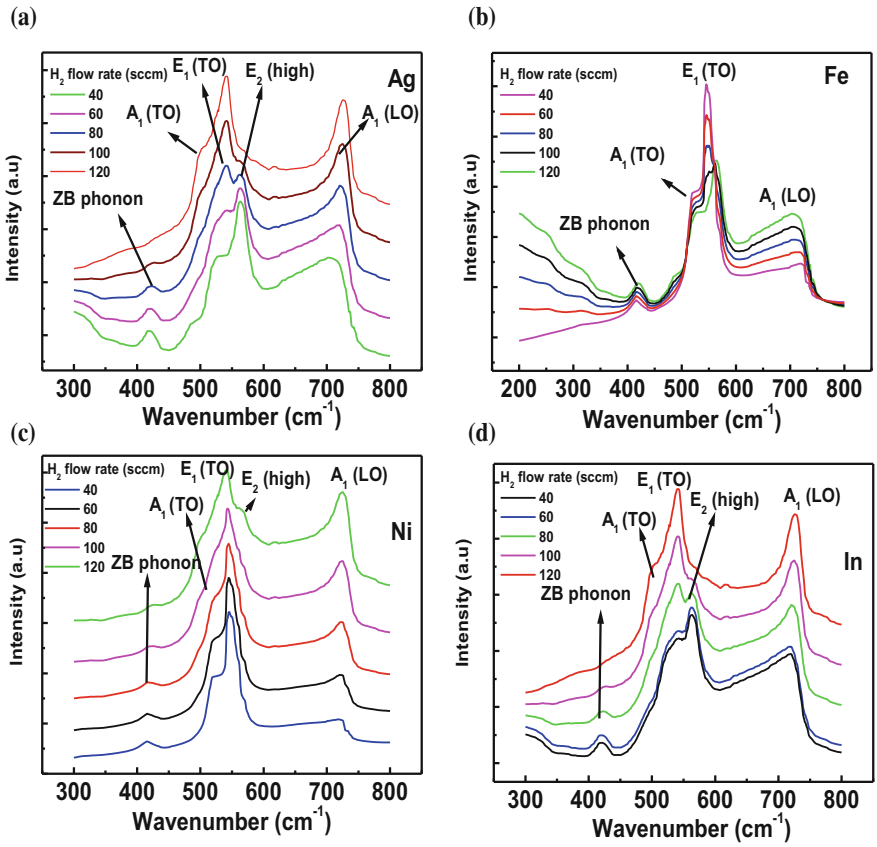


Fig. 3 Broad scans Raman spectra of GaN-NWs synthesized using different catalysts at 40–120 sccm H_2 and 120 sccm N_2 flow rate

3.3 *Transverse Optic Phonon of GaN-NWs*

Figure 4a–b shows the Raman peak position and fwhm of A_1(TO) and E_1(TO) phonons of GaN-NWs grown by using Ag, Fe, In and Ni catalysts. These plots were derived as per the curve fitting data of Fig. 3a–d. From Fig. 4a–b, the A_1(TO) phonon peak of GaN-NWs grown by using Ag catalyst varies from 522.41 to 534.89 cm^{-1} and fwhm increases from 18.61 to 24.38 cm^{-1}. In a similar sideline, the fwhm of A_1(TO) phonon of GaN-NWs grown by using Fe catalyst decreases from 17.99 to 16.08 cm^{-1} respectively, whereas their phonon frequency shifts from 520.3 to 520.7 cm^{-1}. The frequency shift of A_1(TO) peak in GaN-NWs is mainly attributed to the change of nanowires diameter, governed by size effect. For Ni catalyst induced GaN-NWs, the peak position of A_1(TO) phonon increases from 521.01 to 528.17 cm^{-1} and fwhm increases from 16.29 to 21.42 cm^{-1}. The red shift and blue shift of Raman peak can be attributed due to tensile and compressive stress

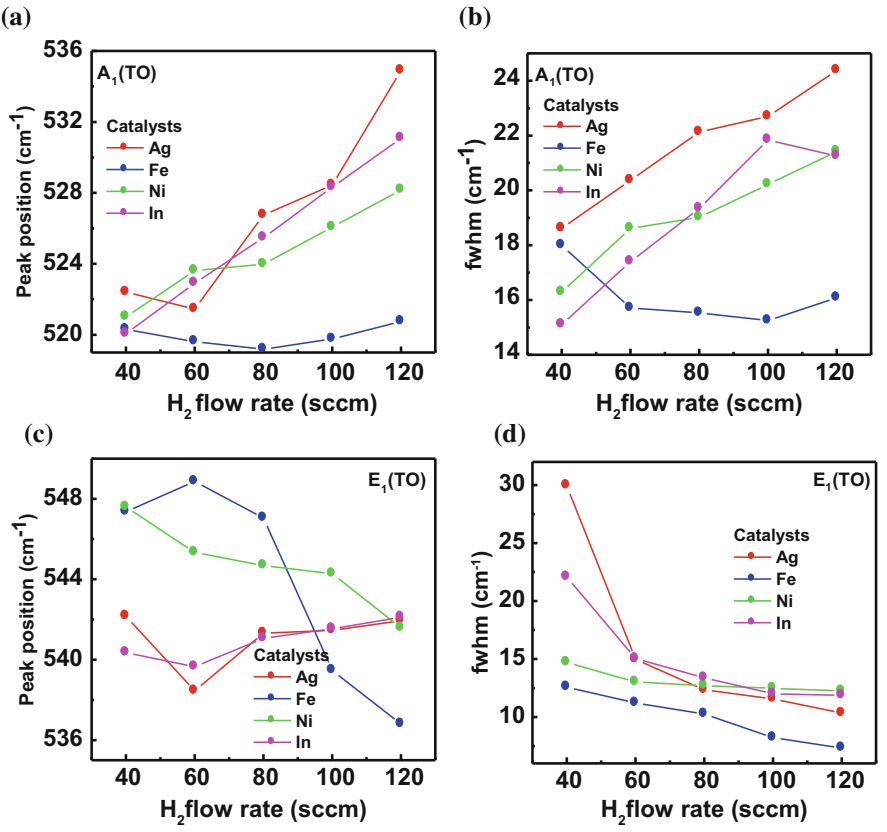


Fig. 4 Peak position, fwhm with increasing H_2 flow rates **a** A_1(TO) phonon, **b** E_1(TO) phonon of GaN-NWs synthesized using different catalyst

in the nanowires. On the other hand, peak position of A_1(TO) phonon of GaN-NWs grown by using In catalyst shifts from lower to higher wavenumber region (520.06–531.08 cm^{-1}) whereas their fwhm varies from 15.1 to 21.25 cm^{-1}. In a similar manner, Fig. 4c–d shows the behavior of E_1(TO) phonon of GaN-NWs grown by using different catalyst with increasing H_2 flow rate from 40 to 120 sccm. The E_1(TO) phonon peak position of Ag catalyst induced GaN-NWs shows slight shifts from 542.16 to 541.94 cm^{-1} whereas huge decrease in their fwhm was observed from 29.95 to 10.33 cm^{-1}. Similarly, E_1(TO) peak position of Fe assist GaN-NWs decreases sharply from 547.36 to 536.8 cm^{-1} and fwhm also decreases from 12.59 to 7.32 cm^{-1}. Further, if we consider Ni catalyst induced GaN-NWs, the peak position and fwhm decreases from 547.6 to 541.58 and 14.72 to 12.24 cm^{-1} respectively. Finally, we came to In catalyst assist GaN-NWs where the peak position of E_1(TO) phonon increases from 540.35 to 542.11 cm^{-1} and their respective fwhm decreases from 22.09 to 11.87 cm^{-1}.

3.4 Longitudinal Optic Phonon of GaN-NWs

Figure 5a–d shows peak position and fwhm of A_1(LO) and E_1(LO) phonons of GaN-NWs grown by using Ag, Fe, In and Ni catalysts. These plots are plotted by taking curve fitting data from Fig. 3a–d. Figure 5a shows the plot of A_1(LO) phonon peak position and fwhm with different H_2 flow rates. The A_1(LO) phonon peak position and fwhm of Ag assists GaN-NWs shifts from its lower value (704.84) to higher value (718.46) and fwhm increases from 12.62 to 21.14 cm^{-1} with increase of H_2 flow rate from 40 to 120 sccm. In as similar trend, A_1(LO) phonon peak position and fwhm of Fe assist GaN-NWs increases from 705.19 to 711.73 and 12.84 to 20.05 cm^{-1} respectively. Further, it was observed that the A_1(LO) phonon peak position and fwhm of Ni catalyst induced GaN-NWs also increased from 706.46 to 717.26 and fwhm (14.08–21.69 cm^{-1}). Lastly, it is observed that, peak position of A_1(LO) phonon of GaN-NWs grown by using In catalyst shifts from 705.02 to 718.88 cm^{-1} and their fwhm increases from 12.9 to 21.52 cm^{-1}. Similarly, Fig. 5b shows the plot of E_1(LO) phonon peak position and fwhm against different H_2 flow rates. The E_1(LO) phonon peak position of Ag catalyst induced GaN-NWs shifts from 721.11 to 729.94 cm^{-1} while their fwhm decrease abruptly from 18.47 to 13.52 cm^{-1}. Similarly, E_1(LO) phonon peak position of Fe assist GaN-NWs increases sharply from 721.19 to 725.41 cm^{-1} and their respective fwhm decreases slightly from 15.53 to 14.22 cm^{-1}. For Ni catalyst induced GaN-NWs, the peak position of E_1(LO) increases from 721.8 to 729.47 cm^{-1} whereas their fwhm decreases from 15.95 to 14.11 cm^{-1} respectively. Finally, for In catalyst assist GaN-NWs, it is observed that the peak position of E_1(LO) phonon increases from 721.14 to 729.96 cm^{-1} and their respective fwhm decreases from 15.89 to 13.32 cm^{-1}.

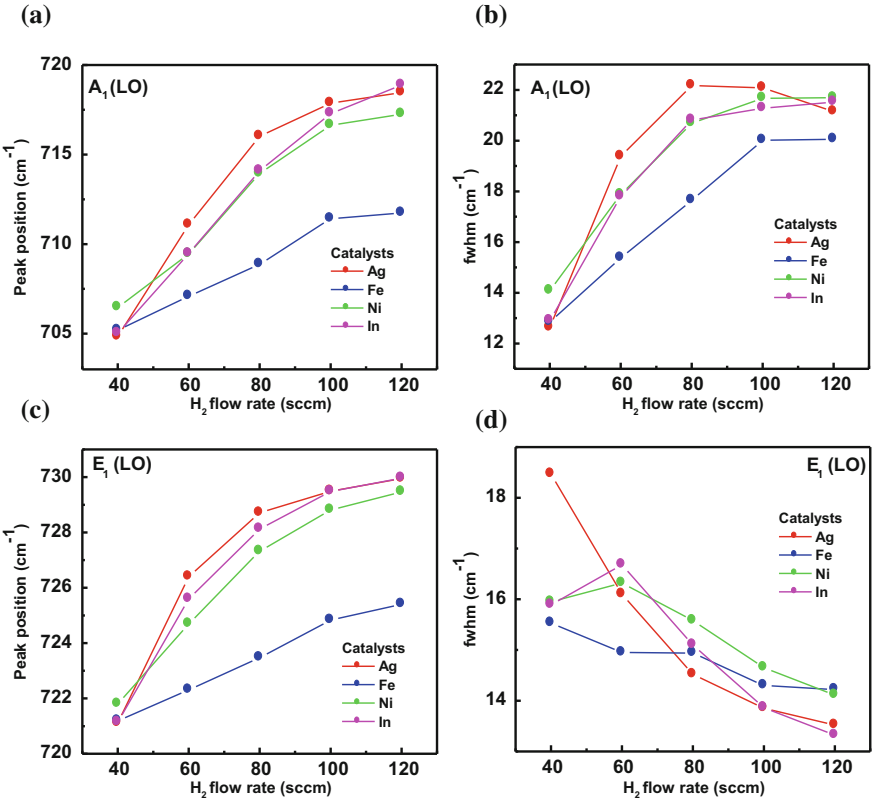


Fig. 5 Peak position, fwhm with increasing H_2 flow rates **a** A_1(LO) phonon, **b** E_1(LO) phonon of GaN-NWs grown by using different catalysts

3.5 E_2 (High) Phonon of GaN-NWs

Figure 6 shows the plot of peak position and fwhm with increasing H_2 flow rates of E_2(high) phonon of GaN-NWs. It is evident from the figure, the E_2(high) phonon peak position of Ag catalyst assist GaN-NWs shifted toward lower wavenumber region varies from 565.71 to 552.96 cm^{-1} and their fwhm increases sharply from 21 to 49.9 cm^{-1} with H_2 flow rates from 40 to 120 sccm. On the other hand, the E_2 (high) phonon peak position of Fe catalyst assist GaN-NWs shifted from lower to higher wavenumber region varies from 551.43 to 563.56 cm^{-1} and their respective fwhm decreases from 31.94 to 23.23 cm^{-1} with H_2 dilution. In a similar sideline, the E_2 (high) phonon peak position of Ni catalyst induced GaN-NWs shifts from its lower value (551.31 cm^{-1}) to higher value (560.97 cm^{-1}), whereas their fwhm

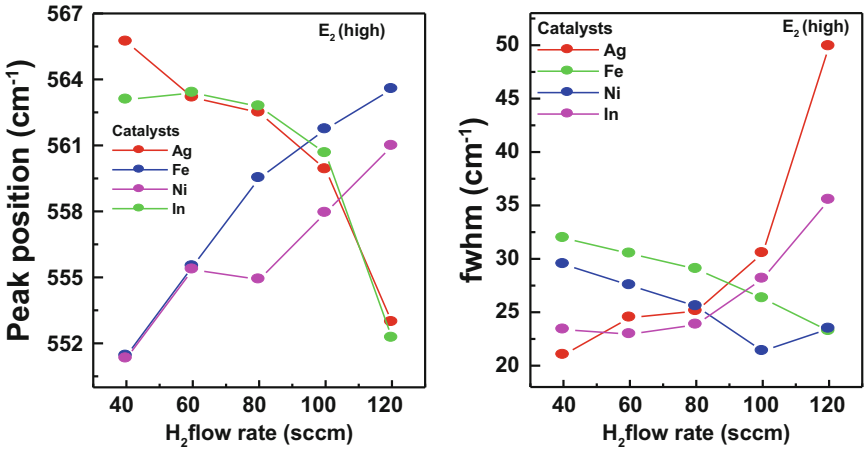


Fig. 6 Peak position, fwhm with increasing H_2 flow rates of E_2 (high) phonon of GaN-NWs

decreases from 29.49 to 23.46 cm^{-1} with H_2 flow rate from 40 to 120 sccm. Lastly, for In catalyst assist GaN-NWs the peak position of E_2 (high) phonon varies from 563.08 to 552.25 cm^{-1} and their fwhm increases from 23.38 to 35.51 cm^{-1} respectively.

3.6 FTIR Spectroscopy

Figure 7 shows the FTIR spectra of GaN-NWs in transmission mode. The major vibration signatures were observed in the range of 400–1400 cm^{-1}. The bonding signature of H_2 diluted GaN-NWs shows five distinguished vibrational bands. The vibrational band at 463 cm^{-1} corresponds to zone boundary phonons [23]. The vibrational signature at 566 cm^{-1} is corresponding to E_2 (high) with various groups [24]. The signature at 566 cm^{-1} generally appeared in the Raman spectra. However, we also observed in FTIR spectra of GaN-NWs. The vibration signature at 610 cm^{-1} is corresponding to Surface optic phonon of GaN-NWs [25]. The vibration signatures at 739 cm^{-1} corresponds to A_1(LO) of the GaN network [24], whereas the signature of 2 E_1(TO) appeared at 1100 cm^{-1} [26].

Figure 8 shows the deconvolution of FTIR spectra of GaN-NWs from 450 to 640 cm^{-1}. The spectra were deconvoluted into six Gaussian peaks taking peak position at 465.12, 500.01, 514.51, 569.14, 609.69 and 622.35 cm^{-1} corresponding to Zone boundary phonon, acoustic overtone, A_1(TO), E_2 (high), SO (A), SO (E) respectively [24]. With nickel and indium catalyst, the fwhm decreases while with Fe and Ag catalyst fwhm increases from 18.433 to 18.445 cm^{-1}. This gives us

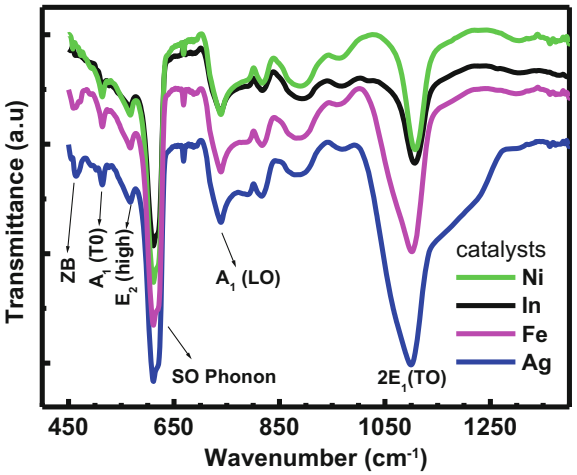


Fig. 7 Broad scan FTIR spectra of GaN-NWs grown in presence of different catalyst

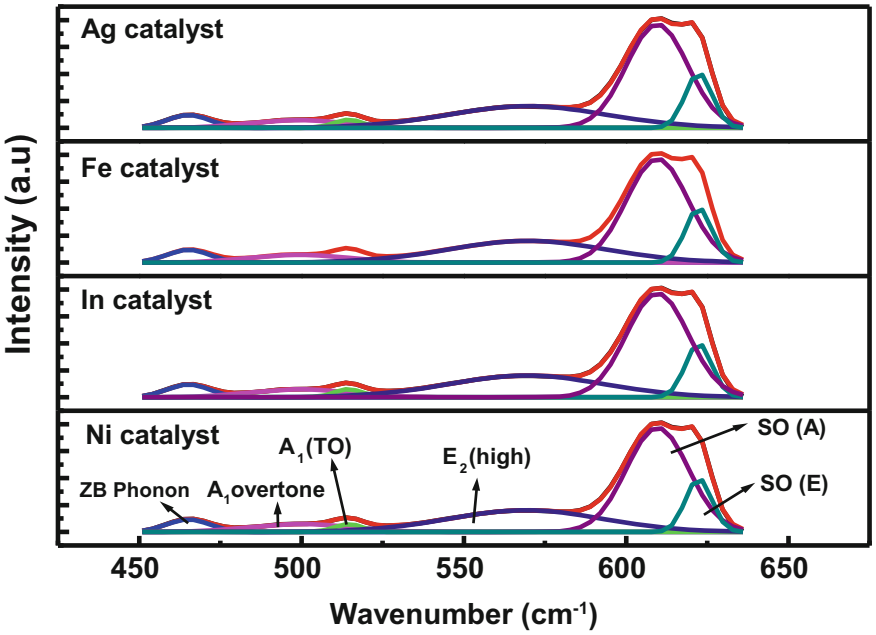


Fig. 8 Deconvolution of FTIR spectrum of the GaN-NWs from 450 to 640 cm^{-1} range

clear cut indication of increase of bonding attachment of Ga-N with different catalyst. Therefore, the selection of suitable catalyst may improve the microstructural and chemical network in GaN-NWs.

To clarify in detail, the LO peaks of GaN-NWs was further deconvoluted into two Gaussian peaks. Figure 9 shows the Gaussian fit of A_1(LO) and E_1(LO) Phonon peak centered at 734 and 768 cm^{-1}. The observed phonon peaks for the GaN-NWs broaden substantially. Within the experimental error, our results are agreed well with those of reported value for GaN bulk. We deconvoluted the LO peak into two Gaussian peaks. The broadening of A_1(LO) mode is due to the size effect [27]. The suppression of E_1(LO) and predominance of A_1(LO) phonon could be assigned to weak electron phonon coupling in case of A_1(LO) phonon. However, detail investigation is still needed to understand this peculiar behavior of phonon. The intensity of A_1(LO) peak decreases with different catalysts whereas its peak position does not show significant variation. The decrease of A_1(LO) phonon intensity with variation of catalyst reveals increase of defect concentration in vicinity of A_1(LO) phonon. However, the E_1(LO) peak shows significant shift in their position toward higher wavenumber. It is also observed that the intensity of E_1(LO) increases consistently. This shows that E_1(LO) phonon does not affected much by the presence of defect in the films whereas A_1(LO) phonon severely affected by presence of defects in the films [28].

Figure 10 shows the deconvolution FTIR spectra of GaN-NWs with four individual Gaussian peaks. The peak position $\sim$1057 cm^{-1} corresponding to Ga-N stretching referred to $2E_1$(TO). The vibration signature at 1106 cm^{-1} corresponds to Si–O–Si. The vibration signature at 1156 cm^{-1} corresponds to Ga–O–N. The vibrational signature at 1228 cm^{-1} corresponds to Ga–N=O. These refer to some oxygen present in GaN-NWs due to atmospheric CVD constrain. The Ga–O–N bond referred to interstitial oxygen present in the GaN-NWs, however, GaN=O bonding indicates surface oxygen present in the GaN-NWs.

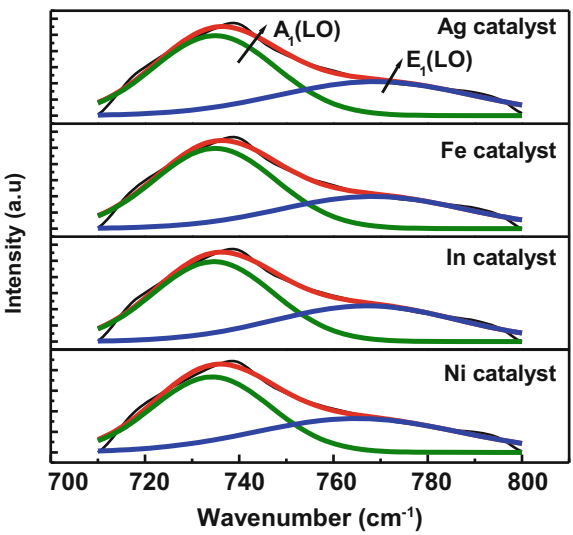


Fig. 9 Deconvolution of FTIR spectrum of the GaN-NWs from 710 to 800 cm^{-1}

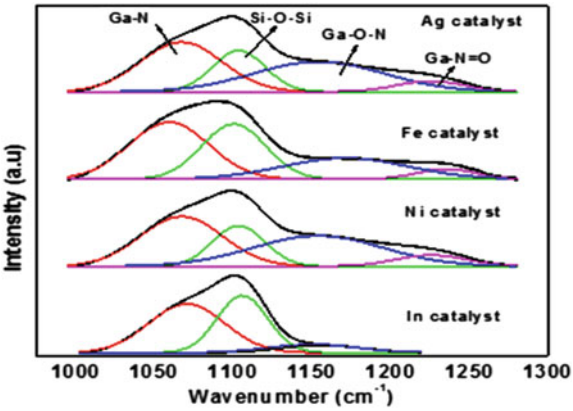


Fig. 10 Deconvolution of FTIR in the range from 1000 to 1300 cm^{-1} into four Gaussian peaks

3.7 Photoluminescence

Figure 11a shows room temperature PL spectra of GaN-NWs synthesized using different catalysts at 80 sccm H_2 flow rate. The excitation energy (3.87 eV) is higher than the bandgap energy of GaN, therefore these PL spectra provide us information about surface states of GaN-NWs. A very broad band ranging from 2.5 to 3.2 eV is observed. The broad band contains some fine emission peaks at 2.7, 2.85 and 2.96 eV respectively. Wu et al. also reported the presence of strong PL band at 2.85 and 2.95 eV of GaN-NWs grown using VLS catalyst [29]. However, it was observed that the shape of PL spectra gets changed with use of different catalyst. Hence, the detail investigation needs to be carried out to understand this effect. It is observed that, all spectra shows strong blue luminescence band at 2.96 eV. It is well evident that, GaN-NWs have large surface area with unsaturated dangling bonds, which are saturated by bonding with neighboring catalyst and H_2 atom. In addition to blue band, other defect related emission such as green band appears at 2.7 eV [30]. Moreover, incorporation of H_2 gas increases the vacancy concentration in the nanowires [31]. Here, we further noticed the appreciable reduction of band gap energy of GaN-NWs. The reduction of band gap energy could be attributed to effects such as strain, Stokes shift, and defect and impurity states. Figure 11b–e shows room temperature PL spectra of GaN-NWs synthesized using different catalysts at different excitation energy. Increasing the excitation energy will change the emission spectra. It is observed that the width of the PL peak increases significantly with rising excitation and it varies with different catalyst accordingly. This anomalous behavior could be due to excitation-induced dephasing [32].

Figure 12 shows the PL spectra of GaN-NWs synthesized using Ni as catalyst with different H_2 at fixed excitation wavelength of 350 nm. It shows the variation of emission band spectra due to different dilution rate of hydrogen gas. As the flow rate of H_2 increases the defect passivation increases. These passivated defects may substantially enhance the PL emission to the extent that would overwhelm the desired band gap fluorescence in GaN-NWs. The defect derived PL emission in

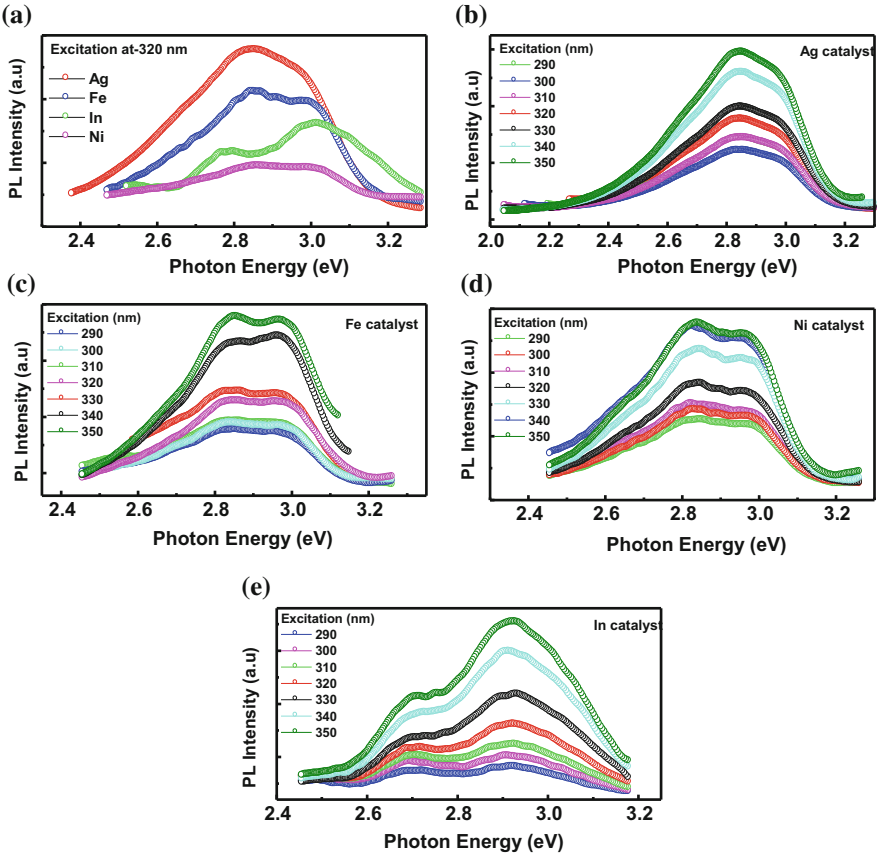


Fig. 11 Room temperature PL spectra of GaN-NWs synthesized using different catalysts at 80 sccm H_2 flow rate and different excitation energy

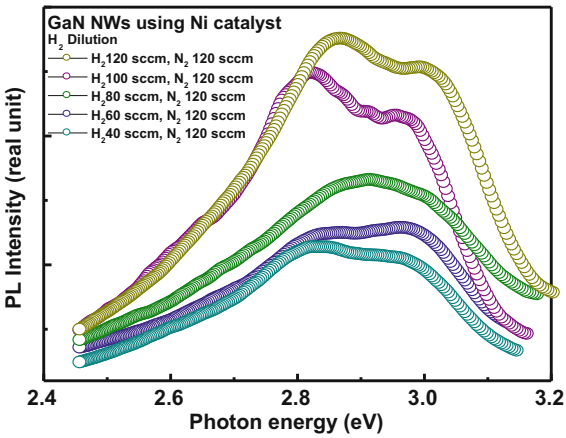


Fig. 12 Room-temperature photoluminescence spectra of GaN-NWs synthesized using Ni as catalyst with different H_2 flow rate

wide band gap semiconductor is generally bright and enhanced significantly when defects are effectively passivated [33].

4 Conclusion

In conclusion, we have studied microstructural, vibrational and optical properties of GaN-NW grown with different metal catalysts (Ag, Fe, Ni, In). We found that GaN-NWs grown via different catalyst, H_2 flow rate have different phononic behaviour and microstructure. This study revealed that catalyst plays vital role in deciding overall behavior of GaN-NWs. The adoption of a proper catalyst in the synthesis process provides a possible way to improve inherent material properties which are critical for their potential application in nanoscale optoelectronic devices. The red shift of E_1(TO) Phonon with different catalyst and increasing H_2 flow rate reveals dominancy of E_1(TO) phononic behavior, whereas blue shift of A_1(TO) phonon indicates stress and disorder in the surrounding environment of A_1(TO) phonon due to catalyst and H_2 incorporation. The room temperature PL spectra of GaN-NWs reveal prominent blue luminescence from catalyst assisted nanowires.

Acknowledgements This study was financially supported by the Department of Science and Technology (Project No: SB/FTP/ETA-295/2011) and Department of Biotechnology (Project No: BCIL/NER-BPMC/2012/650), Govt. of India. Umesh Rizal acknowledges financial support from JRF scheme under the Department of Biotechnology, Government of India.

References

1. Schafer, M., Gunther, M., Langer, C., Mubener, J., Feneberg, M., Uredat, P., Elm, M.T., Hille, P., Schormann, J., Teubert, J., Henning, T., Klar, P.J., Eickhoff, M.: Electrical transport properties of Ge-doped GaN nanowires. Nanotechnology **26**, 135704–135712 (2015)
2. Patsha, A., Amirthapandian, S., Pandian, R., Bera, S., Bhattacharya, A., Dhara, S.: Direct evidence of Mg incorporation pathway in vapor–liquid–solid grown p-type nonpolar GaN nanowires. J. Phys. Chem. **C 118**, 24165–24172 (2014)
3. Kuykendall, T., Pauzauskie, P., Lee, S., Zhang, Y., Goldberger, J., Yang, P.: Metalorganic chemical vapor deposition route to GaN nanowires with triangular cross sections. Nano Lett. **3**, 1063–1066 (2008)
4. Johnson, J.C., Choi, H.J., Knutsen, K.P., Schaller, R.D., Yang, P., Saykally, R.J.: Single gallium nitride nanowire lasers. Nat. Mater. **1**, 106–110 (2002)
5. Stach, E.A., Pauzauskie, P.J., Kuykendall, T., Goldberger, J., He, R.R., Yang, P.: Watching GaN nanowires grow. Nano Lett. **3**, 867–869 (2003).
6. Hong, J., Chang, Y., Ding, Y., Wang, Z.L., Snyder, R.L.: Growth of GaN films with controlled out-of-plane texture on Si wafers. Thin Solid Films **519**, 3608–3611 (2011)
7. Lee, D.S., Stekl, A.J.: Room-temperature grown rare-earth-doped GaN luminescence thin films. Appl. Phys. Lett. **79**, 1962–1964 (2001)
8. Biswas, S., Kar, S., Ghosal, T., Ashok, V.D., Chakrabarti, S., Chaudhuri, S.: Fabrication of GaN nanowires and nanoribbons by a catalyst assisted vapor–liquid–solid process. Mater. Res. Bull. **42**, 428–436 (2007)

9. Zhang, J., Zhang, L.: Growth of semiconductor gallium nitride nanowires with different catalysts. J. Vac. Sci. Technol. **B 21**, 2415–2419 (2003)
10. Wang, Y.Q., Wang, R.Z., Zhu, M.K., Wang, B.B., Yan, H.: Structure and surface effect of field emission from gallium nitride nanowires. Appl. Surf. Sci. **285**, 115–119 (2013)
11. Samanta, C., Chander, D.S., Ramkumar, J., Dhamodaran, S.: Catalyst and its diameter dependent growth kinetics of CVD grown GaN nanowires. Mater. Res. Bull. **47**, 952–956 (2012)
12. Ambacher, O., Angerer, H., Dimitrov, R., Rieger, W., Stutzmann, M., Dollinger, G., Bergmaier, A.: Hydrogen in gallium nitride grown by MOCVD. Physica Status Solidi **159**, 105–119 (1997)
13. Zhang, Y., Li, J.K., Liu, Q.L., Xiao, Y.G., Zhang, Q., Sun, B.J, Rao, G.H.: Phase relations of the Ag–Ga–N system. J. Alloys Compd. **429**, 184–188 (2007)
14. Cheeze, C., Geeldhar, L., Trampert, A., Brandt, O., Riechert, H.: Collector phase transitions during vapor−solid−solid nucleation of GaN nanowires. Nano Lett. **10**, 3426 (2010)
15. Okamoto, H.: Bull. Alloy. Phase Diagram **11**, 576–580 (1990)
16. Anderson, T.J., Ansara, I.: The Ga-In (gallium-indium) system. J. Phase Equilib. **12**, 64 (1991)
17. Cao, G.: Nanostructure and Nanomaterials: Synthesis, Properties and Applications. Imperial College Press (2004)
18. Tekker, K.: Density and morphology adjustments of gallium nitride nanowires. Appl. Surf. Sci. **283**, 1065 (2013)
19. Purushothaman, V., Jeganathan, K.: Investigations on the role of Ni-catalyst for the VLS growth of quasi-aligned GaN nanowires by chemical vapor deposition. J. Nanopart. Res. **15**, 1789 (2013)
20. Tang, W.C., Hong, F.C.N.: Growths of indium gallium nitride nanowires by plasma-assisted chemical vapor deposition. Thin Solid Films **570**, 315 (2014)
21. Wang, C., Chang, D., Tang, C., Su, J., Zhang, Y.: Single Adatom Adsorption and Diffusion on Fe Surfaces. J. Modern Phys. **2**, 1067 (2011)
22. Sun, R., Zhang, H.Y., Wang, G.G., Han, J.C., Zhu, C., Liu, X.P., Cui, L.: Selective growth and characterization of gallium nitride nanowires through an N-Ga2O3 layer. Ceram. Int. **40**, 13967 (2014)
23. Ji, H., Kuball, M., Burke, R.A., Redwing, J.M.: Vibrational and optical properties of GaN nanowires synthesized by Ni-assisted catalytic growth. Nanotechnology **18**, 445704 (2007)
24. Miyazaki, T., Takada, K., Adachi, S., Ohtsuka, K.: Properties of radio-frequency-sputter-deposited GaN films in a nitrogen/hydrogen mixed gas. J. Appl. Phys. **97**, 093516 (2005)
25. Shaoo, P., Dhara, S., Dash, S., Tyagi, A.K.: One dimensional GaN Nanostructures: Growth Kinetics and Applications, Nanosci. Nanotechnol Asia 2, 140 (2011)
26. Liu, H.L., Chen, C.C., Chia, C.T., Yeh, C.C., Chen, C.H., Yu, M.Y., Keller, S., Denbaars, S. P.: Infrared and Raman-scattering studies in single-crystalline GaN nanowires, Chem. Phys. Lett. **345**, 245 (2001)
27. Richter, H., Wang, Z.P., Ley, L.: The one phonon Raman spectrum in microcrystalline silicon Solid State Commun. **39**, 625 (1981)
28. Narayanamurthi, V.: Phonon optics and phonon propagation in semiconductors. Science **213**, 717 (1981)
29. Wu, Z., Hahm, M.G., Jung, Y.J., Menon, L.: Epitaxially grown GaN nanowire networks. J. Mat. Chem. **19**, 463 (2009)
30. Chang, K.W., Wu, J.J.: Low-Temperature catalytic synthesis of gallium nitride nanowires. J. Phys. Chem. B. **106**, 7796 (2002)
31. Kushwaha, A., Aslam, M.: Hydrogen-incorporated ZnO nanowire films: stable and high electrical conductivity. J. Phys. D Appl. Phys. **46**, 4851041–4851048 (2013)
32. Wang, H., Ferrio, K., Steel, D.G., Hu, Y.Z., Binder, R., Koch, S.W.: Transient nonlinear optical response from excitation induced dephasing in GaAs. Phys. Rev. Lett. **71**, 1261 (1993)
33. Cao, L., Meziani, M.J., Sahu, S., Sun, Y.P.: Photoluminescence properties of graphene versus other carbon nanomaterials. Acc. Chem. Res. **46**, 171 (2013)

Selection of an Electric Motor for an Equivalent Internal Combustion Engine by TOPSIS Method

K. Srihari, Parth Raval and Shabbiruddin

Abstract Selection of an electric motor (EM) for the electric car is a challenging task, selecting an improper motor may badly affect the company's production by reducing the feature of the manufactured goods, thereby reducing yield as well as cost-effectiveness. The efficient motor for a specified job is selected by considering several factors. The aim of the proposed paper is to show how, by means of a TOPSIS method, the authors are able to find out if the utilization of motors is aided in performance development as of a requirement view. The proposed technique helps to replace internal combustion (IC) engine with a suitable EM.

Keywords Technique for order preference by similarity to ideal solution method · Internal combustion engine · Electric motor

1 Introduction

Automotive EM is more powerful yet compact too. Proper selection of an EM for a vehicle is an essential duty, as inappropriate choice could disturb the performance of the vehicle. Actually, the propulsion system of a vehicle which mainly depends on these three factors: driver's prospect, vehicle restriction and energy basis. Considering this, it is flawless that the whole motor working idea is not resolutely distinct [1]. So, it is a puzzling job to select the best suitable propulsion system for an electric vehicle (EV). From a manufacturing viewpoint, the most important sorts of EMs adopted for EVs include the induction motor (IM), permanent magnet

K. Srihari (✉) · P. Raval (✉) · Shabbiruddin (✉)
Electrical & Electronics Engineering Department,
Sikkim Manipal Institute of Technology, Majhitar, Sikkim, India
e-mail: Shrihari.hari420@hotmail.com

P. Raval
e-mail: Parthraval31@yahoo.com

Shabbiruddin
e-mail: Shabbiruddin85@yahoo.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_7

motors (PM), dc motor, switched reluctance motor (SRM) and the synchronous motor (SM). Also, based on a complete evaluation of the factors associated with electric propulsion systems, it is detected that investigations on the cage IMs and the PM motors are vastly governing, while that on dc motors are reducing, and that on SRM are gaining ample importance [2, 3].

1.1 Electrical Vehicles

The demand for EVs is rising day by day as they have more advantage over a vehicle with an IC Engine. EVs are more desirable because of their low maintenance cost and running cost. The air pollution emitted by EV is negligible as compared to that of IC Engine Vehicle. Other than this the drivability of EV's is more convenient than that of IC Engine Vehicles. This is due to the availability of the maximum torque from the zero RPM itself. In order to meet the performance norms of standard vehicles, a perfect EM among the various kinds of EM should be selected. Choosing a suitable motor among similar kind of motors is very difficult. Therefore it is necessary to compare the performance characteristics in a suitable manner. Some of the main parameters which affect the performance of an EV are voltage rating (V), current rating (I), torque (τ), power (P), RPM, weight of motor, which are usually known parameters. Other than these known parameters, selection of gearbox for an individual motor also plays an important role in the performance and efficiency of the electric vehicle. The gearbox specification of each motor is mentioned at appendix. There are various kinds of motors which can be used as power train in an EV, but here we choose two kinds of Series Wound DC Motors and two kinds of 3-phase AC Induction Motors, as they have good starting torque.

1.2 Series Wound DC Motor

These are the EMs where the field current and the armature current are same. Neglecting saturation reaction, the central flux ϕ is proportional to the armature current. They have high torque as the torque of the series wound DC motor directly depends on the square of the armature current. So, for higher values, the torque curve remains as a straight line. This leads to its advantage, as they have the high torque at low current, they are better for their acceleration when used in EV. These motors are powering up the local electric trains in Mumbai, India.

1.3 Three Phase AC Induction Motor

These are the motors which are mostly used for heavy applications. The three phase stator winding have the three phase current which produces a rotating magnetic

field [4]. In the case of a rotor, the three phases are short-circuited. This short-circuited circuit induces an e.m.f. which gives rise to current in rotor conductors. The interaction of the rotor currents with rotational flux wave creates torque in the rotor of a three-phase induction motor and as a consequence, rotor begins to rotate [5]. The structure of the three phase AC induction motor is simple. Other than this, they have self-starting torque unlike SM, they do not require any special starting techniques.

2 Proposed Methodology

TOPSIS (Technique for Order Preference by Similarity to Ideal Solution)
The TOPSIS methodology is applied in a total of six steps as follows:

Step 1: Firstly, we find the normalized decision matrix. The normalized value a_{ij} is found as shown below:

$$a_{ij} = b_{ij} \sqrt{\sum_{i-1}^{y} b_{ij}^2} \quad i = 1, 2, \ldots, y \quad \text{and} \quad j = 1, 2, \ldots, z.$$

Step 2: Now we find the weighted normalized decision matrix. The equation for calculating the weighted standardized value c_{ij} is given below:

$$c_{ij} = a_{ij} \times d_j \quad i = 1, 2, \ldots, y \quad \text{and} \quad j = 1, 2, \ldots, z. \tag{1}$$

The term d_j is the weight of the jth criterion and $\sum_{j=1}^{z} d_j = 1$.

Step 3: Now we find the positive ideal (E^*) and negative ideal (E^-) solutions as shown below:

$$E^* = \left\{ \left(\max_i c_{ij} | j \in F_b \right), \left(\min_i c_{ij} | j \in F_c \right) \right\} = \left\{ c_j^* | j = 1, 2, \ldots, y \right\} \tag{2}$$

$$E^- = \left\{ \left(\min_i c_{ij} | j \in F_b \right), \left(\max_i c_{ij} | j \in F_c \right) \right\} = \left\{ c_j^- | j = 1, 2, \ldots, y \right\} \tag{3}$$

Step 4: Now with the help of y-dimensional Euclidean distance we find the separation measures. The separation measures of the positive ideal answer and the negative ideal answer for the entire alternative, respectively, are shown below:

$$H_i^* = \sqrt{\left(\sum_{j=1}^{y} \left(c_{ij} - c_j^* \right)^2, j = 1, 2, \ldots, y \right)} \tag{4}$$

$$H_i^- = \sqrt{\left(\sum_{j=1}^{y}\left(c_{ij} - c_j^-\right)^2, j = 1, 2, \ldots, y\right)} \quad (5)$$

Step 5: Now in order to find the relative closeness to the perfect solution, the relative nearness of the alternative E_i with respect to E^* is as shown below:

$$\mathrm{RK}_i^* = \frac{H_i^-}{H_i^* + H_i^-}, \quad i = 1, 2, \ldots, y \quad (6)$$

Step 6: Now the preference order is listed out.

3 Case Study

We have taken the four EMs X1, X2, X3, X4 with the voltage rating (V), current rating (I), torque (τ), power (P), RPM, weight and cost as the parameters.

Now a person wants to change the 6-year-old Swift VDi car into an equivalent electrical vehicle. He/She desires the performance parameters to be similar as his/her standard vehicle.

Engine	V	I	τ	P	RPM	Weight	Cost

Engine	τ (nm)	P (HP)	RPM	Weight (kg)
Fiat 1.3 L	190	55.2	4000	140

The std. specification of Swift VDi Engine is as below:

Step 1: The Decision Matrix of selected EM is as follows [6, 7]:
where,

X1 Kostov DC K11″ 250 V SFM
X2 Kostov DC 11HV 288 V
X3 HPEV AC 34 × 2
X4 HPEV AC 50

Step 2: The Normalized Matrix is as follows:

Engine	V	I	τ	P	RPM	Weight	Cost
X1	250	210	77	44.8	5550	81	2500
X2	288	225	70	55	7600	103	3500
X3	48	650	264.77	64.18	1750	68	7230
X4	48	650	162.69	52.966	1150	53	3395

Step 3: Here we are taking weight ratios as follows:

Engine	V	I	τ	P	RPM	Weight	Cost
X1	0.6453	0.2166	0.2349	0.4097	0.5756	0.5164	0.2755
X2	0.7434	0.2321	0.2136	0.5030	0.7883	0.6566	0.3858
X3	0.1239	0.6705	0.8079	0.5869	0.1815	0.4335	0.7969
X4	0.1239	0.6705	0.4964	0.4844	0.1192	0.3379	0.3742

Torque (τ) = 0.3, Power (P) = 0.2 and V = I = RPM = Weight = Cost = 0.1
The Weighted Matrix is as follows:

Engine	V	I	τ	P	RPM	Weight	Cost
X1	0.06453	0.02166	0.07047	0.08194	0.05756	0.05164	0.02755
X2	0.07434	0.02321	0.06408	0.1006	0.07883	0.06566	0.03858
X3	0.01239	0.06705	0.2423	0.1173	0.01815	0.04335	0.07969
X4	0.01239	0.06705	0.1489	0.09688	0.01192	0.03379	0.03742

Step 4: Now we are taking positive and negative parameters:

P^+	V	I	τ	P	RPM	Weight	Cost
E^+	0.07434	0.06705	0.2423	0.1173	0.07883	0.06566	0.07969

P^-	V	I	τ	P	RPM	Weight	Cost
E^-	0.01239	0.02166	0.06408	0.08194	0.01192	0.03379	0.02755

Step 5: The value of H^+ is as follows:

$$H_1^+ = 0.2379 \quad H_2^+ = 0.1888$$

$$H_3^+ = 0.08954 \quad H_4^+ = 0.1423$$

Step 6: Similarly we will get the value of H^-:

$$H_1^- = 0.2436 \quad H_2^- = 0.05392$$

$$H_3^- = 0.1832 \quad H_4^- = 0.0984$$

Step 7: Now we will take the value of RK_i to obtain the optimum electric motor:

$$\mathrm{RK}_1 = \left\{H_1^-/(F)\right\} = 0.5059 \quad \mathrm{RK}_2 = \left\{H_2^-/(F)\right\} = 0.2221$$

$$\mathrm{RK}_3 = \left\{H_3^-/(F)\right\} = 0.6717 \quad \mathrm{RK}_4 = \left\{H_4^-/(F)\right\} = 0.4088.$$

4 Result

Ranking of EMs after applying TOPSIS method are: X3 > X1 > X4 > X2. Thus X3 (HPEV AC 34 × 2) is the optimum electric motor.

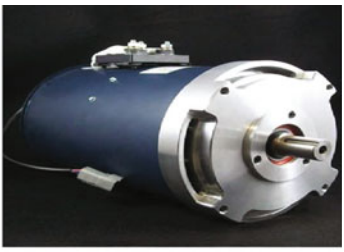
5 Discussion and Conclusion

The projected methodology is the selection, made under the safe bet of the provided statistics. In reality, the accessible data is extremely unclear unlike the ideal assumptions and even sometimes it may be under risk comprising many groups and huge investments, etc. associated with it. Choosing an appropriate electric motor (EM) from desired perspective is really a composite job which involves a separate decision-making, as it comprises many groups and a huge investment. Thus the proper plan and strategy for the evaluation is important for the selection. In this paper we have tried to show the effectiveness of the proposed methodology. TOPSIS method is applied for the selection of electric motor. An attempt is made to select an effective motor which is more beneficial than using a stock IC engine. So here we have selected four different motors whose performance characteristics are similar to FIAT 1.3L DDiS Engine. The result shows HPEV AC 34 × 2 is the most suitable motor for replacing the internal combustion (IC) engine in swift VDi.

Appendix

Images of the Selected Four Motors

(1) KOSTOV DC K11 250V SFM



(2) HPEV AC 50

(3) KOSTOV DC 11 HV 288V

(4) HPEV AC 34X2

Suitable Controllers
For HPEV AC 50 and HPEV 34 × 2
1238-5601 (48 V, 650 A)
1238-6501 (72 V, 550 A)
For KOSTOV DC K11 250V SFM and KOSTOV DC 11 HV 288V:
Soliton JR by EVnetics
Soliton 1 by EVnetics

Suitable Batteries

Lithium batteries are preferable for EVs but voltage developed by the individual battery is very less, so many batteries are combined together to get desired voltage. Power Japan is one of the best manufacturers of such batteries. Even KOSTOV motors offer such kind of batteries for EVs.

Gearbox Designing

It is better to introduce gearbox in order to meet the performance parameters of stock IC vehicles. Usually, it is preferred to design in such a way that:

i. In first gear, it is required to meet the acceleration norms of IC vehicles. So it is designed considering the high torque.
ii. In second gear it is required to reach the maximum speed as that of stock IC vehicles. So here we consider the maximum RPM of the wheel to be obtained to reach the top speed.
iii. As the vehicle reaches its top speed (where no more acceleration required), it is better to design a gear such that the motor would be able to keep up the constant speed of the vehicle at its optimum RPM. This is helpful in reducing the losses and hence results in raising the maximum range of the distance.

References

1. Rahman, Z., et al.: An examination of electric motor drive characteristics for EV and EV propulsion systems. Presented at the SAE Technical Paper Series, Paper# 2000-01-3062 (2000)
2. Chan, C.C.: The state of the art of electric and hybrid vehicles. Proc. IEEE **90**(2), 247–275 (2002)
3. Rajashekara, K.: History of electric vehicles in general motors. IEEE Trans. Ind. Appl. **30**(4), 897–904 (1994)
4. Singh, A.K.: Analysis of induction motor for electric vehicle application based on drive cycle analysis. In: Presented at 2014 IEEE Conference on PEDES (2014)
5. Electrical Machinery by P.S. Bhimbra. Khanna Publication (1 January 2011)
6. HPEV Catalog: (a) Link: hpves.com/catalog-ac-50.htm (For HPEV AC 50 motor), (b) Link: hpevs.com/catalog-ac-35x2.htm (For HPEV AC 34 $\times$ 2 motor)
7. KOSTOV Catalog: (a) Link: kostov-motors.com/files/compare.pdf (For KOSTOV DC K11 250V SFM and KOSTOV DC 11 HV 288V). (b) Link: kostovmotors.com/tractionmotors/kostovevmotors(acdc)/lithiumbatteriesbmsandchargers/ (For batteries)

Analysis of Medium Voltage BTB System by Using Half Bridge Modular Multilevel Converter Topology

Yasmeena and G. Tulasi Ram Das

Abstract The modular multilevel converter topology (MMC) became potential converter topology for various high power applications. These are high voltage DC power transmission and other intertie connections of renewable energy sources to grid. The other application of MMC topology is variable speed drives, for controlling these variable speed drives a sine wave technique and square wave technique will be used. Particularly for high voltage direct current (HVDC) transmission applications, modular topology of voltage source converter gained attention because of its modularity, uniform modules connected in series or parallel. The other considerable advantage of MMC is their high efficiency because of low losses and the filtering requirements for harmonics are very less compared to other topologies. MMC gives increasing converter reliability and reduction of maintenance cost. This paper gives the simulation study of design of 50 Hz BTB system with 200 V and 10 kW. Two MMC-based converters connected back to back and control signals generated by using phase-shifted modulation. The main advantage of this DSC–MMC-based BTB intertie is the DC link capacitor and sensor for voltage is eliminated. The simulation study carried out for the DSC-based MMC for a 200 V, 10 kW, 50 Hz model with phase-shifted PWM. Simulation results of DSC–MMC-based BTB study and transient states are presented in this paper. Simulation carried by using MATLAB/Simulink software.

Keywords MMC topology · HVDC transmission · BTB link · Half bridge MMC

Yasmeena (✉)
EEE Department, VIT Bhimavaram, Vishnupur, AP, India
e-mail: yasminab4u@gmail.com

G. Tulasi Ram Das
Jawaharlal Nehru Technological University Hyderabad, Hyderabad, India

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_8

1 Introduction

From 1990s voltage source converters became popular for high voltage DC transmission applications. The IGBT (Gate Bipolar transistors) device is the revalorized HVDC transmission system. The VSC-based HVDC system is advantageous because it reduces the cost of filtering elements. The VSC-based HVDC system space requirement is less, the compactness of this topology gives the flexibility to install HVDC station at utilization side. The VSC-based HVDC Transmission system is faster for active and reactive power control. VSC-based HVDC is most suitable for industrial applications because of its nature of constant voltage and frequency at output. In VSC-based HVDC transmission system the grid fluctuations may not create the disturbances in output side or industrial connections if proper controlling is provided for VSC-based HVDC system. MMC is the most attractive topology for HVDC transmission application due to its ability of low harmonic content in output at high voltage ranges. The switching frequency of MMC is also less because of low voltage rating of sub-module components.

In MMC sub-modules connected in series or parallel for its requirements. There are two types of MMC models for HVDC applications.

(i) Half bridge MMC model
(ii) Full Bridge MMC model

Figures 1 and 2 show the diagram of half bridge chopper cell of modular multi level converter. The electromagnetic transient modelling of MMC is modelled by Dommel trapezoidal method. In this method when voltage of sub-module capacitor is more than line voltage that is the peak value the capacitor will not consider the current flow in a particular arm. The basic difference between HVDC system and BTB system is for HVDC the both MMCs connected to different controlling unit where as in BTB both are connected to same controlling unit. In this paper a half bridge cell (HBC) MMC model used for the back to back intertie. The basic difference for long distance HBC-MMC-based system and BTB system is DC link voltage for HVDC system DC link voltage for the HVDC system is 250–500 kV. The reason behind it is to reduce the conducting power losses. The DC link voltage for BTB link is 66 or 132 kV. In this paper a 200 V, 10 kW, 50 Hz DSC–MMC-based BTB system simulated by using MATLAB simulink model and also the control system designed which controls the regulating DC link voltage and controlling DC link current. The main advantage of BTB is auxiliary DC voltage balancing circuit or start up circuit of chopper cells is not required. It will reduce the cost of the BTB transmission system. Harmonic filtres are not required for BTB system because of its sinusoidal system of output. Increased leakage inductance of galvanic transformer acts as filtre. The DC link capacitor is not required so, the cost of the capacitor can be eliminated. Due to indirect feedback control loop, indirect feedback control is not required.

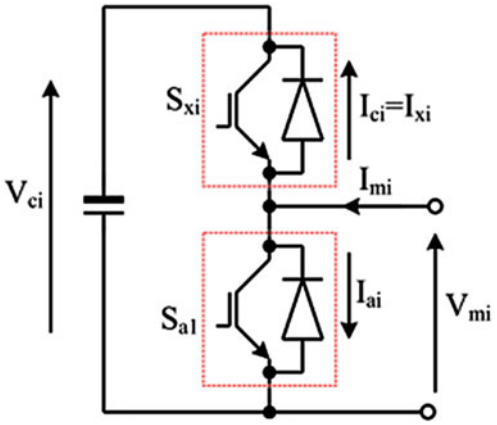


Fig. 1 Half bridge model of MMC sub-module

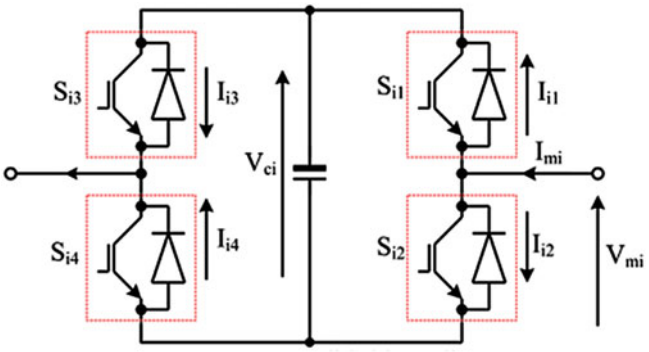


Fig. 2 Full bridge model of MMC sub-module

1.1 Back to Back HVDC Systems in India and Configuration of BTB System

For High power and long distance BTB systems can be used. In India two BTB Systems are commissioned. The details of BTB systems in India is given in Table 1. Vindhyachal BTB station provides power to north and west regions of India. Diversion of load can be done by using this BTB station between north and west regions of India at high demands of power. The length of BTB vindhyachal station is 1.05 km. The second commercial station is Chandrapur BTB station.

A 200 V, 10 kW, Half Bridge MMC Topology-based (HB–MMC-based) BTB system with power frequency range of 50 Hz is simulated by using MATLAB/simulink software. A phase-shifted modulation is used for the BTB system. For phase-shifted modulation a 450 Hz triangular carrier wave is used. Figure 3 shows the block diagram for HBC–MMC-based BTB.

Table 1 BTB systems in India

BTB name	Vindhyachal BTB station	Chandrapur BTB station
Connection between	Vindhyachal Super Thermal Station–Singrauli Super Thermal Power Stations	400 kV network Western region to Southern region Thermal Power Stations in Indian Grid (Chandrapur to Ramagundam stations)
Connection between regions	Northern to western region	Western to Sothern region
Commissioned date	April 1989	November 1993
Power rating	2 × 250 MW	2 × 500
No of poles	2	2
AC (V)	400 kV	400 kV
DC (V)	+70 kV	205 kV
Converter transformer (MVA)	8 × 156 MVA	12 × 234 MVA

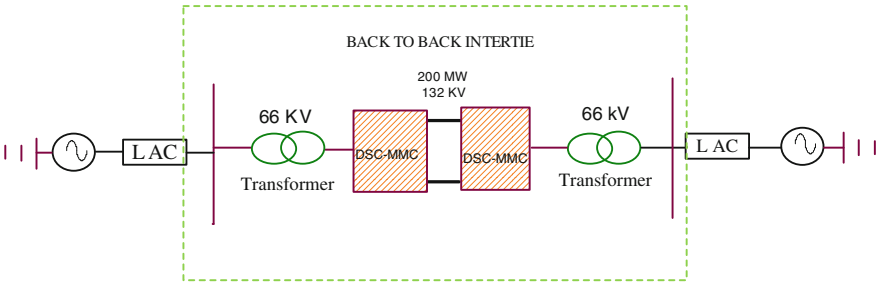


Fig. 3 Block diagram for circuit configuration of HBC–MMC-based BTB for 200 MW 132 kV system

2 Control Circuit of HBC–BTB System

The MMC controllers for the BTB intertie can be described as general voltage control, DC link voltage control, sub-module capacitor voltage control and circulating current control. The basic VSC control contains real power and reactive power control. SM capacitor voltage control can be classified as overall control and balancing between the sub-modules. The Current control block will take care of elimination of circulating current and elimination of zero sequence current.

2.1 Real Power and Reactive Power Control

Real and Reactive power control is done as convention abc to dq conversion as in case of normal VSC control circuit. The reference values of real power and reactive power will be given to control circuit. By referring the set points, the actual active and reactive power values are corrected by generating the respective firing signals. The block diagram of real and reactive power control is shown in Fig. 4.

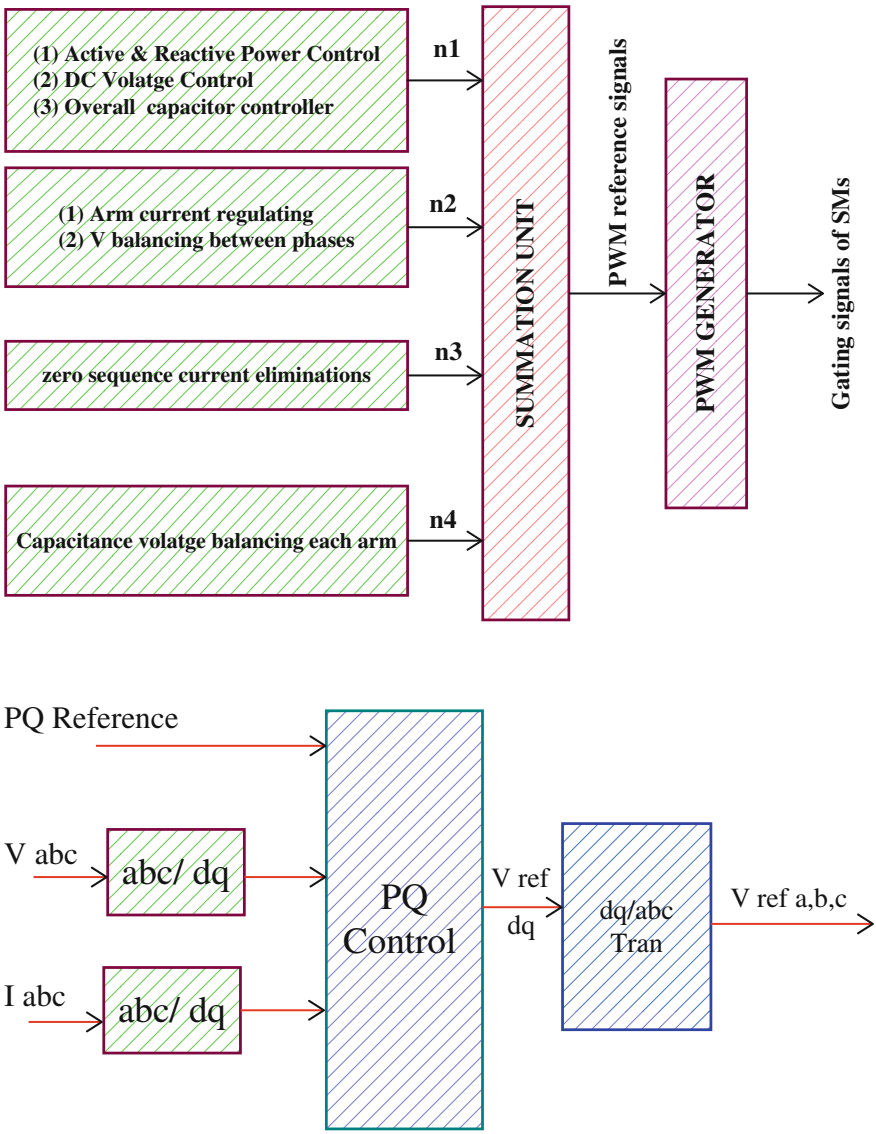


Fig. 4 Active and reactive power control by DQ transformation

2.2 DC Link Voltage Balancing Control

In General Topologies, if the DC link capacitor exists then the DC link voltage control can be done by using active power controlling. But in this type of BTB system the DC link capacitor is not present, so direct controlling of DC link voltage can be done by adding the upper and lower arm total voltage values according to condition. This process is very fast by using digital control system, the circuit diagram for DC link voltage is shown in Fig. 5.

$$V_{\mathrm{dc}} = \sum \left(N_i * V_{\mathrm{cap}-i}\right) + V_{\mathrm{up}-u} \tag{1}$$

$$V_{\mathrm{dc}} = \sum \left(N_i * V_{\mathrm{cap}-i}\right) + V_{\mathrm{low}-u}. \tag{2}$$

2.3 Arm Current Regulating

The upper arm and lower arm contribute equal phase current, the zero sequence component is eliminated. The equation gives the DC link currents. Figure 6 gives the arm current regulating block diagram.

$$i_{\mathrm{dc}-u} = \left(i_{\mathrm{up\ ac}-u} + i_{\mathrm{low\ ac}-u}\right)/2 - i_{\mathrm{circulating}-u} \quad \text{where } u = a, b \text{ or } c. \tag{3}$$

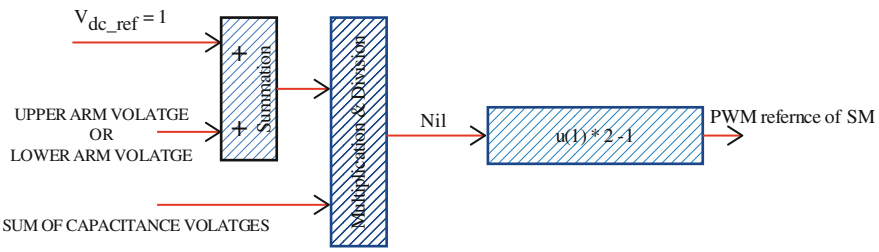


Fig. 5 DC link voltage control unit

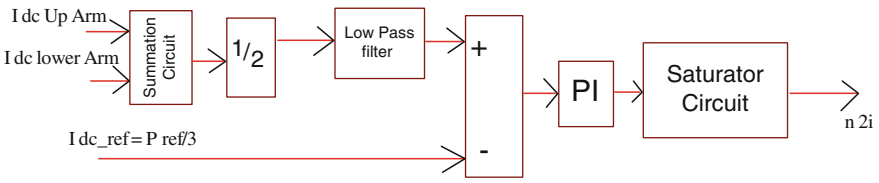


Fig. 6 Arm current control block diagram

The DC component of arm current should be equal among three phases, so the equation for on is the no circulating current is

$$\left(i_{\text{up ac}-u} + i_{\text{low ac}-u}\right)/2 = i_{\text{dc}-u}/3 \tag{4}$$

2.4 Control Circuit for Eliminating Zero Sequence (z_0) Current

The equation for the z_0 is obtained from the difference between positive and negative DC currents. When MMC is connected to star delta transformer z_0 is equal to zero. But if it is star with ground connection the z_0 will exists. The control diagram for zero sequence current is shown in Fig. 7. The eliminating is done by equating positive and negative DC link should be equal. When Upper arm current exists a negative deviation will be added to balance it and vice versa.

$$I_0 = I_a + I_b + I_c = I_{\text{dc}+} - I_{\text{dc}-}. \tag{5}$$

2.5 Sub-Module Capacitor Voltage Control

The sub-module capacitor voltage depends upon the energy stored in all capacitors. When the average voltage of all capacitors is higher than reference value a positive P ref added to the average value. Thus required power will be supplied to grid, but DC link power flow remains constant. So the voltage of capacitor will be reducing.

2.6 Capacitor Voltage Balancing Circuit

The MMC capacitor voltage is balanced in three steps:

1. Balancing capacitor voltage in each arm done by increasing the charging time depending upon the arm current, when arm current is positive capacitor voltage is shifted to more charging.

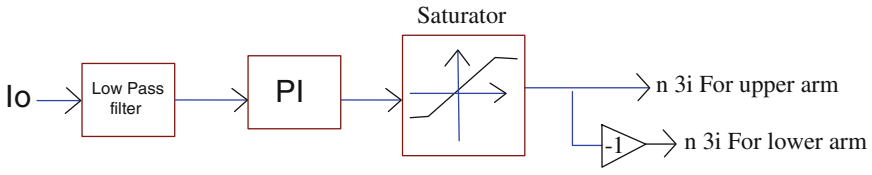


Fig. 7 Control block for zero sequence loop

2. Capacitive voltage value balancing can be achieved by giving additional DC value to the reference of control.
3. The upper and lower arms can be balanced by addition of phase shift angle to the reference voltage.

3 Parameter Selection of MMC for BTB Interties Application

Parameter selection of MMC means selection of arm inductance and capacitor selection.

3.1 Arm Inductance Selection of MMC

The arm inductor L_{armin} reduces the high frequency components of arm currents. The reason for high frequency arm currents is difference existence in upper and lower arm voltages. The main cause of this upper and lower arm currents are by switching time differences. Arm inductance can depend upon the sub-module individual capacitor voltage and modulation technique.

$$L_{\text{arms}} c_{\text{armr}} = C_{\text{arm}} = \frac{1}{C_{\text{arm}}\omega^2} \frac{2(h^2-1)+m_a^2 h^2}{8h}. \tag{6}$$

4 Phase-Shifted Modulation for HBC–MMC-Based BTB System

Different modulation strategies are therefor MMC-based BTB system, the main two systems are carrier-based and sorting-based algorithms. In this paper phase-shifted modulation technique is used to do the simulation and Fig. 8 gives the phase-shifted modulation block diagram. By using phase-shifted modulation, individual controllability is possible.

Figure 9 gives the block diagram for phase-shifted modulation and waveform models. The reference signal projected upon carrier signal and the carrier signal frequency is 450 Hz for HB–MMC-based BTB system control. When reference signal is more than the carrier wave the firing signal generated so that it connect the particular sub-module capacitor in circuit. If n is the number of sub-modules then phase shift must be $2\pi/n$, this phase shift will reduce harmonic in the output voltage.

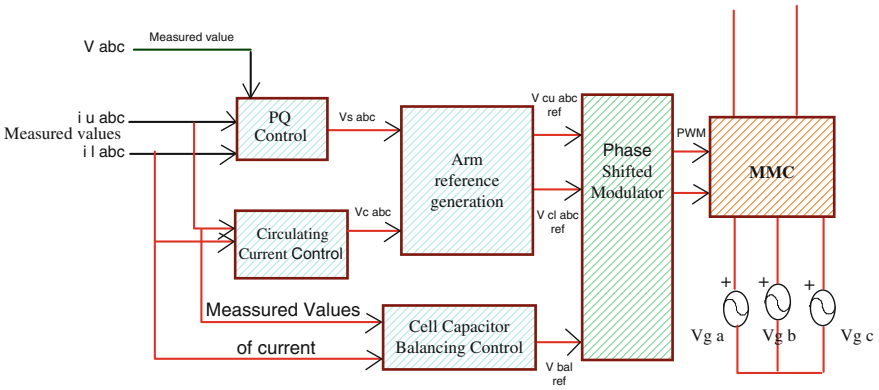


Fig. 8 Phase-shifted modulation block diagram

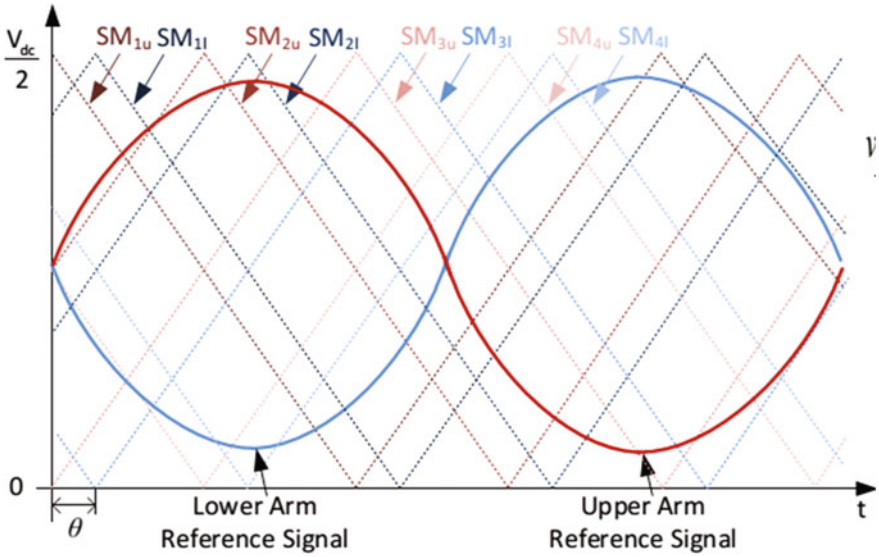


Fig. 9 Wave form for phase-shifted modulation

The circulating current depends upon the sub-module capacitor voltages. The control circuit gives the difference between actual voltage of sub-module capacitor reference voltages and actual capacitor voltages. The charging of capacitor indicated by positive sign and discharging is defined by negative sign. In circulating current adjustment proportional controller is used. Phase-switched Carrier PWM needs a voltage balancing loop for the sub-modules. The balancing of capacitor voltage possible by finding the capacitor with high voltage in discharging mode and low voltage sub-module capacitor in charging mode.

Extra switching losses occur in this intrinsic balancing mode when some SMs discharge slightly below average voltage level, they are exchanged with another modules with higher charge. Switching losses can be set to point known as tolerance band, for phase-shifted modulation the tolerance band is 10%. This tolerance method is known as Capacitor Ripple Control method. So, phase-shifted carrier method with capacitor ripple control is very advantageous with high sampling frequency.

5 Simulation Model of BTB System

The three conditions simulated by using Matlab2009a software. The active power is 8.7 kW and reactive power is −5.0 kVA. The BTB simulated in steady state condition, transient condition and with small step change in active power from 8–10 kW. A 15 kVA, 200 V transformer is connected to BTB in simulation model. The reactive power for B block is +5 kVA and apparent power is 10 kW (Fig. 10).

Figures 11, 12, 13, 14 and 15 show the steady state waveforms simulation study of BTB system.

The current in HBC-A leads by 30° to phase voltage of supply and in second HBC–MMC the supply voltage leads supply current by 150°.

The simulated waveforms of DSCC-B are shown from Figs. 16, 17, 18, 19, 20 when it is in inverter mode active power $p^* = 8.7$ kW and reactive power $q\mathrm{B}^* = 5$ kvar.

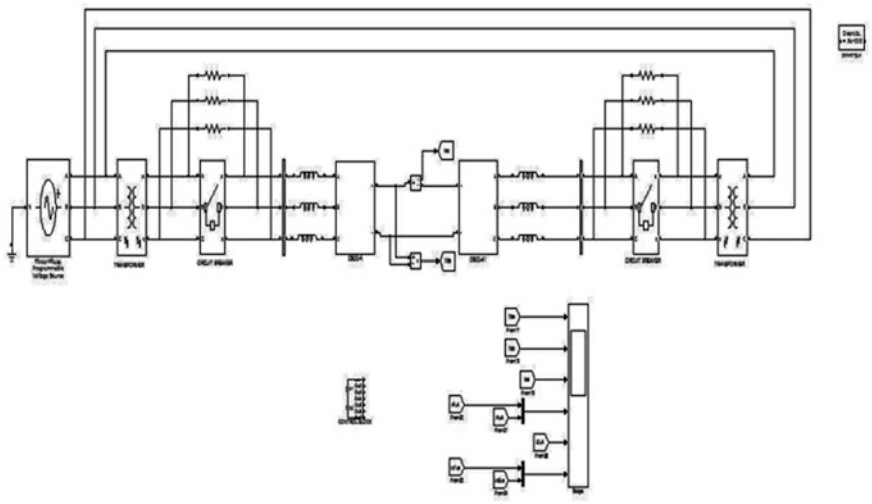


Fig. 10 Simulation circuit of HBC–MMC-based BTB system

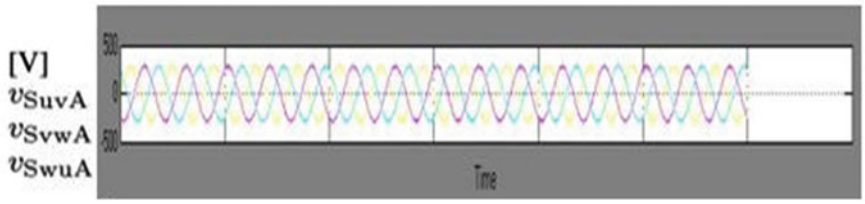


Fig. 11 3-ø voltage source

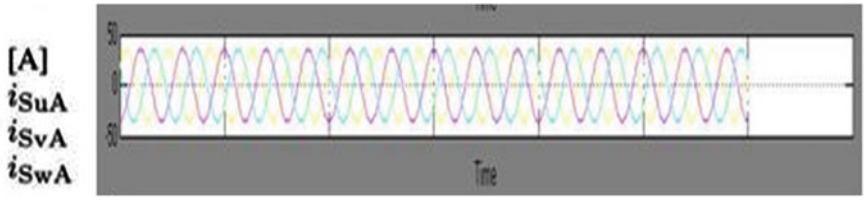


Fig. 12 Supply current

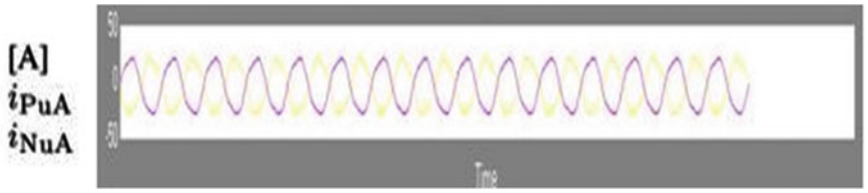


Fig. 13 Positive and negative arm currents

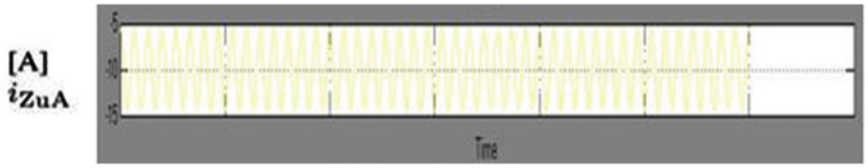


Fig. 14 Circulating current

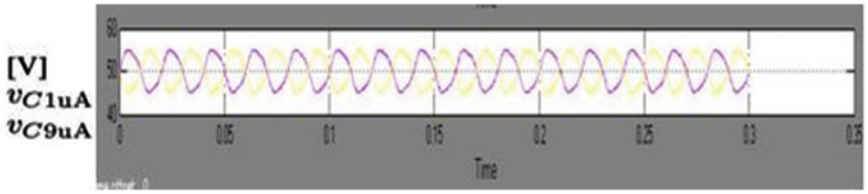


Fig. 15 Voltage across capacitors 1 and 9

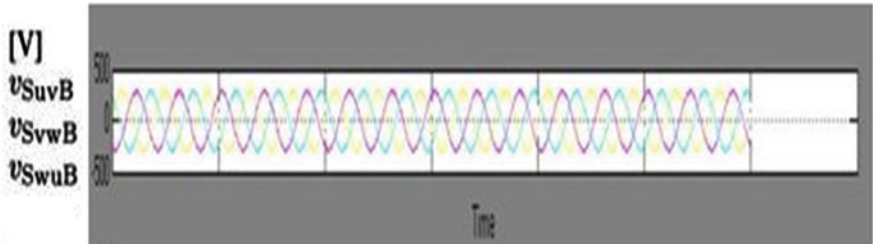


Fig. 16 3-ø voltage source

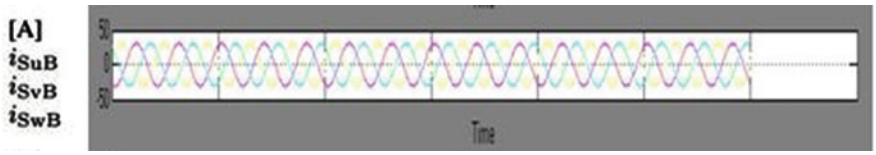


Fig. 17 Supply current

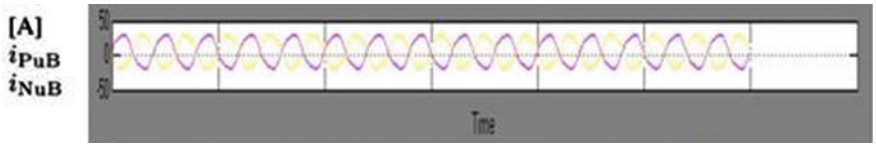


Fig. 18 Positive and negative arm currents

Fig. 19 Circulating current

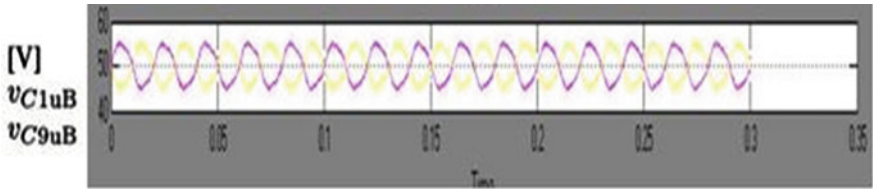


Fig. 20 Voltage across capacitors 1 and 9

Figures 21, 22, 23, 24, 25, 26, 27 and 28 show the response of MMC for ramp change in active power that is rectification mode to inversion mode. The active power changes from 10 to −10 kW the time duration is 20 ms and HBC-B operation changes from inversion mode to rectification mode. The wave forms from Fig. 1.10k–q gives the operation in transient mode. Thus BTB responses faster and enhances the transient system stability and frequency regulation.

Simulated waveforms to a step change of 2 kW in real-power reference from p^* = 8–10 kW where qA^* = qB^* = 0. Figures 29, 30, 31, 32, 33, 34, 35 and 36 give the wave forms of step change of 2 kW in active power where reactive power set to zero.

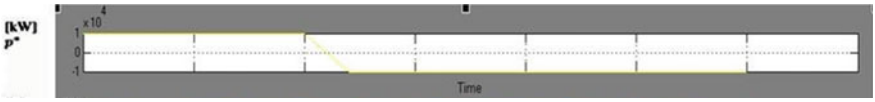


Fig. 21 Active power

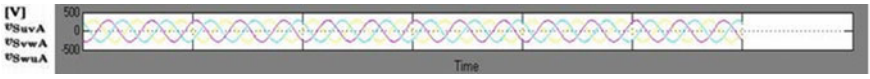


Fig. 22 3-ø voltage source

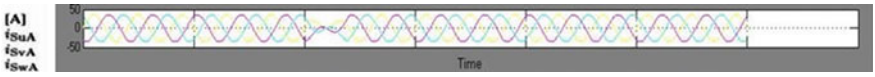


Fig. 23 Supply current

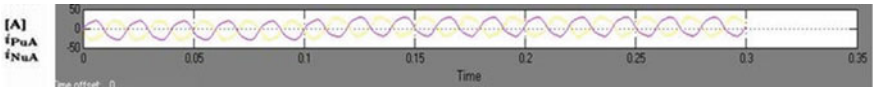


Fig. 24 Positive and negative arm currents

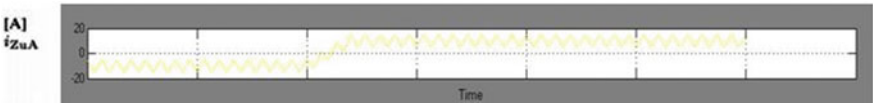


Fig. 25 Circulating current

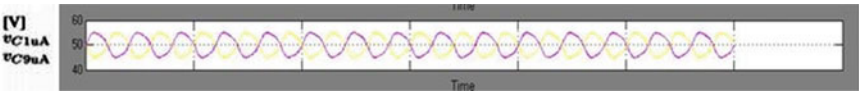


Fig. 26 Voltage across capacitors 1 and 9

Fig. 27 DC voltage

Fig. 28 DC current

Fig. 29 Active power

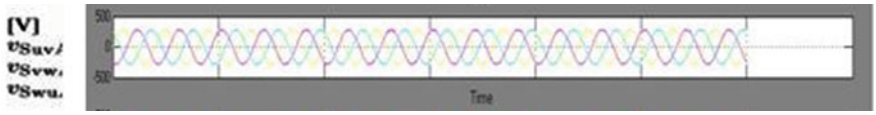


Fig. 30 3-ø voltage source

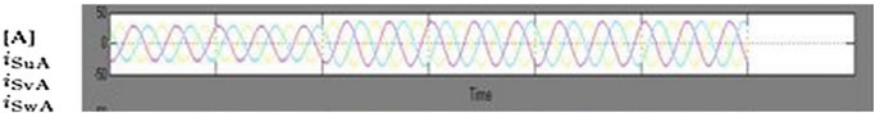


Fig. 31 Supply current

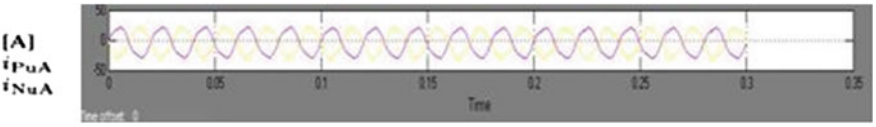


Fig. 32 Positive and negative arm currents

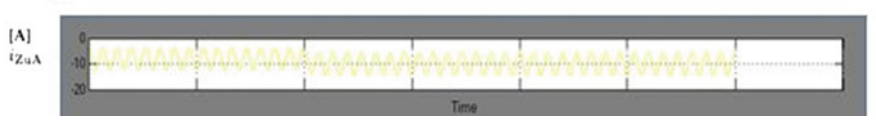


Fig. 33 Circulating current

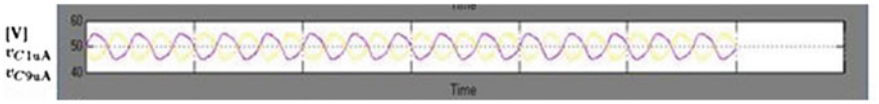


Fig. 34 Voltage across capacitors 1 and 9

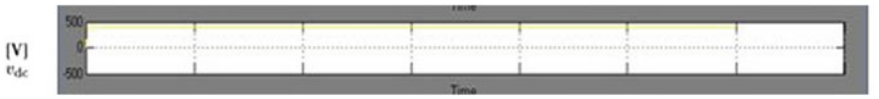


Fig. 35 DC voltage

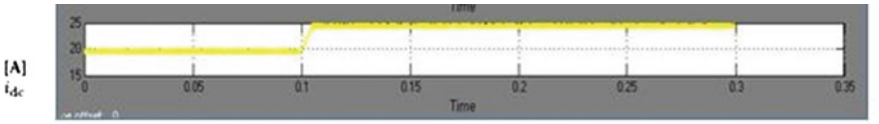


Fig. 36 DC current

6 Conclusions

The basic difference between HVDC transmission and back to back intertie is described in this paper and also this paper has given brief details of BTB intertie systems in India. A phase-shifted modulation technique is used to control the MMC, the circuit and simulation model of phase-shifted modulation presented. The overall control circuit given with block diagram and simulation model also presented. The simulation is carried out by using MATLAB simulink software. In the construction the BTB system two half bridge-based MMCs connected back to back. In this construction there is no DC link capacitor, which can reduce cost and complexity of BTB system. Steady state and transient state wave form presented and also wave forms for unit step change presented. In transient state fault tolerance performance analyzed.

The Need for Uncertainty-Based Analysis in Power System Networks

Yoseph Mekonnen Abebe, P. Mallikarjuna Rao and M. Gopichand Naik

Abstract The increased usage of renewable energy in conjunction with nonrenewable energy source is disturbing the reliability of generation system. This is mainly because of the variability of the power coming from renewable energy sources. Weather change is the main cause for the renewable energy variability. The weather not only disturbs generation, but also transmission line sag-tension and conductor length, thereby varies the voltage drop in the line. The combined transmission line loss, generation variability and load variation make punctual power flow analysis unreliable for planning and forecast purpose. This paper focuses on identifying the main driving forces for power uncertainty. A test case study is conducted and the result shows there is a high variation of the wind and solar energy that led to power variation.

Keywords Network flexibility · Penetration · Reliability · Uncertainty
Wind and solar energy · Weather change

1 Introduction

Due to the depletion of fossil fuels and scarcity of big water resource for hydropower, future energy production is highly dependent on the solar and wind power. One of the advantages of the later energy sources is that they are pollution free, unlike fossil fuel-based generation and low initial cost, unlike hydropower plant. With a growing penetration of this two variable generation system to the main

Y.M. Abebe (✉) · P. Mallikarjuna Rao · M. Gopichand Naik
Department of Electrical Engineering, College of Engineering (A),
Andhra University, Visakhapatnam 530000, AP, India
e-mail: yosephgod@gmail.com

P. Mallikarjuna Rao
e-mail: electricalprofessor@gmail.com

M. Gopichand Naik
e-mail: gopi_905@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_9

grids, their impact must be known. The uncertainty level of this generation system varies in a multiple timescales [1]. One of the aims of using the wind and solar power generation system is to reduce Green House Gas emission which results in the depletion of the ozone layer. Though they are advantageous in terms of pollution, their impact on the smart grid system is non-ignorable. Future planning of any power system network must be with the awareness of the possible variation of the wind and solar energy. Large-scale climate changes like El Nino, which apparently changed the world climate of this year, and temperature gradient of the local vicinity influences the wind speed and solar irradiance [2].

The variation of electric power is divided into three. One is generation variation due to variable generation sources, like the wind and solar power, the second is a transmission line power variation due to the change of transmission line parameter resulting in a varying voltage drop, the third and the most known one is load variation. All the three have an effect on the power flow analysis, which is the main tool in power system planning and control [3]. Transmission line parameter variation is dealt in detail in [4]. This paper mainly focuses on generation uncertainty sources which results a need of uncertain power system analysis in combination with load and transmission line variation.

The application of the wind and solar energy is with the risk of its variability. By disturbing the system network it brings additional cost of mitigation. A sophisticated way of scheduling and reserve allocation is mandatory. In order to allocate a reserve to highly affected area and to control the network from a failure an efficient power system algorithm is needed which considers the input uncertainty [3].

According to [5], power system network flexibility requirement in Europe increases due to the increasing of system size, application of renewable energy and their mix. The ability of the existing power system network to accommodate changes happening after construction determines its flexibility [6]. The main changes come from the variability of demand and VG (Variable Generation) systems. Such variation affects the transmission line in which the power is delivered through to the utility. As a result of this, power system planning must take into consideration the constraints of the transmission lines. When the contribution of the solar and wind energy source is more than thirty percent of the total power generation and the PV (Photo Voltaic) mix is 20–30%, the power disturbance is high and requires the power network to be more flexible than the geographical system size effect [5].

In order to balance the generation and load on time to time bases there is a need to undergo economic dispatch and unit commitment. The ability of a power system network to handle the injection of uncertain power generation is indicated in [7]. The very difficulty mentioned is the congestion of transmission line during load dispatching. This is due to the fact that transmission lines are not designed to handle the worst case scenario when varying generations enter into the system. As a result, the paper proposes the boundary limit during dispatching in order not to congest the lines.

Though the integration of the power system network is evolving itself to smart grid, the day to day increase of the wind and solar energy generation which requires extra high care in prediction is still in its infancy. Since the uncertainty of those energy sources varies in different time scale from place to place and from season to season, the forecasting mechanism has been facing a lot of barriers [8]. Since there is no promising advancement in energy-storing battery system for high power generation, the power generation of the wind plant and PV system is dependent on real time wind speed and solar irradiance [9]. Such kind of variation influences the market badly.

In any grid with high wind and solar power plants, reserve allocation for reliable power delivery is unquestionable duty. In [9] the worst and the best wind power production of Spain for the year 2012 are presented. The best wind production is when it is 110% of the real generation and the worst is when it is 55% of the real generation. From economical point of view the benefit of wind power for the Spanish electric system is when the wind generation is not less than 83% of the real generation. From this one can understand the application of variable generation is subjected to higher and lower values in a real time operation.

According to [10] the application of thermal energy will decrease drastically in the mid of the twenty-first century. The power generation source is then replaced by hydroelectric power in most part of northern Europe, in the Iberian Peninsula, the Baltic and Aegean Sea by wind power and in Germany, United Kingdom and Spain by solar power.

The increased application of the VG sources affects the static variables of a power system, notably, bus voltage magnitude and bus voltage angle. The deterministic power flow analysis only gives information about for predetermined generation and load values at a given time [3]. Since there is a variability from generation to transmission line and finally to the load side, the power flow results are not deterministic values.

There are an extremely high and low values of a generation, as in [9], and load values in a given power system network. As a result, power system networks must be analyzed between the upper and lower interval values in order to deliver a reliable power to the customer and to have a flexible network [11].

Due the variation of generation, transmission line parameters and the usual load change, the application of uncertainty model arises in order to deal with power system analysis [12]. Since transmission line parameter variation is dealt in detail in [4], this paper focuses on generation variation which leads to the need of uncertainty-based power system network analysis. The organization of this paper is as follows: section two deals about solar and wind energy uncertainty due to solar insolation and wind speed variation, respectively; in section three a case study is conducted and finally section four is dedicated to the conclusion.

2 Wind and Solar Generation

Solar and wind energy generation is dependent on the irradiance of the sun and the speed of the moving wind, respectively. Wind is simply the horizontal motion of an air. Though air can also move vertically, the horizontal movement is extremely high. Such moving wind hits the blades of a wind turbine and generates electricity. Unlike hydroelectric power with reservoir and diesel generator, the power generated from wind varies when the wind speed varies. This is mainly due to the impracticality of storing wind speed like water and fossil fuels. The generation of electricity from wind speed is at real time of wind blow. The following formula shows the direct relationship between the wind power and the speed of the wind. Since the power is related to the cubic of wind speed, small variation in wind speed has magnificent change in the power generation [13].

$$P = \frac{1}{2}\rho A V^3 \tag{1}$$

where P is the power generated (W), V is the wind speed (m/s), ρ is the wind density (kg/m^3) and A is the swept area (m^2).

Unlike wind energy, the source of solar energy is the sun residing in our solar system. The sun emits a vast amount of energy which can be converted by PV cells to produce electricity [14]. The electromagnetic radiation emitted by the sun is called solar radiation. The solar radiation per unit area is called solar insolation. The generation of electric power from solar radiation is dependent on the solar insolation. The higher the solar insolation the higher is the power and vice versa.

In order to show the constant variation of the two energy sources, three study areas are selected and their wind speed and solar insolation result for the year 2013–2015 is presented. Since renewable energy sources are gaining high attention due to their pollution free and abundance, their effect on the variation of input power must be considered and a power system analysis, whether it is a power flow, contingency analysis or unit commitment must consider the generation uncertainty beside load variation. This paper aims to show the variation of the wind and solar energy source and hinting the need of power system analysis model which considers the uncertainty in the system.

3 Test Cases

In order to see the variation of power from wind and solar energy, the directly related wind speed and solar insolation can be enough parameter of consideration. As mentioned earlier, the cause of generation variation in today's grid system is mainly due to the application of renewable energy from the wind and solar plants. Three stations are selected for test case study with a coordinate far away from each

other. In order to have a representative outcome, three consecutive years are chosen. Table 1 shows the coordinates of the three stations.

Based on the coordinates of Table 1, the raw data for the wind speed and solar insolation is found from the Ethiopian National Meteorology Agency (NMA) and the NASA data base. The solar insolation results of the three stations for the three consecutive years are depicted in Figs. 1, 2 and 3. Similarly, the wind speed variation measured in the three stations for the three consecutive years is shown in Figs. 5, 6 and 7. In all the figures the x-coordinate represents months of the year and the y-coordinates represents the monthly averaged wind speed or solar insolation value measured at the specified year.

From Figs. 1, 2 and 3 one can easily detect the variation of the solar insolation the monthly averaged values considered. This variation directly affects the generation of a total power of the smart grid networks. When a load variation is also considered with this generation variation, every analysis in power system network is vulnerable to extreme values and needs uncertainty model.

Table 1 Coordinates of the stations

Stations	Area name	Coordinates	
		Latitude	Longitude
A	Adama Town	8° 31′ 34.68″ N	39° 15′ 29.88″ E
B	Bahir Dar Town	11° 34′ 27.1524″ N	37° 21′ 40.8708″ E
C	Wolaita Sodo Town	6° 51′ 10.1124″ N	37° 45′ 39.4884″ E

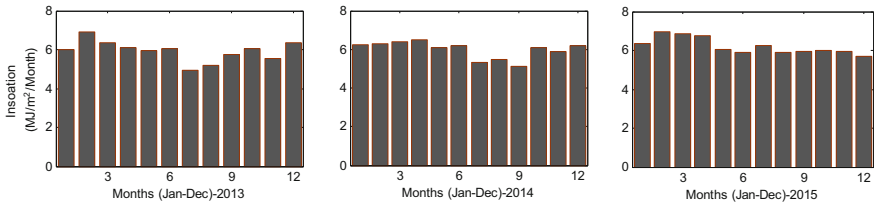


Fig. 1 Solar insolation of station A

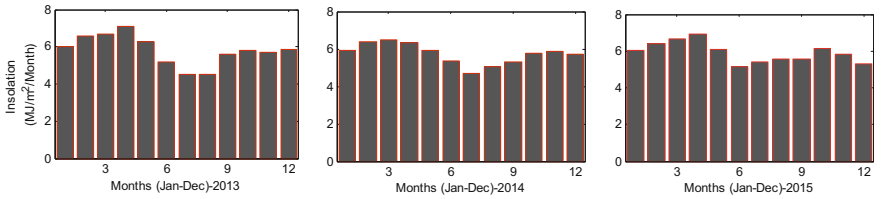


Fig. 2 Solar insolation of station B

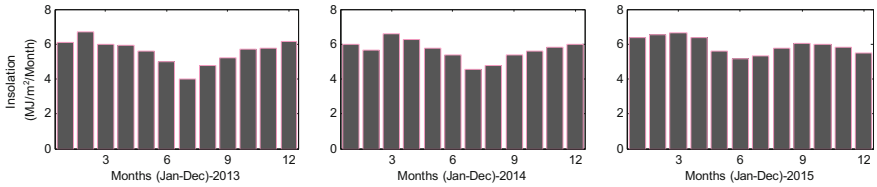


Fig. 3 Solar insolation of station C

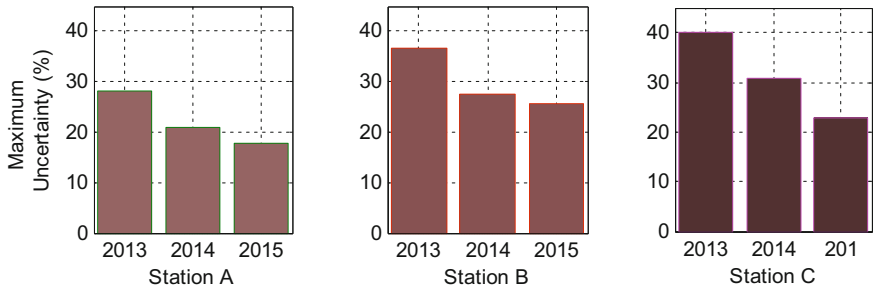


Fig. 4 Maximum solar insolation uncertainty

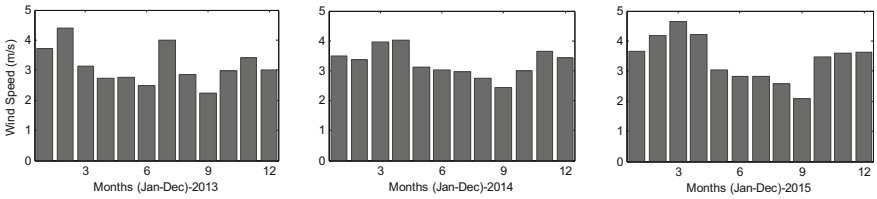


Fig. 5 Wind speed of station A

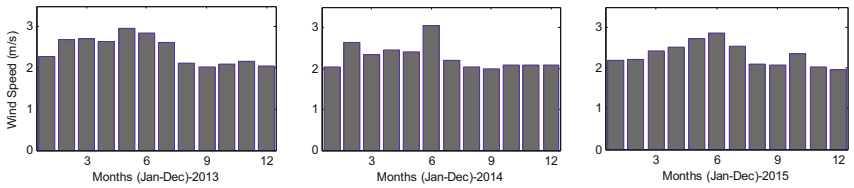


Fig. 6 Wind speed of station B

Some of the powers system network analysis currently under study by different researchers considering uncertainty is power flow analysis, transient stability analysis and voltage assessment. All those studies are initiated by not only load variation, but also the variation of the wind and solar insolation affecting generation

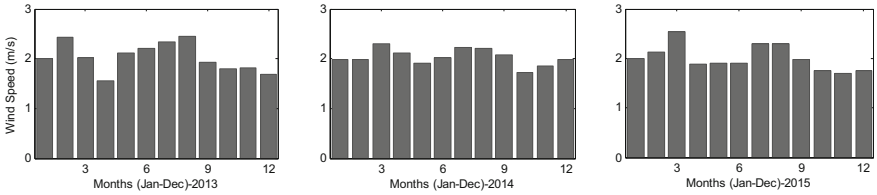


Fig. 7 Wind speed of station C

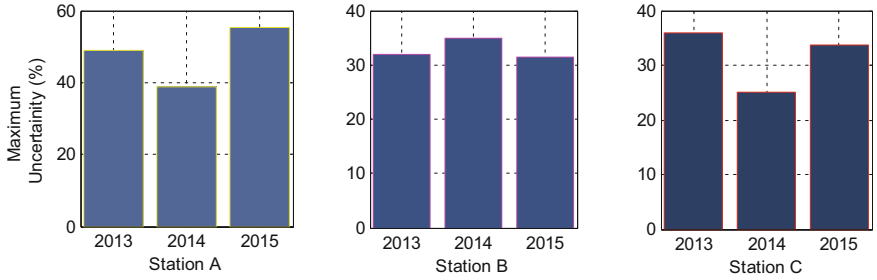


Fig. 8 Maximum wind speed uncertainty

power. A powerful algorithm-based on affine arithmetic (AA) is used to model the uncertain variables, for the aforementioned analysis, and a punctual analysis mechanism proved to be insufficient for future smart grid system analysis [3, 15, 16]. In order to have a better look of the solar insolation variation of the above results, the percentage change between the maximum and the minimum value is depicted in Fig. 4.

From Fig. 4 one can easily detect as the relative high variation of the solar insolation is 39.91% in 2013 in station C. The relative low value of the uncertainty extreme is measured in 2015 at station A which is 17.75%. As a conclusion, the solar insolation which is directly related to the generated power can vary from 17.75 to 39.91% relative extremes during the study period of three consecutive years for the three stations.

Similar to Figs. 1, 2 and 3, the variation of the wind speed which is directly proportional to power generation according to (1) can be detected from Figs. 5, 6 and 7 for the same three stations and three consecutive years. Figure 8 shows the extreme percent of uncertainties for the aforementioned respective stations and study years. According to Fig. 8, the wind speed variation can go from low relative extreme of 25.11% at station C in 2014 to high relative extreme value of 55.17% in station A in 2015.

From the three station case studies, it is deduced that any smart grid system with the solar and wind energy source must take into consideration the presence of input power variation. This is one of the drawbacks of using such renewable energy sources since their output is dependent on the varying weather condition and it is

difficult to precisely predict it [17]. Future planning and control mechanism must be based on the consideration of the entire drawback of such systems. During planning the mathematical model to be applied must be the one which considers the presence of generation, transmission line and load uncertainties in the system. The worst case variation of the wind speed and the solar insolation must be included at the design stage in order to get a realistic result for power system analysis [17].

4 Conclusion

The presence of generation variation due to the wind speed and solar insolation is presented in this paper. A case study of three geographically different stations for three consecutive years is conducted and presented with their share of uncertainty at their respective years. From the result, it is found that the solar insolation can vary as high as 39.91% in station C while the wind speed can vary as high as 55.17% in station A in 2013 and 2015, respectively.

Due to the penetration of the wind and solar energy source more than ever in today's grid system, the only consideration of load variation is an outdated topic. As presented earlier, generation variation is also one of a variable which worth's consideration during planning and controlling of a power system network. This paper proves the non rejection of generation uncertainty with satisfactory case studies. Any power system network analysis, whether it is power flow, contingency, transient stability analysis or the likes must take into consideration the presence of uncertainty both in generation, transmission line and load in order to deliver a reliable power to the customer.

References

1. Ela, E., O'malley, M.: Studying the variability and uncertainty impacts of variable generation at multiple timescales. IEEE Trans. Power Syst. **27**, 1324–1333 (2012)
2. Fant, C., Schlosser, C.A., Strzepek, K.: The impact of climate change on wind and solar resources in southern Africa. Appl. Energy **161**, 556–564 (2016)
3. Abebe, Y.M., Pasumarthi, M.R., Mudavath, G.N.: Load flow analysis of uncertain power system through affine arithmetic. In: Lecture Notes in Electrical Engineering Microelectronics, Electromagnetics and Telecommunications, pp. 217–231 (2015)
4. Abebe, Y.M., Rao, P.M.: Overhead transmission line sag, tension and length calculation using affine arithmetic. In: 2015 IEEE Power, Communication and Information Technology Conference (PCITC), pp. 211–216 (2015)
5. Huber, M., Dimkova, D., Hamacher, T.: Integration of wind and solar power in Europe: assessment of flexibility requirements. Energy **69**, 236–246 (2014)
6. Lannoye, E., Flynn, D., O'malley, M.: Transmission, variable generation, and power system flexibility. IEEE Trans. Power Syst. **30**, 57–66 (2015)
7. Wei, W., Liu, F., Mei, S.: Dispatchable region of the variable wind generation. IEEE Trans. Power Syst. **30**, 2755–2765 (2015)

8. Orwig, K.D., Ahlstrom, M.L., Banunarayanan, V., Sharp, J., Wilczak, J.M., Freedman, J., Haupt, S.E., Cline, J., Bartholomy, O., Hamann, H.F., Hodge, B.-M., Finley, C., Nakafuji, D., Peterson, J., Maggio, D., Marquis, M.: Recent trends in variable generation forecasting and its value to the power system. IEEE Trans. Sustain. Energy **6**, 924–933 (2015)
9. Azofra, D., Jiménez, E., Martínez, E., Blanco, J., Saenz-Díez, J.: Wind power merit-order and feed-in-tariffs effect: a variability analysis of the Spanish electricity market. Energy Convers. Manag. **83**, 19–27 (2014)
10. Stanton, M.C.B., Dessai, S., Paavola, J.: A systematic review of the impacts of climate variability and change on electricity systems in Europe. Energy **109**, 1148–1159 (2016)
11. Jiang, X., Chen, Y.C., Dominguez-Garcia, A.D.: A set-theoretic framework to assess the impact of variable generation on the power flow. IEEE Trans. Power Syst. **28**, 855–867 (2013)
12. Wang, Z., Alvarado, F.: Interval arithmetic in power flow analysis. In: Power Industry Computer Application Conference, pp. 156–162 (1991)
13. Narayana, M., Putrus, G., Jovanovic, M., Leung, P. S.: Predictive control of wind turbines by considering wind speed forecasting techniques. In: Proceedings of the 44th International, pp. 1–4 (2009)
14. Zhang, H., Xin, X., Li, L., Liu, Q.: An improved parametric model for simulating cloudy sky daily direct solar radiation on tilted surfaces. IEEE J. Sel. Top. Appl. Earth Obs. Remote Sens. **6**, 180–187 (2013)
15. Munoz, J., Canizares, C., Bhattacharya, K., Vaccaro, A.: An Affine arithmetic-based method for voltage stability assessment of power systems with intermittent generation sources. IEEE Trans. Power Syst. **28**, 4475–4487 (2013)
16. Vaccaro, A., Canizares, C.A., Villacci, D.: An Affine arithmetic-based methodology for reliable power flow analysis in the presence of data uncertainty. IEEE Trans. Power Syst. **25**, 624–632 (2010)
17. Kamjoo, A., Maheri, A., Putrus, G.: Wind speed and solar irradiance variation simulation using ARMA models in design of hybrid wind-PV-battery system. J. Clean Energy Technol. JOCET. **1**, 14–17 (2013)

Impact of DC Bias on the Magnetic Loading of Three Phase Three Limb Transformer Based on Finite Element Method

Saurabh Kohli, S.B. Mahajan, Padmanaban Sanjeevikumar, Viliam Fedák and Valentin Oleschuk

Abstract This article proposes a modelling mechanism based on Finite Element Method (FEM) to understand the impact of DC currents on the magnetic loading of the transformer. It details on the way magnetizing currents vary and harmonics develop in a transformer. The analysis is performed using ANSYS tool for generating the scaled transformer model and MATLAB for plotting the results. The analysis shows that on varying the primary voltage to different levels of voltages and injecting DC currents based on a weakly coupled multi harmonic approach the three phase three limb transformer is subjected to varying magnetizing currents with the development of odd harmonics based on the saturation level of transformer. The even harmonics are not observed owning to the structure of three phase three limb transformer which offers a high reluctance to DC flux. Furthermore the scaled

S. Kohli (✉) · S.B. Mahajan
Department of Electrical and Electronics Engineering, Marathwada Institute of Technology, Aurangabad, India
e-mail: saurabh.rwth@gmail.com

S.B. Mahajan
e-mail: sagar25.mahajan@gmail.com

P. Sanjeevikumar
Department of Electrical and Electronics Engineering, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

V. Fedák
Department of Electrical Engineering & Mechatronics, Technical University of Košice, Košice, Slovak Republic
e-mail: viliam.fedak@tuke.sk

V. Oleschuk
Institute of Power Engineering of the Academy of Sciences of Moldova, Chisinau, MD 2028, Moldova
e-mail: oleschukv@hotmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_10

transformer is observed in ANSYS and it is visualized that the stray fluxes and the saturation levels of the three limb transformer raises to a higher level on impact of DC currents of varying magnitudes.

Keywords Three phase transformer model · DC bias · Half cycle saturation Harmonics · Magnetizing currents · Geo-magnetically induced currents

1 Introduction

The core of power transformer is generally operated with Alternating Current (AC) fields and hence they are designed so as to carry AC current but the existence of superimposed DC flux over the AC flux may easily cause the transformer to saturate and thereby causing damage to the transformer parts. There is a tendency of the transformer to saturate in the half cycle with the impact of DC, as the magnetizing current shift towards the positive direction owning to unidirectional DC flux in the core. This phenomenon is known as half cycle saturation [1] and is widely the main effect of DC superimposed over AC flux in transformer.

Even a small amount of Direct Current (DC) may result in the production of huge MMF inside the core as the currents get multiplied to the number of turns of the winding. The transformer gets severely affected with the increase in the losses, especially the core losses and stray losses, it also results in the production of harmonics with increased demand of the reactive power, this also affects the structural components of the transformers with overheating in several parts including the tank wall, tie plates and clamping plates. The main source of DC injection into the power transformer is the geo-magnetically induced currents (Geo-magnetically Induced Currents (GIC)) [2–5] are produced by the combination of magnetic field of earth and solar winds. There are other DC sources like the power electronics device example the anti-parallel thyristor arrangement and the HVDC transmission lines. Other source may include neutral offset by DC drives. The odd and even harmonics [6–8] produced as a result of DC magnetization causes increase in the stray losses and sometimes false tripping in power system.

2 Three Limb Transformer Construction and Superimposition of DC Flux

In three limb transformer construction the three legs or limbs of the transformer are wounded with the Cu coil windings which depicts the three phases for the transformer. The construction is such that each limb is connected to yokes on either side

of that limb and hence there are two yoke structure at the top and at the bottom. Thus a transformer flux path is completed by joining the limbs and the yokes. In the normal operating condition, there is a flux flowing through each limb of the transformer and as the source is alternating and sinusoidal, so is the flux and the flux is flowing, such that it is nearly equal in the limbs and the yoke. In balanced condition of the three phase transformer, it can be visualized that the flux oppose and cancels in the yoke area of the transformer and hence no return path for the flux is needed. However, such is not the case for an unbalanced load when the entire flux follows a path of a larger air gap and then has to return back to the core again. This large air gap area offers a very high reluctance for the flux to flow through and hence it becomes interesting to see the impact of this very high reluctance path on the flux of the transformer when it is superimposed with a DC flux.

There is variation in the normal produced flux as the DC flux gets superimposed onto the normally produced AC flux, now this flux produced is a unidirectional DC flux which depends on the reluctance offered to the DC flux path, the winding turns and amplitude of the DC. In one-half cycle of a complete sinusoid the DC flux would be added and in other half it would be subtracted thereby causing a flux shift. The average of the flux starts to increase in the direction of shifting, which increases the saturation in the positive direction, and increases significantly the excitation current in the positive direction. When the flux keeps on increasing and is sufficiently large enough, it reduces the excitation current in the negative half cycle, and so excitation current is significantly positive. This results in partial magnetic saturation of the transformer core and hence transformer does not operate at the expected working point. The peak flux densities in the magnetic core in one half of the cycle are very high and hence plot the B–H curve is non-linear. One can visualize a smaller shift in the flux density owning to higher reluctance offered by the core material and correspondingly the magnetizing currents attain higher peaks and with shorter duration.

3 Modelling Mechanism

The simulation method used for carrying out simulation on the scaled transformer is the Finite Element Method (FEM) [9, 10]. As there are boundary conditions associated with each transformer based on the flux at different areas of the core, this method provides a numerical solution to such boundary conditions. It is possible to predict which areas of the core are heavily impacted by the injection of DC current on the transformers with the help of this method [11]. Figure 1 shows a two-dimensional three phase three limb scaled transformer FE model.

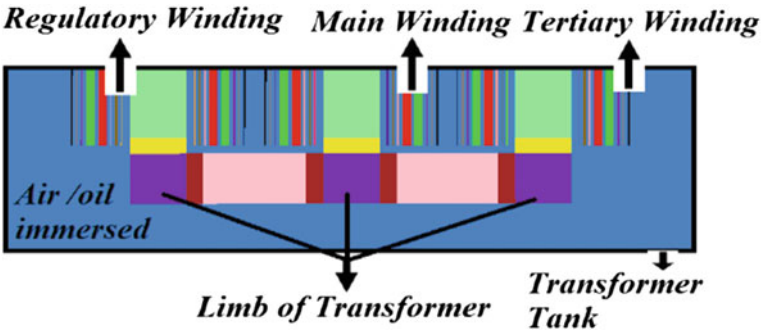


Fig. 1 Two-dimensional three phase three limb transformers FE model

4 Working Point Calculation of Transformer Considering Non-linear Material Properties

Transformers working point is more justifiable if the non-linear properties of the core material are considered. The material of the core will be represented by effective B-H characteristics. Using a weakly coupled multi harmonic [12–14] approach the results of the Finite element is transformed for further analysis in frequency domain and it is understandable to get the harmonics in this domain which is suitable for the evaluation of DC injection.

To calculate the working point of a transformer for non-linear material requires more computational efforts compared to a linear material. Begin with the linear materials and finally end up calculating the exciting currents and vector potential solutions for flux calculations and visualization of the transformer non-linear core material. The idea behind calculating the working point for a non-linear core material is to reach to an operating point in the B-H curve, which is close to the saturation level of the transformer and later see the impact of DC at these operating points. Thus, considering a core reluctivity for the transformer at its rated flux density initially a linear inductance matrix is calculated and then the fundamental component of the transformer currents are obtained and converted into time domain and later calculating the nonlinear inductance matrix at different time steps considering non-linear properties of the selected material. Further from the non-linear inductance's and the flux obtained the magnetizing currents for the non-linear materials in the frequency domain are calculated by taking the Fast Fourier transform to visualize the harmonics in the currents. To obtain the impact of DC for the non-linear core material a DC component is injected as different percentage of a fundamental current after and the Fast Fourier transform (FFT) is calculated to visualize the impact on the magnetizing currents and the harmonics.

5 Simulation Results for Scaled Transformer Model

The transformer model has the three phase with three limb having eight coils on each limb. With two coils as main winding, one coil as the tertiary winding and remaining five coils as the regulating windings. The technical details of the transformer are given in Table 1.

When a transformer saturates, the whole core usually does not saturate on the same level. That is, part of the core may saturate more than other parts, while some part may not saturate at all. The core saturation patterns may vary depending on the core configurations. The flux distribution and the magnetizing current calculation are done based on the working point calculation considering non-linear material properties as discussed for the no load case. The non-linear core material considered for the scaled transformer is TKES C120 with a peak flux density at saturation near to 1.7 T as shown by the B-H Curve in Fig. 2.

While injecting the DC into the model, it has been taken as some percentage of the fundamental current initially injecting a lower percentage of the fundamental component and then higher to visualize the differences. The primary winding has been also excited at different levels of voltage to see the impact of DC close to the saturation point of the transformer. The windings are connected in star and the

Table 1 Technical detail of transformer

S. No	Parameters of transformer	Value
1	Rated power	6.9 kVA
2	Rated voltage	400/400 V
3	Rated current	10/10 A
4	Rated frequency	50 Hz
5	Rated flux density	1.2 T
6	Switching group	Adjustable

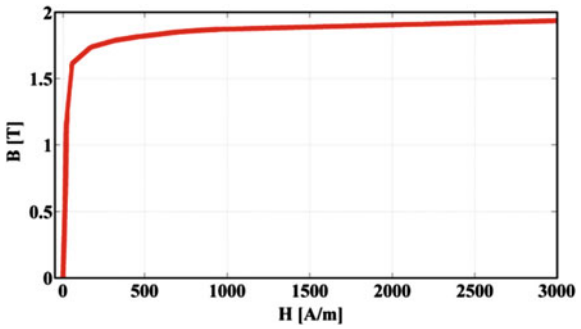


Fig. 2 BH curve for TKESC120 core material

neutral is grounded. The results are plotted in MATLAB in a two way pattern so as to analyze the magnetizing current behaviour and the harmonic content measured for in the non-linear core material with the impact of DC.

6 Results Interpretation of DC Impact on Magnetizing Currents and Harmonics

It is observed that as the level of DC bias increases in the transformer core with non-linear material a small increase in the odd order harmonics based on the saturation level of the transformer (see Figs. 3, 4, 5 and 6). But there is no effect on the even harmonics. This can be attributed to the fact that DC flux in case of a the three phase three limb transformer design is obstructed by magnetic reluctance which is very high and that flux passing through the core-tank magnetic circuit has a zero flux path, but while considering the 2D Model this flux path is not considered and hence DC flux leaves as stray flux. Because the magnetizing currents depend on

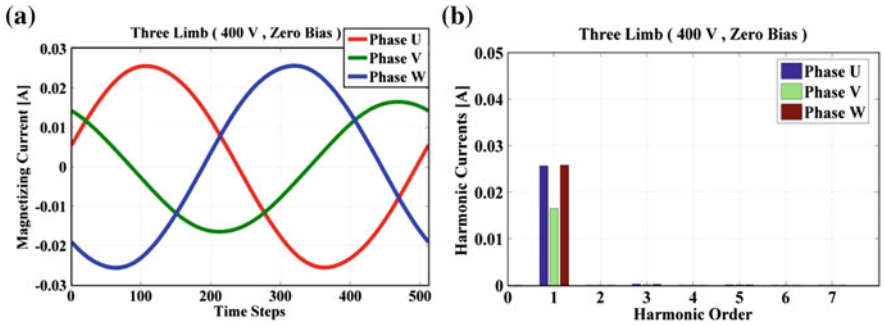


Fig. 3 **a** Magnetizing currents **b** harmonics at zero (0) DC bias

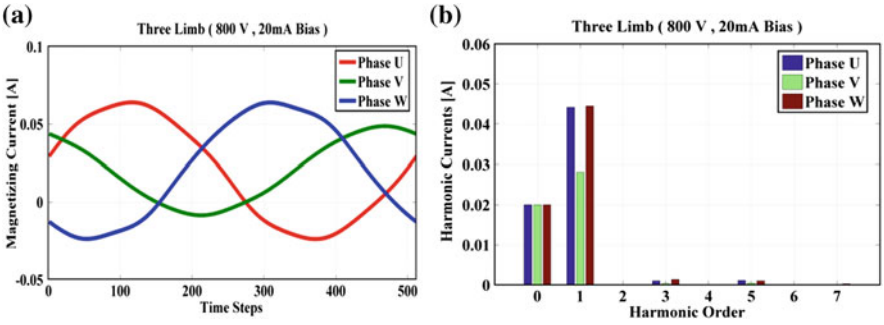


Fig. 4 **a** Magnetizing currents **b** harmonics at [input primary voltage = 800 V, 20 mA DC bias]

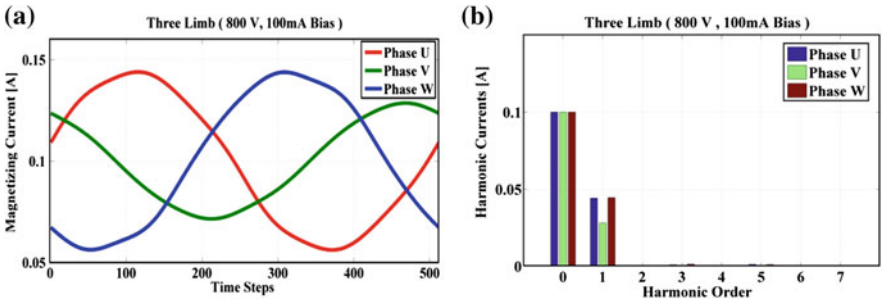


Fig. 5 **a** Magnetizing currents **b** harmonics at [input primary voltage = 800 V, 100 mA DC bias]

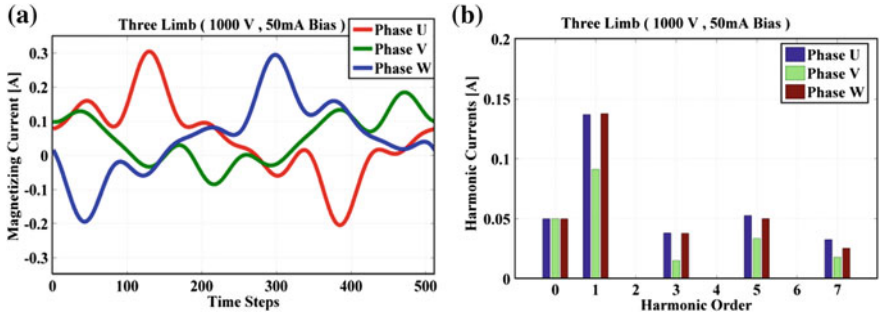


Fig. 6 **a** Magnetizing currents **b** harmonics at [input primary voltage = 1000 V, 50 mA DC bias]

the total flux and since the DC flux has no impact owing to absence of zero flux path there is no increase in even order harmonics and hence for a particular voltage level the magnetizing current remains the same with the absence of even harmonics.

7 Visualizing Flux and Magnetic Vector Potential

For an input primary voltage of 800 V in ANSYS it is visualized the stray fluxes which are leaving the transformer core and see how the saturation level of the flux changes with DC bias of 75 mA as shown in Figs. 7 and 8. It is observed that the influence of stray fluxes is higher with DC bias when the DC flux is superimposed with the alternating flux. Also a comparison can be made between two different DC levels for a transformer core applied with a primary voltage of 1200 V from Figs. 9 and 10 which depict the increase in saturation flux by the magnetic flux density scalar bar with a higher level of DC current of 2 A compared to 1 A.

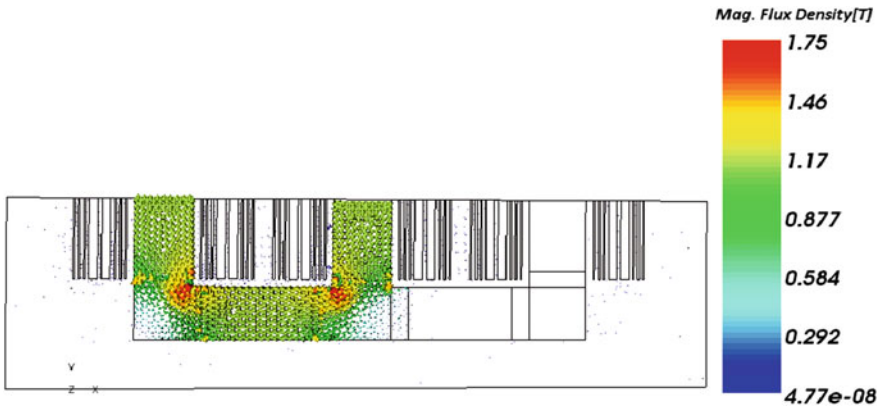


Fig. 7 Flux distribution in transformer without DC [zero or 0] bias

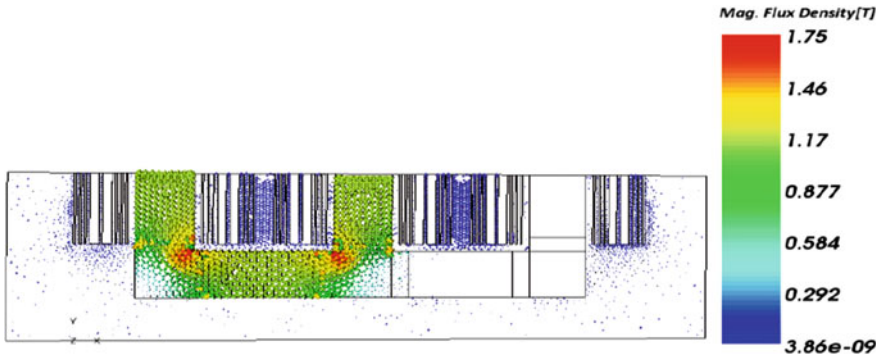


Fig. 8 Flux distribution in transformer with 75 mA bias

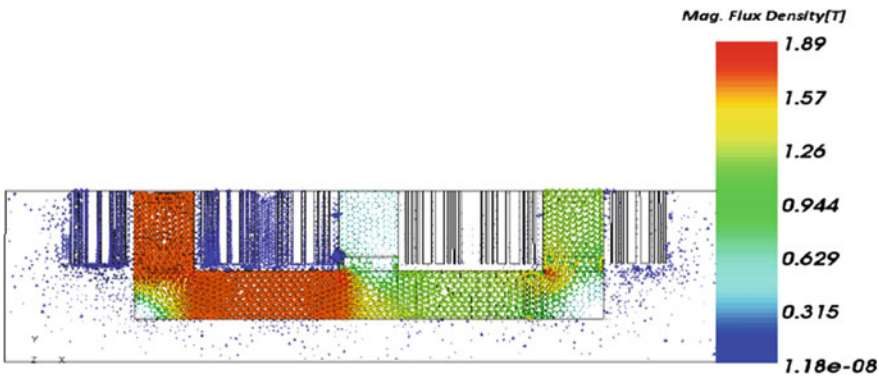


Fig. 9 Flux distribution with DC bias of 1 A

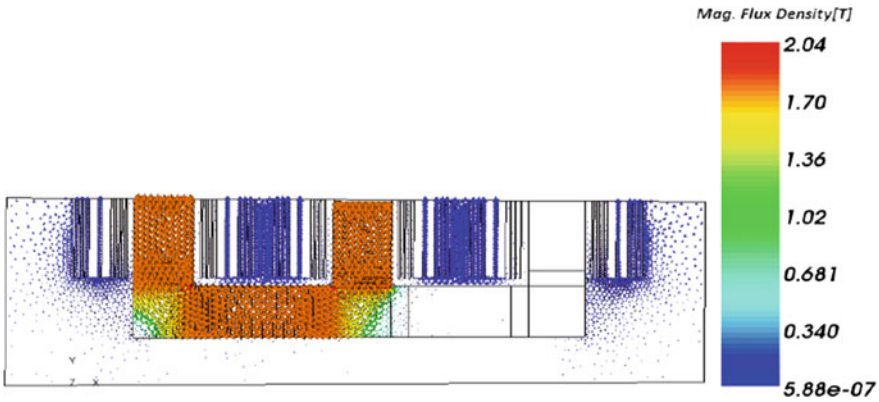


Fig. 10 Flux distribution with DC bias of 2 A

8 Conclusion

On the impact of DC on the three phase three limb transformer, it is visualized that based on the saturation levels and the core structure of a three leg transformer the odd harmonics are visible and increases as the saturation level increases but there is no influence on even harmonics owning to the high reluctance path the 2D model offers. Also the ANSYS results depict an increase in stray fluxes and a higher saturation level with peak flux densities at a higher level of DC.

References

1. Ngnegueu, T., Marketos, F., Devaux, F., Xu, T., Bardsley, R., Barker, S., Baldauf, J., Oliveira, J.: Behavior of transformers under DC/GIC excitation: Phenomenon, Impact on design/design evaluation process and Modeling aspects in support of Design. Cigre (2012)
2. Vassell, G.S.: Northeast blackout of 1965. IEEE Power Eng. Rev. (1991). ISSN: 0272-1724
3. Price, P.R.: Geo-magnetically induced current effects on transformers. IEEE Trans. power deliv. **17**(4), 1002–1008 (2002)
4. Kappenman, J.G.: Geomagnetic storms and their impact on power systems. IEEE Power Eng. Rev. (1996). ISSN: 0272-1724
5. Girgis, R., Vedante, K.: Effects of GIC on power transformers and power systems. In: IEEE Transmission and Distribution Conference and Exposition (T&D), IEEE PES, pp. 1–8 May (2012)
6. Xu, W., Martinich, T.G., Sawada, J.H., Mansour Y.: Harmonics from SVC transformer saturation with direct current offset. IEEE Trans. Power Deliv. **9**(3), 1502–1509 (1994). ISSN: 0885-8977
7. Yarnada, S., Bessho, K., Lu, J.: Harmonic balance finite element method applied to nonlinear AC magnetic analysis. IEEE Trans. Magn. **25**(4), 2971–2973 (1989). ISSN: 0018-9464
8. Lu, S., Liu, Y., De La Ree, J.: Harmonics generated from a DC biased transformer. IEEE Trans. Power Deliv. **8**(2), 725–731 (1993). ISSN: 0885-8977

9. Zhao, X., Li, L., Lu, J., Cheng, Z., Lu, T.: Characteristics Analysis of the square laminated core under dc-biased magnetization by the fixed-point harmonic-balanced FEM. IEEE Trans. Magn. **48**(2), 747–750 (2012). ISSN: 0018-9464
10. Lu S., Liu Y.: FEM Analysis of DC saturation to assess transformer susceptibility to Geo-magnetically induced current. IEEE Trans. Power Deliv. **8**(3), 1367–1376 (1993). ISSN: 0885-8977
11. Fuchs, E.F., You, Y., Roesler, D.J.: Modeling and simulation, and their validation of three-phase transformers with three legs under DC bias. IEEE Trans. Power Deliv. **14**(2), pp. 443–449 (1999). ISSN: 0885-8977
12. Yamada, S., Bessho, K., Lu, J.: Harmonic balance finite element method applied to non linear AC magnetic analysis. IEEE Trans. Magn. **25**(4), 2971–2973 (1989). ISSN: 0018-9464
13. Björn R., Adalbert L. E., Kay H.: Calculation of the flux distribution of three phase five limb power transformers considering nonlinear material properties. Int. J. Comput. Math. Electr. Electro. Eng. **32**(4) (2013).ISSN: 0332-1649
14. Björn, R., Kay, H.: Multi Harmonic approach to determine load dependent local flux variations in power transformer core. Archieve Electr. Eng. **64**(1), 129–138 (2015)

Cost Optimization of a Ring Frame Unit

Rathinadurai Louis Helen Catherine, A. Soundarrajan and Josephine Rathinadurai Louis

Abstract India focuses on many sectors out of which much of its growth in energy consumption is expected to occur in the countries outside the Organisation for Co-operation Economic and Development (OCED) known as non-OCED where demand will be drawn by strong, long-term economic growth and India fits into this particular category. In this research, the spinning mill is considered for optimizing the parameters regarding the energy management with the real-time data taken from a ring frame unit of spinning mill, analysis is done to find the feasible operating conditions with the aim of minimizing the energy cost and increasing the profitability of the sector, thereby suggesting for the spinning mill sector in India.

Keywords Cost optimization · Doff time · Energy management
Ring frame unit · Spinning mill

1 Introduction

Energy is the lifeline growth for any economy. In the case of a developing country like India, energy sector is imperative because when considering the energy needs which are increasing day by day, huge investment is made in the view to meet the

R.L. Helen Catherine (✉)
Electrical & Electronics Engineering, Dr. Mahalingam College of Engineering & Technology, Pollachi 642003, India
e-mail: c.catherineclement@gmail.com

A. Soundarrajan
Information Technology, PSG College of Technology, Coimbatore 641004, India
e-mail: soundaa@yahoo.com

J.R. Louis
Electrical & Electronics Engineering, PSG Institute of Technology & Applied Research, Coimbatore 641062, India
e-mail: Josephinedhayal@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_11

demand. Industrial sector energy use in the non-OCED economic countries including India is expected to increase by 1.8% per year compared to 0.6% per year in the OCED Economics [1–3]. The chasm in the growth rates mirrored both faster anticipated economic expansion outside the OCED and differences in comparison of industrial sector production. Industrial textile sector has an overwhelming presence in the economic life of the country as it is the second last provider of employment next to agriculture. The opening up of the Indian economy in 1991 gave the much needed thrust to the textile industry which has become one of the largest players in the world.

Textile industry of India ranks second in the world and also contributes 11% to industrial production, 14% to manufacturing sector, 4% to the gross domestic product (GDP) and 12% to the country's total export savings. About 35 million people are directly benefitted through employment and also to other 54.85 million people in its related activities [4–7]. High speed drives for textile rotor spinning applications are also considered. In this research a high speed drive and frictionless suspension system for a rotor spinning unit which opens up the field for further textile technology development, potentially leading to higher productivity, reduced power consumption and dust deposit are considered [8].

2 Energy Consumption Details of the Spinning Mill

The spinning mill taken for study consists of 30 ring frames of various counts. There are seven ring frames of the same count that corresponds to 21's count. Only one such ring frame is taken for analysis and is extended for the remaining spinning frames. The ring frame details, motor details are given in Table 1 and it shows the energy consumption of various units of the spinning mill considered.

It can be seen from Table 1, that more energy consumed in the ring frame section and second consumption comes to the preparatory section. Hence in this research a ring frame section is considered. Figure 1 shows the ring frame section taken for analysis. The ring frame section of Fig. 1 is operated at a speed of 17,000 rpm (average of 16,677 rpm) all the times to produce the yarn. For the analysis point of view, the speed of the spindle is varied and the major readings of

Table 1 Energy consumption details of various sections in a spinning mill

S. No.	Units	Energy consumed (%)
1	Spinning (ring frame)	44.21
2	Preparatory	29.42
3	Plant	11.60
4	Auto coner	8.65
5	Compressors	2.93
6	Lights	1.44
7	Others	1.75

Fig. 1 Ring frame section

Table 2 Readings of 1-doff of ring frame section

S. No.	Set speed (rpm)	Average speed (rpm)	Doff time (min)	Displayed yarn length (m)	Displayed production per spindle (g)	Energy consumed (units)	Production per doff (kg)
1	14,000	13,731	75	1589	44.68	33	52
2	15,000	14,975	69	1597	44.9	35	52.1
3	16,000	15,800	65	1589	44.68	36	52.2
4	17,000	16,625	62	1589	44.68	39	52.75
5	18,000	17,650	58	1589	44.68	42	55

doff time, energy consumed and the production made are noted and tabulated in Table 2.

With readings noted down, the cost analysis of energy and the profitability of yarn are done to find the optimum point of speed of the ring frame to be operated with the ultimate aim of attaining higher profit of the spinning mill [9–11].

3 Per Day Mathematical Analysis

The generalized steps involved includes audit current operating conditions of the mill, collection of required identification of the areas that needs to be improved, plotting graphs and inferences and cost analysis. But in order to obtain a paramount cost analysis [12–15] view, a sequential flow chart may be followed is shown in Fig. 2.

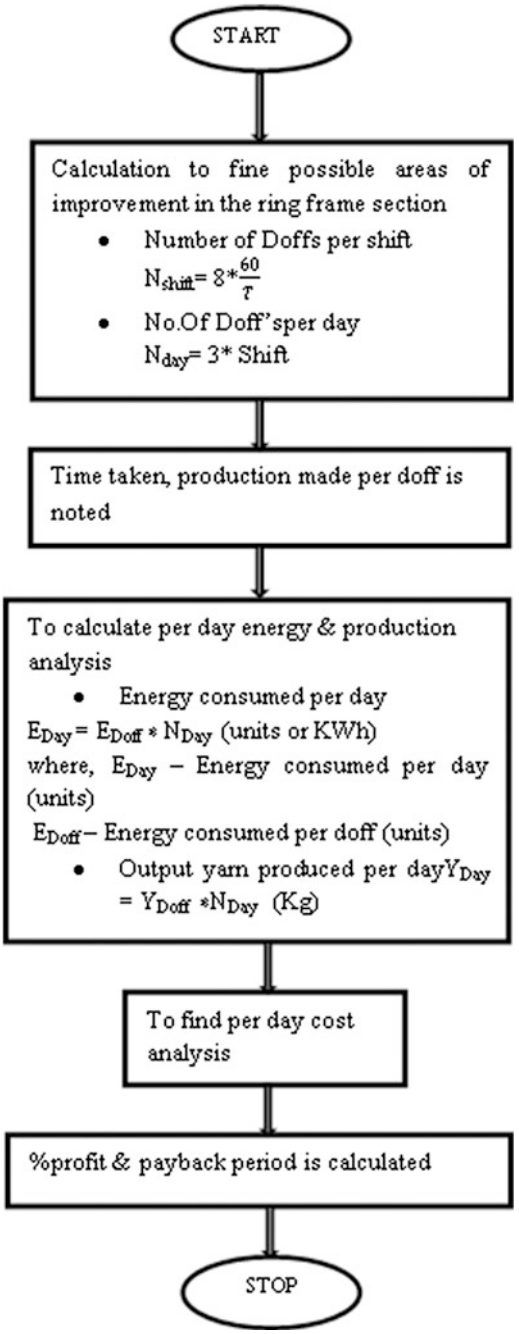


Fig. 2 Flowchart of cost analysis

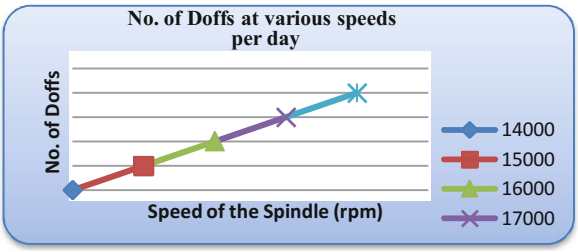


Fig. 3 Number of doffs per day

Table 3 Number of doffs at various speeds of the spindle

S. No.	Set speed (rpm)	Doff time (min)	Doff time, T (min) (approx.)	No. of doffs per shift, N_{Shift}	No. of doffs per day, N_{Day}
1	14,000	75	80	6	18
2	15,000	69	74	6.486	19.45
3	16,000	65	70	6.857	20.57
4	17,000	62	67	7.164	21.49
5	18,000	58	63	7.619	22.85

3.1 Per Day Energy and Production Analysis

With the measured readings of one doff at various speeds of the ring frame, the total production of yarn are calculated for one day and the respective graph is plotted and shown in Fig. 3. Table 3 provides the data for number of doffs per day.

It can be seen from Table 3 that extra 5 min is added to the doff time considering the replacement of the empty spindles in the ring frame after the production. It is noted that the number of doffs per day increases by one consecutively with the increase in speed by 1000 rpm. The minimum number of doffs is at 14,000 rpm (18th Doff) and the maximum number of doff is at 18,000 rpm (22nd Doff) of the spindle.

3.2 Total Energy Consumed and Total Production at Various Speeds of Spindle

Table 4, shows the total energy consumed and total production per day. Figure 4, shows the graphical representation of details mentioned in Table 4. The total energy consumed (units) by the ring frame increases as the speed of the spindle (rpm) increases. From the energy saving point of view, the spindle should be operated at a speed of 14,000 rpm (which consumed energy of 366 units less than in 18,000 rpm

Table 4 Production per shift and per day

S. No.	Set speed (rpm)	Energy consumed per doff (units)	Energy consumed per shift (units)	Energy consumed per day (units)	Production per doff (kg)	Production per shift (kg)	Production per day (kg)
1	14,000	33	198	594	52	312	936
2	15,000	35	227.03	681.08	52.1	337.95	1013.84
3	16,000	36	246.85	740.57	52.2	357.94	1073.83
4	17,000	39	279.40	838.21	52.75	377.91	1133.73
5	18,000	42	320	960	55	419.05	1257.14

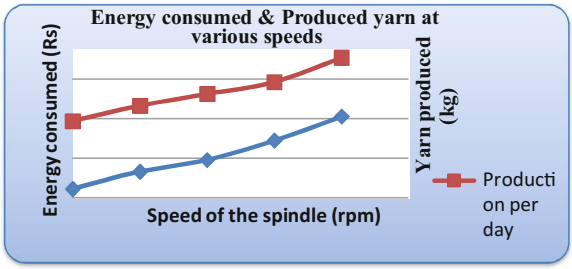


Fig. 4 Energy consumed at various speeds

Table 5 Units consumed per kg

S. No.	Set speed (rpm)	Energy consumed per day (units)	Production per day (kg)	UKG
1	14,000	594	936	0.635
2	15,000	681.08	1013.83	0.672
3	16,000	740.57	1073.82	0.690
4	17,000	838.20	1133.73	0.740
5	18,000	960	1257.14	0.764

per day). The production of the yarn is high at higher speed of the spindle (298 kg increase of yarn produced at 18,000 rpm from a base speed of 14,000 rpm). Therefore, from the productivity point of view, the ring frame should be operated at a speed of 18,000 rpm to yield higher kg of yarn.

3.3 Units Consumed per kg (UKG) Analysis

Table 5 shows the units consumed per kg of yarn and Fig. 5, show the corresponding graphical representation of details mentioned in Table 5.

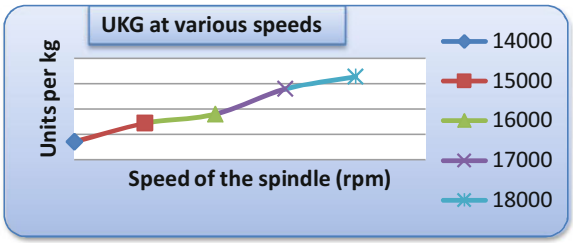


Fig. 5 UKG at various speeds

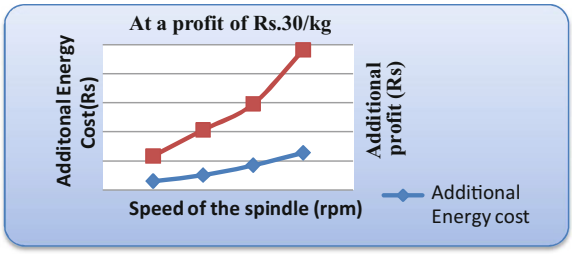


Fig. 6 At a profit of Rs. 30/kg

It can be seen that energy consumed per kg of yarn increases gradually as the speed of the spindle increases [16–18]. It consumes 143 Wh more energy at the highest speed (18,000 rpm) per kg of yarn.

3.4 Per Day Cost Analysis

For cost analysis, two major factors are considered

(i) Energy cost per unit
(ii) Profit of the yarn per kg

Also the following details are taken.

(i) The average cost of energy per unit from various sources (Tamil Nadu electricity board, wind units, third party MALCO thermal and wind units of India) of the spinning mill is taken as Rs. 7(Indian Currency)
(ii) The profit per kilogramme of the yarn has the range of Rs. 5, 10, 15, 20, 25 and 30 based on various market conditions.
(iii) 14,000 rpm is taken as the reference value for analysis.

The additional energy costs (Rs.) and profit per day is shown in Appendix 1. Table 5 shows the calculated value at a profit of Rs. 5/kg of yarn and Rs. 30/kg of yarn. Additional profit and additional energy costs are calculated for Rs. 5, 10, 15, 20, 25, 30/kg of yarn. Figures 6 and 7 shows the graph corresponding to Rs. 5/kg and Rs. 30/kg of the yarn.

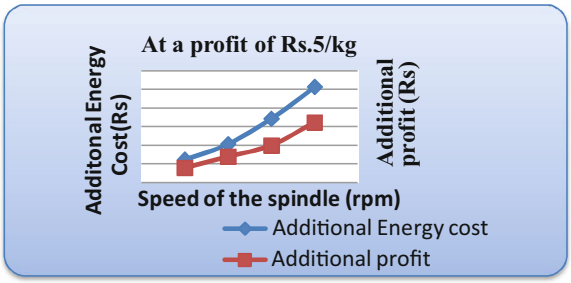


Fig. 7 At a profit of Rs. 5/kg

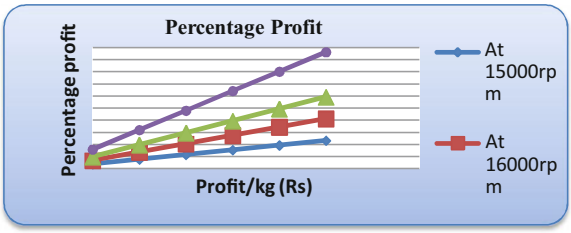


Fig. 8 Percentage profit

4 Results and Discussion

From per day mathematical analysis provided in previous sections with the manual interpretation, it can be seen that when the profit of the yarn is Rs. 5/kg, the additional energy consumption cost is greater than the additional profit for the speed greater than 14,000 rpm (considered as the base value for analysis). When the profit per Kilogramme of yarn is Rs. 10, it is found that the additional profit becomes more than the additional energy cost for all speeds greater than 14,000 rpm of the spindle. The ring frame was operated at its full load with 17,000 rpm of the spindle speed. In order to operate at 18,000 rpm, it is suggested to replace the existing three phase induction motor with a higher rated machine. The payback period (approximate) is calculated and shown in Eq. (1)

$$\text{Payback period} = (\text{Motor price} + \text{Installation charge})/\text{Annual savings}. \quad (1)$$

The additional profit of the yarn for a year (Annual savings) when the spindle is operated at 18,000 rpm is found to be around Rs. 11 lakh. The total price of the new high rated motor around Rs. 7 lakh(inclusive of interest value and installation charges) without considering the utility rebate cost, the payback period is found to be seven months (approximately) when the profit/kg values is calculated and Fig. 8 shows the percentage profit at various speeds of the spindle.

It can be seen from Fig. 8 that there is a huge profit increase at 18,000 rpm speed of the spindle than the other speed. For the available seven ring frames of 21's count the profit analysis for 18,000 rpm is estimated (approximately) for various profit/kg (Rs.) values and tabulated in Table 6.

Table 6 Profit per kg

S. No.	Profit per kg (Rs.)	Additional profit at 18,000 rpm (Rs.) (approx.)
1	5	40 lakh
2	10	80 lakh
3	15	1 crore
4	20	1 crore and 50 lakh
5	25	2 crore
6	30	2 crore and 40 lakh

5 Conclusion

From the cost analysis performed with the real time data, it is clear that there will be loss, if the ring frame is operated at a higher speed (15,000 rpm and above) when the profit of the yarn/kg is Rs. 5. If the operating speed is 17,000 rpm, there may be a loss about Rs. 700 per day (about Rs. 250,000 a year) as the additional energy cost exceeds the additional profit. Also a large amount of energy can be saved by operating at 14,000 rpm.

If profit less than Rs. 10/kg then,
Operate the spindle at 14,000 rpm
else,
If profit greater than Rs. 10/kg then
Operate the spindle at 18,000 rpm

Payback Period:
Example: From the annual cost analysis when the profit is Rs.10/kg and the speed of 18,000 rpm, the payback period for the replacing motor is calculated as follows.
The annual savings for 18,000 rpm is Rs. 1156628. Approximate value of Rs. 1100000 is taken. Then from the price of suggested motor mentioned above,
Payback period = 700000/1100000
= 0.63 years = 7 months (approx.).

Appendix 1

The additional energy cost (Rs.) at various speeds is calculated by subtracting the respective actual energy cost with the energy cost value of 16,000 rpm.

Example: Taking the energy cost of 18,000 rpm from Table 5, the additional energy cost is calculated as:

$$\text{Additional energy cost} = 6720 - 4767 = \text{Rs. } 2562$$

Similarly for the Additional energy consumed (units), Additional production (kg) and Additional profit (Rs.) are calculated for various speeds with the reference values of 16,000 rpm.

The profit per day is calculated as:

$$\text{Profit per day} = ((\text{Profit/kg}) \times \text{Production per day}) = \text{Rs. } 5369.14$$

References

1. Nimon, W., Beghin, J.: Ecolabels and international trade in the textile and apparel market. Wesley Am. J. Agric. Econ. **81**(5), 1078–1083 (1999). http://lib.dr.iastate.edu/card_workingpapers/228/
2. Kneller, R., Stevens, P.A.: Frontier technology and absorptive capacity evidence from OECD manufacturing industries. Oxford Bull. Econ. Stat. **68**(1), 1–21 (2006). http://onlinelibrary.wiley.com/doi/10.1111/j.1468-0084.2006.00150.x/abstract
3. Jimenez-Rodriguez, R.: The impact of oil price shocks: evidence from the industries of six OECD countries. Energy Econ. **30**(6), 3095–3108 (2008). www.sciencedirect.com/science/journal/01409883/30
4. Kumar, D., Singh, D.: Export competitiveness of indian textile industry. Abhinav Nat. Monthly Refereed J. Res. Commer. Manage. **4**(2), 1–7 (2015). http://abhinavjournal.com/journal/index.php/ISSN-22771166/article/view/535
5. Tandon, N., Reddy, E.E.: A study on emerging trends in textile industry in India. Int. J. Adv. Res. Technol. **2**(7), 267–277 (2013)
6. Singh, M.P., Lal, M.: Export performance and competitiveness of Indian textile industry. Int. J. Sci. Res. **2**(11), 315–316 (2013). http://citeseerx.ist.psu.edu/viewdoc/download?doi=10.1.1.685.3177&rep=rep1&type=pdf
7. Sharma, M., Dhiman, R.: Determinants affecting indian textile exports. A Rev. Biz Bytes. **6**(2), 195–201 (2015). http://cbsmohali.org/img/Determinants%20Affecting%20Indian%20Textile%20Exports%20A%20Review
8. Silber, S., Sloupensky, J., Dirnberger, P., Moravec, M., Amrhein, W., Reisinger, M.: High-speed drive for textile rotor spinning applications. IEEE Trans. Ind. Electron. **61**(6), 2990–2997 (2014). http://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=6504511
9. Muthukumar, E., Nisha, K.G.: A study on the effect of material price fluctuations on the profitability of yarn industry in India with special reference to Precot Meridian Ltd. Res. J. Financ. Acc. **5**(19), 134–144 (2014). www.iiste.org/Journals/index.php/RJFA/article/download/16853/17192
10. Gupta, N.: Analysis on the defects in yarn manufacturing process & its prevention in textile industry. Int. J. Eng. Inventions. **2**(7), 45–67 (2013). http://www.ijeijournal.com/papers/v2i7/H02074567.pdf
11. Altas, S., Kadoğlu, H.: Comparison of conventional ring, mechanical compact and pneumatic compact yarn spinning systems. J. Eng. Fibers Fabr. **7**(1), 162–170 (2012). http://www.jeffjournal.org/papers/Volume7/7.1.10.Altas.pdf
12. Koç, E., Kaplan, E.: An investigation on energy consumption in yarn production with special reference to ring spinning. Fibres Text. East. Eur. **15**(4), 18–24 (2007). www.fibtex.lodz.pl/2007/4/18
13. Hasanbeigi, A., Hasanabadi, A., Abdorrazaghi, M.: Energy-efficiency technologies and comparing the energy intensity in the textile industry. In: Industry Reprint version of proceedings of the American Council for an Energy-Efficient Economy's, pp. 26–29 (2011)
14. Hasanbeigi, A., Price, L.: A review of energy use and energy efficiency technologies for the textile industry. Renew. Sustain. Energy Rev. **16**, 3648–3665 (2012). https://publications.lbl.gov/islandora/object/ir:158360/datastream/PDF

15. Shyjith, K., Ilangkumaran, M., Kumanan, S.: Multi-criteria decision-making approach to evaluate optimum maintenance strategy in textile industry. J. Qual. Maintenance Eng. **14**(4), 375–386 (2008). www.emeraldinsight.com/doi/abs/10.1108/13552510810909975
16. Joseph, J., Vetrivel, M.A.: Impact of target costing and activity based costing on improving the profitability of spinning mills in Coimbatore. J. Contemp. Res. Manag. **7**(2), 41–56 (2012). http://www.psgim.ac.in/journals/index.php/jcrm/article/download/226/215
17. Shakil, M., Ullah, M.R., Lutfi, M.: Process flow chart and factor analysis in production of a jute mills. J. Ind. Intell. Inf. **1**(4), 247–254 (2013). www.jiii.org/uploadfile/2013/1118/20131118105220639
18. Khan, M.K.R., Hossain, M.M.: An experimental investigation of the effects of some process conditions on ring yarn breakage. IOSR J. Polym. Text. Eng. **2**(2), 29–33 (2015). www.iosrjournals.org/iosr-jpte/papers/Vol2-issue2/D0222933

Analysis of Power System Harmonics Using PSNR Metric

Srihari Mandava and Ramesh Varadarajan

Abstract In recent times there has been a wide interest in micro grids. One area of concern in micro grids is the generation of harmonics by active devices such as converters and FACTS devices used for reactive power compensation. The currently available literature focuses on the number of operations and fundamental cycles for estimating harmonics. This usually results in a trade-off between accuracy of estimation and the choice of digital filter parameters. In this work a novel orthogonal frequency division multiplexing (OFDM) principle modified as per the power system scenario has been proposed. Odd harmonics up to 31st order are measured by demodulation as if the power signal is OFDM modulated. All these harmonics are measured using only one cycle of voltage signal. Instantaneous detection of harmonics is made possible using the Discrete Wavelet Transform (DWT) instead of the fast Fourier transforms used in conventional OFDM. DWT is also used for noise elimination before the harmonics are analyzed and the performance of proposed method is analyzed using PSNR under different noise conditions.

Keywords Harmonics · OFDM · Demodulation · FFT · DWT · PSNR

1 Introduction

For nearly one decade, attention towards construction of micro grids has been enormously increased due to the constraint of meeting the power demand. The micro grid power generation is majorly dependent on solar and wind sources. But, the power generated from these resources is variable with respect to environmental changes. This puts the system into unstable condition and many works are available

S. Mandava (✉) · R. Varadarajan
School of Electrical Engineering, VIT University, Vellore, India
e-mail: mandavasrihari@vit.ac.in

R. Varadarajan
e-mail: vramesh@vit.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_12

in literature to mitigate the harmful effects of using various control actions. The common issues in micro grid are the control of voltage level, real power and reactive power and when they are coupled to power grid, harmonics are added into the power lines. The negative effects of harmonics, sub-harmonics and inter harmonics may lead to damage of electrical loads, capacitor failure, over heating of conductors, transformers and electromagnetic radiations losses. Harmonics are also introduced in power lines while transporting the power through non-linear devices along with the consumption through non-linear loads [1].

Frequency variations are likely to occur in power systems and these variations are small in case of synchronous generators while dealing with macro grids. Such variations occur during the load mismatches and speed variations in the turbines energized by various non-renewable sources. But in case of micro grids, the scenario may be erratic because the instability is due to both input power variations and instantaneous control actions within the inverter circuits. The three phase frequencies are maintained same in case of synchronous generators with non-renewable energy sources but when renewable energy sources with inverter circuits are involved in grid, the frequency of the three phases may vary based on the performance of the control system parameters. Many methods are proposed to improve the power quality and stability of micro grids and hybrid grids. Among them, more methods concentrate on the control action of converters and very few methods concentrated on measurement domain. As the power quality fully depends on the control actions, it needs sufficient accuracy in measurement. The parameters such as voltage, current, real power and reactive power can be easily calculated using conventional measurements. But, the difficulty arises while measuring and tracking the fundamental frequency and its associated harmonics involving more challenges.

The effectiveness of all control systems purely based on the measurement of power quality with good accuracy and speed. Adaptive Bacterial Swarm Algorithm (ABSA) was used in [2] to measure the changes in fundamental frequency ad harmonics with more accuracy under dynamic conditions of system. Harmonic state estimation (HSE) using weighted least squares (WLS) was used in [3] for 3D visualizations of estimated bus voltage with respect to harmonic number and bus number. The results in this method are close to the bounds computed using Monte Carlo simulations. A mathematical basis for real time implementations on digital signal processors through a restructured recursive-least-squares technique is presented in [4]. This method had been tested in two DSP test platforms, where it considerably reduced the turnaround time through decoupled recursive-least-squares (DRLS). The phasors and harmonics were estimated with better accuracy when compared with Adaptive Linear Combiner (ADALINE) and Recursive Discrete Fourier transform (RDFT). Wavelet transforms were used in [5] to decompose the input time domain signal into various sub-bands using, and train the CHNN (Continuous Hopfield Neural Network). Harmonics up to 9th order are estimated harmonics along with its phase and amplitudes. An adaptive wavelet neural network to detect the harmonics up to 6th order is estimated with its amplitude and phase in [6]. This method is proved

better than FFT, WNN (wavelet neural network), RBFNN (radial basis function neural network), MLPNN (multilayer perceptron neural network). In [7], multi rate filter banks had been used, which estimate the time dependent harmonics in power converters. Harmonics produced during in rush currents and during the change of firing angle had been captured and plotted. Hilbert transform had been used to perform SSB (Single Side Band) modulation to estimate even harmonics. Odd harmonics detection up to 15th harmonic had been done. The instantaneous phase tracking using demodulation method is proposed in [8] and the performances are analyzed by involving various FIR and IIR filters for testing. In this, the design of low pass filters plays a great role in estimation accuracy. The same demodulation-based scheme had been used in [9] to find the frequency of power signal under the influence of the interfering tones. In addition to this, magnitude and frequency of the interfering tones were evaluated. Interfering tones were considered up to 29 Hz while the fundamental frequency was 60 Hz. Frequency and amplitude of harmonics in DFIG (Doubly Fed Induction Generators)-based micro grids are estimated in [10] which is generated in DFIG due to mechanical design of induction machines and Rotor side converters (RSC). Kashyap et al. in [11] estimated harmonics up to 11th order under white Gaussian noise using signal processing algorithm called Variable Constraint-based Least Mean Square (VCLMS) and showed a MSE (Mean Square of 0.0257 at no noise condition. As per the standards of signal processing the MSE should be less than 0.009 and this shows the poor performance of the measurement process flow. A recursive wavelet-based algorithm (IRWT) was introduced in [12] utilizing a new mother wavelet function and overall estimating procedure is used to find the amplitude, phase angle and frequency in power systems. The work in [13, 14] uses Recursive-Least-Square (RLS) harmonic estimation technique and in [15], an Improved Recursive Newton Type (IRNTA) algorithm is implemented to estimate the fundamental frequency.

In [16], the demodulation method is modified to improve the accuracy of harmonics detection following the changes in fundamental frequency. It needs only two cycles of input and an FIR filter in a controlled manner to know the variations in the fundamental frequency and its associated harmonics. The main draw back in this method is that it can estimate only one harmonic for each step as each estimation of harmonic needs a separate carrier frequency. For example, it needs 29 steps to estimate harmonics up to 29th order by generating 29 different carrier frequencies. After the power signal is demodulated and low pass filtered, the frequency and the phase of the *m*th harmonic is estimated as follows.

The method in [16] is purely dependent on tuning the low pass filter and the amplitudes and phase angle of harmonics up to 29th order were captured with a Maximum Absolute Error (MAE) as less as 0.5% when the fundamental frequency varies between 59.5 and 60.5 Hz. In this paper, an attempt is made to measure harmonics by using the principle of OFDM receiver part. This method helps to achieve a better control over stability in power quality parameters. It de-noise the input power signals and decomposes the power signal using wavelet-based quadrature mirror filters as mentioned in [8].

2 OFDM and Its Application to Power System Harmonics Measurement

In communication scenario, 3G systems inevitably use OFDM principle in order to get rid of signal attenuation due to deep fading. OFDM has transmitter and receiver as shown in Figs. 1 and 2. It was found that multi carrier system along with proper guard band reduces the effect of multi path transmission. The major task in communication would be to transmit and receive the data bits without error and hence the best reproduction of the transmitted voice or multimedia data. The basic technique behind the OFDM is to use multiple carriers without using oscillator circuits to generate various orthogonal frequencies. This orthogonality along with guard band insertion efficiently serves to retrieve the transmitted data. But, the proposed work in this paper is meant especially for a power system application. The sub-carriers dealt in OFDM are considered as harmonics in this method as both of them follow the same orthogonality principle. Another important point is the modulation stages in OFDM. There exist two modulation stages, namely, baseband modulation with various sub-carriers and carrier modulation at a single frequency which is far higher than the sub-carrier frequencies. In power system signals, the fundamental frequency is 50 or 60 Hz and inclusion of harmonics may be viewed as baseband modulation done with various orthogonal frequency signals. So, it is very apparent that power signals are not carrier modulated, but only baseband modulated.

In this work, firstly it is assumed that a power signal is modulated by various sub-carriers, i.e. harmonics. The harmonics are then estimated and measured same like the sub-carriers estimation in the OFDM receiver part. The only difference is reconstruction of binary data stream is not necessary since there is no data transmission involved as in the case of typical communication systems. Very few works are present for detecting the harmonics of a signal under noise conditions and the steps for identifying the harmonics of power signal under noise conditions using the proposed method are shown in Fig. 3.

Fig. 1 OFDM transmitter

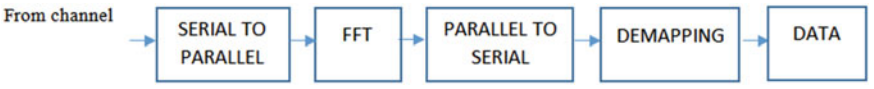


Fig. 2 OFDM receiver

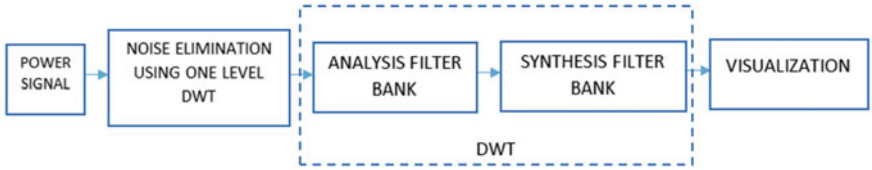


Fig. 3 OFDM-based harmonic visualization

1. De-noise the input power signals using certain new stage of preliminary DWT.
2. Decompose the power signal using analysis filter using wavelet-based quadrature mirror filters.
3. Reconstruct the decomposed signals using synthesis filter banks to visualize the time varying harmonic content as per the gray code sequence in Table 2.

The proposed method can also be applied for micro grid environment to visualize the time varying harmonic content. The performance of the proposed method is analyzed using a metric called Peak Signal to Noise Ratio (PSNR) for different noise conditions.

3 Methodology

Let $x(t)$ be the power signal given by (1).

$$X(t) = A_m(t)\cos(n\Omega_o(t) + \phi_m(t)) + \eta(t) \tag{1}$$

A_m is the amplitude,
Ω_o is the fundamental frequency,
ϕ_m is the phase of the mth harmonic and
$\eta(t)$ is the noise.

Once $X(t)$ is expanded, it resembles (2) in digital form.

$$\begin{aligned} X(n) = {} & A_1(n)\cos(\omega_o(n) + \phi_1(n)) + A_3(n)\cos(3\omega_o(n) + \phi_3(n)) + \cdots \\ & A_{31}(n)\cos(31\omega_o(n) + \phi_{31}(n)) \end{aligned} \tag{2}$$

The amplitude values (A_1, A_2 … A_{31}) considered are shown in Table 1.

The noise $\eta(t)$ is normally filtered using low pass filter. But in the proposed method of wavelet-based decomposition, the noise is filtered out in the preliminary stage using a one level decomposition. Then, the analysis bank and synthesis bank are applied on the signal as shown in Figs. 4 and 5. The sampling frequency of the filter banks is chosen as $f_s = (2^{N+2} \cdot f_0)$ where, f_0 is the fundamental frequency

Table 1 Amplitude values of various harmonic order

Amplitude	Values	Amplitude	Values
$A_1(n)$	1	$A_{17}(n)$	1/17
$A_3(n)$	1/3	$A_{19}(n)$	1/19
$A_5(n)$	1/5	$A_{21}(n)$	1/21
$A_7(n)$	1/7	$A_{23}(n)$	1/23
$A_9(n)$	1/9	$A_{25}(n)$	1/25
$A_{11}(n)$	1/11	$A_{27}(n)$	1/27
$A_{13}(n)$	1/13	$A_{29}(n)$	1/29
$A_{15}(n)$	1/15	$A_{31}(n)$	1/31

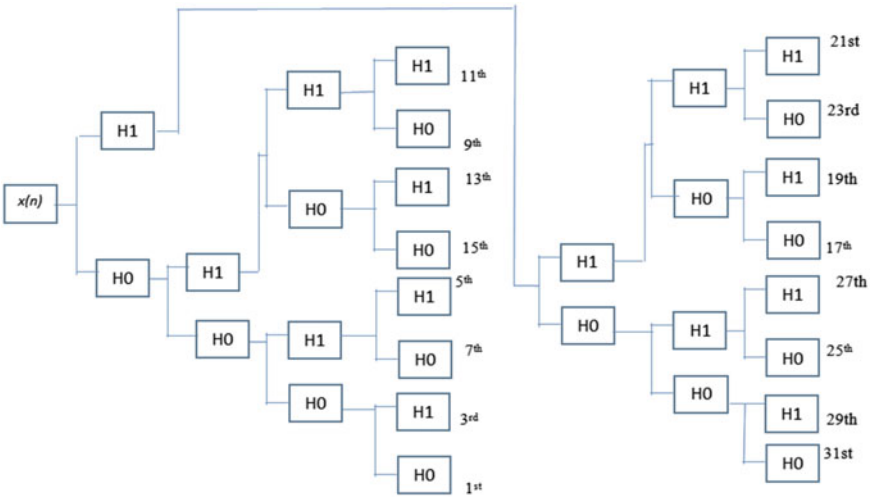


Fig. 4 Structure of analysis bank up to 31st harmonic order

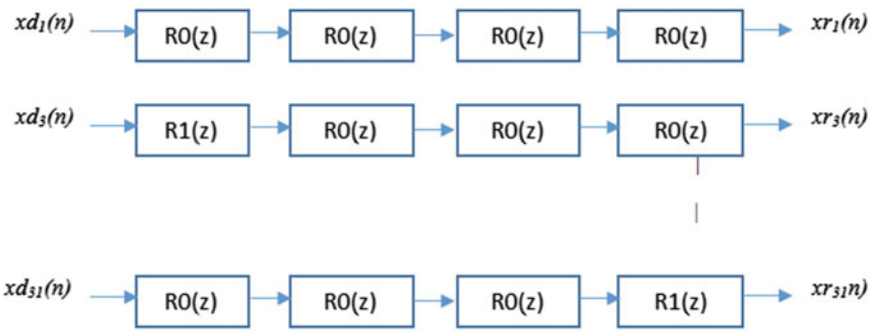


Fig. 5 Synthesis bank constructed upto 31st harmonic order

Table 2 Gray code and it filter bank transfer function

Gray code and transfer function of analysis filter bank		Gray code and transfer function of synthesis filter bank		Harmonic order
0000	$H_0(z)\ H_0(z)\ H_0(z)\ H_0(z)$	0000	$H_0(z)\ H_0(z)\ H_0(z)\ H_0(z)$	1
0001	$H_0(z)\ H_0(z)\ H_0(z)\ H_1(z)$	1000	$H_0(z)\ H_0(z)\ H_0(z)\ H_1(z)$	3
0011	$H_0(z)\ H_0(z)\ H_1(z)\ H_1(z)$	1100	$H_0(z)\ H_0(z)\ H_1(z)\ H_1(z)$	5
0010	$H_0(z)\ H_0(z)\ H_1(z)\ H_0(z)$	0100	$H_0(z)\ H_0(z)\ H_1(z)\ H_0(z)$	7
0110	$H_0(z)\ H_1(z)\ H_1(z)\ H_0(z)$	0110	$H_0(z)\ H_1(z)\ H_1(z)\ H_0(z)$	9
0111	$H_0(z)\ H_1(z)\ H_1(z)\ H_1(z)$	1110	$H_0(z)\ H_1(z)\ H_1(z)\ H_1(z)$	11
0101	$H_0(z)\ H_1(z)\ H_0(z)\ H_1(z)$	1010	$H_0(z)\ H_1(z)\ H_0(z)\ H_1(z)$	13
0100	$H_0(z)\ H_1(z)\ H_0(z)\ H_0(z)$	0010	$H_0(z)\ H_1(z)\ H_0(z)\ H_0(z)$	15
1100	$H_1(z)\ H_1(z)\ H_0(z)\ H_0(z)$	0011	$H_1(z)\ H_1(z)\ H_0(z)\ H_0(z)$	17
1101	$H_1(z)\ H_1(z)\ H_0(z)\ H_1(z)$	1011	$H_1(z)\ H_1(z)\ H_0(z)\ H_1(z)$	19
1111	$H_1(z)\ H_1(z)\ H_1(z)\ H_1(z)$	1111	$H_1(z)\ H_1(z)\ H_1(z)\ H_1(z)$	21
1110	$H_1(z)\ H_1(z)\ H_1(z)\ H_0(z)$	0111	$H_1(z)\ H_1(z)\ H_1(z)\ H_0(z)$	23
1010	$H_1(z)\ H_0(z)\ H_1(z)\ H_0(z)$	0101	$H_1(z)\ H_0(z)\ H_1(z)\ H_0(z)$	25
1011	$H_1(z)\ H_0(z)\ H_1(z)\ H_1(z)$	1101	$H_1(z)\ H_0(z)\ H_1(z)\ H_1(z)$	27
1001	$H_1(z)\ H_0(z)\ H_0(z)\ H_1(z)$	1001	$H_1(z)\ H_0(z)\ H_0(z)\ H_1(z)$	29
1000	$H_1(z)\ H_0(z)\ H_0(z)\ H_0(z)$	0001	$H_1(z)\ H_0(z)\ H_0(z)\ H_0(z)$	31

(50 Hz) of the power systems and N is the number of decomposition levels (Table 2).

Mother wavelets of type "dmey" are used in analysis bank and synthesis bank and harmonics up to 31st order are measured and visualized with $N = 4$, i.e. $(2^{N+1} - 1)\ f_0 = (2^{4+1} - 1)\ 50 = 31$.

4 Results

The specialty of the QMF-based separating the input power signal as sub-band is that, it does not need any reference signal as generated in [5]. The decomposition and reconstruction up to four levels spontaneously output the harmonic order up to 31. Tuning of filter banks is not required in the proposed method as in [5]. The harmonics obtained through the MALTAB simulations are shown in Figs. 6 and 7.

Apart from the values set as per Table 1, time varying nature of harmonics have been analyzed in this work to check the visualization performance. The following changes are made for the harmonics in the input signal.

1. Harmonics of order 1, 3 and 31 are allowed in input from the time 0.005–0.003 s.
2. Harmonic of order 5 is allowed in input from 0.1563 to 0.3122 s.
3. Harmonics of order 7 and 25 is allowed in input from 0.3125 to 0.4684 s.

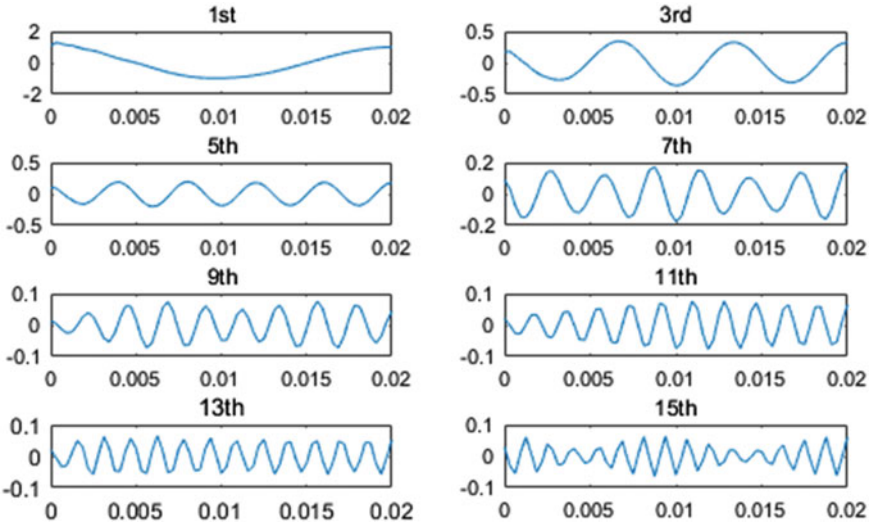


Fig. 6 Visualized harmonics up to 15th order

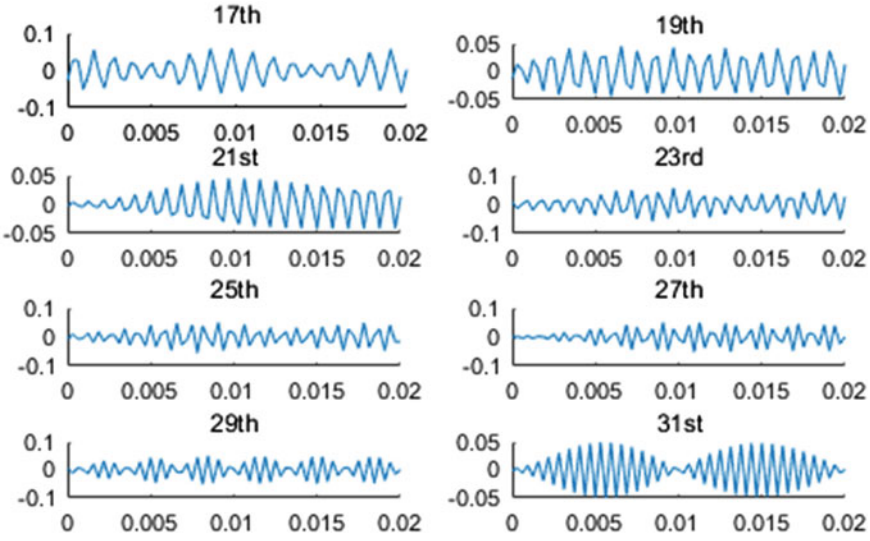


Fig. 7 Visualized harmonics from 17th to 31st order

The results obtained with the modified input are shown in Fig. 8. The changes made for each harmonics signal are clearly seen in the output with the proposed methods which say that the proposed method works satisfactory with time varying harmonics.

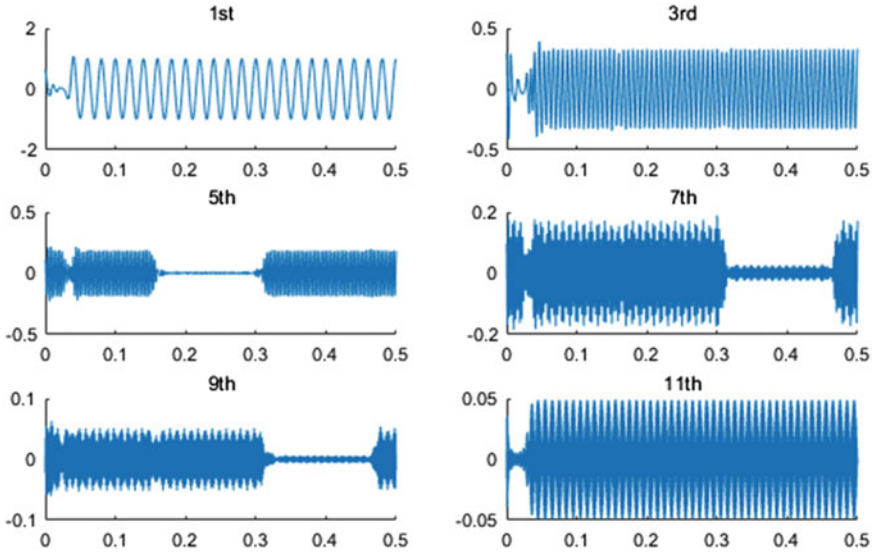


Fig. 8 Visualized time varying harmonics up to 31 harmonics

5 Performance Analysis

PSNR metric had been originally used in EEG reconstruction in [14]. Since visual-based harmonic tracking is performed in this work, a new metric namely, VBAE (Visual-Based Absolute Error) is proposed and it is defined as the difference between the peak value of the original and peak value of the reconstructed signal. It is given by (3).

$$V_{\mathrm{BAE}} = \left| X_m - X'_m \right| \tag{3}$$

where, X_m is the peak value of the original signal and X'_m is the peak value of the reconstructed signal. Though this metric is very sufficient for visualization-based applications, this measure does not provide information regarding the amount of error in the other samples, and hence it is local in nature. It is not meaningful to compare directly V_{BAE} of power signal of different sampling resolutions. Hence, it is essential to normalize the signal range leading to a distortion measure called as PSNR expressed in dB as shown in (4). Higher the PSNR, better is the visualization. The PSNR is given by

$$\mathrm{PSNR} = 10 \log_{10} \left(\frac{(2^Q - 1)}{V_{\mathrm{BAE}}} \right) \tag{4}$$

Figure 9 shows the variation of obtained PSNR for various harmonic order from 1 to 31. Red trace shows the performance of the harmonic visualization when AWGN was set at 10, 20 and 30 dB, respectively. Black trace shows the improved

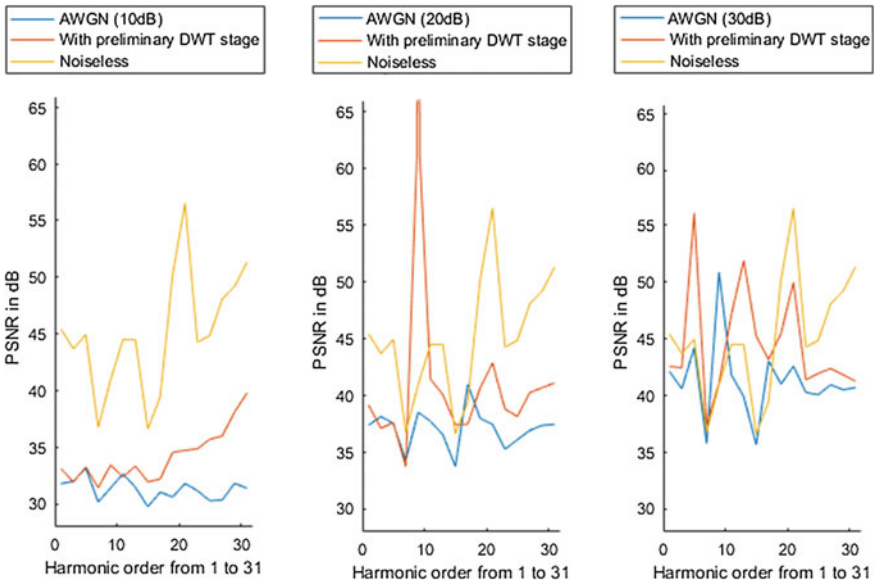


Fig. 9 PSNR performance at 10 dB of AWGN

Table 3 PSNR obtained for various noise levels

Harmonic order	PSNR (dB) (at A_{wgn} = 10 dB)		PSNR (dB) (at A_{wgn} = 20 dB)		PSNR (dB) (at A_{wgn} = 30 dB)		PSNR without noise
	With noise	After DWT	With noise	After DWT	With noise	After DWT	
1	31.8208	33.1315	37.3875	39.1656	42.1284	42.5685	45.4302
3	32.0308	31.9599	38.1644	37.1261	40.6032	42.4521	43.6901
5	33.1803	33.2847	37.5249	37.6330	44.2112	56.0784	44.9502
7	30.2049	31.4517	34.2795	33.7447	35.7967	37.4455	36.7766
9	31.4394	33.4551	38.5368	64.1388	50.8674	41.0891	40.9655
11	32.6885	32.4028	37.7276	41.4294	41.8145	47.1478	44.5053
13	31.4971	33.3619	36.5399	40.0741	39.8942	51.9150	44.4918
15	29.7857	31.9769	33.7618	37.4416	35.6765	45.2361	36.6186
17	31.0707	32.2256	40.9983	37.4847	43.0540	43.1676	39.4557
19	30.6411	34.5711	37.9957	40.6725	41.0086	45.4834	50.2059
21	31.8326	34.7487	37.4657	42.8831	42.5922	49.9832	56.5141
23	31.1952	34.8844	35.2829	38.8182	40.2845	41.3995	44.2699
25	30.3132	35.7315	36.1121	38.1644	40.0798	41.9564	44.8689
27	30.3793	36.0182	36.9336	40.2675	40.9514	42.3863	48.0778
29	31.8434	38.1273	37.3838	40.6997	40.5259	41.8427	49.2025
31	31.4167	39.8068	37.4658	41.1134	40.7017	41.2681	51.3208
Mean PSNR	31.3337	**34.1961**	37.0975	**40.6786**	41.2619	**44.4637**	**45.0840**

PSNR using the proposed method. From Table 3, an average PSNR improvement of 3 dB has been obtained when a preliminary DWT-based noise filtering is employed. An average PSNR obtained at an ideal noiseless condition is 45.0840 dB and a PSNR of 44.4637 dB is obtained at a noise level of AWGN = 30 dB. This clearly says that the performance of filters depends on the amount of noise added in the power signal.

6 Conclusion

This paper presented a novel harmonic estimation method using DWT, which mimics OFDM receiver principle mitigating the effect of noise. A preliminary DWT-based one level decomposition has been proposed in this work to improve the harmonic visualization performance and an average of 3 dB improvement had been achieved. Moreover, the proposed work takes only one full cycle of the input power signal. Wavelet type of "dmey" has been used in our proposal, and further research is required in optimizing the type of mother wavelets and to improve the visual performances because of sampling rate mismatches. This work is highly suitable for visualization applications and outputs are obtained at one step process irrespective of the number of harmonics to be visualized. This work could be a better tool, to further apply this measurement method for typical control actions in micro grid in order to maintain the power quality. Works presented in this paper suffers from the down sampling effect which spoils the visualization performance. An optimal sampling frequency of 3.2 kHz considered in this paper.

References

1. Tolbert, L.M., Hollis, H.D., Hale, Jr., P.S.: Survey of harmonics measurements in electrical distribution systems. IEEE IAS Annual Meeting, San Diego, CA, pp. 2333–2339 (1996)
2. Ji, T.Y., Li, M.S., Wu, Q.H., Jiang, L.: Optimal estimation of harmonics in a dynamic environment using an adaptive bacterial Swarming algorithm. IET Gener. Trans. Distrib. **5**(6), 609–620 (2011)
3. Rakpenthai, C., Uatrongjit, S., Watson, N.R., Suttichai, P.: On harmonic state estimation of power system with uncertain network parameters. In: Transmission & Distribution Conference and Exposition, IEEE Power and Energy Society, Chicago, IL, pp. 0885–8950 (2014)
4. Sadinezhad, I., Agelidis, V.G.: Real-time power system phasors and harmonics estimation using a new decoupled recursive-least-squares technique for DSP implementation. IEEE Trans. Ind. Electron. **60**(6), 2295–2308 (2013)
5. Marques, C.A.G., Ribeiro, M.V., Duque, C.A., Ribeiro, P., Da Silva, E.A.B.: A controlled filtering method for estimating harmonics of off-nominal frequencies. IEEE Trans. Smart Grid. **3**(1), 38–49 (2012)
6. Maofa, G., Xiaocong, L., Longqing, C., Liming, G., Guoliang, L.: Harmonic analysis approach based on wavelet transform and neural network. In: 4th International Conference on

Electric Utility Deregulation and Restructuring and Power Technologies (DRPT), Weihai, China, pp. 774–576 (2011)
7. Jain, S.K., Singh, S.N.: Low-order dominant harmonics estimation using adaptive wavelet neural network. IEEE Trans. Ind. Electron. **61**(1), 428–435 (2013)
8. Duque, C.A., Silveira, P.M., Ribeiro, P.F.: Visualizing time varying harmonics using filter bank. Electr. Power Syst. Res. **81**(4), 974–983 (2011)
9. Djuric, P.M., Begovic, M.M., Doroslovaeki, M.: Instantaneous phase tracking in power networks by demodulation. IEEE Trans. Instrum. Meas. **41**(6), 314–319 (1992)
10. Kamwa, I., Leclerc, M., McNabb, D.: Performance of demodulation-based frequency measurement algorithms used in typical PMUs. IEEE Trans. Power Deliv. **19**(2), 505–514 (2004)
11. Kashyap, S., Singh, A.K.: Most suitable mother wavelet for measurement of power system harmonics using DWT in view of IEEE standard. In: 13th International Conference on Harmonics and Quality of Power, Wollongong, Australia, pp. 1459–2000 (2008)
12. Jaipradidtham, C., Kinnares, V.: Harmonic flow analysis of HV DC systems for discrete wavelet transform with advanced of the harmonic impedances and voltage source transients model of AC-DC converters. In: TENCON, IEEE Region 10 Conference, Hong Kong, China, pp. 1–4 (2006)
13. Bodhe, R., Joshi, S., Narkhede, S.: Comparative analysis of the BER performance of DWT OFDM over that of FFT OFDM in presence of phase noise. In: International Conference on Robotics, Automation, Control and Embedded Systems, Chennai, India, pp. 18–20 (2015)
14. Srinivasan, K., Dauwels, J., Ramasubba Reddy, M.: Multichannel EEG compression: wavelet based image and volumetric coding approach. IEEE J. Biomed. Health Inform. **17**(1), 113–120 (2013)
15. Abdullah, K., Kamarudin, S.I., Hussin, N.F., Jarrot, S.P.W., Ismail, A.F.: Impulsive noise effects on DWT-OFDM versus FFT-OFDM. In: IEEE 17th Asia-Pacific Conference on Communications, Sabah, Malaysia, pp. 488–491 (2011)
16. Agrawal, Sanjay, Mohanty, Soumya R., Agarwal, Vineeta: Harmonics and inter harmonics estimation of DFIG based standalone wind power system by parametric techniques. Int. J. Electr. Power Energy Syst. **67**(1), 52–65 (2015)

Low Power Circularly Polarized Wearable Rectenna for RF Energy Harvesting

B. Naresh, Vinod Kumar Singh and V. Bhargavi

Abstract In this communication, an ameliorate textile circularly polarized (CP) rectenna for harvesting the emitted RF energy in INSAT band is presented. The textile antenna is bendable, robust, and low mass so that it can be weaving into clothes of the smart soldier to charge the portable electronic devices in the battlefield. Weight burden on the soldiers is significantly reduced; indeed power handling capacity is increased by integrating the textile rectifying antenna into soldier clothes. The proposed textile rectenna has a 10-dB return-loss bandwidth of 1200 MHz (6.6–7.8 GHz) with the maximum gain 8.14 dB an overall size of 50×50 1.076 mm^3. This antenna is suitable for INSAT band (6.725–7.025 GHz) RF energy harvesting operations. Measurement results are also shown with theoretical predictions, both of which are in quite good agreement.

Keywords Circularly polarized · INSAT band · Smart soldiers
Textile rectenna · RF energy

1 Introduction

The main motive to design and fabricate the textile rectifying antenna (wearable rectenna) is to harvest the emitted radio frequency energy available in the surrounding environment of the soldier. Numerous wearable rectenna configurations with linearly and circularly polarized characteristic by utilizing different substrate

B. Naresh
Department of Electrical Engineering, Bhagwant University, Ajmer, Rajasthan, India
e-mail: nareshbangari@gmail.com

V.K. Singh (✉)
Department of Electrical Engineering, SR Group of Institutions, Jhansi, UP, India
e-mail: singhvinod34@gmail.com

V. Bhargavi
Government of India, Jhansi, UP, India
e-mail: bhargavivanga1990@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_13

material for RF energy harvesting are reported. Magneto dielectric multi-layer multi-resonant rectenna [1], Dual-band SIW textile antenna with integrated solar harvester [2], Flectron self-adhesive circularly polarized wearable antenna for 2.45 GHz, performance effect of textile antennas interface with human body at millimeter wave frequencies [3–6]. For rescue and military operations wearable antennas are most promising appliance due to invention of portable devices. The electronics of the future will require less power and will draw more of that power from environmental sources.

In RF energy harvesting application, circularly polarized antennas are more preferable over the linearly polarized antennas due to its liberty of orientation. For a line-feed microstrip antenna, CP character can be achieved by loading appropriate slots or slits in the radiating element of the antenna [7–11]. Energy Harvesting (EH) technology will continue to become more resourceful and sooner will be tomorrow's power source for many applications. Today, micro scale EH is generally used to charge batteries, or other energy storage devices. EH technology has particular applicability to sensors that are located in remote, isolated, or environmentally extreme locations without any type of primary power.

In this communication, a novel wearable rectifying antenna for RF energy harvesting to power the micro powered sensor system is presented. To harvest the RF energy there are several techniques, in which Schottky diode and CMOS-based rectification are popular methods. The CP antenna has a dB impedance band covering the INSAT band (6.725–7.025 GHz). The rectenna, together with wearable antenna and rectifier, has been experimentally evaluated at different dBm power levels with a distance of one meter from transmitter.

2 Antenna Configuration

Figure 1 shows the design of the proposed planar textile antenna with defected ground structure. The proposed antenna is fabricated on a textile substrate (jeans) with relative permittivity $\varepsilon_r = 1.7$, thickness $h = 1$ mm, and dielectric loss tangent $\tan \delta = 0.025$ [9]. Conductive Copper tape is used to design the radiating element and the same for ground plane with 0.03 mm thickness. Copper and jeans both materials have the property of being extremely flexible and rigid, so that it can effortlessly integrate into soldier clothes. The proposed antenna contains a rectangular slot of 120×50 mm^2 by truncating a pair of patch corners of equal side length $\Delta L = 12$ mm for producing line-feed CP operation as shown in Fig. 1; on which rectangular etched slot of 100×25 mm^2 is constructed for integration with a flexible solar cell in future to make hybrid energy harvesting system. So that two different energy sources can be utilized in one platform. The partial ground plane is located on the backside of the textile substrate with the overall dimensions of 100×25 mm^2. The antenna is fed by a 50 Ω microstrip line with a width 3.2 mm and length 30 mm. CST microwave studio software is used to study the characteristics of proposed antenna and also optimization technique is used to obtain 6.8 GHz resonance frequency.

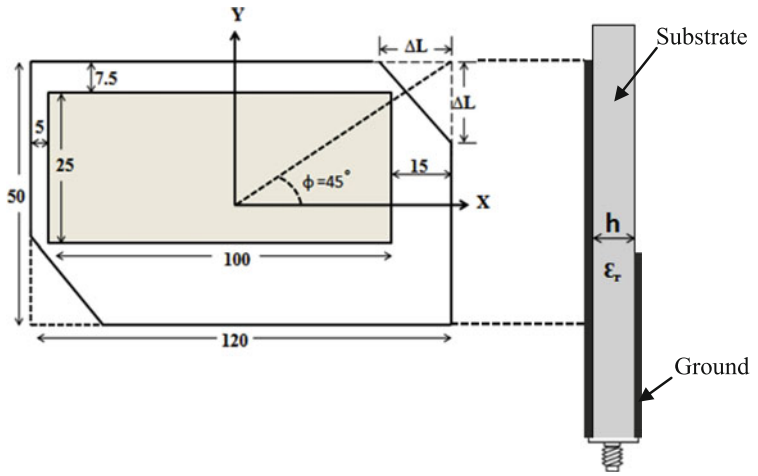


Fig. 1 Geometry of a compact circularly polarized rectangular microstrip antenna with a pair of truncated corners (all dimension in mm)

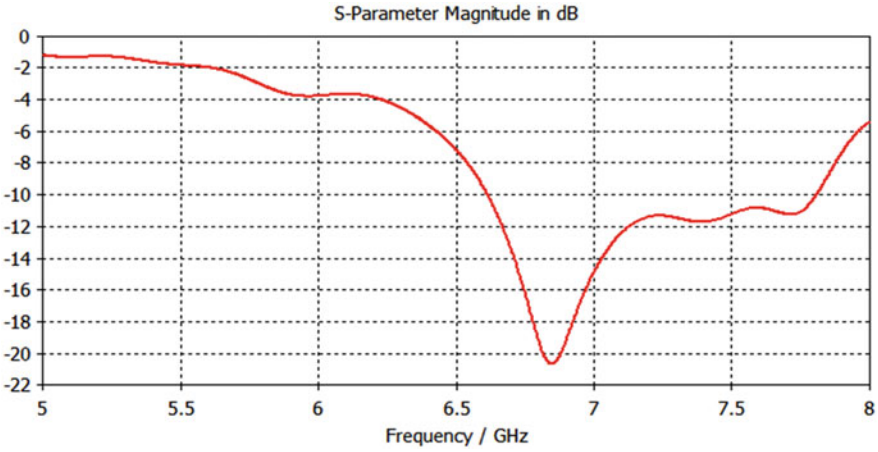


Fig. 2 Simulated return loss versus frequency plot of CP wearable rectenna

Designed antenna has wide impedance bandwidth covering the INSAT receiving band so that textile antenna can easily integrate into clothing and it is two dimensional. The proposed antenna configuration was numerically investigated and optimized using the CST microwave studio. The simulated result of return loss is shown in Fig. 2. It is observed that the proposed antenna is resonating at 6.84 GHz with return loss of −20 dB, giving an impedance bandwidth of 1200 MHz (6.6–7.8 GHz). The simulation result of impedance and gain are shown in Fig. 3a, b. The real part of the

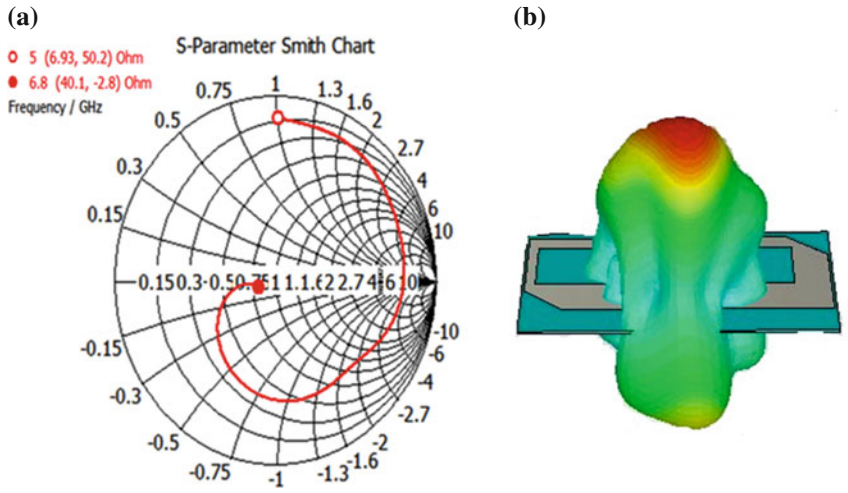


Fig. 3 Smith chart and gain in 3D of proposed CP wearable antenna at 6.8 GHz

impedance at the resonant frequency 6.8 GHz is 40.1 Ω, close to 50 Ω in the desired range of frequency band. The reactive part of the impedance is 2.85 Ω, it is inductive.

3 Rectenna Design

The rectenna design essentially consists of three parts: antenna, matching network, and rectifying circuit. The proposed rectenna design is based on 50 Ω interface. The power incident on the antenna will be reflected back to the environment if impedance of rectenna circuit is not properly matched to its antenna. To match the impedance between the antenna and the rectifier diode is done by input filter and the harmonics generated by rectifier will be rejected by output low pass filter. Low power level series mounted diode rectifier structure is shown in Fig. 4a, b. Dimensioning of passive components used to design the filter elements are optimized by using Agilent's ADS software [12–15].

4 Results Analysis

The proposed circularly polarized wearable rectenna has been fabricated and anechoic chamber is used to carry out the experiments. An Agilent E5071C ENA series vector network analyzer was used to determine the electrical performance of the

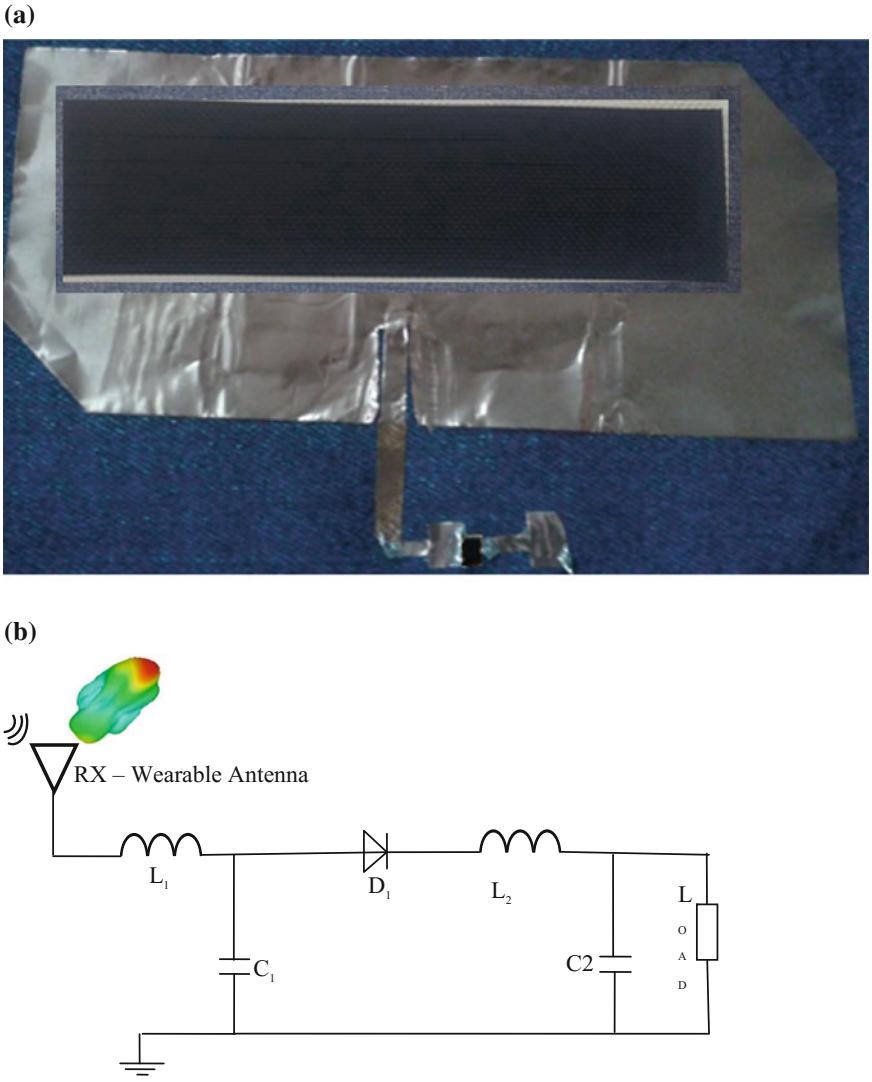


Fig. 4 **a** Photograph of the fabricated CP wearable rectenna **b** schematic view of RF energy harvesting system

proposed textile antenna such as return loss, axial ratio, and gain. The distance (D_r) between the transmitting horn antenna (G_{tX} = 11 dBi) and the rectenna is one meter. The Friis transmission equations (1) and (2) are used to find out the output DC voltage and overall efficiency of the rectenna against power density.

$$P_{rX} = P_{tX} G_{tX} G_{rX} \left(\frac{C}{4\pi D_t f_0} \right)^2 \tag{1}$$

$$P_{tX} = \frac{E^2 r^2}{30} \tag{2}$$

where P_{tX} is the transmitting power at a given field strength E (mV/m); G_{rX} is the receiving antenna gain; so the RF–DC conversion efficiency is calculated by Eq. (3).

$$\eta_{EH} = \frac{P_{outDC}}{P_{rX}} = \frac{V_{outDC}^2 / R_L}{P_{rX}} \tag{3}$$

To determine the DC output voltage obtained at the rectifier end HP 83752b sweeper is connected and positioned to produce a 6.8 GHz frequency with the power −15 to 15 dBm levels. By conducting this experiment CP wearable rectenna, electrical performance is obtained in terms of output power, efficiency, and dc voltage with a fixed distance of one meter. Figure 5a, b shows the comparison results of measured and simulated return loss and axial ratio, respectively. Flexible solar cell is to be integrated with this rectenna to make is device as multi energy harvesting system in future. Table 1 shows the recorded values by the rectenna circuit.

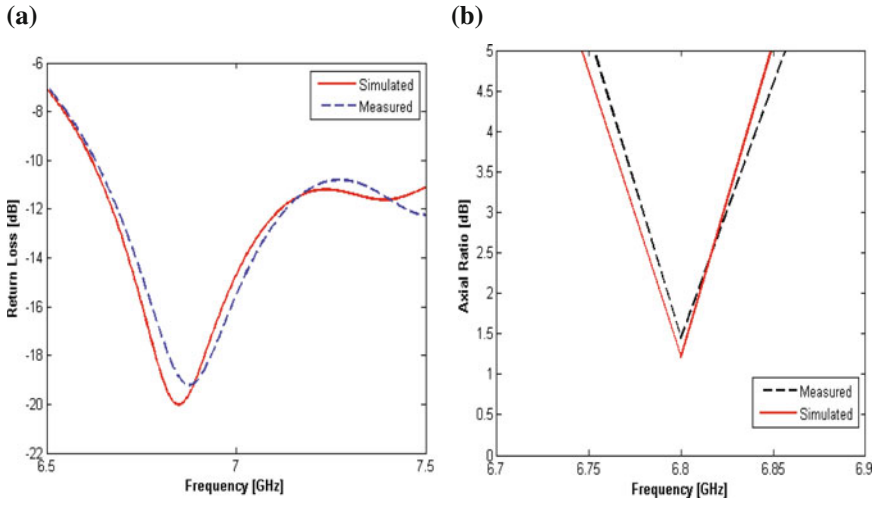


Fig. 5 Comparison of measured and simulated results of proposed CP wearable antenna

Table 1 Measured DC voltage from rectifying circuit

Transmitted power (dBm)	Received power (dBm)	Voltage (V)	P_{outDC}	Efficiency η_{EH} (%)
−15	−16.5	15.4 mV	$0.7208e^{-5}$	17.3
−10	−11.5	42.3 mV	$2.208e^{-5}$	26.7
−5	−6.5	83.7 mV	$6.879e^{-5}$	32.8
0	−1.5	191.6 mV	$4.376e^{-4}$	52
5	3.5	387.2 mV	$1.826e^{-3}$	61.4
10	8.5	0.808 V	$5.195e^{-3}$	72.16
15	13.5	2.25 V	$42.632e^{-3}$	81.6

5 Summary

Power required to operate the portable and microelectronic devices is now a reality by means of energy harvesting technology. In this paper line-feed circularly polarized wearable antenna with low power RF to DC rectifier is proposed. Microstrip antenna, defected ground, and feed line structure are optimized to 6.8 GHz resonance frequency operation. The low power rectenna, based on a series diode circuit has been tested which has recorded efficiency of 81.6% with 13.5 dBm received power. Low pass filter is directly connected to textile rectenna terminals.

References

1. Costanzo, A., Masotti, D., Aldrigo, M.: Compact Wearable Antennas for Battery-Less Systems Exploiting Fabrics and Magneto-Dielectric Materials, vol. 3, pp. 474–490 (2014)
2. Lemey, S., Declercq, F., Rogier, H.: Dual-band substrate integrated waveguide textile antenna with integrated solar harvester. IEEE Antennas Wirel. Propag. Lett. **13**(1), 269–272 (2014)
3. Lui, K.W., Murphy, O.H., Toumazou, C.: A wearable wideband circularly polarized textile antenna for effective power transmission on a wirelessly-powered sensor platform. IEEE Trans. Antennas Propag. **61**(7), 3873–3876 (2013)
4. Chahat, N., Zhadobov, M., Sauleau, R.: Antennas for body centric wireless communications at millimeter wave frequencies. Progress Compact Antennas. ISBN 978-953-51-1723-0 (2014)
5. Din, N.M., Chakrabarty, C.K., Bin Ismail, A., Devi, K.K.A.: Design of RF energy harvesting system for energizing low power devices. Prog. Electromagnet. Res. **132**, 49–69 (2012)
6. Baiya, D.: On the Development of Conductive Textile Antennas-Thesis (2014)
7. Salvado, R., Loss, C., Gonçalves, R., Pinho, P.: Textile materials for the design of wearable antennas: a survey. sensors **12**(11), 15841–15857 (2012)
8. Rafsec, U.P.M.: Tutorial Overview of Inductively Coupled RFID Systems. Available online at: www.rafsec.com/rfidsystems.pdf (2003)
9. Gupta, N., Singh, V.K., Ali, Z., Ahirwar, J.: Stacked textile antenna for multi band application using foam substrate. In: International Conference on Computational Modelling and Security (CMS 2016), Procedia Computer Science, vol. 85, pp. 871–877 (2016)

10. Singh, N.K., Singh, V.K., Naresh, B.: Textile antenna for microwave wireless power transmission. In: International Conference on Computational Modelling and Security (CMS 2016), Procedia Computer Science, vol. 85, pp. 856–861 (2016)
11. Osman, M.A.R., Abd Rahim, M.K., Azfar Abdullah, M., Samsuri, N.A., Zubir, F., Kamardin, K.: Design, implementation and performance of ultra-wideband textile antenna. Prog Electromagnet. Res. B **27**, 307–325 (2011)
12. Marian, V., Allard, B., Vollaire, C., Verdier, J.: Strategy for microwave energy harvesting from ambient field or a feeding source. IEEE Trans. Power Electron. **27**, 4481–4491 (2012)
13. Singh, N., Singh, A.K., Singh, V.K.: Design and performance of wearable ultra wide band textile antenna for medical applications. Microwave Opt. Technol. Lett. **57**(7), 1553–1557 (2015)
14. Singh, V.K., Ali, Z., Singh, A.K., Ayub, S.: A wideband compact microstrip antenna for DCS/PCS/WLAN applications. In: Intelligent Computing, Networking, and Informatics, pp. 1107–1113. Springer, India, (2014). ISBN: 978-81-322-1664-3
15. Singh, V., Ali, Z., Ayub, S., Singh, A.: Bandwidth optimization of compact microstrip antenna for PCS/DCS/bluetooth application. Central Eur. J. Eng., Springer **4**(3), 281–286 (2014)

Performance Analysis of Series-Passive Filter in 5-Phase PWM Inverter Drive and Harmonic Study Using Simulink/Matlab

A.S. Ananda and Manjesh

Abstract Maintaining IEEE Harmonic standards in all Motor drives is most critical while designing. Harmonics has major effects on the output of all the inverters. Several filters are used to suppress the harmonics, there are few drawbacks, increasing number of the components used in the design and bulky circuit components. In the inverters, suppression of all harmonics is the major issue due to its inevitable effect on the load. Series-passive filter is the reliable filter used to reduce the THD. Advancement in the power systems leads to a five phase inverter drives due to applications and advantages over three phase loads. This work represents the performance evaluation of Series-passive filter in 5-phase PWM inverter, reductions of Total Harmonics Distortion are obtained using Simulink/Matlab, and same has been presented.

Keywords Inverter drive · THD · Harmonics · Five phase · Filters
Series-passive filter

1 Introduction

Multi/Poly phase induction motors have wide range of applications in industries and aircraft applications due its high torque and low maintenance by reducing the amplitude, current per phase, and DC-link current harmonics, at the same time there is increase in few other parameters like frequency of torque pulsation, voltage per phase, reliability, and fault tolerance [1–5]. Harmonics at the load connected to inverter with long cable creates voltage sags, which are very dominant factors in affecting the performance of the induction motor drive. Therefore, the system deteriorates efficiency of the motor and causes voltage imbalance in the windings of

A.S. Ananda (✉) · Manjesh
Bangalore University, Bengaluru, India
e-mail: a.sanand@yahoo.com

Manjesh
e-mail: manjesh1972@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_14

the induction motor which intern generates and ripple voltages in converter and inverter systems output.

Harmonic contents are polluting the power system loads by superimposing both in current and voltages in the inverter; it consists of nonlinear elements such as switches which compensate odd harmonics. Harmonics are inconsistent objects that harm the power system in various effects, it results system failure, low power factor, motor torque pulsations, and overheating in the power system are the major problems. Researchers proposed many techniques to eliminate or suppress the content of the harmonics in the inverter. Dominant harmonic order in 5-phase is 3rd order, 5th order, and every 5th multiples harmonic order is absent in the 5-phase inverter. Challenge is reduction of harmonics generated by the nonlinear elements and to get a pure sine waveform at the output of the inverter. To obtain the pure sine waveform various filters are designed and implemented.

Wide range of applications in power systems will use filters to allow or block particular band of frequencies. Filter will have passive circuits, behaves as a blocking agent by affecting the harmonic content and it reduces THD. Many filter techniques are designed to filter out the harmonics; therefore, Series-passive filters have better harmonics suppressive quality at the tuned frequency [6–10].

2 Series-Passive Filter Design

Series-passive filter is placed between the load and inverter. Inductor and capacitor in parallel form creates high impedance at the tuned frequency. The presence of selective or tuned harmonic content are filtered out by the high impedance filters, hence Series-passive filter can be used to filter out a single harmonic order. To remove the leading 3rd harmonic order in 5-phase the resonant frequency is tuned to 150 Hz, since the operated frequency of the five phase inverter is 50 Hz, also for low input frequency 5 Hz the designed resonant frequency 15 Hz has been used. Inductor (L) and Capacitor (C) values are calculated using Eq. (1).

$$f_{\mathrm{r}} = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

3 5-Phase Inverter Drive

The 5-phase inverter constructed with 10 IGBT switches, gating signals are programmed by the pulse generators P_1, P_2, $P_3 \ldots P_{10}$, and circuit diagram of 5-phase inverter is shown in Fig. 1. Ten IGBT switches are turned ON using 180°

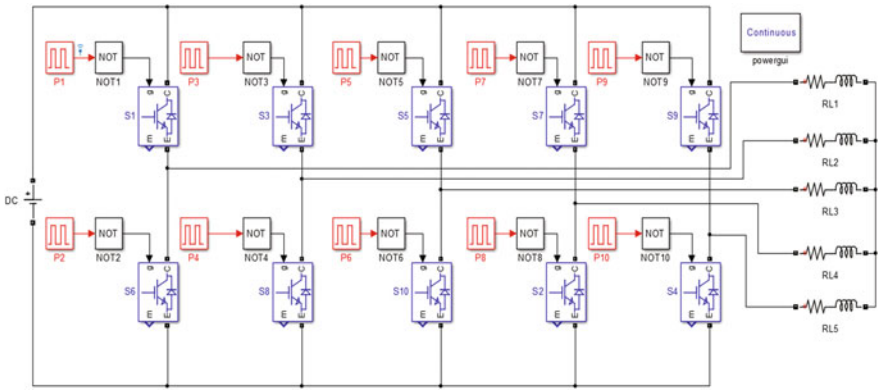


Fig. 1 5-Phase inverter circuit diagram

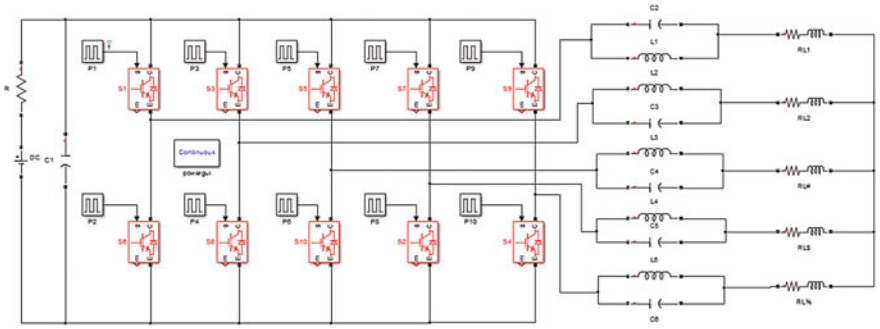


Fig. 2 Construction of 5-phase inverter with series-passive filter

conduction mode and having 72° out of phase difference. Output voltage of the inverter highly depends upon the switching of IGBT's. Two from upper group and three from the lower branch will be ON, or two from lower and three from upper branch will be ON.

4 5-Phase Inverter with Series-Passive Filter

Construction of 5-phase inverter with Series-passive filter as shown in Fig. 2. The Series-passive filter designed values are $C = 1000$ µF, $L = 1.1$ mH.

Therefore $L_1 = L_2 = L_3 = L_4 = L_5 = 1.1$ mH and $C_2 = C_3 = C_4 = C_5 = C_6 = 1000$ µF.

5 Simulation Results

Simulation has been done for the two input frequency of 50, 5 Hz and with RL load of $R = 1.7\ \Omega$ and $L = 1.3$ mH. Harmonics and Total Harmonic Distortion are studied by FFT analysis for both the input frequencies.

5.1 Simulation Results for 50 Hz Frequency

Inverter output voltage are measured and plotted for 5-phase inverter and Series-passive filter, respectively. THD is measured at normal inverter and with Series-passive filter. Figure 3 shows the voltage waveforms of 5-phase inverter. Figure 4 shows the voltage waveforms 5-phase inverter with Series-passive filter.

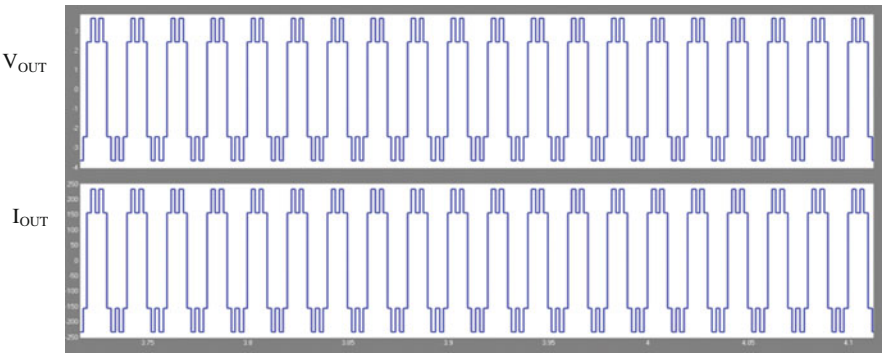


Fig. 3 Output voltage and current waveforms of an individual phase in normal 5-phase inverter for $f_{in} = 50$ Hz

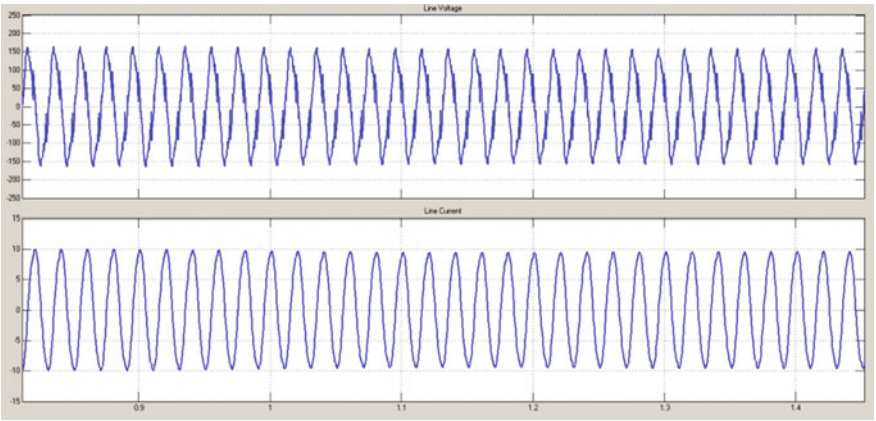


Fig. 4 Output voltage and current waveforms of an individual phase in 5-phase inverter with series-passive filter $f_{in} = 50$ Hz

Table 1 shows the THD in Normal 5-phase inverter and with filter, respectively. Figures 5 and 6 show the FFT analysis at output voltage with and without filter modes.

Table 1 THD comparison of 5-phase inverter normal and with series-passive filter for f_{in} = 50 Hz

Modes	THD in %
5-Phase inverter normal	42.7
5-Phase inverter with series-passive filter	20.07

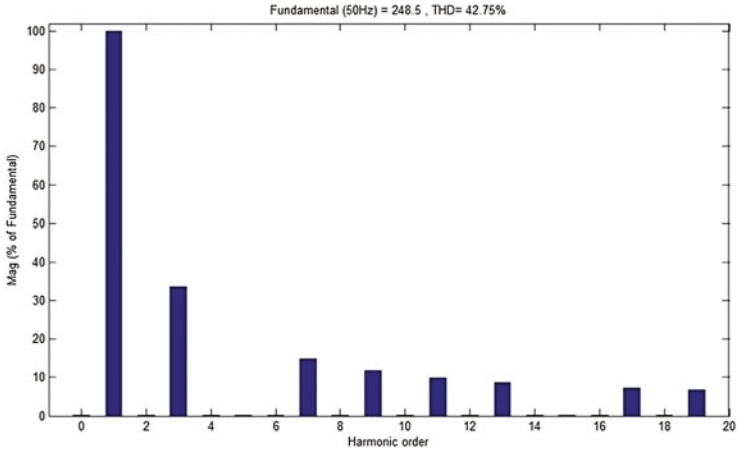


Fig. 5 FFT sequence of normal five phase inverter drive for f_{in} = 50 Hz

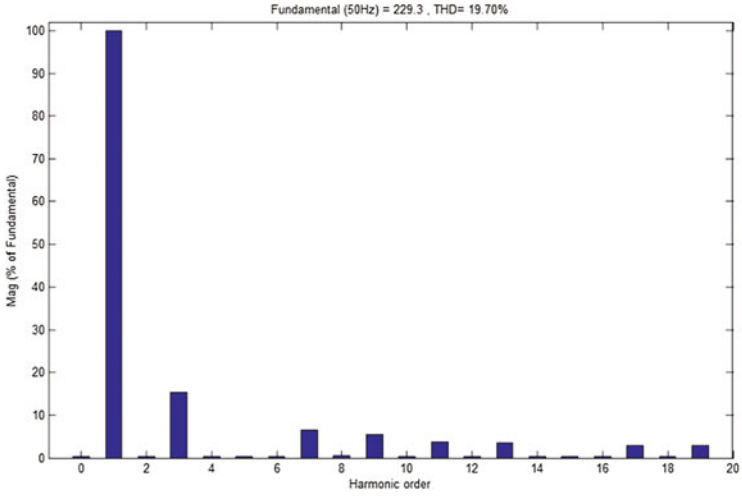


Fig. 6 FFT sequence of normal 5-phase inverter with series-passive filter f_{in} = 50 Hz

Table 2 Individual harmonic order voltage at the output voltage with and without series-passive filter for f_{in} = 50 Hz

Harmonic order	5-Phase inverter (V)	5-Phase inverter with series-passive filter (V)
1	248.28	228.79
2	0	0
3	82.76	36.01
4	0	0
5	0	0
6	0	0
7	35.47	15.08
8	0	0
9	27.59	11.70
10	0	0
11	22.57	9.56
12	0	0
13	19.1	8.10
14	0	0
15	0	0.01
16	0	0
17	14.6	6.23
18	0	0
19	13.06	5.56

Using Simulink/Matlab the individual harmonic order's voltages of a 5-phase inverter Normal and with Series-passive filter can be obtained using Simulink/Matlab and same as shown in Table 2.

5.2 *For a Input Frequency* f_{in} *= 5 Hz*

Input frequency is initialized for 5 Hz then FFT analysis computed for 5-phase inverter Normal and with Series-passive filter, respectively. Figures 7 and 8 shows the FFT analysis, respectively.

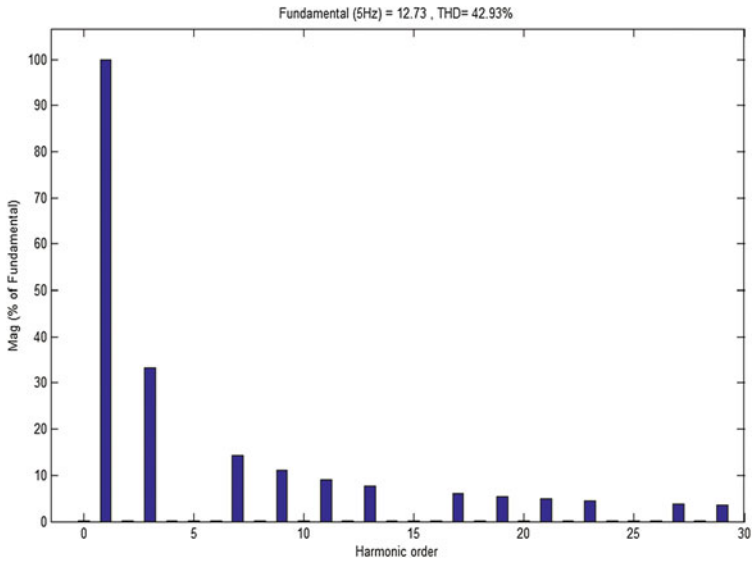


Fig. 7 FFT sequence of normal five phase inverter drive for f_{in} = 5 Hz

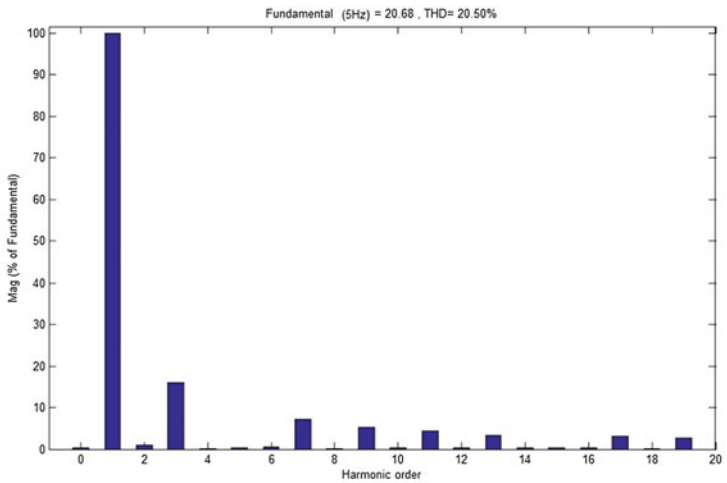


Fig. 8 FFT sequence of normal 5-phase inverter with series-passive filter f_{in} = 5 Hz

6 Conclusion

The effect and performance of Series-passive filter at the output of the inverter has been studied using Simulink/Matlab. The Series-passive filter is tuned to remove the particular harmonic order and coupled to the output of the inverter. Performance

of Series-passive filter has been studied by obtaining the harmonics and Total Harmonic Distortion; the results have been compared with five phase inverter drive and 5-phase inverter with Series-passive filter. Harmonics and the THD have been reduced by using Series-passive filter by tuned at the resonant frequency. In future this work will be incorporated to study the thermal behavior of the 5-phase Induction motor.

References

1. Levi, E., Bojoi, R., Profumo, F., Toliyat, H.A., Williamson, S.: Multiphase induction motor drives-A technology status review. IET Elect. Power Appl. **1**(4), 489–516 (2007)
2. Jones, M., Levi, E.: A literature survey of state-of-the-art in multiphase ac drives. In: Proceedings of 37th International Universities Power Engineering Conference UPEC, pp. 505–510 (2002)
3. Levi, E., Jones, M., Vukosavic, S.N., Toliyat, H.A.: A five-phase two-machine vector controlled induction moto drive supplied from a single inverter. EPE J. **14**(3), 38–48 (2004)
4. Kim, N., Kim, M.: Modified direct torque control system of five phase induction motor. J. Electr. Eng. Techol. **4**(2), 266–271 (2009)
5. Levi, E.: Multiphase electric machines for variable-speed applications. IEEE Trans. Ind. Electron. **55**(5), 1893–1909 (2008)
6. Ananda, A.S., Dr. Manjesh.: Analysis of harmonics in a five phase PWM inverter with LR load and mitigation of harmonics by π filter. In: IEEE 2016 Biennial International Conference on Power and Energy Systems: Towards Sustainable Energy (PESTSE) (2016)
7. Dr. Manjesh,. Ananda, A.S.: Analysis and study of total harmonic distortion in five phase PWM inverter using LC filter with neutral point DC link capacitor voltage balancing scheme. In: IEEE International Conference on Magentics, Machines and Drives (2014)
8. Tawfeeq, O.T.: THD reduction of a current source rectifier-dc motor drive using single tuned filters. Int. J. Inventive Eng. Sci. (IJIES) **1**(12) (2013). ISSN: 2319–9598
9. Memon, Z.A., Uquaili, M.A., Unar, M.A.: Harmonics mitigation of industrial power system using passive filters. Mehran Univ. Res. J. Eng. Technol. **31**(2) (2012)
10. Kanwar, S., Mahela, O.P., Mittal, D.: Power quality improvement in faulty conditions using tuned harmonic filters. IOSR J. Electr. Electron. Eng. (IOSR-JEEE), **6**(5) (2013). e-ISSN: 2278-1676, p-ISSN: 2320-3331

Finding the Initial Variables for Affine Arithmetic-Based Power Flow Analysis

Yoseph Mekonnen Abebe, P. Mallikarjuna Rao and M. Gopichand Naik

Abstract Power flow analysis has been playing a major role in providing information about the power system network. Due to the advancement of variable generation (VG) sources and weather variation, the punctual power flow analysis cannot give any information about the worst case scenario. The introduction of affine arithmetic (AA) is gaining high recognition due to its ability to consider all forms of uncertainty than interval arithmetic (IA). The first work in applying AA for power flow analysis is finding the initial affine forms in order to start the analysis. This paper focuses on finding the initial voltage and angle affine forms for polar coordinates and the initial real and reactive voltage forms for rectangular coordinate system.

Keywords Affine arithmetic · Initial affine forms · Interval arithmetic
Power flow analysis · Variable generation · Weather change

1 Introduction

Affine arithmetic (AA)-based power flow analysis is gaining attention due to the problem associated with interval arithmetic [1]. Unlike IA-based power flow analysis, AA-based power flow analysis needs initial affine forms of variables before the analysis is started [2–4]. In [2] AA-based power flow analysis is proposed and tested in an IEEE bus system and the result is found to be more better suited for worst case scenario due to its slight conservative nature than the Monte

Y.M. Abebe (✉) · P. Mallikarjuna Rao · M. Gopichand Naik
Department of Electrical Engineering, College of Engineering (A), Andhra University, Visakhapatnam 530000, AP, India
e-mail: yosephgod@gmail.com

P. Mallikarjuna Rao
e-mail: electricalprofessor@gmail.com

M. Gopichand Naik
e-mail: gopi_905@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_15

Carlo simulation result proving the necessity of AA. Though the paper highlights on how to solve AA-based power equations using constrained optimization mechanisms, finding the initial values to start the analysis for polar coordinate is given a little attention.

In [5] AA-based analysis is presented to deal with a generation uncertainty. Sensitivity analysis is carried out in order to find the noise symbols representing all sorts of uncertainty at ($\pm 1\%$) perturbation.

The application AA for a radial system with uncertainty is presented in [6]. The analysis is based on backward/forward algorithm. Directly, IA form of power is converted to AA using IA to AA conversion and the algorithm gives the desired output. The information about the noise symbol representing the sensitivity of bus value due to the injection of active and reactive power is not given. One of the main aims of using AA over IA is to get extra information about the share of each uncertainty.

Though some of the work which has been done on AA-based power flow analysis gives highlights on finding either polar or rectangular initial affine forms, the detail and combined works are still pending. Due to the advancement in the usage of AA over IA the mechanism of finding initial affine forms for both coordinates must be solved.

The aim of this paper is to generalize the way of finding the initial affine forms in order to conduct AA-based power flow analysis. This paper provides details of both polar and rectangular initial affine forms with specific examples. Since finding initial affine forms are the basic criteria to start AA-based power flow analysis, the step by step approach presented in this paper will help researchers in developing soft computing mechanism for a power flow network with uncertainty.

The remaining sections of this paper are organized as follows. Section 2 highlights the mathematics of affine arithmetic; Sect. 3 gives details about the polar and rectangular form-based initial affine forms; Sect. 4 is dedicated for result and discussion and finally Sect. 5 provides the conclusion of the overall work.

2 Affine Arithmetic

Basically AA is an extension of IA in order to solve problems associated with the latter [7]. The inventor of AA, Comba, and Stolfi, pointed out that AA can tackle the dependency problem which is turning out to be the worst drawbacks of IA in 1990 [8]. The basic AA mathematics for real number is based on (1) and (2). The two terms represent two variables with the same sensitivity parameters or symbolic variable.

$$\hat{l} = l_0 + \sum_{i=1}^{n} l_i \varepsilon_i \tag{1}$$

$$\hat{m} = m_0 + \sum_{i=1}^{n} m_i \varepsilon_i \tag{2}$$

where

$\hat{l}$, $\hat{m}$ Represents the affine functions,
l_0, m_0 Represents the central values,
l_i, m_i Represents the partial deviations,
ε_i Represents the symbolic variables; its value lies between [−1, 1]

There are two operations in AA: Affine and non-affine operations. Affine operations can be manipulated using ordinary algebra. Non-affine operation needs an extra approximation mechanism in order to be analyzed [8]. The basic affine operations are addition, subtraction, scaling, etc. Notable multi variable-based non-affine operations are multiplication and division. Other functions like logarithmic, exponential, trigonometric, etc. also fall under non-affine operations. Equation (3)–(5) represents affine operations and (6) represents multiplication. The general non-affine approximation for any single variable $\hat{m}$ is given by Chebyshev formula as in (7). In all the equations below α is a real constant.

$$\hat{l} \pm \hat{m} = (l_0 \pm m_0) + \sum_{i=1}^{n} (l_i \pm m_i)\varepsilon_i \tag{3}$$

$$a \pm \hat{m} = (\alpha \pm m_0) + \sum_{i=1}^{n} m_i \varepsilon_i \tag{4}$$

$$a\hat{m} = am_0 + \sum_{i=1}^{n} am_i \varepsilon_i \tag{5}$$

$$\hat{l}\hat{m} = (l_0 m_0) + \sum_{n=1}^{n} (l_0 m_i + l_i m_0)\, \varepsilon_i + \left(\sum_{i=1}^{n} |l_i| \sum_{i=1}^{n} |m_i| \right) \varepsilon_{n+1} \tag{6}$$

The basic difference between affine and non-affine operation is the introduction of unique symbolic variable by non-affine operation at the end of the result. As seen from (6) the new symbolic variable ε_{n+1} is introduced due to approximation error.

$$\hat{z} = \alpha\hat{m} + \xi + \delta\varepsilon_n \tag{7}$$

The details of finding the coefficient of (7) and the mathematical basics of Chebyshev approximation is not the aim of this paper, hence one can easily explore Chebyshev approximation from [7–10].

The conversion of affine to interval and vice versa is a common scenario during AA analysis. For any affine function in (1) and interval $L = [c, d]$, the conversion is given by (8) and (9), respectively.

$$L = l_0 + \sum_{1}^{n} l_i[-1,\ 1\,] \tag{8}$$

$$\hat{l} = \frac{d+c}{2} + \frac{d-c}{2}\varepsilon_k \tag{9}$$

3 Initial Affine Forms

For a punctual or ordinary power flow analysis without uncertainty the initial voltages have a value of '1 p.u' for PQ buses and all buses except the slack bus has an angle value of '0 p.u'. Due to the presence of uncertainties in both the generated power and load, punctual power flow analysis is replaced by uncertainty-based power flow analysis and the initial values are no more flat 1 and 0 rather becomes arrays of partial deviations [2, 4].

3.1 Polar Form

The polar form of Newton–Raphson power equation for both, the real and imaginary power, is given by (10). The first step in formulating initial affine forms is finding the central values. The central values ($V_{0,i}$ and $\delta_{0,i}$) are calculated from ordinary load flow analysis at the center of the interval valued power or at the punctual values of both reactive and active power [1, 2, 4].

$$\left.\begin{aligned} P_i &= \sum_{1}^{n} V_i V_j Y_{ij} \cos(\theta_i - \theta_j - \alpha_{ij}) \\ Q_i &= \sum_{1}^{n} V_i V_j Y_{ij} \sin(\theta_i - \theta_j - \alpha_{ij}) \end{aligned}\right\} \tag{10}$$

The initial affine form of bus voltage and angle for polar coordinate-based Newton–Raphson power flow analysis, including the central value, for 'n' number of total buses, but slack and with 'm' number of load buses, is given by (11) and (12), respectively.

$$\hat{V}_i = V_{i,0} + \sum_{j=1}^{n-1} V_{i,j}^{P} \varepsilon_j^{P} + \sum_{k=1}^{m} V_{i,k}^{Q} \varepsilon_k^{Q} \quad \text{for} \quad i \in nQ \tag{11}$$

$$\hat{\delta}_i = \delta_{i,0} + \sum_{j=1}^{n-1} \delta_{i,j}^{P} \varepsilon_j^{P} + \sum_{k=1}^{m} \delta_{i,k}^{Q} \varepsilon_k^{Q} \quad \text{for} \quad i \in nP \tag{12}$$

where

$V_{i,0}$, $\delta_{i,0}$ The central values of $\hat{V}_i$ and $\hat{\delta}_i$ calculated from load flow analysis at the center of the uncertain power;

$V_{i,j}^{P}$, $\delta_{i,j}^{P}$ Partial deviations of $\hat{V}_i$ and $\hat{\delta}_i$ due to the injection of active power at bus j, respectively;

$V_{i,k}^{Q}$, $\delta_{i,k}^{Q}$ Partial deviations of $\hat{V}_i$ and $\hat{\delta}_i$ due to the injection of reactive power at bus j, respectively;

ε_j^P, ε_k^Q Symbolic variables, bounded by [−1, 1] representing the injection of active and reactive power, respectively.

As mentioned earlier, the central values are calculated from basic load flow analysis at the center of the varying power. The next question is how to find the partial deviations. In fact, finding these values is the main aim of this paper. The partial deviation value indicates the sensitivity of each bus toward the ejection of real and imaginary power to the system [2, 4]. Equation (13)–(14) shows the partial deviation formula for both bus voltage and bus voltage angle because of the injection of active and reactive power, respectively.

$$\left.\begin{aligned} V_{i,j}^{P} &= \left.\frac{\partial V_i}{\partial P_j}\right|_0 \Delta P_j \\ V_{i,k}^{Q} &= \left.\frac{\partial V_i}{\partial Q_k}\right|_0 \Delta Q_k \end{aligned}\right\} \quad \text{for} \quad j \in nP, \quad k, i \in nQ \tag{13}$$

$$\left.\begin{aligned} \delta_{i,j}^{P} &= \left.\frac{\partial \delta_i}{\partial P_j}\right|_0 \Delta P_j \\ \delta_{i,k}^{Q} &= \left.\frac{\partial \delta_i}{\partial Q_k}\right|_0 \Delta Q_k \end{aligned}\right\} \quad \text{for} \quad i, j \in nP, \quad k \in nQ \tag{14}$$

The reactive and active power change at the respective bus is the radius of the specified maximum and minimum power and given by (15).

$$\left.\begin{aligned} \Delta P_j &= \frac{P_j^{\max} - P_j^{\min}}{2} \\ \Delta Q_k &= \frac{Q_k^{\max} - Q_k^{\min}}{2} \end{aligned}\right\} \tag{15}$$

Equation (11) and (12) are found by adding the central bus voltage and angle ($V_{i,0}$ and $\delta_{i,0}$), calculated at the center of the uncertain power using punctual power flow analysis, and the partial deviation of (13)–(14) into, respectively. As a result (11) and (12) are the initial affine forms of voltage and angle for AA-based Newton–Raphson power flow analysis in polar form.

3.2 Rectangular Form

The rectangular form of Newton–Raphson power equation for both powers is given by (16). The initial affine form of real and reactive voltage for rectangular coordinate-based Newton–Raphson power flow analysis, including the central value is given by (17) and (18), respectively [11].

$$\left.\begin{aligned} P_i &= e_i \sum_{j=1}^{n-1} (G_{ij}e_j - B_{ij}f_j) + f_i \sum_{j=1}^{n-1} G_{ij}f_j + B_{ij}e_j) \\ Q_i &= f_i \sum_{j=1}^{n-1} (G_{ij}e_j - B_{ij}f_j) - e_i \sum_{j=1}^{n-1} G_{ij}f_j + B_{ij}e_j) \end{aligned}\right\} \tag{16}$$

Like polar coordinate, the central values ($e_{0,i}$ and $f_{0,i}$) are calculated from ordinary load flow analysis at the center of the varying power.

$$\hat{e}_i = e_{i,0} + \sum_{j=1}^{n-1} e_{i,j}^P \varepsilon_j^P + \sum_{k=1}^{m} e_{i,k}^Q \varepsilon_k^Q \quad \text{for} \quad i \in nP \tag{17}$$

$$\hat{f}_i = f_{i,0} + \sum_{j=1}^{n-1} f_{i,j}^P \varepsilon_j^P + \sum_{k=1}^{m} f_{i,k}^Q \varepsilon_k^Q \quad \text{for} \quad i \in nQ \tag{18}$$

where

$e_{i,0}$, $f_{i,0}$ The central values of the $\hat{e}_i$ and $\hat{f}_i$ calculated from load flow analysis at the center of the varying power;

$e_{i,j}^P$, $f_{i,j}^P$ Partial deviations of $\hat{e}_i$ and $\hat{f}_i$ because of the injection of real power at bus j, respectively;

$V_{i,k}^Q$, $\delta_{i,k}^Q$ Partial deviations of $\hat{e}_i$ and $\hat{f}_i$ due to the injection of imaginary power at bus j, respectively;

ε_j^P, ε_k^Q Symbolic variables, bounded by [−1, 1] representing the injection of real and imaginary power, respectively.

The partial deviation values indicate the sensitivity of all buses toward the ejection of real and imaginary power to the system [12]. Equation (19)–(20) shows the partial deviation formula for both real and reactive voltage due to the injection of active and reactive power, respectively.

$$\left.\begin{aligned} e_{i,j}^P &= \frac{\partial e_i}{\partial P_j}\Big|_0 \Delta P_j \\ e_{i,k}^Q &= \frac{\partial e_i}{\partial Q_k}\Big|_0 \Delta Q_k \end{aligned}\right\} \quad \text{for} \quad i,j \in nP, \quad k \in nQ \tag{19}$$

$$\left.\begin{aligned} f_{i,j}^{P} &= \frac{\partial f_i}{\partial P_j}\Big|_0 \Delta P_j \\ f_{i,k}^{Q} &= \frac{\partial f_i}{\partial Q_k}\Big|_0 \Delta Q_k \end{aligned}\right\} \quad \text{for} \quad j \in nP, \quad k, i \in nQ \tag{20}$$

The real and imaginary power change at the respective bus is the radius of the specified maximum and minimum power as given by (15). Plugging the central bus active and reactive voltage ($e_{i,0}$ and $f_{i,0}$), calculated at the center of the uncertain power using punctual power flow analysis, and the partial deviation of (19)–(20) into (17) and (18), respectively, gives the initial affine form real and imaginary voltage for AA-based Newton–Raphson load flow analysis in rectangular form.

4 Test Case Study

In order to implement the two proposed methods an IEEE bus systems are used. Since the number of noise variable increases with the number of buses, it is difficult to display the result of higher bus systems. The test is performed on IEEE-6, 14, 30 and 57 bus systems. For the sake of explanation the result of IEEE-6 bus system for ten percent of the loads and generation uncertainty is presented for both cases. The number of noise variable at each bus voltage or angle is equal to the number of ($nP + nQ$) buses. Similarly the number of variables is also equal to the number of ($nP + nQ$) buses. For a six bus system with two generators at bus (2 and 3) and three loads at bus (4, 5, 6), the total number of variables and noise variable at each bus is eight.

Table 1 shows the initial partial deviation values for polar coordinate and Table 2 shows the initial partial deviation values for rectangular coordinates. The central values for all the bus system can be calculated from ordinary load flow analysis at the center of the varying powers.

Tables 1 and 2 results are the initial affine partial deviation values for polar and rectangular coordinates, respectively. Including the central value the initial affine form of bus 4 for both cases can be written as follows depending on the above two tables.

$$\begin{aligned} \hat{v}_4 &= 1.005 - 0.0005\varepsilon_{4,1}^{p} - 0.0005\varepsilon_{4,2}^{p} + 0.0022\varepsilon_{4,3}^{p} - 0.0001\varepsilon_{4,4}^{p} - 0.0004\varepsilon_{4,5}^{p} \\ &\quad + 0.0062\varepsilon_{4,1}^{q} + 0.001\varepsilon_{4,2}^{q} + 0.0002\varepsilon_{4,3}^{q} \\ \hat{f}_4 &= 0.005 + 0.0011\varepsilon_{4,1}^{p} + 0.0015\varepsilon_{4,2}^{p} + 0.0063\varepsilon_{4,3}^{p} - 0.0016\varepsilon_{4,4}^{p} + 0.0011\varepsilon_{4,5}^{p} \\ &\quad - 0.0023\varepsilon_{4,1}^{q} - 0.023\varepsilon_{4,2}^{q} - 0.0003\varepsilon_{4,3}^{q} \end{aligned}$$

The two equation represents bus voltage magnitude and complex bus voltage for bus number 4, respectively.

As discussed earlier, the central values of the above table results of all the buses are found from nominal power flow analysis without uncertainty or at the center of the uncertain powers. In the same manner the other initial affine forms are arranged and made ready for affine-based power flow analysis. During AA-based power flow

Table 1 Partial deviation values for polar coordinate

Variables (δ_j, V_j)	Initial partial deviation values							
	$\varepsilon_{j,1}^{p}$	$\varepsilon_{j,2}^{p}$	$\varepsilon_{j,3}^{p}$	$\varepsilon_{j,4}^{p}$	$\varepsilon_{j,5}^{p}$	$\varepsilon_{j,1}^{q}$	$\varepsilon_{j,2}^{q}$	$\varepsilon_{j,3}^{q}$
δ_2	0.0101	0.0087	0.0067	0.0069	0.0088	0.0008	0.0005	0.0003
δ_3	0.0087	0.0172	0.0063	0.0096	0.0137	0.0008	0.0007	0.0002
δ_4	0.0066	0.0062	0.0100	0.0056	0.0062	−0.0019	0.0001	0.0002
δ_5	0.0068	0.0095	0.0056	0.0123	0.0093	0.0003	−0.0019	−0.0002
δ_6	0.0087	0.0136	0.0063	0.0094	0.0169	0.0007	0.0003	−0.0012
V_4	−0.0005	−0.0005	0.0022	−0.0001	−0.0004	0.0062	0.0010	0.0002
V_5	−0.0002	−0.0003	0.0002	0.0023	0.0001	0.0010	0.0070	0.0014
V_6	−0.0001	0.0002	0.0000	0.0005	0.0017	0.0002	0.0014	0.0061

Table 2 Partial deviation values for rectangular coordinate

Variables (e_j, f_j)	Initial partial deviation values							
	$\varepsilon^p_{j,1}$	$\varepsilon^p_{j,2}$	$\varepsilon^p_{j,3}$	$\varepsilon^p_{j,4}$	$\varepsilon^p_{j,5}$	$\varepsilon^q_{j,1}$	$\varepsilon^q_{j,2}$	$\varepsilon^q_{j,3}$
e_2	0.0261	0.0218	0.0173	0.0177	0.0224	0.0020	0.0013	0.0009
e_3	0.0217	0.0518	0.0161	0.0272	0.0398	0.0020	0.0019	0.0003
e_4	0.0183	0.0172	0.0148	0.0134	0.0170	0.0077	0.0020	0.0008
e_5	0.0191	0.0293	0.0136	0.0204	0.0252	0.0026	0.0083	0.0018
e_6	0.0238	0.0423	0.0170	0.0249	0.0361	0.0022	0.0031	0.0066
f_4	0.0011	0.0010	0.0063	0.0016	0.0011	−0.0023	−0.0002	−0.0000
f_5	0.0004	0.0005	0.0011	0.0066	0.0015	−0.0002	−0.0023	−0.0003
f_6	0.0000	−0.0009	0.0001	0.0008	0.0048	−0.0000	−0.0003	−0.0014

analysis the central and partial values of the bus voltage and angles are treated as a vector quantity in order to implement the algorithm in Matlab. The two proposed methods effectively represent all uncertainties considered to analyze the power system network. The partial deviation magnitude increases with the increase of percent of uncertainty.

5 Conclusion

In order to manipulate AA-based power flow analysis for uncertain system, finding the sensitivity of bus variables toward the change of power is mandatory. This paper provides step by step and detail calculation of finding the initial affine form central and partial deviation values for both rectangular and polar coordinate systems.

Since AA result is highly dependent on the number of non-affine operations, it is advisable to use rectangular coordinate systems in order to decrease the number of non-affine operation in finding bus voltage and angle. On the other hand, if the aim of the researcher is to find a conservative bound of voltage and angle, using polar coordinate is advantageous. The paper provides both case initial variables for the researcher to have flexibility in choosing any one of the methods to find desired power flow results for uncertain system using AA.

References

1. Abebe, Y.M., Pasumarthi, M.R., Mudavath, G.N.: Load flow analysis of uncertain power system through affine arithmetic. In: Lecture Notes in Electrical Engineering Microelectronics, Electromagnetics and Telecommunications, vol. 372, pp. 217–231 (2015)
2. Vaccaro, A., Cańizares, C.A., Villacci, D.: An Affine arithmetic-based methodology for reliable power flow analysis in the presence of data uncertainty. IEEE Trans. Power Syst. **25** (2), 624–632 (2010)

3. Muńoz, J., Cańizares, C., Bhattacharya, K., Vaccaro, A.: An affine arithmetic based method for voltage stability assessment of power systems with intermittent generation sources. IEEE Trans. Power Syst. **28**(4), 4475–4487 (2013)
4. Dimitrovski, A., Tomsovic, K., Vaccaro, A.: Reliable algorithms for power flow analysis in the presence of data uncertainties. In Proceedings, Innovations in Power Systems Reliability, pp. 329–357. Springer, London (2011)
5. Pirnia, M., Canizares, C.A., Bhattacharya, K., Vaccaro, A.: A novel affine arithmetic method to solve optimal power flow problems with uncertainties. IEEE Trans. Power Syst. **29**(6), 2775–2783 (2014)
6. Gu, W., Luo, L., Ding, T., Meng, X., Sheng, W.: An affine arithmetic-based algorithm for radial distribution system power flow with uncertainties. Int. J. Electr. Power Energy Syst. **58**, 242–245 (2014)
7. Stolfi, J., De Figueiredo, L.H.: An Introduction to affine arithmetic. Trends Appl. Comput. Math. **4**(3), 297–312 (2003)
8. De Figueiredo, L.H., Stolfi, J.: Affine arithmetic: concepts and applications, vol. 37, pp. 147–158. Kluwer Academic Publisher, Netherlands (2004)
9. Fermia, N., Spagnuolo, G.: True worst-case circuit tolerance analysis using genetic algorithms and affine arithmetic. IEEE Trans. Circ. Syst. Fundam. Theory Appl. **47**(9), 1285–1296 (2000)
10. Abebe, Y.M., Rao, P.M.: Overhead transmission line sag, tension and length calculation using affine arithmetic. In: IEEE Power, Communication and Information Technology Conference (PCITC), pp. 211–216 (2015)
11. Zhang, C., Chen, H., Ngan, H., Yang, P., Hua, D.: A mixed interval power flow analysis under rectangular and polar coordinate system. IEEE Trans. Power Syst. 1–1 (2016)
12. Aghatehrani, R., Kavasseri, R.: Reactive power management of a DFIG wind system in microgrids based on voltage sensitivity analysis. Trans. Sustainable Energy **2**, 451–458 (2011)

Ecology and Energy Dimension in Infrastructural Designs

A. Rajaraman

Abstract With urbanization becoming the core of societal migration, infrastructural needs like transportation, power, water and communication are on the rise. Infrastructural development in recent years call for consideration of new and complex aspects relating to impacts on environment, energy and life cycle performance in any new construction and it is preferable that these are addressed at the planning and design stage itself so that negative effects could be minimized. The present study focuses attention on ecology and energy dimensions at the planning stage so that the resulting system is eco-friendly and at the same time sustainable. Consideration of embodied energy and CO_2 emission in the design and planning stages of two systems are demonstrated for Indian conditions with quantification of the impact on environment. The case studies reveal that new dimensions like energy and emission are to be added to existing cost and weight considerations—normally used in designs—so that one can get a design which is competitive, energy-intensive and eco-friendly to make it sustainable.

Keywords Energy · Environment · Infrastructural systems · Design · Emission

1 Introduction

Cellular communication and Internet are changing many aspects of present day life and more and more research and exploration aspects in different areas like science, engineering, space and even societal outlooks are sprouting every day to reach globally all users. Proliferation of apps, smart electronic gadgets and telemedicine are some of the many innovations which have become common and easily usable. The impact of these on developing and developed countries is phenomenal in opening out a common platform for all users and rendering geographical locations insignificant. Simultaneously other issues like too much urbanization, ozone layer

A. Rajaraman (✉)
Hindustan University, Chennai 603103, India
e-mail: arraman41@yahoo.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_16

depletion and environmental hazards are also on the rise. Here infrastructural systems which form a critical component of any country for its technological advancement play an important role. Environmental aspects of present infrastructural systems are mainly the energy consumption and atmospheric pollution through CO_2 emission and in this study how additional dimensions at planning and design level besides the normally popular cost and weight considerations, can open new designs to cater not only for cost and weight but also environment improvement.

2 Infrastructural Systems

Infrastructural systems which occupy a significant portion in a country's budget—in India it is around 25–30%—normally cater to housing, transportation, power, communication and space technology. Considering housing and transportation, residential systems and bridges occupy a dominant portion and in India most of these are built with concrete/cement and steel besides sand, aggregate and water. Here the production of concrete and steel need energy inputs and both have CO_2 emissions affecting atmosphere. Residential systems either in private or government sector are mostly with reinforced concrete as it is easy to make and form whereas in bridges both steel—normal and high strength like in Hubli bridge—and concrete are used in equal measure. Considering the planning and design stage of these systems, till now only cost and weight consideration dominated and designs are arrived either based on cost or on weight for making it less heavy in construction and on foundations.

3 Energy Dimension

Recent study as given in Fig. 1 shows how the economy in the last two centuries has brought in a sharp increase in demand for natural gas and this resulted in an energy gap which may be a cause of worry in the coming days. Similarly, CO_2

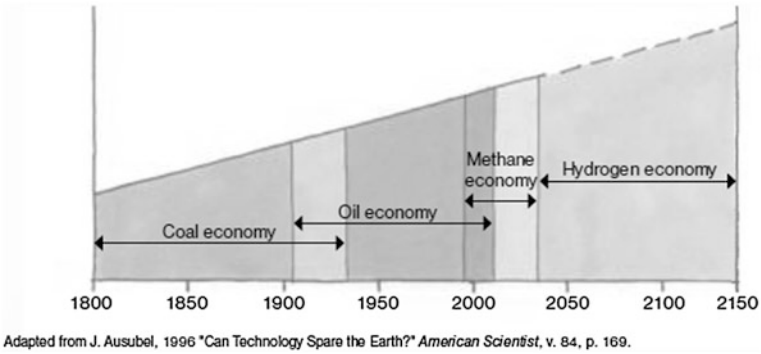


Fig. 1 Economy shift

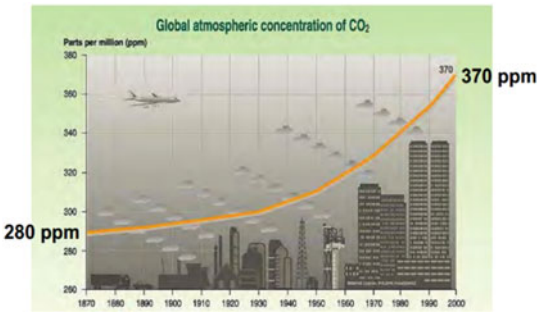


Fig. 2 Growth in CO_2 emission (www.autosteel.org)

emission as given in autosteel web site shows a significant increase in the last decade as in Fig. 2.

Obviously, this has prompted many American and European countries to go into green and sustainable construction on 'war footing'. So one needs to have a shift in construction and planning by adding a new dimension 'Green and sustainability' and this is shown in Fig. 3. In addition to normal entities like cost, materials/weight, one can include energy for production and consequent CO_2 emission. Energy calculations include energy in production, transportation and erection—some time maintenance also—and this depends on materials, process and erection at site. There are different aspects to this and many books and references give an idea from energy management point of view [1].

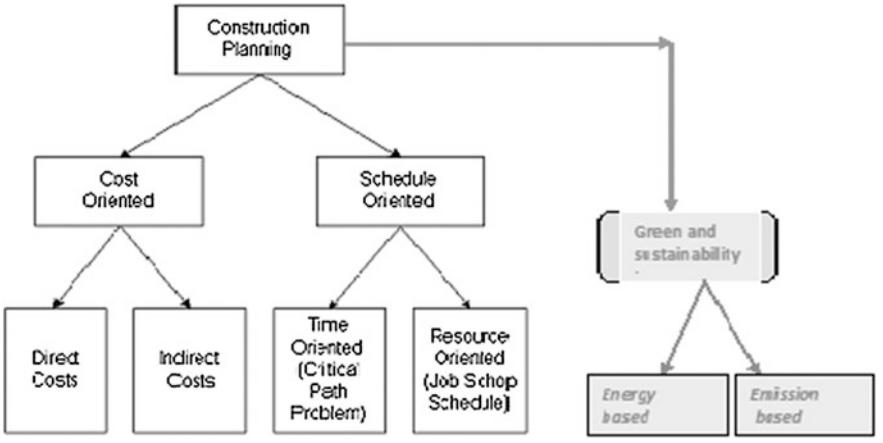


Fig. 3 Energy dimension in planning

4 Case Studies

4.1 Building Systems

The first case study is on reinforced concrete beams used in housing and for demonstration the span is chosen as 10 m and depth of the beam varied from 240 to 960 mm with data on strength of concrete from 20, 40 and 60 Mpa and two types of steel with 250 and 415 Mpa as yield stress. Energy data is taken from [2] and with values of 14 and 22 MJ per kg for the two steels and for concrete the values chosen are 0.95 nJ, 0.96 MJ and 1.06 MJ per kg of concrete. CO_2 emission values are [0.85 and 0.825] for steel and [0.12, 0.13, 0.16] for concrete. Figure 4 shows the steel weights for five design values, three concrete strengths with left one for 250 strength steel and right for 415 steel.

Steel weights get reduced as strength increases for the five sets of variations in designs and one can definitely arrive at an economical design from cost and weight points of view [3].

But the effects on energy and CO_2 emission need to be seen and this is shown in Fig. 5, where cost, weight, energy and emission variations are presented. One can see clearly minimum cost does not guarantee minimum energy or emission and one needs to do trade-off to arrive at eco-friendly design.

4.2 Transportation Systems

Considering bridge systems used profusely in modern-day transportation as fly-overs to tackle traffic in major cities, two systems are possible as shown in Fig. 6 with one being normal uniform girders and another tapered cantilever beams. The designs were done and effects on energy and CO_2 emission were carried for different designs with two different strengths and materials using fly ash as well.

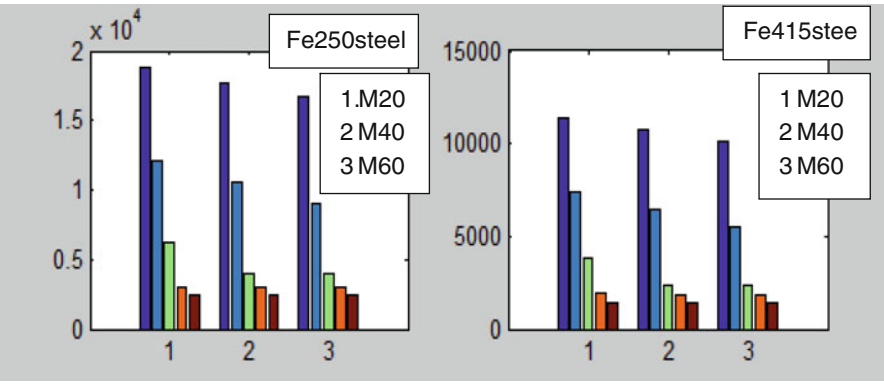
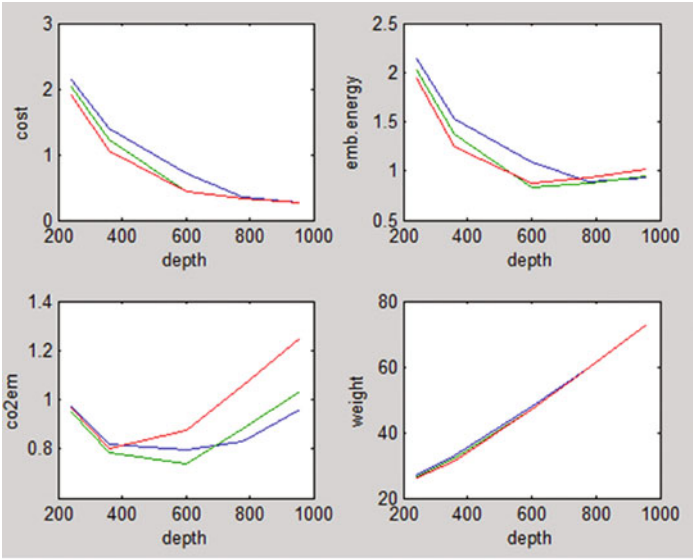
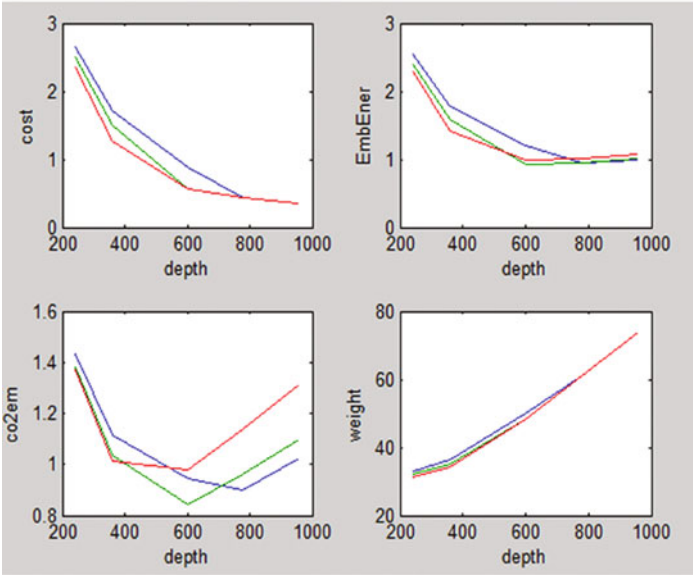


Fig. 4 Steel weights for different designs



(a) Variations for Fe250



(b) Variations for Fe415

Fig. 5 Cost and environmental effects on design

Detailed results have been presented in [4] and salient results are shown in Fig. 7, where it is seen that the effects of adding fly ash considerably brings down the environmental effects to as low as 24%.

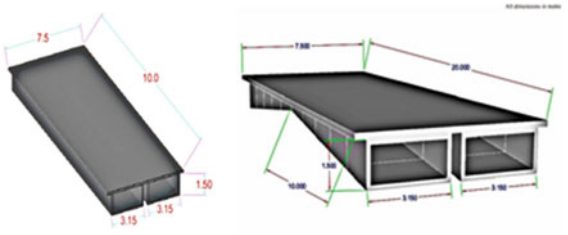


Fig. 6 Two configurations studied

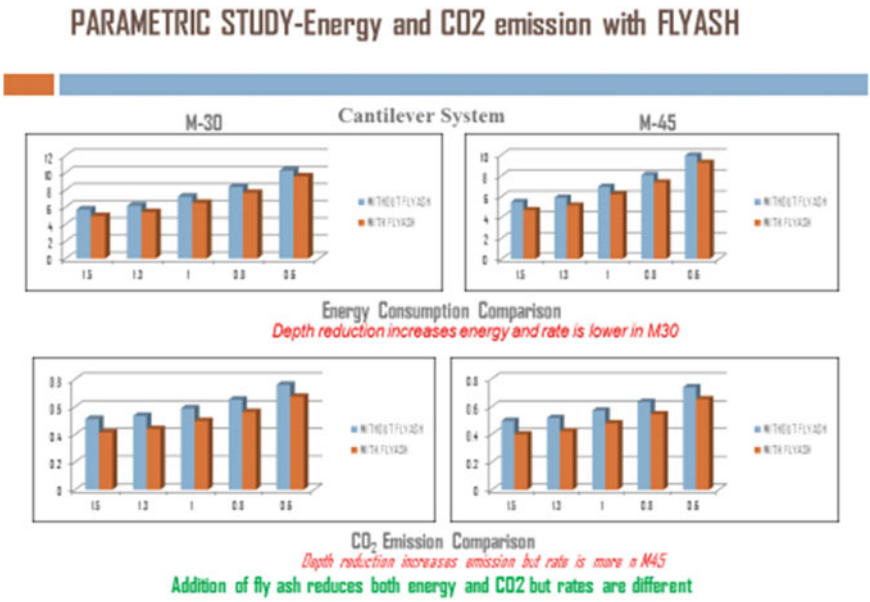


Fig. 7 Ecology results for different cases

5 Conclusions

Consideration of environmental effects at planning and design stage can be taken care of by adding another dimension to cover energy and emission issues so that a sustainable and eco-friendly design could be arrived at. Two case studies are presented to give an idea as to how the weight- and cost-based designs need not be eco-effective and adding waste materials like fly ash can considerably bring down the environmental damage and the energy inputs.

References

1. Mulavdic, E.: Multi-criteria optimization of construction technology of residential building upon the principles of sustainable development. Therm. Sci. **9**(3), 39–52 (2005)
2. Kilbert, C.J.: Sustainable Construction: Green Building Design and Delivery. Wiley, Hoboken (2007)
3. Prabhu, K.S., Rooby, J., Rajaraman, A.: Green and sustainable construction. In: Construction Management Conference, Hyderabad, India (2014)
4. Bhanu, T., Singh, N.: Energy based design for transportation systems. In: Dubai Conference on Engineering Applications (2013)

Energy-Aware Data Aggregation Techniques in Wireless Sensor Network

M. Ambigavathi and D. Sridharan

Abstract A Wireless Sensor Network (WSN) is an exigent technology and it has huge number of applications in disaster management, health monitoring, military, security, and so on. This network faces some critical barriers like fault tolerance, energy consumption due to heterogeneous traffic loads and redundant data transmission. In which, nodes are miniscule and have restricted capability of processing with reduced power of battery. This limitation of reduced power of battery makes the sensor network prone to failure. Data aggregation is a vital technique for active data processing in WSN. With the support of data aggregation, the energy depletion is minimized by eliminating redundant data or by decreasing the number of sent packets. This study reviews various data aggregation techniques such as clustered aggregation, tree-based aggregation, in-network aggregation, and centralized data aggregation with focus on energy consumption of sensor nodes.

Keywords Wireless sensor networks · Data aggregation techniques
Energy efficiency

1 Introduction

Wireless Sensor Network involves huge quantity of nodes, entailing a multi-hop network in which nodes for vicinity interact with each other with responsibilities of routing [1]. WSN is simple to implement in the needed circumstances and information are collected, processed, and transmitted to a desired place. Figure 1 illustrates the overall architecture diagram of WSN. Aggregation of data is the

M. Ambigavathi (✉) · D. Sridharan
Department of ECE, CEG Campus, Anna University, Chennai, India
e-mail: ambigaindhu8@gmail.com

D. Sridharan
e-mail: sridhar@annauniv.edu

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_17

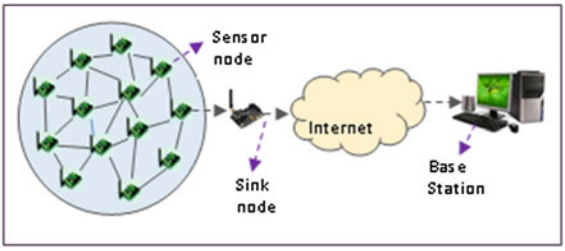


Fig. 1 The overall architecture diagram of WSN

process to collect and aggregate the meaningful data. In WSN, aggregation of data is an efficient way for saving the restricted resources. The major intention of algorithms of data aggregation is to collect the aggregated information in an energy-effective way, thus lifetime of the network is improved. WSNs have restricted battery, memory power, and restricted computational power, this results in maximized complexity for developers of the applications and frequently outcomes in applications which are strictly united with network protocols [2]. There are only less number of studies that focus toward energy-efficient data aggregation techniques related to WSN. This particular research reviews the energy-efficient techniques of data aggregation with specific references to WSN. The rest of this paper is designed as follows: Sect. 2 provides the various challenges of existing data aggregation techniques in WSN. Section 3 discusses about the findings using specific tabulation. Finally, the paper is concluded with recommendations in Sect. 4

2 Energy-Aware Data Aggregation Techniques

This section summarizes the detailed challenges of data aggregation schemes with main focus on energy efficiency. Based on the network structure, the data aggregation methods are categorized into four types.

2.1 Cluster-Based Data Aggregation

Cluster-based approach is considered as the hierarchical approach in which the whole networks are divided into several clusters. A delay-aware network structure for wireless sensor networks with in-network data fusion has been explained in [3]. Authors have pointed out that the clustering aggregation technique has been considered as the effective technique in reducing consumption of energy. In fact, the clustering has introduced bottlenecks to the network and it also causes extra delays in the process of data aggregation. Authors have proposed the structure which has

organized the sensor nodes into the different size clusters and it also has communicated with the center of the fusion in an interleaved manner. The process of optimization also has proposed to enhance the distance of intracluster communication. In the typical algorithm of cluster [4], the number of nodes in the network has been selected as the Cluster Heads (CHs). In addition to these, the clustering has introduced the consumption of extra energy and delay in the process of data collection. Moreover, the small cluster has shortened the process of data aggregation. Setup and steady state are the two phases involved under the operation of cluster-based data aggregation [5].

The algorithm of clustering has played an important role in reorganizing the data structure effectively. Clustering header has performed the data aggregation and it also has removed the redundancy effectively by using other CH intermediate nodes [6]. Finally, the cluster tendency, cluster and group leader finding and the secure aggregation are some of the effective process involved under the clustering and data aggregation techniques. In [7], authors studied about the energy-efficient data aggregation techniques in WSN. The data aggregation protocols have used the deterministic cluster methods to save the node's energy for resource dominant sensor network. The major attributes of data aggregation protocols are latency, energy, cluster head selection, node scheduling, cluster size, and data rate. Authors in [8] investigated the data aggregation techniques for energy efficiency in WSNs. Low-Energy Adaptive Cluster Hierarchy (LEACH) and Hybrid Energy-Efficient Distributed (HEED) are some of the best-known protocols which has played an important role in the cluster-based data aggregation. This approach also has consisted of hierarchical nodes of an organization in which each node has divided into clusters with special nodes to treat as the head of cluster. Data Density Correlation Degree clustering method (DDCD) has been proposed in this study [9] which has resulted in lower data distortion than those achieved using the method of Pearson Correlation Coefficient-based Clustering and Alpha Spatial Clustering. Semantic clustering methods are suitable for detecting the event and it is highly correlated with the domain rules of monitored event. Core sensor node and data density correlation degree are some of the description of clustering method which have played a vital role in the energy efficiency system in the WSN.

2.2 Tree-Based Data Aggregation Technique

Tree-based data aggregation approach has been presented using fitting functions [10]. Local aggregation and prefix filtering are the two methods used in this paper in order to attain the reduction of redundant data transfer in WSN. Energy has been saved by acquiring these methods due to the less data transmission. This tree approach has defined the aggregation by constructing an aggregation tree. Constructing Load-Balanced Data Aggregation Trees (LBDAT) has been implemented in [11]. Data gathering trees have the tendency to perform the aggregation

operations in which it is also called as Data Aggregation Trees (DATs). Deterministic Network Model (DNM) and Probabilistic Network Model (PNM) have closely linked with the DAT and their work has focused on constructing the LBDAT under the PNM. Tree-based topology has preserved the cost of maintaining a routing table at each node and it tends to be more expensive in the nodes with the limited resources.

Optimal data aggregation tree has been constructed based on Intelligent Water Drops (IWDs) [12]. Sensor node has been organized into an optimal data aggregation tree with the selected aggregation nodes for effective data transmission. Further this has obtained the energy-efficient transmission of data within the network. Intelligent water drop is otherwise called as the novel optimization algorithm in which it has adopted to construct the optimal data aggregation trees for the WSNs. IWD algorithm has been proposed in this article in order to improve the tree construction by attempting to increase the probability of selecting optimum aggregation nodes. Treelet-based Clustered Compressive Data Aggregation (T-CCDA) has been proposed in [13]. This method is used to enhance the compressive sensing performance recovery and localized correlation structures among the sensor nodes. Further this implementation has become less efficient from the aggregated communication perspectives of underlying WSNs grow. Treelet transform also has the tendency to avoid the two main drawbacks of typical data regression techniques. Tree-based data aggregation techniques for WSN have been described in [14]. Authors have aimed to review the limitations of General Self-Organized Tree-based Energy Balance routing protocol (GSTEB). Distributed and collection phase are the two major steps involved in the tree-based data aggregation techniques. In this technique, data has been transferred from the leave nodes toward the coordinator node and aggregation has been performed at the parent node. Successive interference cancelation has recovered the signals to lead much reduced latency but increased the usage of energy with the tree-based aggregation approach.

2.3 In-Network Data Aggregation Technique

A cross-layer water marking-based data aggregation integrity mechanism in heterogeneous WSN has been explained in [15]. Efficient water marking-based security strategy has been proposed to ensure the integrity of data aggregation. It has optimized the process of data aggregation on the heterogeneous aggregation nodes. Further the author has adopted the reinforced fragile water marking classification in the high level of network. Homogeneous aggregation node, base station, heterogeneous sensor nodes are some of the components which are closely associated with each other in the network model. They have pointed that the data aggregation has been preserved by this proposed protocol effectively. The

energy-efficient data aggregation and transfer in Periodic Sensor Networks (PSNs) have been elaborated in [16]. Aggregation phase and adaptation phase are the two phases which have managed the efficiency of energy in PSN. In which, the proposed technique has eliminated the PSN redundant data over the network. This approach is similar to cluster which has mainly focused on the local processing and integration.

The delay performance of in-network aggregation in lossy WSN has been evaluated in [17]. The computation process at the intermediate nodes has increased the efficiency of network by reducing the number of transmissions. Further it has increased the information amount contained in the single packet to make the system vulnerable to the loss of packet. Distributed in-network computation has improved the efficiency of the communication in the system. It has resulted in significant improvements of performance in consumption of energy, memory usage, bandwidth, and delay when compared to the previous delivery paradigms of end-end information. Also, they have developed the new network architecture for the in-network computation and energy efficient in lossy environment. Authors in [18] comparatively presented the energy-efficient data collection techniques for WSN. Data aggregation, sleep wake scheduling, and adjustment of transmission power are some of the factors which are closely associated with the in-network approach. Energy efficiency of WSN has affected the lifetime of the network and the efficiency of energy has been increased by avoiding the unnecessary node operations.

2.4 Centralized Data Aggregation

Authors [19] studied about the data aggregation scheduling algorithms in WSN with solutions and challenges, in which the delay sensitive feedback control using the contention-free TDMA MAC protocol is considered as the centralized solutions. Moreover, the adaptive data aggregation for clustering WSN also acts as the centralized solution to reduce the energy consumption. In fact, the time allocation algorithm has been used to ensure the aggregation freshness and it also has the tendency to reduce the data latency in the applications of monitoring system. Data aggregation mechanism has been investigated for WSN in [20]. Centralized approach has been created to sense the data from the sensor nodes. Further it has aggregated the data by using proposed algorithm. Then, aggregated data has been transferred to the sink node by selecting the path efficiently. Flat networks, diffusion, SPIN, hierarchical, cluster-based, chain-based, and tree-based are some of the data aggregation-based networks which have been equipped with the same battery power. Authors reviewed about the energy efficiency data aggregation schemes in [21].

LEACH centralized algorithm has been utilized in a centralized clustering algorithm which has enhanced the clusters and it also requires less energy for

transmitting the data. Sequential aggregation scheduling is considered as the centralized solution and it is used as collision-free schedule with the latency bound at the specified level. Direct diffusion (DD) and the Sensor Protocol for Information via Negotiation (SPIN) are considered as the efficient data-centric protocol which has been involved under the centralized data aggregation effectively. In this technique, the data has gathered at the center node. In fact, the intermediate node has sent the data packets addressed to leader from the child nodes. They have pointed out that the DD has the tendency to sense the data with the attribute value pairs such as duration, localization, and time interval. Apart from these, SPIN has used the meta-data and descriptors in the higher level. Meta-data has exchanged among the sensors through the advertisement mechanism of the data before transmission. The main advantages of the centralized SPIN are simple in nature and it has high avoidance of implosion and economic start-up cost [22]. Apart from these, no feedback mechanism for data delivery is considered as the biggest disadvantages of this centralized SPIN algorithm. But according to the DD centralized algorithm, it extends the lifetime of the network effectively when compared to other algorithms. It is also considered as one of the merit of centralized data aggregation techniques, but the biggest demerits of this DD has not been used for continuous delivery of data. Authors have presented the centralized algorithms, which have been bounded with the hypothetical performance to the homogeneous and heterogeneous networks in optimal level. Authors have pointed out that centralized scheduling with the spatial reuse has created an impact on the energy efficiency of the WSNs effectively when compared to others.

3 Findings and Discussion

There are several challenges in data aggregation techniques such as data aggregation process quality, security, restricting storage and capabilities of processing, energy constraint sensor node and synchronization and link failure. To resolve these challenges, this study discussed about different data aggregation techniques, namely clustered aggregation, tree-based aggregation, in-network aggregation, and centralized aggregation technique. Suitable criterias have been referred to categorize existing solutions of data aggregation. Most existing review focuses on networking problems such as routing with moderate approaches to aggregate the data but how much work still remains to be performed to offer cross-layer solutions accounting for representation of data, application, and so on. A systematic research of relation between system lifetime and energy efficiency is an area of future study. Analytical outcomes on bounds for sensor networks lifetime is another research worth describing. Although several data aggregation techniques are discussed in this study with respect to WSN, there is an essential scope for future study. The comparison of different energy-efficient data aggregation techniques are summarised in Table 1.

Table 1 Energy-efficient data aggregation techniques in WSN

Cluster-based data aggregation technique	Tree-based data aggregation technique	In-network data aggregation technique	Centralized data aggregation technique
Cluster head has performed the data aggregation	Tree has built the data aggregation process effectively	It has optimized the process of data aggregation on the diverse nodes	It has taken the shortest path by using multi-hop protocol
It has removed the redundancy effectively by using other CH nodes	This has obtained the energy-efficient transmission of data within the network	Aggregation and Adaptation phases are the two phases used to manage energy	It has the tendency to reduce the data latency in the monitoring system
Deterministic clustering methods to save the node energy for resource dominant sensor network	It has not robust against the failures of communication which are also common in the sensor networks	Data security and Low energy are the biggest advantages of this technique	Centralized SPIN are simple and it has high avoidance of implosion and economic start-up cost
LEECH and HEED are the two protocols associated with this method	DNM and PNM are closely linked with the DAT	DRINA and Modified DRINA are the two algorithms associated with this technique	DD and SPIN are the two approaches closely linked with this technique
The features of topology are also linked with this scheme to achieve the higher results	Distributed and Collection phase are the two major steps involved in the tree-based data aggregation techniques	It has reduced the network bandwidth and consumptions of power requirements	CIAS has used to minimize the latency of process by using the topology of CDS

4 Conclusion and Future Recommendation

In WSNs, utmost of the energy is consumed for receiving and transmitting the data. The data aggregation process becomes an essential problem and optimization is required. Effective data aggregation not only offers conservation of energy but also removes redundancy data and hence offers useful information only. The techniques of data aggregation play an essential role for accomplishing efficiency of energy as they target to reduce several transmissions needed for collection of data which in turn decreases consumption of energy. Several approaches are provided considering suitable protocols of routing, efficient functions of aggregation and effective ways of representing the data. Several solutions are proposed in cluster, tree-based, in-network, and centralized data aggregation techniques. The future work will

concentrate on evolving new routing algorithms for data routing from source to sink. The approach must confront with the difficulties of topology construction, loss tolerance, and data tolerance by involving many techniques of optimization that further reduce costs of message and develop tolerance to loss and failure.

References

1. Sneha, R., Nithya, D.: Wireless sensor network: a survey. Int. J. Adv. Res. Comput. Sci. Soft. Eng. **6**(2), 92–95 (2016). ISSN: 2277 128X
2. Maraiya, K., Kant, K., Gupta, N.: Architectural based data aggregation techniques in wireless sensor network: a comparative study. Int. J. Comput. Sci. Eng. (IJCSE) **3**(3), 1131–1138 (2011). ISSN: 0975-3397
3. Cheng, C.-T., Leung, H., Maupin, P.: A delay-aware network structure for wireless sensor networks with in-network data fusion. IEEE Sens. J. **13**(5), 1622–1631 (2013)
4. Rajeswari, A., Kalaivaani, P.T.: Energy efficient routing protocol for wireless sensor networks using spatial correlation based medium access control protocol compared with IEEE 802.11. In: International Conference on Process Automation, Control and Computing (PACC), pp. 1–6 (2011)
5. Hirani, P.K.: Energy-efficiency based clustering and data aggregation for wireless sensor networks. Int. J. Comput. Appl. **119**(21), 1–4 (2015)
6. Patel, R.B., Aseri, T.C., Kumar, D.: Energy efficiency heterogeneous clustered scheme for wireless sensor network. Elsevier Int. J. Comput. Commun. **32**, 662–667 (2009)
7. Krishna, M.B., Vashishta, N.: Energy efficient data aggregation techniques in wireless sensor networks. In: 5th International Conference on Computational Intelligence and Communication Networks, pp. 160–165 (2013). doi:10.1109/CICN.2013.143
8. Ujawe, P.V., Khiani, S.: Review on data aggregation techniques for energy efficiency in wireless sensor networks. Int. J. Emerg. Technol. Adv. Eng. **4**(7), 142–145 (2014). ISSN 2250-2459
9. Yuan, F., Zhan, Y., Wang, Y.: Data density correlation degree clustering method for data aggregation in WSN. IEEE Sens. J. **14**(4), 1089–1098 (2014)
10. Atoui, I., Ahmadt, A., Medlej, M.: Tree-based Data aggregation approach in wireless sensor network using fitting functions. 146–150 (2016). ISBN: 978-1-4673-7504-7
11. He (Selena), J., Ji, S., Pan, Y., Li, Y.: Constructing load-balanced data aggregation trees in probabilistic wireless sensor networks. IEEE Trans. Parallel Distrib. Syst. **25**(7), 1681–1690 (2014)
12. Chinh Hoang, D., Kumar, R., Kumar Panda, S.: Optimal data aggregation tree in wireless sensor networks based on intelligent water drops algorithm. IET J. Wireless Sens. Syst. **2**(3), 282–292 (2012)
13. Zhao, C., Zhang, W., Yang, Y., Yao, S.: Treelet-based clustered compressive data aggregation for wireless sensor networks. IEEE Trans. Veh. Technol. **64**(9), 4257–4267 (2015)
14. Kaur, S., Gangwar, R.C.: A study of tree based data aggregation techniques for WSNs. Int. J. Database Theor. Appl. **9**(1), 109–118 (2016)
15. Boubiche, D.E., Boubiche, S., Bilami, A.: A Cross-layer watermarking-based mechanism for data aggregation integrity in heterogeneous WSNs. IEEE Commun. Lett. **19**(5), 823–826 (2015)
16. Harb, H., Makhoul, A., Tawil, R., Jaber, A.: Energy-efficient data aggregation and transfer in periodic sensor networks. IET J. Wireless Sens. Syst. **4**(4), 149–158 (2014)
17. Joo, C., Shroff, N.B.: On the delay performance of in-network aggregation in lossy wireless sensor networks. IEEE/ACM Trans. Netw. **22**(2), 662–672 (2014)

18. Rohankar, R., Katti, C.P., Kumar, S.: Comparison of energy efficient data collection techniques in wireless sensor networks. Procedia Comput. Sci. **57**, 146–151 (2015)
19. Bagaa, M., Challal, Y., Ksentini, A.: Data aggregation scheduling algorithms in wireless sensor networks: solutions and challenges. IEEE Commun. Surv. Tutorials **16**(3), 1339–1369 (2014)
20. Dagar, M., Mahajan, S.: Data aggregation in wireless sensor network: a survey. Int. J. Inf. Comput. Technol. **3**(3), 167–174 (2013). ISSN 0974-2239
21. Gopikrishnan, S., Priakanth, P., Mahendhiran, P.D.: A survey of energy efficient data aggregation schemes in wireless sensor networks. Middle-East J. Sci. Res. **23**(10), 2603–2612 (2015)
22. Yu, Y., Prasanna, V.K., Krishnamachari, B.: Energy minimization for real-time data gathering in wireless sensor networks. IEEE Trans. Wireless Commun. **5**(11), 3087–3096 (2006)

Design and Performance Analysis of Noise Equivalent Model for Optical Fiber Link

Manoj Kumar Dutta

Abstract In optical communication system different types of noises may be introduced into the signal. The effect of noise and corresponding degradation in the signal quality is of great interest for the design of fiber-optic communication systems. In the present paper an electrical equivalent form of different important noises has been developed in order to investigate its effects on the efficiency of an optical fiber link. The basic components of an optical link are laser diodes, fiber, splices, and optical detector. In the proposed model the laser diode is represented as voltage source with internal resistance. Thermal noise in fiber, connectors, and splices is estimated by using an equivalent resistor. PIN photodetector is choosen for the proposed optical link and equivalent circuit model for the same is derived by carrier rate equations using RC circuit with current sources. The variation of noise current with the variation of frequency is shown.

Keywords Noise in optical fiber link · Thermal noise · Shot noise
Modal noise · Electrical equivalent model

1 Introduction

Any fiber-optic communication link is composed of optical transmitter, fiber channel and optical receiver. Each of these components has different functions in order to transmit information from one place to another. Transmitter in optical domain is used for conversion of electrical signal to its equivalent optical form. The generated optical signal is transmitted to the destination through optical fiber. The receiver at the destination receives the optical signal and converts back to its original electrical form. The basic component of an optical receiver is the photodetector. When the signal passes through the different components of the optical links, different impairments, viz., thermal noise, shot noise, inter symbol interfer-

M.K. Dutta (✉)
BIT Mesra, Deoghar Campus, Deoghar 814142, Jharkhand, India
e-mail: manoj@bitmesra.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_18

ence (ISI) and signal dependent noise may be introduced within the original signal. Thermal noise arises from detector load resistor and from random nature of carriers. The effect due to thermal noise is a major limitation in case of p-i-n photodetector. The quantum or shot noise arises from the statistical nature of the production and collection of photoelectrons when an optical signal is incident on a photodetector. This statistics follow a Poisson process. The signal-dependent noises are modal noise, mode partition noise and relative intensity noise. The above-mentioned noises may degrade the quality of signal. The aim of this paper is to model the electrical equivalent circuit for different noises that arise in the optical fiber communication link and to investigate their effects on the signal carrying capacity of the link [1–4]. In this paper a semiconductor laser diode is considered for estimation of shot noise in an optical fiber link. Electrical counterpart of a laser diode, connectors and PIN avalanche photodiode are developed. Total noise in the fiber optic link is also estimated at different frequencies.

2 Methodology

2.1 Noise in Laser Source

The integrated electrical equivalent circuit model of a fiber-optic link is developed by three important steps. First, semiconductor laser model for shot noise and its equivalent circuit is developed by the inclusion of Langevin noise sources. Second, thermal noise in fiber, connectors and splices is estimated and then PIN Avalanche photodiodes model is developed for noise calculation. Finally, total noise of the fiber link is obtained.

Fluctuations of intrinsic intensity in semiconductor laser diode are due to electron hole recombination within the lasing medium and quantum statistical photon generation. In an optical transmission system photocurrent is generated because of the incident photon and noise is generated because of change in electron (N) or photon population (P).

Intensity variation of laser source may be obtained by summation of noise source factor $F_S(t)$ for photons and $F_N(t)$ for electrons. As in [1, 5, 6]

$$\frac{\mathrm{d}N}{\mathrm{d}t} = \frac{I}{q} - \frac{N}{T_s} - (E_c - E_v)p + F_N(t) \tag{1}$$

$$\frac{\mathrm{d}P}{\mathrm{d}t} = (E_c - E_v)p + \frac{\beta N}{T_s} - \frac{P}{T_p} + F_s(t) \tag{2}$$

where

$\mathrm{d}N/\mathrm{d}t$ rate of change of electrons number in the gain medium
$\mathrm{d}P/\mathrm{d}t$ rate of change of photons number in lasing mode

I/q pump rate
T_s electron lifetime
T_p photon lifetime

$\frac{\beta N}{T_s}$ = Amount of coupled spontaneous emission within the lasing mode
E_c and E_v are downward and upward stimulated emission rate respectively.
The gain, $A = E_c - E_v$
The equations for average rates are obtained by setting time average of F_N and F_s equals to zero as

$$\frac{I_0}{q} - \frac{N_0}{I_s} - A_0 P_0 = 0 \tag{3}$$

$$-\frac{P_0}{I_0} + A_0 P_0 + \frac{\beta N_0}{I_s} = 0 \tag{4}$$

where

I_0 DC pump current
A_0 average value of gain
N_0 electron population
P_0 number of photon in the lasing mode

The laser diode can be realized by a combination of a diffusion capacitance C, a diode resistance R and an inductive load L with a series resistance R_L. Using these electrical parameters, small signal noise equivalent of laser diode is developed as shown in Fig. 1. By proper analysis, corresponding noise intensity of a laser diode can be calculated.

In Fig. 1 I, V, I_L and I_N are input signal current, input signal voltage, output signal current and noise current respectively. From the equivalent circuit it is obtained that the value of C, R, L and R_L as follows [4].

$$C = \frac{q}{[mV_T N_0]} \tag{5}$$

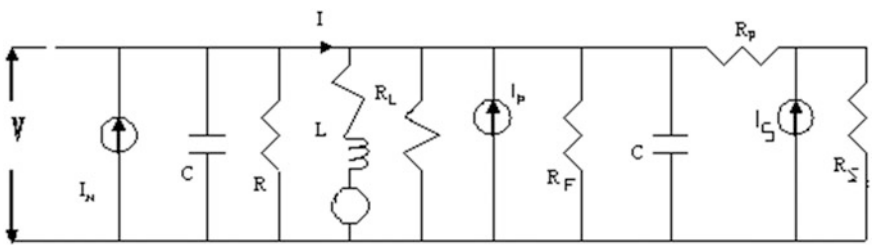


Fig. 1 Shows equivalent noise circuit implementation of a fiber-optic link

$$R = \frac{mV_T}{\left[qN_0\left[Kp_0 + \left(\frac{1}{T_s}\right)\right]\right]} \tag{6}$$

$$L = \frac{mV_T}{\left[qN_0A_0\left[Kp_0 + \left(\frac{\beta}{T_s}\right)\right]\right]} \tag{7}$$

$$R_L = \frac{mV_T\beta}{\left[qT_pp_0A_0\left[Kp_0 + \left(\frac{\beta}{T_s}\right)\right]\right]} \tag{8}$$

where

$K = \frac{dA}{dN}$ = differential gain slope

$$V_T = \frac{KT}{q}$$

'm' may be obtained by Fermi–Dirac distribution function [7].
Intensity due to current noise can be obtained by [4]

$$I_N^2 = [2qI_0 + 4q^2E_vP_0]\Delta f \tag{9}$$

where, $2qI_0$ is the shot noise of a non-lasing diode.

2.2 Noise of Optical Fiber, Splices, and Connectors

The intermodal dispersion properties of optical fiber generates a noise known as modal or speckle noise [1, 8]. The basic conditions for modal noise are

(a) Coherent source narrow spectral width and long coherence length.
(b) Disturbances along the fiber.
(c) Face correlation between two modes.

Thermal noise in optical fiber also degrades the performance of fiber-optic data link [9]. Losses in optical fiber due to splice connector and different bends are a principle factor of thermal noise. This noise can be estimated by using a temperature equivalent resistor R_F in the circuit with noise current sources as shown in Fig. 1.

2.3 Noise of PIN Avalanche Photodetector

The average PIN photocurrent produced by a PIN avalanche photodiode is [10]

$$I_p = \frac{\eta P_w \lambda q}{hc} \tag{10}$$

where

P_W incident optical power
λ wavelength of incident signal
η quantum efficiency

Let us assume modulated signal is

$$P(w) = P_m(1 + m_1 e^{j\omega t})$$

And the r.m.s current is

$$I_p = \frac{(\eta q m_1 P_m \lambda)}{\sqrt{2hc}} \tag{11}$$

where

m_1 modulation index
w modulation frequency
P_m average input power

The contribution to shot noise by PIN diode is

$$\frac{I_s}{\Delta f} = 2q(I_p + I_D) \tag{12}$$

where

Δf frequency bandwidth

Current due to dark noise i_D

$$i_D = 2qI_D\Delta f \tag{13}$$

Thermal noise current I_T

$$I_T = \frac{4KT\delta f}{R_{\text{eq}}} \tag{14}$$

Therefore,

$$I_s = 2q\left(I_p + I_D\right)\Delta f \tag{15}$$

The equivalent resistance is

$$\frac{1}{R_{\text{eq}}} \approx \frac{1}{R_j} + \frac{1}{R_s} \tag{16}$$

3 Results and Discussion

The complete electrical equivalent circuit model for the fiber-optic link is shown in Fig. 1 which is synthesized using derived equations for noise calculation of laser diode, optical fiber, connector, splices and photodiode. The total equivalent noise current is the algebraic summation of the noise current of laser diode I_N^2, noise current due to fiber, connector, splices I_p^2 and noise current due to PIN photodiode I_s^2. In case of single mode fiber the effects due to splices, modal noise and connector losses may be reduced to a large extent in the fiber link. RMS signal to noise ratio can be reduced by around 10 dB using good narrow line width injected laser [8]. Neglecting fiber noise, total noise current of fiber-optic link is plotted against frequency as shown in Fig. 2. It shows that the total noise increases with frequency and noise current is low in infrared region.

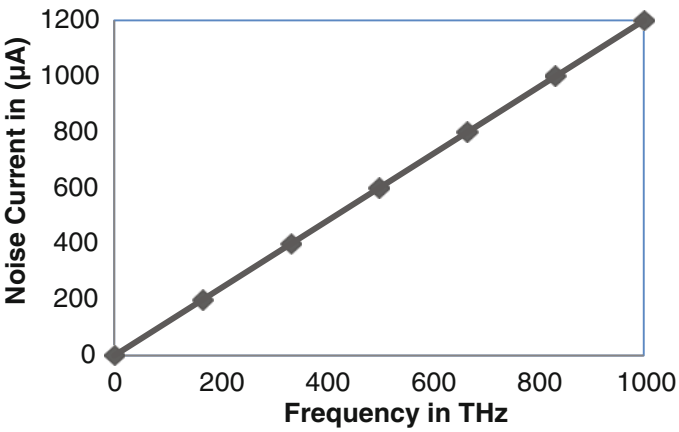


Fig. 2 Total noise current versus frequency curve

4 Conclusion

Electrical noise equivalent circuit analysis of different impairments and nonlinear effects of an optical fiber link have been discussed in this paper. The proposed model has been used to investigate the effects of signal impairments on the optical fiber link performance. The noise equivalent circuit model for a fiber-optic link has been presented by adding current noise sources. The proposed model circuit includes almost all the essential optical components of an optical link, viz., laser diode, optical fiber, splices, connectors and PIN avalanche photodetector. Different noises of the link are replaced by current sources. The integrated equivalent circuit for noise calculation of fiber optic components that are demonstrated here may be useful for design of low noise fiber-optic link.

Acknowledgements The author would like to thank the authorities of Birla Institute of Technology, Mesra and Off-campus Deoghar for all the supports provided and granting institute seed money scheme to carry out this work.

References

1. Moratzy, E., Ahmadi, V., Moravvej-Farshi, M.K.: An integrated equivalent circuit model for relative intensity noise and frequency noise spectrum of a multimode semiconductor laser. IEEE J. Quant. Electron **38**(10), 1366–1371 (2002)
2. Morishita, A., Ohmi, T., Nishizawa, J.: Impedence characteristics of double-heterostructure laser diodes. Solid-State Electron **22**, 951–962 (1979)
3. Katz, J., Margalit, S., Harder, C., Wilt, D., Yariv, A.: The intrinsic equivalent circuit of a laser diode. IEEE J. Quantum Electron **QE-17**, 4–7 (1981)
4. Harder, C., Katz, J., Margalit, S., Shacham, J., Yariv, A.: Noise equivalent circuit of semiconductor laser diode. IEEE J. Quantum Electron **QE-18**, 333–337 (1982)
5. McCumber, D.E.: Intensity fluctuation in the output of cw laser oscillator. Phys. Rev. **141**, 306–322 (1966)
6. Haug, H.: Quantum mechanical rate equations for semiconductor lasers. Phys. Rev. **184**, 338–348 (1969)
7. Joyce, W.B., Dixon, R.W.: Analytic approximation for the fermi energy of an ideal fermi gas. Appl. Phys. Lett. **31**, 354–356 (1977)
8. John, M.: Optical Fiber Communications, 2nd edn. PHI (2005)
9. Arnold, H., Petermann, K.: Intrinsic noise of semiconductor lasers in optical communication systems. Opt. Quantum Electron **12**, 207–219 (1980)
10. Chen, H., Liu, S.: PIN avalanche photodiodes model for circuit simulation. IEEE J. Quantum Electron **31**, 2105–2109 (1996)

Improvement of Efficiency of a Three-Phase Induction Motor Using Robust Control

Anirban Sengupta

Abstract Slip power recovery scheme is widely used for controlling the speed of a three-phase induction motor, but this method can also be used for increasing the efficiency of an induction motor. Here, a three-phase induction motor has been designed using vector-controlled induction motor drive and then the controlled strategy is introduced in this induction motor. The control strategy is based on feeding the slip power back to the rotor of a slip ring induction motor. The efficiency and torque of a three-phase induction motor depend upon the slip of the motor. This controller monitors the speed of the motor from no load to full load and takes the appropriate control action to maintain the speed of the motor. After implementation of this control strategy, it has been seen that the induction motor is trying to maintain the no load speed and as a result, the power output of the motor has been increased considerably.

Keywords Induction motor · Slip power recovery scheme · Losses and efficiency

1 Introduction

With the development of power electronics converters, the use of Induction motor has been increased tremendously for the industrial applications. This is because of its robustness, high torque and long life. More than 60% of the industrial applications are from induction motor [1].

The major disadvantage of a three-phase induction motor is its low efficiency. This is because of many factors. There are several losses in an induction motor. The friction loss of an induction motor can be minimized by increasing the air gap between the stator and rotor. But if we increase the air gap, then the power factor of

A. Sengupta (✉)
Department of Electrical & Electronics Engineering, Sikkim Manipal Institute of Technology, Sikkim Manipal University, Manipal, Sikkim, India
e-mail: anirbansengupta09@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_19

the motor will decrease. Also the power loss is dependent on the slip of the motor [2]. If we increase the slip then the power loss will decrease and vice versa.

In this paper, a three-phase slip ring induction motor has been designed using vector control. The slip power recovery scheme has been introduced to control the speed of the induction motor. Controlling the speed means controlling the slip of the motor as the slip of the motor depends upon the speed of the motor.

The next session describes the different types of power losses of a three-phase induction motor and the factors on which the output of three-phase induction motor depends. Section 3 describes the proposed control strategy to improve the efficiency of the three-phase induction motor. Next at Sect. 4, the result of the simulation is presented and the paper concludes at Sect. 5.

2 Losses of Induction Motor

The losses of an induction motor can be divided into two categories. These losses are

(i) Fixed Loss
(ii) Variable Loss

Fixed losses are those losses which do not depend upon the loading. These losses are always present under the application of normal voltage. Fixed losses occur mainly in the stator of an induction motor.

The variable losses are those which are not fixed. The classification of variable losses is described in Fig. 1.

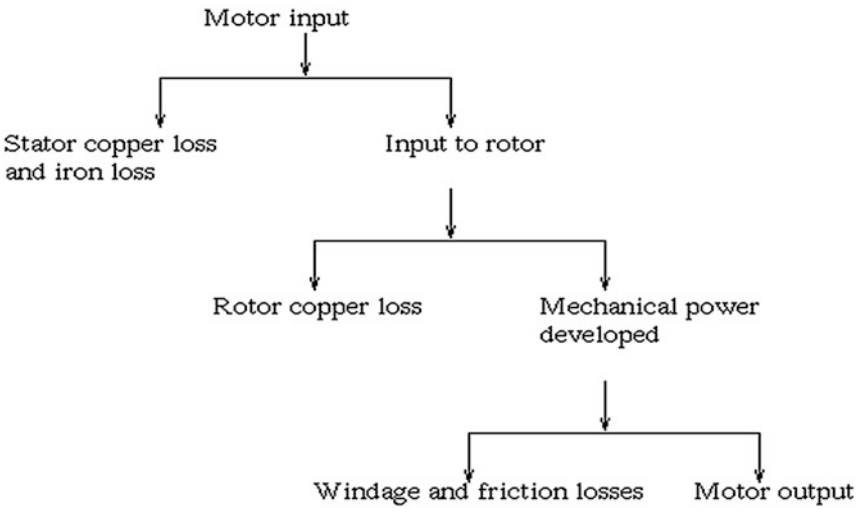


Fig. 1 Variable losses of three-phase induction motor

Variable losses are also known as the copper loss. These losses depend on the amount of load. If the load increases then the current drawn by the motor also increases. As a result the amount of loss of the motor also increases. Since the amount of loading on the motor is not fixed, the variable loss is also not fixed as well [3].

If P_{in} = Electrical power input to the three-phase induction motor, then

$$P_{in} = (\sqrt{3})(V_L)(I_L)\cos\theta, \tag{1}$$

where

V_L Applied line voltage to the stator
I_L Line current
$\cos\theta$ Power factor of the motor

Power input to the rotor can be given by

$$P_R = P_{in} - P_s, \tag{2}$$

where

P_s Total losses in the stator

And rotor copper loss is given by

$$P_{RL} = P_R \times S \tag{3}$$

where

S Slip of the motor

Therefore the output of the motor is given by

$$P_o = P_R - P_{RL} - \text{Friction and windage loss} \tag{4}$$

And the efficiency of the motor is

$$\eta = (P_o)/(P_{in}) \tag{5}$$

3 Proposed Control Strategy

In this proposed technique, we have injected an EMF of slip frequency in the rotor circuit of the induction motor. Thus the output power of the induction motor increases somehow. The phasor diagram of induction motor with EMF of slip frequency injected in its rotor circuit is shown in Fig. 2.

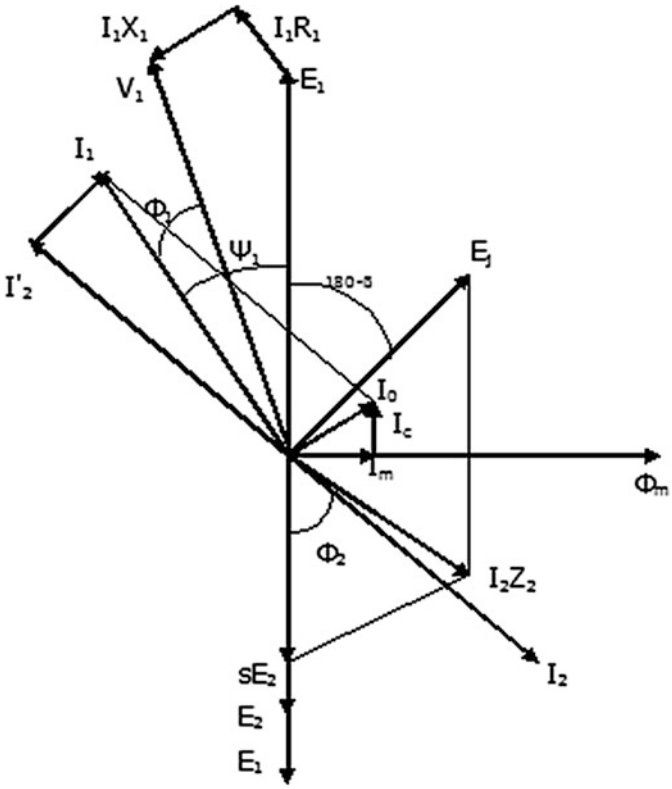


Fig. 2 Phasor diagram of induction motor with slip power injected in its rotor circuit

From Fig. 2 it is clear that

$$\begin{aligned} \text{Power input} &= E_1 I_1 \cos\psi_1 \\ &= I_1^2 R_1 + E_1 I_c + E_1 I_2 \cos\varphi_2 \end{aligned} \tag{6}$$

Resolving EMF on I_2 we get,

$$SE_1 I_2 \cos\varphi_2 = I_2^2 R_2 + E_j I_2 \cos(180^\circ - \beta + \varphi_2) \tag{7}$$

Thus, proceeding in the same way we can find that

$$\begin{aligned} \text{Power transfer to the secondary} = {} & \text{Rotor copper loss} + \text{Slip Power} \\ & + \text{Mechanical power output.} \end{aligned}$$

The schematic diagram and proposed strategy are shown in Figs. 3 and 4, respectively [4, 5].

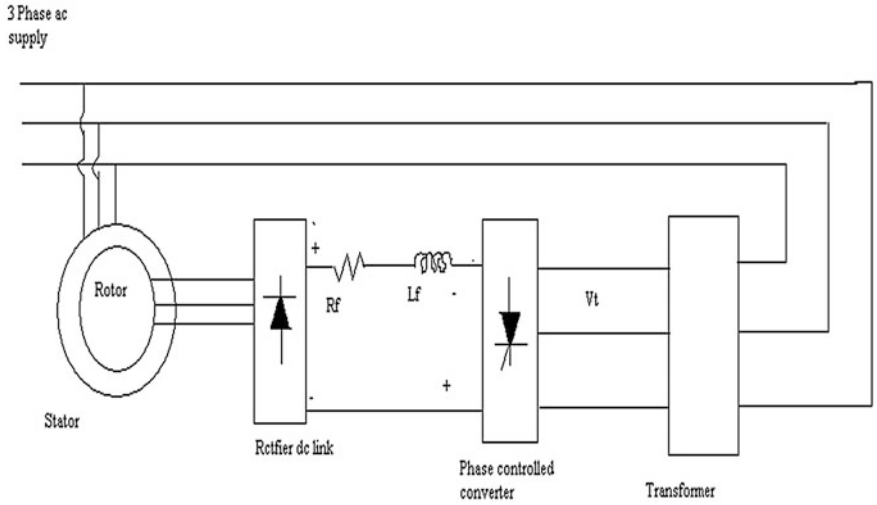


Fig. 3 Schematic diagram of slip power recovery scheme

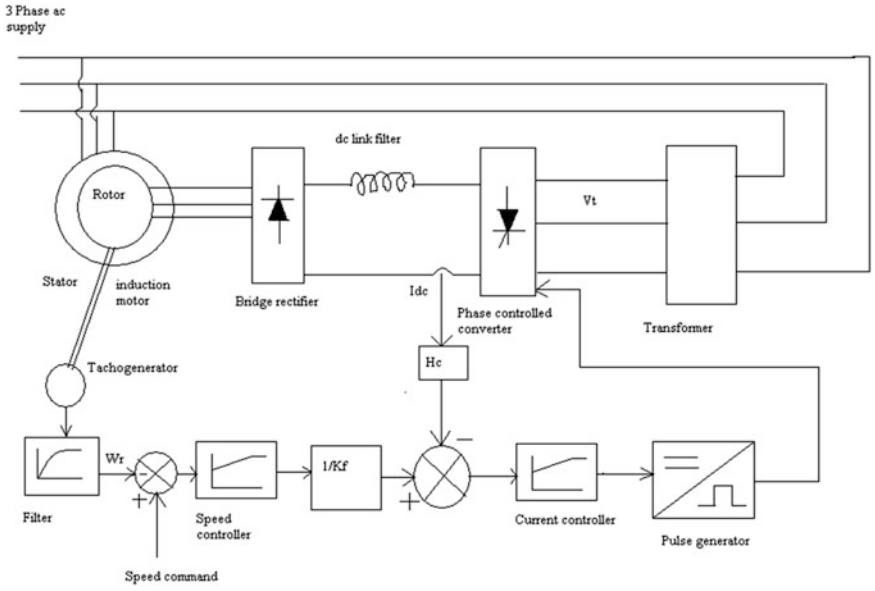


Fig. 4 Proposed control strategy of slip power recovery scheme

A closed-loop control scheme for slip power recovery method is shown in Fig. 3. There are two loops. First loop is current controlled loop. Since torque of an induction motor is dependent on current, the current controlled loop is also known as the torque loop. The second loop calculates the reference speed. If the speed

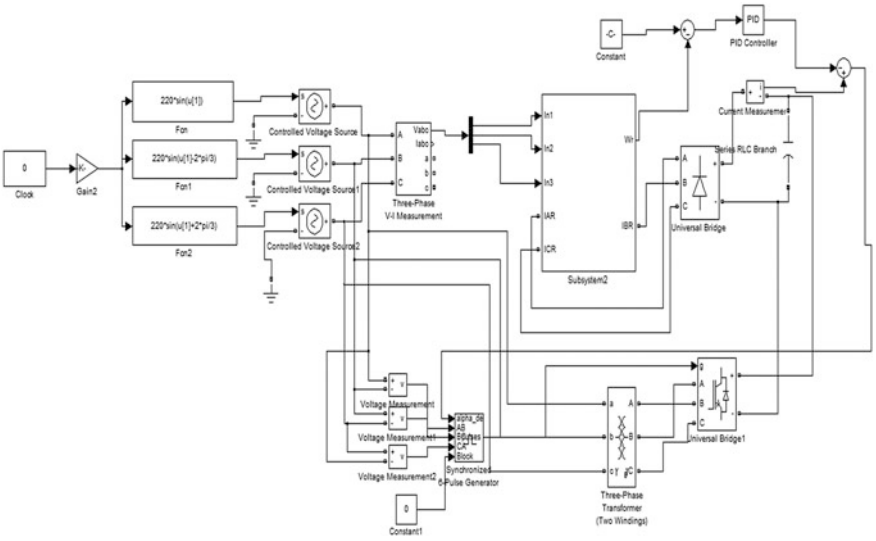


Fig. 5 SIMULINK model of the complete control technique

of the motor is not same as the reference speed, then the difference of speed, which is the error speed, is supplied to a PI controller after amplification. If there is an error then that error produces the torque. Since torque is proportional to current, it can be also concluded that a current will be produced. This current is also converted to control voltage V_C after supplying this error through another PI controller. This voltage can be converted into a gate pulse [6].

The complete SIMULINK diagram of the control strategy is shown in Fig. 5.

4 Result and Discussion

The entire system is simulated in MATLAB/SIMULINK. At first, a three-phase induction motor is modelled in SIMULINK and then a load has been introduced at $t = 3$ s in this induction motor. As a result a change in speed and the rotor current has been seen in the motor and the stator current was unaffected. The result of the load without the efficiency optimization controller is shown in Figs. 6, 7, 8, 9, 10 and 11.

From the figures, it is clear that the efficiency optimization controller reduces the speed and the rotor speed variation from no load to full load. As a result, the slip of the motor reduces because of the efficiency optimization controller. From Eq. (3) it is clear that rotor copper loss depends upon the slip of the motor. Therefore, the

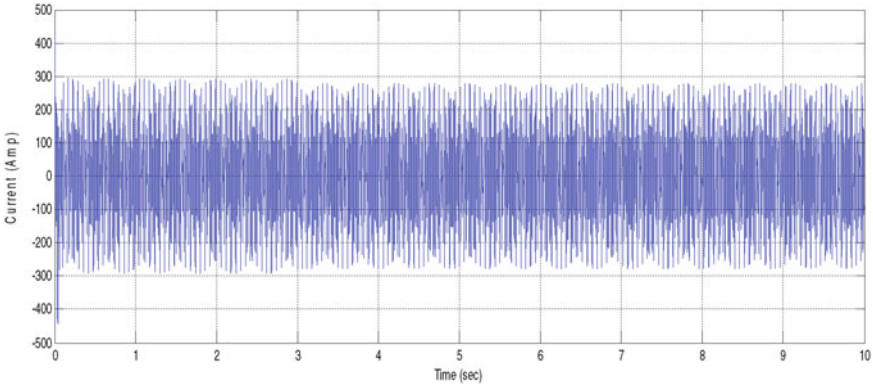


Fig. 6 Variation of stator current without efficiency optimization controller

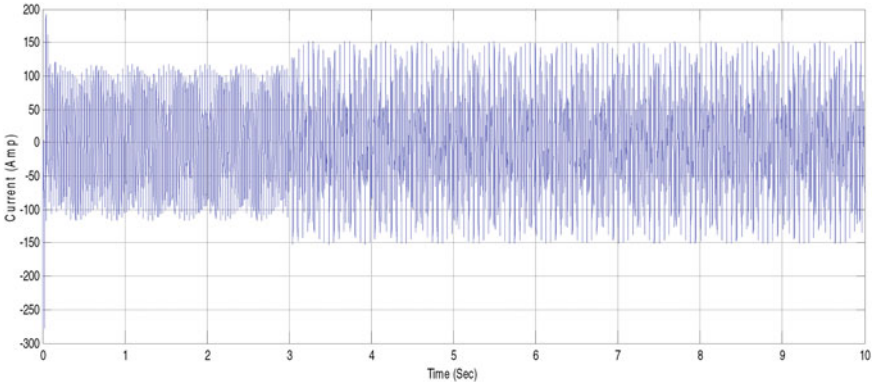


Fig. 7 Variation of rotor current without efficiency optimization controller

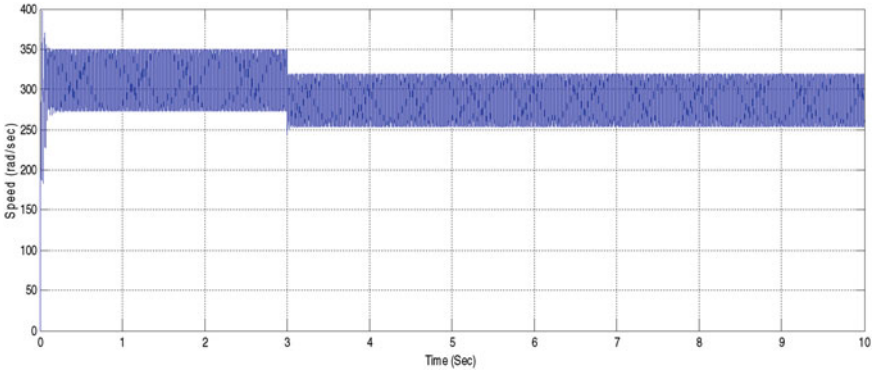


Fig. 8 Variation of rotor speed without the efficiency optimization controller

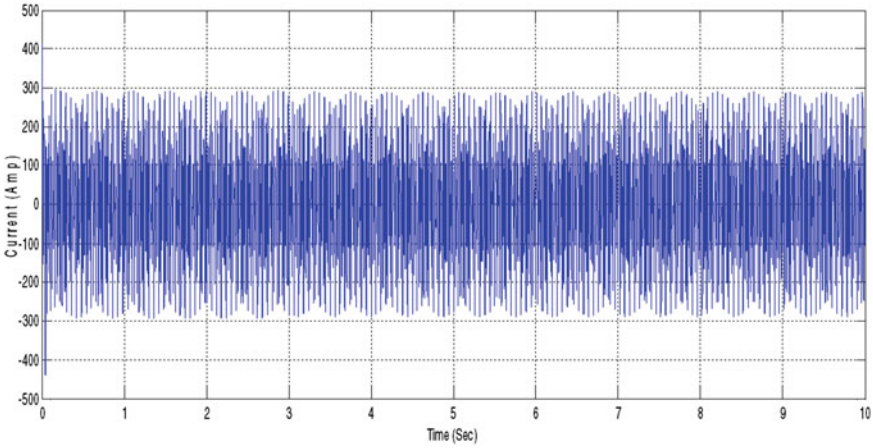


Fig. 9 Variation of stator current with efficiency optimization controller

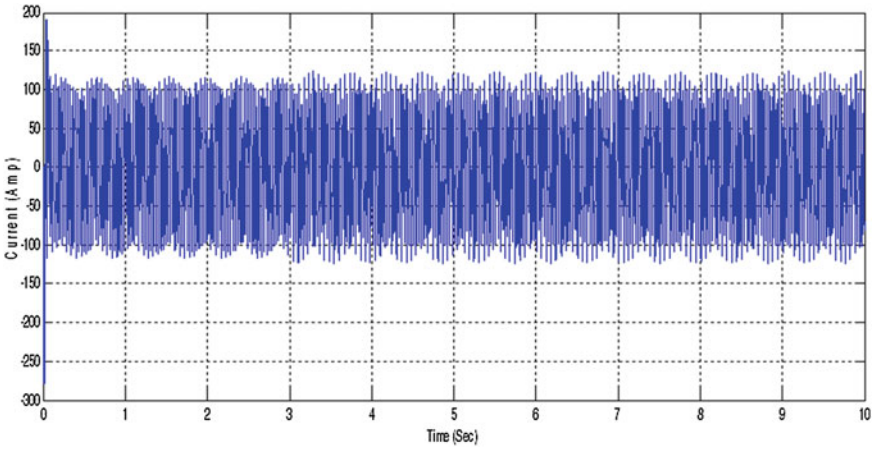


Fig. 10 Variation of rotor current with efficiency optimization controller

efficiency optimization controller reduces the rotor copper loss or it increases the overall efficiency of the motor. Also it can be concluded that the variation of the rotor current also reduces because of the efficiency optimization controller. Therefore, I_2^2R loss in the rotor circuit also reduces with the implementation of the controller.

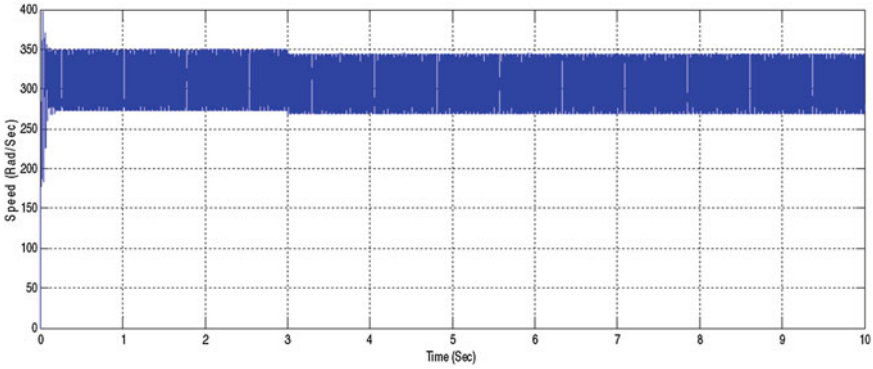


Fig. 11 Variation of rotor speed with efficiency optimization controller

5 Conclusion

The main objective of this paper is to implement an efficiency optimization controller to improve the efficiency of the three-phase induction motor. To achieve that a robust control strategy using slip power recovery method has been implemented. After implementation, it can be concluded that there is a significant improvement in the efficiency of the three-phase induction motor and also the life of the induction motor will be more.

References

1. Vukosavic, S.N.: Controlled Electrical Drives—Status of Technology. Zbornik XLII konf. Etran-a, Vrnjacka Banja, pp. 2–5 (1998)
2. Garcia, G., Luis, J.: An efficient controller for an adjustable speed induction motor drive, IEEE Trans. Ind. Elec. **31**(5), 533–539 (1994)
3. Bottauscio, O., Pellegrino, G., Guglielmi, P., Chiampi, M., Vagati, A.: Rotor loss estimation in permanent magnet machines with concentrated windings. IEEE Trans. Magn. **41**(10), 3913–3915 (2005)
4. Wakabayashi, T., Hori, T., Shimzu, K., Yoshioka, T.: Commutatorless Kramer control system for large capacity induction motors for driving water service pumps. IEEE/IAS Annual Meeting Conference on Record, pp. 822–828 (1976)
5. Weiss, H.W.: Adjustable speed AC drive system for pump and compressor application. IEEE Trans, Ind. Appl. **10**, 157–162 (1975)
6. Pillay, P., Refoufi, L.: Calculation of slip energy recovery induction motor drive behaviour using the equivalent circuit. IEEE Trans. Ind. Appl. **30**(1) (1994)

Improvement of Electrical Power Quality with Distributed Power Flow Controller with Fuzzy PWM Technique

Jyoti Saraswat and Jaydeep Chakravorty

Abstract With the rise in the need of electricity globally and because of an enlargement in industry market and also due to the increase in urbanization, the nonlinear load in the power grid has considerably increased in the few decade. Now electricity has become an essential commodity in our life. To cater this growing demand of power energy, everyone is now a concern about the quality of electrical power. Frequent voltage fluctuations and power loss reduction are the major challenge in the power system sector. So, the quality of power is an issue which is equally important for both the end users and electric utilities. This paper gives a model of distributed power flow controller (DPFC) with fuzzy PI controller for control of electrical power system. In DPFC, multiple series converters and one shunt converter are used and also there is no DC link between them. The proposed model with fuzzy PWM has been implemented in MATLAB/Simulink environment and tested for 5 bus system.

Keywords Power system · Distributed power flow controller (DPFC) Fuzzy · FACTS · PWM

1 Introduction

Reliable and uninterrupted power flow is the most important issue in the power sector nowadays. Power quality issues have become a most important part of a power system [1]. In an AC transmission system, from the power flow calculation, we get the voltage and current at each and every bus in the system at a particular load and also the real and reactive power flow with. This calculation is the most important in the proper design of a stable power system. FCATS devices that were

J. Saraswat · J. Chakravorty (✉)
Electrical Department, Baddi University, Baddi, HP, India
e-mail: jaydeepchak@yahoo.co.in

J. Saraswat
e-mail: jyotisara@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_20

introduced in the power system almost more than two decades ago are a power electronics based device which is used to control the power transfer capability of an A.C. system, and power flow control [2, 3]. To solve the problem of power quality, FACTS devices and DVR can be used in the transmission lines [4–6]. To improve the power quality, the use of UPFC and STATCOM has also become helpful [7, 8]. UPFC is basically the combined effect of static synchronous compensator (STATCOM) and static synchronous series compensator (SSSC). These two devices are connected with each other with a DC link. Because of this DC link, active power can flow in both the directions between the output terminals of the SSSC and the output terminals of the STATCOM. DPFC has similar configuration as that of UPFC only the DC link is absent in case of DPFC. Through the transmission line, at third harmonic frequency, the exchange of active power between the shunt and the series converter takes place [9, 10]. A device having the concept of power exchange by the help of harmonic and also the concept of DEFACTS is called DPFC. Therefore, the DPFC has the combined advantageous properties of UPFC and the DFACTS. The method is actually the concept of power theory of non-sinusoidal components [10]. In this paper, a model of DPFC with fuzzy PWM technique has been given. Also, its effectiveness has been tested in 5 bus system. The complete set-up has been implemented in MATLAB/Simulink environment.

2 Modelling of Proposed DPFC with Fuzzy PWM

The model of DPFC is represented in Fig. 1.

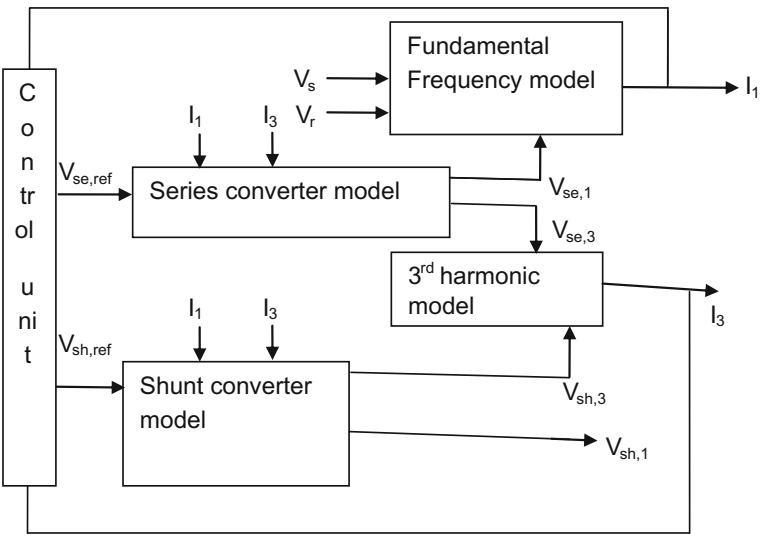


Fig. 1 Block diagram of DPFC

It has mainly five blocks, namely, fundamental frequency block, the third harmonic block, series converter block, the shunt converter block and the block of control unit. Here, V_s and V_r are the voltage of sending end and the voltage of receiving end respectively. I_1 is the first harmonic current, I_3 is the third harmonic current, $V_{se,1}$ is the injected voltage at fundamental frequency by series converter, $V_{se,3}$ is the injected voltage at third frequency by series converter, $V_{se,ref}$ is the modulated amplitude of the reference AC signal generated by series control unit and $V_{sh,ref}$ is the amplitude of modulated AC signal, which is a reference signal, generated by shunt control unit. $V_{sh,1}$ and $V_{sh,3}$ are the magnitudes of voltage of the shunt converters having the ith harmonic [10]. The Simulink implementation of these five blocks is as follows.

The Simulink model of fundamental frequency network is depicted in Fig. 2; it has been modelled from the equation

$$[V_s] - [V_r] - [V_{se1}] = [Z_1] \times [I_1]$$

Here, V_s, V_r, V_{se1}, Z_1 and I_1 are the matrix of three phase voltages, impedance at first harmonic and current, respectively.

The Simulink model in MATLAB of third harmonic network is represented in Fig. 3; it has been modelled from the equation

$$[V_{sh3}] - [V_{se3}] = [Z_3] \times [I_3]$$

Here, V_{sh3}, V_{se3}, Z_3 and I_3 are the matrix of three-phase third harmonic voltages, impedance and current, respectively.

The representation of series converter model has been indicated in Fig. 4, which is modeled from, the equation

$$C_{se}\frac{dV_{dc\_se}}{dt} = \frac{1}{2}\left(V_{se\_1\_d\_ref} \times I_{d\_1} + V_{se\_1\_q\_ref} \times I_{q\_1}\right) + \frac{1}{2}\left(V_{se\_3\_d\_ref} \times I_{d\_3} + V_{se\_3\_q\_ref} \times I_{q\_3}\right)$$

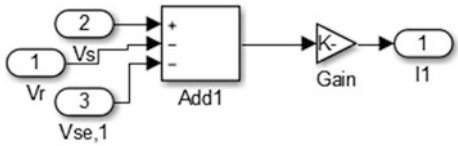


Fig. 2 Fundamental frequency model

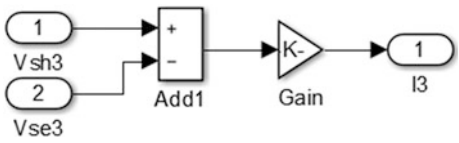


Fig. 3 Third harmonic network model

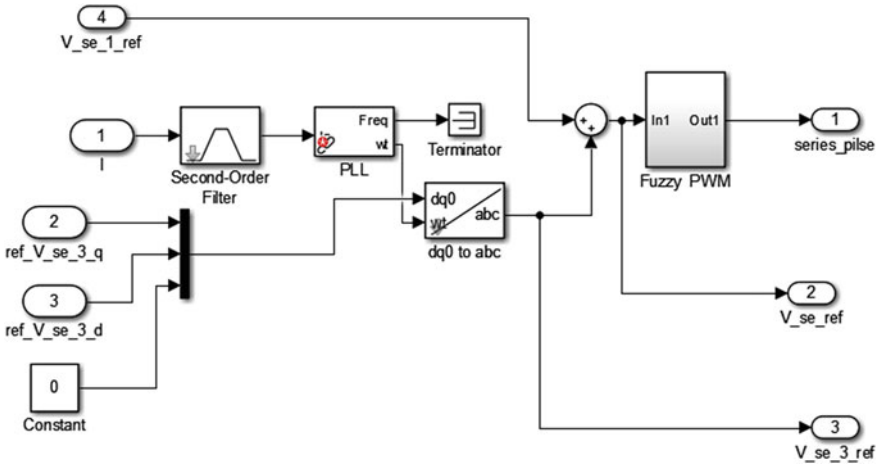


Fig. 4 Series converter

The shunt converter is obtained from the equation and the Simulink model is shown in Fig. 5.

$$C_{\mathrm{sh}}\frac{\mathrm{d}V_{\mathrm{dc\_sh}}}{\mathrm{d}t}=\frac{3}{2}\left(V_{\mathrm{sh\_1\_d\_ref}}\times I_{\mathrm{sh\_d\_1}}+V_{\mathrm{sh\_1\_q\_ref}}\times I_{\mathrm{sh\_q\_1}}\right)-\frac{1}{2}\left(V_{\mathrm{sh\_3\_d\_ref}}\times I_{\mathrm{sh\_d\_3}}+V_{\mathrm{sh\_3\_q\_ref}}\times I_{\mathrm{sh\_q\_3}}\right)$$

Similarly, the Simulink model of series and shunt control is shown in Figs. 6, 7 and 8.

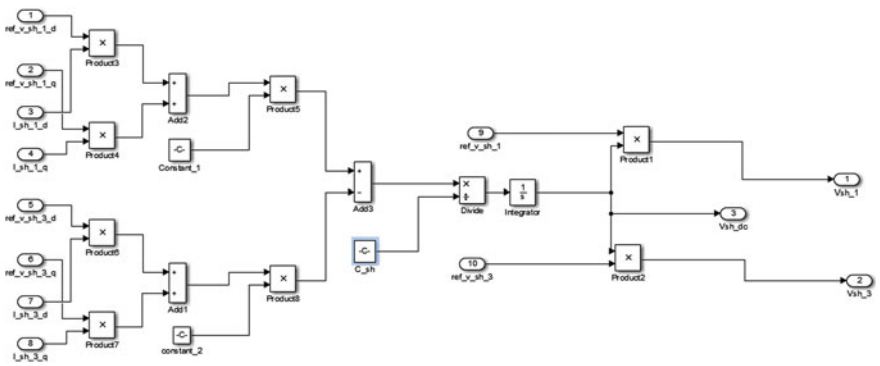


Fig. 5 Shunt converter

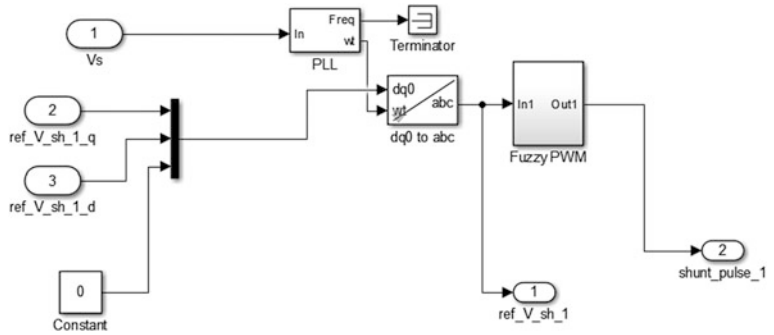


Fig. 6 Series control

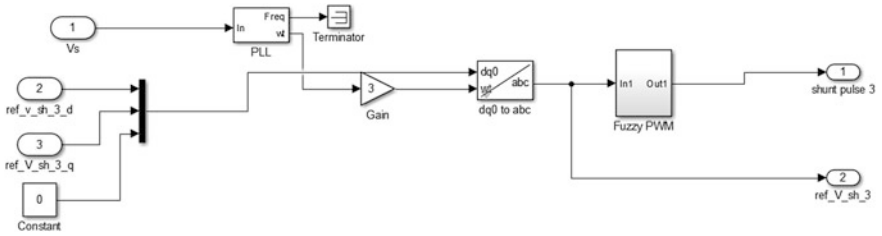


Fig. 7 Shunt control fundamental

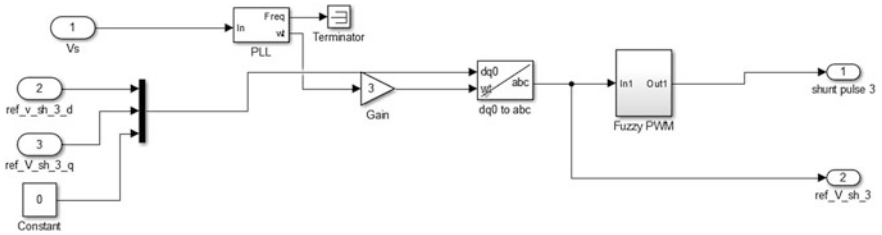


Fig. 8 Shunt control third harmonic

Series converters in the design are having its own series control. Shunt control system, to supply active power to the converter connected in series, injects third harmonic current to the line supplying the system. Grid system, at the same time, at fundamental frequency, absorbs active power and the required amount of reactive current is infused into the grid at fundamental frequency, so that a constant value is kept for the DC voltage of the shunt converter

3 Complete Simulation Model

MATLAB version has been used to simulate the complete model. In the proposed model, DPFC with fuzzy PWM technique has been used. The blocks of the proposed fuzzy PWM are shown in Fig. 9.

The control has two inputs and one output. The fuzzy inputs and output are shown in Fig. 10.

The fuzzy rules are tabulated in Table 1 (Fig. 11).

The proposed system has been tested in the system as shown in Fig. 12. It is a transmission line with two parallel paths. The shunt converter is connected to the second line and the series converter is distributed along the line according to the length of transmission line. The complete model is shown in Fig. 12. The model is tested with the data as shown in Table 2 and is compared with the system having UPFC and with the system having IPQC. The comparative result is tabulated in Table 3.

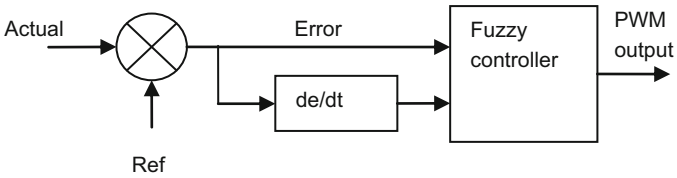


Fig. 9 Block diagram of fuzzy PWM

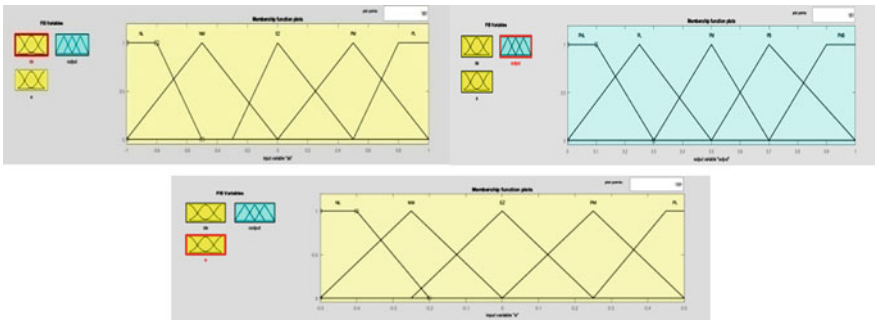


Fig. 10 Fuzzy membership function

Table 1 Fuzzy rules

d*e*	*e*				
	NNL	NNM	Z	PPM	PPL
NNL	B	M	M	M	B
NNM	PB	M	L	M	B
L	VB	M	VL	M	VL
PPM	B	M	L	M	B
PPL	B	M	M	M	B

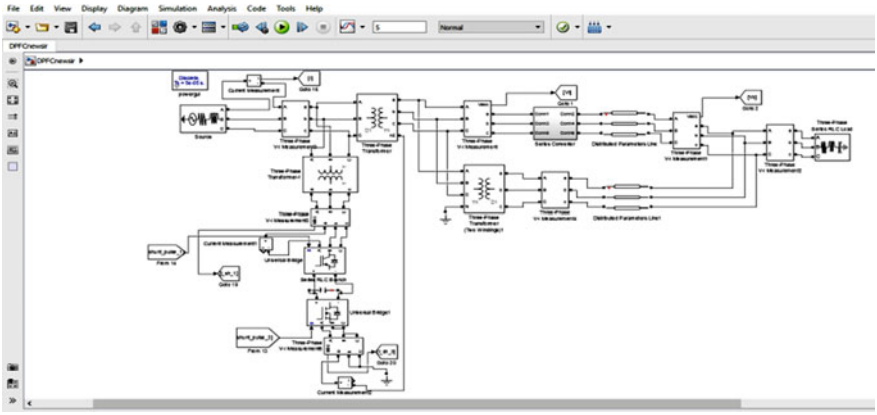


Fig. 11 Two parallel line test network

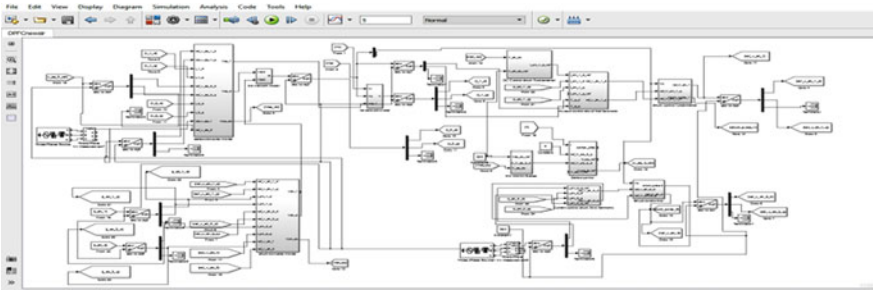


Fig. 12 The complete network

Table 2 Test data

Parameter	Values
Sending end voltage (V)	230
Receiving end voltage (V)	230
Frequency (Hz)	50
V_{sh} DC (V)	20
V_{se} DC (V)	20
$I_{sh,3ref}$ (A)	3
Series capacitor (μF)	1
Shunt capacitor (μF)	1
Length of the transmission line (km)	100
Line resistance (Ω/Km)	0.45
Line inductance (mH/Km)	4.2
X/R ratio	3

Table 3 Comparative result

Bus No.	UPFC [11]				IPQC [11]				Proposed DPFC			
	V	*I*	Real power	Reactive power	*V*	*I*	Real power	Reactive power	*V*	*I*	Real power	Reactive power
1	1.5×10^5	1600	1.5×10^7	3.5×10^8	2.1×10^4	240	7×10^6	1×10^5	1.7×10^5	400	8.7×10^6	7×10^6
2	1.15×10^4	180	2.8×10^6	1.5×10^6	5000	40	2.5×10^5	1.5×10^5	4392	98	6.5×10^5	1.5×10^5
3	2800	28	1.15×10^5	5.5×10^5	1×10^4	100	2×10^5	1×10^5	4300	100	5×10^5	1.8×10^5
4	1.27×10^5	750	0.5×10^7	1.8×10^8	1.1×10^5	100	0.5×10^7	1×10^6	1000	295	3×10^5	2.9×10^5
5	2000	20	6.5×10^4	3×10^5	6000	600	2×10^5	0.5×10^7	300,000	720	3.5×10^5	3.8×10^5

4 Results

The voltage waveform with and without proposed DPFC with fuzzy PWM model is shown in Fig. 13. Similarly, the waveform of the current with and without the proposed DPFC with fuzzy PWM model is in Fig. 14.

Voltage waveform of test results on IEEE-14 bus system with and without the proposed DPFC is shown in Fig. 15 and the real and reactive power with DPFC is shown in Fig. 16.

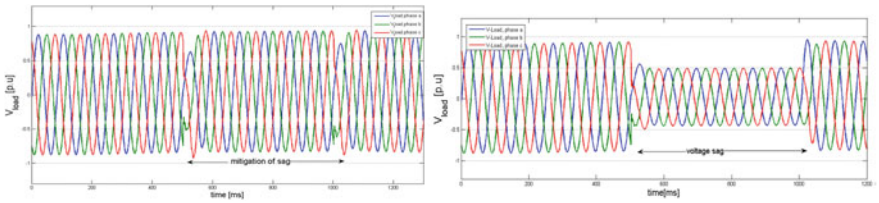


Fig. 13 Voltage waveform

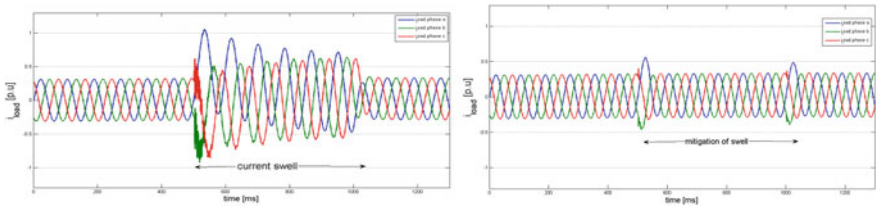


Fig. 14 Current waveform

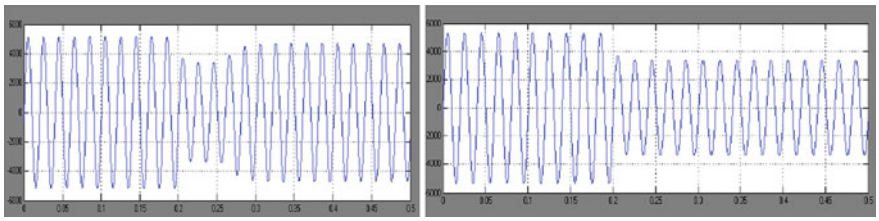


Fig. 15 Voltage waveform

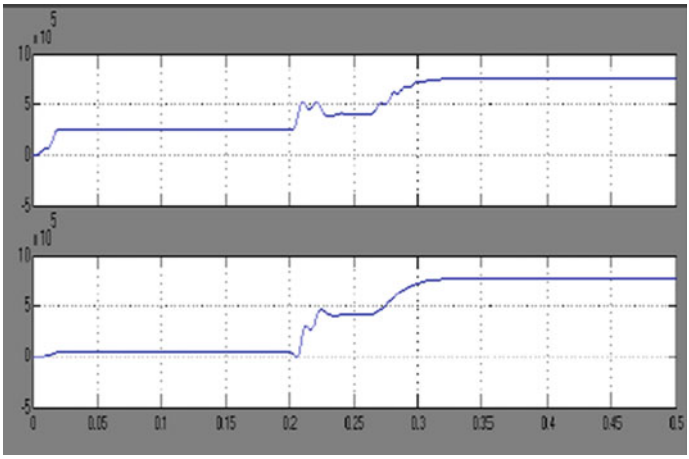


Fig. 16 Power waveform

5 Conclusion

The DPFC is the modified form of UPFC where the DC link is absent. The improvement in power quality of the transmission systems is an important issue for the industry. In this paper, DPFC with fuzzy PWM as an improved device, in mitigating the voltage swell and voltage sag, has been designed in MATLAB/Simulink model. The same model was also tested on IEEE-14 bus system. The observed simulated gives the advantages of using DPFC in improving the power quality mainly to remove the sag and swell. From the simulated results, it is clear that the shunt and series converters in the DPFC at third harmonic frequency have the ability to exchange active power, and the series converters, at fundamental frequency, can infuse manageable active and reactive power. It is shown that the proposed DPFC model gives a good performance in improving the quality of power and also its flow control.

References

1. Faiz, J., Shahgholian, G.H., Torabian, M.: Design and simulation of UPFC for enhancement of power quality in transmission lines. IEEE International Conference on Power System Technology, vol. 24, no. 4 (2010)
2. Yuan, Z., de Haan, S.W.H., Frreira, B., Cevoric, D.: A FACTS device: distributed power flow controller (DPFC). IEEE Trans. Power Electron. **25**(10), 2564–2572 (2010)
3. Moradi, M.: Power Quality Improvement and Mitigation Case Study Using Distributed Power Flow Controller, pp. 464–468. IEEE (2012)

4. Enslin, J.R.: Unified approach to power quality mitigation. In: Proceedings of IEEE International Symposium on Industrial Electronics (ISIE'98), vol. 1 (1998)
5. Singh, B., Al-Haddad, K., Chandra, A.: A review of active filters for power quality improvement. IEEE Trans. Ind. Electron **46**(5), 960–971 (1999)
6. Hannan, M.A., Mohamed, A., Member IEEE.: PSCAD/EMTDC simulation of unified series-shunt compensator for power quality improvement. IEEE Trans. Power Deliv. **20**(2) (2005)
7. Olimpo, A.L., Acha, E.: Modeling and analysis of custom power systems by PSCAD/EMTDC. IEEE Trans. Power Deliv. **17**(1), 266–272 (2002)
8. Pohjanheimo, P., Lakervi, E.: Steady state modeling of custom power components in power distribution networks. In: Proceedings of IEEE Power Engineering Society Winter Meeting, vol. 4, pp. 2949–2954 (2000)
9. Yuan, Z.H., de Haan, S.W.H., Frreira, B., Cevoric, D.: A FACTS device: distributed power flow controller (DPFC). IEEE Trans. Power Electron. **25**(10) (2010)
10. Yuan, Z.H., de Haan, S.W.H., Frreira, B.: DPFC control during shunt converter failure. IEEE Trans. Power Electron (2009)
11. Venkatesh, R., Rekha, M., Sundar, G.: Deciding optimal location for placing FACTS devices [UPFC, IPQC, DPFC] using bang bang control technique. Int. J. Innovative Res. Dev. **3**(1), 132–141 (2014)

New Sliding Mode Control of a Five-Phase Permanent Magnet Synchronous Motor Drive in Wide Speed Range

Anissa Hosseyni, Ramzi Trabelsi, Med Faouzi Mimouni, Atif Iqbal and Padmanaban Sanjeevikumar

Abstract This paper proposes a novel sliding mode control (SMC) for a five-phase permanent magnet synchronous motor (PMSM). This control strategy exhibits stability control system and fast dynamic response. The stability of the proposed control strategy is proved by the Lyapunov theory. Simulated results are reported to prove the efficacy of the proposed strategy. Moreover, the depicted set of numerical simulation results always shows a close conformity with the developed theoretical background.

Keywords Five-phase machine · Permanent magnet synchronous motor Sliding mode controller · Sliding mode observer · Speed controller Current controller

A. Hosseyni · M.F. Mimouni
Monastir National Engineering School, Ibn Eljazzar City, 5019 Monastir, Tunisia
e-mail: hosseyni.anissa@yahoo.com

M.F. Mimouni
e-mail: mfaouzi.mimouni@enim.rnu.tn

R. Trabelsi
High Institute of Applied Sciences and Technology, Ibn Khaldoun City 4003, Sousse, Tunisia
e-mail: trabelsi.ramzi@yahoo.fr

A. Hosseyni · R. Trabelsi · M.F. Mimouni
Research Unit: Systèmes Industriels et des Energies renouvelables, Rue Ibn Eljazzar, 5019 Monastir, Tunisia

A. Iqbal
Department of Electrical Engineering, Qatar University, Doha, Qatar
e-mail: atif.iqbal@qu.edu.qa

P. Sanjeevikumar (✉)
Department of Electrical and Electronics Engineering, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_21

1 Introduction

Multiphase machines have experienced a surge in their research due to their distinct advantages over their three-phase drive counterparts. Indeed, by increasing the number of phases, the current per phase is reduced without increasing the voltage per phase [1]. Multiphase motor drives reduce the torque pulsations. The high phase order offers greater fault tolerant [2]. So that, multiphase motors are used in some critical domains requiring high reliability such as electric aircraft, electric traction and ship propulsion. Recently, PMSM has received an increasing interest due to their attractive features such as high power density and high efficiency. Many nonlinear state feedback methods, and in particular sliding mode control, have become an attractive alternative to the field oriented control (FOC) strategy to achieve high performance of three phase motor drives [3, 4]. This technique has been widely applied for three-phase motor drives proving numerous attractive features compared with the conventional FOC but it is not the case for multiphase motor drives. SMC has received an increasing interest to their attractive features such as:

(1) Its robustness to uncertainties and disturbances.
(2) This control strategy offers a stability control system and fast dynamic response [3].

In this paper, a novel observer is proposed to attain a new sliding mode control of a five-phase PMSM. The rest of this paper is organized as follows: Sect. 2 describes the five-phase PMSM model, Sects. 3 and 4 deal with sliding mode control and simulation results, respectively. Finally, some conclusions are presented in the last section.

2 Model of a Five-Phase Permanent Magnet Synchronous Motor (PMSM)

The mathematical model of five-phase PMSM is presented in a rotating $(d_p - q_p)$ and $(d_s - q_s)$ frame as follows [1]:

$$\begin{cases} \frac{\mathrm{d}I_{dp}}{\mathrm{d}t} = -\frac{R_s}{L_p} I_{dp} + \omega_e I_{qp} + \frac{1}{L_p} v_{dp} \\ \frac{\mathrm{d}I_{qp}}{\mathrm{d}t} = -\frac{R_s}{L_p} I_{qp} - \omega_e I_{dp} - \frac{\sqrt{\frac{5}{2}}\Phi_f \omega_e}{L_p} + \frac{1}{L_p} v_{qp} \\ \frac{\mathrm{d}I_{ds}}{\mathrm{d}t} = -\frac{R_s}{L_s} I_{ds} + 3\omega_e I_{qs} + \frac{1}{L_s} v_{ds} \\ \frac{\mathrm{d}I_{qs}}{\mathrm{d}t} = -\frac{R_s}{L_s} I_{qs} - 3\omega_e I_{ds} + \frac{1}{L_s} v_{qs} \\ \frac{\mathrm{d}\Omega}{\mathrm{d}t} = \frac{\sqrt{\frac{5}{2}} P \Phi_f}{J} I_{qp} - \frac{1}{J} T_L - \frac{f}{J} \Omega \end{cases} \Rightarrow \begin{cases} \frac{\mathrm{d}I_{dp}}{\mathrm{d}t} = f_{dp} + \frac{1}{L_p} v_{dp} \\ \frac{\mathrm{d}I_{qp}}{\mathrm{d}t} = f_{qp} + \frac{1}{L_p} v_{qp} \\ \frac{\mathrm{d}I_{ds}}{\mathrm{d}t} = f_{ds} + \frac{1}{L_s} v_{ds} \\ \frac{\mathrm{d}I_{qs}}{\mathrm{d}t} = f_{qs} + \frac{1}{L_s} v_{qs} \\ \frac{\mathrm{d}\Omega}{\mathrm{d}t} = f_{\Omega} \end{cases}, \quad (1)$$

where

$$\begin{cases} f_{dp} = a_1 I_{dp} + \omega_e I_{qp} \\ f_{qp} = a_1 I_{qp} - \omega_e I_{dp} + a_2 \omega_e \\ f_{ds} = a_3 I_{ds} + 3\omega_e I_{qs} \\ f_{qs} = a_3 I_{qs} - 3\omega_e I_{ds} \\ f_{\Omega} = a_4 I_{qp} + a_5 T_L + a_6 \Omega \end{cases} \tag{2}$$

$$a_1 = -\frac{R_s}{L_p}; \quad a_2 = -\frac{\sqrt{\frac{5}{2}}\Phi_f}{L_p}; \quad a_3 = -\frac{R_s}{L_s};$$

$$a_4 = \frac{\sqrt{\frac{5}{2}}P\Phi_f}{J}; \quad a_5 = -\frac{1}{J}; \quad a_6 = -\frac{f}{J}$$

3 Sliding Mode Control

In this section, a novel SMC of five-phase PMSM is introduced. Two steps are necessary to synthesis the SMC: First, the sliding surface is designed and then the control law is developed. So that, five sliding surfaces with integral actions are considered as follows:

$$s_{\Omega} = e_{\Omega} + q_1 \int_0^t e_{\Omega}(\tau)\mathrm{d}t \tag{3}$$

$$\begin{cases} s_{dp} = e_{dp} + q_2 \int_0^t e_{dp}(\tau)\mathrm{d}t \\ s_{qp} = e_{qp} + q_3 \int_0^t e_{qp}(\tau)\mathrm{d}t \\ s_{ds} = e_{ds} + q_2 \int_0^t e_{ds}(\tau)\mathrm{d}t \\ s_{qs} = e_{qs} + q_5 \int_0^t e_{qs}(\tau)\mathrm{d}t \end{cases}, \tag{4}$$

where q_i (i = 1, 2, 3, 4, 5) are positive constants and e_{Ω} is the speed error, and e_{dp}, e_{qp}, e_{ds}, e_{qs}, the show ($d_p - q_p$) and ($d_s - q_s$) stator currents errors components, respectively, are given by:

$$\begin{cases} e_{\Omega} = \Omega - \Omega^{*} \\ e_{dp} = I_{dp} - I_{dp}^{*} \\ e_{qp} = I_{qp} - I_{qp}^{*} \\ e_{ds} = I_{ds} - I_{ds}^{*} \\ e_{qs} = I_{qs} - I_{qs}^{*} \end{cases} \tag{5}$$

The application of SMC to achieve the control of five-phase PMSM proceeds in two steps: the synthesis of speed controller and then the synthesis of currents controllers.

Speed Controller: The speed controller is designed to achieve the convergence of the speed error to zero by constraining the convergence of the system to the sliding surface $(s_{\Omega} = 0)$

$$s_{\Omega} = 0 \Rightarrow \dot{s}_{\Omega} = \dot{e}_{\Omega} + q_1 e_{\Omega} = 0 \tag{6}$$

The I_{qp} stator current component reference is given by:

$$I_{qpeq}^{*} = \left(\dot{\Omega}^{*} - a_5 T_L - a_6 \Omega - q_1 e_{\Omega}\right)/a_4 \tag{7}$$

In order to achieve performance regardless of the uncertainties on the dynamic of the system, one should add the discontinuous term called 'reaching controller' which is given by [4]:

$$I_{qpn}^{*} = -k_1 \mathrm{sgn}(s_{\Omega}), \tag{8}$$

where k_1 is a positive constant.

The d_p, d_s and q_s are axis current component references that are maintained to zero [1].

4 Current Controller

The current controllers are designed such a way to bring the system to follow the trajectory defined by the sliding surfaces $\left(s_{dp} = 0; s_{qp} = 0; s_{ds} = 0; s_{qs} = 0\right)$

$$\begin{cases} s_{dp} = 0 \\ s_{qp} = 0 \\ s_{ds} = 0 \\ s_{qs} = 0 \end{cases} \Rightarrow \begin{cases} \dot{s}_{dp} = 0 \\ \dot{s}_{qp} = 0 \\ \dot{s}_{ds} = 0 \\ \dot{s}_{qs} = 0 \end{cases} \tag{9}$$

The stator voltage references can be given by:

$$\begin{cases} v_{dpeq} = L_p\left(\dot{I}_{dp}^{*} - f_{dp} - q_2 e_{dp}\right) - k_2 \mathrm{sgn}(s_{dp}) \\ v_{qpeq} = L_p\left(\dot{I}_{qp}^{*} - f_{qp} - q_3 e_{qp} - a_4 e_{qp}\right) - k_3 \mathrm{sgn}(s_{qp}) \\ v_{dseq} = L_s\left(\dot{I}_{ds}^{*} - f_{ds} - q_4 e_{ds}\right) - k_4 \mathrm{sgn}(s_{ds}) \\ v_{qseq} = L_s\left(\dot{I}_{qs}^{*} - f_{qs} - q_5 e_{qs}\right) - k_5 \mathrm{sgn}(s_{qs}) \end{cases}, \tag{10}$$

where k_i (i = 2, 3, 4, 5) are positive constants. The stability of the proposed strategy is proved by the Lyapunov theory.

Let us consider the Lyapunov function

$$V_c = \frac{1}{2}\left(e_{\Omega}^2 + e_{dp}^2 + e_{qp}^2 + e_{ds}^2 + e_{qs}^2\right) \tag{11}$$

To ensure the stability of V_c, q_1, q_2, q_3, q_4, q_5 should be chosen in such a way that:

$$\begin{cases} q_1 \ggg |k_{\Omega}\mathrm{sgn}(s_{\Omega})|; q_2 \ggg \left|k_{dp}\mathrm{sgn}(s_{dp})\right|; q_3 \ggg \left|k_{qp}\mathrm{sgn}(s_{qp})\right|; \\ q_4 \ggg |k_{ds}\mathrm{sgn}(s_{ds})|; q_5 \ggg \left|k_{qs}\mathrm{sgn}(s_{qs})\right| \end{cases} \tag{12}$$

The proposed sliding mode control based on the sliding mode observer. Where I_{dp}, I_{qp}, I_{ds} and I_{qs} are the currents in the rotating frame and ω_e is the rotor speed. '*' is used to indicate that the variables are reference values. The real and the reference speed are processed in the speed sliding mode controller to determine the reference I_{qp} current to obtain the reference I_{qp} current. The commanded I_{dp}, I_{ds} and I_{qs} currents components are fixed to zero. Then, the reference and actual currents components in (d_p, q_p, d_s and q_s) rotating frame is processed in the current sliding mode controllers to obtain as outputs the equivalent commanded voltages to that should be added the reaching term to obtain the total reference voltages given by [10].

5 Numerical Simulation Test Results and Discussion

To check the validity of the proposed sliding mode control of a five-phase PMSM, the feedback control has been modelled in MATLAB/Simulink Computer program. To highlight the performance of the proposed control, the sliding mode control of five-phase PMSM has been tested in two extreme situations: speed inversion under torque application and running at low speed as shown in Figs. 1 and 2, respectively.

Figure 1a shows the reference and real speed. Indeed, the reference speed is in pulse form which is raised from zero speed to rated speed of 157 rad/s and then it is reversed to reach −157 rpm at t = 1 s. The proposed sliding mode control is seen to

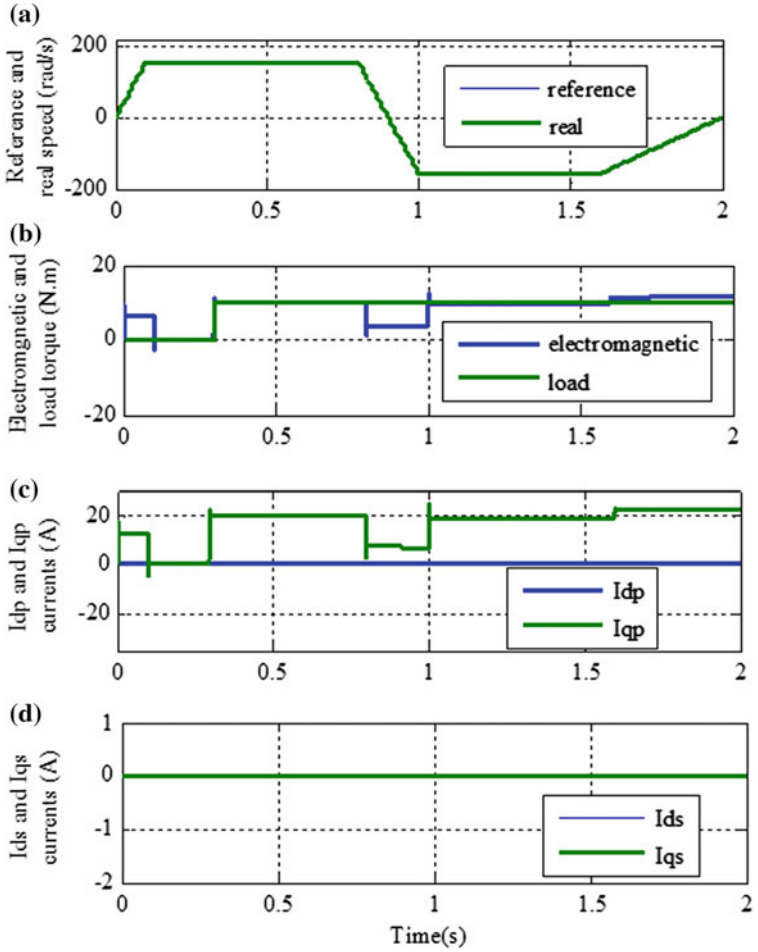


Fig. 1 Sensitivity of the five-phase PMSM performances at speed reverse: **a** reference and real rotor speed, **b** electromagnetic and load torque, **c** I_{dp} and I_{qp} currents components, **d** real I_x and I_y currents components

offer good performance in terms of speed tracking. The load rejection capability of the drive is also proved in the simulation results. Figure 1b illustrates the load and electromagnetic torque of the five-phase motor. The electromagnetic torque varies with the stator current component I_{qp}. The proposed controller shows also good dynamic tracking for $(d_p - q_p)$ and $(d_s - q_s)$ currents components as presented in Fig. 1c, d. Figure 2a represents the reference and the real speed at low speed. The reference speed is a step fixed at 5 rad//s. It can be seen that the proposed controller shows good performance in terms of settling time. Indeed, the speed and perfectly

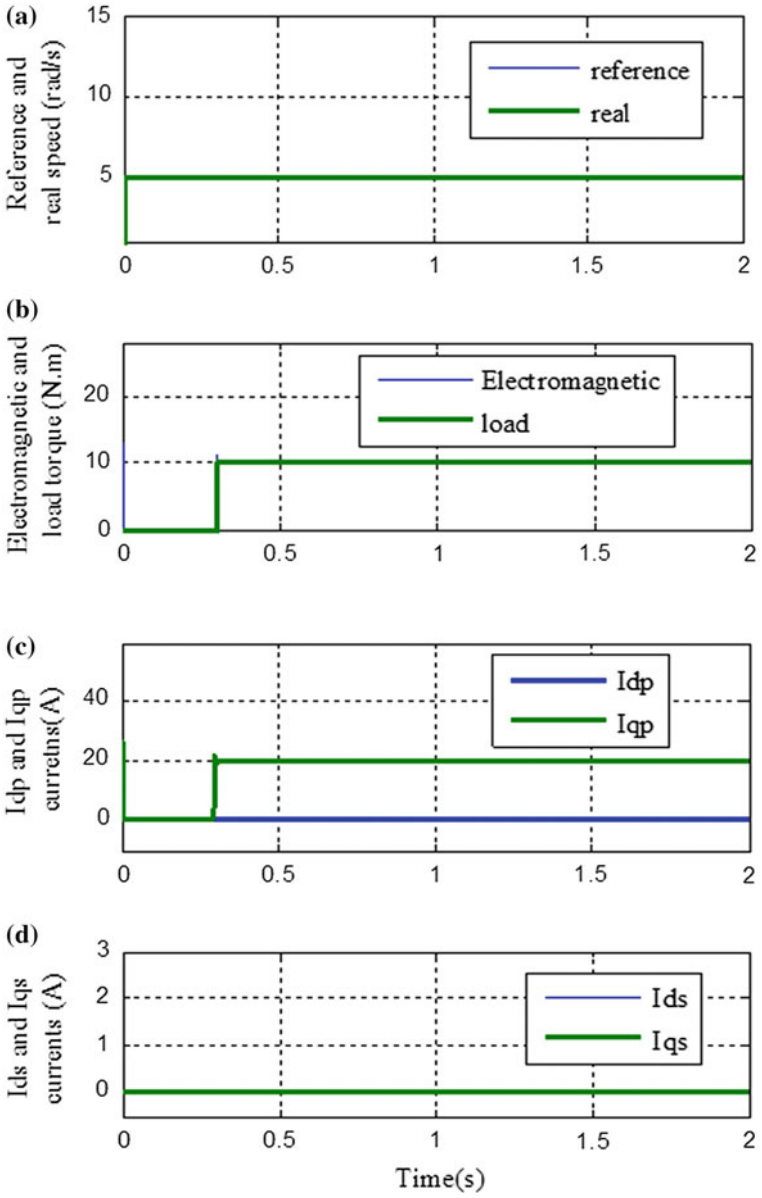


Fig. 2 Sensitivity of the five-phase PMSM performances at low speed: **a** reference and real rotor speed, **b** electromagnetic and load torque, **c** I_{dp} and I_{qp} currents components, **d** I_x and I_y currents components

to its reference value. Figure 2b illustrates the load and electromagnetic torque and Fig. 2c, d show $(d_p - q_p)$ and $(d_s - q_s)$ currents components, respectively. Indeed, the proposed sliding mode control shows good performance at low speed.

6 Conclusions

This paper presented control of a five-phase permanent magnet synchronous motor (PMSM) based on sliding mode control (SMC). A complete model of the AC drive system is numerically developed using simulation software and tested for its dynamics, load rejection and reversal behaviours. Developed sliding control algorithm satisfies the Lyapunov criterion under the stability requirement for transient and dynamic behaviours. Simulation results show satisfactory results of the proposed SMC for different cases such as load disturbance and low speed.

References

1. Hosseyni, A., Trabelsi, R., Mimouni, M.F., Iqbal, A., Alammari, R.: Sensorless sliding mode observer for a five-phase permanent magnet synchronous motor drive. ISA Trans. Elsevier Pub. **58**, 462–473 (2015)
2. Nguyen, N.K., Meinguet, F., Semail, E., Kestelyn, X.: Fault-tolerant operation of an open-end winding five-phase PMSM drive with short-circuit inverter. IEEE Trans. Power Electron **63**(1), 595–605 (2016)
3. Saghafinia, A., Ping, H.W., Uddin, M.N., Gaeid, K.S.: Adaptive fuzzy sliding-mode control into chattering-free IM drive. IEEE Trans. Ind. Appl. **51**(1), 692–701 (2015)
4. Mekki, H., Benzineb, O., Boukhetala, D., Tadjine, M., Benbouzid, M.: Sliding mode based fault detection, reconstruction and fault tolerant control scheme for motor systems. ISA Trans. Elsevier Pub. **57**, 341–351 (2015)

Novel Sensorless Sliding Mode Observer of a Five-Phase Permanent Magnet Synchronous Motor Drive in Wide Speed Range

Anissa Hosseyni, Ramzi Trabelsi, Med Faouzi Mimouni, Atif Iqbal and Padmanaban Sanjeevikumar

Abstract This paper proposes a novel sliding mode observer (SMO) to achieve the sliding mode observer (SMC) for a five-phase permanent magnet synchronous motor (PMSM) in wide speed range. The structure of the proposed SMO is described and its stability is proven in the context of Lyapunov theory. Simulated results are provided to prove the effectiveness of the proposed strategy.

Keywords Five-phase machine · Permanent magnet synchronous motor Sliding mode controller · Sliding mode observer · Speed controller Lyapunov theory

A. Hosseyni · M.F. Mimouni
Monastir National Engineering School, Ibn Eljazzar City, 5019 Monastir, Tunisia
e-mail: hosseyni.anissa@yahoo.com

M.F. Mimouni
e-mail: mfaouzi.mimouni@enim.rnu.tn

R. Trabelsi
High Institute of Applied Sciences and Technology, Ibn Khaldoun City, 4003 Sousse, Tunisia
e-mail: trabelsi.ramzi@yahoo.fr

A. Hosseyni · R. Trabelsi · M.F. Mimouni
Research Unit: Systèmes Industriels et des Energies renouvelables, Rue Ibn Eljazzar, 5019 Monastir, Tunisia

A. Iqbal
Department of Electrical Engineering, Qatar University, Doha, Qatar
e-mail: atif.iqbal@qu.edu.qa

P. Sanjeevikumar (✉)
Department of Electrical and Electronics Engineering, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_22

1 Introduction

During the past years, multiphase drives have gained interest for their advantages. Their features include reduction of torque pulsations and reducing stator phase current [1–3]. The high phase order offers greater fault tolerance. Many nonlinear state feedback methods, and in particular, sliding mode control, have become an attractive alternative to the field-oriented control (FOC) strategy to achieve high performance of three-phase motor drives. The synthesis of SMC control requires the rotor speed and rotor position information, so that the position and speed sensors can be installed on the shaft. Unfortunately, these sensors are costly and touch to temperature and vibration. Nevertheless, many researchers' activities were dedicated to sensorless control techniques and several methods were proposed. One of the known classes of nonlinear observers is the sliding mode observer which posses many special characteristics, namely order reduction control, simple algorithm and disturbance rejection. Numerous researches have been focused on the sensorless control strategies for three-phase PMSM [4–6] but only few researches have been focused on SMO for multiphase motor drives. This paper proposes the synthesis of sliding mode observer to estimate the rotor position and speed for a five phase in closed loop. The rest of this paper is organized as follows. The model of machine is presented in Sect. 2. The design and the stability of the proposed SMO are developed in Sect. 3, respectively. Some simulation results are shown in Sect. 5 and Sect. 6 deals with conclusions.

2 Model of a Five-Phase PMSM

The stator flux of five-phase PMSM in (d_p, q_p, d_s, q_s) is given by:

$$\begin{cases} \dfrac{\mathrm{d}\lambda_{dp}}{\mathrm{d}t} = -R_s I_{dp} + \omega_e \lambda_{qp} + v_{dp} \\ \dfrac{\mathrm{d}\lambda_{qp}}{\mathrm{d}t} = -R_s I_{qp} - \omega_e \lambda_{dp} + v_{qp} \\ \dfrac{\mathrm{d}\lambda_{ds}}{\mathrm{d}t} = -R_s I_{ds} + \omega_e \lambda_{qs} + v_{ds} \\ \dfrac{\mathrm{d}\lambda_{qs}}{\mathrm{d}t} = -R_s I_{qp} - \omega_e \lambda_{ds} + v_{qs} \\ T_{em} = \sqrt{\frac{5}{2}} P \phi_f I_{qp} \end{cases} \tag{1}$$

$$\begin{cases} \lambda_{dp} = L_p I_{dp} + \sqrt{\frac{5}{2}} \Phi_f \\ \lambda_{qp} = L_p I_{qp} \\ \lambda_{ds} = L_s I_{ds} \\ \lambda_{qs} = L_s I_{qs} \end{cases} \tag{2}$$

$\lambda = (\ \lambda_{dp} \quad \lambda_{qp} \quad \lambda_{ds} \quad \lambda_{qs}\ )^{\mathrm{T}}$: stator flux in (d_p, q_p, d_s, q_s).

By transforming (2) in $(\alpha_p, \beta_p, \alpha_s, \beta_s)$, one obtains:

$$\begin{cases} \lambda_{\alpha p} = L_p I_{\alpha p} + \lambda_{\alpha f} \\ \lambda_{\beta p} = L_p I_{\beta p} + \lambda_{\beta f} \\ \lambda_{\alpha s} = L_s I_{\alpha s} \\ \lambda_{\beta s} = L_s I_{\beta s} \end{cases}, \tag{3}$$

where

$$\begin{cases} \lambda_{\alpha f} = \sqrt{\frac{5}{2}} \Phi_f \cos(\theta_e) \\ \lambda_{\beta f} = \sqrt{\frac{5}{2}} \Phi_f \sin(\theta_e) \end{cases} \tag{4}$$

Using (4), the electrical rotor position can be found:

$$\theta_e = \tan^{-1}\left(\frac{\lambda_{\beta f}}{\lambda_{\alpha f}}\right) \tag{5}$$

3 Design of SMO

In this section, a new SMO for speed and rotor position estimation of five-phase PMSM is developed in order to estimate the rotor speed at wide range. Based on (1) and (2), a sliding mode observer can be designed from the SMO developed in [6] and applied to three-phase PMSM as:

$$\begin{aligned} \frac{\mathrm{d}\hat{\lambda}}{\mathrm{d}t} &= D\hat{i} + v + K\tilde{i} + K_{\mathrm{SMO}}\mathrm{sgn}(\tilde{i}), \\ \hat{i} &= L^{-1}\hat{\lambda} - \frac{\mathrm{sqrt}\left(\frac{5}{2}\right)\Phi_f}{L_p}\begin{pmatrix} \cos\hat{\theta}_e \\ \sin\hat{\theta}_e \end{pmatrix}, \end{aligned} \tag{6}$$

where

$$\hat{i} = \begin{pmatrix} i_{\alpha p} & i_{\beta p} & i_{\alpha s} & i_{\beta s} \end{pmatrix}^{\mathrm{T}} \quad \text{and} \quad \hat{\lambda} = \begin{pmatrix} \hat{\lambda}_{\alpha p} & \hat{\lambda}_{\beta p} & \hat{\lambda}_{\alpha s} & \hat{\lambda}_{\beta s} \end{pmatrix}^{\mathrm{T}},$$

where '^' and '$\sim$' indicate the corresponding parameters which are the estimated value and error value, respectively. K and K_{SMO} are the matrix gains.

Where

$$K = \begin{pmatrix} k_{1o} & 0 & 0 & 0 \\ 0 & k_{2o} & 0 & 0 \\ 0 & 0 & k_{3o} & 0 \\ 0 & 0 & 0 & k_{4o} \end{pmatrix} \quad K_{\mathrm{SMO}} = \begin{pmatrix} k_{\mathrm{SMO1}} & 0 & 0 & 0 \\ 0 & k_{\mathrm{SMO2}} & 0 & 0 \\ 0 & 0 & k_{\mathrm{SMO3}} & 0 \\ 0 & 0 & 0 & k_{\mathrm{SMO4}} \end{pmatrix}$$

$$L = \begin{pmatrix} L_p & 0 & 0 & 0 \\ 0 & L_p & 0 & 0 \\ 0 & 0 & L_s & 0 \\ 0 & 0 & 0 & L_s \end{pmatrix} \quad D = \begin{pmatrix} -R_s & 0 & 0 & 0 \\ 0 & -R_s & 0 & 0 \\ 0 & 0 & -R_s & 0 \\ 0 & 0 & 0 & -R_s \end{pmatrix}$$

The estimation rotor position is given by:

$$\hat{\theta}_e = \tan^{-1}\left(\frac{\hat{\lambda}_{\beta f}}{\hat{\lambda}_{\alpha f}}\right), \tag{7}$$

where

$$\begin{cases} \hat{\lambda}_{\alpha f} = \hat{\lambda}_{\alpha} - L_p i_{\alpha} \\ \hat{\lambda}_{\beta f} = \hat{\lambda}_{\beta} - L_p i_{\beta}. \end{cases} \tag{8}$$

4 Stability Analysis

To prove the stability of the proposed of the sliding mode observer, let us define the Lyapunov function:

$$V = \left(\tilde{\lambda}^{\mathrm{T}} L^{-1} \tilde{\lambda}\right), \tag{9}$$

where

$$\frac{\mathrm{d}\tilde{\lambda}}{\mathrm{d}t} = D\tilde{i} - K\tilde{i} - K_{\mathrm{SMO}}\mathrm{sgn}\left(\tilde{i}\right) \tag{10}$$

The derivative $\dot{V}$ is given by:

$$\dot{V} = \tilde{i}^{\mathrm{T}}(D - K)\tilde{i} - K_{\mathrm{SMO}}\tilde{i}\,\mathrm{sgn}\left(\tilde{i}\right) \tag{11}$$

To guarantee stability of V, $\dot{V}$ should be negative, so that from (11):

$$\tilde{i}^{\mathrm{T}}(D-K)\tilde{i}<0 \tag{12}$$

$$K_{\mathrm{SMO}}\tilde{i}\ \mathrm{sgn}(\tilde{i})>0 \tag{13}$$

From (12), the gains $k_{\mathrm{SMO1}}, k_{\mathrm{SMO2}}, k_{\mathrm{SMO3}}, k_{\mathrm{SMO4}}$ in the matrix K_{SMO} should be positive. Equation (13) requires that the eigenvalues of $(D-K)$ must be in the left half plane. So, the gains $k_{1o}, k_{2o}, k_{3o}, k_{4o}$ in the matrix K are selected using the pole placement method.

Speed estimation: The rotor speed can be calculated by differentiating (7) which gives [6]:

$$\hat{\omega}_e=\frac{\hat{\lambda}_{\alpha f}(k-1)\hat{\lambda}_{\beta f}(k)-\hat{\lambda}_{\beta f}(k-1)\lambda_{\alpha f}(k)}{T_s\left(\lambda_{\alpha f}(k)^2+\lambda_{\beta f}(k)^2\right)}, \tag{14}$$

where k and $k-1$ are two consecutive sampling instants and T_s is the sampling period.

5 Numerical Simulation Results and Discussion

A MATLAB/Simulink environment was used to simulate the feedback control based on SMO. To highlight the performance of the proposed observer, developed in the previous sections, the proposed observer has been tested in two different situations. The first scenario was devoted to speed inversion. The second situation analyzes the performance of feedback sensorless control when the motor is running at very low speed. The response of the motor is illustrated under two different profiles. In the first case, the performance of five-phase PMSM to change (Fig. 1).

The estimation error of speed is shown in Fig. 2c proving the high performance of SMO even at very low speed. The rotor position and its estimation error are illustrated in Fig. 2c, d, respectively.

6 Conclusions

In this paper, a SMO for estimation of rotor speed and position of five-phase PMSM has been developed. A complete model of the AC drive system is numerically developed using simulation software and test for its transient and dynamic behaviours. It is verified from the investigation that the proposed control technique offers good response to various perturbation conditions. Moreover, the proposed sliding mode observer improves the accuracy of speed estimation at very low-speed

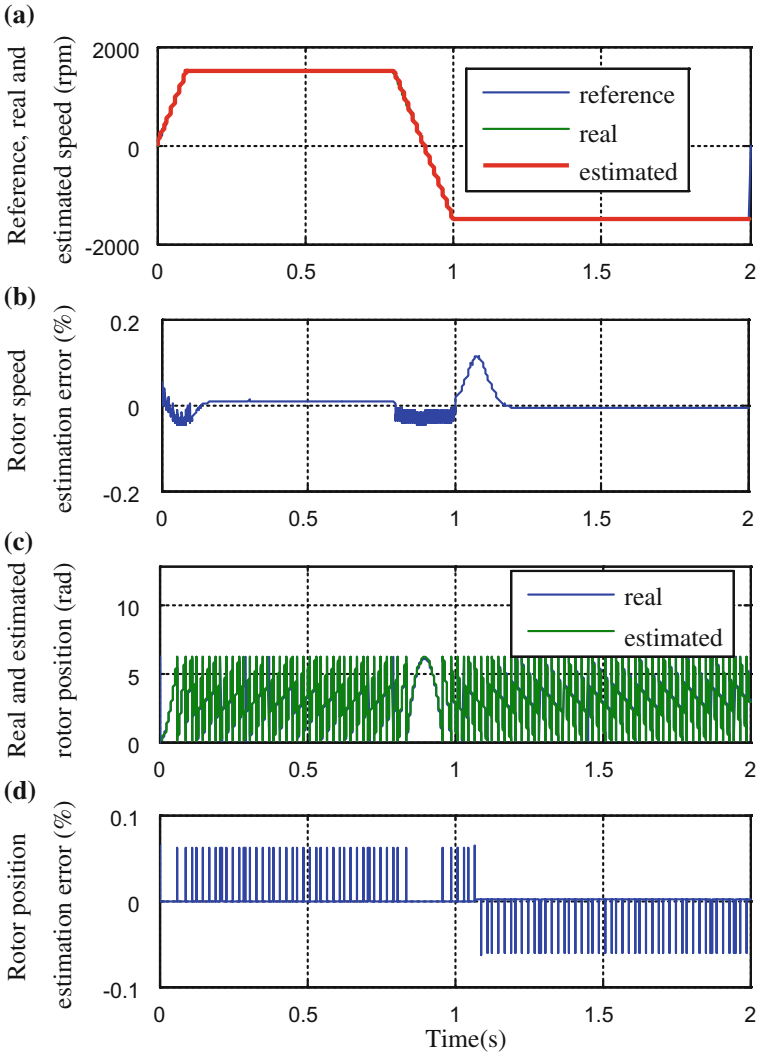


Fig. 1 Sensitivity of five-phase PMSM performances at speed reverse: **a** real, reference and estimated speed, **b** estimation error of rotor speed, **c** estimated and real position, **d** estimation error of position

variations without adoption of speed sensors. Developed sliding control algorithm satisfies the Lyapunov criterion under the stability requirement for transient and dynamic behaviours. The proposed control scheme is applicable to AC drives that need to be adapted to sensitivity, speed control in AC traction, electric vehicles and high-power applications.

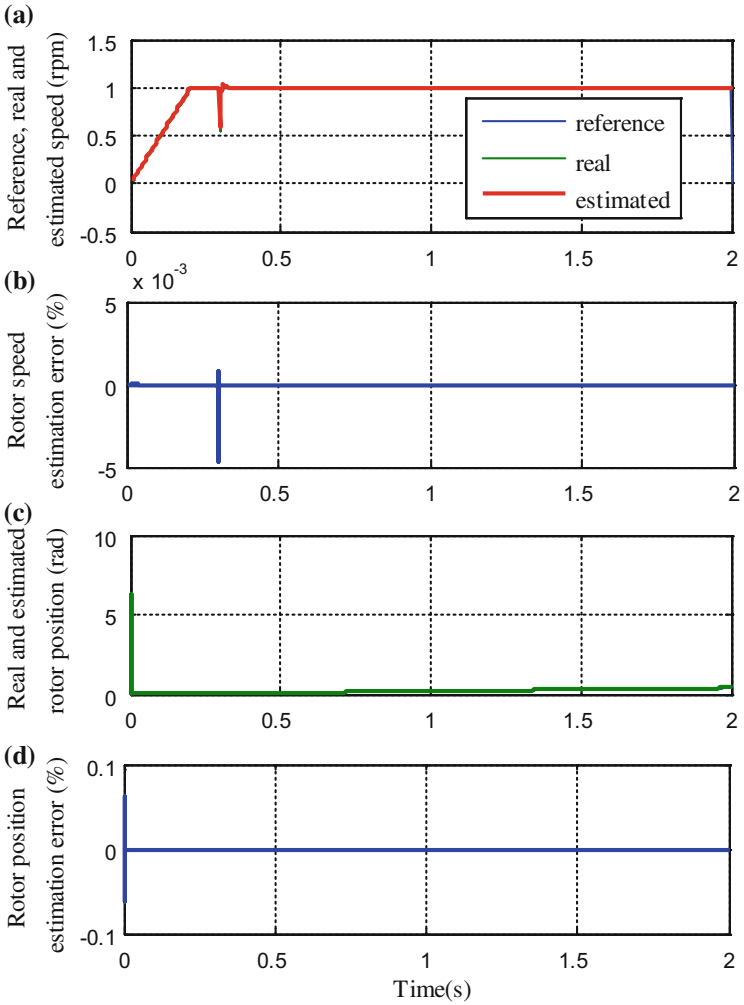


Fig. 2 Sensitivity of five-phase PMSM performances at speed reverse: **a** real, reference and estimated speed, **b** estimation error of rotor speed, **c** estimated and real position, **d** estimation error of position

References

1. Anissa, H., Ramzi, T., Mohamed, F.M., Atif, I., Rashid, A.: Sensorless sliding mode observer for a five-phase permanent magnet synchronous motor drive. ISA Trans. **58**, 462–473 (2015)
2. Nguyen, N.K., Meinguet, F., Semail, E., Kestelyn, X.: Fault-tolerant operation of an open-end winding five-phase PMSM drive with short-circuit inverter. IEEE Trans. Power Electron **63**(1), 595–605 (2016)

3. Guzman, H., Duran, M.J., Barrero, F., Zarri, L., Bogado, B., Prieto, I.G., Arahal, M.R.: Comparative study of predictive and resonant controllers in fault-tolerant five phase induction motor drives. IEEE Trans. Ind. Electron **63**(1), 606–6017 (2016)
4. Xiaoguang, Z., Zhengxi, L.: Sliding-mode observer-based mechanical parameter estimation for permanent magnet synchronous motor. IEEE Trans. Power Electron **31**(8), 5732–5745 (2016)
5. Zhaowei, Q., Tingna, S., Yindong, W., Yan, Y., Changliang, X., Xiangning, H.: New sliding mode observer for position sensorless control of permanent-magnet synchronous motor. IEEE Trans. Ind. Electron **60**(12), 710–719 (2013)
6. Glibert, F., Faz, R.: Direct torque control of an IPM synchronous motor drive at very low speed using a sliding mode stator flux observer. IEEE Trans. Power Electron **25**(4), 933–942 (2010)

Thermal Analysis of Inverter-Fed Induction Motor

Sunam Saha and Mohammed Nasir Ansari

Abstract Reducing the size and cost and increasing the energy efficiency and optimal loading of the motor have a direct impact on the temperature rise of the motor. Motor needs to be operated such that its temperature rise is within the prescribed safe limit. Therefore, easy and precise temperature rise determination of motor becomes critical. Thermal models of motor are widely used for temperature determination. In this paper, a modified thermal model is proposed using which the temperature rise of induction motor fed from raw supply and inverter-fed supply is determined. The parameters of the thermal model are also determined.

Keywords Thermal analysis · Induction motor · Inverter · Lumped parameter Temperature rise

Nomenclature

R_{csylf}	Radial conduction thermal resistance of the stator yoke lower half part
R_{csyuh}	Radial conduction thermal resistance of the stator yoke upper half part
R_{vstag}	Convection thermal resistance between stator teeth and air gap
R_{vrag}	Convection thermal resistance between rotor and air gap
R_{crst}	Radial conduction thermal resistance of the stator teeth
R_{csf}	Axial conduction thermal resistance of the shaft
R_{vswia}	Convection thermal resistance between stator winding, external connection and inner air
R_{cswec}	Convection thermal resistance between stator winding, external connection and external case
R_{viaec}	Convection thermal resistance between internal air and end caps
R_{cscss}	Conduction thermal resistance between stator copper and stator slot

S. Saha (✉) · M.N. Ansari
Department of Electrical and Electronics, Sikkim Manipal Institute of Technology, Majhitar 737136, Sikkim, India
e-mail: sunamsaha.ee@gmail.com

M.N. Ansari
e-mail: nasirans@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_23

R_{vcan} Natural convection thermal resistance between external case and ambient
P_{rcu} Rotor copper loss
P_{ir} Stator iron loss
P_{scu} Stator copper loss
R_{sc} Resistance in the stator conductor
R_{sr} Resistance between stator and rotor
R_{sy} Resistance between stator and yolk
R_{rc} Resistance in the rotor conductor
R_{re} Resistance between rotor and external case
P_{scu} Stator copper loss
P_{rcu} Rotor copper loss
P_{ir} Stator iron loss
θ_s Temperature at outer stator surface
θ_r Temperature at outer rotor surface
ΔP_i Losses in the ith node (some are zero)
θ_i Temperature rise on the ith node
$\propto_{ik}$ Thermal conductivities between ith and the kth node (some are zero)

1 Introduction

Rotating electric machines are mainly used for energy transfer, from electrical energy to mechanical energy or vice versa. During this energy transfer some losses occur, which as a result generates heat. Due to this heat generation, temperature rise takes place in various parts of the motor and if the thermal limit is crossed, it may give rise to many undesirable effects [1]. Moreover, modern electric machines are designed using new materials and improved manufacturing techniques to make the size smaller and have higher loading capability. They are being operated much nearer to the point of overload [2]. Therefore, for the motor to have a good life span, its temperature rise should be within the prescribed safe limit [3]. As a result, it is important to carry out thermal analysis of the motor. There are different types of thermal analysis to determine the thermal behaviour of the machine such as lumped parameter thermal model, finite difference and finite element or other alternative numerical techniques. The numerical techniques require very long processing time and also are expensive due to the usage of expensive software. The lumped parameter thermal model on the other hand is fast and requires less number of computations and is most suitable for small and medium size motors [1]. Basically, thermal modelling is designing a thermal network similar to an electrical circuit. It consists of thermal impedances, nodes and heat sources [2]. The different motor parts have been divided into different nodes and the losses acts as the heat source. These thermal parameters can be obtained by solving few equations or can be calculated by tests [1]. Thermal parameters are conduction, convection and

radiation resistances for different parts of the motor. Conduction resistance is given by the length divided by the area and the conductivity of the material used. The convection and radiation resistances are given by one divided by the surface area and heat transfer coefficient of the material [2, 4].

There are many different thermal models proposed in the literature. Mellor, Robert and Turner proposed a lumped parameter thermal model for both steady-state and transient analysis [5]. Aldo, Andrea, Mario and Michele proposed a simple thermal model [6] as compared to the model proposed by Mellor, Robert and Turner [5]. In [3], a generalized thermal model is proposed, where the temperature rise under no load as well as full load is calculated. In [7], some difficult aspects in thermal analysis are covered. Thermal analysis of a wound rotor induction motor is discussed in [8]. In this paper, a lumped parameter thermal model of an induction motor is synthesized. The thermal parameters of the model are obtained based on the geometric information of various parts of the induction motor and the information on the material used for design. This paper also predicts and compares the temperature rise at the outer stator and the outer rotor part of an induction motor driven directly from the main supply with that of an inverter-fed induction motor. Due to the presence of harmonics in the inverter waveforms, more losses are generated in the motor and as a result more temperature rise takes place. In Sect. 2 of this paper, a modified thermal model is proposed and in Sect. 3 the calculation of the temperature rise along with the calculation of thermal parameter and the stator and rotor losses have been explained. The experimental calculations and data obtained are discussed in Sects. 4 and 5 concludes the paper.

2 Thermal Model

Thermal modelling is to synthesize a heat transfer circuit, which is similar to an electrical network. When a motor operates, losses occur, as a result of which heat is developed in different parts of the motor [9, 10]. The heat dissipation takes place via conduction, convection and radiation and various motor parts act as the path for the dissipation. The parameters of the network are calculated by obtaining the resistances and capacitances, which are offered by the path for heat dissipation, completely based on the material used and the dimensional information of the motor parts.

2.1 Simple Thermal Model

Aldo, Andrea, Mario and Michele proposed a simple thermal model [6] as compared to the model proposed by Mellor, Robert and Turner [5]. In this paper, a slightly modified thermal model is proposed. Figure 1 shows a modified thermal model. The forced convection thermal resistance between the external case and

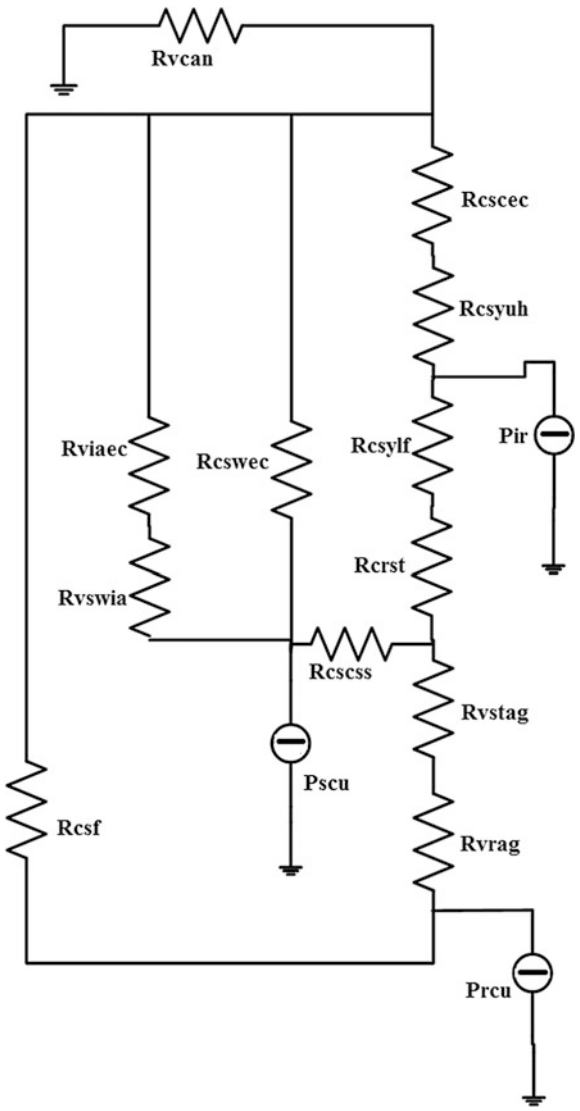


Fig. 1 Modified lumped parameter thermal model

external air has been neglected considering the data of the velocity of the air is not uniform and difficult to calculate. If obtained, will be an inaccurate value, which will lead to inaccurate calculation of the thermal parameter. The thermal analysis for the motor in steady state is performed. As a result, the capacitance in the thermal network is neglected. The asymmetric distribution of temperature in the machine is neglected. The heat transfer in the axial direction is considered only for the shaft of the motor. As a result of the assumptions, the number of thermal parameters in the

model is reduced and the thermal parameters (i.e. the thermal resistances) are calculated based on the equations that are applicable for hollow cylinders [6].

Thermal analysis proposed in this paper is a steady-state analysis and therefore only thermal resistances are considered in the network. The thermal parameters present in the thermal model are conduction, radiation and convection resistances. The effect of radiation is small and can therefore be neglected. The calculations of the thermal parameter are done similar to that as shown in [6].

3 Temperature Determination

The temperature rise of an electric machine can be obtained from the thermal model which is similar to the electrical network. To obtain the temperature rise, the thermal parameters need to be calculated first. For calculating the thermal parameters, the information about the material used in every part of the motor along with the dimensional details of the induction motor needs to be obtained. The thermal parameters can be calculated by substituting the geometric data and the material coefficient in the equations as shown in [6].

The losses that occur in an electric machine act as the thermal sources for the machine. In this model, three most important thermal sources are taken into consideration, i.e. stator copper loss, rotor copper loss and stator iron loss. The other losses of the machine are neglected.

$$\Delta P_i = \propto_{i1} (\theta_i - \theta_1) + \propto_{i2} (\theta_i - \theta_2) + \cdots + \propto_{ik} (\theta_i - \theta_k) \tag{1}$$

Using these three losses in the thermal model of Fig. 1 and Eq. (1) and solving for temperature rise in the stator and temperature rise in rotor, following equations can be obtained [3].

$$\theta_s = R_{sc} P_{scu} + R_{sr} P_{rcu} + R_{sy} P_{ir} \tag{2}$$

$$\theta_r = R_{rs} P_{scu} + R_{rc} P_{rcu} + R_{re} P_{ir} \tag{3}$$

To obtain the temperature rise, Eqs. (2) and (3) are used. For determination of the losses in the motor, two simple tests can be performed. The two tests are blocked rotor test and no-load test. These two tests are performed twice. Once for an induction motor fed from main supply and again for inverter-fed induction motor. The results obtained from this test are used to calculate the stator and the rotor losses for both the cases separately. The thermal parameters can be calculated based on the geometry of the machine. All the data obtained from the no-load test, blocked rotor test and thermal parameter calculations are substituted in the Eqs. (2) and (3) to obtain the temperature rise for the two different cases and the results can be compared. The entire process for temperature rise determination is shown in Fig. 2.

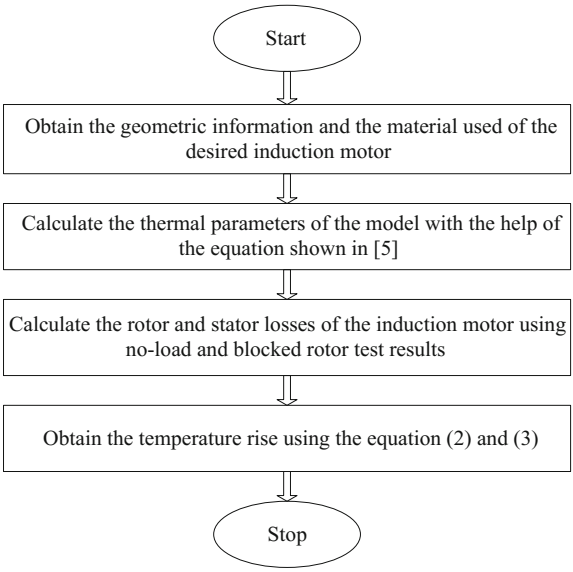


Fig. 2 Flowchart for calculation of temperature rise

Table 1 Calculated values of thermal parameter

Thermal parameters	Values obtained (°C/W)
R_{csylf}	0.0012
R_{csyuh}	0.0011
R_{vstag}	0.1541
R_{vrag}	0.2119
R_{crst}	0.0039
R_{csf}	0.1546
R_{vswia}	0.0061
R_{cswec}	5.304×10^{-6}
R_{viaec}	0.39
R_{cscss}	0.265
R_{vcan}	0.35

4 Results and Discussion

In this paper, thermal parameters are calculated for an induction motor of 0.5 H.P., 220 V, 1500 rpm, 3 A. The calculations of the thermal parameters are entirely based on the information obtained on the materials used and the geometric information for the induction motor [6]. The thermal model obtained is shown in Table 1. To obtain the stator copper loss, stator iron loss and rotor copper loss, a no-load test and blocked rotor test is performed on an induction motor of 0.5 H.P., 220 V, 1500 rpm, 3 A, when it is operated with the raw supply and again when fed

Table 2 Comparison of temperature rise

	Induction motor with sinusoidal supply (°C)	Inverter-fed induction motor (°C)
θ_s	53.76	56.40
θ_r	55.56	59.22

from inverter drive circuit. The losses in both the cases are recorded and substituted in the Eqs. (2) and (3).

Therefore, the temperature rise can be obtained simply by solving Eqs. (2) and (3). In our case the temperature rise is noted in Table 2.

From the results, we see that the temperature rise for inverter-fed induction motor is higher than that of the induction motor run from the raw supply and it has already been established in the literature that induction motor fed from inverter supply will have more losses as compared to the one fed from raw supply. As a result, we can say that the results that have been obtained are justified.

5 Conclusion

This paper presented a comparison of temperature rise of an induction motor when fed from main supply and inverter-fed induction motor. The main aim of this paper is to help the designer to obtain the temperature rise at the outer stator and rotor part for a small- or medium-sized motor in a simple and easy way. In this paper a lumped parameter model is used. With the help of knowledge on geometry and properties of material used, lumped parameter thermal model is synthesized as shown in Fig. 1. A no-load and blocked rotor test is performed to obtain the losses. To obtain the temperature rise, these data are used in Eqs. (2) and (3). The result obtained shows that the temperature rise for inverter-fed induction motor is higher than that of the induction motor fed from raw supply. The reason for this can be the presence of harmonics in the inverter supply.

References

1. Dutta, B., Dr. KarChowdhury, S.: Steady state thermal model of tefc induction machine. In: IEEE International Conference on Power Electronics, Drives and Energy Systems, Bengaluru, India (2012)
2. Boglietti, A., Cavagnino, A., Staton, D., Shanel, M., Mueller, M., Mejuto, C.: Evolution and modern approaches for thermal analysis of electrical machines. IEEE Trans. Ind. Electron. **56** (3) (2009)
3. Shenkman, L., Chertkov, M.: Experimental method for synthesis of generalized thermal circuit of polyphase induction motors. Trans. Energy Convers. **15**(3) (2000)
4. Boglietti, A., Cavagnino, A., Staton, D.A.: TEFC induction motors thermal models: a parameter sensitivity analysis. IEEE Trans. Ind. Appl. **41**(3) (2005)

5. Mellor, P., Roberts, D., Turner, D.: Lumped parameter thermal model for electrical machines of TEFC design. Proc. Inst. Elect. Eng. pt. B **138**(5) (1991)
6. Boglietti, A., Cavagnino, A., Lazzari, M., Pastorelli, M.: A simplified thermal model for variable-speed self-cooled industrial induction motor. IEEE Trans. Ind. Appl. **39**(4) (2003)
7. Staton, D., Boglietti, A., Cavagnino, A.: Solving the more difficult aspects of electricmotor thermal analysis in small and medium size industrial induction motors. IEEE Trans. Energy Convers. **20**(3) (2005)
8. Boglietti, A., Cavagnino, A., Popescu, M., Staton, D.: Thermal model and analysis of wound rotor induction machine. IEEE Trans. Ind. Appl. **49**(5) (2013)
9. Jankowski, T.A., Prenger, F.C., Hill, D.D., O'Bryan, S.R., Sheth, K.K., Brookbank, E.B., Hunt, D.F.A., Orrego, Y.A.: Development and validation of a thermal model for electric induction motors. IEEE Trans. Ind. Electron. **57**(12) (2010)
10. Venkataraman, B., Godsey, B., Premerlani, W., Shulman, E., Thakur, M., Midence, R.: Fundamentals of a motor thermal model and its applications in motor protection. In: IEEE 58th Annual Conference for Protective Relay Engineers (2005)

Contingency Analysis Reliability Evaluation of Small-Signal Stability Analysis

A. Murugan, S. Jayaprakash and R. Raghavan

Abstract Mainly, this paper discusses about electrical power systems. Power systems are linked with power flow control, admittances matrix, eigenvalues, stability and contingency analysis. But here essentially it focuses on stability and contingency analysis. Under all possible operating conditions, new control techniques are presented in great demand. The small-signal stability model for 9-bus system and two-area four-machine 11-bus system is considered in this paper. All buses are modelled as classical model and six and eight state variables are used for the analysis. Individual machine rotor coordinates are transformed from reducing the network equations. The state variable formation came from linearizing network equations and machine differential equations. Generally, the small kind of fault is occurring at transmission area. To observe the system stability, find out the value of eigenvalues and eigenvectors. Finally, results show contingency analysis using IEEE 9-bus system and 11-bus four-machine power systems. The eigenvalues, participation matrix and sensitivity analysis value and all were produced based upon MATLAB Coding.

Keywords Eigenvalues · Left and right eigenvector · Participation matrix
Power system modelling · Small-signal stability · Contingency analysis

1 Introduction

Under small perturbation condition, the small-signal stability of the power system is to maintain synchronism. Whenever small variations or deviations are changing depends upon the load and generation due to continuous changes of synchronism.

A. Murugan (✉) · S. Jayaprakash · R. Raghavan
Department of EEE, Sathyabama University, Chennai 600119, India
e-mail: murugana2007@gmail.com

S. Jayaprakash
e-mail: jakash123@yahoo.com

R. Raghavan
e-mail: rajuraghavan1988@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_24

With the help of machines or generators can be restored forces in the system as well as can be bring in maintain stable conditions [1]. The stable conditions mainly depend on the load. Actually, the small signal is nothing but small kind of disturbances or faults of the power system [2]. Then linearization of system equations is allowable for the purpose of analysis.

The stability of power system networks is an important aspect in reliability of power supply. If the small disturbances are produced in the power system the phenomenon is referred as small-signal stability. Generally while transmitting the power, a disturbance is created in transmission side because of mal operation of the system or changing the circuit breaker or natural causes [3]. Basically two different approaches are used at behaviour and study of power system dynamics. One mainly depends upon time simulation. This accounts for system nonlinearity, but specifically is unable to present frequency domain information. Another one is linear system analysis; it avoids system nonlinearity [4].

After certain period, the system begins or makes the first move; the steady-state system will not be attained. The transient state is recognized in the initial condition during this beginning period [5] in the face of a dynamic equilibrium is happened while two or more turn around development takes place. So this kind of system known as steady state, Actually this kind of steady state stability and all is comes only by the way of small-signal stability in the dynamic system [6].

In synchronism condition, the power is produced through synchronous generators with the intention of operation in synchronism. At the time, this system is presented in rest position of the power system [7]. Suppose if the system frequency, voltage profile and phase sequences are maintained in the same position, then the generators or creators will be synchronized via bus. Normally the power system stability is in stable condition only [8]. Suppose if any kind of fault occurred then at the time it will go into oscillating condition. That kind of fault will be an intended one. It will happen due to mal operation or natural causes or effect [9]. This stability is divided into three different categories. These categories are considered about steady state, transient and dynamic stability.

2 Modelling of SMIB and Multi-machine System

2.1 System Description and Modelling

The SMIB system is connected to the large system via transformer and transmission line with the help of generator. The machine is represented by classical model which has one winding on the rotor (field winding) (Fig. 1).

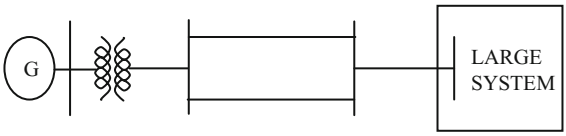


Fig. 1 Single line diagram of the SMIB system

For a classical model of the synchronous machine, the states are incremental changes in rotor side speed and angle. Our analysis the super bar notation on per unit quantities are dropped out.

This is in the form of $\dot{X} = Ax + Bu$.

From this equation, A is the state matrix of the elements. This is dependent mainly on the system parameters of K_D, H, X_T and also the initial operating condition represented by the values of E_1 and δ_0.

Where

Delta-omega is in per unit
Delta-delta is in radians

The synchronizing torque coefficient is given by

$$K_s = \frac{|E'||V_\infty|}{\left(X'_d + X_{\text{tr}} + X_{\text{line}}\right)} \cos\delta \tag{1}$$

3 Multi-machine System

Refer Fig. 2, the SMIB model is only tolerable for analyzing local mode of oscillations. However, for analysis of inter-area mode, we entail a more detailed representation of the network including machines. For a general detailed model

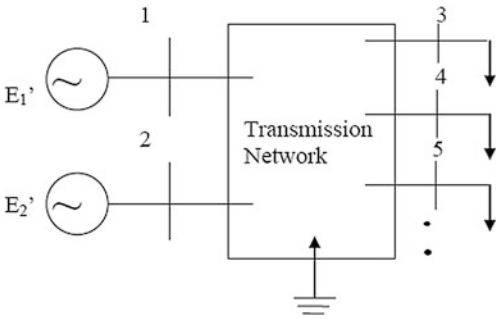


Fig. 2 Representation of the two-machine n-bus system

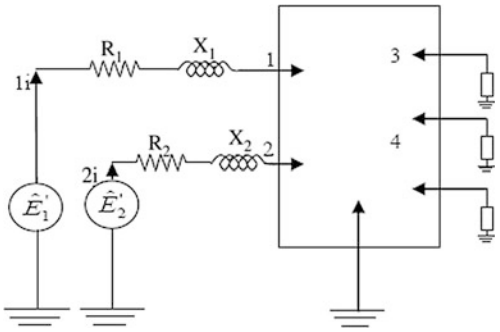


Fig. 3 Equivalent circuit for the two-machine *n*-bus system

which accounts for the state variables voltage behind transient reactance, speed and angle, the differential equations are expressed in the respective *d-q* reference frame (Fig. 3).

Here, two different symmetrical regions are the main system is available s of two symmetrical areas fixed via somewhat weak tie. Each region has one generating division with equal outputs. The generators and excitation a system of dynamic data is used in power system. In setting up, the various power flows used in the studies, capacitors were added necessarily to ensure that the systems voltage profile was satisfactory. Our experience with large interconnected systems confirms some of the results of our studies using the small system, and we are confident that the general conclusions drawn from our work will apply to large systems. The following equations pertain to the four-machine system as well as can be used for IEEE 9-bus system.

3.1 Synchronous Machine Model

Using classical model, synchronous generators were modelled with the help of angles and frequencies in the state variables. In two-area system, the generators were divided into two categories. One is presented in the first area and another one is in second area.

Finally, we are getting the admittance matrix including diagonals of generator.

$$J\frac{\mathrm{d}\omega}{\mathrm{d}t} = T_{\mathrm{m}} - T_{\mathrm{e}} \tag{2}$$

$$\frac{\mathrm{d}\delta}{\mathrm{d}t} = \omega - \omega_0 \tag{3}$$

3.2 Transmission Line Model (Short Line)

The transmission lines are divided into three categories. First one is short transmission line, second one is medium transmission line and finally long transmission line. These and all using depends on the distance and voltages. But this paper has presented the short transmission line because of using the low transmission voltages.

3.3 Load Model

The loads are modelled as a constant admittance in transient stability studies.

3.4 Introduction to Two-Area System

In 11-bus system, one area contains seven buses and two generators and the second area contains four buses and two generators. Here the machines are considered to be classical model. Out of two regions, one region is connected in left half of the system and another one is connected in right half of the system. In 11-bus system, the line between 7 and 9 is considered as weak system. In figure shows that two shunt capacitors are connected bus 7 and 9.

The generator rating is used as 900 MVA and 20 kV.

3.5 Performed Processes

- Calculate the power flow control
- To determine the linear analysis and modal analysis
- To simulate the time domain analysis.

The performed processes are shown based on the following flow chart.

4 Small-Signal Stability

4.1 State Equation

For a classical model of the synchronous machine, the states are incremental changes in rotor speed and angle. In our analysis, the super bar notation on per

unit quantities are dropped out. The state equations for the SMIB system shown below

$$\begin{bmatrix} \overline{\Delta\omega} \\ \overline{\Delta\delta} \end{bmatrix} = \begin{bmatrix} \frac{-K_D}{2H} & \frac{-K_s}{2H} \\ \varpi_0 & 0 \end{bmatrix} \begin{bmatrix} \Delta\omega \\ \Delta\delta \end{bmatrix} + \begin{bmatrix} \frac{1}{2H} \\ 0 \end{bmatrix} \Delta T_{\mathrm{m}} \tag{4}$$

This is the form of $\dot{X} = Ax + Bu$.

A is the state matrix of the elements. It is dependent on the system parameters K_D, H, X_T and the initial operating condition represented by the values of E_1 and δ_0.

Where

Δω is in per unit,
Δδ is in radians

The synchronizing torque coefficient is given by

$$K_s = \frac{\left|E^{'}\right||V_{\infty}|}{\left(X_d^{'} + X_{\mathrm{tr}} + X_{\mathrm{line}}\right)} \cos\delta \tag{5}$$

4.2 Assumptions

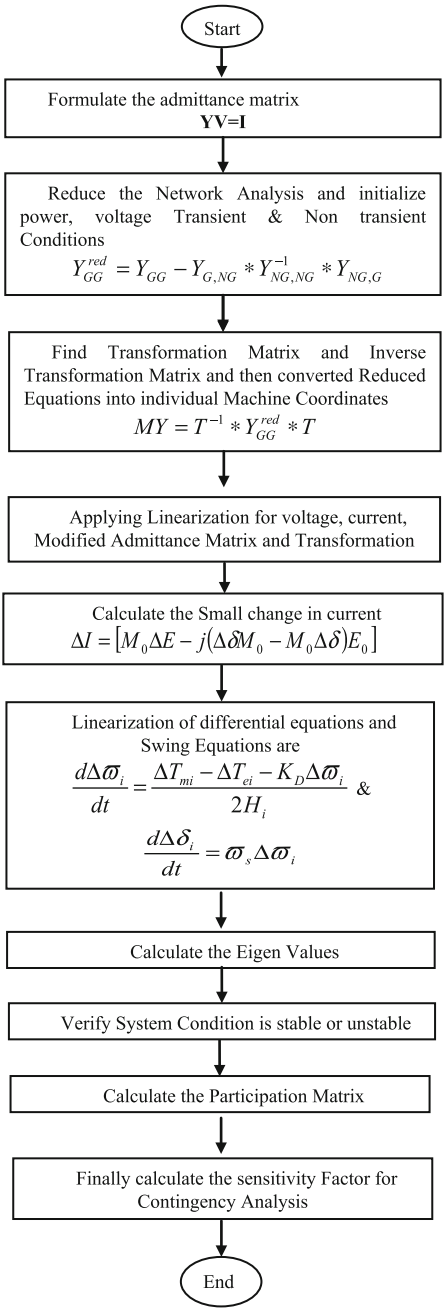
In this paper fully modelled as classical model (Type 0)

(i) Damping is ignored
(ii) The buses between 7 and 9 are considered as a constant admittance

4.3 Preparation

From this small-signal stability analysis, angles, frequencies and voltages are considered as initial conditions as well as it attains from load flow.

5 Multi-machine Small-Signal Stability Algorithm



6 Eigen Analysis

The differential equations of power system model to be formed literalizing network. Then eigenvalues and eigenvectors can be evaluated from the above differential equations.

$$\Delta X = [A]X, \tag{6}$$

where x is a state vector and A is the state matrix, then size of the matrix is $n \times n$; the state equation is expressed by taking the Laplace transform of the system. Then this new equation is derived in the S domain and is given by

$$\det(S[I] - [A]) = 0 \tag{7}$$

The matrix of the poles or values of s of the system is satisfied means then that matrix is called eigenvalues of the Matrix (A). The Matrix A values should be real or complex. If complex conjugate of Matrix A is presented only in the real eigenvalues [10]

$$\lambda = \alpha + j\varpi \tag{8}$$

6.1 Eigenvalues and Stability

If the eigenvalues are presented in the left axis area of the imaginary axis, then the system is stable. Mainly, this system depends on real value. On other hand if any of the eigenvalues comes at right axis area of the imaginary axis, then the system is unstable. Oscillating mode has only a real eigenvalue.

$$\lambda = \sigma + j\varpi \tag{9}$$

(i) Suppose if a system is having complex of negative real value of eigenvalues in the oscillatory mode then the system known is globally stable.
(ii) Suppose if a system has complex of positive real value of eigenvalues in the oscillatory mode means then the system is unstable.
(iii) Suppose if above two conditions or criteria are not satisfied then system is known as an undamped oscillatory response.

7 Participation Matrix

Multiplication of left eigenvector and right eigenvector is called as participation matrix. This matrix is used to calculate the state variables in the eigen factor.

$$P_j = \begin{bmatrix} P_{1j} \\ P_{2j} \\ \vdots \\ \vdots \\ P_{nj} \end{bmatrix} \begin{bmatrix} \phi_{1j}\varphi_{j1} \\ \phi_{2j}\varphi_{j2} \\ \vdots \\ \vdots \\ \phi_{nj}\varphi_{jn1} \end{bmatrix} \tag{10}$$

Here left eigenvector is ψ_{ni} The element $p_{ni} = \psi_{ni}\ \varphi_{jn}$ is called a participation factor. It is a measure of the relative participation of the nth state variable in the ith mode, and vice versa [3].

Small-signal stability analysis is carried out by performing the following steps:

(i) With the help of system data feeding the loads.
(ii) Here, Matrix A has to be formed using load flow analysis of the system linearizing equations.
(iii) If above criteria over successfully then the final results of eigenvalues and frequency will be formed.

7.1 Eigenvalue Sensitivity to Load Changes

The state matrix of sensitivity of an eigenvalue λ_i to an element α_{kj} is equal to the product of the left eigenvector element ψ_{ik} and right eigenvector element φ_{ij}.

$$\frac{\partial \lambda_i}{\partial \alpha_{kj}} = \psi_{ik}\phi_{ij} \tag{11}$$

In power system, by varying the load power at bus 7 and 9 matrix of the system was computed.

8 Contingency Analysis

A contingency analysis is the major action of power system. This is the simulated model using computer application. Mainly contingency analysis is nothing but security analysis. A contingency is the failure or loss of an element (e.g. generator, transformer, transmission line, etc.) in power systems. After solving the problems, results can be classified into three different ways. First one is none; Second one is severe, and finally critical.

None—In power system without any loads or any one element can be rebalanced.

Severe—If using no of elements (Capacitor or Inductor) or lines it will arise some problems or overloaded.

Critical—System is stable means no problem otherwise (unstable) it is create big problem.

It provides an automatic way of looking at all the statistically likely contingencies. In this example, the contingency set is all the single line/transformer outages

9 Simulation Results

The simulation results were shown in the following table. From Table 1 a system can be identified as stable or unstable easily.

From Table 1, all eigenvalues become negative. So we see that system is stable.

Participation matrix for 9-bus system

$$\begin{bmatrix} 0 & 0 & 0 \\ -0.2043 + 0.0011i & -0.2043 - 0.0011i & 0.2951 - 0.0000i \\ -0.2957 - 0.0030i & 0.2957 + 0.0030i & 0.2022 + 0.0000i \end{bmatrix}$$

Sensitivity factor for 9-bus system

$$\begin{bmatrix} 0 & -0.0012 & -0.2324 \\ 0.0016 & -0.2043 - 0.0011i & -0.2310 \\ 0 & -0.2391 & 0 \end{bmatrix}$$

Participation matrix for 11-bus system

$$\begin{bmatrix} 0.3297 - 0.0i & 0.3297 + 0.0i & -0.0010 + 0.0046i & -0.0010 - 0.0046i \\ 0.1764 - 0.0i & 0.1764 + 0.0i & 0.0015 + 0.0059i & 0.0015 - 0.0059i \\ -0.0084 + 0.0i & -0.0084 - 0.0i & 0.2491 + 0.0029i & 0.2491 - 0.0029i \\ 0.0023 - 0.0i & 0.0023 + 0.0i & 0.2504 - 0.0134i & 0.2504 + 0.0134i \end{bmatrix}$$

Table 1 Eigenvalues for 9- and 11-bus system

9-Bus system for three-machine	11-Bus system for two-area four-machine
−0.0091 + 2.4366*i*	−0.0000 + 11.4038*i*
−0.0091 − 2.4366*i*	−0.0000 − 11.4038*i*
−1.2766	−6.3407 + 6.3077*i*
−1.2905	−6.3407 − 6.3077*i*
−0.0017	−8.145 + 6.150*i*
−0.0000	−8.145 − 6.150*i*
–	−0.0000
	−0.0000

Sensitivity factor for 11-bus system

$$\begin{bmatrix} 0 & -0.0012 & -0.3899 & -0.0497 \\ 0.0002 & 0 & -0.0915 & -0.0482 \\ 0.0481 & 0.0251 & 0 & 0.6217 \\ 0 & -0.0305 & -0.4507 & 0 \end{bmatrix}$$

10 Conclusion

The paper proposes an investigation of 9-bus and 11-bus power system. It shows various values of generator and non-generator of admittance matrix, Eigenvalues and participation matrix with the help of eigenvectors. Table 1 analyzed all eigenvalues become negative values. i.e. the system is presented in stable condition. Participated matrix is calculated by two different eigenvectors. Even though if small disturbances occurred in the transmission line, system will come to stable condition after the disturbances are cleared.

- Whenever generating power capacity increases automatically, it will cause the machine loss of synchronism.

References

1. Manokaran, T., Karpagam, V.: Performance Evaluation of a Distance Relay as Applied to a Transmission System with UPFC. IEEE Trans. Power Syst. **21**(3), 1137–1147 (2006)
2. Murugan, A., Thamizmani, S.: A new approach for voltage control of IPFC and UPFC for power flow management. In: IEEE International Conference on Energy Efficient Technologies for Sustainability (ICEETS), pp. 1376–1381 (2013)
3. Gao, F., Strunz, K.: Multi-scale simulation of multi-machine power systems. Int. J. Electr. Power Energy Syst. **31**(9), 538–545 (2009)
4. Kundur, P.: Power System Stability and Control. McGraw-Hill (1994)
5. Jung, K., Suh, Y., Kim, T., Park, T., Lee, Y.: Arc stability control of a high-power thyristor rectifier system in a DC arc furnace. IEEE Trans. Power Electr. **29**(12), 6342–6351 (2014)
6. Stanković, A.M., Sarić, A.T.: Dynamic voltage stability assessment in large power systems with topology control actions. IEEE Trans. Power Syst. **31**(4), 2892–2902 (2016)
7. Potamianakis, E.G., Vournas, C.D.: Short-term voltage instability: effects on synchronous and induction machines. IEEE Trans. Power Syst. **21**(2), 791–798 (2006)
8. Bilgin, H.F., Ermis, M.: Design and implementation of a current source converter for use in industry applications of D-STATCOM. IEEE Trans. Power Electr. **25**(8), 1943–1957 (2010)
9. Ramya, M.V., Surendar, V.: Advanced converter for industrial application using MPPT. J. Control. Converters **1**(1), 1–7 (2016)
10. Angelidis, G., Semlyen, A.: Improved methodologies for the calculation of critical eigen values in small signal stability. IEEE Trans. Power Syst. **11**(3), 1209–1217 (1996)

Finite Element Method Based Determination of Magnetic Loading of Three-Phase Five-Limb Transformer with Impact of DC Offset

Saurabh Kohli, S.B. Mahajan, S.M. Badave, Padmanaban Sanjeevikumar and Atif Iqbal

Abstract In this article, modelling mechanism based on finite element method (FEM) to understand the impact of DC currents on the magnetic loading of the three-phase five-limb transformer is articulated. This paper provides detailed features of magnetizing current variations and progressions of harmonics in transformer. On variation of primary voltage and injecting DC currents based on a weakly coupled multi-harmonic approach, the three-phase five-limb transformer is subjected to irregular magnetizing currents with formation of odd and even harmonics based on saturation level of transformer. Furthermore, the scaled transformer is modelled and it is visualized that the stray fluxes and the saturation levels of the five-limb transformer raise to a higher level on impact of DC currents of varying magnitudes. The analysis of proposed work is performed using ANSYS tool for generating the scaled transformer model and MATLAB for plotting the results which validates the proposed concept.

Keywords Three-phase five-Limb transformer model · DC impact Half-cycle saturation · Harmonics · Magnetizing currents · Geomagnetically induced currents

S. Kohli (✉) · S.B. Mahajan · S.M. Badave
Department of Electrical & Electronics Engineering, Marathwada Institute of Technology, Aurangabad, India
e-mail: saurabh.rwth@gmail.com

S.B. Mahajan
e-mail: sagar25.mahajan@gmail.com

S.M. Badave
e-mail: smb.eed@gmail.com

P. Sanjeevikumar
Department of Electrical & Electronics Engineering, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Iqbal
Department of Electrical Engineering, Muslim Aligarh University, Aligarh, India
e-mail: atif2004@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_25

1 Introduction

The power transformers are utilized in the power system network to modulate the voltage levels at a constant frequency. The transformation of this voltage level takes place in various steps in the network and hence it becomes essential to see the impact of an unintentional direct current which gets into the core of this transformer which is suitably designed to carry alternating current. The phenomenon which is involved in the superimposition of direct currents with the alternating currents is called the half-cycle saturation [1]. The normal operation of the power transformer involves the principle of mutual induction where two coils are wound around the core having a high value of mutual inductance. The flux, which is alternating, flows along the core path because of the alternating voltage being applied to the source coil and is responsible for the production of electromotive force by Faraday's law. Most of the flux remains inside the core owning to its high permeability compared with the surrounding air but there is a part of the flux which passes through the air and this flux is the leakage flux or stray flux. It becomes vital to observe how this unwanted flux is affected when the transformer has two additional limbs compared to a conventional transformer. A very minute dc flux can bring major changes in the flow of alternating flux in the core. This dc flux can enter the core of the transformer through several means. One of the major causes is the geomagnetically induced currents [2–5] which is an atmospheric phenomenon. These currents which are induced in the conductors due to the geomagnetic variations happening in the atmosphere can easily flow into the coils or the windings of transformer if they are star-connected and the neutrals are earthed. These GICs are equivalent to dc currents as they occur over a small frequency. There have been incidents all across the world even causing blackouts due to these GICs. Other sources include power electronics devices which are used in the power network to obtain different regulations based on voltage and currents. An example of such a device is a static VAR compensator in which a small voltage drop causes a direct current flowing into the SVC transformer and eventually causing saturation of the core in one half cycle.

The various after effects of the DC bias may include hot spot heating. When the transformer is affected by DC causing half-cycle saturation of core there is some amount of leakage flux which also induces eddy currents in the core material. Now this flux leaks into other parts of the core like the tank structure like the tie plates and tank walls which results in heating of these parts of the transformer. Magnetostriction is another property which is responsible for changing the shape of the ferromagnetic core material and cause of hissing sound is amplified owning to injection of DC currents. The addition of DC increases the harmonic content of the magnetizing currents and both even and odd harmonics are evident. The impact of these harmonics [6–8] can be devastating on the transformers if they are in large magnitudes.

2 Five-Limb Transformer Construction and Half-Cycle Saturation

In a five-limb transformer, the three limbs which are at the middle are wounded by the three-phase windings which is the exactly the same as in a three-limb but the difference is that there are two other limbs at the end of the three middle limbs who have a smaller area compared to the three main limbs. The cross-section area for the main yoke is also smaller than the main limb cross-sectional area. An additional flux can flow through the added two yokes on the five-limb transformer which is beneficial when we are considering an unbalancing on the secondary side of the transformer possible due to unbalanced loads. There are conditions when the main yoke is not able to carry more flux or else the saturation can take place, in such cases excessive flux finds path to flow through two additional limbs. The flux which originates from the main limb has no fixed path as to which way it flows given the two alternative path and hence the flux is non-sinusoidal. This difference in the structure of five-limb transformer causes the magnetizing currents to vary differently compared to a conventional transformer.

Now as the DC gets injected into the transformer owning to the different sources, there will be a merger of this DC flux into the alternating flux which is flowing already in the transformer during its normal operation. This additional DC flux is produced in a single direction and its magnitude depends on the intensity of the DC currents, the obstruction which is happening in the path of this DC flux and its amplification based on the number of turns of the windings. There is deviation in the normal AC flux owning to the fact that DC flux which is constant will lead to an additional flux in one half cycle but in the other half cycle, i.e. in the negative cycle there will be a subtraction of the flux. Considering the median flux it is observed that it increases in the positive direction and hence the magnetizing currents also see a spike in the positive direction. As the DC is injected further, this distortion in the flux keeps on increasing until the magnetizing currents are of short duration and peaky in nature which results in beginning of the saturation of the core and because of its intensity being higher in one direction it is supposed to be causing half-cycle saturation of the core of transformer. The transformer is severely affected by this causing a shift in the normal flux and the stray flux affecting the parts of transformers. The variation of this DC flux in case of a five-limb transformer is thus essential to visualize.

3 Transformer Scaled Model

The method used for simulating the scaled transformer is the finite element method (FEM) [9, 10]. The method is useful in giving a numerical solution to the associated boundary conditions of a transformer like the flux densities at the various end of core. The impact of the DC current on different areas of the core in terms of

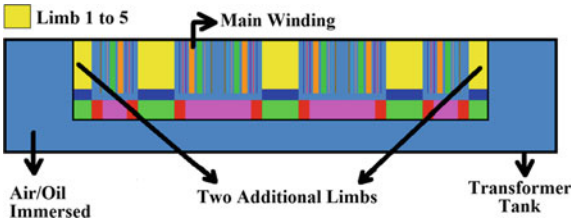


Fig. 1 Two dimensional three-phase five-limb transformers FE Model

variation in flux density and the flux path followed can easily be predicted by using this method [11]. Figure 1 shows a five-limb scaled transformer FE model.

3.1 Working Point Calculation of Transformer

Considering the nonlinear material properties of the core, the working point calculation for the transformer is performed. A weakly coupled multi-harmonic [12, 13] approach is being used and the results of the finite element method are transferred in the frequency domain, where it is possible to visualize the harmonics along with the normal component of the magnetizing currents.

Initially, we consider the core to be made of linear material as it becomes easier to begin the calculations and lesser efforts are involved. Using the fundamental equations, it is possible to calculate the magnetizing currents and also to have a better visualization of the flux and the vector potential solutions are obtained for a transformer with nonlinear core material. It becomes essential to evaluate the performance of the transformer with the inclusion of DC bias at a point which is close to the saturation level of that transformer. Hence considering the flux density at rated value, the initial linear inductance matrix is being obtained. Furthermore, the initial or the fundamental component of the currents in transformer is calculated and then transferred into the time domain and then considering the core material properties to be nonlinear, the nonlinear inductance matrix is obtained at various time steps. The fast Fourier transform (FFT) is then performed on the results obtained for calculating the exciting currents from the nonlinear inductance matrix. To study the effect of DC, an amount in percentage of the fundamental component of the currents is being biased into as DC current. Later, the FFT is calculated to visualize the effect of exciting currents and harmonics in the transformer core.

4 Simulation Result for Scaled Transformer Model

The transformer model has three phases and three limbs having eight coils on each limb, with two coils as main winding, one coil as the tertiary winding and remaining five coils as the regulating windings. The technical details of the transformer are given in Table 1.

Table 1 Technical detail of transformer

S. No	Parameters of transformer	Value
1	Rated power	6.9 kVA
2	Rated voltage	400/400 V
3	Rated current	10/10 A
4	Rated frequency	50 Hz
5	Rated flux density	1.2 T
6	Switching group	Adjustable

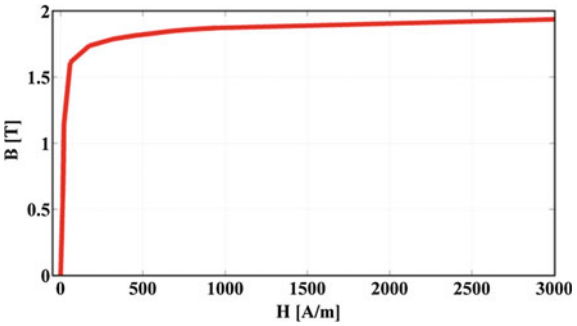


Fig. 2 BH curve for TKESC120 core material

The saturation of the core is being visualized for a three-phase five-limb transformer configuration. The core of the transformer is saturated unevenly and not same for all parts. The effect on the magnetizing currents and harmonics is being visualized for the above model. The nonlinear core material considered for the scaled transformer is TKESC120 with a peak flux density at saturation near to 1.7 T as shown by the B-H Curve in Fig. 2.

Initially, the DC fed into the model is lower and is gradually increased to visualize the effects. The primary winding has been also excited at different levels of voltage to see the impact of DC close to the saturation point of the transformer. The windings are connected in star and the neutral is grounded. The results are plotted in MATLAB so as to analyze the magnetizing current behavior and the harmonic content measured in the nonlinear core material with the impact of DC.

5 Results Interpretation of DC Impact on Magnetizing Currents and Harmonics

Owning to the return flux path, the five-limb transformer will have circulating DC flux in the core which means the saturation of the core would be faster and stronger and hence the magnetizing currents would be larger and with high peaks. The magnetizing currents are higher in three-phase five-limb transformers subjecting them to be more affected by the DC bias as visualized comparing Fig. 3 without DC bias, Figs. 5 and 7 with DC bias and at higher voltage levels. Owning to the dc flux

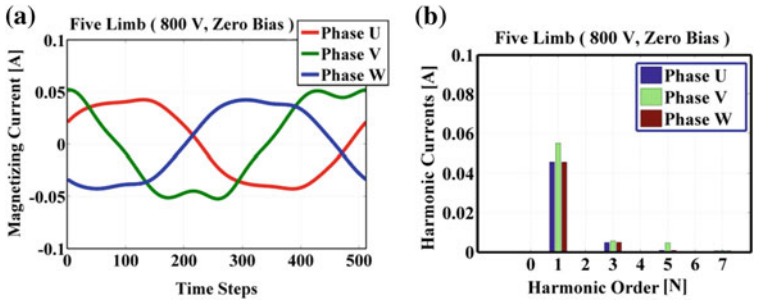


Fig. 3 **a** Magnetizing currents **b** harmonics at zero at [input primary voltage = 800 V, zero (0) DC bias]

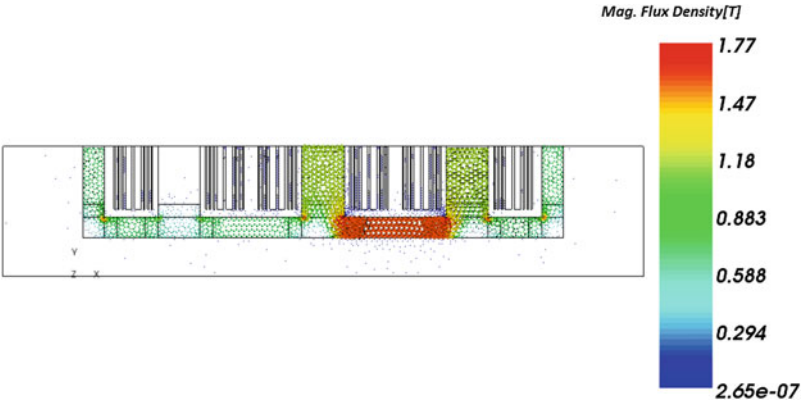


Fig. 4 Flux distribution without DC bias

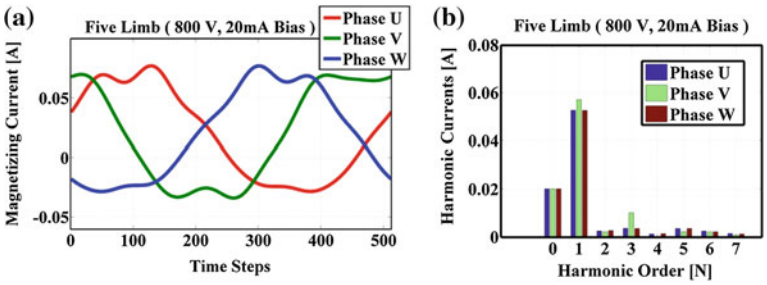


Fig. 5 **a** Magnetizing currents **b** harmonics at [input primary voltage = 800 V, 20 mA DC bias]

flowing through three phases forming circular path in all the phases, the appearance of even harmonics along with odd harmonics is observed. On observing Figs. 7 and 9, it can be visualized that magnetizing currents are peaky and magnitudes are twice as compared to a smaller voltage level with the same DC bias of 100 mA. Also the

Fig. 6 Flux distribution with 20 mA DC bias

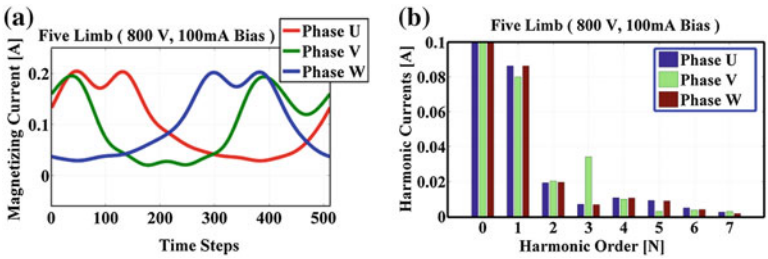


Fig. 7 **a** Magnetizing currents **b** harmonics at [input primary voltage = 800 V, 100 mA DC bias]

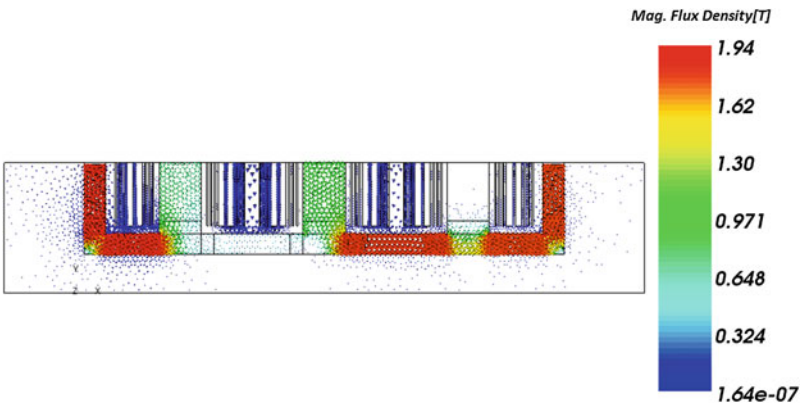


Fig. 8 Flux distribution with 100 mA DC bias

fourth and sixth even harmonics are of higher magnitudes. Thus, all the odd and even harmonics are evident in the case of five-limb transformer model (Figs. 4, 6 and 8).

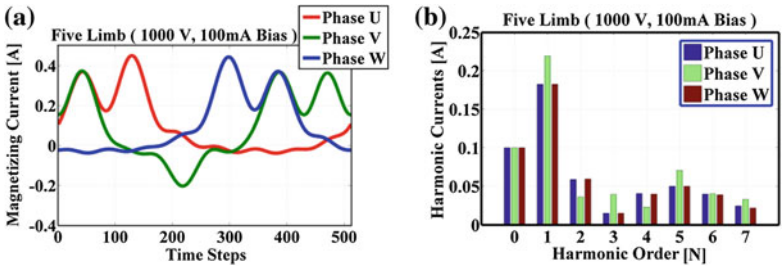


Fig. 9 **a** Magnetizing currents **b** harmonics [input primary voltage = 1000 V, 100 mA DC bias]

6 Visualizing Flux and Magnetic Vector Potential

On comparing Figs. 4, 6, and 8, the stray fluxes which are leaving the transformer core are higher and it is visualized as to how the saturation level of the flux changes with DC bias of 100 mA to 1.94 T compared to a saturation level of 1.78 T at lesser DC bias level of 20 mA. These stray fluxes are visualized to be moving towards the transformer tank structure which eventually leads to hot spots development on the tank structure.

7 Conclusion

A modelling mechanism based on finite element method (FEM) to understand the impact of DC currents on the magnetic loading of the three-phase five-limb transformer is articulated in this article. The impact of DC on the magnetic loading of the three-phase five-limb transformer is presented and it is visualized that owning to the three-phase five-limb transformer structure where an additional two limbs provide an additional path for the superimposed dc flux to pass through and there is no lower reluctance path for it to escape owning to which the saturation of the core material is faster and stronger compared to a conventional transformer. The irregular behavior of magnetizing currents is observed whose magnitude and the peak value increase as the DC bias increased with increasing the voltage levels. Both even and odd harmonics are observed whose magnitude is also directly proportional to the amount of DC flux induced along with AC flux. The quantity of stray or leakage flux is higher and its intensity is also more at higher DC bias levels with clear visualization of stray fluxes in ANSYS.

References

1. Ngnegueu, T., Marketos, F., Devaux, F., Xu, T., Bardsley, R., Barker, S., Baldauf, J., Oliveira, J.: Behavior of transformers under DC/GIC excitation: phenomenon, impact on design/design evaluation process and modeling aspects in support of design. Cigre (2012)

2. Vassell, G.S.: Northeast blackout of 1965. IEEE Power Eng. Rev. (1991) ISSN: 0272-1724
3. Zhang, R.: Transformer modelling and influential parameter identification for geomagnetic disturbance events. pp. 36–40. University of Manchester; S (2012)
4. Kappenman, J.G.: Geomagnetic storms and their impact on power systems. IEEE Power Eng. Rev. (1996) ISSN: 0272-1724
5. Girgis, R., Vedante, K.: Effects of GIC on power transformers and power systems. In: IEEE Transmission and Distribution Conference and Exposition (T&D), IEEE PES, pp. 1–8 (2012)
6. Xiaoping, L., Xishan, W., Lei, L., Yadong, F.: Harmonics study for three-phase transformer under DC inrushing. In: 17th International Zurich Symposium on Electromagnetic Compatibilty, IEEE, singapore (2006)
7. Yarnada, S., Bessho, K., Lu, J.: Harmonic balance finite element method applied to nonlinear AC magnetic analysis. IEEE Trans. Magn. **25**(4), 2971–2973 (1989) ISSN: 0018-9464
8. Lu, S., Liu, Y., De, La, Ree, J.: Harmonics generated from a DC biased transformer. IEEE Trans. Power Deliv. **8**(2), 725–731 (1993) ISSN: 0885-8977
9. Zhao, X., Li, L., Lu J., Cheng, Z., Lu, T.: Characteristics analysis of the square laminated core under DC-biased magnetization by the fixed-point harmonic-balanced FEM. IEEE Trans. Magn. **48**(2), 747–750 (2012) ISSN: 0018-9464
10. Lu, S., Liu, Y.: FEM analysis of DC saturation to assess transformer susceptibility to Geo-magnetically induced current. IEEE Trans. Power Deliv. **8**(3), 1367–1376 (1993) ISSN: 0885-8977
11. Fuchs, E.F., You, Y., Roesler, D.J.: Modeling and simulation, and their validation of three-phase transformers with three legs under DC bias. IEEE Trans. Power. Deliv. **14**(2), 443–449 (1999) ISSN: 0885-8977
12. Björn, R., Adalbert, L. E., Kay, H.: Calculation of the flux distribution of three phase five limb power transformers considering nonlinear material properties. Int. J. Comput. Math. Electr. Electron. Eng. **32**(4) (2013) ISSN: 0332-1649
13. Björn, R., Kay, H.: Multi harmonic approach to determine load dependent local flux variations in power transformer core. Arch. Electr. Eng. **64**(1), 129–138 (2015)

Sensorless Back Stepping Control for a Five-Phase Permanent Magnet Synchronous Motor Drive Based on Sliding Mode Observer

Anissa Hosseyni, Ramzi Trabelsi, Padmanaban Sanjeevikumar, Atif Iqbal and Med Faouzi Mimouni

Abstract This paper presents the development of a speed control technique for a five-phase permanent magnet synchronous motor drive (PMSM) based on sliding mode observer (SMO) and back stepping controller. The design of back stepping controller is detailed. The stability of the closed-loop system is demonstrated in the context of Lyapunov theorem. In order to apply a sensorless five-phase PMSM control, a SMO is used which estimates the rotor speed and the rotor position. Simulation results are reported to prove the efficacy of the proposed strategy in closed loop.

Keywords Back stepping control · Five-phase PMSM · Lyapunov stability Multiphase · Sliding mode observer

A. Hosseyni · M.F. Mimouni
Monastir National Engineering School, Monastir University, Monastir, Tunisia
e-mail: hosseyni.anissa@yahoo.com

M.F. Mimouni
e-mail: mfaouzi.mimouni@enim.rnu.tn

R. Trabelsi
High Institute of Applied Sciences and Technology, Ibn Khaldoun City, 4003 Sousse, Tunisia
e-mail: trabelsi.ramzi@yahoo.fr

A. Hosseyni · R. Trabelsi · M.F. Mimouni
Research Unit: Systèmes Industriels et Des Energies Renouvelables, Rue Ibn Eljazzar, 5019, Monastir, Tunisia

P. Sanjeevikumar (✉)
Department of Electrical and Electronics Engineering, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Iqbal
Department of Electrical Engineering, Qatar University, Doha, Qatar
e-mail: atif.iqbal@qu.edu.qa

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_26

1 Introduction

During the last years, multiphase drives have gained interest for their advantages. Among their features are reduction of torque pulsations and reducing stator phase current [1–3]. The high phase order offers greater fault tolerance. Recently, PMSM has acquired interest [4, 5]. The advantages of this type of machine are numerous, among which we can mention: low inertia, robust and low maintenance cost [3, 4]. Various methodologies to achieve the control of multiphase motor drives are presented in the literature. The most famous one is the vector control [6] which has been used in most industrial drive applications due to its applicability and simplicity. Nevertheless, the five-phase PMSM is a highly nonlinear system so that the vector control, based on conventional PI and PID regulators, fails to achieve the high performance requirements of industrial applications. To compensate for the effects of nonlinearity, many nonlinear control strategies have been developed to control PMSM drives such as sliding mode control [7], the direct torque control [8] and the back stepping control [9–12]. Recently, back stepping control technique is widely developed and studied. A back stepping controller is known as a recursive and systematic design with the flexibility to avoid cancellations of useful nonlinearity [13]. It is a robust and powerful methodology that has been studied in the last two decades. Numerous researches have been focused on the back stepping controller to three-phase PMSM [9–11]. In [9], an adaptive backstepping technique is designed to achieve the sensorless control of PMSM supplied by a current source inverter. The control system is based on the adaptive backstepping observer and adaptive backstepping controller. In [10], an improved direct torque control method of three-phase PMSM based on backstepping control with a recursive least squares algorithm to identify machine parameters is presented. Another new adaptive nonlinear backstepping controller is proposed to compensate the unknown system parameters [11]. Furthermore, a novel trajectory generator is designed to constrain the motor reference current. Several research activities were dedicated to the concept of sensorless control technique of three-phase PMSM drives. One of the known classes of nonlinear observers is the sliding mode observer which posses many special characteristics, namely order reduction control, simple algorithm and disturbance rejection. Numerous papers were dedicated to the observation of PMSM based on SMO [14, 15].

In this paper, the sensorless backstepping controller of five-phase permanent magnet synchronous motor drive is proposed. This paper is organized in five sections including the introduction as follows. Section 2 introduces the model of five-phase PMSM. Then the backstepping controller is discussed in Sect. 3. Section 4 deals with simulation results and the conclusions are presented in Sect. 5.

2 Model of a Five-Phase PMSM

The five-phase PMSM model can be given in a decoupled rotating frame $(d_1q_1 - d_3q_3)$ [4]:

$$\begin{cases} \dfrac{dI_{d1}}{dt} = -b_1 I_{d1} + \omega_e I_{q1} + \dfrac{1}{L_p} v_{d1} \\ \dfrac{dI_{q1}}{dt} = -b_1 I_{q1} - \omega_e I_{d1} - b_2 \omega_e + \dfrac{1}{L_p} v_{q1} \\ \dfrac{dI_{d3}}{dt} = -b_3 I_{d3} + 3\omega_e I_{q3} + \dfrac{1}{L_s} v_{d3} \\ \dfrac{dI_{q3}}{dt} = -b_3 I_{qs} - 3\omega_e I_{d3} + \dfrac{1}{L_s} v_{q3} \\ \dfrac{d\Omega}{dt} = \dfrac{1}{J}\left(\sqrt{\dfrac{5}{2}}\Phi_f P I_{qp} - T_l\right) - \dfrac{f}{J}\Omega \end{cases} \tag{1}$$

where

$\left(I_{d1}, I_{q1}, I_{d3}, I_{q3}\right)$: stator currents in $(d_1 - q_1 - d_3 - q_3)$ frame.

$\left(v_{d1}, v_{q1}, v_{d3}, v_{q3}\right)$: stator voltages in $(d_1 - q_1 - d_3 - q_3)$ frame.

Ω and ω_e are the mechanical and electrical speed respectively. J, f and Φ_f are the inertia moment, the friction coefficient and amplitude of magnet flux respectively. P pair poles and T_l load torque.

$$b_1 = \frac{R_s}{L_p}; b_2 = \frac{\sqrt{\frac{5}{2}}\Phi_f}{L_p}; b_3 = \frac{R_s}{L_s}$$

R_s is stator resistance, L_p and L_s are the inductances of the main fictitious machine and secondary fictitious machine respectively

Equation (1) can be written as:

$$\begin{cases} \dfrac{dI_{d1}}{dt} = g_1 + \dfrac{1}{L_p} v_{d1} \\ \dfrac{dI_{q1}}{dt} = g_2 + \dfrac{1}{L_p} v_{q1} \\ \dfrac{dI_{d3}}{dt} = g_3 + \dfrac{1}{L_s} v_{d3} \\ \dfrac{dI_{q3}}{dt} = g_4 + \dfrac{1}{L_s} v_{q3} \\ \dfrac{d\Omega}{dt} = g_5 \end{cases}, \tag{2}$$

where

$$\begin{cases} g_1 = -b_1 I_{d1} + \omega_e I_{q1} \\ g_2 = -b_1 I_{q1} - \omega_e I_{d1} - b_2 \omega_e \\ g_3 = -b_3 I_{d3} + 3\omega_e I_{q3} \\ g_4 = -b_3 I_{q3} - 3\omega_e I_{d3} \\ g_5 = b_4 I_{qp} - \dfrac{1}{J} T_l - b_5 \Omega \end{cases} \tag{3}$$

where

$$b_4 = \frac{\sqrt{\frac{5}{2}} \Phi_f P}{J};\ b_5 = \frac{f}{J}$$

The control objective is to make the mechanical speed Ω track desired reference Ω_c: such a tracking can be achieved through a backstepping controller algorithm. The stator voltages are $\left(v_{d1}, v_{q1}, v_{d3}, v_{q3}\right)$ considered as inputs.

3 Speed Backstepping Controller

The basic idea of the backstepping control strategy is to make the complex nonlinear closed-loop system equivalent in cascade subsystems of order one. The stability is provided by Lyapunov strategy. The synthesis of the backstepping controller proceeds in two steps.

3.1 Calculation of Current References

The system should follow the trajectory for output variable. The speed error is defined by:

$$e_1 = \Omega_c - \Omega \tag{4}$$

The derivative with respect to time of Eq. (4) gives:

$$\dot{e}_1 = \dot{\Omega}_c - \dot{\Omega} \tag{5}$$

Accounting for Eqs. (2), (5) can be written as:

$$\dot{e}_1 = \dot{\Omega}_c - g_5 \tag{6}$$

In order to check the tracking performances, let us define the first Lyapunov function v_1 associated with speed error, such as:

$$v_1 = \frac{1}{2}e_1^2 \tag{7}$$

Using Eq. (6), the derivative of Eq. (7) is given by:

$$\dot{v}_1 = e_1(\dot{\Omega}_c - g_5) \tag{8}$$

Equation (8) can be rewritten as follows:

$$\dot{v}_1 = e_1(\dot{\Omega}_c - g_5) = -k_1 e_1^2 \tag{9}$$

where $k_1 > 0$, which gives:

$$\dot{e}_1 = \dot{\Omega}_c - \dot{\Omega} = -k_1 e_1 \tag{10}$$

The q_1 axis current contributes towards torque whereas d_1, d_3 and 3 current components do not. This allows maintaining d_1 axis current, d_3 axis current and q_3 axis current equals to zero in order to obtain maximum average torque for given copper losses [2].

The references currents then are given by:

$$\begin{cases} \left(I_{q1}\right)_c = (\dot{\Omega}_c + \dfrac{1}{J}T_l + b_5\Omega + k_1 e_1)/b_4 \\ \left(I_{d1}\right)_c = 0 \\ \left(I_{q3}\right)_c = 0 \\ \left(I_{d3}\right)_c = 0 \end{cases} \tag{11}$$

3.2 Calculation of Currents References

The aim is to obtained the references current obtained by the previous step. The stator current errors are defined as:

$$\begin{cases} e_2 = \left(I_{q1}\right)_c - I_{q1} \\ e_3 = \left(I_{d1}\right)_c - I_{d1} \\ e_4 = \left(I_{d3}\right)_c - I_{d3} \\ e_5 = \left(I_{q3}\right)_c - I_{q3} \end{cases} \tag{12}$$

Considering Eqs. (11), (12) is given by:

$$\begin{cases} e_2 = (\dot{\Omega}_c + \frac{1}{J} T_l + b_5 \Omega + k_1 e_1)/b_4 - I_{q1} \\ e_3 = -I_{d1} \\ e_4 = -I_{d3} \\ e_5 = -I_{q3} \end{cases} \tag{13}$$

Using Eqs. (13), (6) can be given as:

$$\dot{e}_1 = b_4 e_2 - k_1 e_1 \tag{14}$$

The derivative of Eq. (14) gives:

$$\begin{cases} \dot{e}_2 = (\dot{I}_{q1})_c - \dot{I}_{q1} \\ \dot{e}_3 = (\dot{I}_{d1})_c - \dot{I}_{d1} \\ \dot{e}_4 = (\dot{I}_{d3})_c - \dot{I}_{d3} \\ \dot{e}_5 = (\dot{I}_{q3})_c - \dot{I}_{q3} \end{cases} \tag{15}$$

By substituting Eq. (2) in Eq. (15), one obtains:

$$\begin{cases} \dot{e}_2 = (\dot{I}_{q1})_c - \dot{I}_{q1} = (\dot{I}_{q1})_c - g_2 - \frac{1}{L_p} v_{q1} \\ \dot{e}_3 = (\dot{I}_{d1})_c - \dot{I}_{d1} = (\dot{I}_{d1})_c - g_1 - \frac{1}{L_p} v_{d1} \\ \dot{e}_4 = (\dot{I}_3)_c - \dot{I}_{d3} = (\dot{I}_{d3})_c - g_3 - \frac{1}{L_s} v_{d3} \\ \dot{e}_5 = (\dot{I}_{q3})_c - \dot{I}_{q3} = (\dot{I}_{q3})_c - g_4 - \frac{1}{L_s} v_{q3} \end{cases} \tag{16}$$

In order to prove the stability of the overall system, let us choose a new Lyapunov function defined as:

$$v_2 = \frac{e_1^2 + e_2^2 + e_3^2 + e_4^2 + e_5^2}{2} \tag{17}$$

The derivative of Eq. (17) is given by:

$$\begin{aligned} \dot{v}_2 = & -k_1 e_1^2 - k_2 e_2^2 - k_3 e_3^2 - k_4 e_4^2 - k_5 e_5^2 \\ & + e_2 \left(k_2 e_2 + a_4 e_1 + (\dot{I}_{q1})_c - g_2 - \frac{1}{L_p} v_{q1} \right) + e_3 \left(k_3 e_3 + (\dot{I}_{d1})_c - g_1 - \frac{1}{L_p} v_{d1} \right) \\ & + e_4 \left(k_4 e_4 + (\dot{I}_{d3})_c - g_3 - \frac{1}{L_s} v_{d3} \right) + e_5 \left(k_5 e_5 + (\dot{I}_{q3})_c - g_4 - \frac{1}{L_s} v_{q3} \right) \end{aligned} \tag{18}$$

The derivative of the whole Lyapunov function Eq. (18) is negative, if the quantities between parentheses in the same equation are equal to zero.

$$\begin{cases} k_2 e_2 + b_4 e_1 + (\dot{I}_{q1})_c - g_2 - \dfrac{1}{L_p} v_{q1} = 0 \\ k_3 e_3 + (\dot{I}_{d1})_c - g_1 - \dfrac{1}{L_p} v_{d1} = 0 \\ k_4 e_4 + (\dot{I}_{d3})_c - g_3 - \dfrac{1}{L_s} v_{d3} = 0 \\ k_5 e_5 + (\dot{I}_{q3})_c - g_4 - \dfrac{1}{L_s} v_{q3} = 0 \end{cases} \tag{19}$$

The stator voltages are given by:

$$\begin{cases} v_{q1} = L_p\left(k_2 e_2 + b_4 e_1 + (\dot{I}_{q1})_c - g_2\right) \\ v_{d1} = L_p\left(k_3 e_3 + (\dot{I}_{d1})_c - g_1\right) \\ v_{d3} = L_s\left(k_4 e_4 + (\dot{I}_{d3})_c - g_3\right) \\ v_{q3} = L_s\left(k_5 e_5 + (\dot{I}_{q3})_c - g_4\right) \end{cases} \tag{20}$$

where k_2, k_3, k_4 and k_5, are positive constants.

The synthesis of back stepping controller requires the rotor position and rotor speed information. So that the speed and rotor speed transducers should be installed in the shaft. However, these sensors are sensitive to environment conditions and increase the system cost. The algorithm-based sliding mode observer used in this work was developed with details in [2] but not described in this paper. The sliding mode observer was applied to five-phase PMSM to estimate the rotor speed and the rotor position. For more details refer to [2].

4 Simulation Results

A MATLAB/Simulink environment was used to simulate the feedback back stepping control based on SMO.

The corresponding results under the two different profiles: reversing transient and low speed are illustrated by Figs. 1 and 2 respectively. Figure 1 illustrates the drive performance to reversing the speed command. Figure 1a shows the reference, estimated and real speed. One notes that the observed speed converges to the reference one with good estimation. It seems clear from Fig. 1b that the developed observer displays good results in terms of speed estimation. Indeed, the estimation error of rotor speed is almost zero in steady state. Figure 1c displays the observed and the actual position. The five-phase PMSM performances at low speed are reported in Fig. 2. The reference speed is set at 10 rad/s. Figure 2a displays the real,

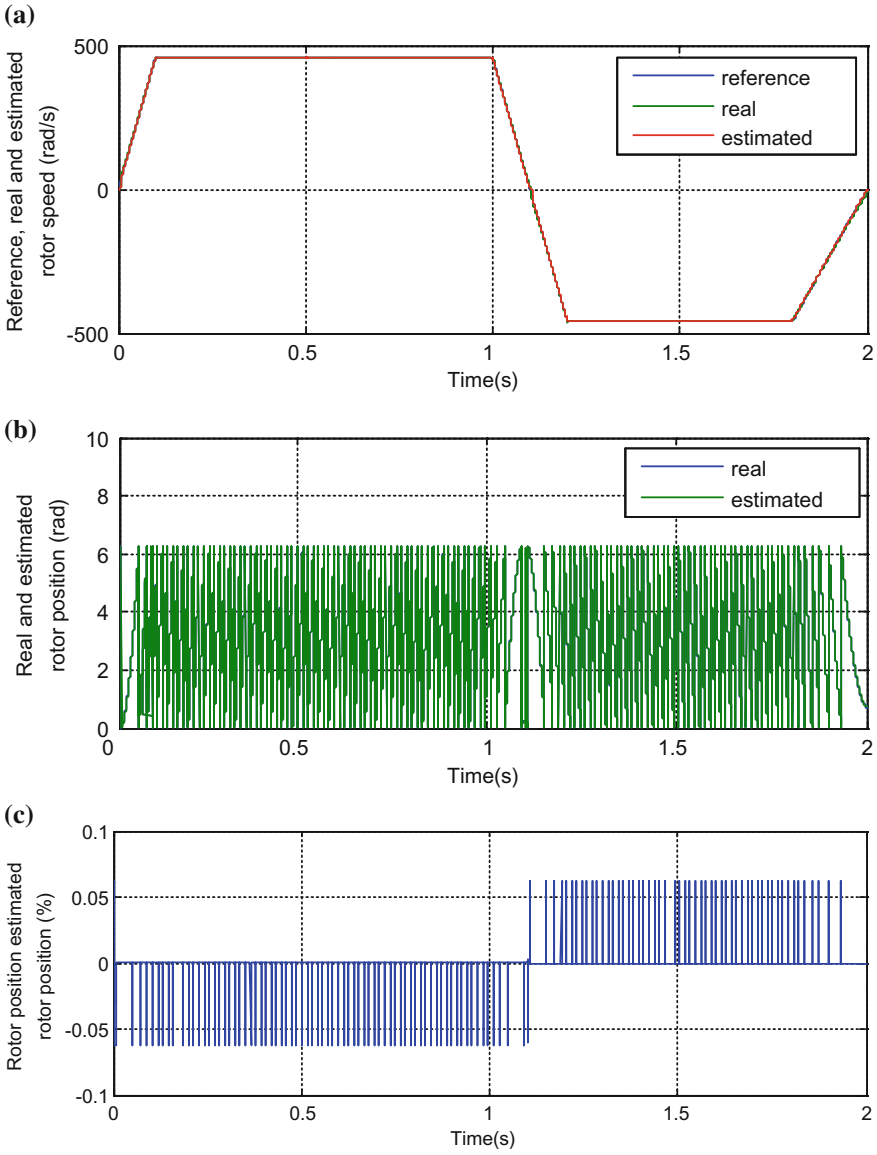


Fig. 1 Performances of five-phase PMSM to speed change: **a** speed; **b** estimation error of rotor speed **c** rotor position

observed and reference rotor speed. We can conclude a good estimation in terms of trajectory tracking. Nevertheless, there is a small estimation error in transient state as shown in Fig. 2b. Figure 2c displays the observed and real rotor position and its estimation error is shown in Fig. 2d. The corresponding results prove the performance of the SMO.

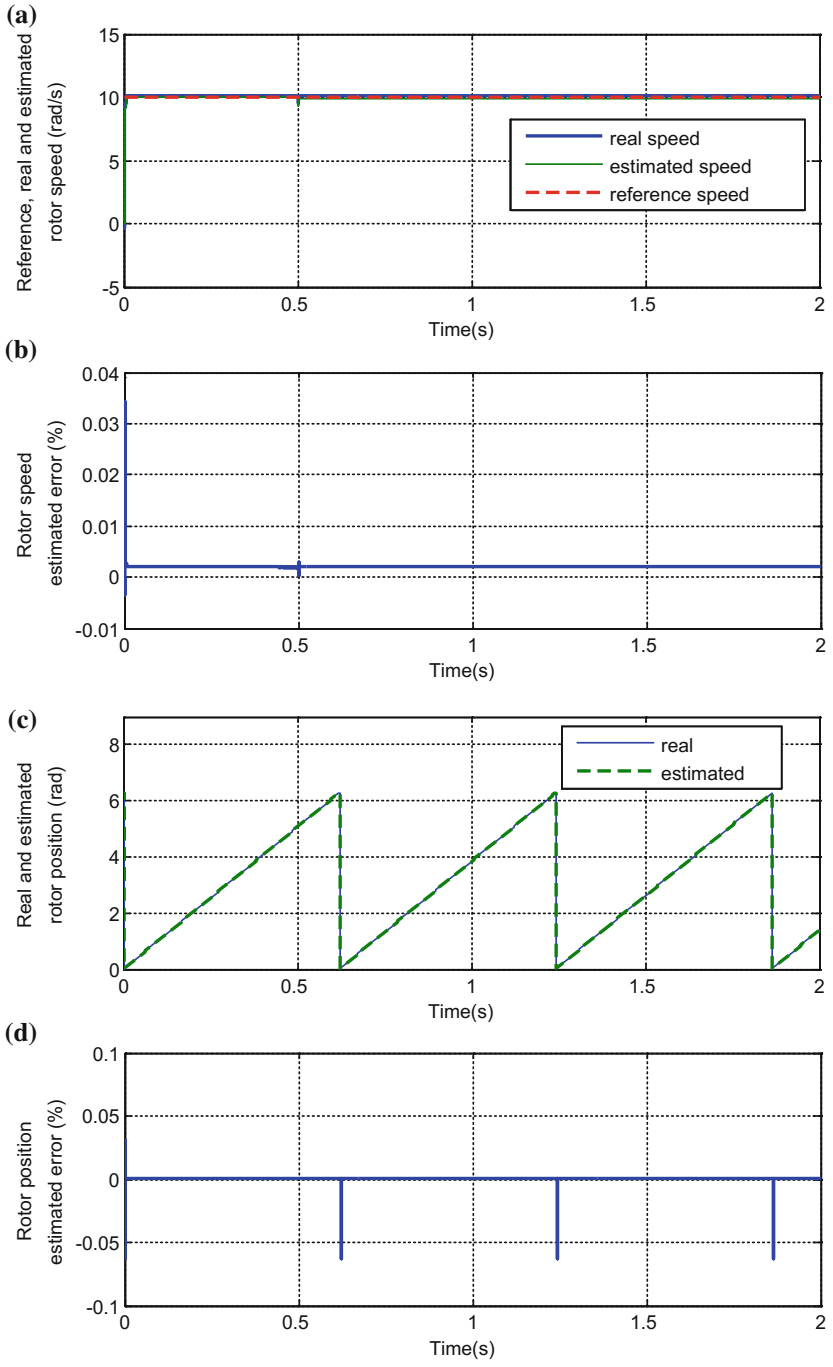


Fig. 2 Performances of five-phase PMSM to speed change: **a** speed; **b** estimation error of rotor speed **c** rotor position, **d** estimation error of rotor position

5 Conclusion

This work presented the sensorless backstepping controller of a five-phase PMSM based on SMO. Developed controller satisfied the stability condition under Lyapunov criterion for both transient and dynamic behaviours. Numerical results verify the developed theoretical background in terms of rotor speed and rotor position estimation under different profiles.

References

1. Hosseyni, A., Trabesi, R., Mimouni, M.F., Iqbal, A.: Vector controlled five-phase permanent magnet synchronous motor drive. In: Conference Proceedings IEEE Indian Symposium on Industrial Electronics IEEE-ISIE'14, Turkey, pp. 2122–2127 (2014)
2. Hosseyni, A., Trabelsi, R., Mimouni, M.F., Iqbal, A., Alammari, R.: Sensorless sliding mode observer for a five-phase permanent magnet synchronous motor drive. ISA Trans. Elsevier J. **58**, 462–473 (2015)
3. Guo, L., Parsa, L.: Model reference adaptive control of five-phase IPM Motors based on neural network. IEEE Trans. Ind. Electron. **59**(13), 1500–1508 (2012)
4. Parsa, L., Toliyat, H.: Five-phase permanent-magnet motor drives. IEEE Trans. Ind. Appl. **41** (11), 30–37 (2005)
5. Mohammadpour, A., Parsa, L.: A unified fault-tolerant current control approach for five-phase pm motors with trapezoidal back Emf under different stator winding connections. IEEE Trans. Power Electron. **28**(17), 3517–3527 (2013)
6. AbuRub, H., Iqbal, A., Guzinski, J.: High Performance control of AC Drives with Matlab/Simulink Models. Wiley, West Sussex, United Kingdom (2012)
7. Chang, S.H., Chen, P.Y., Ting, Y.H., Hung, S.W.: Robust current control-based sliding mode control with simple uncertainties estimation in permanent magnet synchronous motor drive systems. IET. Power Appl. **4**(6), 441–450 (2010)
8. Changliang, X., Jiaxin, Z., Yan, Y., Tingna, S.: A novel direct torque control of matrix converter-fed PMSM drives using duty cycle control for torque ripple reduction. IEEE Trans. Ind. Electron. **61**(6), 2700–2713 (2014)
9. Xu, Y., Lei, Y., Sha, D.: Backstepping direct torque control of permanent magnet synchronous motor with RLS parameter identification. In: Proceedings of IEEE International Conference Electrical Machines, IEEE-ICEMS'14, China, pp. 573–578 (2014)
10. Bernat, J., Kolota, J., Stepien, S., Szymanski, G.: Adaptive control of permanent magnet synchronous motor with constrained reference current exploiting backstepping methodology. In: Proceedings of IEEE International Conference Control Applications, IEEE-CCA'14, France, pp. 1545–1550 (2014)
11. Karabacak, M., Eskikurt, H.I.: Speed and current regulation of a permanent magnet synchronous motor via nonlinear and adaptive backstepping control. Mathematical and Computer Modelling, Elsevier J. **53**, 2015–2030 (2011)
12. Hsu, C.F.: Adaptive backstepping Elman-based neural control for unknown nonlinear systems. Neurocomput. Elsevier J. **136**, 170–179 (2014)
13. Trabelsi, R., Khedher, A., Mimouni, M.F., M'sahli, F.: Backstepping control for an induction motor using an adaptive sliding rotor-flux observer. Electr. Power Syst. Res. Elsevier J. **93**, 1–15 (2012)

14. Kim, H., Son, J., Lee, J.: A high-speed sliding-mode observer for the sensorless Speed control of a PMSM. IEEE Trans. Ind. Electron. **58**(19), 4069–4077 (2011)
15. Qiao, Z., Shi, T., Wang, Y., Yan, Y., Xia, C., He, X.: New sliding-mode observer for position sensorless control of permanent-magnet synchronous motor. IEEE Trans. Ind. Electron. **60** (12), 710–719 (2013)

A Compact Dual-Band N-Way Wilkinson Power Divider for GSM

Aijaz M. Zaidi, Syed A. Imam and Binod K. Kanaujia

Abstract In this paper, a compact dual band equal split N-way Wilkinson power divider (WPD) is presented for GSM. A coupled line is also proposed as dual-band quarter wavelength transmission line transformer (DBQWTLT). To understand the dual-band operation of DBQWTLT, the complete derivation for the design equations is also done herein. By replacing each quarter ($\lambda/4$) wavelength transmission line (TL) of the single-band equal split N-way WPD with the proposed DBQWTLT, the proposed circuit is obtained. To validate the proposed approach, dual-band equal split two-way- and five-way WPD for 900 and 1800 MHz (GSM frequencies) operating frequencies are presented here. The simulated results of the dual-band equal split two-way and equal split five-way Wilkinson power dividers validate the theoretical approach.

Keywords Wilkinson power divider · Quarter wavelength transmission line transformer · Advanced design system (ADS)

1 Introduction

The wireless communication industry is very charismatic and challenging now. The new advancements in the technology imposed some requirement on the wireless communication systems such as compact size, multiband operations, and wide

A.M. Zaidi (✉) · S.A. Imam
Department of Electronics and Communication Engineering, Jamia Millia Islamia University, New Delhi, India
e-mail: aijaz.zaidi72@gmail.com

S.A. Imam
e-mail: imaam_jmi@yahoo.co.in

B.K. Kanaujia
Department of Electronics and Communication Engineering, Ambedkar Institute of Advanced Communication Technologies & Research, New Delhi, India
e-mail: bkkanaujia@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_27

bandwidth. Power dividers/splitters are used to divide the single signal in more than one signal, for example, three-way power divider divides the input signal into three output signals. Previous work on single band N-way power divider was done in [1–3]. Several metrics namely cost, size, bandwidth, have been adopted to define the effectiveness of these components. Significant work was also done to make it dual band [4–6]. But each these techniques has its limitations and drawbacks. For example, in [4] two section transmission lines in cascaded form were used for dual-band operation. But shows poor isolation loss. In [5] two-way dual band, WPD was proposed using stubs. But occupies large area because of shunt stubs. Multiband N-way Wilkinson power dividers were also proposed in [7].

In this paper, a compact dual-band equal split N-way Wilkinson power divider for Global System for Mobile communication (GSM) is proposed. This paper is divided into five sections. The coupled line as DBQWTLT with its dual-band operation is explained in Sect. 2. The proposed dual-band N-way equal split WPD is explained in Sect. 3. Simulation results of dual-band equal split two-way- and five-way Wilkinson power divider with explanation are given in Sect. 4.

2 Dual-Band Quarter Wavelength Transmission Line Transformer

The structure of the conventional $\lambda/4$ TL and the proposed DBQWTLT are shown in Fig. 1. Z_C, Z_E, Z_{odd}, and θ are the characteristics parameters (characteristics impedance, even, odd, impedance, and electrical length) of the conventional $\lambda/4$ TL and the proposed DBQWTLT respectively. The design equations for the dual-band operation for DBQWTLT are obtained by doing even-odd-mode analysis.

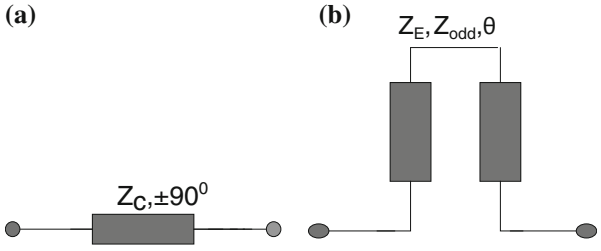


Fig. 1 **a** Quarter wavelength transmission line, **b** proposed dual band quarter wavelength transmission line transformer

2.1 Even-Mode Analysis

The even-mode half circuit of the conventional ƛ/4 TL is an open stub of electrical length ±45° and even-mode half circuit of the DBQWTLT is an open stub of electrical length θ, shown in Fig. 2. Equations (1) and (2) are obtained for the impedances of the even-mode half circuit of the conventional quarter wavelength TL and proposed DBQWTLT. By taking Eqs. (1) and (2) equal, Eq. (3) is obtained.

$$Z_{\text{in}} = \frac{Z_E}{j \tan \theta} \tag{1}$$

$$Z_{\text{in}} = -jZ_C \tag{2}$$

$$Z_E = Z_C \tan \theta. \tag{3}$$

2.2 Odd-Mode Analysis

The odd-mode half circuit of the proposed DBQWTLT and the conventional quarter wavelength transmission line are shown in Fig. 3. The odd-mode half circuit of both the structures is short stubs of electrical length ±45° and θ respectively. The equivalent impedances of short stubs of electrical length ±45° and θ are given in Eqs. (4) and (5) respectively. Both the structures, shown in Fig. 3, are equivalent. So, on taking this condition, Eq. (6) is obtained.

$$Z_{\text{in}} = jZ_{\text{odd}} \tan \theta \tag{4}$$

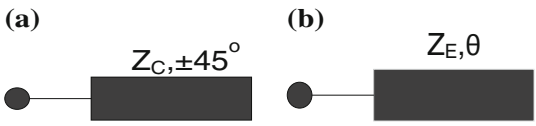


Fig. 2 Even-mode half circuit **a** quarter wavelength transmission line, **b** proposed dual band quarter wavelength transmission line transformer

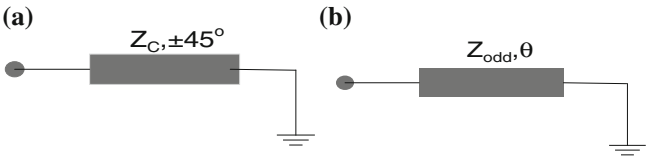


Fig. 3 Odd-mode half circuit **a** quarter wavelength transmission line, **b** proposed dual band quarter wavelength transmission line transformer

$$Z_{\text{in}} = jZ_C \tag{5}$$

$$Z_{\text{odd}} = Z_C \cot\theta. \tag{6}$$

2.3 Dual-Band Operation

The equations for the dual operation of the proposed structure can be obtained with the help of the mathematical concept. The coupled line exhibits dual-band characteristics at two frequencies. So, Eqs. (3) and (6) should be justifiable at two frequencies. Here, we assume f_1 and f_2 are the operating frequencies of the circuit. Let $f_2 = kf_1$, where k is the ratio of the f_2 and f_1. If θ_2 and θ_1 are the electrical lengths of the coupled line at the operating frequencies f_2 and f_1. Equations (3) and (6) are re-expressed as.

$$\begin{aligned} Z_E &= Z_C \tan\theta_1 \\ Z_E &= Z_C \tan\theta_2 \end{aligned} \tag{7}$$

$$\begin{aligned} Z_{\text{odd}} &= Z_C \cot\theta_1 \\ Z_{\text{odd}} &= Z_C \cot\theta_2 \end{aligned} \tag{8}$$

For Eqs. (7) and (8) validation,

$$\theta_1 + \theta_2 = a\pi$$

$$\frac{\theta_2}{\theta_1} = \frac{f_2}{f_1} = k, \tag{9}$$

where a is an integer. The value of the θ_1 and θ_2 are obtained from Eq. (9).

$$\theta_1 = \frac{a\pi}{1+k} \tag{10}$$

For the compact size, take $a = 1$.

3 Proposed Dual-Band Equal Split N-Way Wilkinson Power Divider

3.1 *Single-Band Equal Split N-Way Wilkinson Power Divider*

The conventional single-band equal split N-way WPD is shown in Fig. 4, where $Z_0\sqrt{N}$ is the characteristics impedance of conventional 90° TL and N is the number of the way. Each TL of the conventional single-band WPD is replaced with proposed DBQWTLT; we obtained the proposed dual-band WPD, Fig. 5. The required values of the Z_E, Z_{odd}, θ can be obtained using Eqs. (3), (6), (9) and (10).

3.2 *Dual-Band Equal Split Two-Way Wilkinson Power Divider*

Let the terminals impedance (Z_0) of the two-way WPD are 50 Ω. For two-way WPD, $N = 2$. Then $Z_0\ \sqrt{2} = 70.7106 = Z_c$. This Wilkinson power divider is for GSM applications. So, 900 and 1800 MHz frequencies have taken as operating frequencies. The ratio of the operating frequencies/electrical length is equal to two. This is the value of $k = 2$. For the compact design, we have taken $a = 1$. By putting the value of a and k in Eq. (10), the electrical length of the coupled line (DBQWTLT), has been obtained, $\theta = 60°$. The value of the even-odd-mode impedances, $Z_E = 122.474\ \Omega$, $Z_{odd} = 40.824\ \Omega$ of the DBQWTLT, have been obtained from Eqs. (3) and (6). A schematic of two-way WPD is shown in Fig. 6.

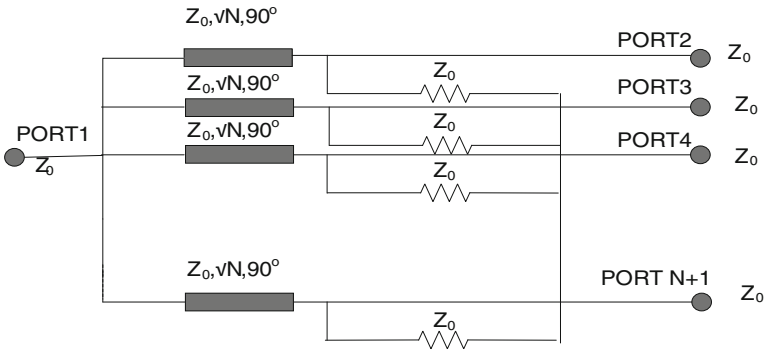


Fig. 4 Single-band equal split N-way Wilkinson power divider

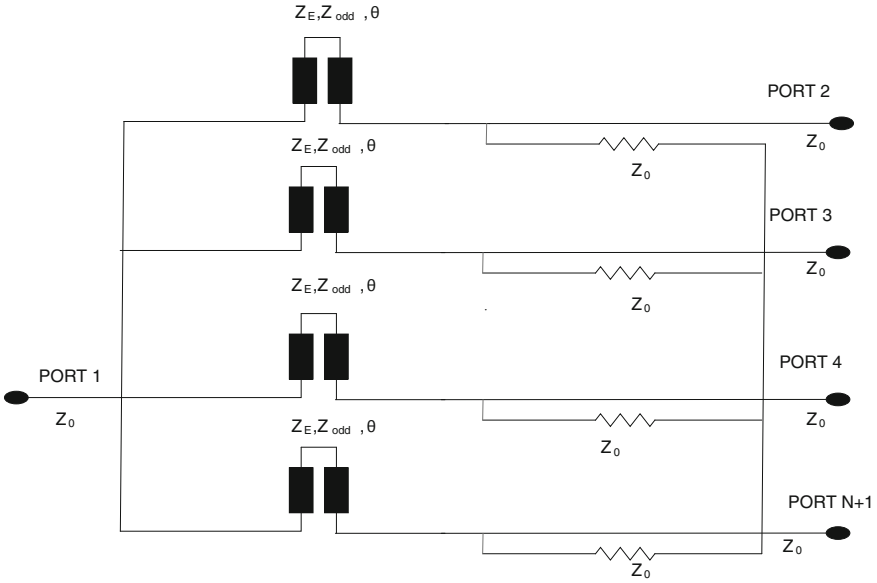


Fig. 5 Proposed dual-band equal split N-way Wilkinson power divider

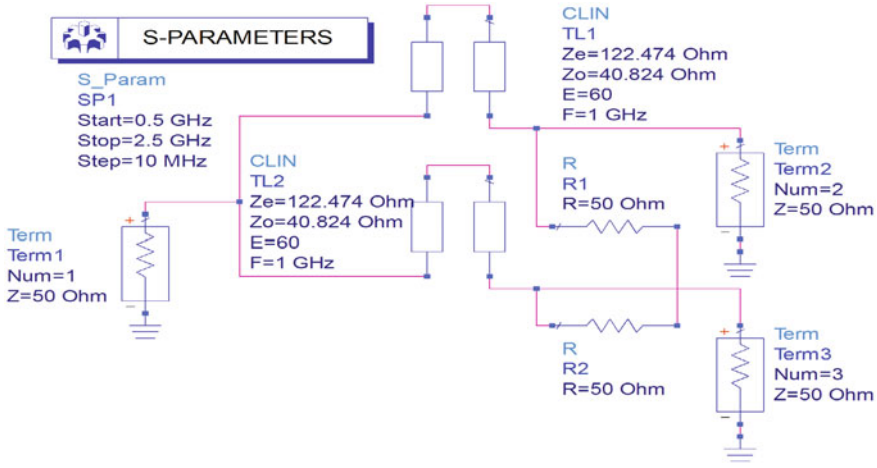


Fig. 6 Dual-band equal split two-way Wilkinson power divider

3.3 *Dual-Band Equal Split Five-Way Wilkinson Power Divider*

For the five-way WPD, $N = 5$. So, $Z_0\sqrt{5} = 111.803\ \Omega = Z_c$. Rest of the procedure to find the desired values of the components of the presented dual-band equal split two-way WPD has been applied. The values of the coupled line (DBQWTLT) parameters Z_E, Z_{odd} and θ have been obtained as $Z_E = 193.649\ \Omega$, $Z_{odd} = 64.549\ \Omega$ and 60° respectively for the dual-band equal split five-way WPD. The schematic of the dual-band equal split five-way WPD is shown in Fig. 7.

4 Simulation Results

Two verify the design approach, the schematic circuits of the presented dual-band equal split two-way- and five-way WPD has been simulated in Agilent Technologies ADS. Ideal coupled lines have been used for the simulation. The simulated results of the presented dual-band equal split two-way WPD and five-way WPD have been satisfied all the characteristics conditions of single-band equal split N-way WPD like ports matched condition ($S_{11} = S_{22} = S_{33} = S_{44} = S_{55} = S_{66} = 0$), output ports isolation ($S_{23} = S_{32} = S_{43} = S_{45} = S_{56} = 0$) and equal power/insertion losses ($S_{21} = S_{31} = S_{41} = S_{51} = -7$ dB) at both the frequency bands. The return loss, insertion loss, and port isolation of the presented dual-band equal split two/

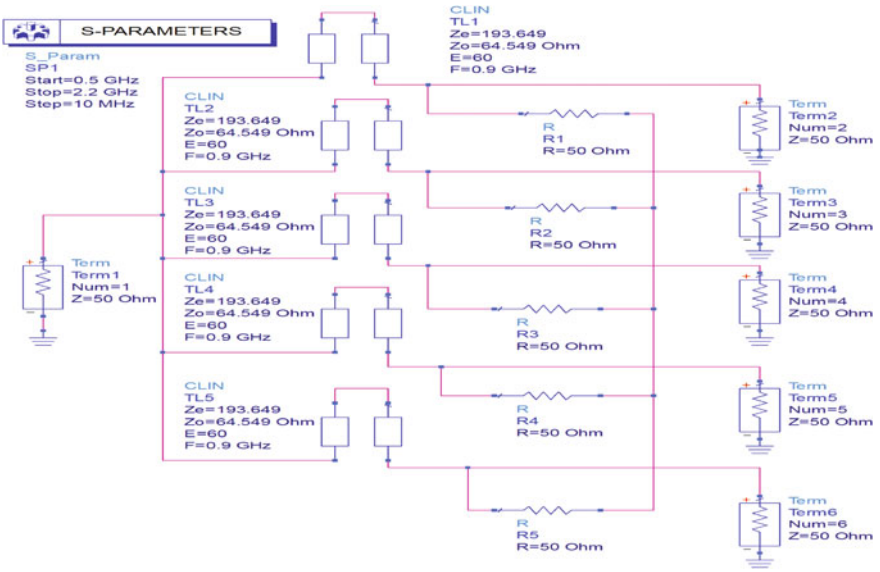


Fig. 7 Dual-band equal split five-way Wilkinson power divider

five-way WPDs are <−60.0 dB/<−70.0 dB, −3.01 dB/−6. 99 dB and <−60.0 dB/<−70.0 dB respectively, have been achieved at both the frequency bands, Figs. 8, 9, 10, 11, 12, 13, 14 and 15.

4.1 *Results of the Presented Two-Way Wilkinson Power Divider*

See Figs. 8, 9, 10, 11 and 12.

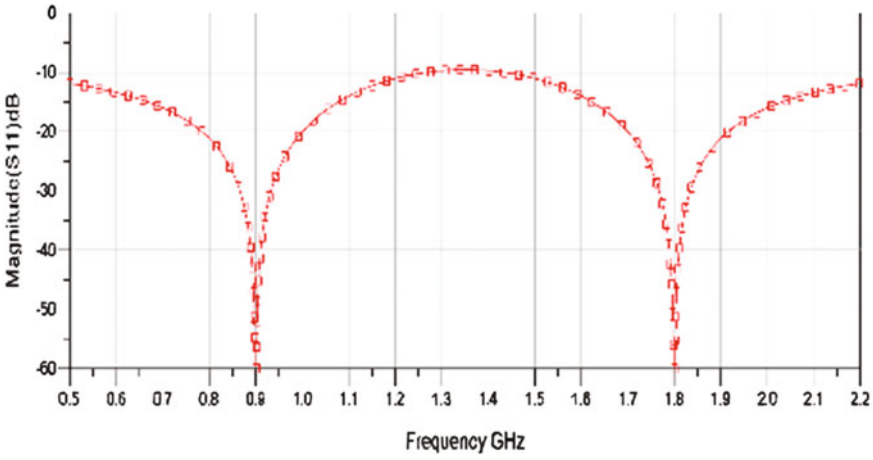


Fig. 8 Input return loss

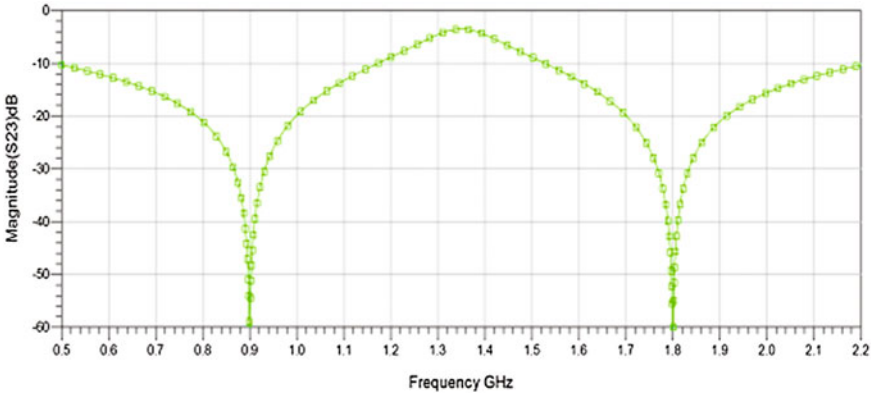


Fig. 9 Port isolation

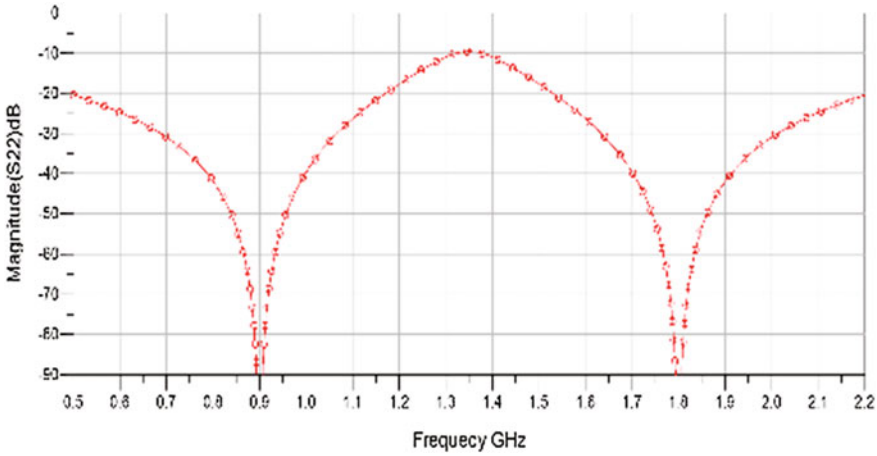


Fig. 10 Output return loss

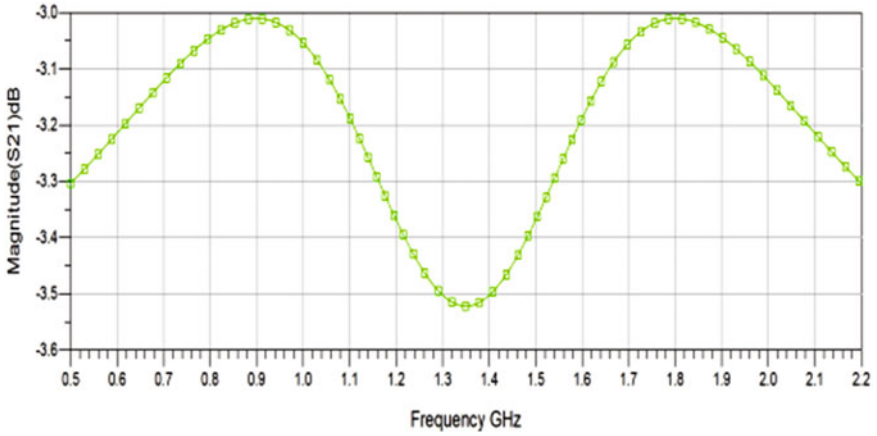


Fig. 11 Insertion loss

4.2 *Results of the Presented Five-Way Wilkinson Power Divider*

See Figs. 12, 13, 14 and 15.

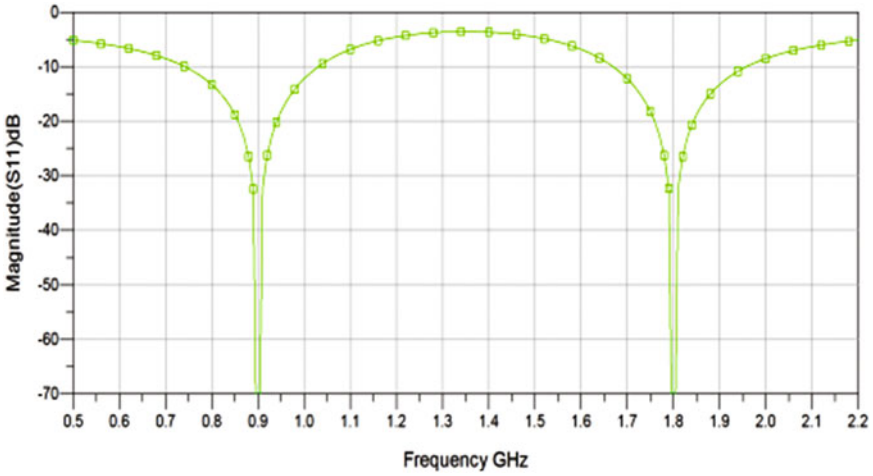


Fig. 12 Input return loss

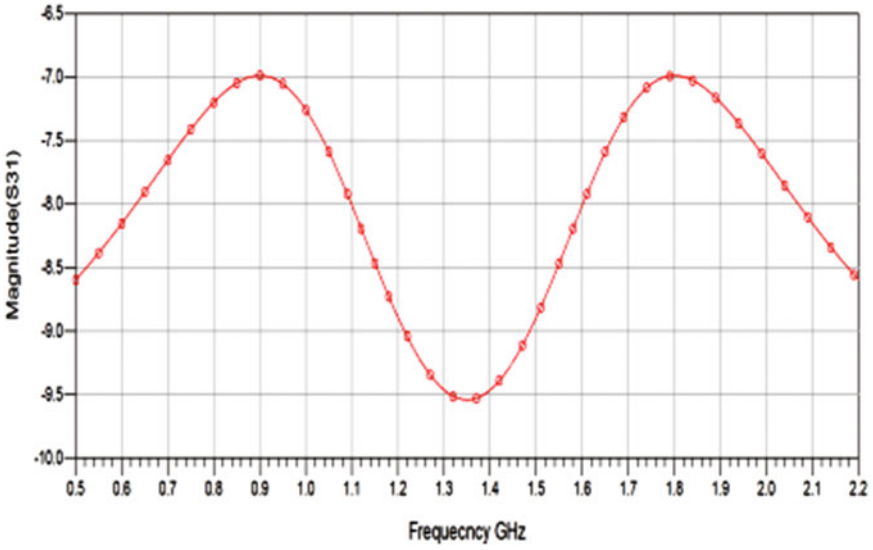


Fig. 13 Insertion loss

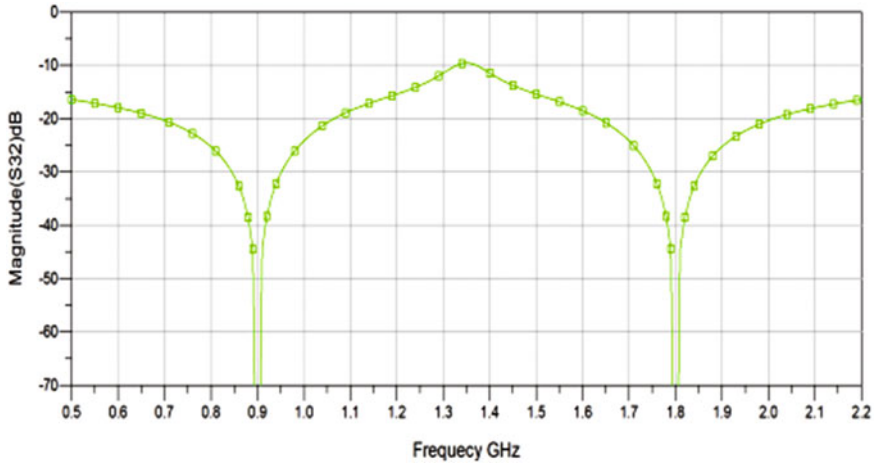


Fig. 14 Port isolation

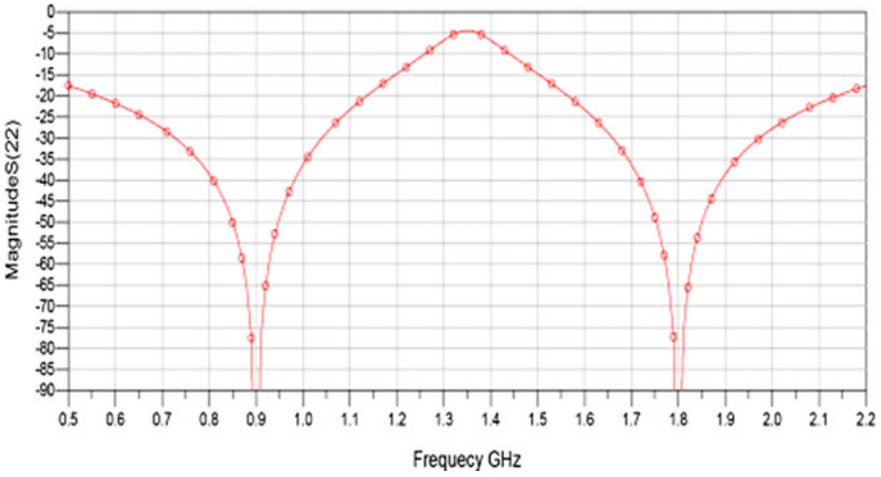


Fig. 15 Output return loss

5 Conclusion

A compact dual-band equal split N-way Wilkinson power divider for GSM has been presented in this paper. A novel architecture of the dual-band quarter wavelength transmission line transformer with design is also presented in this paper. The proposed DBQWTLT possesses wide bandwidth characteristics and compact in size as compared to the previous tactics. The proposed approach has been verified by simulating the dual-band equal split two-way- and five-way WPD in ADS.

The simulated results validated the proposed approach. The proposed circuit has good matching, equal split, and good output port isolation.

References

1. Wilkinson, E.J.: An N-way power divider. IRE Trans. Microwave Theory Tech. **8**, 116–118 (1960)
2. Pozar, D.M.: Microwave Engineering, 3rd edn. Wiley, New York (2005)
3. Taub, J.J., Fitzgerald, B.: A note on N-way hybrid power dividers (correspondence). IEEE Trans. Microwave Theory Tech. **12**(2), 260–261 (1964)
4. Srisathit, S., Chongcheawchamnan, M., Worapishet, A.: Design and realization of dual-band 3 dB power divider based on two-section transmission-line topology. IEE Electron. Lett. **39**(9), 723–724 (2003)
5. Cheng, K.-K.M., Wong, F.-L.: A new Wilkinson power divider design for dual band applications. IEEE Microw. Wireless Compon. Lett. **17**(9), 664–666 (2007)
6. Wu, Y., Liu, Y., Li, S., Yu, C., Liu, X.: Closed-form design method of an N-way dual-band wilkinson hybrid power divider. Prog. Electromagnet. Res. PIER **101**, 97–114 (2010)
7. Qaroot, A., Dib, N.: General design of N-way multi-frequency unequal split wilkinson power divider using transmission line transformers. Prog. Electromagn. Res. C **14**, 115–129 (2010)

Comparative Analysis of DC/DC Converters with MPPT Techniques Based PV System

S. Saravanan, N. Ramesh Babu and Padmanaban Sanjeevikumar

Abstract This paper focuses on the comparison of perturb and observe (P&O) and adaptive neuro-fuzzy inference system (ANFIS) based maximum power point tracking to track the optimum maximum power from PV system. This article also points out the performance of the boost converter and modified Single-Ended Primary-Inductor Converter (SEPIC) using above two techniques for PV. P&O and ANFIS techniques are used to generate duty cycle of DC/DC converters. The study is performed by using MATLAB/Simulink with the rating of 200 W PV and it has been observed that the modified SEPIC converter based ANFIS produces superior results compared with classical boost converter.

Keywords Maximum power point tracking · Adaptive neuro-fuzzy inference system · Perturb and observe · Photovoltaic · Boost converter

1 Introduction

Due to the increase of energy demand and huge expense of fossil fuel, the conventional energy source will not be capable for the production of power in the upcoming years. To overcome that the renewable energy based power generation is an eminent energy source, the renewable energy sources used are Photovoltaic (PV), fuel cell, and small wind turbines [1]. The PV-based power generations have become most prominent source for off-grid power generation. Many researches at

S. Saravanan · N. Ramesh Babu (✉)
School of Electrical Engineering, VIT University, Vellore, India
e-mail: nrameshbabu@vit.ac.in

S. Saravanan
e-mail: saravanansjncf@gmail.com

P. Sanjeevikumar
Department of Electrical and Electronics Engineering, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_28

present focus on this domain to improve the efficiency and to cultivate the maximum power effectively. The installation of PV system requires higher initial cost with less maintenance. The PV system mainly converts the solar energy into electricity and it mostly utilizes the irradiance and temperature. The solar power produced introduces disturbance due to changing climatic conditions. To enhance the generating powers from PV, Maximum Power Point Tracking (MPPT) techniques are used to track [2]. There are various MPPT techniques to track the optimal power from PV system, they are, hill climbing method, Perturb and Observe method [3], Incremental Conductance [4], Fuzzy Logic Controller, Neural Networks, Genetic Algorithms, Particle Swarm Optimization, Adaptive Neuro-Fuzzy Inference System and so on [5, 6].

PV-based energy has low voltage characteristic in nature to step up the voltage by using DC/DC converter as per the required application. The converter is used to generate the fixed output voltage for the load during environmental changing condition in the PV system. The converter depends on pulse for the switch according to that the boost up operation will perform which was generated from the MPPT technique [7]. The general block diagram of the PV-based converter using MPPT technique was shown in Fig. 1. When the PV source varies according to the climatic condition, the duty cycle is produced by tracking the optimum power using MPPT technique to the converter and voltage transfer to the loading condition.

This paper provides the study of PV system with P&O and ANFIS MPPT methods along with the usage of boost converter and modified SEPIC under changing irradiance conditions.

1.1 PV Panel Modelling

Solar cell is designed by connecting current source in parallel with pn junction diode which absorbs the irradiance and temperature of the solar energy and converts it into dc current [8]. When the cells are connected in series, it generates large voltage, whereas if it is connected in parallel, large current will be generated.

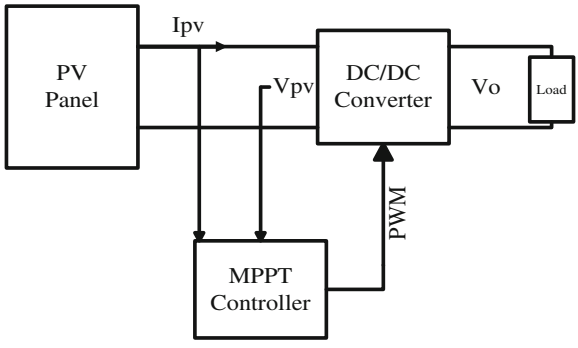


Fig. 1 A general overview of PV-based system

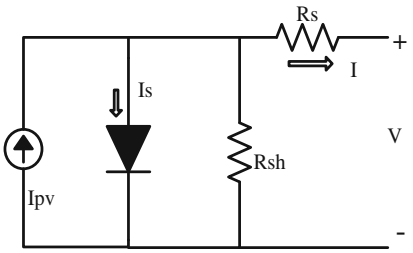


Fig. 2 Solar cell equivalent circuit

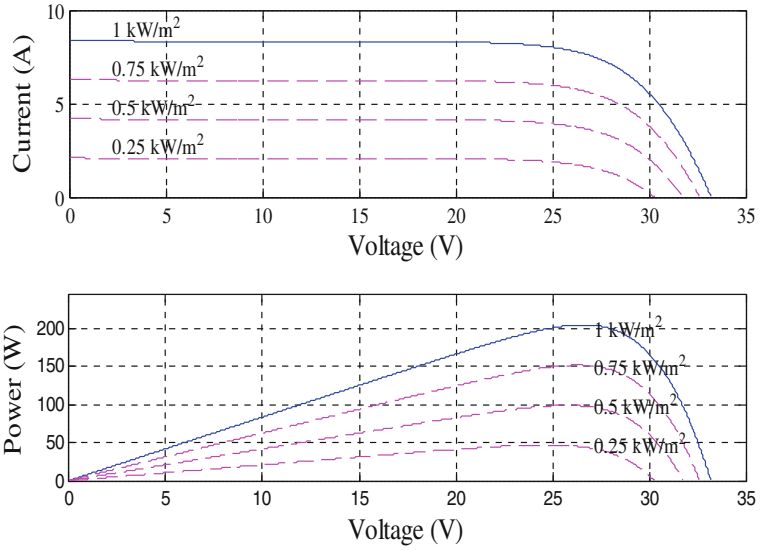


Fig. 3 I-V and PV characteristics of solar PV array

The equivalent circuit diagram of the single diode PV panel was shown in Fig. 2. The modelling of the solar cell is defined by voltage–current relationship of PV system as follows [9]:

$$I = I_{\text{pv}} - I_{\text{s}}\left(\exp\left(\frac{q(V + R_{\text{s}}I)}{N_{\text{s}}kTa}\right) - 1\right) - \frac{V + R_{\text{s}}I}{R_{\text{sh}}}, \tag{1}$$

where, I_{pv}—PV current (A), I_s—saturation current (A), q—the electron charge (1.60217×10^{-19} °C), k—Boltzmann constant (1.38065×10^{-23} J/K), a—diode ideality constant, R_{s} and R_{sh}—series and parallel resistances of cell (Ω), N_s—no. of cells in series, and T—temperature (K).

The relation between the power versus voltage and current versus voltage characteristics for different irradiance condition of the PV panel is shown in Fig. 3. From these characteristics, it is decided to incorporate a MPPT algorithm to track the optimum power and current by choosing appropriate duty cycle in the converter.

1.2 MPPT Modelling

1.2.1 Perturb and Observe Method

P&O based MPPT technique is one most commonly used because of its simple operation and efficiency. In this method, the PV voltage and current is measured by using sensor and calculate the power as the result is obtained. By comparing present power with previous power, the controller will choose the next perturbation size. According to the perturbation step size, the oscillations will increases or decrease and there should be an optimum step size with a tradeoff [10]. The duty cycle of the P&O method is computed by the voltage and power relationship as given in Eq. (2).

$$\frac{\mathrm{d}P}{\mathrm{d}V_{\mathrm{pv}}}(n) = \frac{P(n) - P(n-1)}{V_{\mathrm{pv}}(n) - V_{\mathrm{pv}}(n-1)} \tag{2}$$

The main demerits of this system are the oscillations around the maximum power point and the low tracking efficiency under rapidly changing environmental conditions.

1.2.2 ANFIS-Based MPPT Method

The combination of fuzzy logic control (FLC) and artificial neural network (ANN) is called as ANFIS. The neural networks controller is used to mapping the nonlinearity from the task and FLC used to deciding the output for the task by using correct fuzzy rules based on error and change in error. Because of the hybrid operation of FLC and ANN, the ANFIS becomes more precise in controlling part of the system by comparing other techniques [11].

The input 1 is the PV voltage and input 2 is the PV current and output is the duty cycle with the set of 1200 data for the DC/DC converter. Its operation is divided into five layers as shown in Fig. 4. The layer 1 is input layers and error (E) and change in error (CE) are sent to layer 2 which performs the fuzzification operation to produce the crisp fuzzy values. Layer 3 is a rule-based layer which tracks the output to input based on the match. The layer 4 is a normalization layer which strengthens the firing measured from a given rule. Layer 5 is defuzzification layer which converts fuzzy values to crisp values and produces the appropriate duty cycle to tune the MPPT to track the optimum point with more accuracy.

To train the ANFIS, the 1200 number of epochs with membership function of both input variables E and CE are 5 and 5. Therefore, total numbers of rules are 25 as shown in Fig. 5.

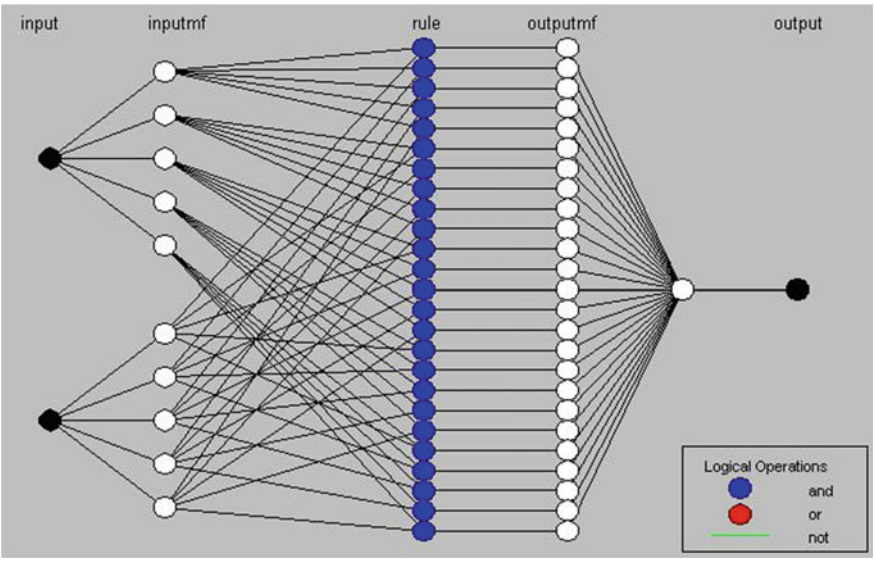


Fig. 4 Structure for ANFIS

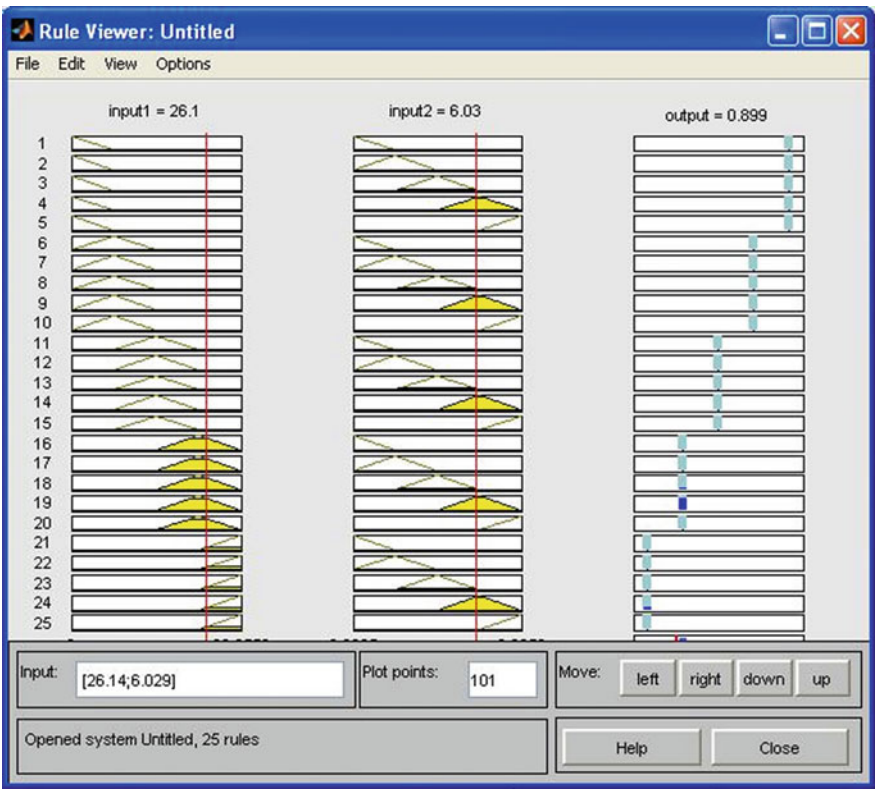


Fig. 5 Rule viewer with two inputs and an output

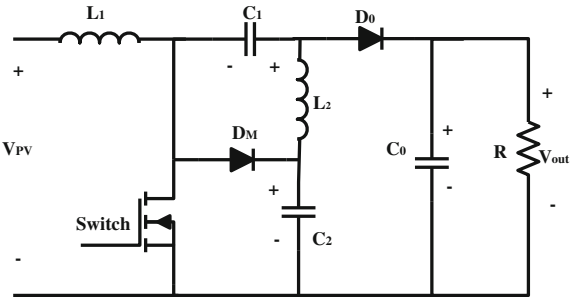


Fig. 6 Circuit diagram of a modified SEPIC

1.3 Modelling of DC/DC Converter

This paper compares both the boost converter topology [12] and modified SEPIC converter topology of the PV system using two MPPT methods. The two converters are used to generate high output voltage for the PV system and also it is validated under the constant temperature with varying irradiance conditions.

1.3.1 Modified SEPIC Converter

This converter operates by the combination of classical boost and SEPIC converter to generate the voltage gain. The converter used diode D_M and capacitor C_2 in the circuit as shown in Fig. 6. The circuit consists of a single switch, diodes D_0 and D_M, inductors L_1 and L_2 and capacitors C_1, C_2 and C_0 [13]. When the switch is in turned ON condition, the diode D_0 and D_M gets blocked condition and the charges are stored in inductors L_1 and L_2. The input current flows through inductor L_1 to the inductor L_2 through capacitors C_1 and C_2. When the switch is in turned OFF condition, the diode D_0 and D_M are in conduction mode and stored energy starts discharge from L_1. The current flows through capacitors C_1, C_2 and the inductor L_2 discharges the energy through diode D_0 to load. The parameter design equation of classical boost and modified SEPIC converters are tabulated in Table 1.

1.4 Implementation and Results

The detailed implementation of P&O and ANFIS based MPPT with DC/DC converters for PV systems are modelled and simulated using MATLAB/Simulink software. To validate the performance of MPPT algorithm, sudden changes in irradiance level of PV system is introduced and verified the performance. The P&O and ANFIS techniques produce the control pulse in accordance with the changes of irradiance occurred at the PV panel. The system is simulated with conventional boost and modified SEPIC converters.

Table 1 Equations for design of converters

Parameter	Boost converter	SEPIC
Switch duty cycle	$D = 1 - \frac{V_{in}}{V_{out}}$	$D = \frac{V_{out} - V_{in}}{V_{out} + V_{in}}$
Inductance	$L = \frac{V_{out} D}{\Delta i_L f}$	$L_1 = L_2 = \frac{V_{out} D}{\Delta i_L f}$
Capacitors	$C = \frac{D}{R(\Delta V_{out}/V_{out})f}$	$C_1 = C_2 = \frac{I_{out}}{\Delta V_C f}$, $C_0 = \frac{D}{R(\Delta V_{out}/V_{out})f}$

V_{out} is the output voltage, V_{in} is the input voltage, D is the duty cycle, f is the switching frequency, Δi_L is the inductor ripple current, and ΔV_C is the capacitor ripple voltage

Table 2 Converter parameters chosen for testing

Parameters	Boost converter	Modified SEPIC
Switching frequency (f)	24 kHz	24 kHz
Duty cycle (D)	0.9	0.82
L_1	195 µH	177.2 µH
L_2	–	177.2 µH
C_0	128 µF	115 µF
C_1 and C_2	–	2.24 µF
R	338 Ω	338 Ω

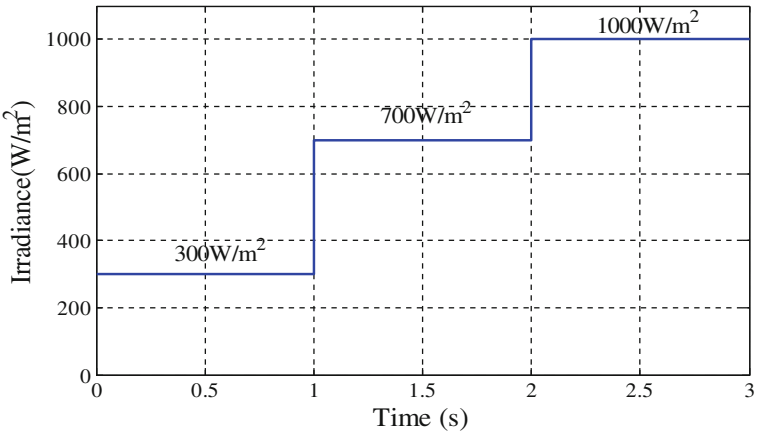


Fig. 7 Change in irradiance level of PV

For the analysis, both converters are designed for 200 W PV panel. The designed parameter values for both boost and modified SEPIC are tabulated in Table 2. By using the both MPPT techniques track the maximum power from the panel and generate the duty cycle for the converters. The performance of the MPPT techniques based on boost and modified SEPIC converters was compared by varying irradiance (300, 700, and 1000 W/m^2) with constant temperature (25 °C).

The varying irradiance for different time period is shown in Fig. 7. The output power of the boost converter based PV system is shown in Fig. 8. From the graph,

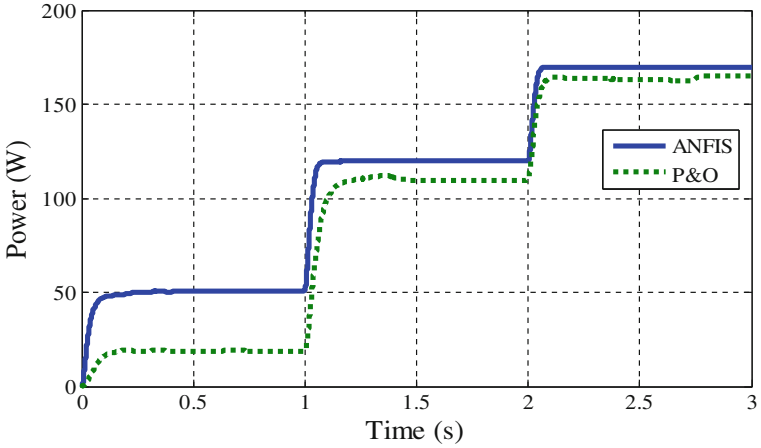


Fig. 8 Output power of PV based boost converter

Table 3 Comparison of maximum power for boost converter

MPPT techniques	Boost converter		
	300 W/m^2	700 W/m^2	1000 W/m^2
P&O	18.92 W	106.6 W	162.9 W
ANFIS	50.73 W	119.6 W	169.8 W

it is clearly shown that the ANFIS based boost converter produce maximum power than the P&O technique for PV system. The output power of boost converter based PV system with both MPPT technique is listed in Table 3. The maximum power generates around 169.8 W by ANFIS and 162.9 W by P&O based boost converter at standard irradiance (1000 W/m^2) and temperature (25 °C) condition. Compare to P&O based MPPT, the ANFIS technique generate maximum output power for PV with boost converter.

The output power of the modified SEPIC based PV system is shown in Fig. 9. From the result, we can observe that the ANFIS-based modified SEPIC converter produces maximum output power than the other MPPT technique. The maximum output power produced for modified SEPIC converter using two MPPT techniques is tabulated in Table 4. From the table, converter produces 174.9 W for ANFIS technique and 170.9 W for P&O technique. By comparing both Tables 3 and 4, we can find that the combination of modified SEPIC converter generates maximum output power for PV system.

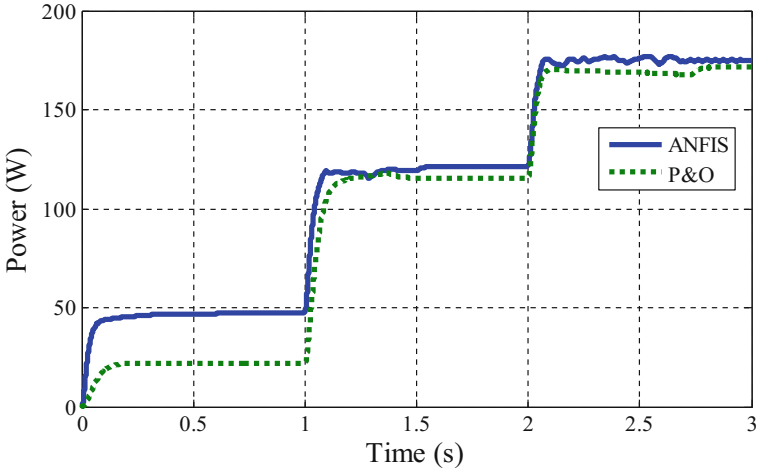


Fig. 9 Output power of PV based modified SEPIC converter

Table 4 Comparison of maximum power for modified SEPIC converter

MPPT techniques	Modified SEPIC		
	300 W/m^2	700 W/m^2	1000 W/m^2
P&O	21.75 W	115.5 W	170.9 W
ANFIS	47.47 W	121.4 W	174.9 W

2 Conclusions

In this paper, two MPPT methods namely P&O and ANFIS and converter circuits like boost and modified SEPIC were used to model PV system. The performances of the PV system with different combinations were analyzed under different irradiance and constant temperature condition for PV system. The simulated results cleared that the modified SEPIC converter based ANFIS techniques performs better than the conventional methods. Compared to boost converter, the modified SEPIC based MPPT techniques produces maximum output power.

References

1. Tiwari, R., Ramesh Babu, N.: Recent developments of control strategies for wind energy conversion system. Renew. Sustain. Energy Rev. **66**, 268–285 (2016)
2. Saravanan, S., Ramesh Babu, N.: Maximum power point tracking algorithms for photovoltaic system—A review. Renew. Sustain. Energy Rev. **57**, 192–204 (2016)
3. Lian, K.L., Jhang, J.H., Tian, I.S.: A maximum power point tracking method based on perturb-and-observe combined with particle swarm optimization. IEEE J. Photovoltaics **4**(2), 626–633 (2014)

4. Lin, C.-H., Huang, C.-H., Du, Y.-C., Chen, J.-L.: Maximum photovoltaic power tracking for PV array using the fractional-order incremental conductance method. Appl. Energy **88**(12), 4840–4847 (2011)
5. Jordehi, A.R.: Maximum power point tracking in photovoltaic (PV) systems: a review of different approaches. Renew. Sustain. Energy Rev. **65**, 1127–1138 (2016)
6. Lyden, S., Haque, M.E.: Maximum power point tracking techniques for photovoltaic systems: a comprehensive review and comparative analysis. Renew. Sustain. Energy Rev. **52**, 1504–1518 (2015)
7. Li, W., He, X.: Review of nonisolated high-step-up DC/DC converters in photovoltaic grid-connected applications. IEEE Trans. Power Electron. **58**(4), 1239–1250 (2011)
8. Sera, D., Teodorescu, R., Rodriguez, P.: PV panel model based on datasheet values. In: Proc. IEEE. ISIE, pp. 2392–2398 (2007)
9. Villalva, M.G., Gazoli, J.R., Filho, E.R.: Comprehensive approach to modeling and simulation of photovoltaic arrays. IEEE Trans. Power Electron. **24**(5), (2009)
10. Abdelsalam, A.K., Massoud, A.M., Ahmed, S., Enjeti, P.N.: High-performance adaptive perturb and observe mppt technique for photovoltaic-based microgrids. IEEE Trans. Power Electron. **26**(4), 1010–1021 (2011)
11. Cheired, F., Mellit, A., Kaliogiru, S.A., Larbas, C.: Intelligent maximum power point trackers for photovoltaic applications using FPGA chip: a comparative study. Sol. Energy **101**, 83–99 (2014)
12. Sanjeevikumar, P., Grandi, G., Blaabjerg, F., Wheeler, P., Siano, P., Hammami, M.: A comprehensive analysis and hardware implementation of control strategies for high output voltage dc-dc boost power converter. Inter. J. of Comput. Intelli. Sys. (IJCIS), Atlantis Press and Taylor and Francis publications, 2 Sept 2016. (Accepted for publication and in Press)
13. Saravanan, S., Ramesh Babu, N.: RBFN based MPPT algorithm for PV system with high step up converter. Energy Convers. Manag. **122**, 239–251 (2016)

Single Phase Asymmetric Switched-Inductor Quasi-Z-Source CHB Multilevel Inverter

G. Prem Sunder, B. Shanthi, Alamelu Nachiappan, S.P. Natarajan and Padmanaban Sanjeevikumar

Abstract Asymmetric Switched-Inductor Quasi-Z-Source Cascaded H-Bridge Multilevel Inverter (A-SL-qZS-CHB-MLI) with seven-level high-boosted load voltage is discussed in this article. Each unit of the proposed A-SL-qZS-CHB-MLI is comprised of a Quasi-Z-Source (qZS) network with SL cell and H-Bridge unit. The SL cell is formed with three diodes and two inductors. The qZS network facilitates the operation of shoot-through (ST) state control to provide boosted output voltage. The inclusion of SL cell increases the boosted output for the same ST duty ratio as compared with conventional qZS-CHB-MLI. The performance analysis of this topology in connection with THD for load voltage obtained from simple boost control and multicarrier PWM method is presented. Simulation results obtained from the proposed A-SL-qZS-CHB-MLI reveals high boost output voltage with reduced THD as compared with the traditional qZS-CHB-MLI.

G. Prem Sunder (✉)
Department of Electrical and Electronics Engineering, Mailam Engineering College, Mailam, Tamil Nadu, India
e-mail: premgsunder@gmail.com

B. Shanthi
Centralized Instrumentation and Service Laboratory, Annamalai University, Chidambaram, Tamil Nadu, India
e-mail: au_shan@yahoo.com

Alamelu Nachiappan
Department of Electrical and Electronics Engineering, Pondicherry Engineering College, Pondicherry, India
e-mail: nalam63@pec.edu

S.P. Natarajan
Department of Electronics and Instrumentation Engineering, Annamalai University, Chidambaram, Tamil Nadu, India
e-mail: spn_annamalai@rediffmail.com

P. Sanjeevikumar
Department of Electrical and Electronics, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_29

Keywords Quasi-Z-Source network · Switched-inductor cell · CHB-MLI Simple boost control · Multicarrier PWM · THD

1 Introduction

In recent research works, many of the researches focused on renewable energy power generation systems. Unfortunately, the input voltage obtained from the renewable energy sources is sometimes low, discontinuous and affected by the environment. Multilevel inverters are effectively employed in power-conversion systems for high-power applications [1, 2]. The CHB multilevel inverters are readily utilized in renewable energy applications as it provides output voltage with reduced THD using multiple input dc voltage sources.

The CHB-MLI has reduced number of switches in its configuration as compared with diode-clamped- and capacitor-clamped MLIs for a given number of voltage levels [3]. The CHB-MLIs can only provide the summation of the input voltages, but have no voltage boosting capability. Impedance-source networks (Z-Source networks) are extensively used to increase boost ability of the inverters. Quasi-ZS network is the improvement of the ZS network for providing improved reliability as well as to provide continuous input current. The ZS and q-ZS network fed inverters have remarkable applications in grid-connected distributed energy systems [4, 5]. The limits allied with the ZSI such as increased voltage stress applied on capacitors, discontinuous input current, and no common ground between the CHB inverter and dc source can be undertaken with the progress of q-ZS-MLI [6]. The SL-qZS-MLI affords an extended boosted dc-link voltage with the recompenses of common ground with the dc source as well as continuous input current. Productive advantages can be obtained by including the SL-QZS network in the CHB-MLI. Hence, the SL-qZS-CHB-MLI provides buck as well as boost functionality. This incorporation allows extended boost load voltage and power conversion concurrently in one stage by utilizing ST states. Introduction of SL cell in the qZS inverter formed a topology, which provided a higher boost factor as explained in [7, 8]. The ST states can be generated by simple boost control, maximum boost control and constant boost control techniques [9–16]. The SL cell makes it possible to operate the proposed topology with high value of modulation index, thus reducing the switching device voltage stress. The proposed topology significantly reduces the ST time which results in decreased switching loss and improved efficiency. Analysis on the performance of the A-SL-qZS-CHB-MLI with seven-level output voltage provides outstanding performance with combined advantages of the SL cell, qZS network and the H-Bridge cell. The simulated results of the A-SL-qZS-CHB-MLI were obtained using MATLAB. Figure 1 shows the traditional qZS-CHB-MLI and its qZS network consisting of inductors L_1, L_2, diode D_1 and capacitors C_1, C_2. In this traditional topology, qZ source network shares the common ground with

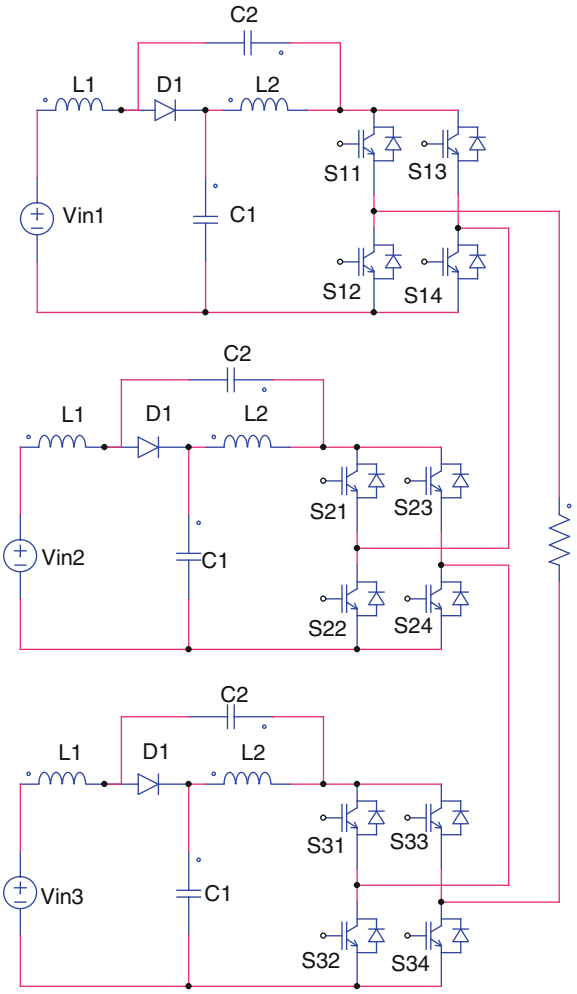


Fig. 1 Traditional qZS-CHB-MLI

inverter, and draws continuous input current from the dc source. The boost factor of the qZS-CHB-MLI is given in (1)

$$\textit{Boost factor},\ B = \frac{V_{\text{dc}}}{V_{\text{in}}} = \frac{1}{(1 - 2D_{\text{sh}})} \tag{1}$$

The A-SL-qZS-CHB-MLI topology is given in Sect. 2. The simple boost control of the proposed is explained in Sect. 3. The simulation results were depicted in Sect. 4, which elucidates the output voltage with THD. The conclusion is given in Sect. 5.

2 Asymmetric SL-qZ-Source CHB-MLI

The proposed A-SL-qZS-CHB-MLI for generating seven-level load voltage is as depicted in Fig. 2. The proposed topology consists of a SL-qZS network with SL cells, and H-Bridge unit. The SL cell consists of diodes D_2, D_3, D_4 and inductors L_2, L_3. The SL-qZS network affords the common ground point with the CHB inverter.

The SL cells increases the voltage boost functionality for the A-SL-qZS-CHB-MLI topology with addition of only three diodes and one inductor. The A-SL-qZS-CHB-MLI operation is explained with non-ST and ST states. The mode diagram of the non-ST state is shown in Fig. 3 and that of the ST state is shown in Fig. 4. In the non-ST state, the diode D_1, D_4 are forward biased, while D_2, D_3 are

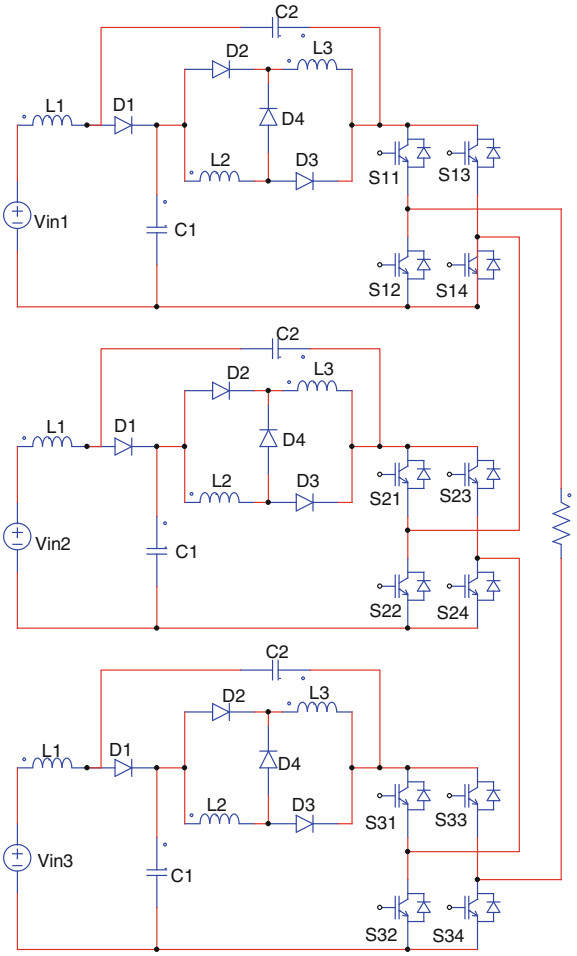


Fig. 2 Proposed seven-level asymmetric SL-qZS-CHB-MLI

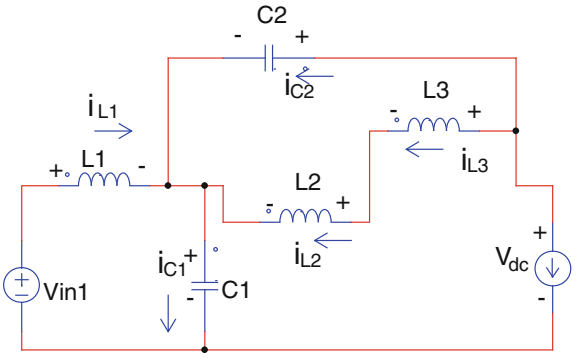


Fig. 3 Non-shoot-through state of the proposed topology

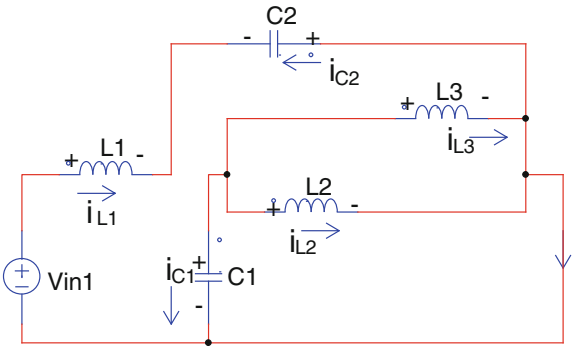


Fig. 4 Shoot-through state of the proposed topology

reverse biased which connects L_2 and L_3 in series. The energy is transferred from the input dc source to the CHB-MLI through the inductors L_1, L_2, L_3 and at the same time the capacitors C_1, C_2 are charged. In the ST state, the inverter side is shorted due to the cross-conduction of switching devices in any leg.

During the ST state, D_1 and D_4 are reverse biased, while D_2 and D_3 are turned on which connects the inductors L_2, L_3 in parallel, discharges the capacitors C_1, C_2 and stores energy in inductors L_1, L_2, L_3.

The value of the voltage across capacitor C_1 is given in (2)

$$V_{C_1} = \frac{1 - D_{\text{sh}}}{1 - 2D_{\text{sh}} - D_{\text{sh}}^2} V_{\text{in}} \tag{2}$$

The value of the voltage across capacitor C_2 is given in (3)

$$V_{C_2} = \frac{2D_{\text{sh}}}{1 - 2D_{\text{sh}} - D_{\text{sh}}^2} V_{\text{in}} \tag{3}$$

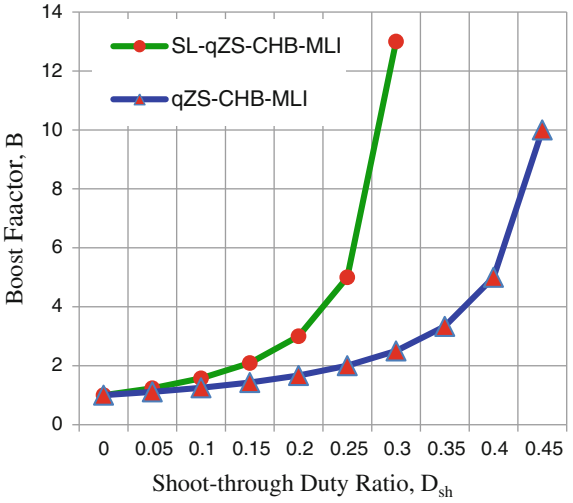


Fig. 5 The relationship of B with ST duty ratio for qZS-MLI and A-SL-qZS-CHB-MLI using simple boost control

The dc-link voltage is given in (4)

$$v_{\mathrm{DC}} = V_{C_1} + V_{C_2} = \frac{1 + D_{\mathrm{sh}}}{1 - 2D_{\mathrm{sh}} - D_{\mathrm{sh}}^2} V_{\mathrm{dc}} = BV_{\mathrm{dc}} \tag{4}$$

The value of AC load voltage depends on the Modulation Index (M) and B as provided in (5)

$$v_{\mathrm{ac}} = M \cdot B \cdot \frac{V_{\mathrm{dc}}}{2} \tag{5}$$

Figure 5 shows the B versus D_{sh} for A-SL-qZS-CHB-MLI and qZS-CHB-MLI topologies. The boost functionality of the A-SL-qZS-CHB-MLI topology is extended more than that of the traditional topologies.

3 Simple Boost Control of the Proposed A-SL-qZS-CHB-MLI

ST states can be generated by simple, maximum and constant boost control techniques. The ST states provide buck, boost and extended boost operations of the proposed topology. Switching signals for the proposed topology are produced by using Phase Disposition Pulse Width Modulation (PD-PWM) technique. In this paper, the simple boost control method is applied for introducing ST states in the

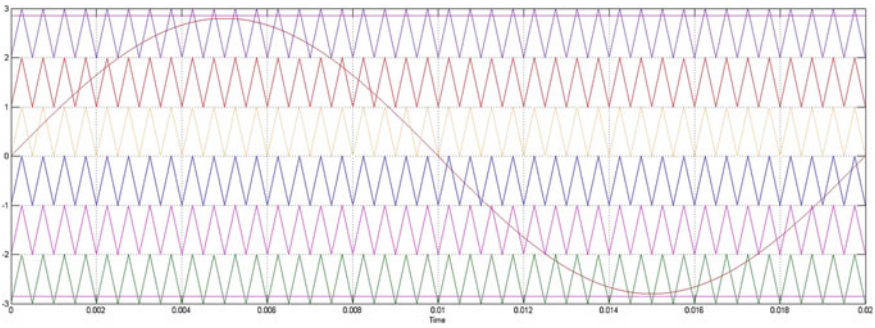


Fig. 6 Phase Disposition PWM scheme (PD-PWM)

generated pulses from PD-PWM technique by varying ST duty cycle. The simple boost technique produces the ST states by using two constant control signals, where the amplitude of the control signal is compared with the carrier signal above the peak value of the modulating reference signal. The reference signal, the carrier signals, and constant lines for simple boost control technique are shown in Fig. 6.

The ST duty ratio for this case is given in (6)

$$D_{\text{sh}} = \frac{T_{\text{sh}}}{T} = 1 - M \tag{6}$$

The correlation between M and D_{sh} is given in (7)

$$M < 1 - D_{\text{sh}} \tag{7}$$

The B of the A-SL-qZS-CHB-MLI is shown in (8)

$$B = \frac{1 + D_{\text{sh}}}{1 - 2D - D_{\text{sh}}^2} \tag{8}$$

The proposed topology requires lower ST duty ratio when compared with qZS-MLI for attaining the same boost gain. This advantage of the proposed topology facilitates the larger improvement in the output voltage. Figure 7 shows the voltage gain G versus M characteristics of the proposed topology, and it is observed from the plot that the G increases for the higher M as compared with conventional qZS-MLI.

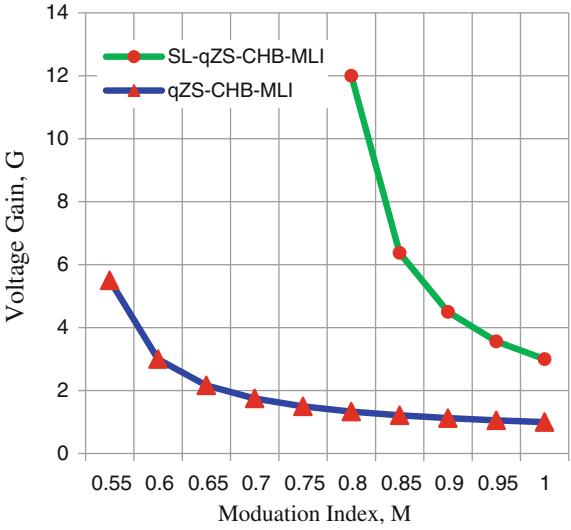


Fig. 7 Relationship of voltage gain with modulation index for qZS-MLI and A-SL-qZS-CHB-MLI using simple boost control

Table 1 Performance indices of the simulated output voltage

S. No.	Duty ratio D_{sh} (%)	Boost factor $B = \frac{(1+D_{sh})}{(1-2D_{sh}-D_{sh}^2)}$	Simulated output voltage		
			THD (%)	$V_{rms\text{-}fundamental}$ (V)	$V_{peak\text{-}fundamental}$ (V)
1.	5	1.2	22.02	286.8	405.6
2.	10	1.39	21.59	293.8	415.6

4 Simulation Results

Simulation study using MATLAB software is carried for the proposed new asymmetric SL-qZS-CHB-MLI topology. The simulation parameters are given as: inductors, $L_1 = L_2 = L_3 = 40$ mH and capacitors, $C_1 = C_2 = 6000$ µF, switching frequency $f_s = 5$ kHz, the input voltage $V_{in1} = V_{in2} = V_{in3} = 100$ V and resistive load, R-load = 50 Ω.

Table 1 displays the three important performance indices namely V_{rms} (fundamental), V_{peak} (fundamental) and % THD of simulated output voltage of asymmetric SL-quasi-Z-Source fed seven-level CHB inverter for $D_{sh} = 5$ and 10%.

Figure 8 shows sample output voltage waveform for ST duty ratio $D_{sh} = 10\%$ and the corresponding THD spectrum is presented in the Fig. 9.

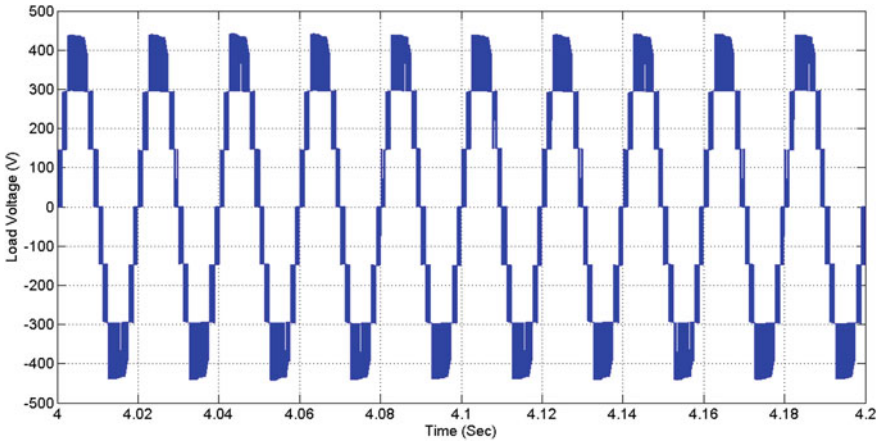


Fig. 8 Simulated sample output voltage wave form of the asymmetric SL-qZ-source fed CHB seven level inverter (D_{sh} = 10%)

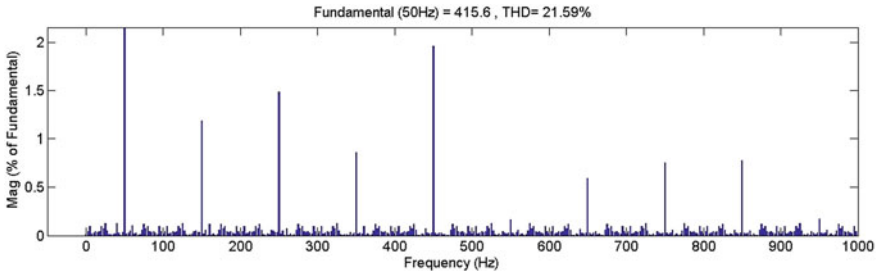


Fig. 9 FFT plot of the simulated output voltage (D_{sh} = 10%)

5 Conclusion

The performance analysis of the A-SL-qZS-CHB-MLI topology with extended boost capability is presented in this paper. The boosted output voltage and the THD of the proposed topology for 5 and 10% shoot-through duty ratio are presented with the simulated results using MATLAB. The simulation results ensure reduced THD and boosted load voltage for the proposed seven-level topology. This topology can be effectively applied for renewable energy power-conversion systems such as photovoltaic and/or wind power-conversion system.

References

1. Rodriguez, J., Lai, J.-S., Peng, F.Z.: Multilevel inverters: a survey of topologies, controls, and applications. IEEE Trans. Ind. Electron. **49**(4), 724–738 (2002)
2. Sanjeevikumar, P., Blaabjerg, F., Wheeler, P., Ojo, O.: Three-phase multilevel inverter configuration for open-winding high power application. In: conference proceedings, of the 6th IEEE international symposium on power electron. For distributed generation systems, pp. 22–25, IEEE-PEDG'15, Aachen (Germany) (2015)
3. Rodriguez, J., Bernet, S., Wu, B., Pontt, J.O., Kouro, S.: Multilevel voltage source converter topologies for industrial medium voltage drives. IEEE Trans. Ind. Electron. **54**(6), 2930–2945 (2007)
4. Zhu, M., Kun, Y., Luo, F.L.: Switched inductor z-source inverter. IEEE Trans. Power Electron. **25**(8), 2200–2210 (2010)
5. Anderson, J., Peng, F.Z.: A class of quasi-Z-source inverters. In: Conference record IEEE IAS annual meeting, Edmonton, Alta, Canada, pp. 1–7 (2008)
6. Nguyen, M.K., Lim, Y.C., Cho, G.B.: Switched inductor quasi Z-source inverter. IEEE Trans. Power Electron. **26**(11), 3183–3191 (2011)
7. Adamowicz, M., Strzelecki, R.: Boost-buck inverters with cascaded qZ-type impedance networks. Electr. Rev. **86**, 370–375 (2010). ISSN 0033-2097
8. Peng, F.Z., Shen, M., Qian, Z.: Maximum boost control of the Z-source inverter. IEEE Trans. Power Electron. **20**(4), 833–838 (2005)
9. Shen, M.S., Wang, J., Joseph, A., Peng, F.Z., Tolbert, L.M., Adam, D.J.: Constant boost control of the Z-source inverter to minimize current ripple and voltage stress. IEEE Trans. Ind. Appl. **42**(3), 770–778 (2006)
10. Sun, D., Ge, B., Zhang, H., Yan, X., Bi, D., Abu-Rub, H., Peng, F.Z.: An energy stored quasi-z source cascaded multilevel inverter based photovoltaic power generation system. IEEE Trans. Indus. Electron. **62**(9), 5458–5467 (2015)
11. Du, Z., Ozpineci, B., Tolbert, L.M.: Modulation extension control of hybrid cascaded H-bridge multilevel converters with 7-level fundamental frequency switching scheme. In: Proceedings IEEE Power Electronics Specialists Conference, pp. 2361–2366 (2007)
12. Veenstra, M., Rufer, A.: Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives. IEEE Trans. Ind. Appl. **41**(2), 655–664 (2005)
13. Vinnikov, D., Jalakas, T., Roasto, I., Agabus, H., Tammet, K.: Method of shoot-through generation for modified sine wave Z-source, quasi-Z-source and trans-Z-source inverters. WIPO patent WO2012/116708A2 (2012)
14. Sanjeevikumar, P., Blaabjerg, F., Wheeler, P., Khanna, R., Mahajan, S.B., Dwivedi, S.: Optimized carrier based five-level generated modified dual three-phase open-winding inverter for medium power application. Conf. Prof. of IEEE International Transportation Electrification Conference and Expo, Asia-Pacific, (IEEE-ITEC'16), Busan (Korea), pp. 40–45 (2016)
15. Liu, Y., Ge, B., Peng, F.Z., Haitham, A.R., Almeida, A.T. de., Ferreira, F.J.T.E.: Quasi-Z-source inverter based PMSG wind power generation system. In: IEEE Energy Conversion Congress and Exposition (ECCE), pp. 291–297 (2011)
16. Sun, D., Ge, B., Bi, D., Peng, F.Z.: Analysis and control of quasi-Z source inverter with battery for grid-connected PV system. Electr. Power Energy Syst. **46**, 234–240, (2012)

Buck–Boost LED Driver with Dimming Characteristics

R. Gunabalan, D.R. Binu Ben Jose and Padmanaban Sanjeevikumar

Abstract Light Emitting Diode (LED) lighting plays a major role nowadays in industry and commercial applications. An efficient control technique is introduced for low power LED lighting with dimming characteristics. The driver circuit consists of a simple buck–boost converter with dc input voltage. The dimming characteristics are achieved by relating a low and high frequency control signal in order to eliminate flickering and colour shift. Software implementation is performed in MATLAB-simulink for a power rating of 10 W and tested under diverse brightness conditions. The simulation results demonstrate that dimming can be achieved with high efficiency.

Keywords Buck–boost converter · LED lighting · Pulse width modulation LED dimming

1 Introduction

Light emitting diode market is increasing day by day and preferred for low power flash light to medium power street light applications because of its longer life [1], no poisonous content (mercury free) [2], pollution free with high efficiency, low voltage operation, high colour rendering index, maintenance free, no requirement of ballast, low heat emission, easy dimming and high efficacy (lm/W) [3, 4]. The operational lives of LED bulbs can be determined by the driving technique and

R. Gunabalan · D.R. Binu Ben Jose
School of Electrical Engineering, Vellore Institute of Technology (VIT) University, Chennai, India
e-mail: gunabalan.r@vit.ac.in

D.R. Binu Ben Jose
e-mail: binuben.jose@vit.ac.in

P. Sanjeevikumar (✉)
Department of Electrical and Electronics Engineering, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_30

operating temperatures. The voltage and current ratings of LED lighting is entirely different from the rest of lighting devices. The voltage rating of LED lighting depends on the number of LEDs connected in series and the current ratings vary from 100 mA to 5 A. The typical current value of single LED for lighting applications is 350 mA. LEDs are current controlled devices and to retain constant current, the LED driver circuits are intended to work in continuous conduction mode [5]. LED dimming is necessary in street light applications during off-peak period and very low power applications such as the backlight for smart phones and flashlights [6]. Dimming of LEDs is adopted by varying the current through them. Both analog and digital (PWM) dimming methods regulate the LED drive current, which is proportional to the light output.

Simple pulse width modulation (PWM) dimming circuits were employed to avoid flickering and colour shift in LED lighting with a low frequency range of 120–480 Hz for a fundamental frequency of 60 Hz [7]. Digital dimming using low frequency pulse width modulation to avoid chromaticity shift problem was studied and experimentally verified for a frequency of 200 Hz [8]. High frequency series power dimming was proposed for slow dynamic converters achieving good power factor and total harmonic distortion [9]. A double PWM (DPWM) low frequency gate driver circuit was adopted to regulate the average current and its amplitude to stop the LED lighting from colour swing [10]. The biological effects of flickering effect of dimming LED lighting at low frequencies are discussed in detail in case of car taillights [11]. In this proposed work, double PWM method is incorporated with simple buck–boost converter to drive the LED by a pulsed current for better efficiency and low current ripple and it is compared with the high frequency PWM dimming technique.

2 DPWM Buck–Boost Converter

The configuration of buck–boost converter for LED lighting with dimming characteristics was employed in [12] where the average voltage and current through the LED was varied by adjusting the duty cycle of high frequency signal. DPWM control method for dimming feature was proposed to improve the performance of

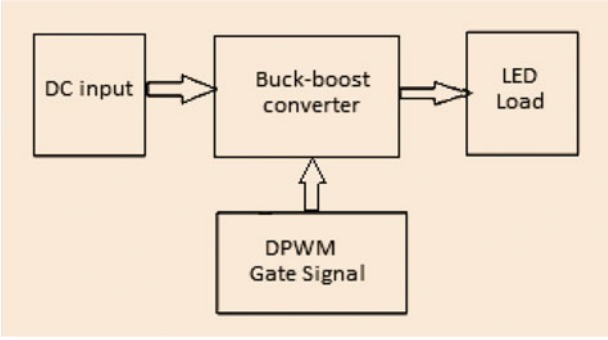


Fig. 1 Block diagram of buck–boost converter with DPWM method

the existing dc–dc buck–boost converter. The block diagram representation of the buck–boost dc–dc converter is shown in Fig. 1.

The circuit diagram of the buck–boost converter is shown in Fig. 2. The circuit is formed by a dc voltage source, ideal semiconductor switch, inductor, free-wheeling diode and filter capacitor (Fig. 3).

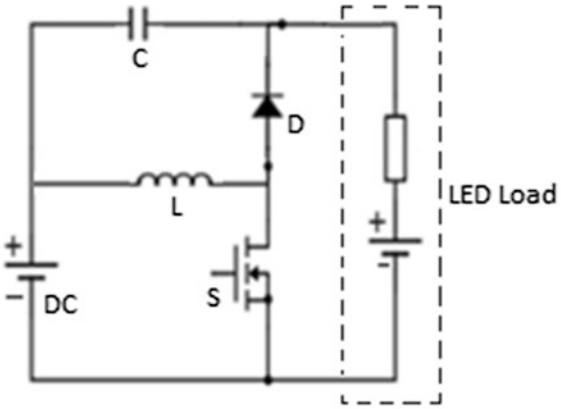


Fig. 2 Buck–boost converter LED driver

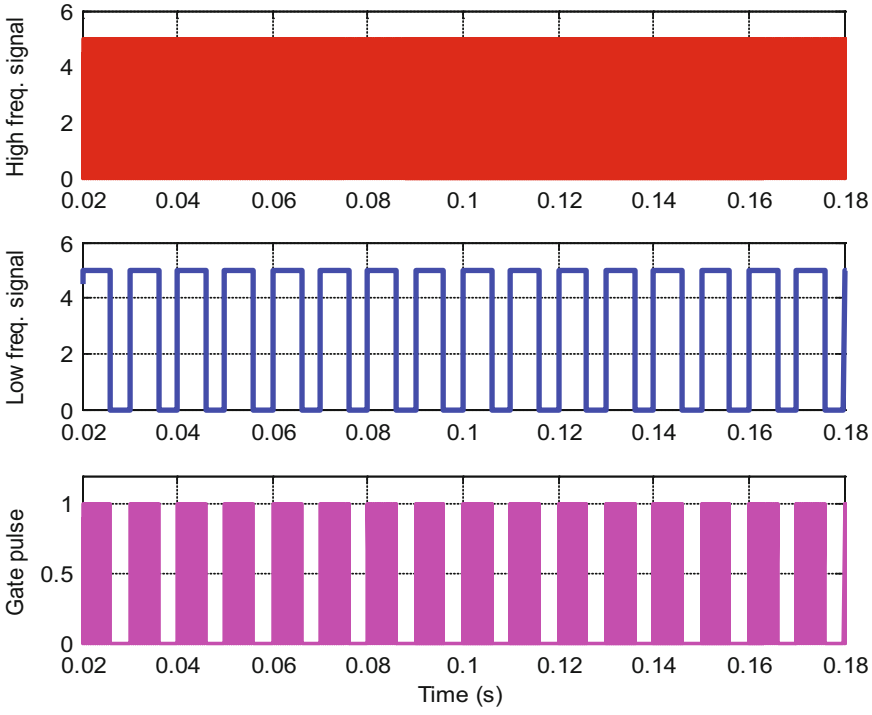


Fig. 3 Double pulse width modulation control signal for LED driver

3 Results and Discussions

The control signal for the switch is generated by a combination of 50 kHz high frequency and 100 Hz low frequency signal for dimming. The converter is operated in discontinuous conduction mode during dimming mode and LEDs are in on state when the low frequency PWM signal is in high state. The magnitude and the average current of the LED lighting are controlled by high and low frequency signals respectively. The circuit variables are designed for an input voltage of 12 V. The LED load is designed for an output voltage of 24 V at maximum brightness conditions with 350 mA. The load has a string of eight LEDs connected in series and the rating of each LED is 3 V and 350 mA. The designed circuit parameters and specifications are given in Table 1.

The buck–boost converter circuit is designed to operate for a minimum current of 8.22 mA to the rated current of 350 mA by varying the pulse width of high frequency signal from 23.75 to 52% for SPWM dimming. The average output voltage variation is from 20.44 to 24 V. In DPWM dimming, the pulse width of high frequency signal is maintained at 52% which is the maximum value to obtain the rated voltage (24 V) in SPWM and the duty cycle of low frequency signal is varied from 16.5 to 69% for a current of 8.22–262 mA (3/4th of the rated current). The average output voltage varies from 20.45 to 22.98 V. It is evident that smaller variations of output voltage across LEDs made large impact in its current and the brightness.

The key waveforms of the PWM techniques are presented in Figs. 4 and 5 for a minimum load current of 8.22 mA. In single PWM method, the amplitude as well as the average current of the LED is controlled whereas in double PWM, the amplitude (peak value) is maintained constant and the average current is controlled. Current is discontinuous in both switching methods. The switching and conduction losses are less in DPWM but the switching stress is high during the initial period.

The voltage and current waveforms are attained for half the rated current of 175 mA in single and double PWM method and are depicted in Figs. 6 and 7. The current through the inductor, LED, switch, diode and capacitor are observed. Current is continuous in SPWM and discontinuous in DPWM and reduces the conduction losses for the same load current. The rated current of 350 mA is

Table 1 Specifications of buck–boost converter

Parameters	Values
Input voltage	12 V
Output voltage	24 V
Output current	350 mA
Inductance	110 µH
Capacitance	10 µF

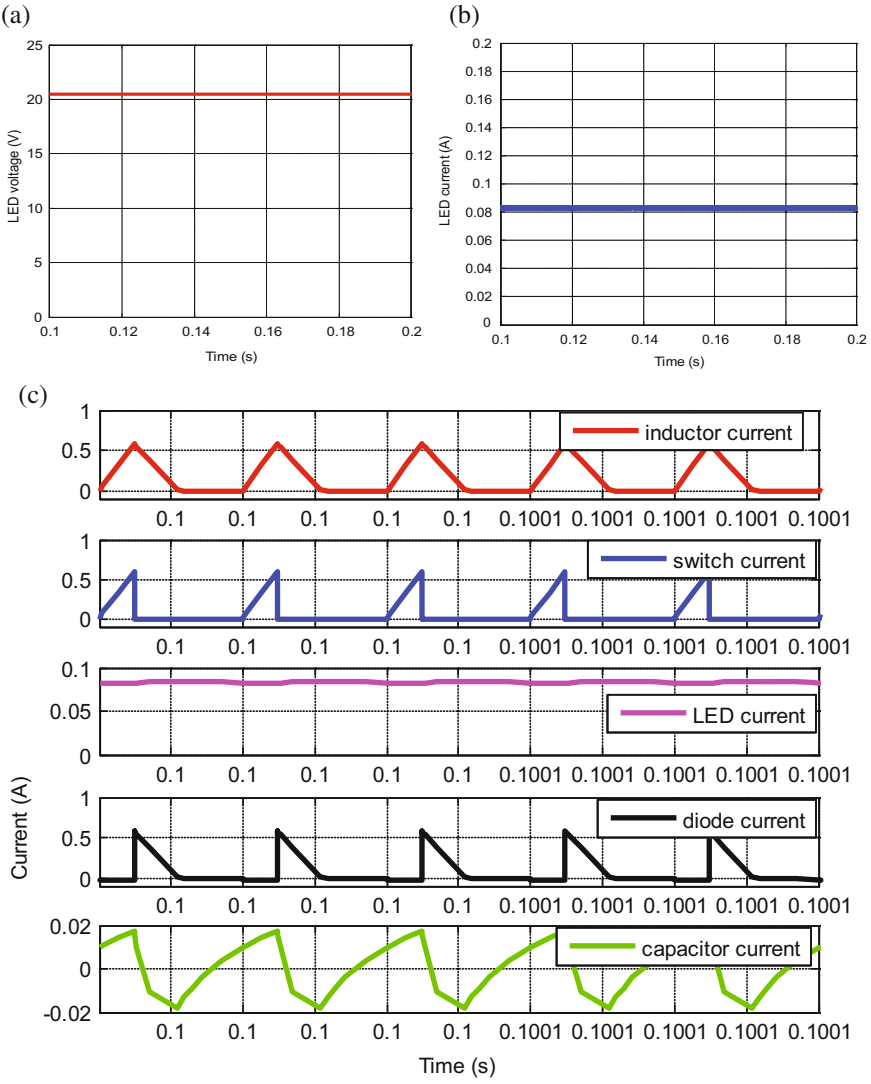


Fig. 4 Simulation results in LED dimming with minimum current with SPWM method. **a** LED voltage. **b** LED current. **c** Current waveforms through inductor, switch, LED, diode and capacitor

achieved by operating the switch in continuous conduction in SPWM as dimming is not required. The corresponding waveforms are illustrated in Fig. 8. The efficiency of the control techniques are calculated for different load currents and are given in Table 2. The efficiency of DPWM is better at low dimming current and high brightness state.

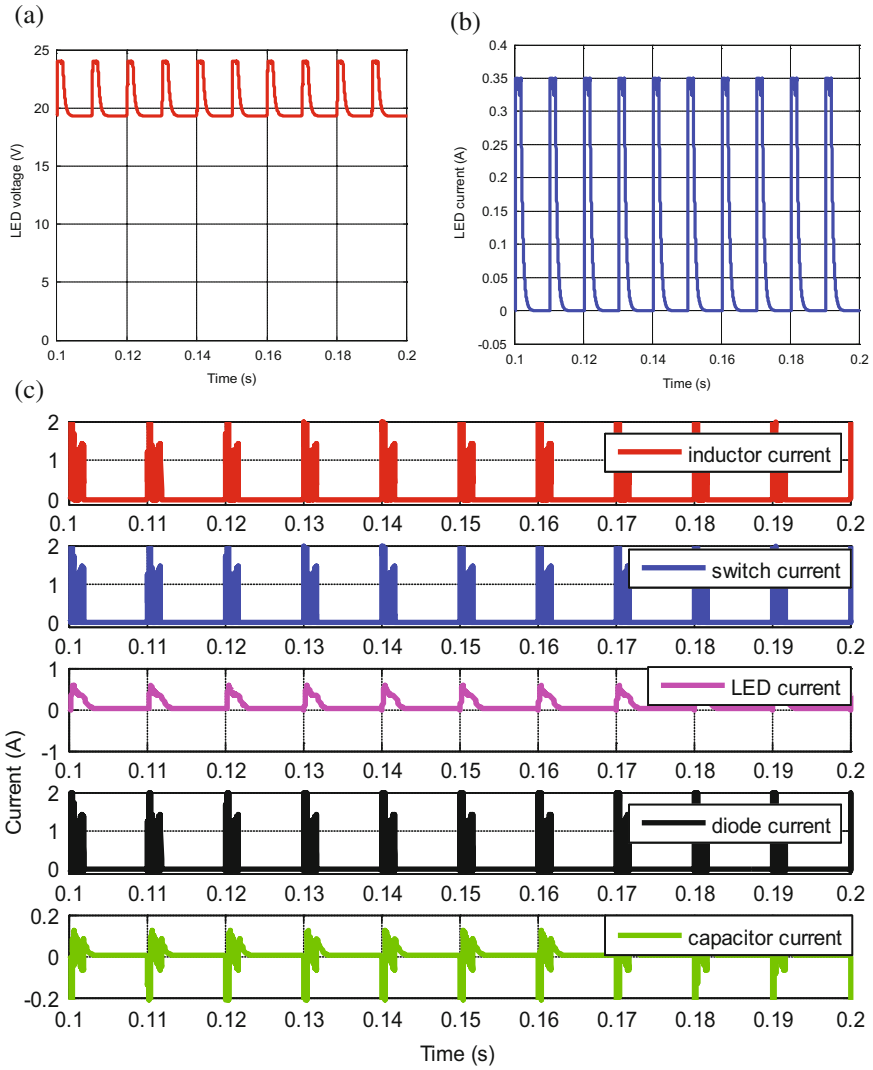


Fig. 5 Simulation results in LED dimming with minimum current with DPWM method. **a** LED voltage. **b** LED current. **c** Current waveforms through inductor, switch, LED, diode and capacitor

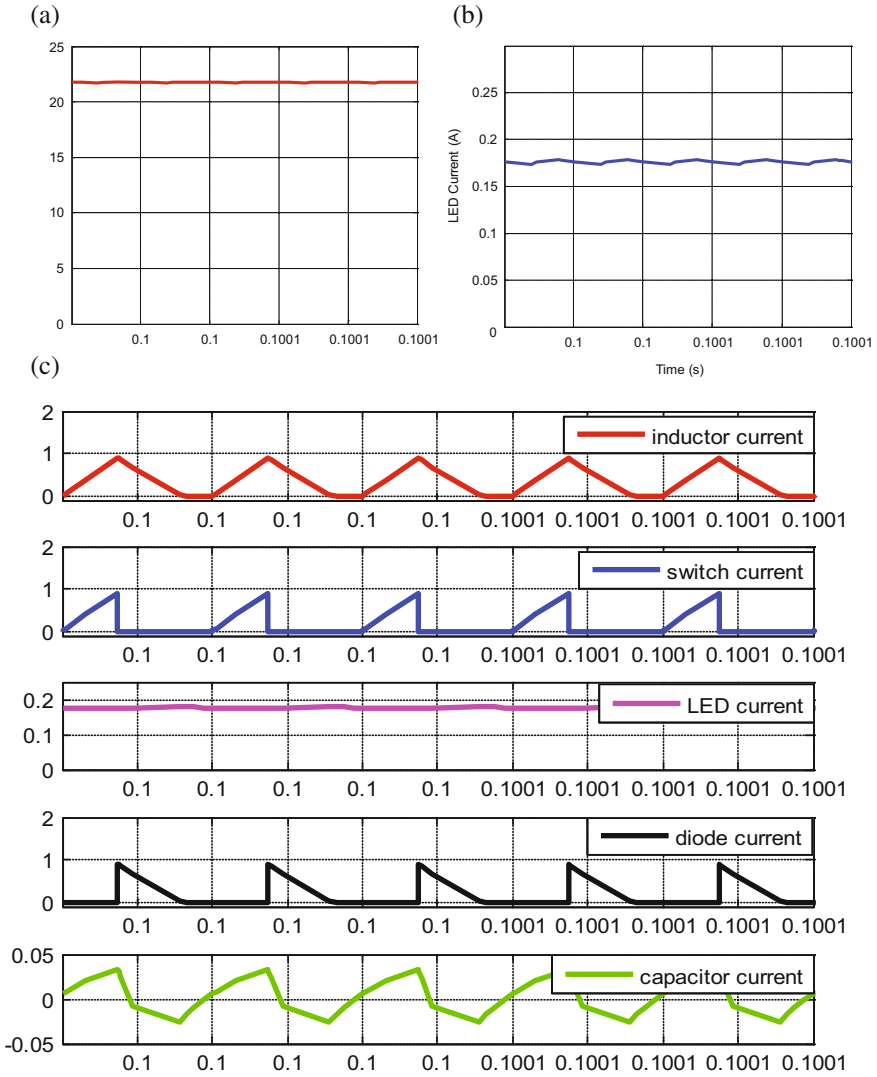


Fig. 6 Simulation results in LED dimming with half the rated current with SPWM method. **a** LED voltage. **b** LED current. **c** Current waveforms through inductor, switch, LED, diode and capacitor

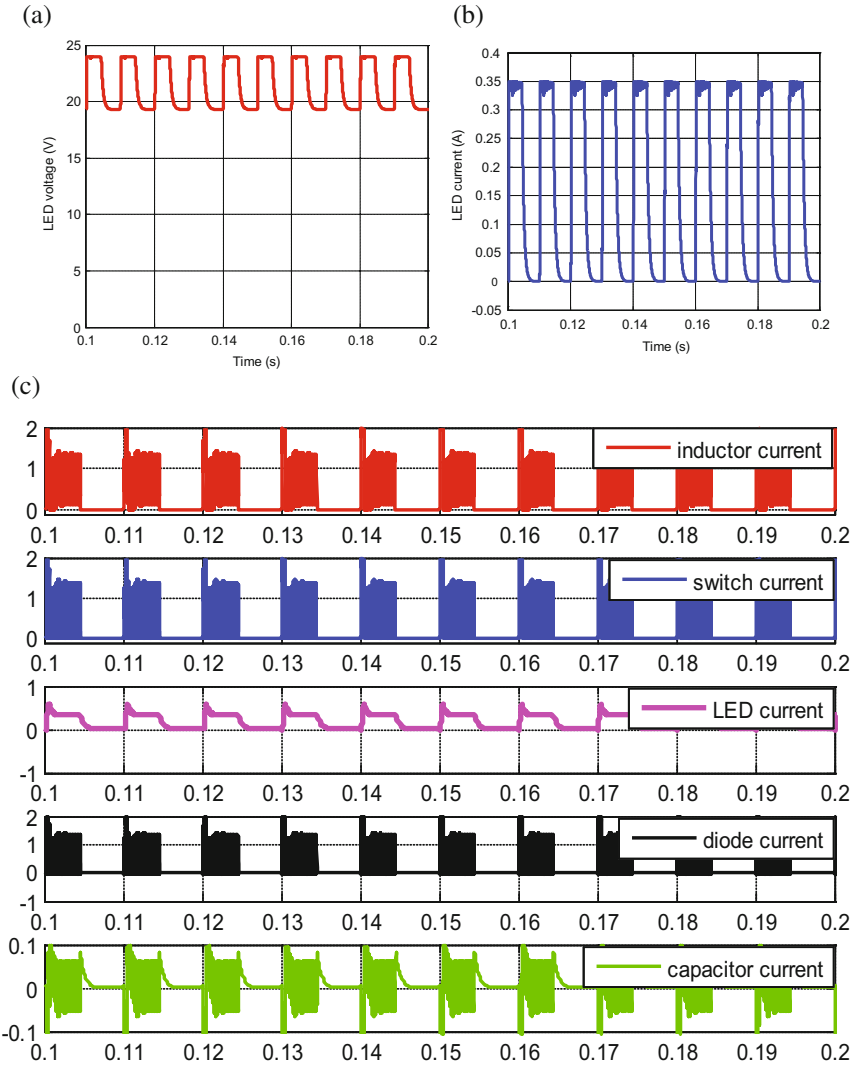


Fig. 7 Simulation results in LED dimming with half the rated current with SPWM method. **a** LED voltage. **b** LED current. **c** Current waveforms through inductor, switch, LED, diode and capacitor

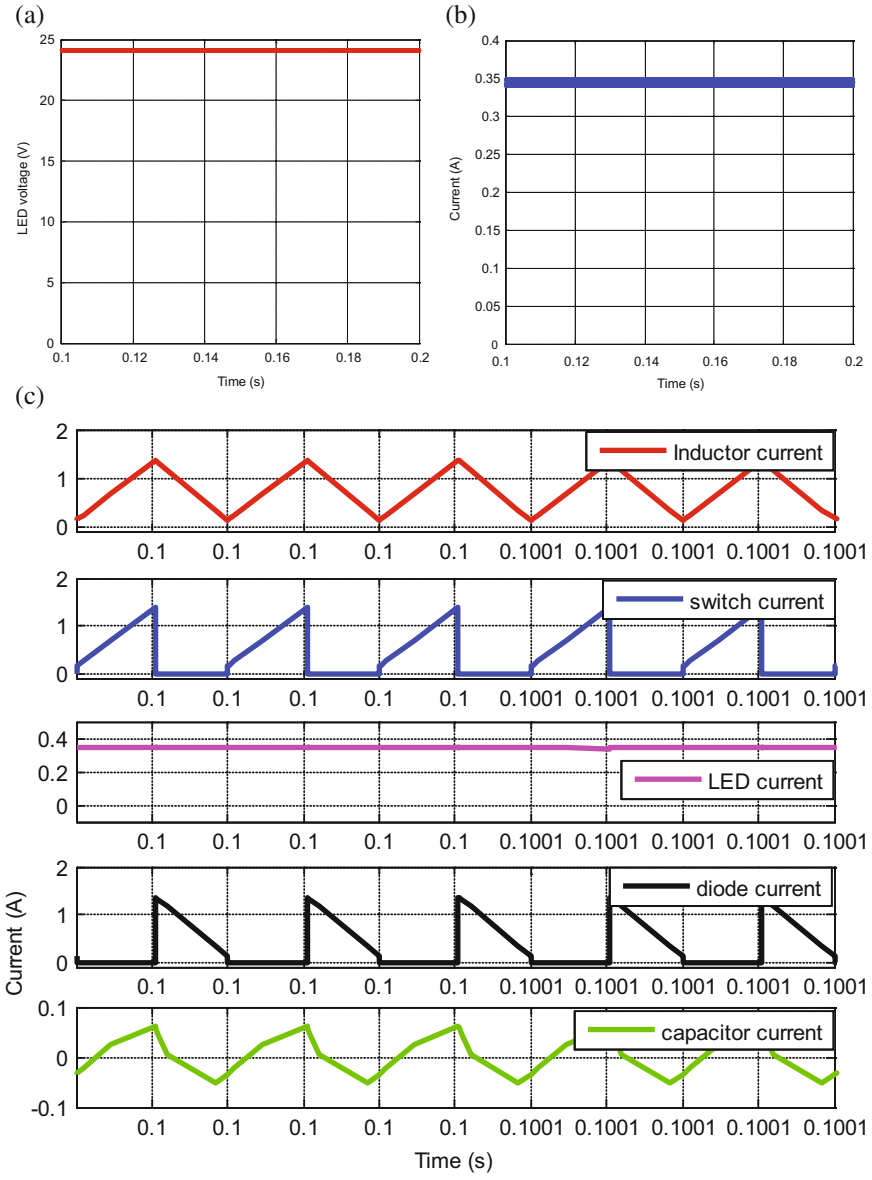


Fig. 8 Simulation results in LED dimming with rated current with SPWM method. **a** LED voltage. **b** LED current. **c** Current waveforms through inductor, switch, LED, diode and capacitor

Table 2 Efficiency of SPWM and DPWM (input voltage = 12 V)

Output load current (A)	Single PWM			Double PWM		
	Duty cycle	Output voltage (V)	% η	Duty cycle	Output voltage (V)	% η
0.0822	23.75	20.44	90.3	16.5	20.45	97.7
0.0875	25	20.56	89.8	18	20.52	96.9
0.175	37	21.77	91	43.5	21.75	95.7
0.2625	47.5	22.97	92.7	69	22.98	97.6
0.35	52	24.13	93.8	96	24	97.7

4 Conclusion

The dimming characteristics are achieved by employing DPWM technique in a simple buck–boost converter with minimum number of switches and energy storage devices. The performance of the driver circuit is improved by operating the converter in discontinuous conduction mode for current regulation. The low frequency reduces the flickering and colour difference under discontinuous conduction. It is possible to achieve wide output current range with minimum voltage variations without any additional coupling inductive components.

References

1. Chen, W., Hui, S.Y.R.: Elimination of an electrolytic capacitor in AC/DC light emitting diode (LED) driver with high input power factor and constant output current. IEEE Trans. Power Electron. **27**, 1598–1607 (2012)
2. Qu, X., Wong, S.C., Tse, C.K.: Noncascading structure for electronic ballast design for multiple LED lamps with independent brightness control. IEEE Trans. Power. Electron. **25**, 331–340 (2010)
3. Lam, J.C.W., Hui, J.C.Y., Jain, P.K.: A dimmable high power factor single switch electronic ballast for compact fluorescent lamps with incandescent phase-cut dimmers. IEEE Trans. Ind. Electron. **59**, 1879–1888 (2012)
4. Shagerdmootaab, A., Moallem, M.: A double-loop primary–side control structure for HB-LED power regulation. IEEE Trans. Power Electron. **31**, 2476–2484 (2016)
5. Hu, Q., Zane, R.: LED driver circuit with series-input-connected converter cells operating in continuous conduction mode. IEEE Trans. Power Electron. **25**, 574–582 (2010)
6. Christobher, G.: Analog technique simplifies LED dimming in portable applications. LEDs Mag. (2011)
7. Poplawski, M., Miller, N.J.: Exploring flicker in solid state lighting: what you might find, and how to deal with it. In: Proceedings CIE Centenary Conference, Paris, France
8. Ko, C.L., Liang, T.J., Chen, K.H., Chen, J.F.: Design and implementation of high frequency AC-LED driver with digital dimming. In: Proceedings IEEE International Symposium on Circuits and Systems, Paris, France, pp. 3713–3716 (2010)
9. Gacio, D., Alonso, J.M., Garcia, J., Campa, L., Crespo, M.J., Ricosecades, M.: PWM series dimming for slow dynamics HPF LED drivers: the high frequency approach. IEEE Trans. Ind. Electron. **59**, 1717–1727 (2012)

10. Moo, C.S., Chen, Y.J., Yang, W.C.: An efficient driver for dimmable LED lighting. IEEE Trans. Power Electron. **27**(11), 4613–4618 (2012)
11. Lehman B., and Wilkins A. J.: Designing to mitigate the effects of flicker in LED lighting reducing risks to health and safety. IEEE Power Electron. Mag. **1**(3), 18–26 2014
12. Chen, J.J., Yang, W. C., Moo, C.S., and Hsieh, Y.C.: A high efficiency driver for high-brightness white LED lamp. In: Proceedings IEEE TENCON'10, Fukuoka, Japan, pp. 2313-2317 (2010)

S-Parameter Based Evaluation of Cable Losses for Precise Low Frequency Voltage and Current Calibration

Swati Kumari, Sunidhi Luthra, Jyoti Chauhan, Bijendra Pal, Saood Ahmad, Ravinder Kumar, P.S. Negi and V.N. Ojha

Abstract LF (low frequency) voltage and current are important parameters in electrical metrology. Evaluation of cable losses has been undertaken to improve measurement accuracy for LF voltage and current calibration at CSIR-National Physical Laboratory India (NPLI). The measurement has been done by measuring its S-parameters using Vector Network Analyzer (VNA) in the frequency domain. Insertion Loss method and Return loss method have been used to validate the VNA based measurement results. This paper presents evaluation of cable losses for two designated coaxial cables. The applied corrections for both these cables have been evaluated in frequency range from 300 to 1 MHz at different LF voltage points. In order to improve LF voltgae and current calibration accuracy and precision in measurements, the coaxial cables must be characterized for their impedances and losses. This paper presents and discusses two different methods used to characterize the coaxial cables.

Keywords Coaxial cable · Insertion loss · Return loss · Cable loss Calibration · Accuracy · VNA

1 Introduction

To measure the broadband S-parameters using VNA, it has to be calibrated [1] first. A conventional short-open-load-thru (SOLT) method [2, 3] has been used to calibrate the VNA. Since in this study device under test (DUT) is coaxial cable with Type N connector, 85032F—a mechanical calibration kit having short open and load has been used for VNA calibration. Before starting the measurements, VNA's

S. Kumari (✉) · S. Luthra · J. Chauhan · B. Pal · S. Ahmad · P.S. Negi · V.N. Ojha
CSIR-National Physical Laboratory, Dr. K.S. Krishnan Marg, New Delhi 110012, India
e-mail: kumaris1@nplindia.org

R. Kumar
Al-Falah School of Engineering and Technology, Dhauj Village, Faridabad 121004, Haryana, India

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_31

reference plane must be calibrated [4]. Since here we are concerned about coaxial cable losses by two different VNA based measurement methods. So first S_{21} parameter is being measured and evaluated using two-port based Insertion loss method and then S_{11} parameter is being measured and evaluated using one-port return loss method, where one end of the cable is terminated by a matched 50 Ω load. Now S_{21} is evaluated based on S_{11} measurements using Eq. (3).

Based on insertion loss method and return loss method cable loss is measured in terms of logarithmic scale then evaluated using standard S-parameter formula [5]:

$$S21(dB) = 10\log_{10}\frac{outputpower}{inputpower}, \tag{1}$$

$$S11(dB) = 10\log_{10}\frac{transmittedpower}{receivedpower}, \tag{2}$$

$$S21(dB) = \frac{S11}{2} \tag{3}$$

So, the contribution due to cable losses has been evaluated in terms of correction. Correction has been calculated using following standard S-parameter formula [5]

$$S21 = \frac{b2}{a1} \mid a2 = 0 \tag{4}$$

$$\text{Correction} = \text{Applied value} - \text{Measured value} \tag{5}$$

where, a1 is incident power at the network input
a2 is incident power at the network output
b2 is reflected power at the network output

For many decades, research work has been going on around the globe to be at par in terms of national standards. It is a known fact that to reduce the overall uncertainty for a measurement, all sources of errors must be considered. Generally for any calibration setup, a standard source must be electrically connected to Device under Test (DUT) through cables and connectors. This paper discusses evaluation of cable losses for LF voltage and current calibration. Ideally the DUT must read the same value from the source without any degradation but unfortunately this is not always the case. So for precise and accurate measurements, appropriate cables must be used, otherwise serious errors may be introduced which can affect the overall uncertainty. So, to minimize the effect on total uncertainty one must consider these possible sources of errors.

2 LF Voltage and Current Calibration at NPLI

Being a National Metrology Institute (NMI), NPLI is responsible for providing apex-level calibration services within the country. For precise and accurate measurements, bank of multijunction thermal converters (MJTC) are used as primary standard for LF voltage and current parameter. MJTC's are used to assign AC–DC Transfer difference in frequency range from 10 Hz to 1 MHz for LF voltage and 40 Hz to 10 kHz for LF Current [6]. The AC–DC transfer difference thus assigned is transferred to working standards such as calibrators and digital multimeter.

The calibration setup shown in Fig. 1 consists of designated co-axial cables to connect the source with the DUT. The errors caused due to each and every component of calibration setup, especially cable losses must be included in the reported results. This paper presents the analysis done in support of this goal.

3 Experimental Setup

The experimental setup for insertion loss method evaluating cable loss is shown in Fig. 2. Corresponding S_{21} parameter of the coaxial cables have been measured and uncertainty calculated accordingly. To achieve our goal, designated coaxial cables as shown in Fig. 3 were measured for their S-parameter.

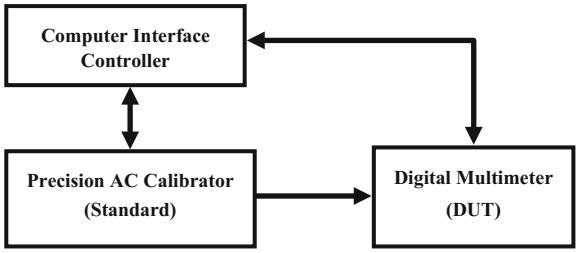


Fig. 1 Calibration setup for direct LF voltage and current measurements

Fig. 2 Two-Port VNA based insertion loss measurement setup for cable loss measurement

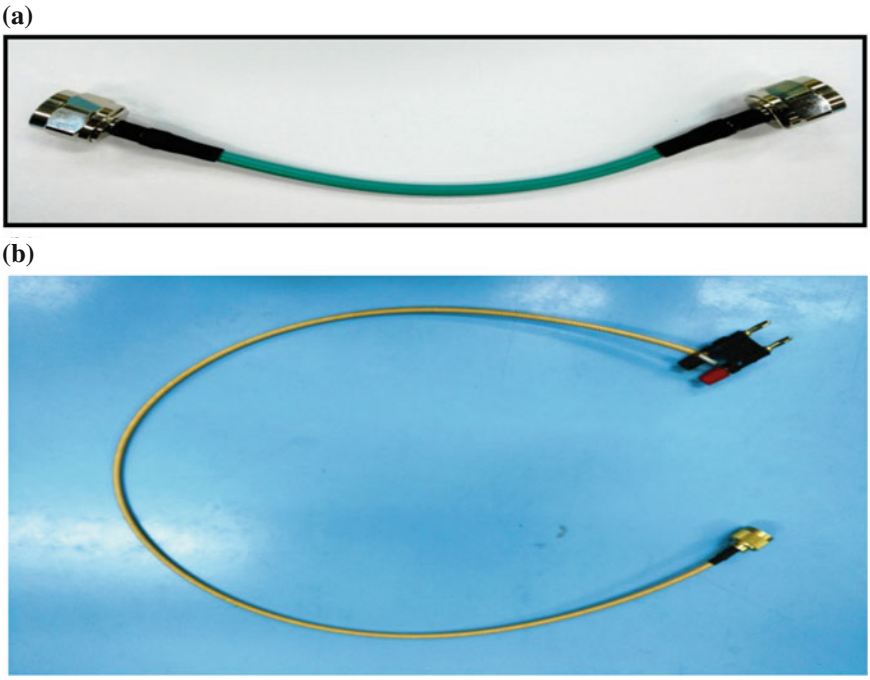


Fig. 3 **a** Cable 1: Type N (male) cable used in LF voltage measurements **b** Cable 2: Type N (male) to banana (male) cable used in LF voltage and current measurements

Table 1 Coaxial cable loss for cable 1 and cable 2 respectively

Freq. (kHz)	Cable 1		Cable 2	
	Insertion loss method (dB)	Return loss method (dB)	Insertion loss method (dB)	Return loss method (dB)
300	−0.015	−0.015	−0.023	−0.024
400	−0.015	−0.014	−0.023	−0.025
500	−0.015	−0.014	−0.024	−0.025
1000	−0.016	−0.014	−0.025	−0.026

4 Measurement Results

Measurement of cable losses has been done for higher end of LF range that is from 300 kHz to 1 MHz as shown in Table 1. Uncertainty of the cables has been calculated from the obtained sets of measurements [7]. Plot of uncertainty in cable loss measurements with frequency for both the cables are shown in Figs. 4 and 5

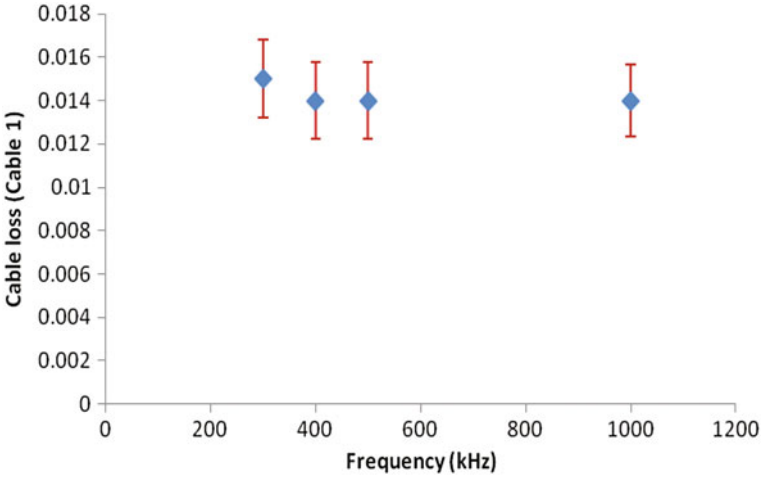


Fig. 4 Uncertainty in cable loss with respect to frequency for cable 1

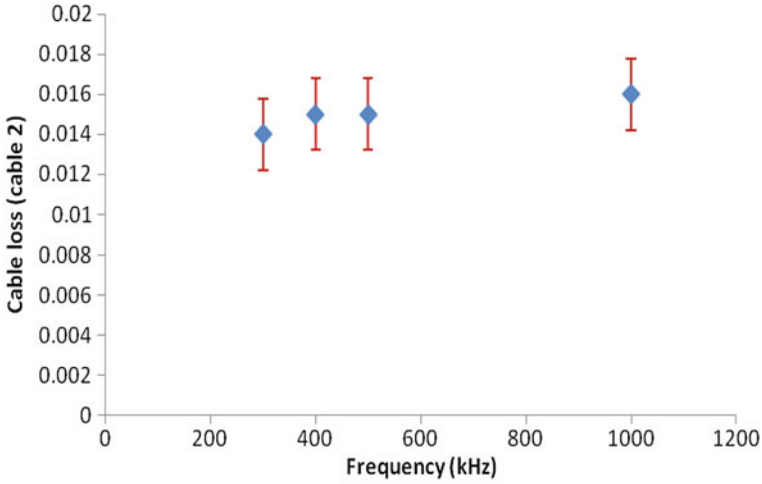


Fig. 5 Uncertainty in cable loss with respect to frequency for cable 2

respectively. Vertical bar shows uncertainty in the cable loss for LF range. As we can see from Table 1 that cable loss for cable 1 and cable 2 is approximately same for both the methods. Difference in cable loss for cable 2 as compared to cable 1 can be due to impedance mismatching between different types of end connectors. Further mismatch uncertainty [8] can be evaluated to validate the results.

Table 2 Correction for cable1 at different applied voltages

Applied voltage	Correction (V)				
Frequency (kHz)	1 mV	100 mV	1 V	100 V	1000 V
300	0.0000017	0.00017	0.0017	0.17	1.7
400	0.0000016	0.00016	0.0016	0.16	1.6
500	0.0000016	0.00016	0.0016	0.16	1.6
1000	0.0000016	0.00016	0.0016	0.16	1.6

Table 3 Correction for cable 2 at different applied voltages

Applied voltage	Correction (V)				
Frequency (kHz)	1 mV	100 mV	1 V	100 V	1000 V
300	0.0000016	0.00016	0.0016	0.16	1.6
400	0.0000017	0.00017	0.0017	0.17	1.7
500	0.0000017	0.00017	0.0017	0.17	1.7
1000	0.0000018	0.00018	0.0018	0.18	1.8

5 Conclusion

Coaxial cable losses have been evaluated for the LF voltage in the frequency range from 300 kHz to 1 MHz. Broadband S-parameter for designated cables has been measured and analysed and corresponding corrections have been calculated using Eqs. (1), (2), (3), (4) and (5) for different voltage points as shown in Tables 2 and 3. Measurement results shows that both methods are validated. Correction factor is sensitive to cable losses which concludes that higher end of LF range need to be addressed and corrections must be applied for absolute measurements. For accurate and precise LF voltage and current calibration, cable losses must be incorporated in the results.

Acknowledgements Financial assistance provided by CSIR under Network Project NWP-045 is gratefully acknowledged. Finally authors express their deep gratitude to Dr. D.K.Aswal, Director, National Physical Laboratory for his constant encouragement and motivation.

References

1. Blackham, D., Wong, K.: Latest advances In VNA accuracy enhancements. Microw. J. **48**(7), 78–94 (2005)
2. Lu, K.C., Lin, Y.C., Horng, T.S., Wu, S.M., Wang, C.C., Chiu, C.T., Hung, C.P.: Vertical interconnect measurement techniques based on double-sided probing system and short-open-load-reciprocal calibration. In: 61st Electronic Components and Technology Conference (ECTC), pp. 2130–2133, IEEE (2011)

3. Padmanabhan S., Kirby P., Daniel J., Dunleavy L.: Accurate broadband on-wafer SOLT calibrations with complex load and thru models. In: 61st ARFTG Conference Digest, Spring 2003, IEEE, pp. 5–10 (2003)
4. Eul, H.J., Schiek, B.: A generalized theory and new calibration procedures for network analyzer self-calibration. IEEE Trans. Microw. Theory Tech. **39**(4), 724–731 (1991)
5. Agilent Test and measurement application note 95-1: S-Parameter techniques. Literature number 5989-9273EN (1996)
6. Rustagi, V.K., Govil, A.K., Agrawal, V.K.: Multijunction thermal converters as the primary standards of AC & LF voltage and current at national physical laboratory. In Mathur, B.S., et al. (eds) Advances in Metrology and its Role in Quality Improvement and Global Trade. pp. 360–364 (1996)
7. National Accreditation board for testing and calibration laboratories: guidelines for estimation and expression of uncertainty in measurement, Doc. No: NABL 141, Issue No: 02, Issue Date: 02.04.2000
8. Agilent fundamentals of RF and microwave power measurements (Part 3): power measurement uncertainty per international guides AN 1449–3. Literature number 5988-9215EN

Buck–Boost Current Converter Using Duality Concept and Its DC Transformer Modelling

S.B. Mahajan, Padmanaban Sanjeevikumar, K.M. Pandav, R.M. Kulkarni and V.A. Sherke

Abstract In this chapter, DC–DC current buck–boost converter using duality concept is articulated with the help of DC transformer modelling. Buck–boost converter plays a dominant part of switch mode power supply (SMPS) and drives applications for voltage and current control. Advantage of employing buck–boost converter is that it provides voltage less as well as greater than input voltage. The suggested converter is dual of traditional buck–boost converter and provides a flexible control of current for SMPS and drives applications. The duality concept is applied on conventional voltage source buck–boost converter to obtain proposed converter (current buck–boost converter). The formation of proposed circuit is discussed in detail along with its mathematical analysis and equations. MATLAB is used to simulate proposed and results prove practicability and operation of proposed circuit of converter.

Keywords Duality approach · DC–DC · Buck–boost · DC transformer modelling Current

S.B. Mahajan (✉) · K.M. Pandav · R.M. Kulkarni · V.A. Sherke
Department of Electrical and Electronics Engineering,
Marathwada Institute of Technology (MIT), Aurangabad, Maharashtra, India
e-mail: sagar25.mahajan@gmail.com

K.M. Pandav
e-mail: kiranpandav88@yahoo.co.in

R.M. Kulkarni
e-mail: kulkarni.rishi123@gmail.com

V.A. Sherke
e-mail: sherke.vaibhav@gmail.com

P. Sanjeevikumar
Department of Electrical & Electronics Engineering, University of Johannesburg,
Auckland Park, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_32

1 Introduction

Now-a-days many industrial applications require a variable DC voltage from fixed DC voltage [1–12]. Buck–boost converter is DC–DC high frequency switching converter and it merges the characteristic of boost converter and buck converter to feed the constant power to load [1–4]. This converter requires DC input which results into low as well as high output voltage and output is depends on duty ratio. Traditional buck–boost converter gives low as well as high negative output compared to input [5–12]. Some industrial drives application requires current converter to control the torque of the drives. In this paper, buck–boost current converter is proposed using duality approached to control the current through load. In proposed converter dual model of voltage source buck–boost converter is employed to control the load as per the industrial requirement which helps to achieve high or low current. When OFF state duty cycle of switch decreases, then output of proposed converter is decreased and converter is operates as a buck current converter. When OFF state duty cycle of switch is increases then output of proposed converter is increased and converter is operates as a boost current converter. Electrostatic components (Capacitors) and magnetic components (Inductor) play a very crucial role in operation of the proposed converter and operating at the high frequency as they possess remarkable property of getting charged or discharged in short time span. In Sect. 2, duality concept is applied to obtain proposed converter. In Sect. 3, proposed converter circuit analysis given with numerical equation, DC transformer modelling and its diagrammatic representation. The relationships of DC current and DC voltages are represented by DC transformer modelling [1–4]. MATLAB software is used to verify the practicability of proposed converter. In Sect. 4 proposed converter simulation results is discussed and examined in detail.

2 Proposed DC–DC Buck–Boost Current Converter with Duality Concept

A circuit and its dual circuit are different from each other but they show the same characteristics equation. Hence, two circuits are dual of each other if they described by similar characteristic equations with only its dual pair interchanged [1–4]. Duality is obtained between voltage and current source, resistance and conductance, capacitor and inductor, open circuit and short circuit, and many more as elaborated in the Table 1. Proposed current buck–boost converter is obtained by using duality concept on conventional voltage source buck–boost converter. Figure 1 shows traditional buck–boost converter with voltage source which is consisting of single switch, inductor, diode and capacitor.

To find the network of proposed current converter (dual circuit of traditional voltage buck–boost converter), following steps are to be followed and the duality operation is articulated in Fig. 2.

Table 1 Duality relationship between circuit terms and components

Components and terms in circuit	↔	Dual of components and terms
Voltage source (independent)	↔	Current source (independent)
Current source (independent)	↔	Voltage source (independent)
Capacitor	↔	Inductor
Resistance	↔	Conductance
ON-time duty cycle (Ton/T)	↔	OFF-time duty cycle (Toff/T)
Short circuit	↔	Open circuit
Mesh/loop	↔	Node
Inductor volt second balance	↔	Capacitor ampere second balance
Power transistor	↔	Power transistor
Power diode	↔	Power diode
Star connection	↔	Delta connection

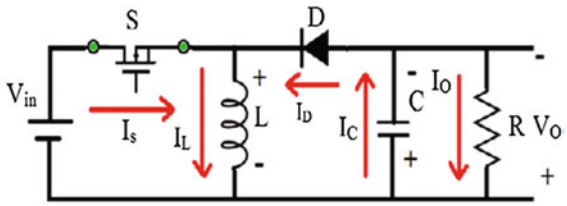


Fig. 1 Traditional buck–boost voltage source converter

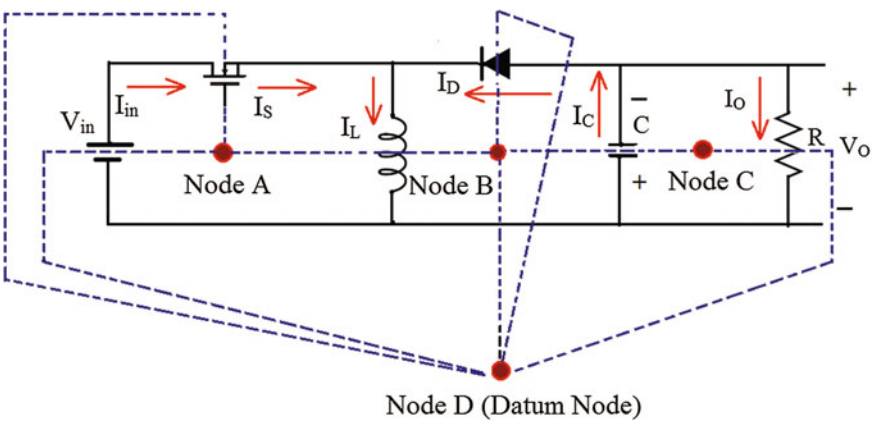


Fig. 2 Duality concept for traditional buck–boost voltage source converter

1. Consider a node at the middle of each mesh of traditional buck–boost voltage source converter.
2. Now, mark a datum node (known as reference node) away from all nodes outside the circuit.
3. Join the considered nodes, such that every line joining the nodes should pass through an element in the circuit.
4. If the line drawn from the nodes leaves the circuit after passing through a circuit element, then join the line with datum node.
5. Now, replace each element by its dual pair element as shown in the table.
6. After considering the dual elements, the polarity of voltage source must be determined. If the mesh current produced by voltage source is positive then in the duality circuit, consider the current direction from datum node to associated node of mesh.

Figure 3 depicts the proposed current buck–boost converter and it required single inductor, single control switch, single uncontrolled switch and capacitor. Control switch is directly connected in parallel with current source to control the operation of modes of proposed converter. Single inductor is connected in series with load. Capacitor is connected in intermediate to transfer of energy of the source to loads. When *S* is turned ON, all the input current is passed through the switch *S*. Capacitors transfer its energy to load and inductor through switch *S*. Because of capacitor voltage diode *D* is in reverse biased (negative voltage is appeared across diode). In this mode series connection of control switch, Load, Inductor *L*, capacitor forms a closed loop. Negative buck or boost current is obtained at the load. The equivalent circuit of proposed converter when switch *S* is turn ON is given in Fig. 4a.

$$\left.\begin{array}{l} I_{\text{in}}{=}I_{\text{S}}, V_{\text{S}} = 0, I_D = 0 \\ I_C = -I_L = I_o \\ V_{\text{O}} - V_L + V_C = 0 \end{array}\right\} \quad \text{ON State Equation} \tag{1}$$

When switch *S* is turned OFF, all input current flows through the capacitor and diode. Thus in this mode capacitor is charged by input source. Diode, load and inductor form a closed loop and inductor provides energy to load through diode. The diode is forward biased and current through diode is equal to summation of capacitor and inductor current. Finally negative buck and boost current is obtained

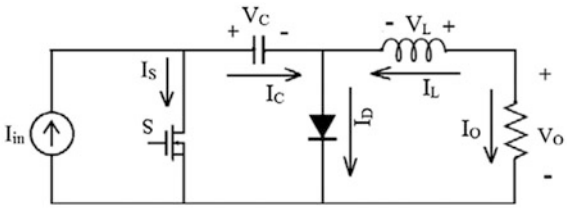


Fig. 3 Proposed current buck–boost converter

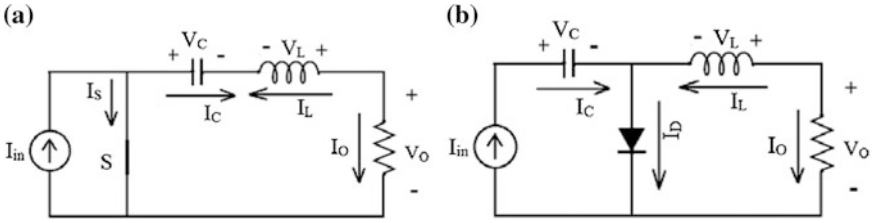


Fig. 4 **a** ON state **b** OFF state of equivalent circuit of proposed buck–boost current converter

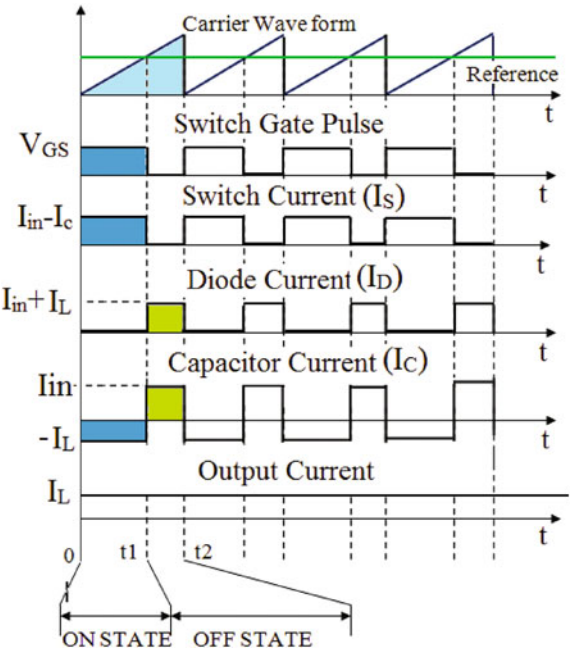


Fig. 5 Characteristics waveform of the proposed converter

at the output of converter. The equivalent circuit of proposed converter when switch S is turn OFF is given in Fig. 4b.

$$\left.\begin{aligned} I_D &= I_C + I_L = I_C - I_O \\ I_S &= 0, I_{\text{in}} = I_C \\ V_O - V_L &= 0 \end{aligned}\right\} \quad \text{OFF State Equation} \tag{2}$$

In Fig. 5 characteristics waveform of the proposed current source converter is shown. In proposed current buck–boost converter inductor and capacitor is used as a filter and intermediate component respectively. The main function of capacitor is to deliver energy to load from input source. Proposed converter follows the capacitor ampere-second balanced method which is a dual of inductor volt second balanced

method. It means during one complete cycle of switching, the amount of charge flowing in and out of the capacitor is the same in its steady state condition. Thus the integration of capacitor current over a complete switching cycle is equal to zero.

$$(1-D)I_{\text{C (when switch is ON)}} + (D)I_{\text{C (when switch id OFF)}} = \Delta Q \tag{3}$$

where, OFF-time duty cycle denoted by D (ON-time duty cycle).

$$(1-D)(-I_L) + D(I_{\text{D}} - I_L) = 0 \tag{4}$$

$$(1-D)(I_{\text{O}}) + DI_{\text{in}} = 0 \tag{5}$$

$$\text{Current gain of proposed converter, } G(D) = \frac{I_{\text{O}}}{I_{\text{in}}} = \frac{-D}{1-D} \tag{6}$$

$-D/(1-D)$ is current gain of proposed converter. Proposed converter operated as buck current converter when D is less than 0.5 and operated as boost converter when D is greater than 0.5. Proposed converter provides a workable solution to control the current of load.

3 Proposed Buck–Boost Converter DC Transformer Modelling

The DC transformer model is utilized in order to obtain the circuit equivalent of proposed converter, which represents the direct and apparent relation of DC currents and DC voltages of a converter. Considerable and accepted approach is provided by this model which allows transformer gets saturated with DC; hence, transformer is employed physically without considering the parameter to model equivalent circuit of proposed converter. Both side of transformer, i.e., primary as well as secondary are represented by dependent sources and turn ratio is the functions of OFF state duty cycle provided control system. There are usually three distinct ports in a power converter: input port, output port and control signal port as illustrated in Fig. 6. The efficiency of switching converters is ideally equal to 100%. This is the reason; it is found that input power is always equal to power obtained at output.

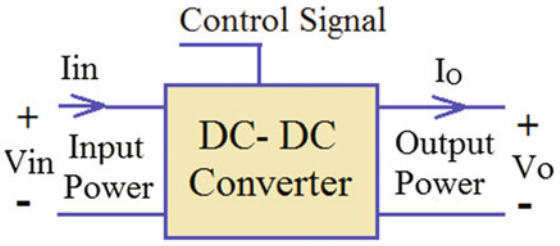


Fig. 6 Generalized power converter port

$$\left.\begin{array}{l}\text{Input power } (P_{\text{in}}) = \text{Output power } P_{\text{O}} \\ \text{or } I_{\text{in}} \times V_{\text{in}} = I_{\text{o}} \times V_{\text{o}}\end{array}\right\} \tag{7}$$

$$\left.\begin{array}{lll} I_{\text{in}} = I_{\text{o}} \times \frac{1}{G(D)} & \text{or} & I_{\text{o}} = I_{\text{in}} \times G(D) \\ V_{\text{o}} = V_{\text{in}} \times \frac{1}{G(D)} & \text{or} & V_{\text{in}} = V_{\text{o}} \times G(D) \end{array}\right\}, \tag{8}$$

where $G(D)$ is based on duty y ratio (OFF state duty cycle). Conversion ratio of proposed converter does not depends on the load and it is equal to negative value of $D/(1 - D)$. Further Model-I network and Model-II network are obtained by using proposed current converter as shown in Fig. 7a, b.

Using Ideal DC transformer model, an equivalent but actually more significant and upgraded model of any DC–DC Converter can be acquired as exposed in Fig. 8a. Solid horizontal lines indicated that transformer is capable to work on DC voltage and Current. The set of rules applied to simplify the equivalent circuit of proposed converter and final DC transformer model is shown in Fig. 8b.

To make the circuit much simpler, all the elements on primary sides are shifted to transformer's secondary side as illustrated in Fig. 9. Now, with the help of current division rule, the circuit can be simplified in order to find the resultant output current. The graph for OFF state duty cycle versus current gain is illustrated in Fig. 10.

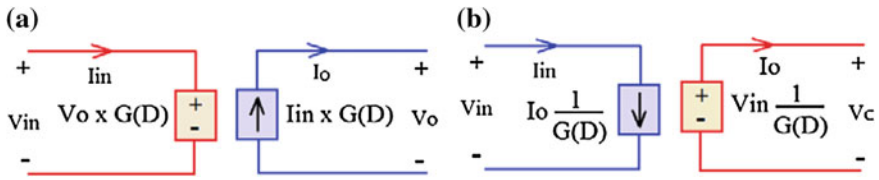


Fig. 7 Proposed converter modelled based on dependent source **a** model-I **b** model-II

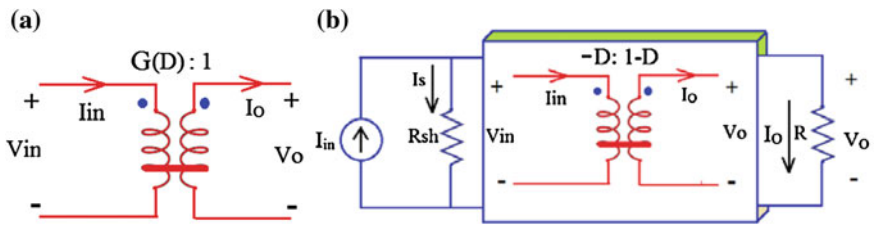


Fig. 8 DC–DC converter model using DC transformer **a** generalized model using DC transformer **b** proposed converter using DC transformer

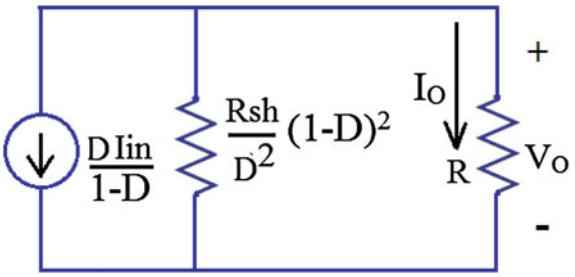


Fig. 9 Proposed converter DC transformer model by referring the entire primary element to secondary side

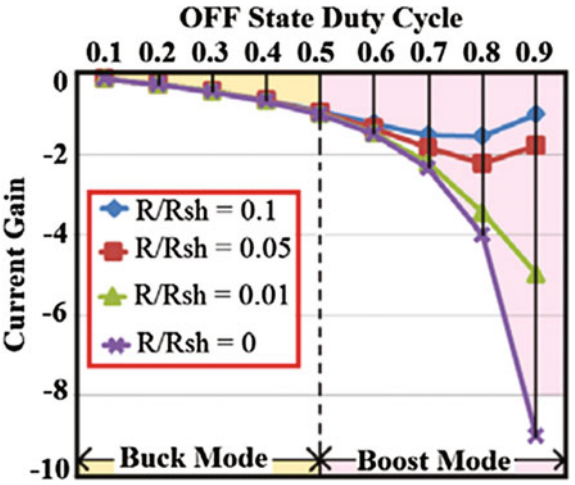


Fig. 10 The current gain versus OFF state duty cycle graph of proposed converter

4 Simulation Result of Proposed Buck–Boost Converter

The proposed buck–boost current converter is simulated in MATLAB to verify the feasibility and operation with 20 kHz switching frequency, 100 W rated, input current 4 A, off state duty cycle is 75% for boost Mode of converter and 25% off state duty cycle for buck Mode. Simulation result of proposed converter in buck mode and boost mode is shown in Fig. 11a, b respectively. In buck mode it is observed that for 25% off state duty cycle, the current is step down to −1.34 A from 4 A. In boost mode, it is observed that for 75% off state duty cycle, the current is step up to −12 A from 4 A. It is also observed that diode is in reversed biased when switch is ON. In OFF state voltage across diode is summation of voltage across load and inductor. The voltage across switch in OFF state is equal to capacitor voltage.

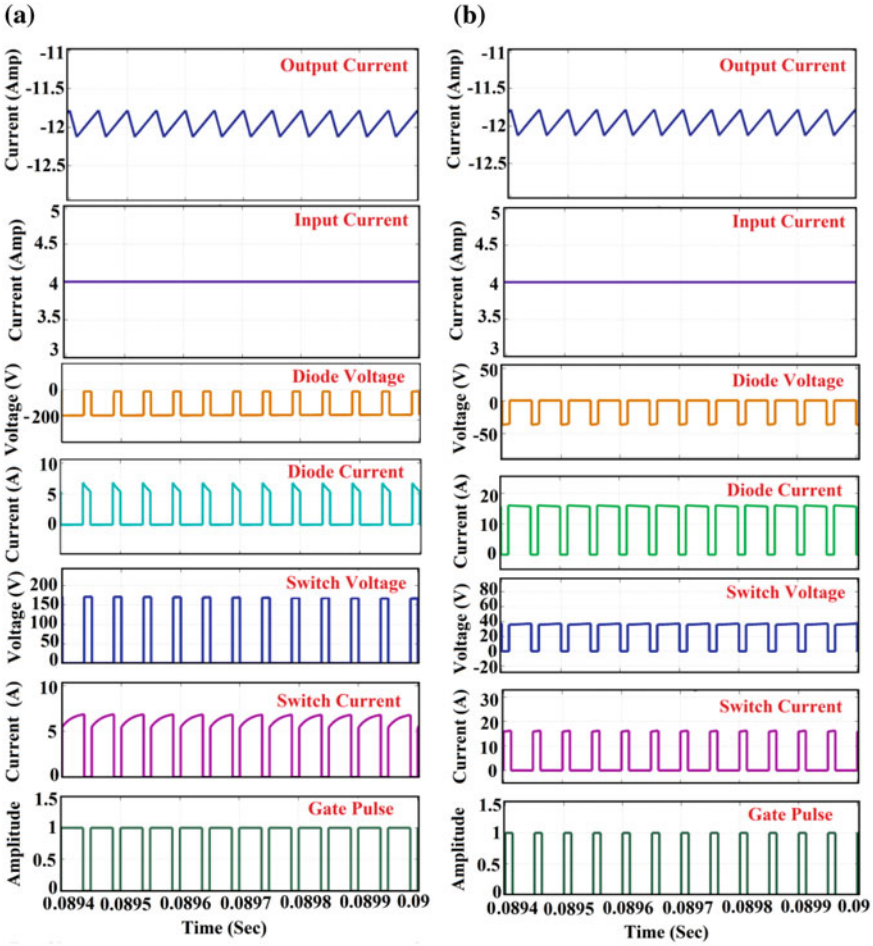


Fig. 11 Simulation Result **a** buck mode (25% OFF state duty cycle) **b** boost mode (75% OFF state duty cycle)

5 Conclusions

Buck–boost current converter using concept of duality is articulated in this paper with DC Transformer model to control the load current. Using duality concept and capacitor ampere second balance method conversion ratio is obtained. Proposed converter operates as a buck current converter when off state duty cycle is lesser than 50% and operates as a boost current converter when off state duty cycle is higher than 50%. Simulation results prove the viability of proposed circuit and duality concept.

References

1. Mahajan, S.B., Sanjeevikumar, P., Blaabjerg, F., Fedák, V., Kulkarni, R.: Non isolated and non-inverting cockcroft walton multiplier based hybrid 2Nx interleaved boost converter for renewable energy applications. In: International Conference on IEEE Power Electronics and Motion Control, Bulgaria (2016)
2. Mahajan, S.B., Kulkarni, R., Sanjeevikumar, P., Pierluigi, S., Blaabjerg, F.: Hybrid non-isolated and non inverting Nx interleaved dc-dc multilevel boost converter for renewable energy applications. In: International Conference on IEEE Environment and Electrical Engineering, Florence (2016)
3. Mahajan, S.B., Badave, S.M., Kiran, P.M., Mule, S.M., Kulkarni, R.:DC-DC current buck converter through duality approach and its DC transformer modeling for current based loads. In: IEEE International Conference on Circuit, Power and Computing Technologies, Nagarcoil (2016)
4. Mahajan, S.B., Mule, S.M., Kardile, A.H., Kulkarni, R.M.: DC-DC buck converter through duality approach for current based loads. In: IEEE International Conference on Electrical Electronics, and Optimization Techniques, Chennai (2016)
5. Wai, R., Jheng, K.: High efficiency single input multiple outputs DC-DC converter. IEEE Trans. Power Electron. **28**(2), 886–898 (2013)
6. Tan, N.M.L., Abe, T., Akagi, H.: Design and performance of a bidirectional isolated DC-DC converter for a battery energy storage system. IEEE Trans. Power Electron. **27**(3), 1237–1248 (2012)
7. Mahajan, S.B., SriRevati, B.: Modeling and analysis of a novel multifunctional converter for solar applications. Int. J. Res. Electr. Electron. Eng. **1**(2), 39–46 (2013)
8. Plesko, H., Biela, J., Luomi, J., Kolar, J.W.: Novel concept for integrating the electrical drive and auxiliary dc-dc converter for hybrid vehicles. IEEE Trans. Power Electron. **23**(6), 3025–3034 (2008)
9. Mahajan, S.B., Maroti, P.K., Prabhakar, K.: Novel topological derivations for dc-dc converters. Int. J. Comput. Eng. Manag. **16**(6), (2013)
10. Iqbal, Z., Nasir, U., Raasheed, M.T., Munir, K.: A comparative analysis of synchronus buck, isolated buck and buck converter. In: IEEE Environment and Electrical Engineering International Conference, Italy (2015)
11. Mok, K.T, Lai, Y.M., Tse, C.K., Loo, K.H.: Synthesis of two state ladder structured DC-DC power converters by duality principle. In: IEEE Industrial Electronics Society annual conference, IECON (2012)
12. Samie, M., Perinpanayagam, S., Alghassi, A., Motlagh, A.M.S., Kapetanois, E.: Developing prognostic models using duality principles for DC to DC converters. IEEE Trans. Power Electron. **30**(5), 2872–2884 (2015)

2.4 kW Three-Phase Inverter for Aircraft Application-Hardware Implementation

K.M. Pandav, S.B. Mahajan, Padmanaban Sanjeevikumar, S.M. Badave and R.M. Pachagade

Abstract In this article 2.4 kW, three-phase inverter for aircraft application is articulated. When aircraft above 1000 m altitude, power amplifiers are employed to increase the strength of signal during transmission. The circuitry consist of input filter, three-phase output obtained by connecting three single-phase H-bridge inverter, transformers and LC filters at the star connected load end. The (THD) of proposed three-phase inverter is 2.8%. The Total Harmonics Distortion (THD) of the circuit is reduced by using sinusoidal pulse width modulation technique (SPWM). The component size is reduced by using high frequency modulating signal (400 Hz). The proposed circuit performance is verified with experimental and simulation result. The experimental and simulation result confirms the feasibility of proposed converter.

Keywords Three-phase inverter · H-Bridge · Aircraft application
High frequency · Sinusoidal pulse width modulation (SPWM)

K.M. Pandav · S.B. Mahajan (✉) · S.M. Badave · R.M. Pachagade
Department of Electrical & Electronics Engineering, Marathwada Institute of Technology, Aurangabad, India
e-mail: sagar25.mahajan@gmail.com

K.M. Pandav
e-mail: kiranpandav88@yahoo.co.in

S.M. Badave
e-mail: smb.eed@gmail.com

R.M. Pachagade
e-mail: ruchi.pachagade@gmail.com

P. Sanjeevikumar
Department of Electrical & Electronics Engineering, University of Johannesburg, Auckland Park, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_33

1 Introduction

The invention of aircraft by Wright Brothers helped mankind to take a step up in the ever-fascinated dream of flying. Recently major challenge is to adopt power conversion static inverters technology to supply the aircraft's electrical instruments. The recent era of fresh aircraft systems, a most important challenge is conversion of supply for the aircraft's electrical instruments. Present aircrafts depend exhaustively on electrical power owing to wide application of electronic flight instrument systems to normalize, produce and allocate electrical power throughout the aircraft. To accomplish consistency in the electrical systems suitable energy conversion device with fewer distortions, minimum number of semiconductor devices and protection unit is installed in such a way that it will not be subjected to harmful on circumstances of any kind. Three-phase inverter utilizes the renowned technologies for reliable and fault tolerant, redundant with low-voltage and high-current configurations [1–5]. Due to capability of reduction in per phase inverter semiconductor rating it is more suited for high power applications. The radio detection and ranging (RADAR) is used in aircraft to transmit and receive the signal from the ground station. If aircraft flying at altitude below 1000 m, then the signal strength is good at receiving end of the ground station. But when aircraft flying above 1000 m altitude, the strength of the signal received at ground station is weak, to get good signal strength throughout the way at the ground station power amplifier is used. This power amplifier increases the strength of signal by increasing the gain of the system. The high power rated system is required to turn on the power amplifier. Inverter plays a dynamic role in gaining the symmetrical AC output voltage of desired magnitude and frequency. The inverters have been extensively used for engineering applications such as AC motor drives and uninterruptible power supply (UPS), [1–13]. Recently, the inverters are also playing an important role in various renewable energy conversions as these are used for harnessing electricity from grid of Wind Energy System or solar System.

Three phase power generation proves to be more economical when compared with single-phase power generation. In three-phase systems, 120° phase difference achieved in each phase of waveforms implies a spatial displacement of 120° delay in time every power cycle [3–5]. Reference to electrical systems definitions, a three-phase power can be denoted by three separate power circuits. Under ideal situations three-phase power systems designate a balanced behaviour. Three-phase systems are termed unbalance in cases where either of the three-phase voltages is unequal or the phase angle deviates from 120°.

The renowned benefits such as reduction Total Harmonic Distortion (THD) and limited dv/dt in the output voltages with limited rating devices ease of splitting phase windings the Three-phase inverters are more advantageous than conventional inverter. In this paper, 2.4 kW three-phase converter for aircraft application is articulated with hardware and simulation results. The Total Harmonics Distortion (THD) of the circuit is reduced by using sinusoidal pulse width modulation technique (SPWM).

2 Three-Phase Proposed Inverter

Three single-phase inverters are linked in parallel to configuration the three-phase inverter as depicted in Fig. 1. To achieve balance three-phase voltages gating signals of single phase inverters should be 120° phase shift with respect to each other. Isolated winding is employed in primary side of the transformer whereas the secondary windings linked to a filter. The working of single phase inverter depends on the switching sequence. The single-phase inverter is operating in 180° conduction means every switch conduct for 180°. For positive and negative half cycle the load voltage is equal to the V_S and $-Vs$ respectively where, Vs is supply voltage.

Ideal situation is considered to evaluate proposed three-phase inverter. The angular difference between voltages and current in each phase of three-phase power system is φ.

Then the voltage and current of R phase will be

$$\left.\begin{aligned} V_R &= V_m \sin \omega t \\ I_R &= I_m \sin(\omega t - \varphi) \end{aligned}\right\} \tag{1}$$

The voltage and current of Y phase will be

$$\left.\begin{aligned} V_Y &= V_m \sin(\omega t - 120^\circ) \\ I_Y &= I_m \sin(\omega t - \varphi - 120^\circ) \end{aligned}\right\} \tag{2}$$

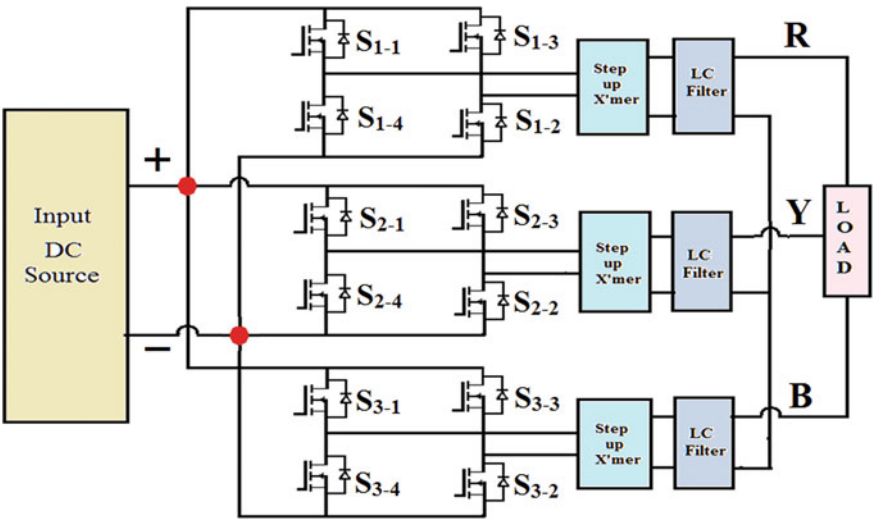


Fig. 1 Block diagram of three-phase inverter

And the voltage and current of B phase will be

$$\left.\begin{aligned} V_{\mathrm{B}} &= V_{\mathrm{m}} \sin(\omega t + 120^{\circ}) \\ I_{\mathrm{B}} &= I_{\mathrm{m}} \sin(\omega t - \varphi + 120^{\circ}) \end{aligned}\right\} \tag{3}$$

Therefore, the expression instantaneous power in R, Y and B phase is

$$\left.\begin{aligned} V_{\mathrm{R}} * I_{\mathrm{R}} &= V_{\mathrm{m}} I_{\mathrm{m}} \sin(\omega t) \sin(\omega t - \varphi) \\ V_{\mathrm{Y}} * I_{\mathrm{Y}} &= V_{\mathrm{m}} I_{\mathrm{m}} \sin(\omega t - 120^{\circ}) \sin(\omega t - \varphi - 120^{\circ}) \\ V_{\mathrm{B}} * I_{\mathrm{B}} &= V_{\mathrm{m}} I_{\mathrm{m}} \sin(\omega t + 120^{\circ}) \sin(\omega t - \varphi + 120^{\circ}) \end{aligned}\right\} \tag{4}$$

The total three-phase power of the system is summation of the individual power in each phase

$$P = V_{\mathrm{R}} * I_{\mathrm{R}} + V_{\mathrm{Y}} * I_{\mathrm{Y}} + V_{\mathrm{B}} * I_{\mathrm{B}} \tag{5}$$

Substituting Eq. (4) in Eq. (5) implies

$$P = 3 * \left(\frac{V_{\mathrm{m}}}{\sqrt{2}}\right) * \left(\frac{I_{\mathrm{m}}}{\sqrt{2}}\right) * \cos\varphi = 3VI\cos\varphi \tag{6}$$

The Eq. (6) illustrates the total instantaneous power is constant and equal to three times of the real-power per phase.

2.1 Inverter Card and PWM Generation

The Pulse Width Modulation (PWM) based inverters are superior when compared to inverters designed using conventional technologies [1–7]. The PWM MOSFET inverters are used which provide output switching stage. The PWM inverters have a lot of protection and control circuits in comparison to the traditional inverters. PWM is used to keep the output voltage of the inverter at the rated voltage (110/220 V AC) irrespective of the output load and to reduce THD. This is accomplished by changing the width of the switching frequency generated by the oscillator section. The AC voltage at the output is based on the width of the switching pulse. The control process is achieved by feeding back a part of the inverter output to the PWM controller section (PWM controller IC). Based on this feedback, voltage the PWM controller will make necessary corrections in the pulse width of the switching pulse generated at oscillator section. This change will cancel the changes at the output voltage and the inverter output will stay constant irrespective of the load variations. The AC voltage obtained at the output of inverter can be boosted up by step-up transformer that converts low AC voltage into high AC voltage as per requirement. In Sinusoidal PWM inverter the widths of the pole-voltage pulses, over the output cycle, vary in a sinusoidal manner.

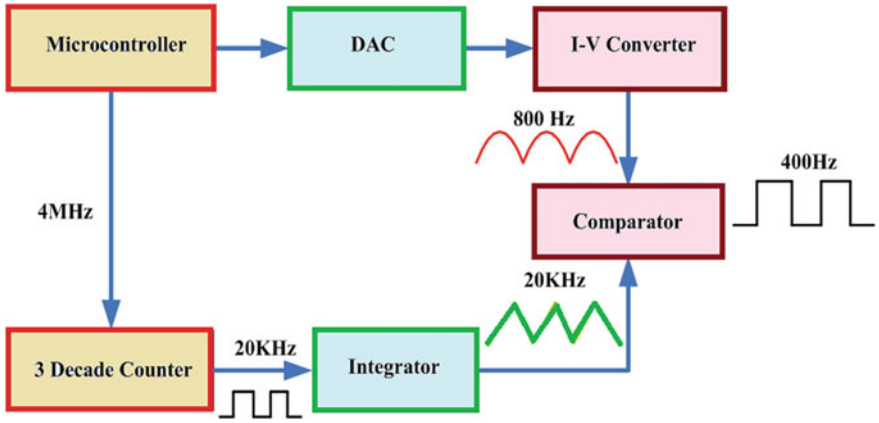


Fig. 2 Flow chart for PWM generation

The scheme, in its simplified form, involves comparison of a high frequency triangular carrier voltage with a sinusoidal modulating signal that represents the desired fundamental component of the pole voltage waveform. The proposed logic flowchart to generate PWM is shown in Fig. 2. The positive sine wave is compared with the triangular wave by op-amp comparator. The output of the comparator is the PWM pulse of 20 kHz frequency. The output of comparator again compares with the synchronizing square-wave signal of frequency 400 Hz using NAND gate. For lower switches, the synchronizing pulse first inverted and then compared with the output of comparator using NAND gate. The ratio of the peak magnitudes of the modulating wave (V_m) and the carrier wave (V_c) is defined as modulation index.

$$\text{Modulation index} = \frac{V_m}{V_c} \tag{7}$$

The switching pulses are generated by using P89V51RD2 microcontroller used in PWM card. The values of the sine function vary from −1.0 to + 1.0 for 0 to 360° angles. This method ensures that only integer numbers are input to the DAC by the 89V51RD2 microcontroller. Table 1 represents the angles, the sine values, the voltage magnitudes, and the integer values representing the voltage magnitude for each angle (with 300 increments). The full-scale voltage of 10 V obtained using Eq. (8) is assumed for DAC output. V_{out} of DAC for various angles is calculated as shown in the Table 1.

$$V_{out} = 5V + (5 \times \sin\theta) \tag{8}$$

The digital signal from microcontroller is given to DAC0800 IC which converts digital signal to analog signal. The output of DAC is an analog current signal given to an I-V converter that gives analog positive half sine wave signal at its output and of 800 Hz frequency. The generation of triangular wave of 20 kHz cannot be

Table 1 Angle versus voltage magnitude for sine wave

Angle (degree)	Sin θ	V_{out} (voltage magnitude)	Value send to DAC (decimal)
0	0	5	128
30	0.5	7.5	192
60	0.866	9.33	238
90	1.0	10	255
120	0.866	9.33	238
150	0.5	7.5	192
180	0	5	128
210	−0.05	2.5	64
240	−0.866	0.669	17
270	−1.0	0	0
300	−0.866	0.669	17
330	−0.5	2.5	64
360	0	5	128

obtained directly. By using the microcontroller 89V52RD2 at ALE pin a square wave of 4 MHz frequency is generated, further it is reduced to 20 kHz by using decade counter IC 54LS90. On applying square wave to the input of decade counter the square wave of 400 kHz is obtained at the output. This 400 kHz frequency square waves are again reduced by using two decade counters. The integration of a square wave to triangular wave is achieved by applying a square wave at the input of integrator, gaining a triangular wave at the output of the Integrator.

2.2 Base Drive Circuit

The driver which is used in inverter to drive MOSFET is nothing but the "Concept Scale Driver" or "Base Drive card". The SCALE driver from concept is based on chipset that was developed specially for the reliable driving and safe operation of MOSFET's. Features of Scale Driver are (i) Short circuit and over current protection (ii) Extremely reliable, long service life (iii) Electrical isolation from 500 V to over 10 kV (iv) High Gate current from ±6 to ±30 A. There are two inputs A and B. The input to this scale driver is sine weighted 180 upper level PWM signals. Then two outputs (channel 1 and gate channel 2) are provided by SCALE driver. This output is given to the MOSFET's Gate terminal. A spike at the gate terminal of the MOSFET and this is done by Concept SCALE Driver. Emitter and Collector terminal are connected to the emitter sense channel and the collector sense channel of SCALE driver respectively. When Base drive card gives 1 A spike at every pulse the inverter card generates sine waveform which is 180° phase shifted. It provides all types of protection to the inverter card.

3 Numerical Simulation and Experimental Results

The performance of proposed circuit is verified with experimental and simulation result. Table 2 gives the detail of designed parameters of inverter with filter taken for investigation under balanced conditions. Figures 3 and 4 show phase and line output voltages waveforms of three-phase inverters. The windings of each phase of inverter are having spatial displacement of 120° as evaluated in Eqs. (1), (2), (3). The phase current in each winding is shown in Fig. 5. The proposed converter is implemented experimentally and the experimental results are compared with simulation result. For experimentation, the gate signals pattern of the switches of the converter is generated by microcontroller (P89V51RD2) which provides the switching pulses and base drive card is used for the isolation of the pulses obtained

Table 2 Electrical parameters of proposed system

Parameters	Value
Input DC voltage/DC current	29–30 V/85 A
Input DC current	85 A
Output AC voltage	115 V (P-P), 200 V (L-L) with 400 Hz
Output power	2.4 kVA
Load	16.50 Ω (Star)
Transformer	400 Hz, Step-up (30–115 V)

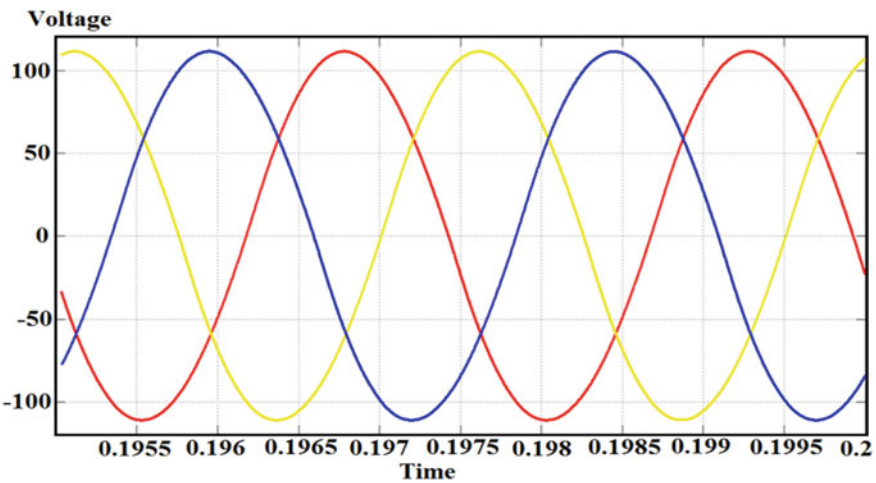


Fig. 3 Phase output voltage waveform

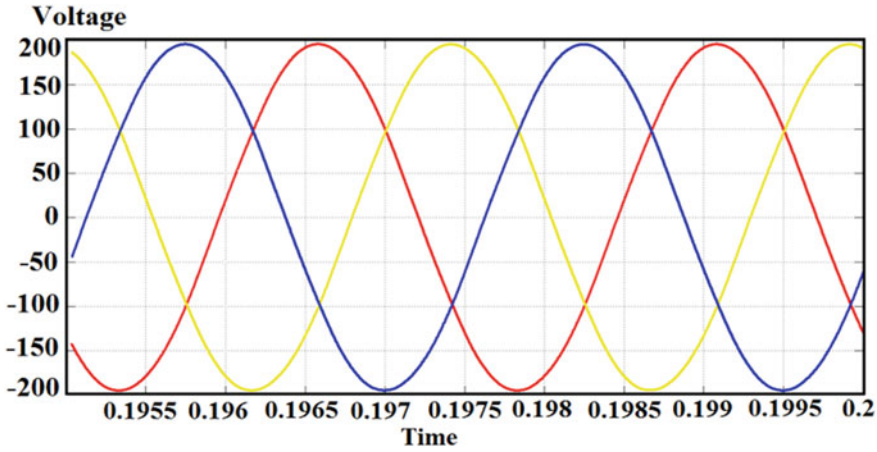


Fig. 4 Line output voltage waveform

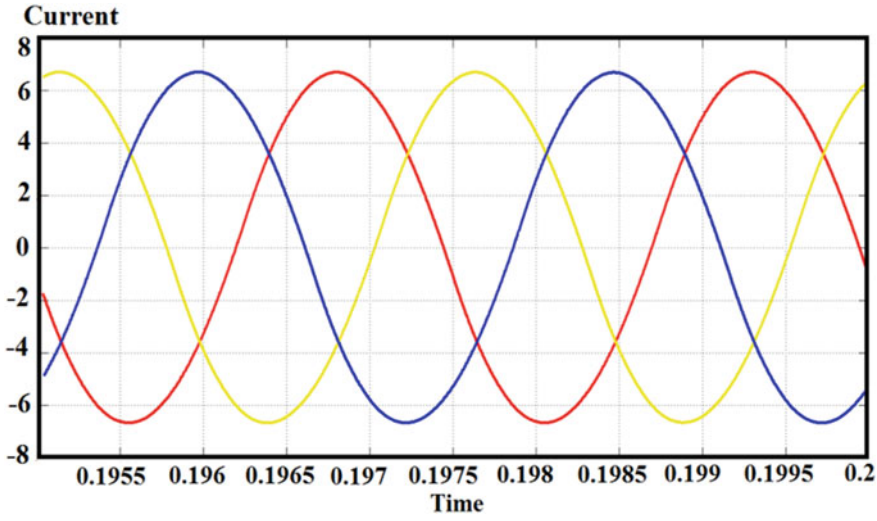


Fig. 5 Current waveform in each phase

from microcontroller. IRF2907-type MOSFETs is used to design proposed converter. The inverter consists of VSI inverter, high frequency transformer and filter.

The hardware setup of proposed system is depicted in Fig. 6. To minimize the distortions and ripple content in inverters SPWM (sinusoidal PWM) with 0.9 modulation index is employed. Also sinusoidal PWM technique is used to eliminate up to harmonic. To eliminate harmonic, an L-C filter of value L = 0.15 mH and C = 4 μf is also used. The odd harmonics content present in square pulse can be

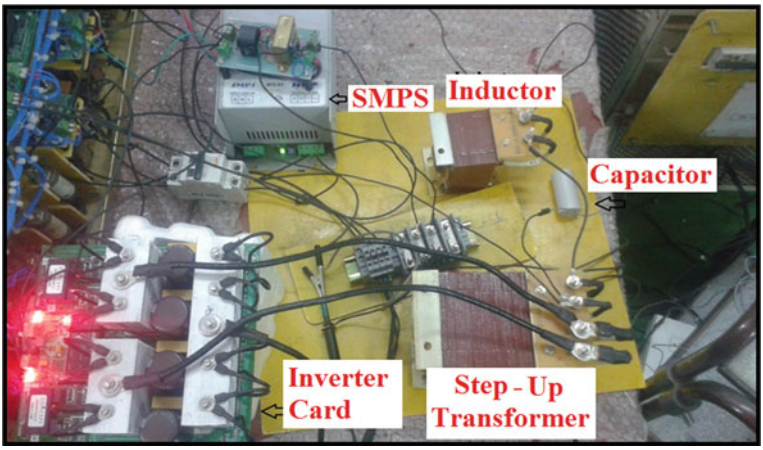


Fig. 6 Experimental prototype model set-up

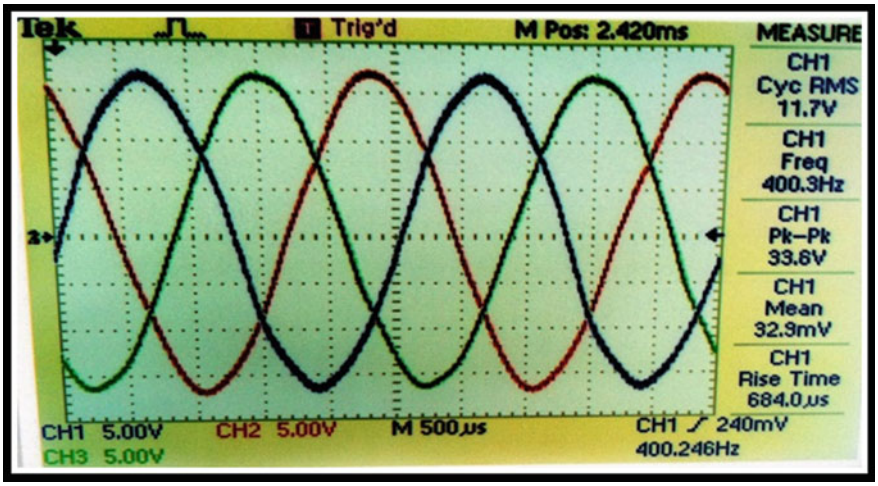


Fig. 7 Three phase output voltage waveform

removed by designing low-pass L-C filter which rejects 20 kHz frequency and passes the 400 Hz waveform. Three phase output waveform of hardware model is shown in Fig. 7. The Total Harmonic Distortion (THD) of output waveform with filters is 2.8% as shown in Fig. 8.

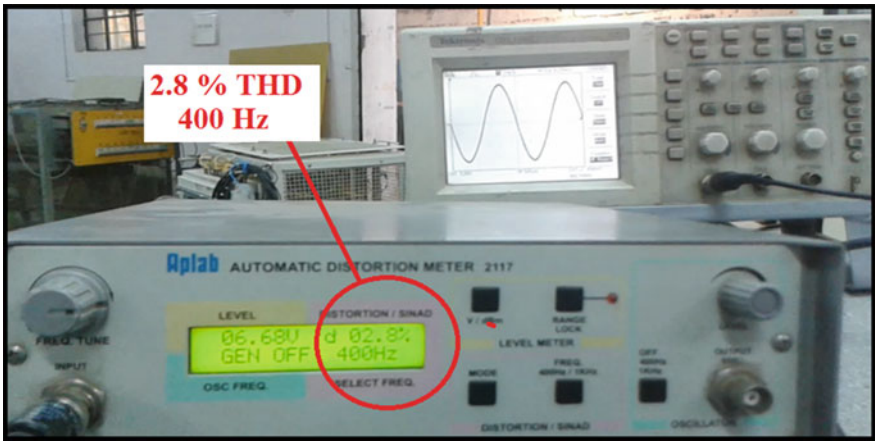


Fig. 8 THD of output waveform

4 Conclusion

Three-phase inverter with power rating 2.4 kW for aircraft application is articulated in this paper. Three-phase output obtained by connecting three single-phase H-bridge inverters in parallel to feed star connected load. The proposed circuit performance is verified with experimental and simulation result. The experimental and simulation result confirms the feasibility of proposed converter for aircraft application.

References

1. Pachagade, R., Mahajan, S., Pandav, K., Maheshwari, R.: A new multilevel inverter with fewer number of control switches. In: IEEE Conference PCCCTSG, India (2015)
2. Draxe, K., Mahajan, S., Pandav, K.: A cascaded asymmetric multilevel inverter with minimum number of switches for solar applications. In: IEEE International Conference PESTSE, India (2014)
3. Sanjeevikumar, P., Blaabjerg, F., Wheeler, P., Kyo-Beum, L., Mahajan, S., Dwivedi, S.: Five-phase five-level open-winding/star winding inverter drive for low-voltage/high-current applications. In: IEEE International conference ITEC, South Korea (2016)
4. Sanjeevikumar, P., Blaabjerg, F., Wheeler, P., Khanna, R., Mahajan, S., Dwivedi, S.: Optimized carrier based five-level generated modified dual three-phase open-winding inverter for medium power application. In: IEEE International conference ITEC, South Korea (2016)
5. Sanjeevikumar, P., Mahajan, S., Pandav, K., Siano, P., Oleschuk, V.: Hexuple-inverter configuration for multilevel nine-phase symmetrical open-winding converter. In: IEEE ICPS, India (2016)
6. Mahajan, S.B., Prasad, W., Gondhalekar, N.: A Modified cascaded H-bridge multilevel inverter for solar applications. In: IEEE ICGCCEE, India (2014)

7. Mahajan, S.B., Pandav, K.M., Revathi, B.: A novel single phase multilevel inverter with single photovoltaic source and less number of switches. IEEE ICDCS, India (2014)
8. Bowes, S.R., Grewal, S.: Modulation strategies for single phase inverter. IET J. Mag. (1998)
9. Chen, D., Xu, L., Zhang, R., Zhang, H.: Combined three-phase inverter with high frequency pulse DC link. IEEE PESC (2005)
10. Constantine C.C., Danila C.: Analyses and simulation of the three-phase controlled inverter using space phasors and spice model. compatibility in power electronics, CPE (2007)
11. Wang, Z., Chang, L.: A novel Vdc voltage monitoring and control method for three-phase grid-connected inverter. CPE (2007)
12. Milanovic, M., Dolinar D., Ravnjak A.: DC to three-phase inverter based on two-phase to three-phase transformation. IEEE ISIE (2002)
13. Isen, E., Bakan, A.F.: 10 kW grid-connected three-phase inverter system: control, simulation and experimental results. IEEE PEDG (2012)

Control Algorithm Concept for AC Voltage Stabilizer Based on Hybrid Transformer with a Matrix Converter

Paweł Szcześniak, Jacek Kaniewski and Padmanaban Sanjeevikumar

Abstract This paper presents the concept of a control algorithm and a study of its properties for an AC voltage stabilizer based on a three-phase hybrid transformer with matrix converter. Presented in this paper is an approach for obtaining continuous control of the voltage magnitude and phase shift using a conventional transformer with two windings and power electronics devices, referred to as a matrix converter. By adjustment of these voltage parameters we can reduce the effects of overvoltage and voltage sags. The concept of a closed-loop control algorithm and properties of the proposed voltage stabilizers are discussed in this paper.

Keywords Hybrid transformer · AC voltage stabilizers · Matrix converter

1 Introduction

Modern home and industrial devices more often are exposed to interference coming from the power grid. The most significant disturbances are: voltage sags, swells and voltage interruptions [1, 2]. Even a short shutdown of industrial process equipment can lead to large additional economical costs connected with: longer production downtimes, costly and complex restart of the production process and waste from the unfinished production process. It is necessary to applied protection of electronic

P. Szcześniak (✉) · J. Kaniewski
Institute of Electrical Engineering, University of Zielona Góra, Zielona Góra, Poland
e-mail: P.Szczesniak@iee.uz.zgora.pl

J. Kaniewski
e-mail: J.Kaniewski@iee.uz.zgora.pl

P. Sanjeevikumar
Department of Electrical and Electronics Engineering, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_34

equipment from the negative effects coming from the power grid. This paper focuses on the problem of voltage sags/swells and a novel concept for their compensation. Power electronic converters enable regulations in levels, frequency and phase shift of voltage at their output connectors. There are two main methods for compensation of voltage disturbance in power systems: parallel–current (STATCOM—static synchronous compensator, SVC—static VAR compensator) and series–voltage (DVR—Dynamic Voltage Restorer, series switching compensator) [1, 2]. A large group of voltage compensators based on conventional electromagnetic transformer with a tap changer [3]. This type of voltage compensators is equipped with thyristor or mechanical tap changer. Tap changers are characterized by relatively low dynamics and step adjustment process. Also the range of voltage regulation using such compensator is small. The group of compensators which are based on power electronic devices (STATCOM, SVC and DVR etc.) guarantees good dynamic properties, and can also control the power flow in the power system [1].

This paper proposes a novel compensation concept for voltage sag, swell and fluctuations, using a hybrid transformer (HT), installed at a typical distribution station. Proposed HT consists of an electromagnetic transformer, which cooperates with the AC/AC power electronics converter with PWM modulation [4–6]. In the HT with series compensator windings, the HT output voltage arises as a result of summation of the power converter output voltage and the voltage of the transformer secondary winding [4–6]. High frequency voltage PWM chopping is employed in the power converter to continuously adjusted the RMS value of the output voltages and/or voltage phase shift. The main difference between the HT and power electronic transformers (PET) [7–9] is that systems with a HT do not convert all of the energy through the power converter. Part of the energy flows only through the power converter. In the literature, one can find many different solutions of hybrid compensators [4–6, 10–16]. The main focus of this paper is to present concepts of the HT and their use in solving voltage stabilization problems in the quality of electric power affecting the energy consumer. Basic topologies and their adjustment capabilities will be presented. In addition, the study of the properties of the topology of the selected HT with matrix converter MC [11] with a proposed closed-loop control algorithm will be presented.

2 Hybrid Transformer Configurations

As mentioned earlier, the HT concept offers important benefits when applied to the distributed grid due to the high levels of available functionality and the potential to improve energy power quality when compared to standard station transformers. An example of the classification of hybrid transformers is shown in Fig. 1 [5]. The first division of HTs relates to a method for electrical energy injection into the system by the power electronic converter. Transformers with parallel and serial methods of energy injection can be distinguished. The second classification relates to the use of

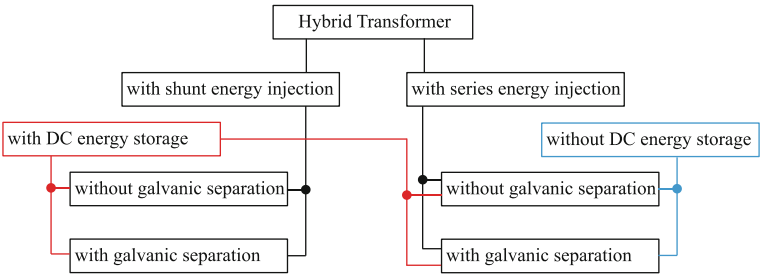


Fig. 1 Diagram of possible hybrid transformer configurations

power electronic converters and here we distinguish systems with and without DC energy storage. The HTs with an AC/AC power converter without DC energy storage are used in a subset of devices with series energy injection into the system. They can be used either as AC/AC choppers [17] or matrix converters (direct or indirect) [18]. Systems with DC energy storage have their advantages and disadvantages. The advantages of the system may include the ability to compensate large voltage dips, with correspondingly large energy storage devices. On the other hand, the disadvantage of such systems is the price, size and reliability of DC energy storage [19]. In the proposed systems it should be considered whether it is necessary to use expensive DC energy storage. The question is whether there are enough systems without energy storage, with a smaller range of voltage dip compensation. A final division of HTs relates to the use galvanic separation (GS) between the power converter input and/or load terminals. The converter can be powered directly from a HT load terminal or from an additional transformer winding. Similarly, the output voltage of the converter can be added together with a second winding voltage directly or via an additional separating transformer.

The examples of HT configurations in the form of single-phase model are depicted in Fig. 2 [5]. Topologies in Fig. 2a–d include circuits with DC energy storage with shunt (Fig. 2a, b) and series (Fig. 2c, d) energy transmission to the compensated system. Whereas topologies in Fig. 2e–i represent concepts of HTs with AC–AC converters which are supplied from compensated lines. The converter can be fed directly from a compensated line (Fig. 2e, g) or with the use of additional windings in the electromagnetic transformer (Fig. 2f, h, i). Also, the output of the converter can be connected to the load through the separation transformer as shown in Fig. 2e, f. In HT systems, there may be used any of the PWM AC/AC converters, e.g., AC/DC/AC with voltage source inverter (VSI), matrix and matrix-reactance choppers, matrix converter or AC/DC/DC/AC with high frequency transformer (HFT) [17]. In using a system with AC/DC/AC converter there can be connected an additional DC energy storage to support the compensation process.

By analogy to the topology of a single-phase HT, a three-phase hybrid transformer can be created. Figure 3 shows the four configurations of three-phase converters which are used in the proposed HT solutions [17–19]. The first topology is called a matrix chopper, and is used to adjust AC voltage amplitude on the output

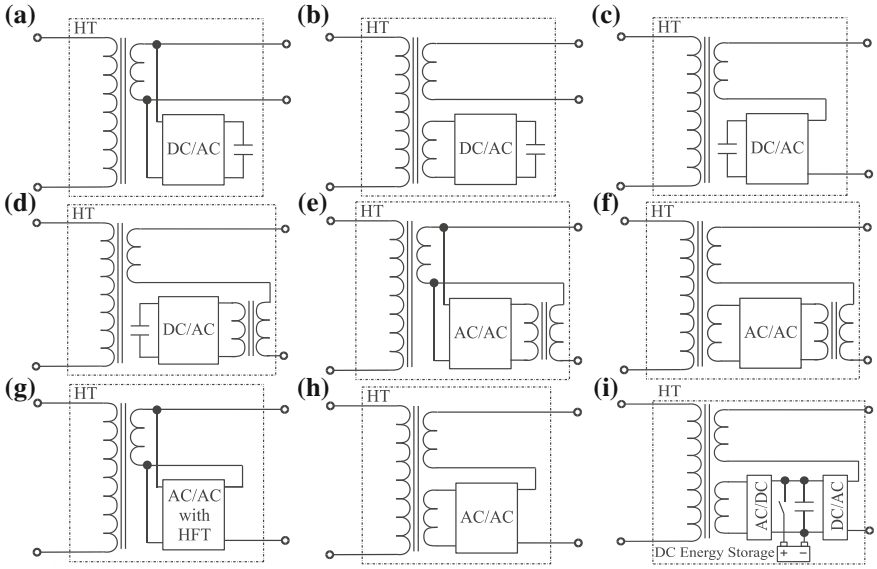


Fig. 2 The single-phase realizations of different configurations of HTs: **a** shunt without galvanic separation (GS) and with DC energy storage, **b** shunt with GS and with DC energy storage, **c** series with DC energy storage, **d** series with DC energy storage and GS, **e**, **f** series without DC energy storage and GS, **g** series with HFT, **h** series with AC/AC converter with GS, **i** series with AC/DC/AC converter and additional DC energy storage element and GS

connectors. The output voltage is adjustable from zero to the supply voltage (buck regulation) [17]. Using the matrix-reactance chopper topology, shown in Fig. 3b, it is also possible to adjust the amplitude of the output voltage but it is the buck–boost regulation [17]. In the articles presenting the properties of this type of HT [4, 6, 19] there were used transformers with a windings gain equal to n_a = 1:4/3 and n_b = 1:2/3 respectively. Whereas, in the HT structure a frequency converter topology is used, presented in Fig. 3c (back-to-back converter) or in Fig. 3d (matrix converter) [18], thus yielding the possibility to control the RMS value and phase shift of output voltages—which gives the HT topology an additional degree of regulation. In this type of HT it is possible to use an electromagnetic transformer with a winding voltage gain equal to $n_a = n_b$ = 1:1. This transformer windings configuration allows disconnection of compensating windings from the power converter during nominal conditions of supply voltage. Then the compensation winding may be short-circuited by the bypass switch, thereby increasing the energy efficiency of the whole system. It should be noted that all the converters shown in Fig. 3 use an input and output low pass LC filter to minimize higher harmonics of voltages and currents. This article will discuss only the topology of HT with MC [11]. In addition, the proposed control algorithm in a closed-loop feedback will be presented. Also, in order to verify the proposed algorithm and the effectiveness of voltage distortion compensation the selected simulation results will be shown.

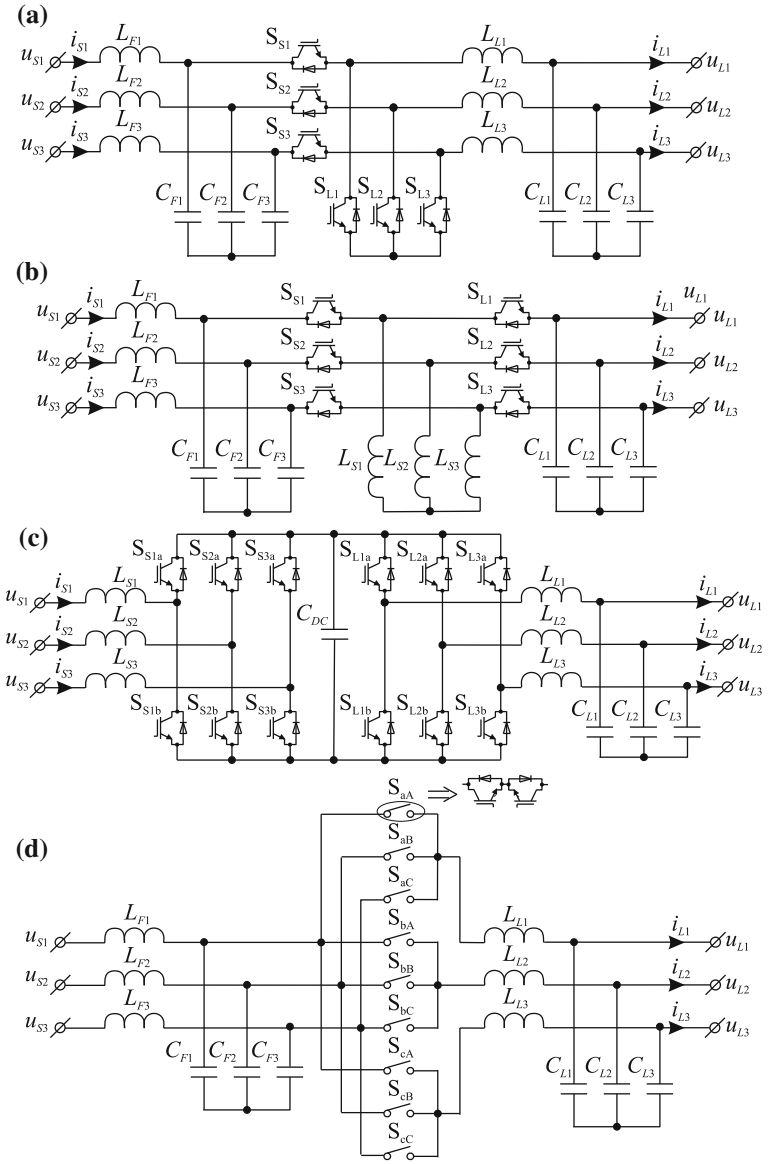


Fig. 3 Three-phase converters which can be used in proposed HT solutions: **a** matrix chopper, **b** buck–boost matrix-reactance chopper, **c** back-to-back frequency converter, **d** matrix converter

3 AC Voltage Stabilizer Based on Hybrid Transformer with Matrix Converter and Proposed Control Algorithm

A schematic diagram of the considered three-phase AC voltage stabilizer based on a hybrid transformer with matrix converter and the proposed control algorithm is shown in Fig. 4 [11]. As illustrated in Fig. 1, the proposed system consists of two main units: a three-phase matrix converter and a conventional transformer with two taps for each of the output phases. The voltage turn ratios of both windings are equal 1:1.

The hybrid transformer output voltage is the sum of the matrix converter output voltage and voltage of the first secondary winding. The matrix converter output voltage is adjusted using voltage gain q and the voltage phase shift φ_L. The reference voltage signals and phase shift φ_L are calculated in a PLL unit. Reference MC voltage gain q_{ref} is calculated from the signals coming from the d-q detector of sag/swell input voltage and the d-q detector of output voltage amplitude (Fig. 4) [20]. The signals from these detectors are reference and measurement signals of PI controller. After adding the output signal of the PI controller, values of q coefficient and the constant factor k there is obtained the value of the

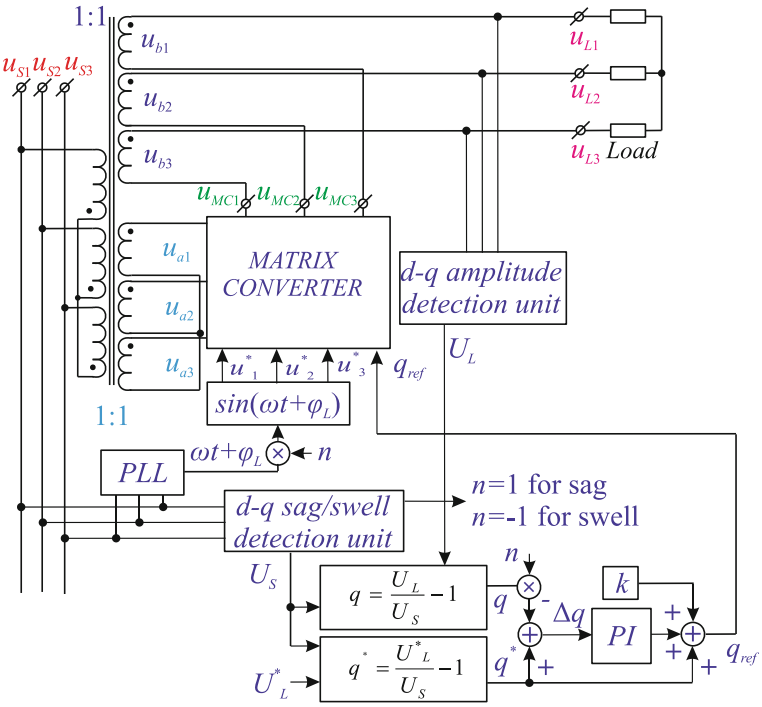


Fig. 4 AC voltage stabilizer based on hybrid transformer with matrix converter and proposed closed-loop control algorithm

reference voltage gain q_{ref}. The values of coefficients q and q^* stem from the principle of compensation, the output voltage is the sum of the source and compensator voltages

$$U_L = U_S + U_C = (1+q)U_S \Rightarrow q = \frac{U_L}{U_S} - 1 \Rightarrow q^* = \frac{U_{L\text{ref}}}{U_S} - 1 \tag{1}$$

In addition, in the control unit the information signal n is generated. It informs whether there has been a voltage sag ($n = 1$) or voltage swell ($n = -1$). Coefficient n determines the phase shift φ_L of the reference voltage and the sign of factor q in the feedback loop. These signals are multiplied by the coefficient n (Fig. 4). For modulation of the matrix converter switch function, the space vector modulation (SVM) technique has been used [18, 21]. The SVM method for the MC has been described many times in various publications. Therefore, this article will not give detailed information about SVM. More information can be obtained in the following publications: [18, 21].

In order to verify the proposed control algorithm and the effectiveness of voltage distortion compensation the selected simulation results will be presented. Figure 5a shows the time waveforms of the AC voltage stabilizer based on the HT with MC during a step change in the sag of source voltages from 1.0 to 0.5 pu, obtained during the simulation with the help of Matlab Simulink. In this figure, there are presented the following time waveforms: from the top down, source voltage, HT output voltage in first phase, MC output voltage after the LC filter in first phase, line-to-line MC output voltage before the LC filter, reference and measurement amplitude of load voltage, and finally, the time waveforms at the bottom is the value of the setting MC voltage gain q_{ref}. As can be seen from the displayed waveforms, the proposed control system in a closed loop perfectly fulfils its job. At the output is kept constant voltage amplitude, and the step change of the source voltage parameters are compensated with very good dynamics. In the proposed solution it is possible to compensate the voltage sag with a depth of up to 53.6%. Where the voltage sag is deeper, it is not a fully compensated, as seen in Fig. 5a in the range of 0.5–0.6 s.

Corresponding waveforms to those shown in Fig. 5a are presented in Fig. 5b during step changes in the overvoltage of source voltages from 1.0 to 1.5 pu. Moreover, the presented waveforms show the proper operation of the AC voltage compensator with very good dynamics and precision.

It should be emphasized that the presented method is not optimal in terms of the number of measured signals and the ability to compensate for different variations in mains voltage distortion. A large number of voltage sags in the power network are single-phase or unbalanced sags, resulting from a single-phase short circuit to ground, a two-phase short circuit or a two-phase short circuit to ground. The analysis of this type of compensation requires a complex form of power converter switch modulation strategy [11].

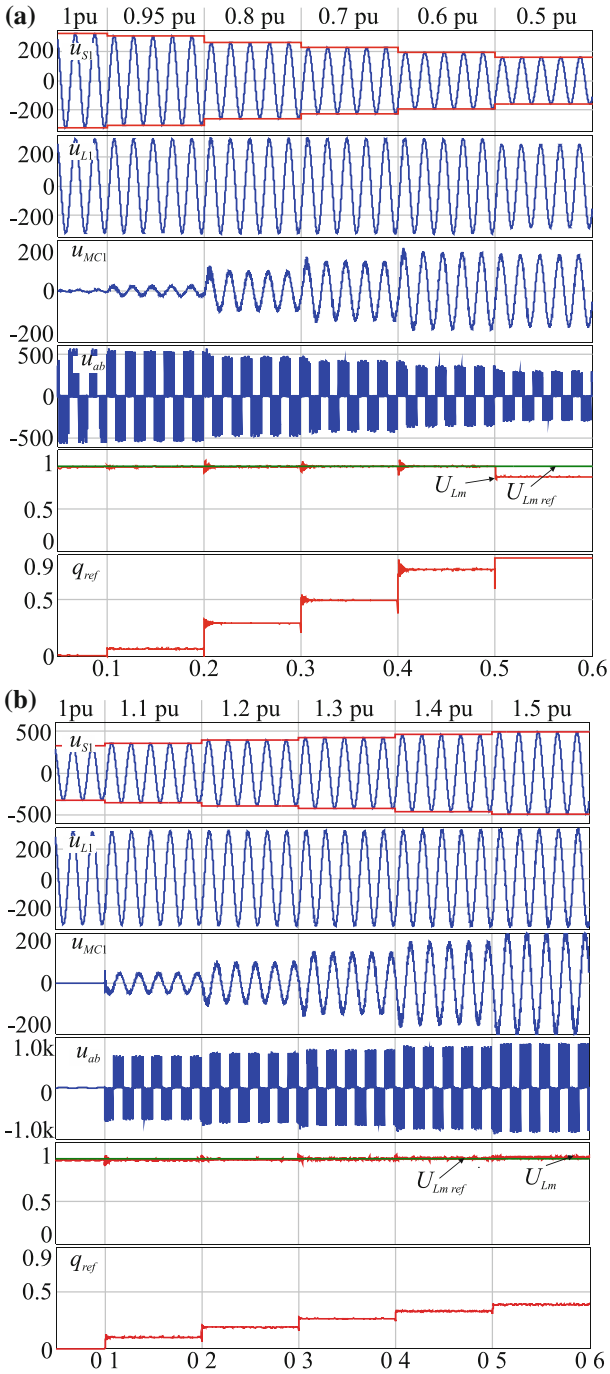


Fig. 5 Simulation results of a AC voltage stabilization using HT with MC and proposed closed-loop control algorithm: **a** during voltage sag, **b** during voltage swell

4 Conclusion

The paper has dealt with the concept of a hybrid transformer with power electronic converter without DC energy storage element as the compensator of voltage fluctuation at the point of common coupling of the industrial consumer for the supply of selected loads or the whole plant. The HT thanks to the application of a power electronic converter has the capability of fluent regulation of voltage at its load connectors. A few concepts of three-phase AC voltage compensators based on the hybrid transformer have been discussed in this article. In some detail the compensator with hybrid transformer including matrix converter has been discussed. The electrical circuit scheme, its operational conditions and the proposed closed-loop control algorithm have been described. In order to verify the proposed control algorithm and the effectiveness of voltage distortion compensation with the help of the proposed HT, selected simulation results have been shown. The proposed HT is able to compensate symmetrical voltage sags and overvoltage, as shown in the simulation investigation.

It should be emphasized that such a system may already be easily implemented to protect consumers in the power range equal to a few kVA. The next step of the research will focus on experimental applications and verification of properties in closed-loop control. Also part of further research will be checking operational properties of the proposed AC voltage compensator for unbalanced voltage distortion as well as defining a compensation range of voltage sag and overvoltage.

Acknowledgements The research was carried out within the scope of the project funded by the "National Science Centre, Poland" under the reference number 2015/19/D/ST7/01371.

References

1. Benysek, G.: Improvement in the Quality of Delivery of Electrical Energy Using PE Systems. Springer, London (2007)
2. Moreno-Munoz, A.: Power Quality: Mitigation Technologies in a Distributed Environment. Springer, London (2007)
3. Choi, J.-H., Moon, S.-I.: The dead band control of LTC transformer at distribution substation. IEEE Trans. Power Sys. **24**(1), 319–326 (2009)
4. Kaniewski, J., Fedyczak, Z., Benysek, G.: AC voltage sag/swell compensator based on three-phase hybrid transformer with buck-boost matrix-reactance chopper. IEEE Trans. Ind. Electron. **61**(8), 3835–3846 (2014)
5. Burkard, J., Biela, J.: Evaluation of topologies and optimal design of a hybrid distribution transformer. In: European Conference on Power Electronics and Applications, In Proceedings EPE '15 ECCE Europe, Geneva, Switzerland, pp. 1–10 (2015)
6. Kaniewski, J.: Practical application of series active compensators. In: Benysek, G., Pasko, M (eds.) Power Theories for Improved Power Quality, pp. 187–210. Springer, London (2012)
7. She, X., Huang, A.Q., Burgos, R.: Review of solid-state transformer technologies and their application in power distribution systems. IEEE J. Emerg. Sel. Topics Power Electron. **1**(3), 186–198 (2013)

8. Kolar, J.W., Ortiz, G.: Solid-state-transformers: key components of future traction and smart grid systems, In: Proceedings of the International Power Electronics Conference, IPEC and Proceedings of ECCE Asia 2014, Hiroshima, pp. 18–21 (2014)
9. Pinto, S.F., Mendes, P.V., Silva, J.F.: Modular matrix converter based solid state transformer for smart grids. Electr. Power Syst. Res. **136**, 189–200 (2016)
10. Kaniewski, J., Szcześniak, P., Jarnut, M., Benysek, G.: Hybrid voltage sag/swell compensators: a review of hybrid AC/AC converters. IEEE Ind. Electron. Mag. **9**(4), 37–48 (2015)
11. Szcześniak, P., Kaniweski, J.: Hybrid transformer with matrix converter. IEEE Trans. Power Del. **31**(3), 1388–1396 (2016)
12. Haj-Maharsi, M.Y., Tang, L., Gutierrez, R., Bala, S.: Hybrid distribution transformer with ac & dc power capabilities. US Patent US 2010/0201338 A1, ABB Research Ltd. (2010)
13. Haj-Maharsi, M.Y., Bala, S., Tang, L.: Hybrid distribution transformer with an integrated voltage source converter. US Patent US2010/0220499 A1, ABB Research Ltd. (2010)
14. Radi, M.A., Darwish, M., Alqarni, M.: Voltage regulation considerations for the design of hybrid distribution transformers. In: Proceedings of UPEC 2014, pp. 1–6 (2014)
15. Sastry, J., Bala, S.: Considerations for the design of power electronic modules for hybrid distribution transformers. In: Proceedings of ECCE 2013, pp. 1422–1428 (2013)
16. Bala, S., Das, D., Aeloiza, E., Maitra, A., Rajagopalan, S.: Hybrid distribution transformer: concept development and field demonstration. In: Proceedings of ECCE 2012, pp. 4061–4068 (2012)
17. Szcześniak, P., Kaniewski, J., Jarnut, M.: AC-AC power electronic converters without DC energy storage: a review. Energ. Convers. Manage. **92**, 483–497 (2015)
18. Szcześniak, P.: Three-Phase AC-AC power converters based on matrix converter topology. Matrix-Reactance Frequency Converters Concept. Springer, Berlin (2013)
19. Szcześniak, P., Kaniewski, J.: Power electronics converters without DC energy storage in the future electrical power network. Elec. Power Syst. Res. **129**, 194–207 (2015)
20. Nielsen, J.G., Blaabjerg, F., Mohan, N.: Control strategies for dynamic voltage restorer compensating voltage sags with phase jump. In: Proceedings APEC 2001, vol. 2, pp. 1267–1273 (2001)
21. Rodriguez, J., Rivera, M., Kolar, J.W., Wheeler, P.W.: A review of control and modulation methods for matrix converters. IEEE Trans. Ind. Electron. **59**(1), 58–70 (2012)

Design and Analysis of Ultra-Low Power QCA Parity Generator Circuit

Trailokya Nath Sasamal, Ashutosh Kumar Singh and Umesh Ghanekar

Abstract Quantum-dot cellular automata (QCA) are a new paradigm in nanoscale technology with high frequency and low power consumption capabilities. This work presents a low complexity two-input XOR gate, which achieves low power consumption compared to prior ones using an efficient five-input majority gate. To show the novelty of this structure, different bits even parity generators are addressed. The result shows proposed parity generators are more superior over the existing designs. We show a 32-bit even parity generator, which requires 40% less cell count and saves 50% area occupation over the previous best design. QCA Designer-2.0.3 and QCA Pro have been considered to evaluate the accuracy of presented designs and to evaluate the power dissipation respectively.

Keywords QCA · Parity generator · XOR gate · Majority gate Power dissipation

1 Introduction

In traditional CMOS-based VLSI technology, as size of the devices are shrinking, devices are exposed to circuit noise and yield high leakage current [1, 2]. Several nanoscale devices have been gained popularity in research community during recent years. These include technologies like quantum-dot cellular automata (QCA), tunneling phase logic (TPL), single electron tunneling (SET), and carbon nanotube (CNT). In this aspect, QCA could be a feasible competitive alternative,

T.N. Sasamal (✉) · U. Ghanekar
Department of Electronics & Communication, NIT Kurukshetra, Kurukshetra, India
e-mail: tnsasamal.ece@nitkkr.ac.in

U. Ghanekar
e-mail: ugnitk@nitkkr.ac.in

A.K. Singh
Department of Computer Applications, NIT Kurukshetra, Kurukshetra, India
e-mail: ashutosh@nitkkr.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_35

which promises ultra-low power consumption with molecular size and high speed operation [3, 4]. It provides a new horizon for the information computation, where a binary data is represented by charge configuration. The binary information is propagated due of polarization between two cells. Unlike traditional CMOS circuits, QCA-based circuits carry no current, therefore, transfer of logic does not contribute to the total energy dissipation [5]. This paper is structured as follows: QCA logic and clocking preliminaries are demonstrated in Sect. 2. Section 3 introduces an optimal coplanar two-input XOR gate circuit based on five-input majority gate. Simulated results of proposed designs and comparative analysis are inspected in Sect. 4 by considering previous works. Finally paper concludes in Sect. 5.

2 QCA Preliminaries

2.1 QCA Logic

The main unit of QCA is a quantum well cell. It has four quantum-dots located on four vertices of a square. Two injected electrons are free to occupy any of the four dots based on columbic repulsion among them. These two electrons position at the two corners due to repulsion and yield two possible polarizations as shown in Fig. 1a [6]. By applying proper clocks electrons are able to tunnel through the inter dot barrier by electrons interaction. Any digital circuits can be made of a combination single QCA cells. In QCA circuits, majority gates and inverters are the essential elements. Two different layouts of an inverter are shown in Fig. 1c, d. The Boolean equation of a majority gate is expressed as MV (a,b,c) = ab + bc + ca. In Fig. 1e, QCA implementation of a majority gate is shown [7]. By fixing one of the inputs to '0' or '1', an AND gate or OR gate can be realized. Input signals can be made available at the output end, if QCA cells are positioned in serial manner, as depicted in Fig. 1b.

2.1.1 QCA Clocking

For proper functioning of QCA circuits, clocks are necessary. QCA clocking serves two requirements: information synchronization, and delivers required power gain for the cell. This clocking scheme allows the electrons in a cell to arrange themselves by breaking the inter dot barrier. Generally, it requires four phase clocking scheme. The QCA circuit is divided into four clock zones, where individual zone is distinct with 90° phase shifted to one another. A clock zone defines four phases: *Switch*, *Hold*, *Release*, and *Relax* [8].

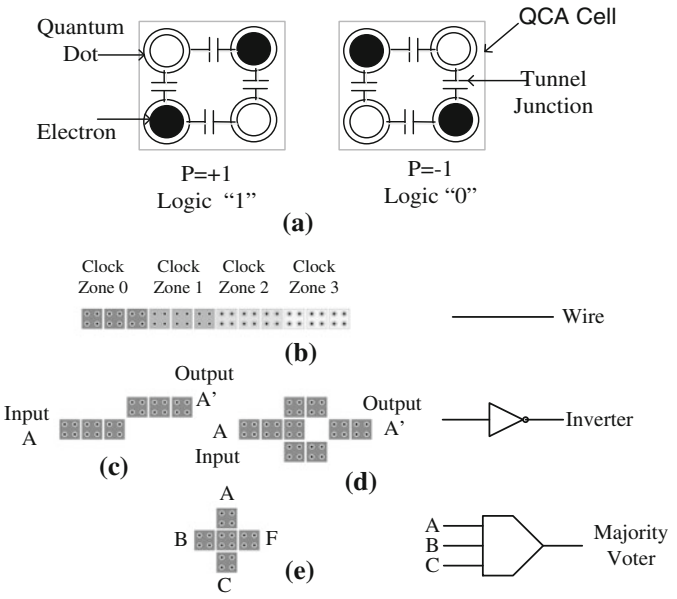


Fig. 1 QCA logic **a** cell **b** wire **c**, **d** inverters **e** majority voter (MV) gate

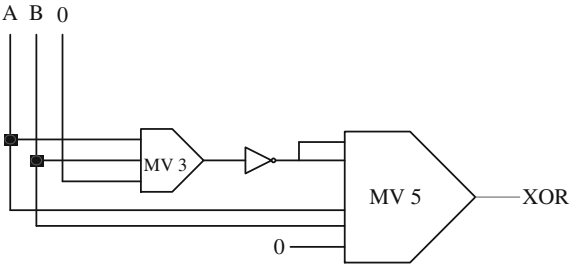


Fig. 2 XOR schematic diagram

3 Proposed Structures

3.1 Proposed XOR Circuit

In this section, an efficient two-input XOR gate is presented based on the design in [9]. A schematic for the gate is depicted in Fig. 2. It comprises one inverter, one three-input, and five-input majority gate. The Boolean representation of this structure can be formulated as

$$\mathrm{XOR} = \mathrm{MV5}(\mathrm{A}, \mathrm{B}, 0, \overline{\mathrm{MV3(A,B,0)}},\ \overline{\mathrm{MV3(A,B,0)}}) = \overline{\mathrm{A}}\mathrm{B} + \mathrm{A}\overline{\mathrm{B}} \qquad (1)$$

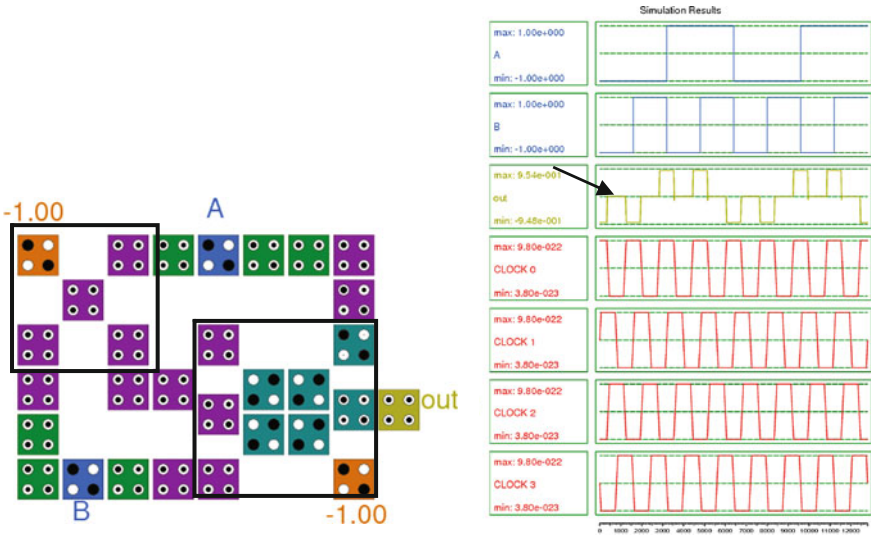


Fig. 3 **a** Layout of proposed XOR gate. **b** Simulation result for proposed XOR gate

Figure 3a shows the QCA realization of the proposed XOR gate, which allows accessing both input and output cells using coplanar QCA technology. This structure composed of a novel five-input and rotated three-input majority gate [9] represented by solid squares. It is worth noting that this optimal single layer layout requires only 0.75 clock cycles to generate a valid output. The simulation waveforms for our two-input XOR gate is illustrated in Fig. 3b. It is easy to perceive that our structure results correct output at clock 2 as pointed by black arrow.

3.2 *Power Dissipation Analysis*

To measure the power consumption of the presented XOR gate and existing ones, QCAPro [10] has been used as a power evaluator tool. For evaluation three different tunneling energies are taken (0.5 E_k, 1.0 E_k, 1.5 E_k) at 2 K temperature. Figure 4 shows energy dissipation map of our proposed XOR gate with tunneling energy of 0.5 E_k. Cells with higher power dissipation are represented by darker colors in thermal hotspot maps. A comparative analysis of power consumption is depicted in Table 1, where leakage and switching energies contribute to total energy dissipation. As is shown, the proposed design is superior over the designs [11–13] and one of the designs in [14] achieves least leakage energy. However, proposed gate produces less switching energy and the total energy dissipation is much lower than existing designs [11–14] for different tunnelling energies. This low power and minimum area features facilitate designers to realize ultra-low power and complex QCA circuits.

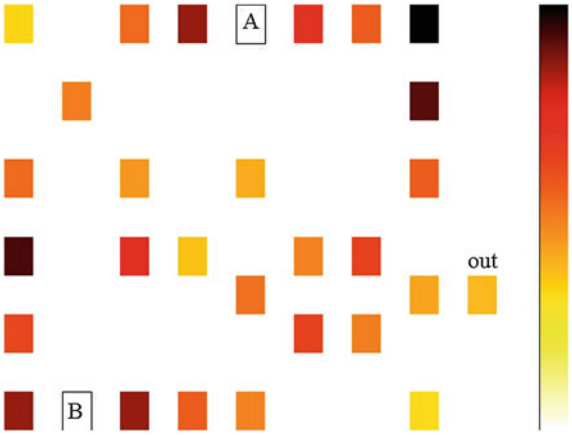


Fig. 4 Power dissipation map for proposed 2-input XOR gates at 2 K temperature and tunneling energy of 0.5 E_k

Table 1 Power consumption comparative analysis

Designs	Avg. leakage energy dissipation (meV)			Avg. switching energy dissipation (meV)		Total energy dissipation (meV)			
	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k	0.5 E_k	1 E_k	1.5 E_k
[13]	19.54	59.09	106.32	127.35	112.84	98.43	146.89	171.93	204.75
[14]	14.71	47.84	87.41	82.39	70.67	59.38	97.1	118.51	146.79
[12]	18.11	54.40	95.40	65.02	53.94	44.37	83.13	108.34	139.77
[12]	11.87	37.32	67.15	57.54	49.11	41.13	69.41	86.43	108.28
[14]	11.18	33.42	58.34	38.23	31.43	25.70	49.41	64.85	84.04
[11]	11.51	31.91	54.69	35.78	30.48	25.66	47.29	62.39	80.35
Proposed	11.64	31.85	53.68	27.42	21.78	17.40	39.06	53.63	71.08

4 Results and Discussions

Simulator QCA Designer-2.0.3 has been used to check the functionality of the proposed circuits [15]. The simulation engine used bi-stable approximation with following parameters cell size = 18 nm, number of samples = 50,000, convergence tolerance = 0.001, radius of effect = 65 nm, relative permittivity = 12.9, clock high = $9.8e^{-22}$ J, clock low = $3.8e^{-23}$ J, clock amplitude factor = 2, layer separation = 11.5 nm, maximum iterations per sample = 100.

Table 2 illustrates the difference between proposed XOR gate and previous coplanar designs over different performance parameters. It is worth to notice that the complexity, area occupation and delay of the proposed XOR design outperform the previous designs [11–14].

Table 2 Structural analysis of coplanar 2-input XOR gate

XOR circuits	Area (μm^2)	Cell count	Delay (clocks)	Cross-over type
[11]	0.02	32	1	Coplanar
[12]	0.07	41	1	Coplanar
	0.09	55	2	Coplanar
[13]	0.06	67	1.25	Coplanar
[14]	0.06	34	1	Coplanar
	0.05	42	0.5	Coplanar
Proposed	0.02	30	0.75	Coplanar

Table 3 Comparison of parity generator designs

Designs	Bits	Cell count	Area (μm^2)	Delay (clocks)
[16]	4	187	0.32	2.75
	8	456	0.92	4
	16	1024	2.41	5.25
	32	2220	5.96	6.5
[17]	4	168	0.28	2.75
	8	408	0.8	4
	16	912	2.09	5.25
	32	1968	5.16	6.50
[13]	4	188	0.2	2.25
	8	369	0.49	2.25
	16	847	1.46	3.25
	32	1862	3.58	4.25
Proposed	4	97	0.1	1.75
	8	235	0.3	2.75
	16	523	0.76	3.75
	32	1126	1.82	4.75

A thorough comparison between recent even parity generator designs and our proposed one are depicted in Table 3 for operands word lengths ranging from 4- to 32-bit. Clearly, the presented structures exhibit more superiority over known designs in the literature [13, 16, 17] with respect to cell complexity, spanning area and delay. For example, a compact 32-bit parity generator design shown in Fig. 5 is made of 1126 cells, which is 63.3% less than the most optimized design in this segment [13]. In addition, it is worth noting that the proposed 32-bit parity generator gains 92% improvement in area occupation.

In addition, we have also studied the effect of temperature variation on the output polarization to evaluate the robustness of the presented two-input XOR gate. From Fig. 6, it can be concluded that the output polarization remains positive for a wide range of temperature, and start decreasing after 16 K, where the output cell results logic 1 for polarization of 0.568.

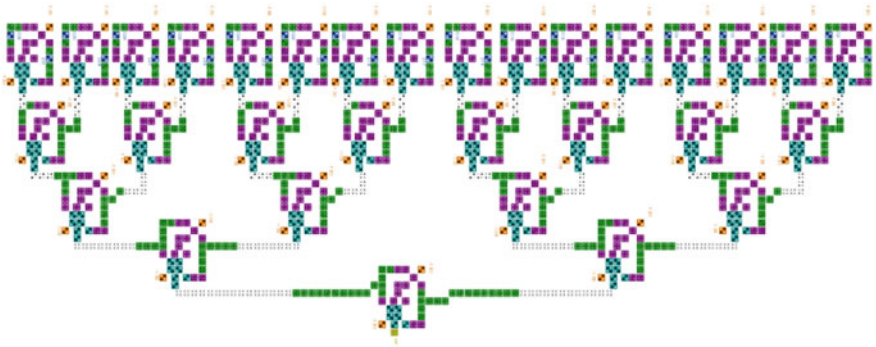


Fig. 5 Proposed QCA layout for 32-bit even parity generator

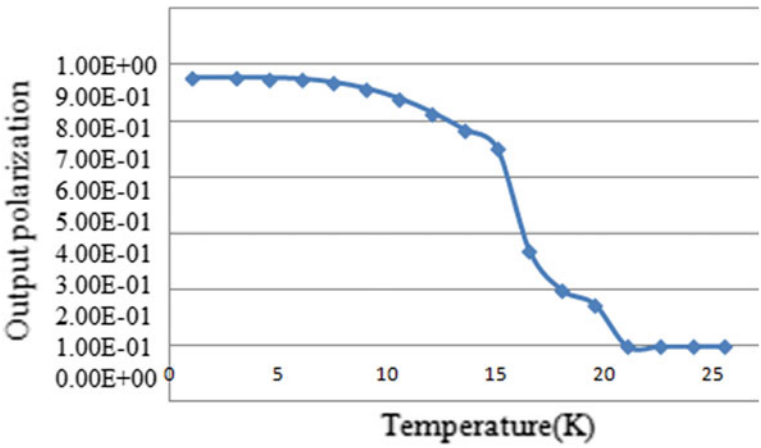


Fig. 6 Temperature versus output polarization for the proposed XOR gate

5 Summary/Conclusion

Designing an efficient and coplanar QCA XOR is of great importance in error detection circuits in digital data transmissions. In this work, a power efficient two-input QCA XOR was reported. A compact and low power five-input majority gate was considered as the building block for the proposed XOR gate. Further, we designed and implemented parity generator circuit of various lengths using the proposed XOR gate. The comparison results show that the presented structures outperformed existing best designs with respect to area occupation, latency, cell counts. These structures are more suitable elements for realizing complex and high-performance QCA circuits.

References

1. Zhang, R., Walus, K., Wang, W., Jullien, G.A.: A method of majority logic reduction for quantum cellular automata. IEEE Trans. Nanotechnol. **3**, 443–450 (2004)
2. Orlov, A.O., Amlani, I., Bernstein, G.H., Lent, C.S., Snider, G.L.: Realization of a functional cell for quantum-dot cellular automata. Science **277**, 928–930 (1997)
3. Tougaw, P.D., Lent, C.S.: Logical devices implemented using quantum cellular automata. Appl. Phys. **75**, 1818–1824 (1994)
4. Lent, C.S., Tougaw, P.D., Porod, W., Bernstein, G.H.: Quantum cellular automata. Nanotechnology **4**, 49–57 (1993)
5. Hossein, A., Behjat, F., Ali, A.K.: High-performance low-leakage regions of nano-scaled CMOS digital gates under variations of threshold voltage and mobility. J. Zhejiang Univ. Sci C **13**, 460–471 (2012)
6. Timler, J., Lent, C.S.: Power gain and dissipation in quantum-dot cellular automata. J. Appl. Phys. **91**, 823–831 (2002)
7. Lent, C.S., Tougaw, P.D.: A device architecture for computing with quantum dots. Proc. IEEE **85**, 541–557 (1997)
8. Toth, G., Lent, C.S.: Quasi adiabatic switching for metal-island quantum-dot cellular automata. J. Appl. Phys. **85**, 2977–2984 (1999)
9. Sasamal, T.N., Singh, A.K., Mohan, A.: An optimal design of full adder based on 5-input majority gate in coplanar quantum-dot cellular automata. Optik **127**(20), 8576–8591 (2016)
10. Srivastava, S., Asthana, A., Bhanja, S., Sarkar, S.: QCA Pro-an error power estimation tool for QCA circuit design, In: IEEE International Symposium Circuits System, pp. 2377–2380 (2011)
11. Sheikhfaal, S., Angizi, S., Sarmadi, S., Moaiyeri, M.H., Sayedsalehi, S.: Designing efficient QCA logical circuits with power dissipation analysis. Microelectron. J. **46**, 462–471 (2015)
12. Mustafa, M., Beigh, M.R.: Design and implementation of quantum cellular automata based novel parity generator and checker circuits with minimum complexity and cell count. Indian J. Pure Appl. Phys. **51**, 60–66 (2013)
13. Angizi, S., Alkaldy, E., Bagherzadeh, N., Navi, K.: Novel robust single layer wire crossing approach for exclusive or sum of products logic design with quantum-dot cellular automata. J. Low Power Electron. **10**, 259–271 (2014)
14. Beigh, M.R., Mustafa, M., Ahmad, F.: Performance evaluation of efficient XOR structures in quantum-dot cellular automata (QCA). Circuits Syst. **4**, 147–156 (2013)
15. Walus, K., Dysart, T.J., Jullien, G.A., Budiman, R.A.: QCA designer: a rapid design and simulation tool for quantum-dot cellular automata. IEEE Trans. Nanotechnol. **3**, 26–31 (2004)
16. Niemier, M.T.: Designing digital systems in quantum cellular automata master's thesis. University of Notre Dame, Notre Dame, Indiana, USA (2004)
17. Hashemi, S., Farazkish, R., Navi, K.: New quantum dot cellular automata cell arrangements. J. Comput. Theor. Nanosci. **10**, 798–809 (2013)

Modeling of the State Space Vector PWM (SVPWM) Based STATCOM for Voltage Improvement in the Transmission Line

Rubi Kumari and Chitrangada Roy

Abstract In the present era, the increase in population has led to the increase of load as a result the generated voltage is not equal to the received voltage. This has affected the stability of the power system. Flexible Alternating Current Transmission Devices shortly termed as FACTS devices came into use for better voltage regulation and stability in the power system. A Static Synchronous Compensators (STATCOM) is the most effective device among all the other FACTS devices. This paper explains about the State Space Vector Pulse Width Modulation (SVPWM) technique used for generating pulses in the STATCOM to maintain the voltage stability of transmission line in more efficient way. The proposed STATCOM model is able to compensate the voltage dip at 0.6 s transient time due to addition of load in the system. The entire project has been conducted in the MATLAB software

Keywords Static synchronous compensator (STATCOM) · Point of common coupling (PCC) · State space vector pulse width modulation (SVPWM) Flexible alternating current transmission system (FACTS) · Voltage source converter (VSC)

1 Introduction

Nowadays, the voltage stability improvements is very important in the power system. Earlier, mechanically switched shunt and series capacitors, reactors were present to increase the stability of the voltage in the power system. But, power system was not able to achieve the desired result [1]. In order to make the system

R. Kumari · C. Roy (✉)
Department of Electrical & Electronics Engineering, Sikkim Manipal Institute of Technology, Rangpo, India
e-mail: roychitrangada@gmail.com

R. Kumari
e-mail: rubi09kumari@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_36

fast, flexible, and to increase the controlling capability, FACTS devices came into use. Among various FACTS devices STATCOM has been used due to its various advantages over other FACTS device. A STATCOM works like a Voltage Source Converter (VSC). It is a power electronic device used for providing reactive power compensations to high voltage transmission networks. It also contributes for the improvement of the continuous and dynamic voltage profile and provides high efficiency in the power system [1]. In this paper, STATCOM with PI controller has been implemented. The control parameters of the PI controller play an important role in STATCOM performance [2]. There are various methods of providing pulse to the voltage source converter but the most used PWM techniques are Sinusoidal PWM technique and State Space Vector PWM (SVPWM) techniques. In this paper, SVPWM technique has been implemented due to its various advantages such as easy digital realization and better DC bus utilization as compared to the other PWM techniques [3]. This paper gives detailed explanation about the effects of the STATCOM with SVPWM technique so that it gives the desired response at the time of change in load. The results obtained explain how using STATCOM in the transmission networks can improve the voltage dip and increase the voltage stability of the system.

2 System Modeling

The MATLAB blocks represent a three-phase test system model. The test system model comprises of a three-phase source which generates 11 kV at 50 Hz. The voltage has been stepped up to 33 kV using a 11/33 kV, 5 MVA three-phase transformer. The length of three-phase 33 kV pi-section line is 50 km. A 1 MW load has been connected to the 33 kV transmission network. At the receiving end side voltage has been stepped down to 11 kV using a 33/11 kV, 5 MVA three-phase transformer. The receiving end comprises of two RL loads of 1 MW and 4.25 MW at 0.8 pf lagging each. The transient time given to the three-phase breaker is 0.6 s and at that instant the 4.25 MW load is introduced to the system (Fig. 1).

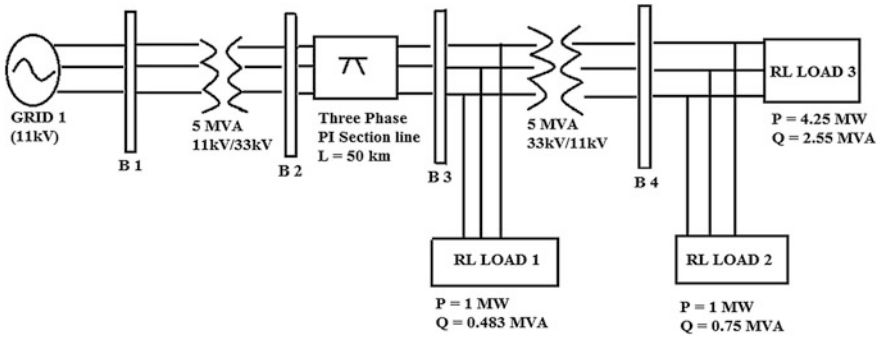


Fig. 1 Three-phase test system model

3 STATCOM Controller Design

A STATCOM is a three-phase Voltage Source Converter (VSC) with a Direct Current (DC) bus capacitor. The simplified equivalent circuit of the STATCOM has been shown in Fig. 2, which comprises of a DC link capacitor, a VSC, three resistors denoted as R_{stat}, and three inductors which has been denoted as L_{stat}. The R_{stat} has been connected in series with the AC transmission lines. The R_{stat} resistance represents conduction losses of the transformer, whereas the L_{stat} inductance represents the filter leakage inductances [4]. The purpose of the STATCOM controller is to make reactive power compensation to the AC power system to improve the voltage downfall in the system. The magnitude and phase of the designed STATCOM output voltage is used to control the exchange of power between STATCOM and the three-phase transmission network [5]. The three-phase equations of the STATCOM have been converted into the d-q components using Clark's transformation method.

The equations of the STATCOM as shown in Fig. 2 can be written as:

$$v_{\text{d}} = R_{\text{stat}} i_{\text{d}} + L_{\text{stat}} \frac{\text{d}i_d}{\text{d}t} - \omega_{\text{e}} L_{\text{stat}} i_{\text{q}} + v_{\text{sd}} \tag{1}$$

$$v_q = R_{\text{stat}} i_q + L_{\text{stat}} \frac{\text{d}iq}{\text{d}t} + \omega_e L_{\text{stat}} i_d + v_{sq} \tag{2}$$

In Eqs. (1) and (2), (v_d, v_q) are the STATCOM output voltages, (i_d, i_q) are the STATCOM output current, (v_{sd}, v_{sq}) are the transmission line voltages.

The power losses in the system have been neglected for easies simplification. Therefore, the instantaneous power balance between the AC and DC sides is written in Eq. (3).

$$P_{\text{dc}} = P_{\text{ac}} \tag{3}$$

$$v_{\text{dc}} i_{\text{dc}} = v_a i_a + v_b i_b + v_c i_c \tag{4}$$

$$C_{\text{stat}} v_{\text{dc}} \frac{\text{d}v_{\text{dc}}}{\text{d}t} = \frac{3}{2}(v_{sd} i_d + v_{sq} i_q) \tag{5}$$

where, v_{dc} stands for the DC link voltage and i_{dc} stands for DC link current in the system.

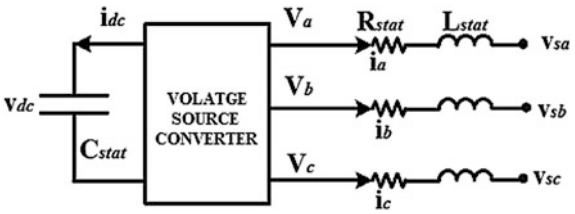


Fig. 2 STATCOM equivalent model

Thus Eq. (5) can be written as:

$$\frac{dv_{dc}}{dt} = \frac{3}{2}\frac{v_{sd} i_d}{C_{stat} v_{dc}} \tag{6}$$

According to Eq. (6) the d component of the STATCOM current (i_d) has been controlled by maintaining the DC bus voltage constant.

The reactive power generated by the STATCOM has been calculated using Eq. (7).

$$Q_{stat} = \frac{3}{2} v_{sd} i_q \tag{7}$$

Considering Eqs. (1) and (2), the d-q components of STATCOM current has been cross-coupled, $\omega_e L_{stat} i_q$ in V_d and $\omega_e L_{stat} i_d$ in V_d in the control law used. The two PI controllers have been used for the implementation of the voltage control schemes. Equations (1) and (2), gives the current control loop dynamics as: (Fig. 3).

$$G(s) = \frac{i_d(s)}{v'_d}\frac{i_q(s)}{v'_q} = \frac{1}{R_{stat} + L_{stat}} \tag{8}$$

where,

$$v'_d = i_d R_{stat} + L_{stat}\frac{di_d}{dt} \tag{9}$$

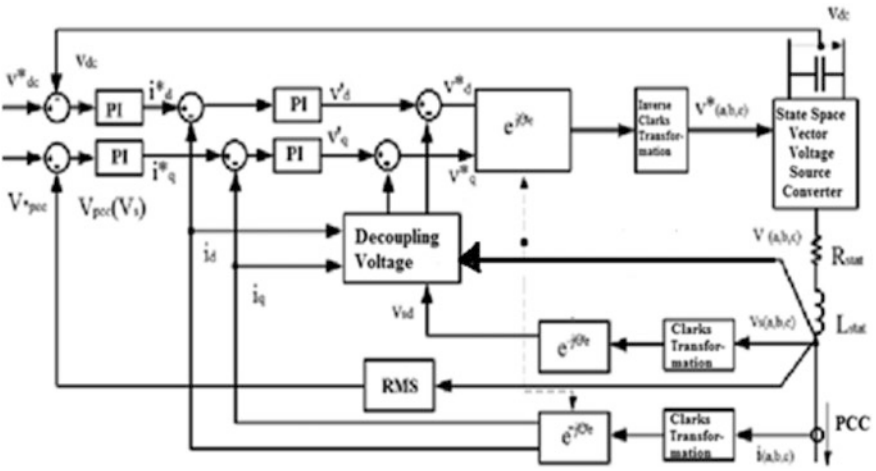


Fig. 3 STATCOM control block diagram

$$v'_q = i_q R_{\text{stat}} + L_{\text{stat}} \frac{\mathrm{d}i_q}{\mathrm{d}t} \tag{10}$$

$$v^*_d = v'_d - \omega_e L_{\text{stat}} i_q + v_{sd} \tag{11}$$

$$v^*_q = v'_q + \omega_e L_{\text{stat}} i_d \tag{12}$$

There are two loops present in the STATCOM control block diagram, i.e., voltage control loop and current control loop. Comparison between two voltages i.e. DC link voltage and voltage at the point of common coupling (V_{dc} and V_{pcc}) has been done with their respective reference voltages (V_{ref} and V_{pccref}) to get an error signal. The error signals obtained from comparing the two voltages was further allowed to pass through another PI controllers so that it can generate the reference current signals for d-q axis. The current and voltage components has been transformed from three phase to d-q reference frame using Clarks Transformation. In order to get error signals, at steady state the reference current (i_{aref}, i_{bref}, i_{cref}) has been compared with the actual currents (i_a,i_b,i_c) in the controller block. The error signals obtained (voltage error and current error signals) has been used to generate the control signal in order to drive the PWM converters. In this paper SVPWM technique has been used to generate pulses.

4 State Space Vector PWM

The circuit diagram of the three-phase voltage source PWM converter has been shown in Fig. 4

The switches S1–S6 are the six power switches which has been controlled by the switching variables a, a′, b, b′ and c, c′. When the upper switches are turned on, i.e., when a, b or c are 1, then the respective lower switches are turned off, i.e., a′, b′ or c′ are 0. Therefore, the off and on states of the upper switches S1, S3 and S5 are used to determine the output voltages [6].

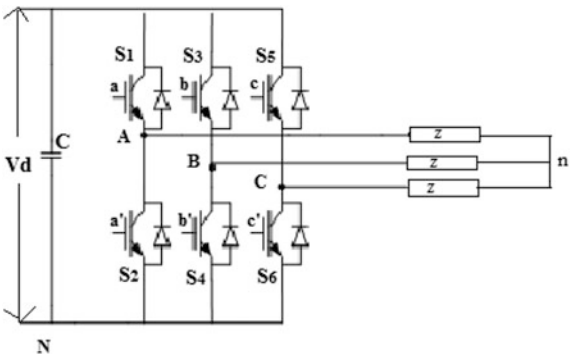


Fig. 4 Three-phase voltage source PWM converter

Thus, total eight possible switching vectors of on and off patterns for the upper three switches can be achieved as shown in the Fig. 5. The on and off states of the lower switches are opposite to the upper switches.

The phase-to-neutral voltages of a star-connected load have been defined by the voltage difference between the star point n of the load and the negative rail of the dc bus N. Thus the eight possible combinations denoted as switching vectors (V_0 to V_7) has been explained using the following equations:

$$v_A = v_{nN} + v_a \tag{13}$$

$$v_B = v_{nN} + v_b \tag{14}$$

$$v_C = v_{nN} + v_c \tag{15}$$

The phase voltage shown in the star-connected load is equal to zero. Therefore, the average of the above three equation will be:

$$v_{nN} = \frac{1}{3}(v_A + v_B + v_C) \tag{16}$$

On substituting the Eq. (16) in Eqs. (13)–(15) respectively, the phase-to-neutral voltages are given as:

$$v_a = \frac{2}{3}v_a - \frac{1}{3}(v_B + v_C) \tag{17}$$

$$v_b = \frac{2}{3}v_b - \frac{1}{3}(v_A + v_C) \tag{18}$$

$$v_c = \frac{2}{3}v_c - \frac{1}{3}(v_B + v_A) \tag{19}$$

The switching time and corresponding switching state of each power switch has been calculated according to the Fig. 6.

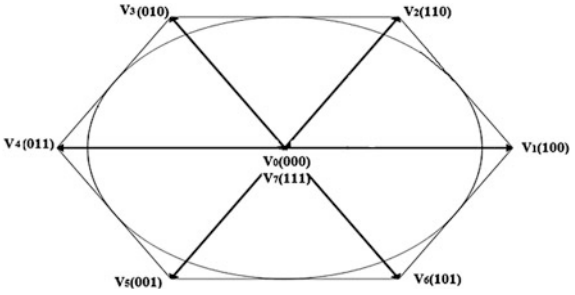


Fig. 5 Eight possible vector states

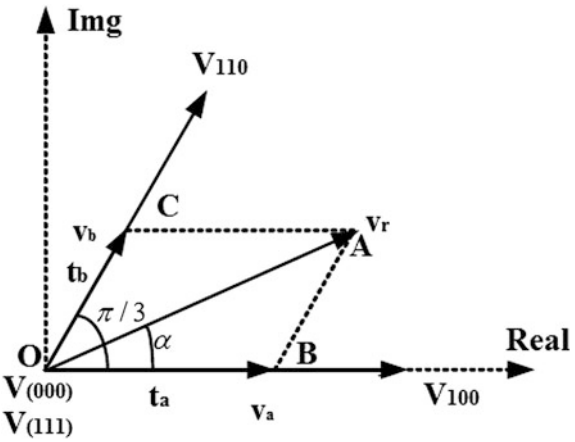


Fig. 6 Space vector time calculation

According to the sine rule in triangle OAB we get:

$$v_a = v_r - \frac{(\sin\frac{\pi}{3} - \alpha)}{\sin\frac{2\pi}{3}} \tag{20}$$

Similarly, in triangle OCA we get:

$$v_b = v_r - \frac{(\sin\alpha)}{\sin\frac{2\pi}{3}} \tag{21}$$

In other words,v_r has been obtained by the time averaging the voltage vectors of sectors. Thus,

$$v_r = V_{100}\frac{t_a}{T_0} + V_{110}\frac{t_b}{T_0} + V_{000}\frac{t_0}{T_0}, \tag{22}$$

where T_0 is the complete time period when switch S_1 is on to off and t_0 is the time given to zero vector.

$$T_0 = t_a + t_b + t_c \tag{23}$$

Therefore,

$$t_a = \frac{v_a}{V_{100}} T_0 \tag{24}$$

On substituting the value of the v_a in Eq. (24) we get

$$t_a = \frac{v_r}{V_{100}} \frac{(\sin\frac{\pi}{3} - \alpha)}{\sin\frac{2\pi}{3}} \tag{25}$$

Similarly,

$$t_b = \frac{v_b}{V_{100}} T_0 \tag{26}$$

On substituting the value of the v_b in Eq. 26 we get

$$t_b = \frac{v_r}{V_{100}} \frac{(\sin\alpha)}{\sin\frac{2\pi}{3}} T_0 \tag{27}$$

The main advantage of SVPWM is that it gives higher switching frequency which is not possible by Sinusoidal PWM technique and also there is degree of freedom of space vector placement in the switching cycle. Because of this the harmonic performance of SVPWM get improved [4].

The two phase reference voltages v_d, v_q obtained from the STATCOM model has been transformed from Cartesian to polar. Later a ramp time signal has been generated by using the repeating sequence block taken from the sub-library. Further the signal has been fed to the Embedded MATLAB Function where the time period for each sector has been calculated using the above equations. The MATLAB codes have been used for the generation of the switching pattern. The calculation of the angle is done to identify the sectors in the MATLAB code. The ramp time signal generated in the MATLAB codes has further been compared with the ramp timer signal. The switching calculated has been further fed to the converter block [3].

5 Results and Discussion

In this paper, initially the test system without the STATCOM has been observed under various load conditions. Later the same three-phase test system with STATCOM has been examined under the respective load conditions.

Figure 7 shows the voltage response of the stepped up transformer connected to bus no. 3 to the test system in absence of the STATCOM. The voltage received at bus no. 3 is 33 kV.

Initially a load of 1 MW at 0.8 pf lagging (reactive load) was connected to the test system. At 0.6 s the second load, i.e., 4.25 MW at 0.8 pf lagging has been introduced at receiving end side. The graphs shows that without any compensating device there was a voltage drop at 0.6 s due to sudden change in load which is shown in Fig. 8. Due to the voltage dip the stability of the entire AC system gets disturbed which is not desirable.

In order to overcome the voltage dip shunt FACTS device named STATCOM has been introduced to the system. When the STATCOM controller detects the voltage mismatch between the reference values (V_{ref}) and the point of common coupling (V_{pccref}) value of voltage, it will start injecting reactive power at the point

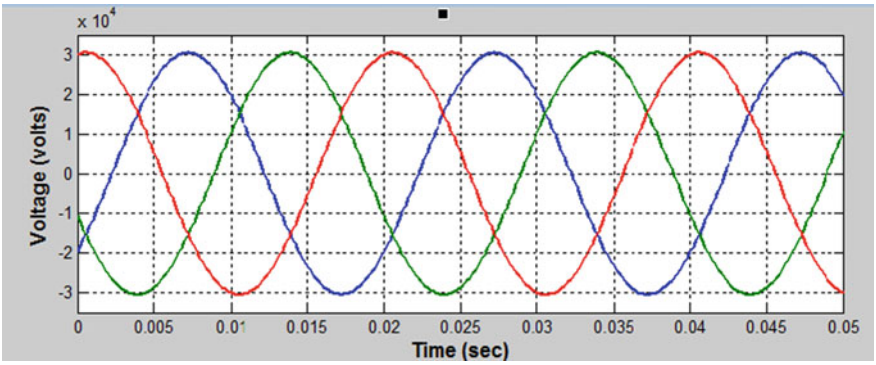


Fig. 7 Transmission line voltage at bus no. 3 without STATCOM

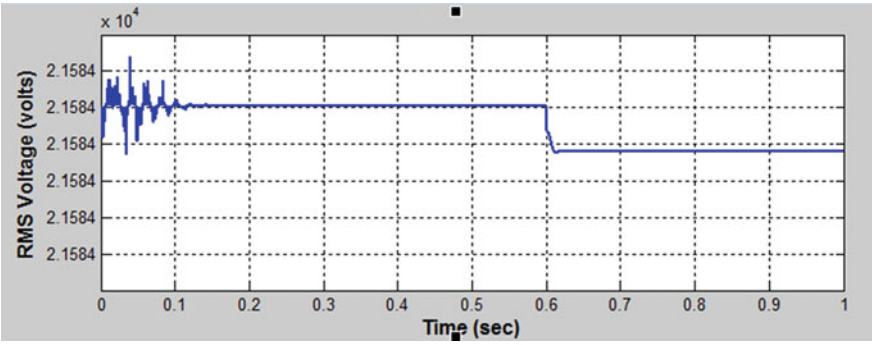


Fig. 8 RMS voltage of the transmission line system at bus no. 3 without the STATCOM

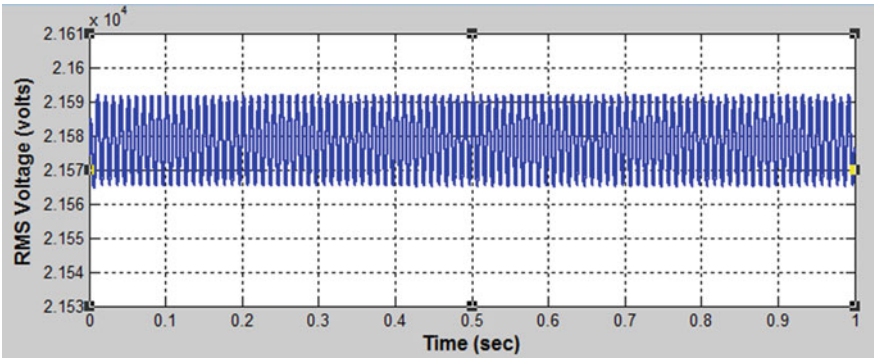


Fig. 9 RMS voltage of the transmission line system at bus no. 3 with STATCOM

of voltage dip to the system so that the voltage level come back nominal value. Therefore in the presence of SVPWM-based STATCOM, it has been observed in Fig. 9 that the voltage diphas been recovered successfully.

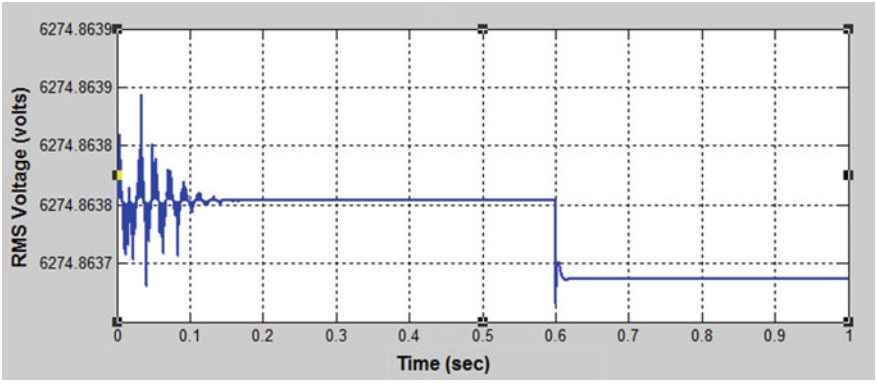


Fig. 10 RMS voltage of the transmission line at bus no. 4 without the STATCOM

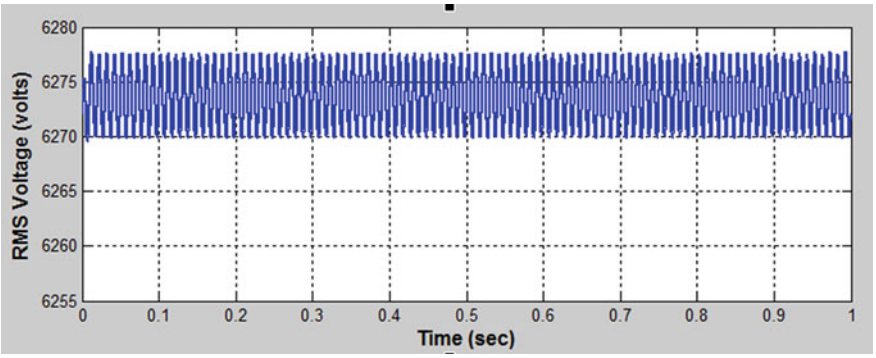


Fig. 11 RMS voltage of the transmission line at bus no. 4 with the STATCOM

Figure 10 shows voltage profile at bus no: 4 of the receiving end side of the three-phase transmission line without STATCOM. There is a voltage dip at 0.6 s due to change in load in the system.

Here it is observed that after connecting STATCOM to the three-phase transmission line the voltage at bus no: 4 have been recovered as shown in Fig. 11.

6 Conclusion

In this paper, State Space Vector PWM (SVPWM) based STATCOM model has been implemented. In the proposed work, the simulation results of the three-phase test system without the STATCOM have been compared with the three-phase test system with the STATCOM. The three-phase test system model without STATCOM showed a significant voltage dip when sudden load change occurs in

the system. The purpose of using STATCOM is that it will inject reactive power to the transmission system in order to reduce the voltage saturation occurring in the power system due to change in loads. Thus it helps to increase the voltage stability of the power system by improving the voltage of AC transmission line. From the above results shown it is clear that the STATCOM successfully improves the voltage dip in the power system.

References

1. Hossain, A.R.K.: Design of STATCOM for power system stability improvement. Global J. Res. Eng. **14**(2) (2014)
2. Xu, Y., Li, F.: Adaptive PI control of STATCOM for voltage regulation. IEEE Trans. Power Deliv. **29**(3), 1002–1011 (2014)
3. Iqbal, A., Lamine, A., Ashraf, I.: MATLAB/SIMULINK model of space vector PWM for three-phase voltage source inverter. In: Proceedings of the 41st International Universities Power Engineering Conference, vol. 3, pp. 1096–1100, IEEE September 2006
4. Fadaeinedjad, R., Moschopoulos, G., Moallem, M.: Using STATCOM to mitigate voltage fluctuations due to aerodynamic aspects of wind turbines. In: IEEE Power Electronics Specialists Conference, 2008, pp. 3648–3654, IEEE June 2008
5. Roy, C., Sengupta, A.: Implementation of STATCOM to overcome disturbances in grid connected wind farm. In: International Conference on, Energy, Power and Environment: Towards Sustainable Growth (ICEPE), 2015, pp. 1–4, IEEE June 2015
6. Ajitha, A., Mutharasan, A., Dhal, P.K.: Power quality improvement using unified power flow controller in matrix converters for WECS. Int. J. Appl. Eng. Res. **10**(76) (2015) ISSN: 0973-4562
7. Hingorani, N.G., Gyugyi, L.: Understanding FACTS: concepts and technology of flexible AC transmission systems. Wiley-IEEE press (2000)

Common-Mode Voltage Regulation of Three-Phase SVPWM-Based three-Level NPC Inverter

Subramaniam Umashankar, Vishnu Kalaiselvan Arun Shankar, Padmanaban Sanjeevikumar and K. Harini

Abstract This paper presents the implementation of the modulation strategy to balance the neutral point potential (NPP) in three-level NPC inverters. This method employs the space vector pulse width modulation technique which gives the strong regulating ability of common-mode voltage of DC link capacitors. Apart from balancing the dc bus voltage this paper also examines the switching losses and junction temperature associated with the three-level inverters. The comparison of three-level inverter with two-level inverter, on the basis of switching losses, has also been explored. The performance of the modulation strategy to balance NPP has been validated and verified using MATLAB/Simulink.

Keywords Three-level neutral point clamped (NPC) inverters · Space vector modulation (SVM) · Neutral point voltage balancing

1 Introduction

Mostly, the multilevel inverter has been found more applications in industries for producing high voltage and power for power quality compensators, marine drives, renewable energy system, etc. with better quality of output. The reason behind the

S. Umashankar (✉) · V.K. Arun Shankar · K. Harini
Department of Energy and Power Electronics, Vellore Institute of Technology (VIT) University, Vellore, Tamil Nadu, India
e-mail: umashankar.s@vit.ac.in

V.K. Arun Shankar
e-mail: arunshankarvk@gmail.com

K. Harini
e-mail: harini.2733@gmail.com

P. Sanjeevikumar
Department of Electrical and Electronics Engineering, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_37

tremendous increasing popularity of MLI is the better output voltage [1]. Due to the unbalanced DC link voltage the neutral point potential (NPP) deviates from its zero reference value and simultaneously introduces harmonic distortion in the output voltage [2, 3].

Several methods of capacitor voltage balancing which have been implemented earlier are as follows:

By addition of extra hardware components [4–9] with the inverter which includes inductance, capacitance, and power semiconductor components to control the potential at neutral point of DC bus, common-mode voltage control technique using sinusoidal pulse width modulation (SPWM) is used [10, 11].

In the technique mentioned above the current flowing through the two capacitors generates a disturbing current which unbalances the voltage across the dc link capacitors and the correction current flowing through the proposed circuit which balances the capacitor voltages. But the inclusion of the low VA transformer in it adds to the cost and complexity of the overall circuit. Among the other method, the dc common-mode voltage (DC-CMV) method is the most conventionally used technique [12]. But this method is unsuitable at the pure reactive power and also depends on the output current.

Another method which is suitable for pure reactive power and further reduces switching losses is proposed [13]. In minimum gate-on time injection method the two methodologies are combined namely conventional SVM and three-vector modulation. The shortcoming of this method is poor balancing ability at low power factor and high MIs.

Further another methods that can control the dc link voltage are as follows:

- Modifying the magnitude of CMV corresponding to unbalance parameters at neutral point is dynamic CMV method [14]. But the complexity of this method is higher than the minimum gate—on time injection method. On the other hand it is also not feasible for high MIs and low PFs.
- Overpowering the disadvantages of the fore-mentioned methods, the sixth harmonic CMV injection method is proposed. The demerits of this technique are its complexity and the poor balancing ability at low PFs [15, 16].

These days space vector modulation technique (SVM) is widely used due to its several advantages. It offers flexibility in optimization of switching waveform and is simple to implement in digital controllers [17].

2 Description of Inverter

Figure 1 illustrates the circuit diagram of three-level NPC inverter. In the operation of three-level inverter, there exist three switching states: [P], [O], and [N]. The turning ON of the middle two switches signifies the [O] switching state.

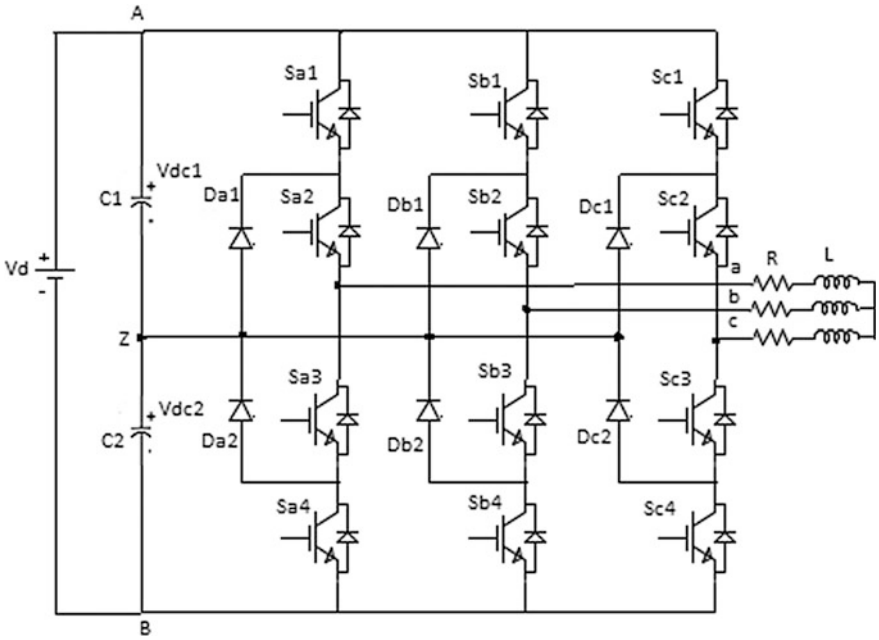


Fig. 1 Structure of DCMLI

The neutral voltage gets affected because of the nonuniform charge distribution across capacitor due to which NPP gets deviated from the reference value. To reduce the effect of neutral point deviation, space vector modulation technique is introduced.

As previously mentioned, consider the three switching states of each phase leg as [P], [O], and [N]. Therefore, totally 27 switching states are possible. Figure 2 shows switching states and relative space voltage vectors. The magnitudes and the switching states of the different voltages are represented in Table 1.

3 Modulation Strategy and Loss Calculations

3.1 Loss Calculation

Losses of the inverter significantly influence by temperature generation across switches, in particular across the junction of the switches. Thermal network and electrical network are analogous to each other, where heat dissipation analogous to current. So the temperature loss = [Heat dissipation × Thermal resistance], so the junction temperature also affects switching losses.

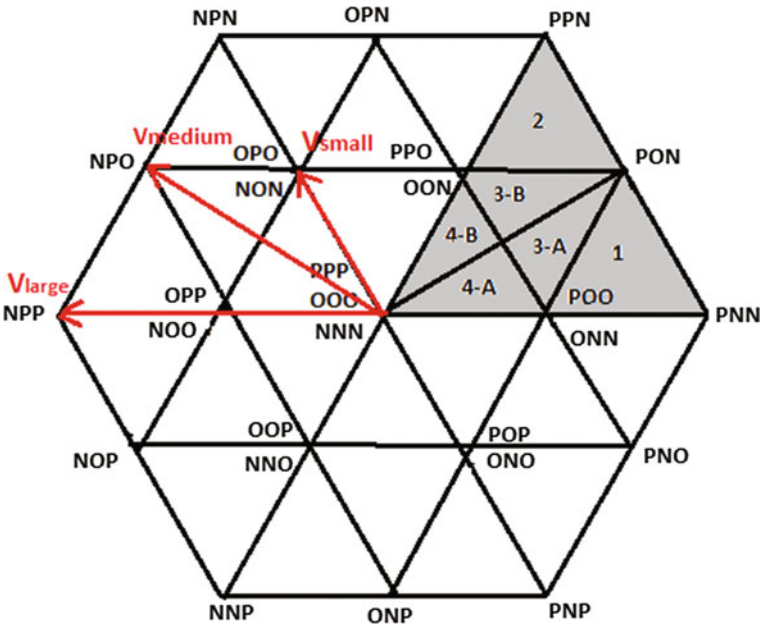


Fig. 2 Three-level inverter space vector diagram

Table 1 Switching state and voltage vector

Vector	Magnitude	Switching state	
Zero vector	0	[PPP] [OOO] [NNN]	
Small vector	$\frac{1}{3}$Vd	P-type	N-type
		[POO]	[ONN]
		[PPO]	[OON]
		[OPO]	[NON]
		[OPP]	[NOO]
		[POP]	[ONO]
		[OOP]	[NNO]
Medium vector	$\frac{\sqrt{3}}{3}$Vd	[PON]	
		[OPN]	
		[NPO]	
		[NOP]	
		[ONP]	
		[PNO]	
Large vector	$\frac{2}{3}$Vd	[PNN]	
		[PPN]	
		[NPN]	
		[NPP]	
		[NNP]	
		[PNP]	

3.2 Implementation of Modulation Strategy

The neutral point potential is majorly affected by switching states. Medium vectors do consist of O-state, but their effect on the neutral point potential depends upon the direction of the current. Small vectors are of two types P-type (consist of P-state and O-state) and N-type (consist of N-state and O-state). P-type small vector increases the neutral point potential and N-type small vector decreases the neutral point potential. From above discussion, it is clear that small vectors play vital role in variation of neutral point potential. The proposed method does exactly the same. In proposed method, small vectors are replaced by zero vectors. As mentioned above, N-type small vectors decrease the neutral point potential, and in particular, it makes Vdc2 lesser than Vdc1.

While designing switching states, each change of switching state includes only one switching from any of the phases. That means each seven-segment switching sequence consists of six switching transitions, so that switching losses are reduced.

Figure 3 shows the proposed methodology block diagram. The complexity of the dwell time calculation is reduced by new modulation strategy which is presented. In this, offset time is added with the gate turn on times of the NPC inverter. The controlled output voltage of PI controller is fed to the dq–abc transformation

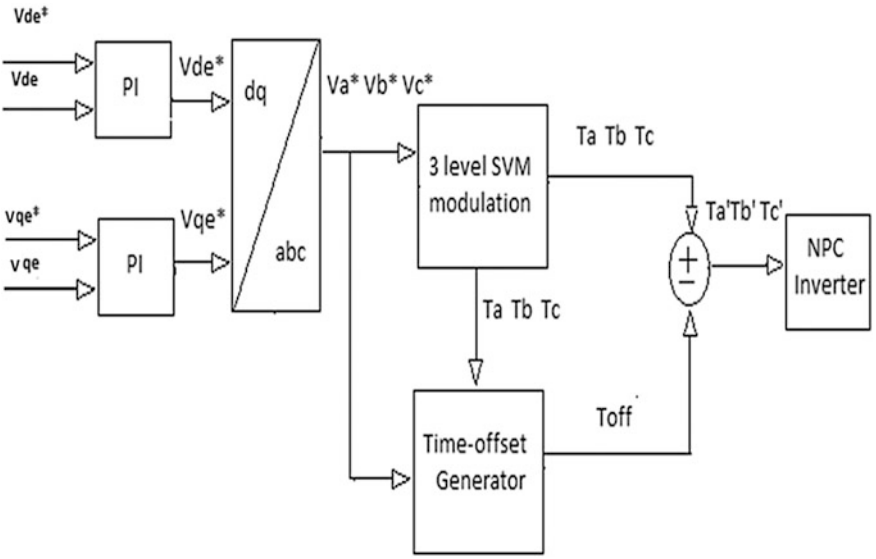


Fig. 3 Proposed method block diagram

block at the output of this block and three-phase reference voltage is obtained. This reference voltage is fed to three-level space vector modulator and time offset generator. At the output of these, dwell timing and offset time are generated which are added and given to the NPC inverter.

4 Simulation Results

Figures 4 and 5 show the loss calculation results of three-and two-level NPC inverter. From this it is clear that the temperature generation at the junctions is more as compared to that of three-level NPC. So the losses due to the junction temperature according to the formula stated in section (A) are more in two-level inverter as compared to three-level NPC.

Figures 6 and 7 show the output phase voltage waveforms and output current waveforms. From Fig. 6 it can be seen that there are distortions in the voltage output when proposed modulation strategy is not applied to the inverter gating control system. Figure 7 shows the output of the inverter after proposed modulation strategy is implemented. Figures 8 and 9 show the difference in current waveforms with and without proposed modulation strategy.

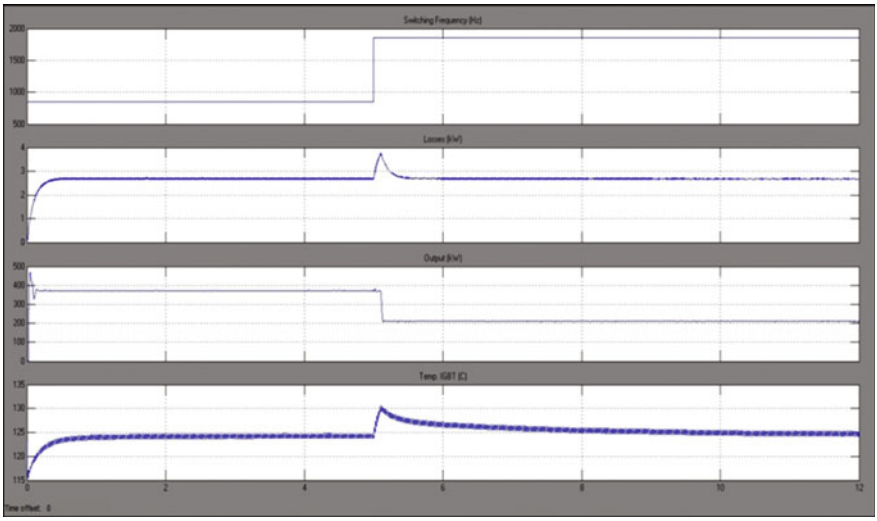


Fig. 4 Three-level NPC

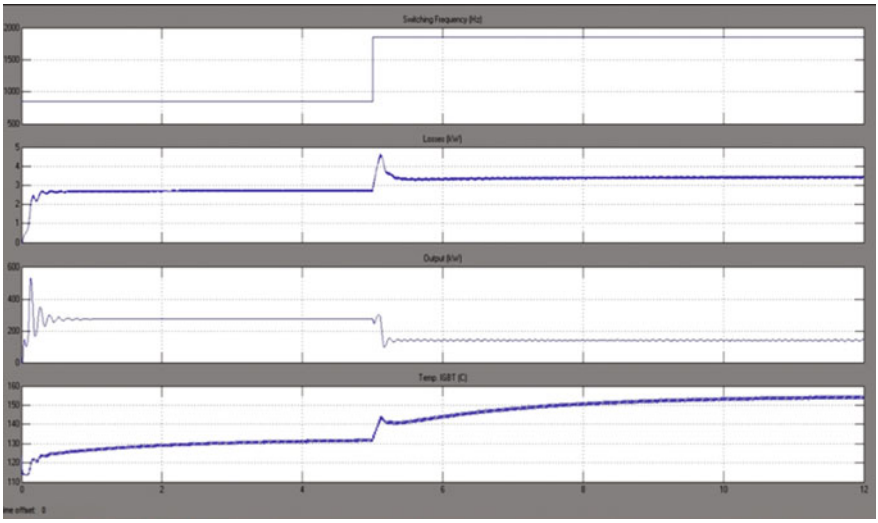


Fig. 5 Two-level NPC

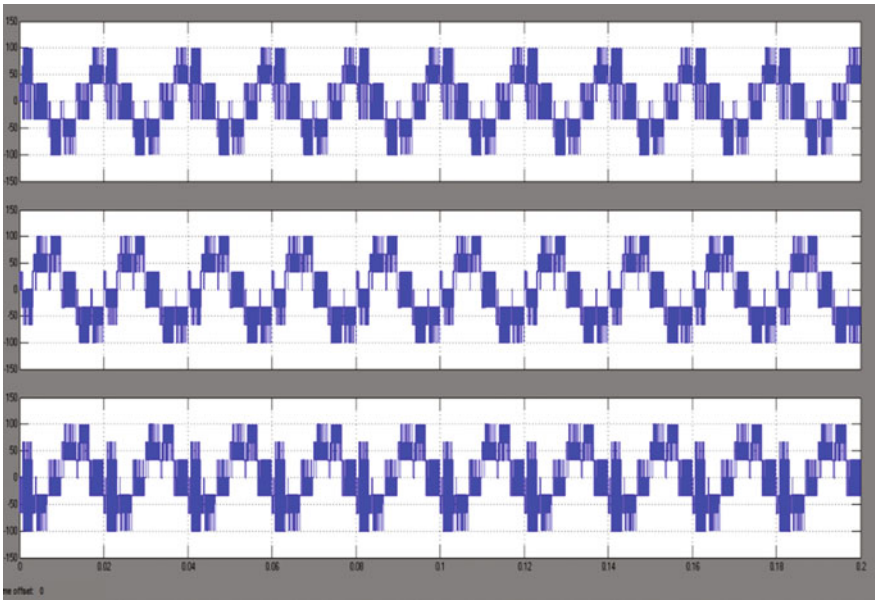


Fig. 6 Output phase voltages without using proposed modulation strategy

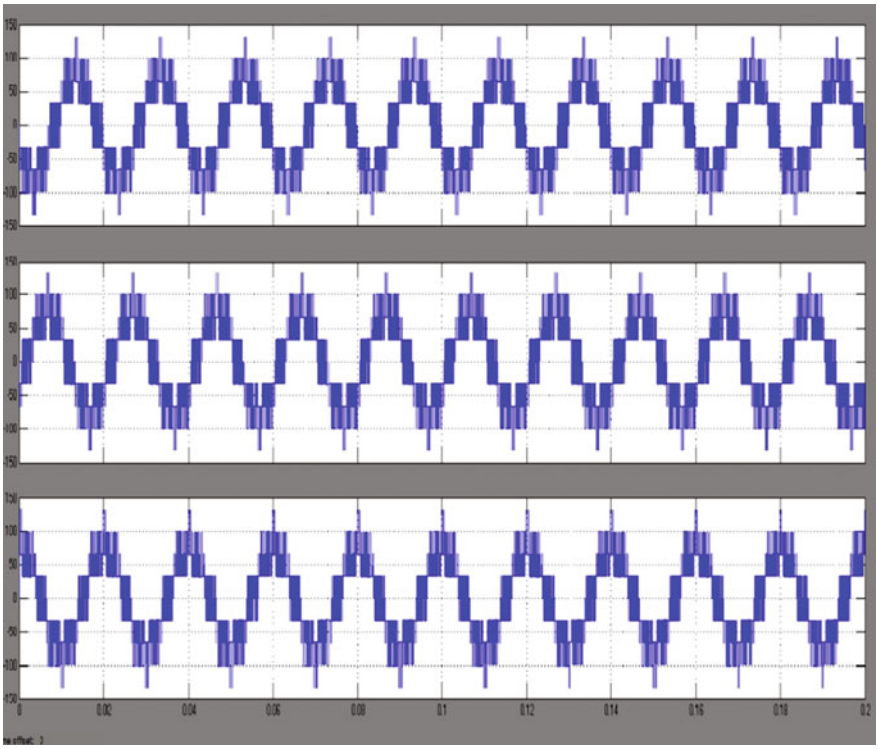


Fig. 7 Simulated results of output phase voltages with proposed strategy

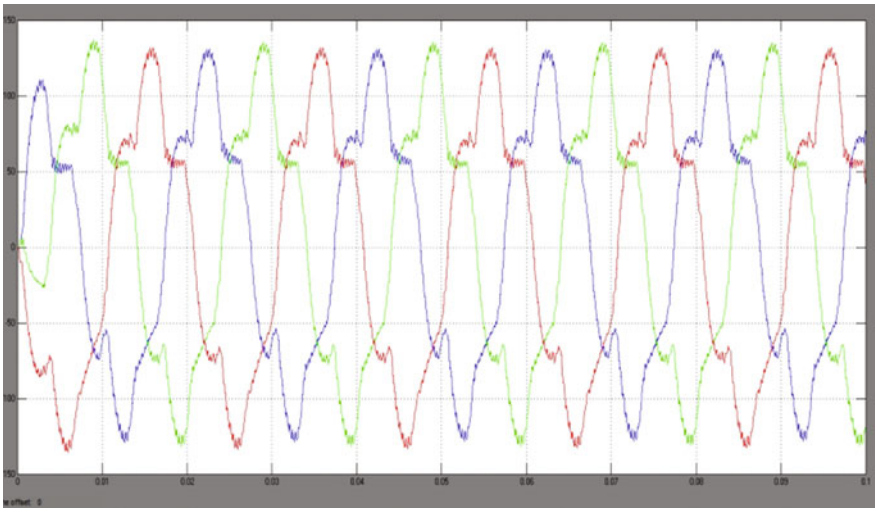


Fig. 8 Simulated results of output current with proposed strategy

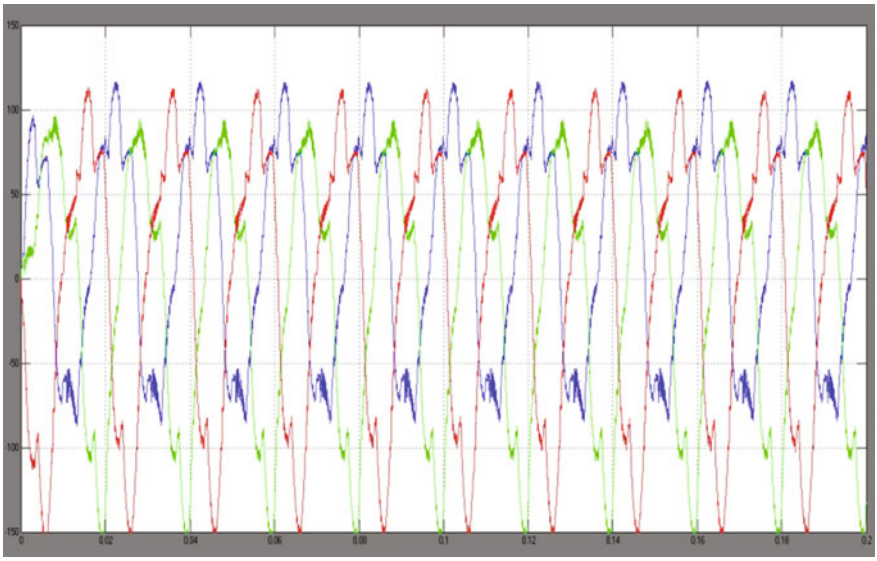


Fig. 9 Simulated results of output current without using proposed modulation strategy

5 Conclusion

This paper presents SVM-based technique for the neutral potential. In this technique vectors do not affect the neutral point potential. Conventional seven-level switching is considered, which offers lesser harmonic, also switching sequence so chosen that only one switch of any of the leg experience the transition in its state. This will also reduce the switching losses. Moreover, this paper also compared the switching losses and the losses due to the junction temperature of the NPC (two and three level) inverter.

References

1. Wu, B.: High-Power Converters and Ac Drives. Wiley, Hoboken, NJ, USA (2006)
2. Rodríguez, J., Bernet, S., Wu, B., Pontt, J.O., Kouro, S.: Multilevel voltage source converter topologies for industrial medium voltage drives. IEEE Trans. Ind. Electron. **54**(6), 2830–2945 (2007)
3. Rodríguez, J.R., Lai, J.S., Peng, F.Z.: Multilevel inverters: a survey of topologies, controls, and applications. IEEE Trans. Ind. Electron. **49**(4), 724–738 (2002)
4. Sakasegawa, E., Shinohara, K.: Compensation for neutral point potential in three-level inverter by using motor currents. Trans. Inst. Elect. Eng. **121**(8), 855–861 (2001)
5. Song, Q., Liu, W., Yu, Q., Xie, X., Wang, Z.: A neutral point potential balancing algorithm for three-level NPC inverters using analytically injected zero sequence voltage. Proc. IEEE APEC **1**, 228–233 (2003)

6. Bendre, A., Venkataramanan, G., Srinivasan, V., Rosene, D.: Modeling and design of a neutral point voltage regulator for a three level diode clamped inverter using multiple carrier modulation. IEEE Trans. Ind. Electron. **53**(3), 718–726 (2006)
7. Bento, A.A.M., de Almeida, K.V.D., Oliveira, A.R.M., da Silva, E.R.C., Jacobina, C.B.: A high power factor three-phase three-level rectifier. Proc. IEEE PESC 3040–3045 (2007)
8. Bhuvaneswari, G., Nagaraju, : Multi-level inverter—a comparative study. IETE J. Res **51**(2), 141–153 (2005)
9. Yazdani, A., Iravani, R.: A generalized state space averaged model of the three-level NPC converter for systematic DC voltage balancer and current controller design. IEEE Trans. Power Del. **20**(2), 1105–1114 (2005)
10. Newton, C., Summer, M.: Neutral point control for multilevel inverters: Theory, design and operational limitations. In: Conference Record IEEE IAS Annu. Meeting, New Orleans, LA, USA, pp. 1336–1343 (1997)
11. Newton, C., Summer, M., Alexander, T.: Multilevel converters: a real solution to high voltage drives. IEEE Colloq. Update New Power Electron. Tech 1–5 (1997)
12. Chaturvedi, P., Jain, S., Agarwal, P.: Carrier-based neutral point potential regulator with reduced switching losses for three-level diode-clamped inverter. IEEE Trans. Ind. Electron. **61**(2), 613–624 (2014)
13. Choi, U.M., Lee, K.B.: Space vector modulation strategy for neutral point voltage balancing in three-level inverter systems. IET Power Electron. **6**(7), 1390–1398 (2013)
14. Shen, J., Schroder, S., Duro, B., Roesner, R.: A neutral-point balancing controller for a three-level inverter with full power-factor range and low distortion. IEEE Trans. Ind. Appl. **49**(1), 138–148 (2013)
15. Akagi, H., Hatada, T.: Voltage balancing control for a three-level diode clamped converter in a medium-voltage transformerless hybrid active filter. IEEE Trans. Power Electron. **24**(3), 571–579 (2009)
16. Tallam, R.M., Naik, R., Nondahl, T.A.: A Carrier-based PWM Scheme for neutral-point voltage balancing in three-level inverters. IEEE Trans. Ind. Appl. **41**(6), 1734–1743 (2005)
17. Mekhilef, S., Abdul Kadir, M.N.: Voltage control of three-stage hybrid multilevel inverter using vector transformation. Power Electron. IEEE Trans. **25**, 2599–2606 (2010)

Survey of Power Quality Discrete Disturbances in an Educational Institution

Subramaniam Umashankar, Vishnu Kalaiselvan Arun Shankar, Shanmugam Paramasivam, Padmanaban Sanjeevikumar and K. Anil Kumar

Abstract There are number of studies based on power quality events, but very few literatures are focused only on the discrete disturbances which also known as events of power quality disturbances. To answer several questions about the discrete disturbances, the power quality survey was conducted at VIT University, India. This survey intended to lay out information related to power quality disturbances mainly focused on swells, dips, transients, rapid voltage changes, voltage interruptions, and other parameters. The result from the survey will give a better knowledge and understanding about the above parameters.

Keywords Nonlinear loads · Discrete disturbances · Swells · Dips

S. Umashankar (✉) · V.K. Arun Shankar · K. Anil Kumar
Department of Energy and Power Electronics, Vellore Institute of Technology (VIT) University, Vellore, Tamil Nadu, India
e-mail: umashankar.s@vit.ac.in

V.K. Arun Shankar
e-mail: arunshankarvk@gmail.com

K. Anil Kumar
e-mail: anilkumar.kanneli@gmail.com

S. Paramasivam
Danfoss Industries Private Limited, Chennai, Tamil Nadu, India
e-mail: paramsathya@yahoo.com

P. Sanjeevikumar
Department of Electrical and Electronics Engineering, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_38

1 Introduction

Power quality survey is the recording and analysis of the exact power supply available to the customers [1, 2]. It provides details of the power, voltage, current, and other parameters which help maintain a standard power supply quality. Power quality disturbances are important aspects of power quality which is mainly classified into main categories, continuous or variation type and discrete or event type [3]. Continuous type is present in a repeated manner in every cycle, comprising the voltage level, unbalance, flicker, and harmonics [4]. The discrete disturbance, as suggested by the term, is independent and isolated events, which can be recorded as entries mentioning the date and time for each event. Discrete disturbances mainly involve voltage sags, swells, oscillatory, and impulsive transients.

This work aims at reviewing the existing characterizations, their patterns, and limitations. This will be followed by a study for developing a single-site index for each discrete disturbance-type event recorded at varied 415 V sites in VIT University's main building substation with different types of load feeders at utility primary side of their facilities. Characterization of discrete disturbances in power quality will help improve power quality survey conducted in the university during these project results of power quality survey.

2 Details of VIT Power System and the Survey

The main receiving transformer 33/11 kV is connected with three different transformers where the utility supply stepped down to 11 kV in the academic side of the university. These three 11 kV transformers are connected and distributed to the different places in the campus stepping down the voltage to 415 V at 16 different buildings. In this paper we are going to talk about only one of three transformers, which will be called as main build power house's transformer during the survey which include two hostel buildings, four academics buildings library, and other buildings with different types of loads.

As we have mentioned earlier, this power quality survey is monitoring and collecting different load feeder's raw measurement data, which will be collected by connecting PQ-Box 200, what is also known as the Network Analyzer PQ-Box 200 [5]. This instrument has been connected to different feeders approximately for 24 h to record the data. PQ-Box 200 also meets all the measurement standards as required.

3 Objective

The objective of this study is

- to inspect the discrete disturbances as per standards;
- to study and understand the power quality at various load feeders at the institute; and
- to have proper explanations for the particular disturbances.

4 Observations

While describing about the power system of VIT University, we have mentioned, we will be talking about only one transformer (main building power house), which is feeding 16 different builds. Most of the buildings have two types of feeder like lighting feeder and power-UPS feeder, and few building has three feeders, where the ACs are connected separately like AC feeder, lighting feeder, and power-UPS feeder. The lighting feeders feed the lighting loads of all the buildings where we have a different AC feeder to feed the AC loads. Otherwise for most of the buildings, ACs are fed by power-UPS feeder including the big loads like lifts, machines, and fans. A detail load structure has been given in Table 1. From the 24 h recorded data from different sites, we focused on the following events.

5 Details About PQ Events

A. Frequency deviations

Normally, the value of the frequency in India is 50 Hz. It is a fact that supply system's frequency is depended on the actions of generators and loads. The

Table 1 Load type details

AC load	Lighting loads	Power load and UPS
Central AC	Fluorescent LAMP	Fans
Split AC	CFL	Motors
Window AC	Halogen lamps	Lifts
	LED light	Power plugs
	Exit light	Water cooler
		PC
		Projectors
		UPS

variation range is smaller and higher which is totally based on the ratio between the loads and the generation capacity [6].

In the event list, if any of 10 s frequency measurement overreaches the limits of the setup for narrow tolerance, it is noted as a frequency deviation (narrow tolerance). The narrow tolerance (normally 99.5%) is positive or negative limit if overreached, and the event is noted. Again in the event list, if any of 10 s frequency measurement overreaches the limits of the setup for narrow tolerance, it is noted as a frequency deviation (wide tolerance). The wide tolerance (normally 100%) is positive or negative limit if overreached, and the event is noted, and so for the 50 Hz frequency (see Table 2).

B. Dip and swell

A voltage dip is generated due to sudden reduction of voltage changes limit of a 10 ms voltage. In other words, if r.m.s value of voltage is reduced to 90%, then it is noted as dip. On the other hand, a voltage swell is generated due to sudden increase of voltage changes limit of a 10 ms voltage. If the r.m.s value of voltage is increased to 110%, then it is noted as swell. To understand and analyze the sag and swell events, we prefer to use EN50160 standards and as well as ITIC curves with respect to duration of supply voltage interruption. Using the EN50160 standards, the results (PQ events) are tabulated. Table's cells are alleging, as an aggregate of the after-effects from locations with numbers of dips and swells including classes of depth and durations. In each table, the duration of voltage dips is less than 1 min.

C. Rapid voltage changes

A fast dejection of the r.m.s value of voltage caused by specific load like motor switching on is known as a rapid voltage changes. Between two steady states, the 'Tolerance band' and in other hand 'Detection limit for RVC', a voltage change that occurs is known as rapid voltage change. The 'Tolerance band' is defined as the acceptable voltage range that is permissible to be considered as 'steady state'. The voltage must be within this range for at least 1 s. The threshold limit is triggered by the 'Detection limit for RVC' that must be exceeded between two sequential steady-state conditions for the event to be classified as a RCV event.

The typical settings for rapid voltage change are as follows:

- Tolerance band = 1%
- Detection limit for RVC (%) = 5% (Normal range is 5–10%, but less than Dip/Swell limits). It is taken into consideration that any voltage excursion passing the dip/swell threshold limits will be a dip/swell event and not a RVC event.

Table 2 Frequency deviations

Feeders	Maximum PQ events	Reasons
Lighting	Infraction harmonics	LED lights with power electronics drivers
Power and UPS	Rapid voltage change	UPS and VFDs
Lighting	Infraction harmonics	Fluorescent light, lift motor VFDs
Power and UPS	Infraction harmonics	Monitors, UPS and VFDs

D. Voltage interruptions

According to EN50160, supply voltage interruption is subdivided into two:

1. Short supply interruptions—the duration is less or equal to 3 min; and
2. Long supply interruptions—the duration is more than 3 min.

When 10 ms values should fall below 99% of 'nominal' voltage, a voltage interruption event is generated.

E. Infraction Long-Term Flicker

This event is generated if the Plt long-term exceeds the 95% limit threshold as defined in the setup (see Table 3).

G. Infraction Harmonics

This event is generated if the average of any one harmonic voltage exceeds the 95% limit for that harmonic, during each measuring interval. It is expected that for a single measuring interval, multiple events will occur as each harmonic is considered individually.

Among all the PQ events, only infraction harmonics use 10 s values, and it is therefore independent of the measuring interval.

If multiple events occur within a measuring interval, then they are captured.

If an event spans one or more measuring interval, it is still classed as a single event.

H. Recorded PQ events

(a) Site 1: Lighting Feeder

Before start discussing about the PQ events of this feeder, it is to be noted that this feeder fed load of 94.67% LED bulbs and 5.33% different lighting types such as halogen lights and TL type. Like other nonlinear loads, LEDs comply with the international standards as discussed earlier. In Table 4, frequency deviation is noted as 2; from Fig. 1 it is clear that both the frequency deviations happed due to power cuts or shutdown at 22:06:29 for three lines at the same time. Figure 2 indicates the same about frequency deviations. In Fig. 2 the voltage drops that is noted as swell and dips for the first 6 are due to same power cut at the same time and other swells and dips are due to the 98% LED lighting loads and they are connected to this feeder.

Figures 3 and 4 shows a clear idea about the rapid voltage changes in the voltage time curve for the power electronics LED loads and due to the functioning of switching devices of the LED driver. ITIC curve explains about various regions of the PQ events (Figs. 5 and 6).

Table 3 Infraction long-term flicker

Tolerance 95%	1.00
Tolerance 100%	5.00

Table 4 PQ events

PQ event	No of times
Frequency deviations	2
Swell	1435
Dip	135
Rapid voltage change	300
Voltage interruptions	9
Long time flicker	12
Infraction harmonics	1501

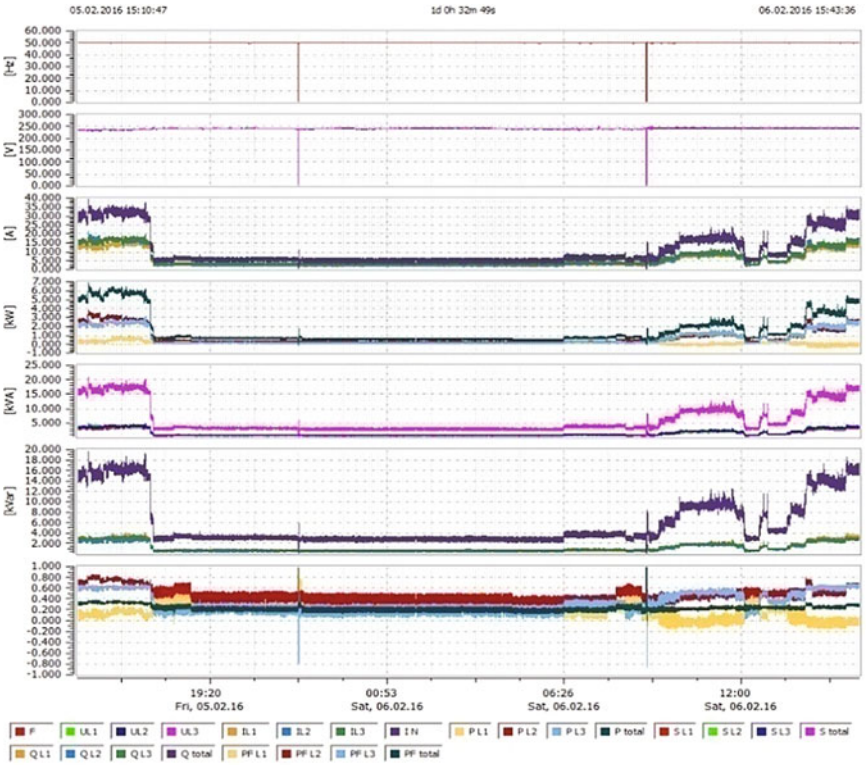


Fig. 1 Time plots for F, V, A, kW, kVA, kVar for lighting feeder

These LEDs are driven by a simple nonlinear direct current which in converted by rectifiers in the LED drivers. The equivalents used inside the LED drivers use simple performance input configuration which has high nonlinearities and capacitive loads, which create significant upper harmonics. This harmonic cause serious voltage distortions, rapid voltage changes, long time flickers, as well as infraction harmonics.

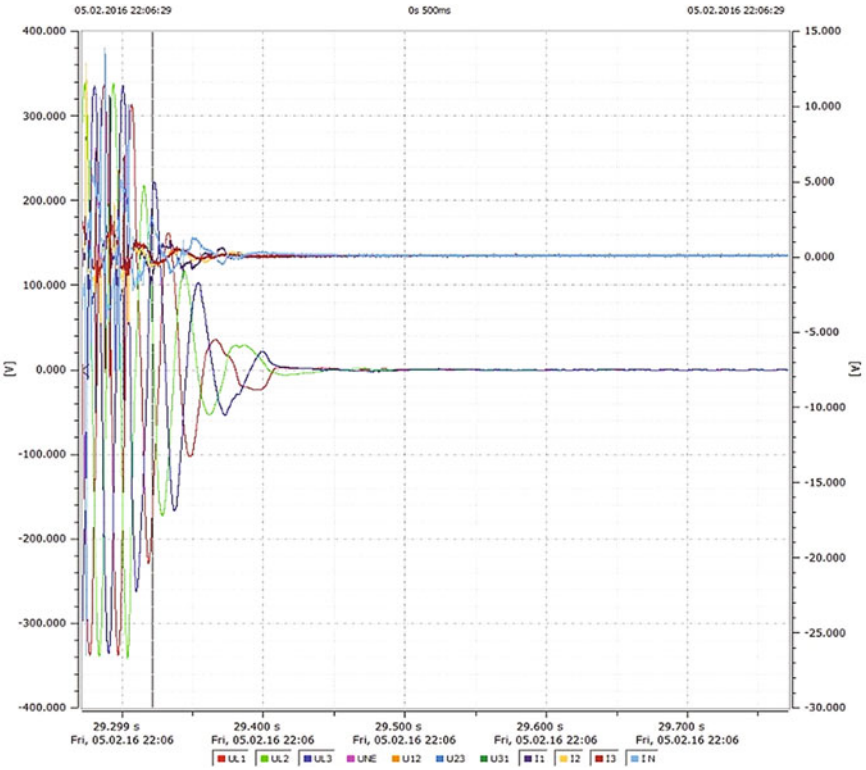


Fig. 2 Time plot for line voltages and currents

(b) AC-UPS Feeder

In the PQ events table, the dips are noted as 3. These dips have occurred due to short-circuit fault as shown in Fig. 7; it is clear that three line voltage waveforms dropped at different times as power shutdown is not possible. After few seconds, the voltage started increasing and crossed the limit for line 1 and line 2, which are noted as voltage swells. The voltage interruptions are noted down due to the same reason; there were three voltage drops which are also noted as the dips. Harmonics are created due to the control of induction motors.

Figure 7 explains the voltage dips noted in Table 5. Voltage for line 3 did not cross the voltage limit. So there are only two voltage swells as shown in Fig. 8; Fig. 9 shows the difference between the line 1, line 2, and line 3 voltage changing differences at the same time, which is also noted as a rapid voltage change in the PQ

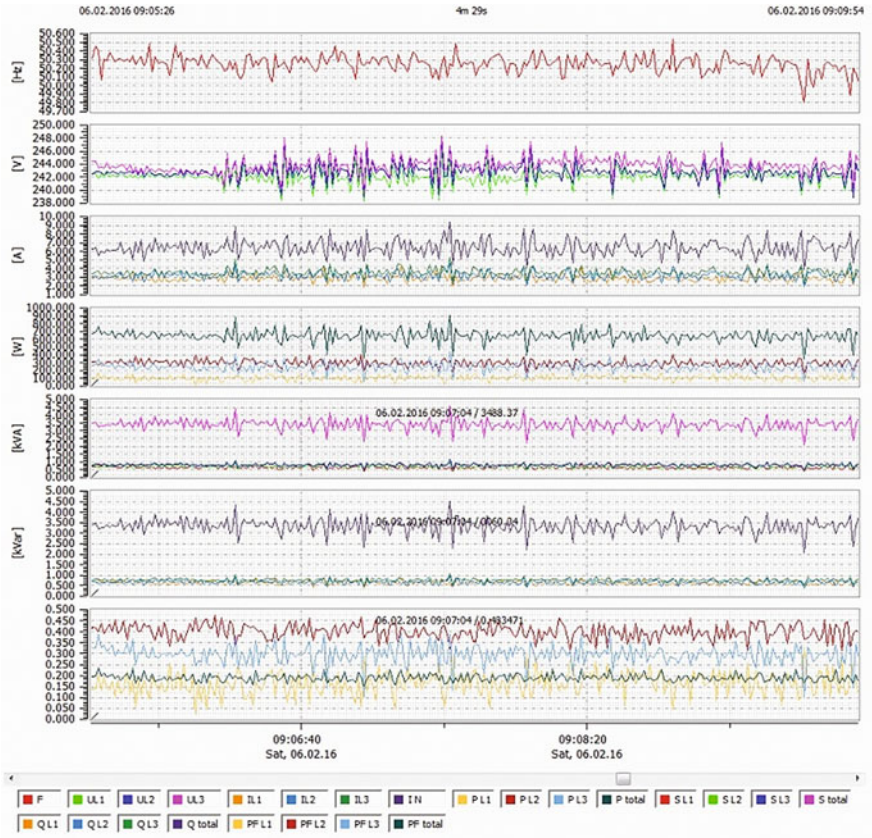


Fig. 3 Time plots for F, V, A, kW, kVA, kVar for power electronic loads

event list. There are no major PQ events but the number of events has happened due to the variable speed control of induction machine used in the central AC as shown in Fig. 10.

(c) Site 2: Lighting Feeder

This feeder does not have much of different types of PQ events but a huge number of infraction harmonics. This can be explained by the load type, which is CFLs and FLs. Due to ballasts, this feeder has a huge number of PQ events. Few rapid voltage changes are noted only in line 2 voltage plot, probably due to switching of light loads. This feeder also connected with capacitor banks, according to their ratings and designs, and it has been noted that most of the PQ events like harmonics are created due to the capacitor banks failures. In other words, the capacitance

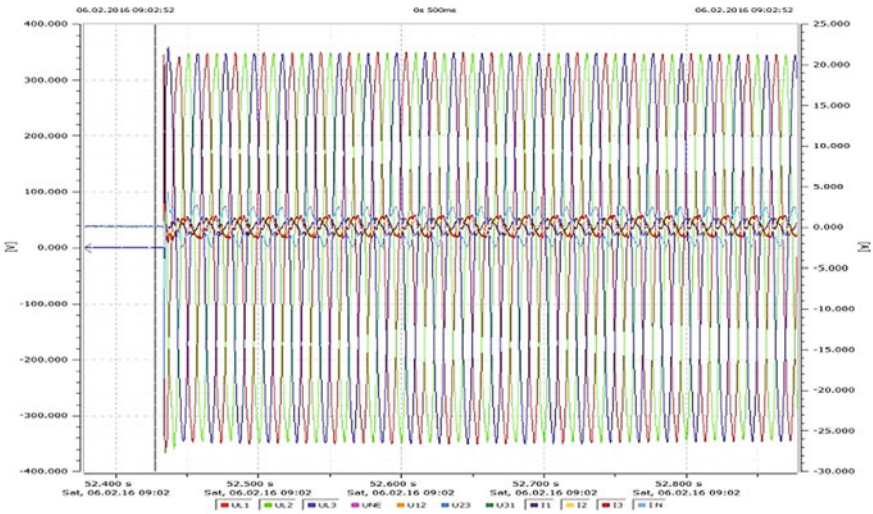


Fig. 4 Time plots for line voltages and currents

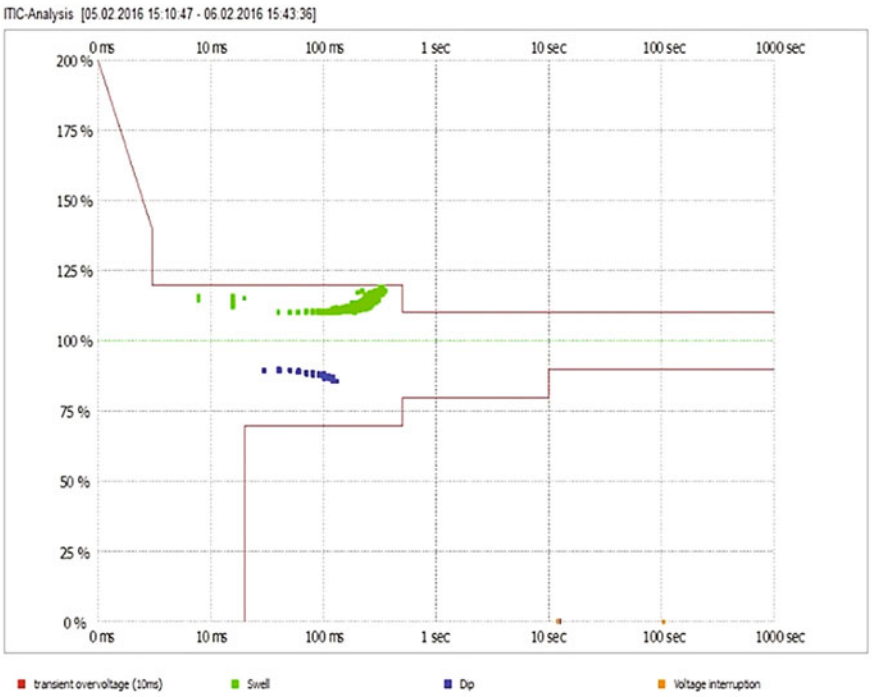


Fig. 5 ITIC curve for LED loads

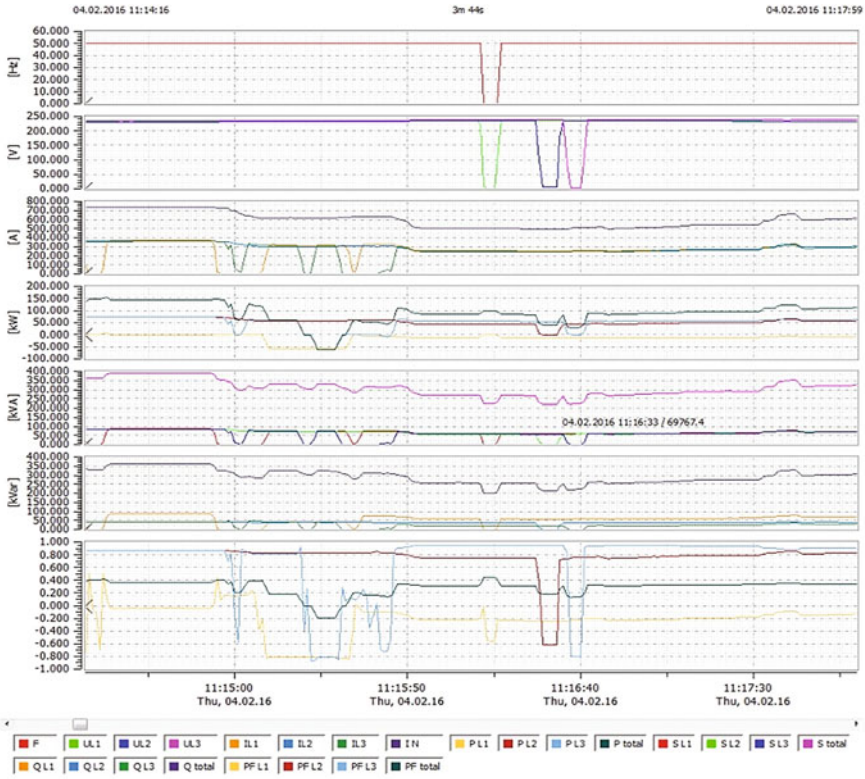


Fig. 6 Time plots for F, V, A, kW, kVA, kVar due to LED drivers

resistance is inversely proportional to frequency, which causes harmonics. Due to the harmonics, harmonics currents get in the capacitor banks which cause overload in the power systems (see Table 6).

(d) ***AC-UPS Feeder***

In the PQ event table list, dips are noted down as 3; these three dips are happened due to the power cut, and these three line voltages are noted as three singular dips. The same power cut has caused the voltage interruptions, which are noted down in the PQ event table. The other rapid voltage changes and infractions harmonics are happed due to the load is central AC which has huge three-phase induction motors with different variable speeds. This feeder has loaded with numbers of UPS and monitors, which can have an effect on the infraction harmonics. As the increase of

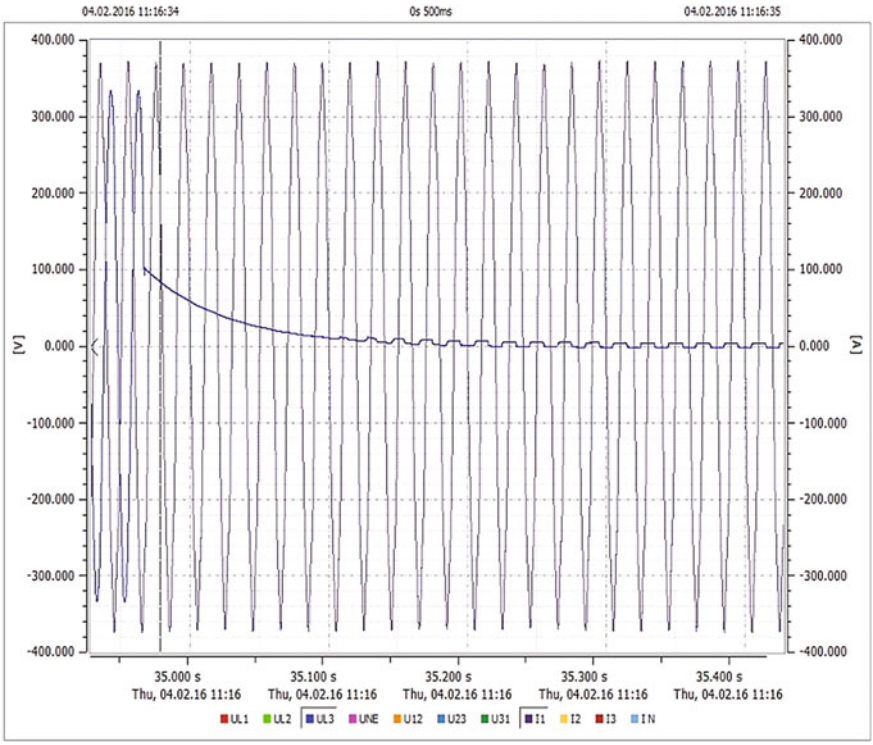


Fig. 7 Time plots for line voltage and current

Table 5 PQ events AC-UPS feeder

PQ event	No of times
Frequency deviations	0
Swell	2
Dip	3
Rapid voltage change	37
Voltage interruptions	3
Long time flicker	3
Infraction harmonics	15

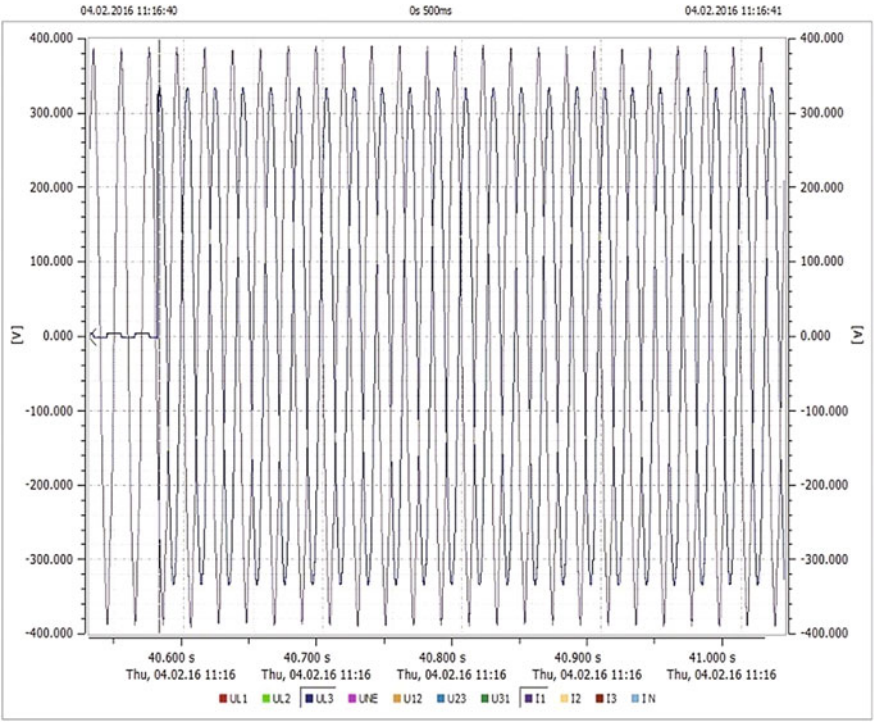


Fig. 8 Time plot for line voltage and current

uses of variable frequency drives in central ACs which is also known as VFDs, it can create high harmonics frequency components by the current and voltage emanating from it. As eddy current and hysteresis losses are major effects in a motor and hysteresis is directly proportional to frequency, it can be noted that eddy current and hysteresis losses can have an effect of the PQ events (see Table 7).

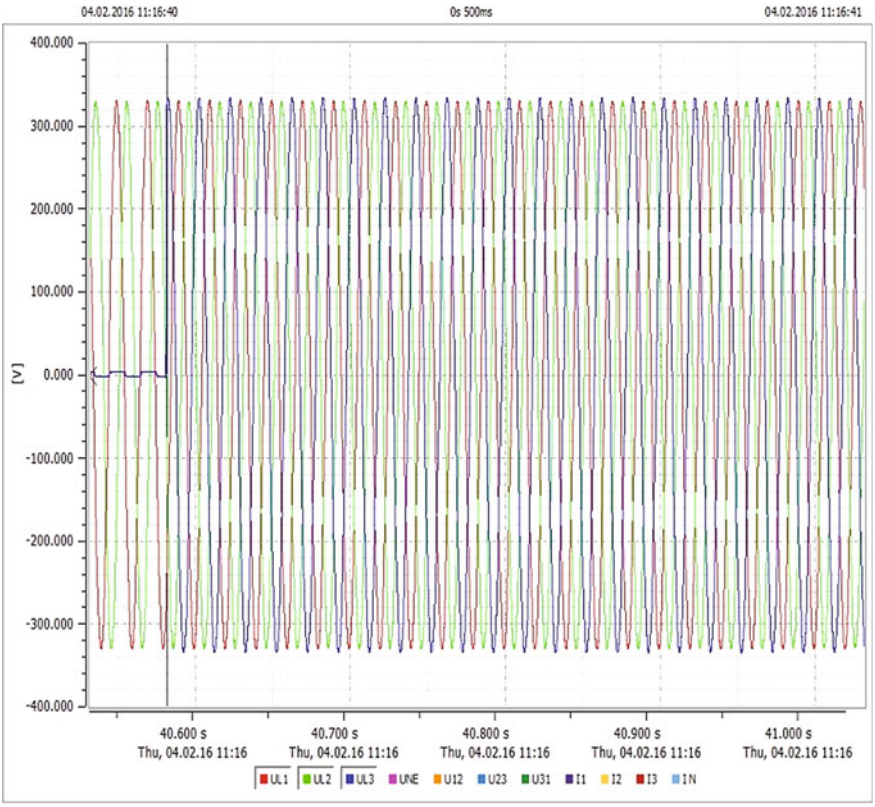


Fig. 9 Time plot for line voltages

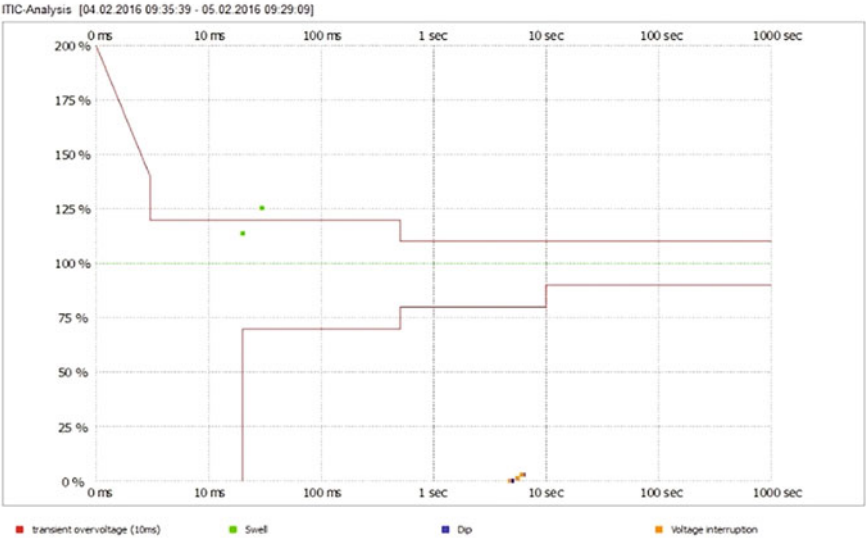


Fig. 10 ITIC curve for induction motor loads

Table 6 PQ events lighting feeder

PQ event	No of times
Frequency deviations	0
Swell	0
Dip	0
Rapid voltage change	5
Voltage interruptions	0
Long time flicker	0
Infraction harmonics	82,194

Table 7 PQ events for motor loads

PQ event	No of times
Frequency deviations	0
Swell	0
Dip	3
Rapid voltage change	1
Voltage	3
Long time flicker	0
Infraction harmonics	1

6 Conclusion

The survey of power quality discrete disturbances conducted in the academic campus of VIT University, Vellore, gave promising data to understand the various parameters of power quality, such as voltage interruptions, swells, dips, transient voltages, etc. The study involved understanding the subclasses of power quality disturbances and their characterization. Literature review suggests that characterizations of continuous disturbances have been carried out in various institutes and residence complexes; however, the discrete disturbances have not been subjected to characterization. This study also involved developing a single-site index for each discrete disturbance-type event recorded at varied 415 V sites in VIT University's main building substation with different types of load feeders at utility primary side of their facilities. Tabulated and graphical representations of each of the parameters are measured and analyzed, which help to conclude the proposed characterization of discrete disturbances and improve the power quality survey conducted in the university.

References

1. Karthikeyan, N., Sasitharan, S., Bhaskar, K.S., Mishra., M.K., Kumar, B.K.: Power quality survey in a technological institute. In: IEEE International Conference on Power Systems, pp. 1–6 (2009)
2. Herath, H.C., Gosbell, V.J., Perera, S.: Power quality (PQ) survey reporting: discrete disturbance limits. IEEE Trans. Power Deliv. **20**(2), 851–858 (2005)

3. Khalid, S., Dwivedi, B.: Power quality issues, problems, standards and their effects in industry with corrective means. Inter. J. Adv. Eng. Technol. **1**(2), 1–11 (2011)
4. EN B. 50160: Voltage characteristics of electricity supplied by public distribution systems. British Standards Institution (2000)
5. Explanation of PQ-Box 100 Limits, from help of WIN PQ Box software
6. Oliver, J.A., Lawrence, R., Banerjee, B.B.: How to specify power-quality-tolerant process equipment. IEEE Ind. Appl. Mag. **8**(5), 21–30 (2002)

Study of AGC in Two-Area Hydro-thermal Power System

Bibhu Prasad Ganthia, Anita Pritam, Krishna Rout, Siddhartha Singhsamant and Jayashree Nayak

Abstract Energy lack trouble united with fresh lofty petroleum cost has effected in strict crashes to various technical parts. In the past various decades, huge quantity of usual capitals of the earth have been unlimitedly used, and our living setting has been strictly razed and infected. An electrical grid may have several types of generators and loads; generators should be managed to preserve steady process of the system. In power systems, the inequity between generation and load should get exacted in tiny times, or else it will make the power line frequency to stray from the small worth. Huge frequency variation might intimidate the constancy and safety of the power system, or still bad, source eternal injure to the services. So in this article matching generation with load and regulating frequency at the usual point was calculated applying AGC with different controllers in two-area hydro-thermal power system.

Keywords AGC · LFC · Two area · Fuzzy · TLBO optimization

B.P. Ganthia (✉)
Department of Electrical Engineering, Indira Gandhi Institute of Technology, Sarang, Dhenkanal, India
e-mail: jb.bibhu@gmail.com

A. Pritam
Department of Mechanical Engineering, Balasore College of Engineering & Technology (BCET), Balasore, Odisha, India
e-mail: anitapritam@gmail.com

K. Rout
Indira Gandhi Institute of Technology, Sarang, Dhenkanal, India
e-mail: Krishna.chhoti@gmail.com

S. Singhsamant
Indira Gandhi Institute of Technology, Sarang, Dhenkanal, India
e-mail: siddharthasns.singhsamant@gmail.com

J. Nayak
Department of Mechanical Engineering, Indira Gandhi Institute of Technology, Sarang, Dhenkanal, India
e-mail: jayashree.nayak@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_39

1 Introduction

In an electric power system, automatic generation control (AGC) is a system for regulating the power output and frequency of numerous generators at various power plants, in retort to alter in the load. As a power grid needs that generation and load intimately poise instant by instant, common changes to the output of generators are essential. The poise can be referred by assessing the system frequency; if it is rising, more power is being created than applied, and every machine in the system is hastening. If the system frequency is falling, extra loads are on the system than the immediate creation can offer, and all generators are slowing down [3].

Where the grid has tied interlinks to nearby control areas, automatic generation control aids preserve the power exchanges above the tie lines at the listed heights. With computer-based control systems and numerous inputs, an automatic generation control system can get into version such stuffs as the mainly economical parts to regulate, the organization of thermal, hydroelectric, and other generation types, and even constraints narrated to the constancy of the system and ability of interlinks to other power grids.

Usually, the load–frequency control is achieved by two unusual control actions in inter-attached power systems:

(a) The primary speed control; and
(b) Supplementary or secondary speed control actions.

2 Automatic Generation Control

For huge level power a system which comprises interrelated control areas, and load frequency, it is vital to be the frequency along with bury area tie-line power close to the listed worth.

Load frequency control is the roots of several proceeded ideas of the huge level organize of the power system.

Mathematically,

$$P = \frac{EV}{X}\sin\delta \tag{1}$$

$$Q = \frac{EV}{X}\cos\delta - \frac{V^2}{X} \tag{2}$$

The swing equation is given by

$$\begin{aligned} \frac{\mathrm{d}^2\delta}{\mathrm{d}t^2} &= \Pi f(P_m - P_e) \\ &= \Pi f P_a \end{aligned} \tag{3}$$

where δ is the torque angle or load angle,

P_m	is the mechanical power input to the shaft of the generator,
P_e	is the output electrical power, and
$P_a = P_m - P_e$	is the net power.

When there is an unbalance between the torques operating in the rotor, the net torque reasoning acceleration or deceleration is

$$T_a = T_m - T_e$$

3 AGC in Two-Area Hydro-thermal Power System

In an electric power system, automatic generation control (AGC) is a scheme for regulating the power output and frequency of multiple generators at various power plants, in reply to varies in the load.

In several cases, a set of generators are directly joined inside and angle in unity. Also, the generator turbines lean to contain the equal reply individuality. Such a set of generators are supposed to be logical. Next, it is the potential to allow the LFC loop to signify the entire system and the set is named the control set [9]. Every control area is signified by an equal generating part intersected by a P_{tie}-line with reactance X_{12}. Below steady-state process, the shift of power over the P_{tie}-line P_{tie} can be inscribed like

$$P_{\text{tie}} = \frac{|E_1||E_2|}{X_{12}} \sin \delta_{12} \tag{4}$$

where $\delta_{12} = \delta_1 - \delta_2$ and $X_{12} = X_1 + X_2 + X_{\text{tie}}$.
Where E_1 and E_2 are the magnitudes of the end voltages of control areas 1 and 2 correspondingly, and δ_1 and δ_2 are the voltage angles of E_1 and E_2, correspondingly (Fig. 1).

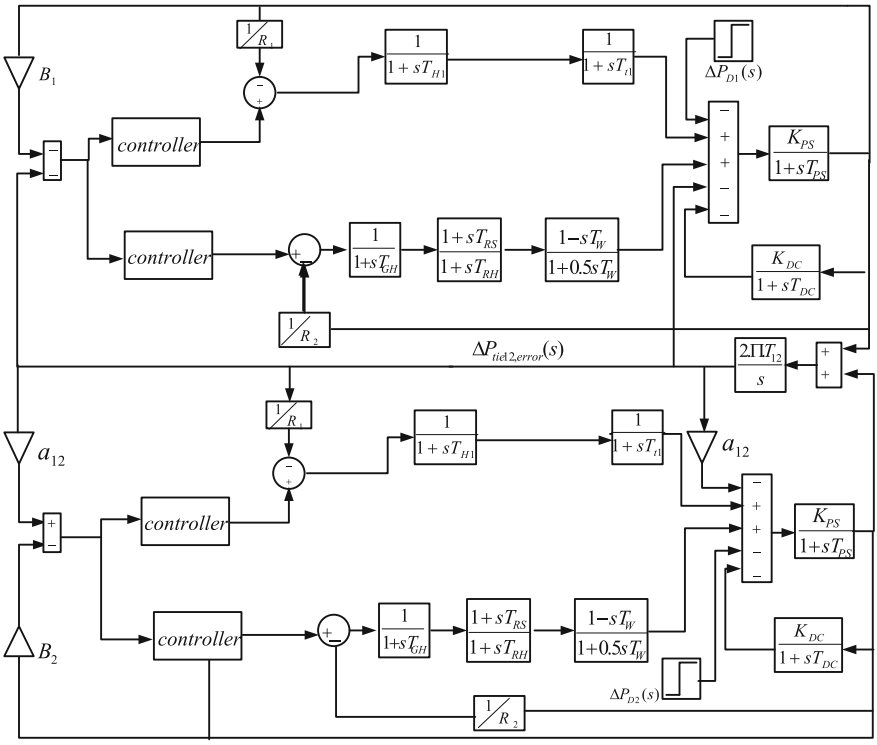


Fig. 1 Two-area multi-unit hydro-thermal power system

4 Simulation Results

Various controllers like PID, PD-PID, fuzzy PI, and PD-fuzzy PI are concerned to manage two-area hydro-thermal power system optimized by TLBO algorithm and its dynamic and transient actions are calculated (Figs. 2, 3, 4 and 5).

4.1 Extension to HVDC Link

See Figs. 6, 7 and 8; Tables 1, 2, 3 and 4.

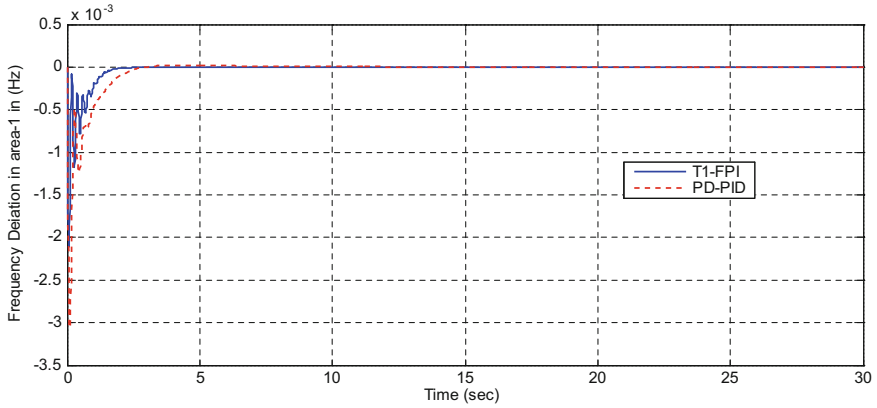


Fig. 2 Frequency deviation in area-1 multi-units hydro-thermal power system

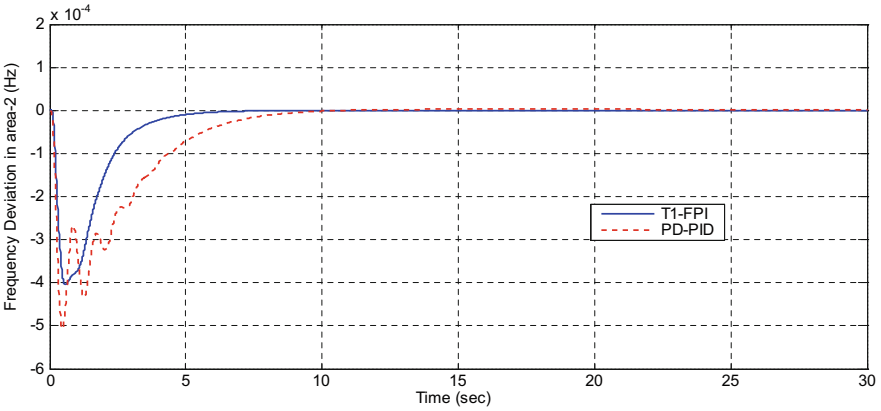


Fig. 3 Frequency deviation in area-2 multi-units hydro-thermal power system

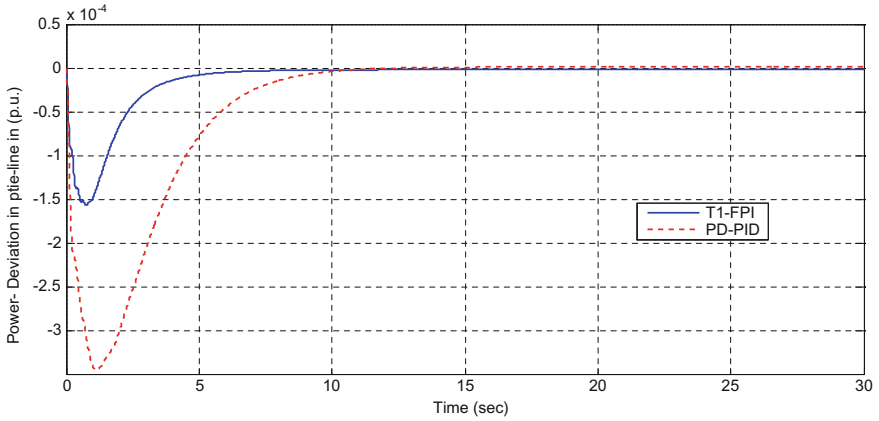


Fig. 4 Tie-line power deviation in multi-units hydro-thermal power system

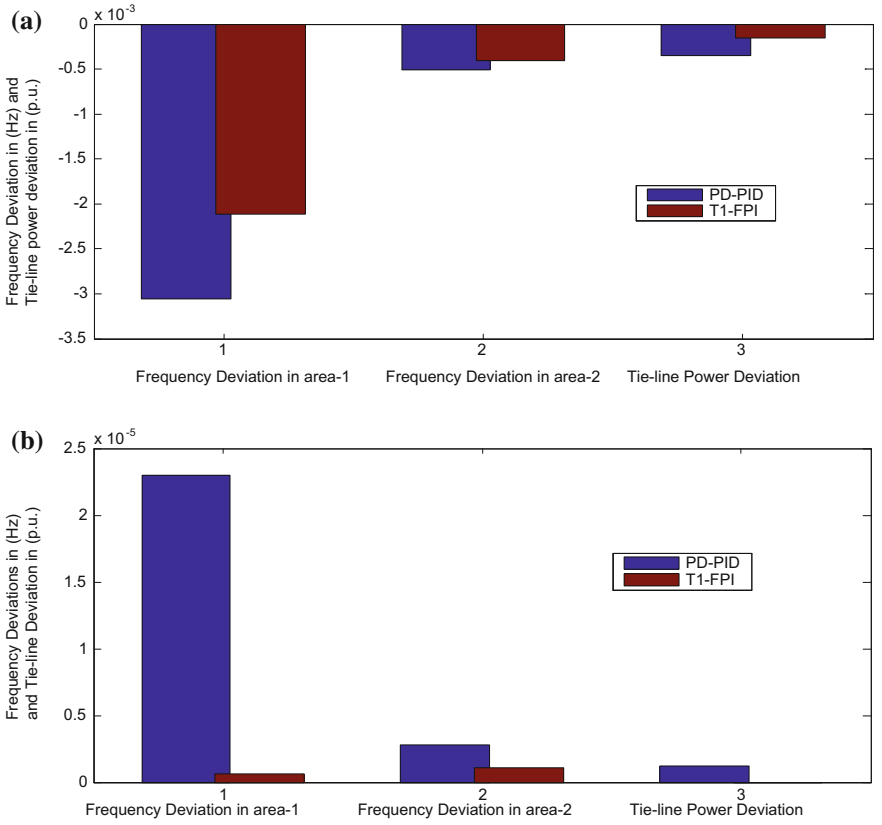


Fig. 5 Performance comparison of proposed TLBO optimized PD-PID and fuzzy-PI controller: **a** undershoots, **b** overshoots

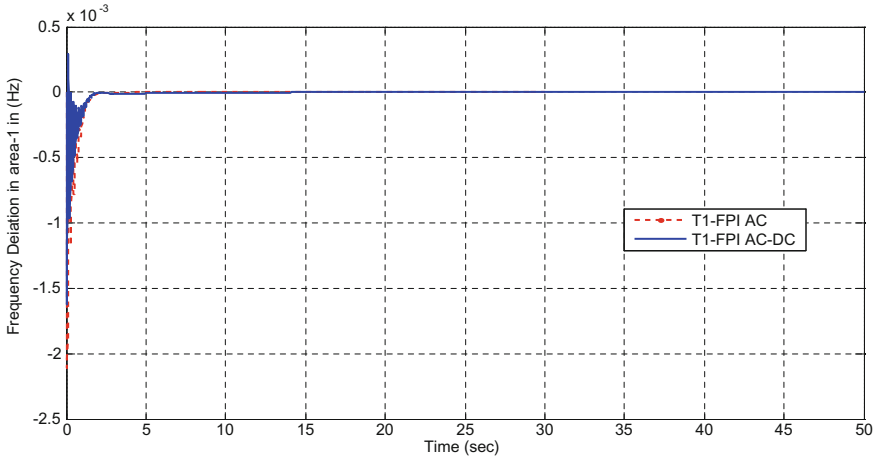


Fig. 6 Frequency deviation in area-1 multi-units hydro-thermal power system with HVDC link

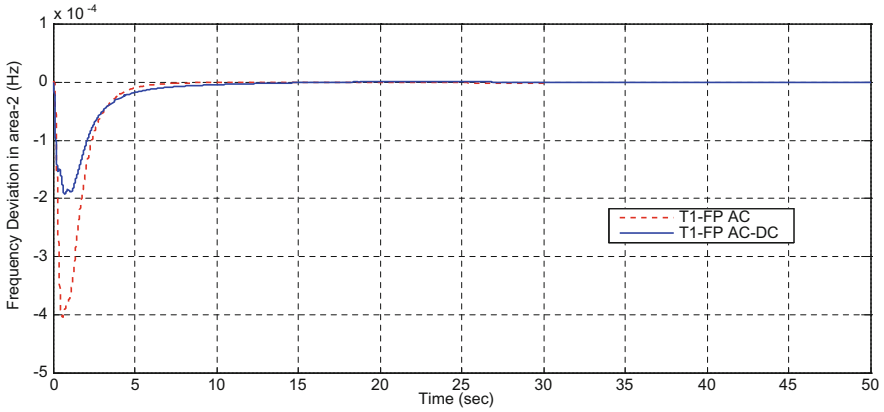


Fig. 7 Frequency deviation in area-2 multi-units hydro-thermal power system with HVDC link

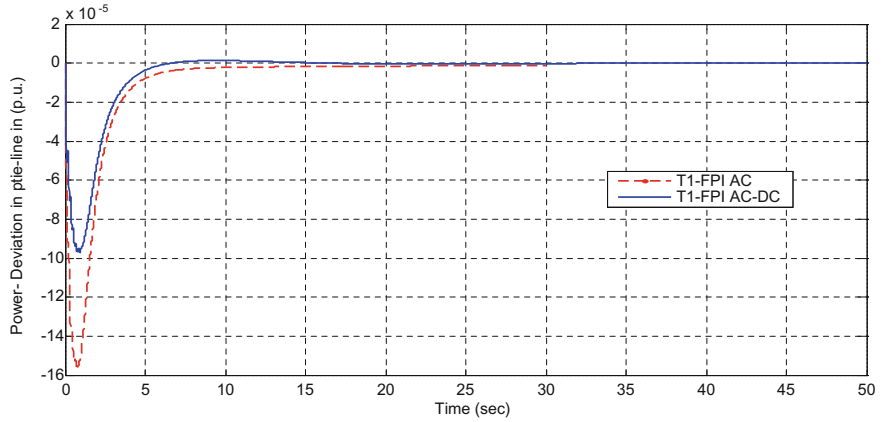


Fig. 8 Tie-line power deviation in area-1 multi-units hydro-thermal power system with HVDC link

Table 1 TLBO optimized controller parameters of cascade PD-PID and fuzzy-PI controllers for two-area multi-units thermal power system

Controller	Gains	Area-1		Area-2	
		Thermal	Hydro	Thermal	Hydro
PD-PI	K_1	1.9999	0.3255	1.4340	1.9989
	K_2	1.9898	0.4661	0.3806	0.4699
	K_3	1.9997	0.0415	2.0000	1.9991
	K_4	1.9899	0.6061	0.0102	0.0101
Fuzzy-PI	K_1	1.9989	0.0101	0.1816	0.0101
	K_2	0.9685	1.2606	0.3702	0.5378
	K_3	2.0000	0.2137	0.6040	1.5471
	K_4	1.9919	1.5006	0.0104	0.1211

Table 2 Peak undershoots (O_{sh}) and peak overshoots (O_{sh}) of Δf_1, Δf_2 and ΔP_{tie} for PD-PID and fuzzy-PI controllers

Controller structures		Δf_1(Hz)	Δf_2(Hz)	ΔP_{tie}(p.u.)
PD-PID	U_{sh} ($\times$ 10^{-3})	−3.0609	−0.5064	−0.3454
	O_{sh} ($\times 10^{-3}$)	0.0230	0.0028	0.0012
Fuzzy-PI	U_{sh} ($\times 10^{-3}$)	−2.1108	−0.4041	−0.1570
	O_{sh} ($\times 10^{-3}$)	0.0006	0.0011	0

Table 3 Two-area multi-units hydro-thermal system with HVDC link

Controller	Gains	Area-1		Area-2	
		Thermal	Hydro	Thermal	Hydro
Fuzzy-PI	K_1	3.0000	0.0100	0.8506	1.5824
	K_2	0.9793	0.2414	0.1846	0.9745
	K_3	3.0000	0.1441	2.3509	0.2972
	K_4	1.8461	0.1888	0.0100	2.1387

Table 4 Comparative analysis of two-area hydro-thermal power system with HVDC link in terms of undershoot and settling time as compared with Table 2

Controller structures		Δf_1(Hz)	Δf_2(Hz)	ΔP_{tie}(p.u.)
PD-PID	U_{sh} ($\times 10^{-3}$)	−1.6212	−0.1923	−0.0969
	T_{sh} ($\times 10^{-3}$)	1.4400	3.0000	2.0200

5 Conclusion

In this thesis an effort is finished to learn the presentation of regular generation manage for dissimilar power systems provided dissimilar controllers. Allowing for two-area hydro-thermal power system optimized by TLBO algorithm and applying different controllers, the dynamic and transient performances are calculated here. The innovation of the suggested system is exposed and fuzzy-PI controller explains superior transient study in terms of undershoot, and settling time. The suggested nonlinear three-area thermal power system replica is calculated by allowing for the result of generation speed constraints.

References

1. Sahu, R.K., Panda, S., Sekhar, G.C.: A novel hybrid PSO-PS optimized fuzzy PI controller for AGC in multi area interconnected power systems. Electr. Power Energy Syst. **64**, 880–893 (2015)

2. Pati, T.K., Nayak, J.R., Sahu, B.K.: Application of TLBO Algorithm to Study the Performance of Automatic Generation Control of a Two-Area Multi-Units Interconnected Power System, 978-1-4799-1823-2/15/$31.00 © IEEE (2015)
3. Del Valle, Y., Venayagamoorthy, G.K., Mohagheghi, S., Hernandez, J.C., Harley, R.G.: Particle swarm optimization: basic concepts, variants and applications in power systems. IEEE Trans. Evol. Comput.12(2) (2008)
4. Qin, A.K., Huang V.L., Suganthan, P.N.: Differential evolution algorithm with strategy adaptation for global numerical optimization. IEEE Trans. Evol. Comput. **13(**2) (2009)
5. Xiao, L., Zuo, X.: Multi-DEPSO: a DE and PSO based hybrid algorithm in dynamic environments. In: WCCI 2012 IEEE World Congress on Computational Intelligence, June 10–15. Brisbane, Australia, (2012)
6. Tang, K.S., Man, K.F., Chen, G., Kwong, S.: An optimal fuzzy PID controller. IEEE Trans. Industr. Electron. **48**(4) (2001)
7. Talaq, J., Al-Basri, F.: Adaptive fuzzy gain scheduling for load frequency control, IEEE Trans. Power Syst. **14**(1) (1999)
8. Elgerd, O.: Control of electric power systems. IEEE (1981)
9. Ganthia, B.P., Rout, K.: Deregulated power system based study of agc using pid and fuzzy logic controller. Int. J. Adv. Res. **4**(06) (2016)

Wavelet Technique-Based Fault Classification in Transmission Lines

Avagaddi Prasad and J. Belwin Edward

Abstract Power systems constitute a very big part of the electrical system pertaining in the current world. Each and every part of this system plays a very big role in the availability of the electrical power one utilizes at their homes, industries, offices, factories, etc. Power system constitutes of generation, utilization, distribution, and most importantly transmission of electricity. Any fault in any of these portions of the system causes a lot of trouble for the maintenance of the system. Overhead lines are the significant constituents of the power system and the issues happening are real purpose of concern toward this work. This paper aims to identify both the presence of faults and also the type of the fault in order to reach the conclusion to apply the best possible measure to reduce the loss that may be caused due to the fault. In order to do that simulation-based model in MATLAB is used and a code is realized in order to find out the detailed coefficient and energy of these coefficients of the faulty current signal. The coefficients are found out through the discrete wavelet transform. These characteristic features of the signal help identify and classify the fault type quickly. The GUI-based model of the code helps to bring down the human effort to calculate or compute the results.

Keywords Fault · Fault detection · Fault classification · Multi-resolution analysis Wavelet technique

1 Introduction

Fault conditions in the power system can cause a lot of issues and losses. These losses can be fatal too. The condition of a faulty phase if not understood and taken care of quickly would most probably lead to major problems. In order to get to the

A. Prasad (✉) · J. Belwin Edward
School of Electrical Engineering, VIT University, Vellore 632014, Tamil Nadu, India
e-mail: prasadavagaddi@gmail.com

J. Belwin Edward
e-mail: jbelwinedward@vit.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_40

conclusion of whether the fault is present and if yes, then which type of fault is present in the system needs to be identified as quick as possible. The electrical framework flaws are the best risk to the congruity of power supply. Deficiencies on overhead lines are an unavoidable issue. Thus, an all-around composed protection system must be given to distinguish and disengage faults quickly so that the harm and interruption brought on to the transmission system is minimized. Main part of the fault clearing system is the circuit breaker. Power circuit breakers are used at all voltage levels in a power system, i.e. faults which can either be single phase to ground (LG) or phase to phase (LL) or double phase to ground (LLG) or a three-phase fault (LLLG). Protection of power system using conventional methods is a slightly longer process. The real procedures utilized are fuzzy logic [1–3], wavelet strategy [4, 5], artificial neural systems [6, 7], wavelet-fuzzy [8], wavelet-neuro-fuzzy [9], and other latest techniques [10–13]. The accuracy of wavelet methodology is prevalent in correlation with different strategies and it gives greatly enhanced results.

The essential point of this article is to make sense of the sort of fault and whether the fault is present or not in a power system. The faults in concern are predominantly transmission line faults and all types of these faults are to be covered. This work also looks forward to providing a universal method to recognize faults and also discriminate among the types in case of any power system setup, specifications, parameters, etc. In order to reduce manual switching and calculation, the code tries to show the results of the scenario through minimum manual effort, hence providing results quicker for further measures.

2 Discrete Wavelet Transform (DWT)

A wavelet is a wave-like swaying with plentifulness that starts at zero, increments, and afterward diminishes back to zero. Wavelets can be joined, utilizing an "opposite, shift, duplicate and coordinate" procedure called convolution, with bits of a known signal to concentrate data from the obscure signal.

The DWT can be composed as

$$T_{m,n} = \int_{-\infty}^{\infty} x(t)\varphi_{m,n}(t)\mathrm{d}t. \tag{1}$$

The 1-D wavelet transform is given by

$$W_f(a,b) = \int_{-\infty}^{\infty} x(t)\varphi_{a,b}(t)\mathrm{d}t. \tag{2}$$

Table 1 MDC, E, and ER for no-fault condition

Condition	Phase A			Phase B			Phase C		
	MDC	E	ER	MDC	E	ER	MDC	E	ER
No fault	0.175	81.65	0.001	0.174	81.45	0.001	0.18	87.06	0.001

The inverse 1-D wavelet transform is given by

$$x(t) = (1/c) \int_0^{\infty} \int_{-\infty}^{\infty} W_f(a,b) \varphi_{a,b}(t) \mathrm{d}b \left(\frac{\mathrm{d}a}{a^2} \right), \tag{3}$$

$$\text{where } c = \int_{-\infty}^{\infty} \left(\frac{|\varphi\omega|^2}{\omega} \right) \mathrm{d}\omega < \infty.$$

3 Fault Classification Using DWT

For implementing the proposed method for fault detection and classification, a three-phase simulation model with a source voltage of 400 kV and corresponding zero load angle was used. This identification is based on the DWT energy coefficient of the signal. It generates a high-frequency component to signal. Initially generate the power signal using generator. Then design network power system using three-phase current signal. DWT analysis is performed to identify and classify the fault. Circuit breaker is used to make fault in the signal. Ratio is calculated to find the fault. Fault can be classified based on the ratio. The values of maximum detail coefficient (MDC), energy of the signal (E), and energy ratio (ER) after signal compression in no-fault condition are tabulated in Table 1. These values are used as a reference to compare with respective values in faulty conditions.

4 Numerical Simulation Results and Discussion

Output current waveform at no-fault condition is shown in Fig. 1. The detailed coefficients are close to zero in this case of fault. The energy ratios after signal compression can be seen to be similar for all the phases and nearing zero.

In LG, fault condition is shown in Fig. 2. The phase under fault can be identified by the MDC, E, and ER. From Table 2, it is clear that whichever phase the fault occurs in LG fault, that corresponding phase shows in increase in MDC, E, and ER. The other two phases show very little or no change in parameter values.

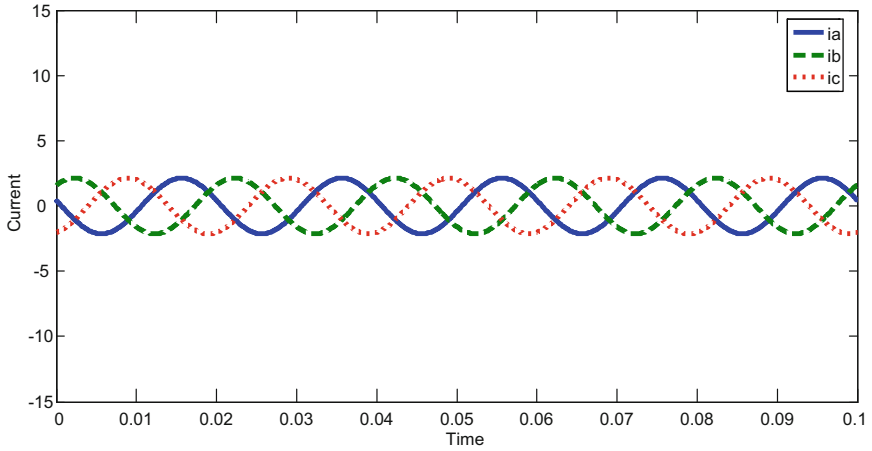


Fig. 1 Output current waveform at no-fault condition

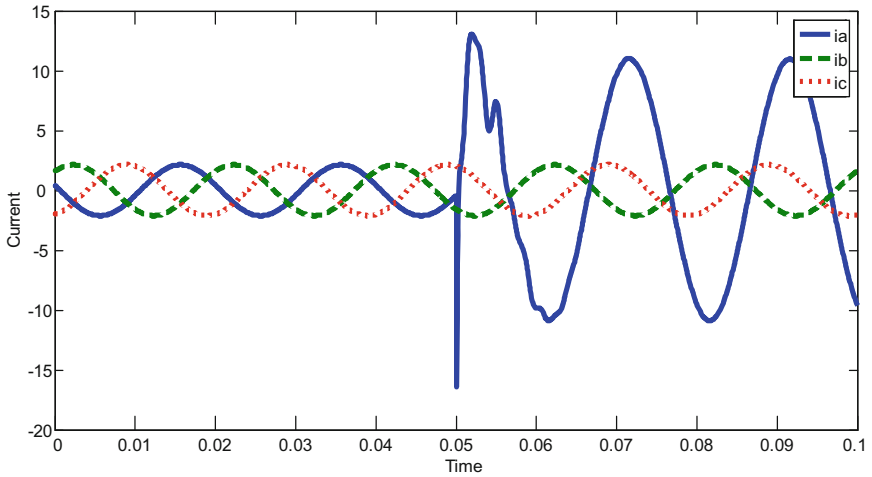


Fig. 2 Output current waveform at LG fault (AG) condition

Table 2 MDC, E, and ER for LG faults

Condition	Phase A			Phase B			Phase C		
	MDC	E	ER	MDC	E	ER	MDC	E	ER
No fault	0.175	81.65	0.001	0.174	81.45	0.001	0.18	87.06	0.001
AG	**0.966**	**195.5**	**0.008**	0.174	81.52	0.001	0.178	84.16	0.001
BG	0.175	81.51	0.001	**0.56**	**176.8**	**0.02**	0.178	84.16	0.001
CG	0.001	81.51	0.001	0.001	81.52	0.001	**0.029**	**173.6**	**0.029**

When the fault occurs in a LLG fault scenario, the current in both affected phases significantly changes as shown in Fig. 3. The unaffected phase has more or less the same characteristics as the no-fault condition. The faulty phases have maximum or higher values of detail coefficient; energy and energy ratio of the compressed signal are shown in Table 3. Here two of the phases are affected, so naturally those two respective phases have shown in increase in parameter values. The key thing to note here is that although energy ratio has increased for both the concerned phases they are not equal to each other. This is one of the key differentiators between LL and LLG fault.

In LL fault, the fault incidence in this case will show great amount of change in the faulty phases shown in Fig. 4.

Unaffected phase has the same current flow as in normal condition and also the values of detail coefficient and ratio after compression. The output values of the faulty phases are more than normal, but they being similar show that they are not in contact with ground. Here two of the phases are affected, so naturally those two respective phases have shown an increase in parameter values as shown in Table 4. The key thing to note here is that energy ratio has increased for both the concerned phases and they are equal or almost equal to each other.

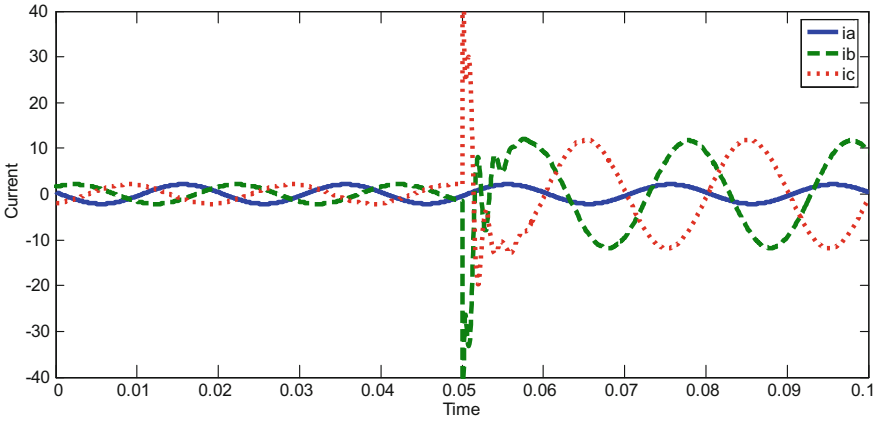


Fig. 3 Output current waveform at LLG fault (BCG) condition

Table 3 MDC, E, and ER for LLG faults

Condition	Phase A			Phase B			Phase C		
	MDC	E	ER	MDC	E	ER	MDC	E	ER
No fault	0.175	81.65	0.001	0.174	81.45	0.001	0.18	87.06	0.001
ABG	**0.966**	**195.5**	**0.008**	**0.56**	**176.8**	**0.02**	0.178	84.16	0.001
BCG	0.175	81.51	0.001	**0.561**	**176.9**	**0.02**	**0.599**	**173.7**	**0.029**
ACG	**0.966**	**195.5**	**0.008**	0.174	81.52	0.001	**0.599**	**173.7**	**0.029**

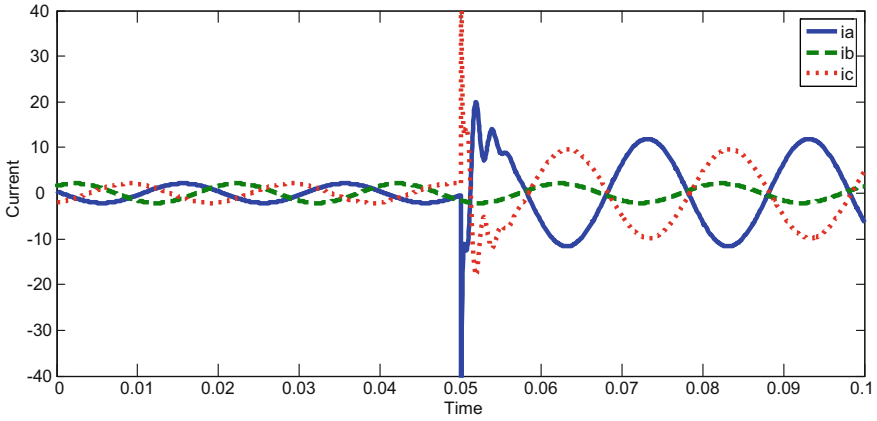


Fig. 4 Output current waveform at LL fault (AC) condition

Table 4 MDC, E, and ER for LL faults

Condition	Phase A			Phase B			Phase C		
	MDC	E	ER	MDC	E	ER	MDC	E	ER
No fault	0.175	81.65	0.001	0.174	81.45	0.001	0.18	87.06	0.001
AB	**0.006**	**180.2**	**0.006**	**0.006**	**155.4**	**0.006**	0.001	87.06	0.001
BC	0.001	81.65	0.001	**0.009**	**176.1**	**0.024**	**0.25**	**146.4**	**0.025**
AC	**0.712**	**142**	**0.018**	0.174	81.44	0.001	**0.549**	**174.7**	**0.019**

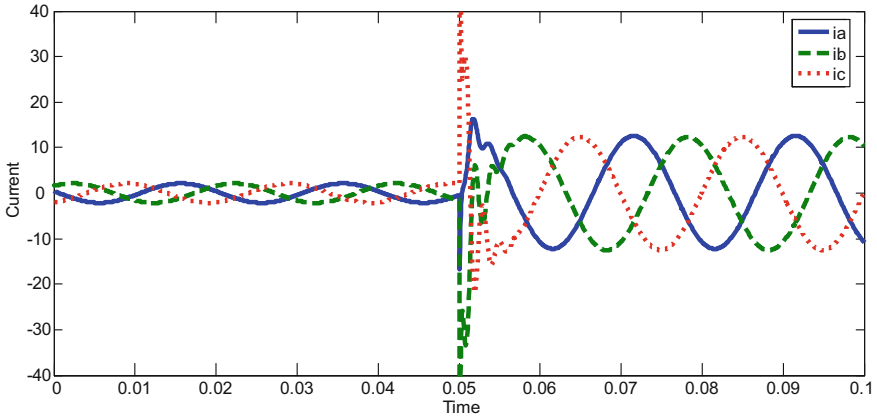


Fig. 5 Output current waveform at LLLG (ABCG) condition

In three-phase fault at fault inception, the current signal of all the three phases change drastically as shown in Fig. 5. The ratios and coefficient values can also be seen to be more than the normal condition. For three-phase fault, it can observe an

Table 5 MDC, E, and ER for LLLG fault

Condition	Phase A			Phase B			Phase C		
	MDC	E	ER	MDC	E	ER	MDC	E	ER
No fault	0.175	81.65	0.001	0.174	81.45	0.001	0.18	87.06	0.001
ABCG	**0.008**	**200**	**0.008**	**0.56**	**176.8**	**0.002**	**0.484**	**163.9**	**0.029**

increase in energy of signal and energy ratio of compressed signal for all three phases which are shown in Table 5.

5 Conclusion

The principle point of the work is to identify and classify faults in overhead lines. This is realized using wavelet analysis because it takes into consideration both frequency and time domain. This work uses parameters like MDC, E, and ER after compression to make observations. This is because these parameters are characteristic for a particular type of fault current. Hence, they are optimal for the classification process. Taking the values of the three parameters of no-fault condition as base, we can compare the respective values of the parameters of every type of fault in order to make comparisons and arrive at a conclusion. The outcome signifies that during the no-fault condition all the three parameter values for each phase are comparatively lower. Under fault conditions the value of the respective phase under fault increases and hence shows the result as to which fault is present. Using reverse bi-orthogonal wavelet for transform helps to get the result quicker and the use of this wavelet is helpful to realize the aim. Using wavelet as a method instead of other available toolbox allows faster calculation because wavelet transform considers both frequency and time domain. Using this technique a lot of effects and losses due to faults in transmission lines can be avoided. This will help in reducing damages in electrical systems and potentially help for continuous power supply.

References

1. Samantaray, S.R.: A systematic fuzzy rule based approach for fault classification in transmission lines. Appl. Soft Comput. **13**(2), 928–938 (2013)
2. Guillen, D., Paternina, M.R.A., Zamora, A., Ramirez, J.M., Idarraga, G.: Detection and classification of faults in transmission lines using the maximum wavelet singular value and Euclidean norm. IET Gener. Transm. Distrib. **9**(15), 2294–2302 (2015)
3. Prasad, A., Edward, J.B., Roy, C.S., Divyansh, G., Kumar, A.: Classification of faults in power transmission lines using fuzzy-logic technique. Ind. J. Sci. Technol. **8**(30), 1–6 (2015)
4. Pérez, F.E., Orduna, E., Guidi, G.: Adaptive wavelets applied to fault classification on transmission lines. IET Gener. Transm. Distrib. **5**(7), 694–702 (2011)
5. Prasad, A., Edward, J.B.: Application of wavelet technique for fault classification in transmission systems. Procedia Comput. Sci. **92**, 78–83 (2016)

6. He, Z., Lin, S., Deng, Y., Li, X., Qian, Q.: A rough membership neural network approach for fault classification in transmission lines. Electr. Power Energy Syst. **61**, 429–439 (2014)
7. Seyedtabaii, S.: Improvement in the performance of neural network-based power transmission line fault classifiers. IET Gener. Transm. Distrib. **6**(8), 731–737 (2012)
8. Reddy, J.M., Mohanta, D.K.: A wavelet-fuzzy combined approach for classification and location of transmission line faults. Electr. Power Energy Syst. **29**(9), 669–678 (2007)
9. Jung, C.K., Kim, K.H., Lee, J.B., Klockl, B.: Wavelet and neuro-fuzzy based fault location for combined transmission systems. Electr. Power Energy Syst. **29**(6), 445–454 (2007)
10. Moravej, Z., Pazoki, M., Khederzadeh, M.: New pattern-recognition method for fault analysis in transmission line with UPFC. IEEE Trans. Power Delivery **30**(3), 1231–1242 (2015)
11. Pan, S., Morris, T., Adhikari, U.: Classification of disturbances and cyber-attacks in power systems using heterogeneous time-synchronized data. IEEE Trans. Industr. Inf. **11**(3), 650–662 (2015)
12. Biswal, M.: Faulty phase selection for transmission line using integrated moving sum approach. IET Sci. Meas. Technol. **10**(7), 761–767 (2016)
13. Rosa, G., Costa, M.A.: Robust functional analysis for fault detection in power transmission lines. Appl. Math. Model. **40**(21–22), 9067–9078 (2016)

Comparative Analysis of Feed-Forward and Synchronous Reference Frame Control-Based Dynamic Voltage Restorer

A. Rini Ann Jerin, K. Palanisamy, S. Umashankar and Padmanaban Sanjeevikumar

Abstract The protection of nonlinear and sensitive loads can be achieved economically through series compensation-based dynamic voltage restorer. The effective voltage compensation by dynamic voltage restorer depends on the controller used for voltage sag detection. In this paper, the sag detection of dynamic voltage restorer employing feed-forward control and synchronous reference frame control are compared. The efficiency of sag detection of these controls in dynamic voltage restorer for in-phase compensation of balanced sags with PWM-based injection of compensation voltage is analyzed. Comparisons on the performance of the controllers are shown clearly using Matlab/Simulink-based simulated results.

Keywords Dynamic voltage restorer · Series compensation · Balanced sags Voltage sag · Feed-forward control · SRF control

1 Introduction

Voltage sags are the most frequent power quality issues among power quality disturbances during any fault conditions. This calls for compensation and protection of sensitive loads to maintain a constant voltage and current. Voltage sags can be defined as reduction in the supply voltage by 10% or even up to 90% from the nominal voltage for a duration of 10 ms to 1 min [1]. The steady increase in the power electronic equipment usage has also raised the harmonic levels in the system thereby requiring mandatory power quality improvement to maintain the system

A. Rini Ann Jerin (✉) · K. Palanisamy · S. Umashankar
School of Electrical Engineering, VIT University, Vellore
632014, Tamil Nadu, India
e-mail: riniannjerin@gmail.com

P. Sanjeevikumar
Department of Electrical and Electronics Engineering, University of Johannesburg,
Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_41

stability. The efficiency of voltage profile improvement using dynamic voltage restorer (DVR) with new control strategy is a very important study in the current scenario. Studies of power quality issues in grid-connected wind turbines have been carried out in the recent past and have even suggested the implementation of DVR for improving the LVRT capability [2]. Therefore, comparative analysis of the control strategies utilized for DVR operation will help in analyzing the operation and functionality of the device [3].

DVR is connected through a series injection transformer between the grid and the sensitive or nonlinear loads, and a voltage source converter (VSC) injects voltage in series [4]. The compensation voltages are injected across the distribution line according to the controlled switching sequence of the VSC, by drawing real power from the energy source connected [5]. Filters based on inductors and capacitors are connected to mitigate the ripples and harmonics in the injected voltage. A DVR is capable of restoring voltage sags, swells, harmonics, and even transients [5]. The DVR using conventional feed-forward control and synchronous reference frame (SRF) theory controller for voltage sag detection is compared in this paper. Based on the compensation the load voltage is restored back to the nominal voltage amplitude during fault conditions [6].

Generally, the controller efficiency determines the performance of a DVR. Therefore, design of high-performance control algorithms which are robust and have effective steady-state and transient performance becomes crucial. Hence, the voltage injection control using conventional feed-forward control and the SRF theory control of DVR system as shown in Fig. 1 is compared in this paper.

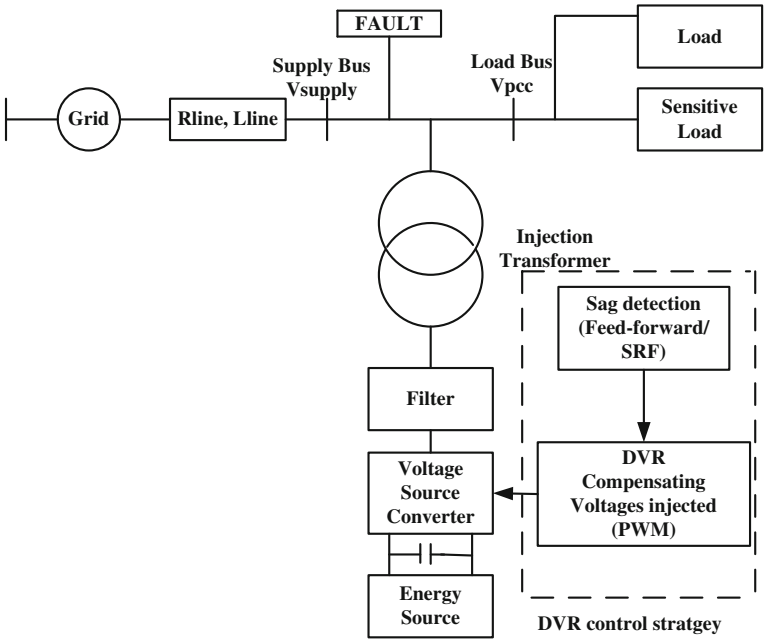


Fig. 1 Dynamic voltage restorer-based power quality improvement

The comparison is made for the total harmonic distortion (THD) values using both the control strategies. The Matlab/Simulink-based simulation results for comparison of the control strategies using in-phase compensation technique are shown to validate the results.

2 DVR Operation and Control

DVR operation is very simple and consists of a voltage source converter controlled through voltage sag detection and reference generation. The sag detection method discussed in this paper consists of the conventional feed-forward control and the SRF theory control. The control method measures and analyzes the voltage sag in the grid voltage based on the specific control strategy. The efficiency of the DVR operation during different disturbance conditions is determined by the control technique employed for the sag detection [7]. The reference signal for injecting the series injection voltage is obtained through any one of the three compensation strategies which are available. The three compensation strategies for reference generation are in-phase compensation, pre-sag compensation, and minimal energy compensation methods [1].

During in-phase compensation, the PLL will not be locked and the voltage rating in the dc-link is minimal. Therefore, reduced rating of voltage source converter is possible by utilizing this in-phase compensation method. But since this method leads the load voltage magnitude, it is unable to correct the voltage sags with phase jumps [1]. Therefore, this compensation method is not suitable for loads which are sensitive for phase jumps. In Fig. 2 V_s denotes supply voltage, V_{s1} denotes the supply voltage with reduced amplitude due to sag, and I_L *i*s the load current. V_{c1} is compensation voltage with same magnitude and in-phase to the supply voltage but not in-phase to load voltage, therefore not suitable for loads sensitive to phase jump. V_{c2} is the compensation voltage where it is compensated to pre-sag values with same amplitude and phase angle in pre-sag compensation but requires higher rating of the voltage source converter. V_{c3} is the compensation voltage in quadrature to load current in minimized energy compensation with only reactive power supply from DVR and this method is utilized for self-supported DVR [3]. In this paper the in-phase compensation is utilized.

The compensation voltage is injected by the voltage source converter based on the signals generated using PWM control strategy. A series injection transformer is connected between the point of common coupling (PCC) of the distribution side of

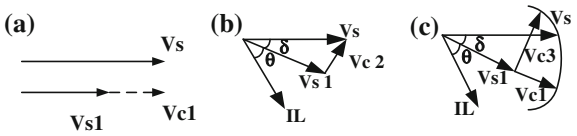


Fig. 2 DVR compensation techniques, **a** In-phase. **b** Pre-sag. **c** Minimum energy compensation

the grid and load. The control strategy and the compensation technique are chosen to determine the efficiency of the DVR.

2.1 Feed-Forward Control

Feed-forward is a conventional open-loop type control technique which compares the supply voltage with the reference values and measures the error to give the required value of injected voltage. In this control, the three-phase supply voltage is transformed into d-q components using a PLL [3]. Using in-phase compensation technique, the PLL is synchronized and therefore will not be locked during the compensation. The supply of d-q components is compared and subtracted from the reference voltage d-q components $(v_{\text{dref}}, v_{\text{qref}})$ to obtain the necessary injected voltage d-q components. The transformed three-phase injection voltage is supplied from the voltage source converter through the series injection transformer. This control strategy is shown in Fig. 3 where the supply voltage components are v_{sa}, v_{sb}, v_{sc}, and v_s is the supply voltage for determining θ value for calculating phase angle using PLL. (v_{ca}, v_{cb}, v_{cc}) are the compensation voltage components injected through the voltage source converter.

2.2 Synchronous Reference Frame (SRF) Control Technique

The synchronous reference frame (SRF) theory is used for detecting the sag and generating the appropriate reference for deriving the IGBT gating signals [8]. This control includes the feedback control of the reference load voltage v_L^* which is derived and converted to rotating reference frame using abc-dq0 by Park's transformation [9]. This is done using the $\sin\theta$, $\cos\theta$ unit vectors from a phase-locked loop (PLL) [10].

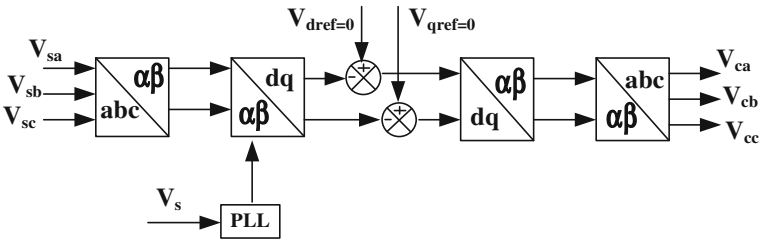


Fig. 3 Feed-forward control strategy for DVR

$$\begin{bmatrix} v_{Lq} \\ v_{Ld} \\ v_{L0} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin\theta & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} v^*_{La} \\ v^*_{Lb} \\ v^*_{Lc} \end{bmatrix} \tag{1}$$

$$v_{Dd} = v_{Sd} - v_{Ld} \tag{2}$$

$$v_{Dq} = v_{Sq} - v_{Lq} \tag{3}$$

$$v^*_{Dd} = v^*_{Sd} - v_{Ld} \tag{4}$$

$$v^*_{Dq} = v^*_{Sq} - v_{Lq}. \tag{5}$$

The reference calculated by subtracting the reference from the actual is used to regulate using two PI controllers [11].

where load voltages in abc frame are as follows:
Load voltages: (v_{La}, v_{Lb}, v_{Lc}); Reference load voltages: $\left(v^*_{La}, v^*_{Lb}, v^*_{Lc}\right)$.
Load voltages in d-q frame are as follows:
Load voltages: $\left(v_{Ld}, v_{Lq}, v_{L0}\right)$; Reference load voltages: $\left(v^*_{Ld}, v^*_{Lq}\right)$.
PCC voltages in rotating reference frame in d-q frame are as follows:
Supply voltage: $\left(v_{sd}, v_{sq}\right)$; Reference supply voltage: $\left(v^*_{sd}, v^*_{sq}\right)$

$$\begin{bmatrix} v^*_{dvra} \\ v^*_{dvrb} \\ v^*_{dvrc} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \sin(\theta) & 1 \\ \cos(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} v^*_{Dq} \\ v^*_{Dd} \\ v^*_{D0} \end{bmatrix}. \tag{6}$$

DVR voltages in rotating reference frame in d-q frame are as follows:
DVR voltages: $\left(v_{Dd}, v_{Dq}\right)$; DVR reference voltages: $\left(v^*_{Dd}, v^*_{Dq}, v^*_{D0}\right)$.

DVR voltage in abc frame are as follows: Actual DVR voltages: $(v_{dvra}, v_{dvrb}, v_{dvrc})$; Reference DVR voltages: $\left(v^*_{dvra}, v^*_{dvrb}, v^*_{dvrc}\right)$. These are used to generate the PWM pulses to a voltage source converter of the DVR which is operated at 10 kHz. The control strategy operates as shown in Fig. 4.

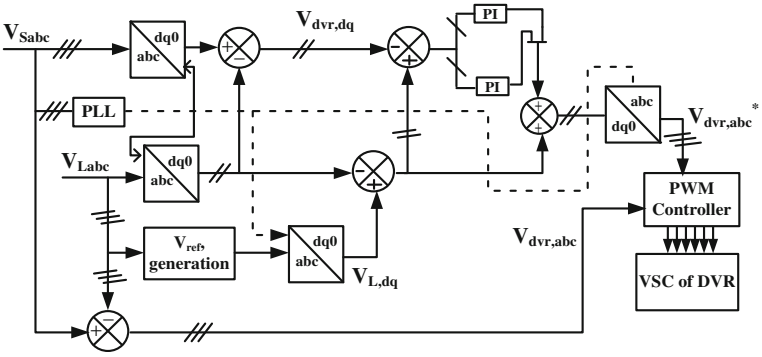


Fig. 4 Synchronous reference frame theory (SRF) control for DVR

Table 1 Parameters used for simulation

System parameters	Values
Supply voltage and frequency	415 V, 50 Hz
Line impedance	(L_s) 1 mH
	(R_s) 0.1 Ω
Turns ratio series injection transformer	1:1
Filter inductance	0.9 mH
Filter capacitance	10 μF
Load-active power	1 kW
DC voltage of DVR	300 V

3 Simulation Results

The simulation of the DVR using feed-forward control and SRF control for RL load during 0.3 pu balanced sag for 0.8 ms time interval is observed. The sag compensation and harmonic mitigation are observed and the THD values are compared. Table 1 gives the parameters used in the simulation done with MATLAB/Simulink tool.

Figure 5 shows compensation of the balanced sag using feed-forward control. But this control is not suitable for unbalanced voltage sags due to the negative sequence components. Using abc to d-q transformation in SRF control, simple PI structures are used for the power and current controllers. Since they operate on DC converter variables in the synchronous frame and they can achieve zero steady-state error because of the infinite DC gain of a PI regulator, and also, when the voltage is unbalanced, negative sequence component appears. Therefore, proper current reference calculation and regulation is required to fully control the system. The compensation of balanced sag using SRF control is shown in Fig. 6.

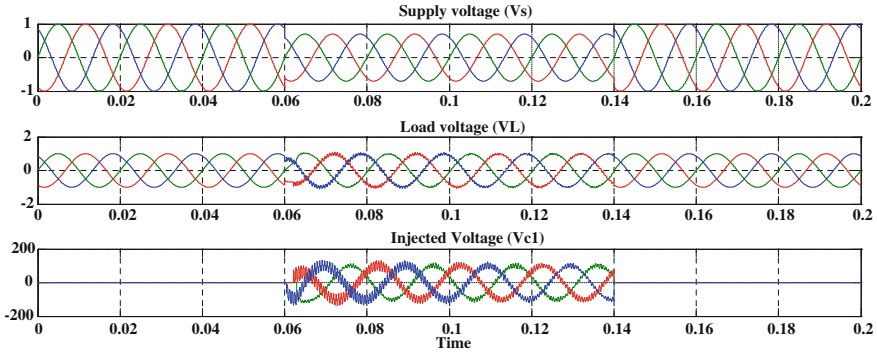


Fig. 5 DVR with feed-forward control for 0.3 pu balanced sag between 0.06 and 0.14 s

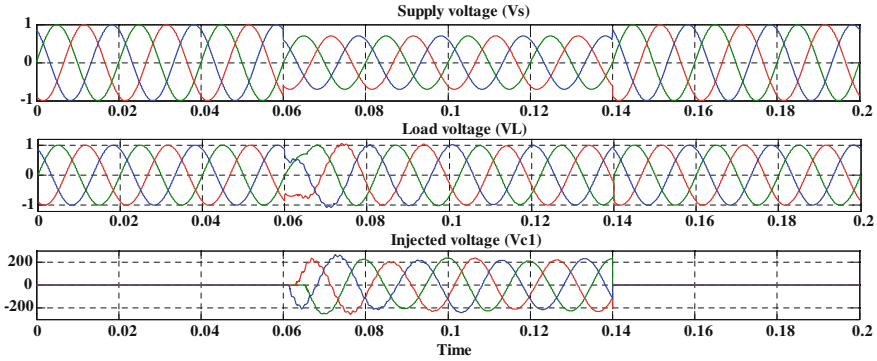


Fig. 6 DVR with SRF control for 0.3 pu balanced sag between 0.06 and 0.14 s

Table 2 Comparison of THD values for the feed-forward and SRF control

THD values	Feed-forward control (%)	SRF control (%)
Supply voltage	30	30
Supply current	5.18	1.34
Load voltage	5.24	1.35
Load current	5.18	1.34

4 Comparison and Discussion

The comparison of the performance of feed-forward control and SRF control of DVR based on the total harmonic distortion (THD) values with RL load for 30% harmonics in supply voltage is done and shown in Table 2.

The harmonic compensation using feed-forward control is shown in Fig. 7 and using SRF control is shown in Fig. 8. Figure 9 shows that the THD value of DVR

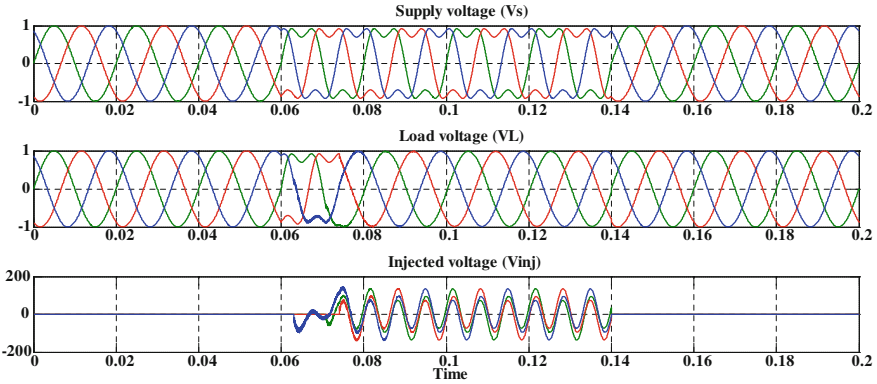


Fig. 7 Harmonic mitigation of DVR with feed-forward control for 30% harmonics in the supply voltage sag between 0.06 and 0.14 s

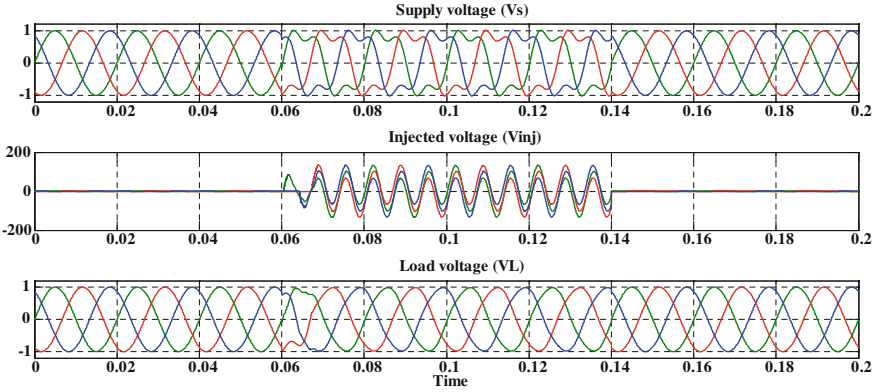


Fig. 8 Harmonic mitigation of DVR with SRF control for 30% harmonics in the supply voltage sag between 0.06 and 0.14 s

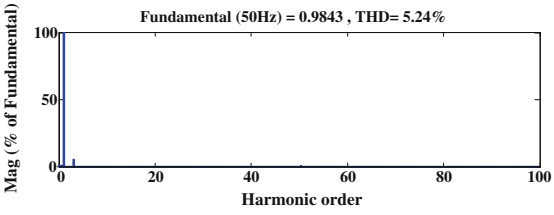


Fig. 9 THD of DVR Load voltage with feed-forward control

load voltage after sag mitigation using feed-forward control is 5.24%, and Fig. 10 shows THD value of DVR load voltage using SRF control with 1.35%. It is quite obvious that the THD values are improved using SRF control. Also, it is observed

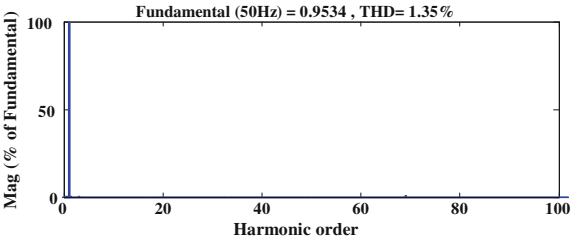


Fig. 10 THD of DVR load voltage with SRF control

that feed-forward control causes phase jump, whereas the SRF control avoids phase jump. Therefore, SRF control is comparatively better and more suitable for phase-sensitive critical loads.

5 Conclusion

The power quality improvement using DVR through series voltage compensation is considered. The performance of DVR with feed-forward control and SRF control are compared in this paper. The comparison of THD values shows the effectiveness of the control strategies. The comparison of the THD values indicates that the SRF control could be more suitable for power quality improvement during unbalanced sag and transient conditions. The reduced rating of the DVR voltage source converter could be possible with in-phase compensation. But this may require external source and at the cost of phase jumps, which may not be desirable for loads which are sensitive to phase jumps. In comparison the SRF control has lower THD and within the IEEE 519 standard compared to the feed-forward control. Therefore, SRF control seems to be more suitable for critical loads which are sensitive to phase jumps.

References

1. Sadigh, A.K., Smedley, K.M.: Review of voltage compensation methods in dynamic voltage restorer (DVR). In2012 IEEE Power and Energy Society General Meeting, pp. 1–8 (2012)
2. Thirumoorthy, A.D., Chellamuthu, C.: Study on Power Quality Issue Of Grid Connected Wind Farm. Centre for Wind Energy Technology (CWET), March 2014, http://cwet.res.in/
3. Padiyar, K.R.: FACTS controllers in power transmission and distribution. New Age International (2007)
4. Jing, W., Aiqin, X., Yueyue, S.: A survey on control strategies of dynamic voltage restorer. In: 2008 13th International Conference on Harmonics and Quality of Power, pp. 1–5. IEEE (2008)
5. Jayaprakash, P., Singh, B., Kothari, D.P., Chandra, A., Al-Haddad, K.: Control of reduced-rating dynamic voltage restorer with a battery energy storage system. IEEE Trans. Ind. Appl. **50**(2), 1295–1303 (2014)

6. Prabaharan, N., Palanisamy, K.: Investigation of single phase reduced switch count asymmetric multilevel inverter using advanced pulse width modulation Technique. Int. J. Renew. Energy Res. **5**(3), 879–890 (2015)
7. Prabaharan, N., Palanisamy, K.: Comparative Analysis of Symmetric and Asymmetric Reduced Switch Multilevel Inverter Topology Using Unipolar Pulse Width Modulation Strategies. IET Power Electronics. doi:10.1049/iet-pel.2016.0283
8. Kanjiya, P., et al.: "SRF theory revisited" to control self-supported dynamic voltage restorer (DVR) for unbalanced and nonlinear loads. IEEE Trans. Ind. Appl. **49**(5), 2330–2340 (2013)
9. Li, Y.W., Vilathgamuwa, D.M., Blaabjerg, F., Loh, P.C.: A robust control scheme for medium-voltage-level DVR implementation. IEEE Trans. Industr. Electron. **54**(4), 2249–2261 (2007)
10. Fitzer, C., Barnes, M., Green, P.: Voltage sag detection technique for a dynamic voltage restorer. In: Industry Applications Conference, 2002. 37th IAS Annual Meeting. Conference Record of the, vol. 2, pp. 917–924, (2002)
11. Kanjiya, P., Singh, B., Jayaprakash, P.: A robust control algorithm for self supported dynamic voltage restorer (DVR). In: India International Conference on Power Electronics 2010 (IICPE2010), pp. 1–8. IEEE (2011)

Performance Comparison of Two Real-Time Power System Frequency Estimation Methods

R.B. Sharma, G.M. Dhole and M.B. Tasare

Abstract A comparative study of two well-known online power system frequency estimation methods is presented in this paper. These methods are least squares error (LES) and least squares new approach (LS). The performance of the frequency estimation methods is tested in laboratory with an Advantech data acquisition system and Matlab tool. The performance of LS online frequency estimation method with and without filtering is examined along with LES method. The experimental results show that the frequency measurement method using LES could be the optimal frequency measurement method, and thus can be applied to frequency measurement apparatus.

Keywords Frequency · Taylor series · Least square · Sample · Sampling rate

1 Introduction

In a power system, frequency is mainly the basic factor for grid monitoring, protection, and control applications. Frequency can represent the dynamic balance of power between generator mechanical input power and load. For this reason, fast

R.B. Sharma (✉)
Government College of Engineering, Chandrapur, Chandrapur, Maharashtra, India
e-mail: adityasharmaji@rediffmail.com

G.M. Dhole
R.H. Sapat College of Engineering, Management Studies and Research, Nasik, Maharashtra, India
e-mail: gm_dhole@gmail.com

M.B. Tasare
Prof. Ram Meghe College of Engineering and Management, Badnera, Maharashtra, India
e-mail: mohantyytasre@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_42

and precise frequency measurement is vitally necessary. Due to deregulated electricity market, the continuous load growth without increase in existing electrical network capacities and increased applications of modern power electronic devices have stressed the power system further. As a result quick and accurate frequency deviation measurement becomes more difficult. Hence, accurate real-time frequency estimator is necessary for power system.

In the last two decades, engineers and researchers have focused their attention on frequency estimation algorithms. Different methodologies based on discrete Fourier transform (DFT) have been proposed for online frequency measurement. Methods [1–3] based on the leakage effect of the DFT and the phasor angle analyses are used for frequency estimation. Most commonly used frequency estimation techniques are the zero-crossing detection and its modifications [4, 5]. The power system frequency estimation techniques based on Kalman filtering (KF) concept has been described in [6–8]. A Wavelet-based algorithm is developed in [9] to obtain real-time power system frequency. With the development of Artificial Intelligence systems, expert systems based on adaptive neural network (ANN) have been employed for online frequency measurement [10, 11]. In [12, 13], the three-phase-locked loop (PLL) method of phase and frequency estimation is proposed. A variety of digital filtering techniques have been proposed during recent years [14–17] for online power system frequency estimation. However, the majority of the above-mentioned techniques have tradeoff between measurement accuracy and execution time.

The work presented in this paper is focused on two real-time frequency estimation techniques [18, 19] implemented in laboratory. In this experimentation Advantech data acquisition system and Matlab is used for on line frequency estimation. The experimental results show that the LES-based technique can be optimal frequency measurement method, and thus can be applied to frequency measurement device such as digital fault recorder. The rest of this paper is structured as follows. At first, in Sect. 2, the frequency measurement methods are briefly described. Section 3 describes hardware structure and software tool used for algorithm testing. Section 4 presents the results obtained. Finally, Sect. 5 summarizes the conclusion reached in this study.

2 Brief Overview of Frequency Estimation Methods

In this section, the theoretical aspects of LES and LS new approach are presented.

2.1 Least Error Square Algorithm

In this subsection, the Taylors series expansion based on LES technique is discussed in brief. Let us consider a voltage signal $v(t)$, which is sampled for measuring real-time frequency that is described by Eq. (1):

$$v(t) = V_m \sin(\omega t + \theta) \tag{1}$$

where V_m is the voltage amplitude, $\omega = 2\pi f$ is the actual frequency, t represents time in seconds, and symbol θ is an arbitrary phase angle. Using the trigonometric identity, $\sin(2\pi ft + \theta)$ Eq. (1) can be expanded using the Taylor series of $\sin(2\pi ft)$ and $\cos(2\pi ft)$ centered on the nominal frequency f_0 as follows:

$$\begin{aligned} v(t) = {} & V_m \cos\theta[\sin(2\pi f_0 t)] + [2\pi t \cos(2\pi f_0 t)](f - f_0)V_m \cos\theta \\ & + [\cos(2\pi f_0 t)]V_m \sin\theta + [-2\pi t \sin(2\pi f_0 t)(f - f_0)V_m \sin\theta] \\ & + \left[t^2 \sin(2\pi f_0 t)\right]\left[\frac{-(2\pi)^2}{2} f^2 + (2\pi)^2 f f_0 - \frac{(2\pi)^2}{2} f_0^2\right] V_m \sin\theta \end{aligned} \tag{2}$$

Consider Eq. (1) is sampled at Δt seconds and set of m samples may be defined as $v(t_1)$, $v(t_2) \ldots v(t_m)$. Equation (2) is given by Eq. (3)

$$\begin{aligned} v(t_1) &= a_{11}x_1 + a_{12}x_2 + a_{13}x_3 + a_{14}x_4 + a_{15}x_5 + a_{16}x_6 \\ v(t_2) &= a_{21}x_1 + a_{22}x_2 + a_{23}x_3 + a_{24}x_4 + a_{25}x_5 + a_{26}x_6 \\ &\vdots \\ v(t_m) &= a_{m1}x_1 + a_{m2}x_2 + a_{m3}x_3 + a_{m4}x_4 + a_{m5}x_5 + a_{m6}x_6 \end{aligned} \tag{3}$$

where $x_1 = V_m \cos\theta$, $x_2 = (f - f_0)V_m \cos\theta$, $x_3 = V_m \sin\theta$,
$x_4 = (f - f_0)V_m \sin\theta$, $a_{i1} = \sin(2\pi f_0 t_i)$, $a_{i2} = 2\pi t_i \cos(2\pi f_0 t_i)$,
$a_{i3} = \cos(2\pi f_0 t_i)$, $a_{i4} = 2\pi t_i \sin(2\pi f_0 t_i)$, $a_{i5} = t_i^2 \sin(2\pi f_0 t_i)$,
$a_{i6} = t_i^2 \cos(2\pi f_0 t_i)$

$v(t_1)$, $v(t_2) \ldots v(t_m)$, are considered inputs, and all a_s can be calculated if the sampling time and nominal frequency f_0 are known. Equation (3) in the matrix form for six unknowns (Xs) can be rewritten as follows:

$$[A][X] = [V] \tag{4}$$

where A is $m \times 6$ matrix and $m \geq 6$, the LES assessment of X is

$$[X] = \left[\left[A^T A\right]^{-1} A^T\right] V \tag{5}$$

where $[A^T A]^{-1} A^T$ is the pseudo-inverse matrix which acts as a filter and amplifies or suppresses noise depending on its coefficients. Using Eq. (5) the frequency deviation $\Delta f = (f - f_0)$ can be estimated as

$$\frac{x_2}{x_1} = \frac{(f - f_0) v_m \cos\theta}{v_m \cos\theta} = f - f_0 \quad \text{OR} \quad \frac{x_4}{x_3} = \frac{(f - f_0) v_m \sin\theta}{v_m \sin\theta} = f - f_0 \tag{6}$$

From this equation the frequency of the sampled signal can be computed as

$$f = f_0 + \frac{x_2}{x_1} \quad \text{OR} \quad f = f_0 + \frac{x_4}{x_3} \tag{7}$$

2.2 Least Squares New Approach Algorithm

This subsection presents the LS new approach based on frequency estimation algorithm for online frequency estimation. Consider a voltage signal of frequency $\omega = 2\pi f$ can be given by Eq. (8)

$$v(t) = V_m \cos(\omega t + \phi_0) \tag{8}$$

where V_m = voltage maximum value and ϕ_0 = initial phase angle. Consider that Eq. (8) is sampled with a sampling frequency *fs* Hz to produce sample $\{v(k)\}$

$$v(k) = V_m \cos(\omega t + \phi_0) \tag{9}$$

Similarly, v_{k-1} and v_{k+1} are represented as follows:

$$\begin{aligned} v(k-1) &= V_m \cos(\omega t_{k-1} + \phi_0) \\ v(k+1) &= V_m \cos(\omega t_{k+1} + \phi_0) \end{aligned} \tag{10}$$

Using trigonometric identities, Eq. (10) can be expanded by Eq. (11):

$$v(k-1) + v(k+1) = 2vk \cos(\omega \Delta t) \tag{11}$$

$$fk = fs/2\pi \cos^{-1}(v(k-1) + v(k+1))/2vk. \tag{12}$$

Now, $\cos(\omega \Delta t)$ can be estimated using the least squares method. One must calculate pseudo-inverse of $v(k)$ Eq. (11). Let G denotes the pseudo-inverse of $v(k)$. Thus

$$G = \left(V_k^T V_k\right)^{-1} V_k^T \tag{13}$$

$$\cos(\omega \Delta t) = V_k^T \left(V_k^- + V_k^+\right) / \left(2 V_k^T V_k\right) \tag{14}$$

Finally, the frequency of the sampled signal is computed using the following formula:

$$f_k = f_s/(2\pi)\cos^{-1}\frac{V_k^T\left(V_k^- + V_k^+\right)}{2V_k^T V_k} \tag{15}$$

3 Laboratory Setup

To assess the performance of LES and LS online frequency estimation techniques, an exhaustive experimentation is carried out on the experimental setup shown in Fig. 1. The setup consists of MS window-based host computer which is facilitated with analog scaling and isolation. The isolation and analog scaling block consists of the gain control circuit and voltage transducer. The microcomputer block consists of Advantech data acquisition system and MSXP-based host computer. The voltage signals are recorded at a sampling rate of 1000, 1200, 2500, and 5000 samples/s.

4 Experimental Results

In this section, practical results of LES and LS new approach for online frequency estimation techniques are presented and discussed.

4.1 Least Error Square Method

The performance of LES algorithm for online frequency measurement is investigated in this subsection section. In order to examine the performance of the discussed algorithm practically, input signals are recorded at sampling rates 1000, 1200, 2500, and 5000 samples/s respectively. While experimenting, the combinations of eight unknowns with the duration of 0.04 s are considered with mentioned sampling rates. Moreover, online frequency estimation is done by varying the number of samples per cycle and the number of Taylor series expansion terms.

Figure 2 depicts the frequency estimates of phase voltage by LES approach. The estimated frequency of a phase voltage by LES method is summarized in Table 1. Comparing to the results sampling rates of 2500 and 5000 samples/s gives better results.

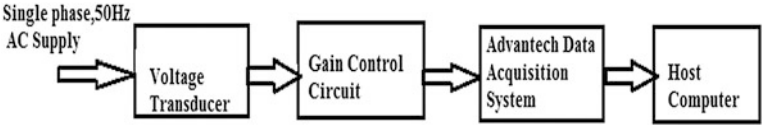


Fig. 1 Experimental setup block diagram

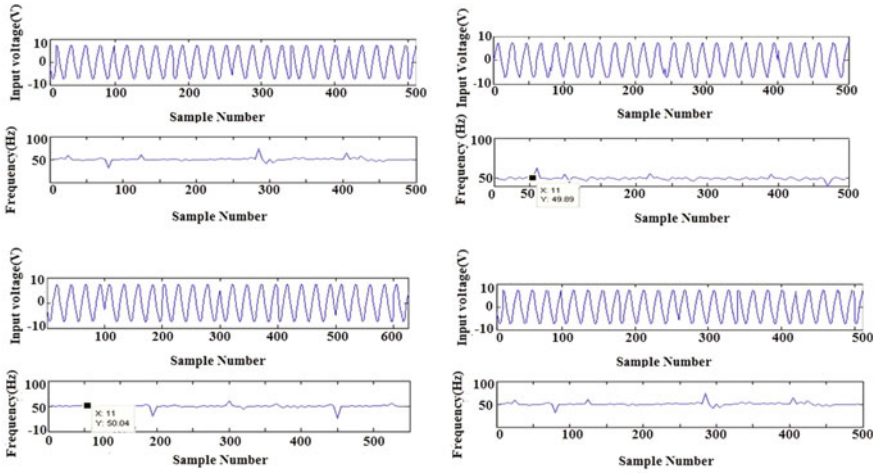


Fig. 2 LES-based real-time estimated frequency

Table 1 Online estimated frequency using LES

No. of unknowns	Sampling frequency (Hz)	Estimated frequency (Hz)		
		Min.	Max.	Avg.
8	1000	39.6	62.5	47.72
8	1200	55.3	61.8	49.51
8	2500	25.6	60.2	49.68
8	5000	31.8	73.8	50.64

4.2 Least Squares New Approach Method

The performance of LS new approach algorithm for online frequency estimation with and without filtering is examined for various sampling frequencies. Test signals are recorded at various sampling rates, such as 1000, 1200, 2500, and 5000 samples/s with data window length of 9. The actual frequency is considered to be 50 Hz.

The estimated frequency response without filtering for LS new method is shown in Fig. 3. The relative frequency estimates with the LS new method without filtering are depicted in Table 2. The obtained result shows the estimated frequency variation in the range of 44.06 to 49.25 Hz for given sampling rates.

Figure 4 depicts the estimated frequency estimation of the LS new algorithm with filter. In this experimentation a data window of 9 samples at sampling rates 1000, 1200, 2500, and 5000 samples/s is used. Table 3 illustrates the relative real-time frequency estimates. It is evident that the estimated frequency with

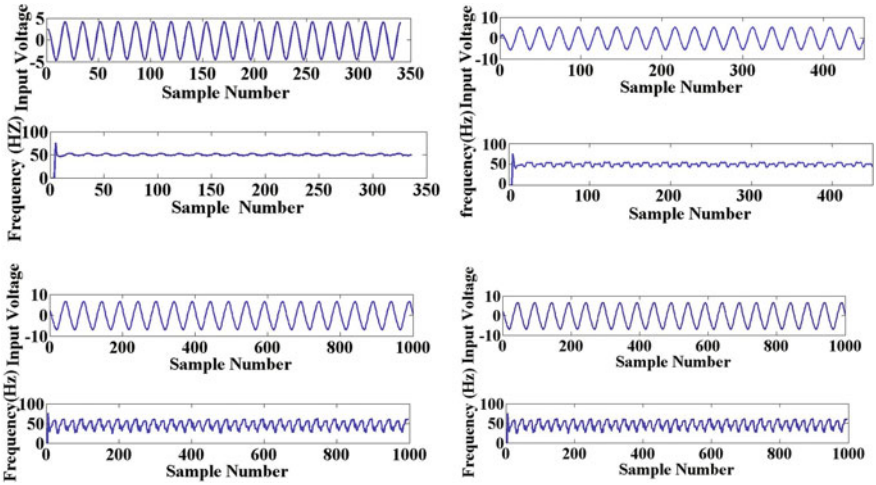


Fig. 3 LS new approach based on real-time estimated frequency without filtering

Table 2 Online estimated frequency using LS new approach without filtering

Sampling frequency (Hz)	Estimated frequency (Hz)		
	Min.	Max.	Avg.
1000	46.60	58.91	49.25
1200	43.82	58.95	48.11
2500	44.27	64.72	44.06
5000	45.93	52.80	44.47

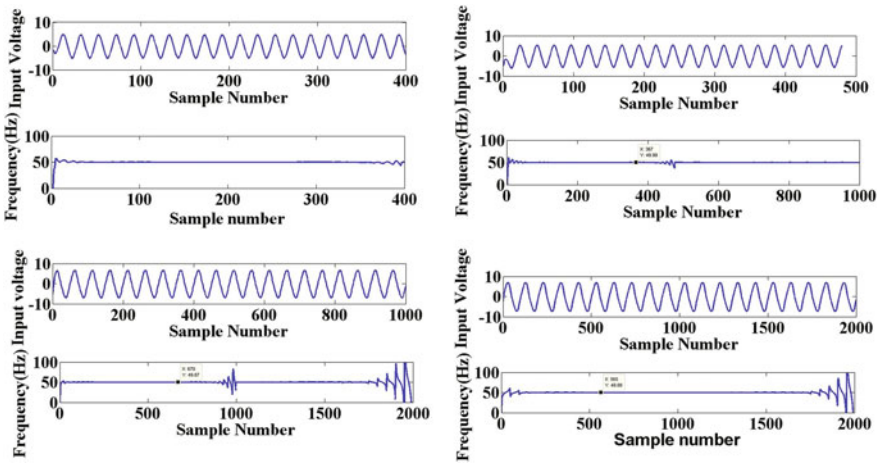


Fig. 4 LS new approach based on real-time estimated frequency with filtering

Table 3 Online estimated frequency using LS new approach with filtering

Sampling frequency (Hz)	Estimated frequency (Hz)		
	Min.	Max.	Avg.
1000	45.93	85.06	48.95
1200	37.28	57.13	49.64
2500	–46.79	131.88	49.62
5000	46.00	58.04	49.42

filtering is varied from 48.95 to 49. 42 Hz. Thus, LS new approach based on real-time estimation of frequency with filtering is a better method than without filtering. However, this is an inefficient method for window size of three samples.

5 Conclusion

In this experimentation, LES and LS algorithms for power system frequency estimation are analyzed and tested, and estimated frequency is presented. The novelty introduction in this work is real-time frequency estimation using LES and LS algorithms. From the experimental results it is evident that LS new approach shows the degraded performance for sampling frequency more than 1200 Hz. However, filtering improves this degradation and hence filtering is must in LS. Moreover, LS seems to be inefficient when window size of three samples is used. In case of LES the pseudo-inverse matrix acts as a filter, which amplifies or suppresses noise depending on its coefficients. Experimentation shows almost stable performance of LES in terms of estimated frequency at higher sampling rates and thus LES could be the optimal frequency measurement method.

References

1. Phadke, A.G., Thorp, J.S., Adamiak, M.G.: A new measurement technique for tracking voltage phasors, local system frequency and rate of change of frequency. IEEE Trans. Power Apparatus. Syst. **PAS-102**, 1025–1038 (1983)
2. Girgis, A.A., Ham, F.M.: A FFT based digital relay for load shedding. IEEE Trans. Power Apparatus Syst. **PAS-101**, 433–439 (1982)
3. Wang, M., Sun, Y.: A practical, precise method for frequency tracking and phasor estimation. IEEE Trans. on Power Delivery **19**(4), 1547–1552 (2004)
4. Terzija, V., Djuric, M., Kovacevic, B.: A new self tuning algorithm for the frequency estimation of distorted signals. IEEE Trans. Power Delivery **10**(4), 1779–1785 (1995)
5. Nguyen, C.T., Srinivasan, K.: A new technique for rapid tracking of frequency deviations based on level crossings. IEEE Trans. Power Apparatus Syst. **103**(8), 2230–2236 (1984)
6. Routray, Y., Pradhan, A.K., Rao, K.P.: A novel Kalman filter for frequency estimation of distorted signals in power systems. IEEE Trans. Instrum. Meas. **51**, 469–479 (2002)

7. Girgis, A.A., Hwang, T.L.D.: Optimal estimation of voltage phasors and frequency deviation using linear and nonlinear Kalman filtering. IEEE Trans. Power Apparatus. Syst. **PAS-103**, 2943–2949 (1984)
8. Dash, P.K., Pradhan, A.K., Panda, G.: Frequency estimation of distorted power system signals using extended complex Kalman filter. IEEE Trans. Power Delivery **14**, 761–766 (1999)
9. Lin, T., Tsuji, M., Yamada, E.: Wavelet approach to real time estimation of power system frequency. SICE 2001, Tokyo, Japan (2001)
10. Lai, L.L., Chan, W.L., Tse, C.T.: Real-time frequency and harmonic evaluation using artificial neural networks. IEEE Trans. Power Delivery **14**, 52–59 (1999)
11. Dash, P.K., Swain, D.P., Routray, A., Liew, A.C.: An adaptive neural network approach for the estimation of power system frequency. Elect. Power Syst. Res. **41**, 203–210 (1997)
12. Karimi-Ghartemani, M., Bakhshai, A.: Application of enhanced phase locked loop system to the computation of synchrophasors. IEEE Trans. Power Delivery **26**(1), 22–32 (2011)
13. Mojiri, M., Karimi-Ghartemani, M., Bakhshai, A.: Estimation of power system frequency using an adaptive notch filters. IEEE Trans. Instrum. Meas. **56**(6), 2470–2477 (2007)
14. Kusljevic, M.D.: Simultaneous frequency and harmonic magnitude estimation using decoupled modules and multirate sampling. IEEE Trans. Instrum. Meas. **59**(4), 954–962 (2011)
15. Xia, Y., Mandic, D.P.: Widely linear adaptive frequency estimation of unbalanced three-phase power systems. IEEE Trans. Instrum. Meas. **61**(1), 74–83 (2012)
16. Kamwa, I., Samantaray, S.R., Joos, G.: Wide frequency rage adaptive phasor and frequency PMU algorithms. IEEE Trans. Smart. Grid **5**(2), 569–579 (2014)
17. He, Z., Fu, L., Han, W., Mai, R., Dong, Z.U.: Precise algorithms for frequency estimation under dynamic and step change conditions. IET Sci. Meas. Tech. **9**(7), 842–851 (2015)
18. Sachdev, M.S., Giray, M.M.: A least square technique for determining power system frequency. IEEE Trans. Power Apparatus. Syst. **PAS-104**, 437–443 (1985)
19. Abdollahi, A., Matinfar, F.: Frequency estimation: a least squares new approach. IEEE Trans. Power Delivery **26**(2), 790–798 (2011)

Brushless DC Electric Motor Speed Control and Power Factor Correction Using Single-Ended Primary Inductor Converter

Shaw Bikash, Sengupta Anwesha, S.B. Mahajan, Padmanaban Sanjeevikumar and Shaikh Aamer

Abstract In this treatise, Brushless DC electric motor (BLDC electric motor), Power Factor Correction (PFC), and control of speed using Single-Ended Primary Inductor Converter (SEPIC) are articulated. An original approach is proposed for the controlling of motor speed and PFC using SEPIC and managing the DC link voltages and also it provides a viable solution for driving applications. At AC mains, inherent power factor correction is achieved for speed control in wide range using SEPIC in discontinuous mode. The system is simulated in MATLAB and a result confirms the validity and feasibility.

Keywords BLDC electric motor · SEPIC · Speed control · Power factor correction · Discontinuous inductor current mode

S. Bikash (✉)
Department of Power Electronics & Drive, SRM University, Chennai, India
e-mail: shaw.bikash10@gmail.com

S. Anwesha
Department of Electrical Engineering, DIT, Kolkata, India
e-mail: anwesha142@gmail.com

S.B. Mahajan · S. Aamer
Department of Electrical and Electronics Engineering, MIT, Aurangabad, India
e-mail: sagar25.mahajan@gmail.com

S. Aamer
e-mail: aamer32shaikh@gmail.com

P. Sanjeevikumar
Department of Electrical and Electronics Engineering, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_43

1 Introduction

The brushless direct current (BLDC) motor is becoming very popular because of striking features such as EMI (Electromagnetic Interference) problems, less maintenance, superior efficiency, and flux density [1–4]. BLDC motors are not only limited to the domestic applications, but also suitable for Aero-modeling and industrial applications such as motion control, actuation systems, positioning systems, High voltage AC (HVAC), ventilation, and medical and transportation systems [1–4].

According to load requirement, many converters are employed to step-down or step-up the voltage level [5–7]. In few applications, buck–boost converter provides a solution to increase or decrease the voltage where load voltage requirement is in the range of supply voltage. Single inductor, capacitor, diode, and power switch are required to design a traditional buck–boost converter [1]. However, high ripples are experienced in input current of converter. Highly capacitive or LC filter necessitates for suppress the cause of ripple but makes the buck–boost converter expensive.

Brushless DC motor drive using buck–boost converter is proposed to control the speed and block diagram as shown in Fig. 1 [1]. At AC mains inherent PFC is achieved by operating buck–boost converter in discontinuous mode. Figure 2 depicts circuit diagram of brushless DC motor drive using buck–boost converter.

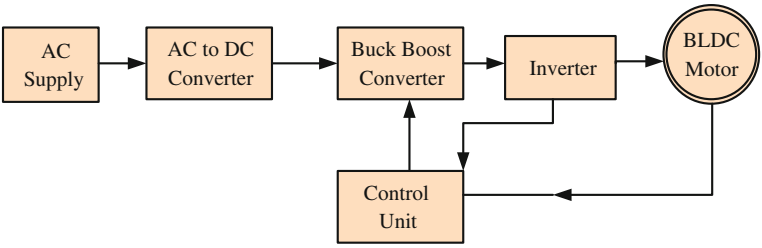


Fig. 1 Block diagram of brushless DC motor drive using buck–boost converter

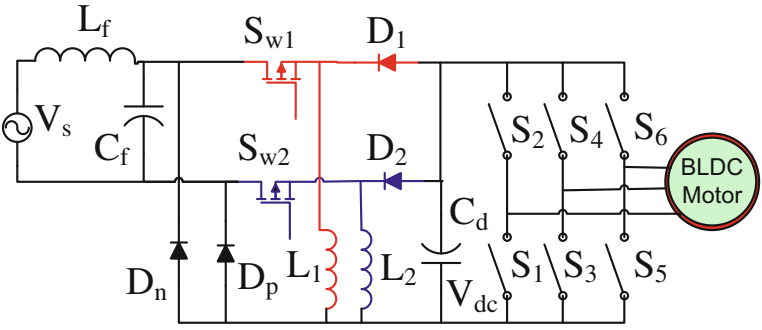


Fig. 2 Circuit diagram of brushless DC motor drive using buck–boost converter

An inverting output voltage is obtained through buck–boost converter and fed to the inverter for motor control application. The control unit is employed to control and maintain the switching signal of the system. It senses the speed change of BLDC motor. Inverter input side DC link voltage is managed using converter to control the speed of BLDC motor. DC link capacitor Cd is energized in positive half cycle of input supply using power switch Sw_1, inductor L_1, and diodes D_P, D_1. Similarly, DC link capacitor Cd is energized in negative half cycle of input supply using power switch Sw_2, inductor L_2, and diodes D_n, D_2. Cuk rectifier is operated in discontinuous mode to achieve maximum power factor with minimal input current THD [8]. In [9] Single-Sided Matrix Converter (SSMC) for BLDC, electric drive is proposed for aerospace application.

2 Proposed BLDC Motor Drive Control Using SEPIC

SEPIC is employed in the proposed BLDC motor control to maintain the DC link voltage. For the efficient control of motor, high and low frequencies are used to switching the power switch of the SEPIC and inverter, respectively. High-frequency MOSFET is used in SEPIC, whereas in low-frequency inverter, IGBT is used for proposed BLDC motor drive control (Fig. 3).

The ac supply voltage is given to the rectifier circuit and output of the rectifier is supplied to the SEPIC. The function of control unit is to control the duty cycle of SEPIC converter according to BLDC drive requirement. Driver circuit is also used for isolation purpose and to drive the switches of converter. The SEPIC is synonymous to a traditional buck–boost converter but it generates non-inverted step-down or step-up output voltage (the output has the same voltage polarity as the input) using two-inductor and single-intermediate capacitor. Figure 4 depicts the power circuit of proposed brushless DC motor drive using SEPIC. The operation of proposed SEPIC is essentially divided in two modes—one when switch S_{W1} is ON and OFF (positive cycle of input) and another when switch S_{W2} is ON and OFF (Negative cycle of input). Switches Sw1 and Sw2 are operated in positive and negative cycles, respectively.

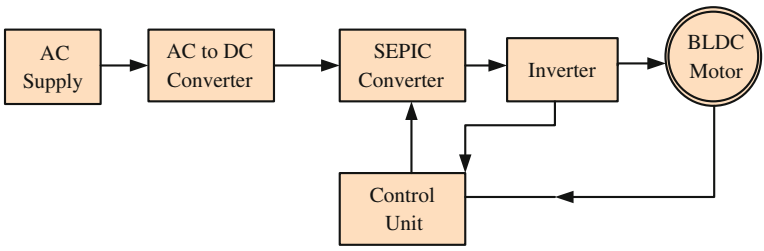


Fig. 3 Proposed block diagram of brushless DC motor drive using SEPIC

In positive cycle of input supply Sw1 is turned ON and Sw2 is fully turned OFF. Inductor L_1 is charged from the supply voltage through diode Dp and simultaneously capacitor C_1 provides energy to inductor L_3. When switch Sw1 is turned OFF, inductor L_1 and supply voltage provides energy to load. Capacitor C1 is charged by supply voltage and inductor L_1. Inductor L_3 also delivers its energy to capacitors C_d of DC link through diode D_1. The stored energy of the capacitor C_d is transferred to BLDC motor through inverter. The equivalent circuit when switch Sw1 is turned ON and turned OFF is shown in Figs. 5 and 6 respectively.

In negative cycle of input, supply S_{w2} is turned ON and S_{w1} is fully turned OFF. Inductor L_2 is charged from the supply voltage through diode Dn and simultaneously capacitor C_2 provides energy to inductor L_3. When switch Sw2 is turned OFF, inductor L_2 and supply voltage provide energy to load. Capacitor C_2 is charged by supply voltage and energy stored in the inductor L_2. Inductor L_3 also delivers its energy to capacitor C_d of DC link through diode D_1. The stored energy of the capacitor C_d is transferred to BLDC motor through inverter. The equivalent circuit when switch S_{W2} is turned ON and turned OFF is shown in Figs. 7 and 8, respectively.

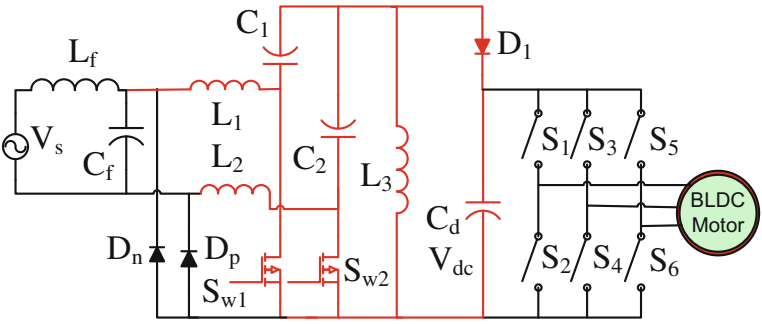


Fig. 4 Power circuit of proposed brushless DC motor drive using SEPIC

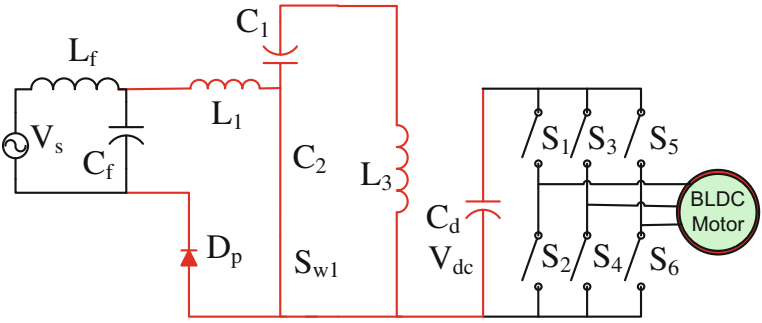


Fig. 5 Proposed drive system equivalent circuit (when switch S_{W1} is ON)

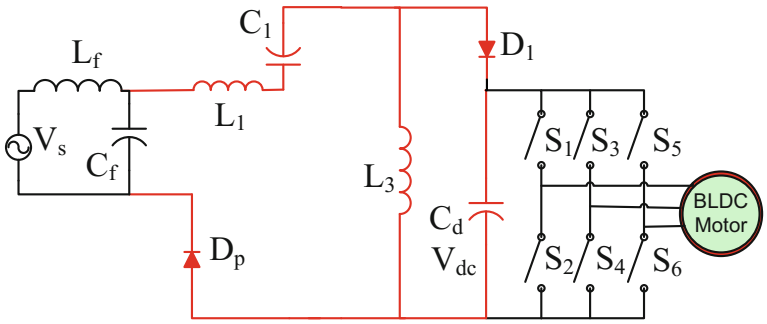


Fig. 6 Proposed SEPIC converter-fed BLDC motor drive equivalent circuit (when switch S_{W1} is turned OFF in positive cycle of input)

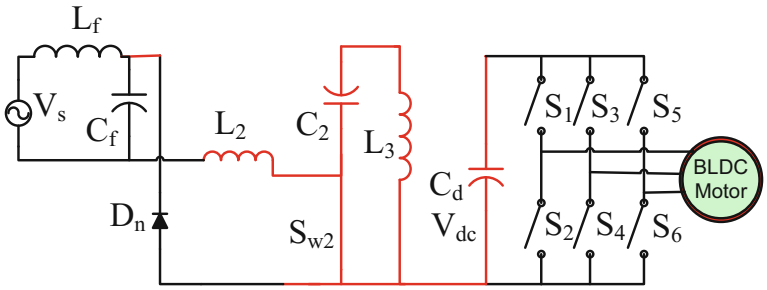


Fig. 7 Proposed drive system equivalent circuit (when switch S_{W2} is ON)

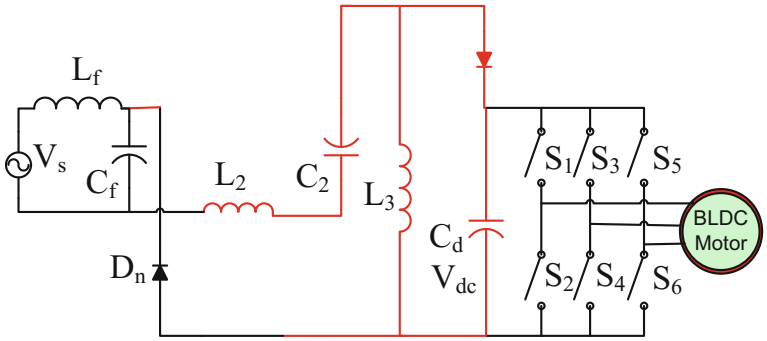


Fig. 8 Proposed drive system equivalent circuit (when switch S_{W2} is OFF)

3 Simulation Results

The proposed SEPIC-based BLDC drive motor drive system is simulated in MATLAB to verify the functionality of system. To achieve efficient speed control of BLDC motor for wide range DC link voltage varies with references. Proposed system DC voltage is varied with the reference voltage to achieve a wide variation and control over the BLDC motor. SEPIC converter is operated in discontinuous mode to provide input for the inverter. 700 μH inductors (L_1, L_2 and L_3) and 220 μf capacitors (C_1, C_2 and C_d) are used to design the proposed converter. The speed versus time graph for DC Link voltage 97 V is shown in Fig. 9.

It is observed that approximately 1000 rpm speed is achieved at DC link voltage 97 V. The graph of DC link voltage to achieve 1000 rpm is shown in Fig. 10. The speed versus time graph for DC link voltage 120 V is shown in Fig. 11. It is observed that 1189 rpm speed is achieved at DC link voltage 120 V. The graph of DC link voltage to achieve 11,189 rpm is shown in Fig. 12. It is observed that 0.956 power factor is achieved at DC link voltage 120 V and 0.999 power factors is achieved at DC link voltage 199.6 V. Figure 13 depicts power factor of proposed system which is achieved at 200 V. The result of proposed system is summarized in Table 1.

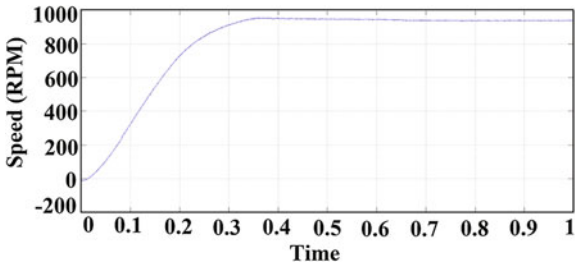


Fig. 9 Speed versus time graph of proposed system for DC link voltage 97 V

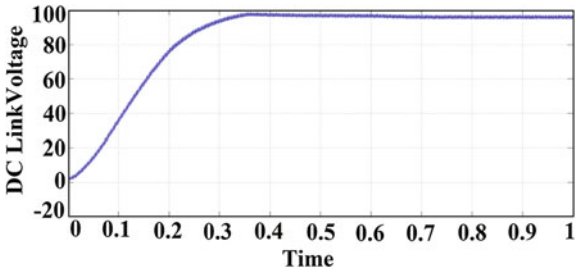


Fig. 10 DC link voltage at the output of SEPIC to achieve speed 1000 rpm

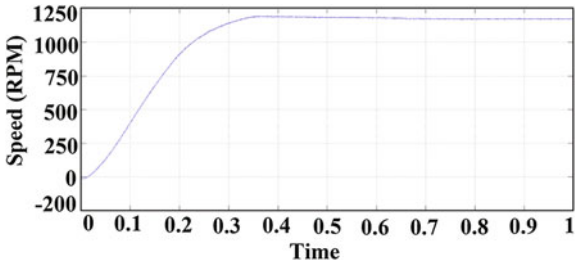


Fig. 11 Speed versus time graph of proposed system for DC link voltage 120 V

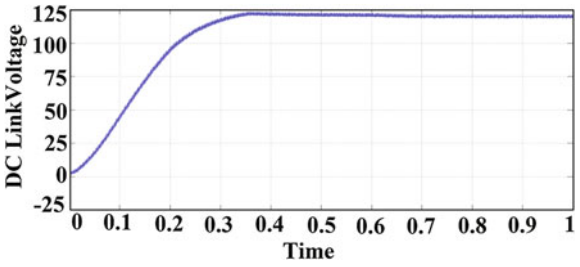


Fig. 12 DC link voltage at the output of SEPIC to achieve speed 1189 rpm

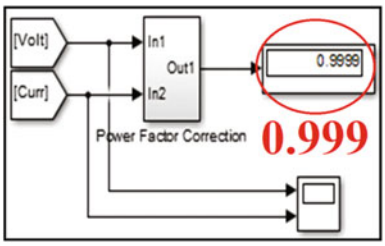


Fig. 13 Power factor of proposed system at 200 V (1949 rpm)

Table 1 Simulation results of proposed converter

Parameters	Values					
Vdc (V)	39.24	59.11	98.9	120	158	199.6
Speed (rpm)	358	575	982	1189	1550	1949
Power factor (PF)	0.908	0.918	0.935	0.956	0.972	0.999

4 Conclusions

Speed control and Power Factor Correction (PFC) of brushless DC electric motor (BLDC electric motor) is proposed using SEPIC and proposed system provides a practicable solution for drive application. Voltage source inverter (VSI) with three

phases is employed as an electronic commutated switch for BLDC electric motor. At the AC mains maximum power factor is achieved with the variation of the DC link voltage of SEPIC. The DC link SEPIC voltage is varied by setting a corresponding constant value of a reference voltage to get control over the BLDC motor. The proposed drive system is simulated in MATLAB and a result confirms the validity and feasibility.

References

1. Vashist, B., Singh, B.: An adjustable speed PFC bridgeless buck-boost converter fed BLDC motor drives. IEEE Tran. Ind. Electron. **61**(6), (2014)
2. Gieras, J.F., Wing, M.: Permanent Magnet Motor Technology-Design and Application. Marcel Dekker, New york (2002)
3. Puttaswamy, C.L., Singh, B., Singh, B.P.: Investigation on dynamic behavior of permanent magnet brushless DC motor drives. Electric Mach. Power Syst. **23**(6), (1995)
4. Singh, S., Singh, B.: Single-phase SEPIC based PFC converter for PMBLDCM drive in air-conditioning system. Asian Power Electron. J. **4**(1), (2010)
5. Mahajan, S.B., Pandav, K.M., Draxe, K.P.: Novel topological derivations for DC–DC converters. Int. J. Comput. Eng. Manage. **16**(6), (2013)
6. Mahajan, S.B., Nandyala, S.R., Repalle, K.P.: A novel SEPIC based dual output DC–DC converter for solar applications. In: IEEE International Conference 2014 Power and Energy Systems: Towards Sustainable Energy (2014)
7. Bhaskar, M.S., Kulkarni, R.M., Padmanaban, S., Siano, P., Blaabjerg, F.: Hybrid non-isolated and non inverting Nx interleaved DC–DC multilevel boost converter for renewable energy applications. In: IEEE International Conference on Environment and Electrical Engineering, Italy (2016)
8. Fardoun, A.A., Ismail, E.H., Sabzail, A.J., Al-saffar, M.A.: New efficient bridgeless Cuk rectifier for PFC applications. IEEE Trans. Power Electron. **27**(7), (2012)
9. Huang, X., Goodman, A., Gerada, C., Fang, Y., Lu, Q.: A single sided matrix converter drives for a brushless DC motor in aerospace applications. IEEE Trans. Ind. Electron. **59**(9), (2012)

Naturally Clamped, Isolated, High-Gain DC–DC Converter with Voltage Doubler for Battery Charging of EVs and PHEVs

Abhinav Bhattacharjee, Sangit Saha, D. Elangovan and G. Arunkumar

Abstract Plug-in hybrid electric vehicles (PHEVs) have a conventional internal combustion (IC) engine running on fossil fuels as well as an electric motor that gets supply from a battery which can be charged using external supply like electric vehicles (EVs). Using renewable energy sources like fuel cells or solar photovoltaics (PVs) for charging the battery, EVs and PHEVs can become even cleaner as far as the environment is concerned. These energy sources generate a low voltage which is limited to around 40–50 V due to practical constraints, while batteries that power EVs and PHEVs need a charging voltage of around 350 V. This paper presents a novel naturally clamped, isolated, DC–DC converter which has a voltage doubler rectifier at the output end which converts 12 V supply from renewable sources to 350 V to enable battery charging.

Keywords EV · PHEV · Battery charging · DC–DC · Electric vehicles Naturally clamped · Voltage doubler · ZCS · ZVS

A. Bhattacharjee (✉) · S. Saha
Power Electronics & Drives, VIT University, Vellore, Tamil Nadu, India
e-mail: abhinav.joydeep2015@vit.ac.in

S. Saha
e-mail: sangit.saha2015@vit.ac.in

D. Elangovan · G. Arunkumar
Department of Energy and Power Electronics, SELECT, VIT University, Vellore, Tamil Nadu, India
e-mail: elangovan.devaraj@vit.ac.in

G. Arunkumar
e-mail: g.arunkumar@vit.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_44

1 Introduction

Each fuel cell or solar PV cell can produce about 1 V and by connecting many such cell stacks in series and parallel, it is possible to realize the required voltage and current rating for the system [1]. Practically, it is not easy to connect a huge number of cells in series and as a result the voltage that can be obtained from these sources is limited to around 40–50 V max. We need to use a DC–DC boost converter to boost this voltage to the required value as per the application. Batteries for electric vehicles need a charging voltage of around 350 V. This necessitates that a high-gain DC–DC converter be used to make battery charging for PHEVs from renewable energy sources possible. This paper discusses simulation as well as a reduced power hardware model of the proposed converter for battery charging application. Various converters have been proposed for this application. A number of non-isolated high step-up DC–DC converters are reviewed in [2–4] review cascaded boost converters and switched capacitor converters, respectively. Boost converters using coupled inductor concept are shown in [5]. A combination of the above two concepts is shown in [6].

The voltage output from renewable sources is considered to be a modest 12 V, which is then boosted to 350 V using the proposed converter. The converter needs to have low losses. Switching losses cause most of the loss in the converter [7], and therefore techniques like soft switching can be implemented to reduce the switching losses. The proposed converter uses a naturally clamped topology. Isolation of the output and the input sides is achieved using a transformer which also provides boost action using a 1:5 turns ratio. The output features a voltage doubler rectifier. In Fig. 1, a schematic of the proposed converter is shown.

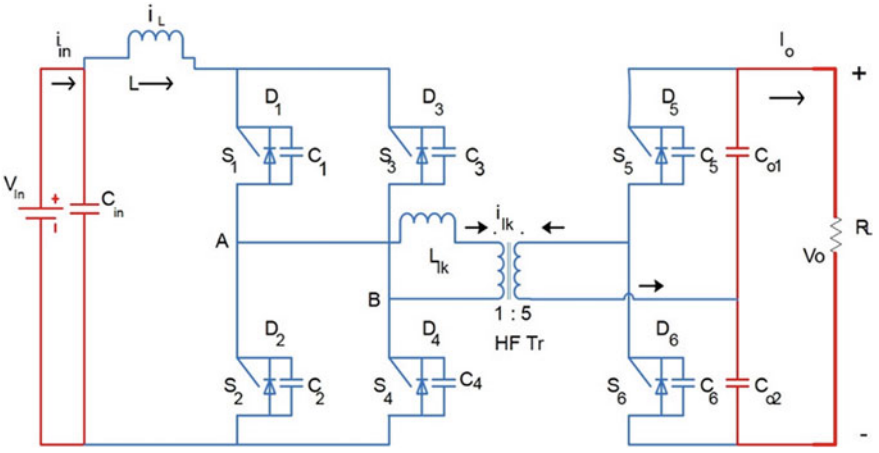


Fig. 1 Schematic of the proposed converter

2 Steady-State Analysis and Design of the Converter

The operation of the converter can be studied by doing mode-wise study of its operating stages. There are a total of eight modes which are described below. The conduction paths for all the modes are illustrated in Fig. 2.

Mode 1 ($t_o < t < t_1$): In this mode, switches S2 and S3 are conducting. On the output side, capacitor C_{O2} gets charged as both the switches are off and current flows through diode D_6.

Mode 2 ($t_1 < t < t_2$): During Mode 2, switches S2 and S3 are still conducting. Just before switches S1 and S4 start conducting, capacitors C1 and C4 connected across switches S1 and S4 discharge for some time.

Mode 3 ($t_2 < t < t_3$): The switches at the input side are simultaneously conducting here. Since the output voltage $v_o/2_n$ falls on the leakage inductance L_{lk}, current from switches S2 and S3 is diverted to switches S1 and S4. The currents flowing through the various components in this time duration are given in Eqs. (1), (2), (3), and (4):

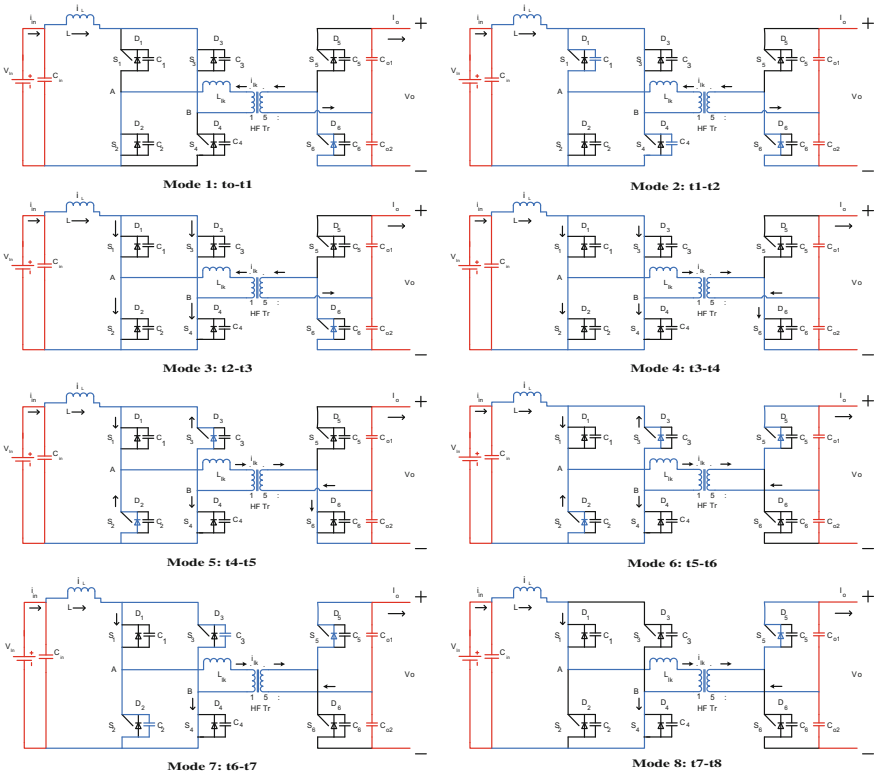


Fig. 2 Modes of operation of the converter

$$I_{\mathrm{lk}} = -I_{\mathrm{in}} + \frac{v_o}{2n * L_{\mathrm{lk}}}(t - t2) \tag{1}$$

$$I_{\mathrm{s1}} = I_{\mathrm{s4}} = \frac{v_o}{4n * L_{\mathrm{lk}}}(t - t2) \tag{2}$$

$$I_{\mathrm{s2}} = I_{\mathrm{s3}} = I_{\mathrm{in}} - \frac{v_o}{4n * L_{\mathrm{lk}}}(t - t2) \tag{3}$$

$$I_{\mathrm{D6}} = \frac{I_{\mathrm{in}}}{n} - \frac{v_o}{2n^2 * L_{\mathrm{lk}}}(t - t2). \tag{4}$$

Since diode D6 is conducting and it is anti-parallel to switch S6, S6 turns on with zero voltage switching. When this mode ends, diode D6 will turn off naturally. The final values of the currents through all the components by the end of the mode are given in Eq. (5):

$$I_{\mathrm{lk}} = 0, I_{\mathrm{S1}} = I_{\mathrm{S2}} = I_{\mathrm{S3}} = I_{\mathrm{S4}} = I_{\mathrm{in}}/2, I_{\mathrm{D6}} = 0. \tag{5}$$

Mode 4 ($t_3 < t < t_4$): In continuation with Mode 3, the current in switches S2 and S3 will keep decreasing till it reaches zero and the switches are naturally commutated. While on the output side switch S6 starts to conduct with zero voltage switching (ZVS). The currents through all the components in this mode are given by Eq. (6):

$$I_{\mathrm{S1}} = I_{\mathrm{S4}} = I_{\mathrm{lk}} = I_{\mathrm{in}}, I_{\mathrm{S2}} = I_{\mathrm{S3}} = 0, I_{\mathrm{S6}} = I_{\mathrm{in}}/n. \tag{6}$$

Mode 5 ($t_4 < t < t_5$): As a confirmation that zero current switching (ZCS) has taken place in switches S2 and S3, the diodes D2 and D3 start to conduct. Current through leakage inductance L_{lk} starts to rise linearly and the current through switches S1 and S4 reaches max value. The currents through the various components in this mode are given in Eqs. (7), (8), (9), and (10):

$$I_{\mathrm{lk}} = I_{\mathrm{in}} + \frac{v_o}{2n * L_{\mathrm{lk}}}(t - t4) \tag{7}$$

$$I_{\mathrm{s1}} = I_{\mathrm{s4}} = I_{\mathrm{in}} + \frac{v_o}{4n * L_{\mathrm{lk}}}(t - t4) \tag{8}$$

$$I_{\mathrm{D2}} = I_{\mathrm{D3}} = \frac{v_o}{4n * L_{\mathrm{lk}}}(t - t4) \tag{9}$$

$$I_{\mathrm{S6}} = \frac{I_{\mathrm{in}}}{n} + \frac{v_o}{2n^2 * L_{\mathrm{lk}}}(t - t4). \tag{10}$$

Mode 6 ($t_5 < t < t_6$): Here, switch S6 on the output side is turned off and diode D5 starts to conduct, thereby charging capacitor C_{O1}. On the input side, switches S2 and S3 are off while S1 and S4 conduct. The currents through all the components in this mode are given in Eqs. (11), (12), (13), and (14):

$$I_{\mathrm{lk}} = I_{\mathrm{lk\,peak}} - \frac{v_o}{2n * L_{\mathrm{lk}}}(t - t5) \tag{11}$$

$$I_{\mathrm{s1}} = I_{\mathrm{s4}} = I_{\mathrm{sw\,peak}} - \frac{v_o}{4n * L_{\mathrm{lk}}}(t - t5) \tag{12}$$

$$I_{\mathrm{D2}} = I_{\mathrm{D3}} = I_{\mathrm{D2\,peak}} - \frac{v_o}{4n * L_{\mathrm{lk}}}(t - t5) \tag{13}$$

$$I_{\mathrm{D5}} = \frac{I_{\mathrm{lkpeak}}}{n} - \frac{v_o}{2n^2 * L_{\mathrm{lk}}}(t - t5). \tag{14}$$

Currents through diodes D2 and D3 become zero by the end of this mode and current through switches S1 and S4, and the transformer reach their peak value. The currents through all the components at the end of the mode are given in (15):

$$I_{\mathrm{S1}} = I_{\mathrm{S4}} = I_{\mathrm{lk}} = I_{\mathrm{in}}, I_{\mathrm{D2}} = I_{\mathrm{D3}} = 0, I_{\mathrm{D5}} = I_{\mathrm{in}}/n. \tag{15}$$

Mode 7 ($t_6 < t < t_7$): Capacitors C2 and C3 charge to maximum value $v_o/2_n$ while switches S2 and S3 gain forward blocking capacity. The output side is similar to Mode 6.

Mode 8 ($t_7 < t < t_8$): Switches S1 and S4 conduct and maximum input current flows through them constantly. The output side is again similar to Mode 6 with diode D5 conducting and charging capacitor C_{O1}. Current through diode D5 depends on the turns ratio and is given as I_{in}/n. The voltage and current values at the end of the mode are given by Eq. (16):

$$I_{\mathrm{S1}} = I_{\mathrm{S4}} = I_{\mathrm{lk}} = I_{\mathrm{in}}, I_{\mathrm{S2}} = I_{\mathrm{S3}} = 0, I_{\mathrm{D5}} = I_{\mathrm{in}}/n, V_{\mathrm{S2}} = V_{\mathrm{S3}} = v_o/2_n. \tag{16}$$

3 Design of the Converter

The output voltage is given by Eq. (17):

$$V_o = \frac{n * V_{\mathrm{in}}}{1 - d}, \tag{17}$$

where

n Turns ratio of the transformer and
d Duty cycle

To meet the given specifications, the input side switches need a duty cycle of 80% while the output side switches have a duty cycle of 15%.

The input inductor value is provided by the formula mentioned in (18):

$$L = \frac{V_{\text{in}} * (d - 0.5)}{\Delta I_{\text{in}} * f_s}, \tag{18}$$

where

L Inductance value,
V_{in} Input voltage,
f_s Switching frequency
ΔI_{in} Current ripple in the inductor which is assumed as 1 A

Leakage inductance value of transformer is given by Eq. (19):

$$L_{\text{lk}} = \frac{V_o * (d - 0.5)}{4 * n * I_{\text{in}} * f_s}, \tag{19}$$

where

L_{lk} Leakage inductance
V_{o} Output voltage
f_s Switching frequency
I_{in} Average input current

Average value of input current can be found using Eq. (20):

$$I_{\text{in}} = \frac{P_o}{\alpha V_{\text{in}}}, \tag{20}$$

where α—efficiency, assumed as 95%.

The transformer turns ratio needs to be 1:5 to generate the required output voltage. Using the above designed values, we can achieve ZCS on the input side and ZVS on the output side.

4 Simulation Results

The simulation has been done using P-Sim software. Pulses for switches S1 and S4 are same and for switches S2 and S3 are same. It can be seen that both sets of switches have 80% duty cycle. Switching pulses for the output side switches S5 and

S6 are also shown for 15% duty cycle. Figure 3 shows the current through the input side switches along with the switching pulses of both the sets of switches for comparison.

Figure 4 shows the current and voltage of the output side switches along with the switch pulse. Figure 5 shows the input current and voltage waveforms during steady-state operation of the converter, while Fig. 6 shows the output current and voltage waveforms during steady state.

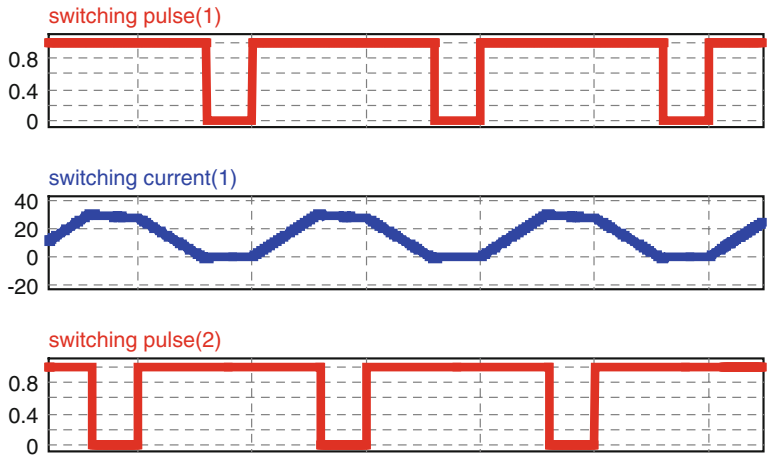


Fig. 3 Input side switch current with switching pulse

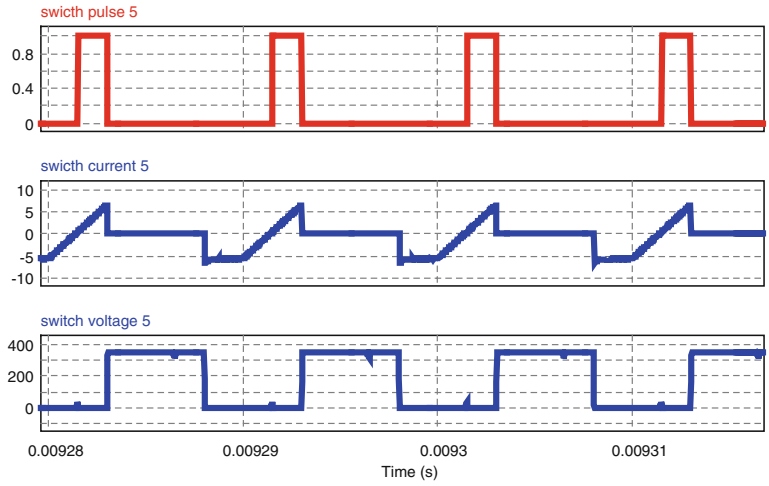


Fig. 4 Output side switch current and voltage along with switching pulse

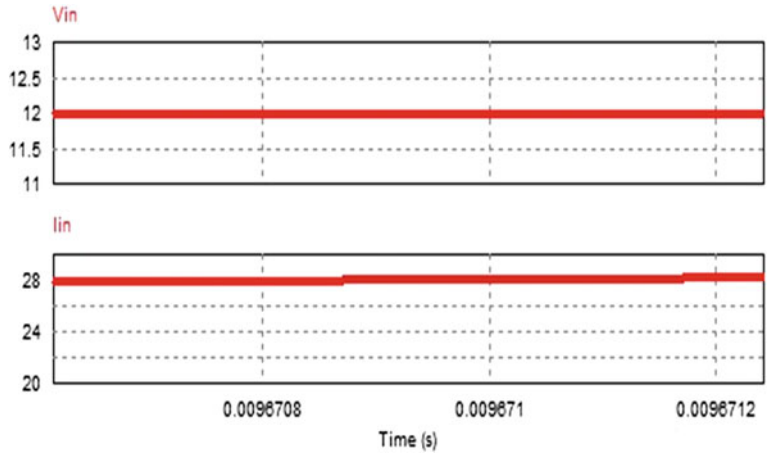


Fig. 5 Input voltage and current waveforms

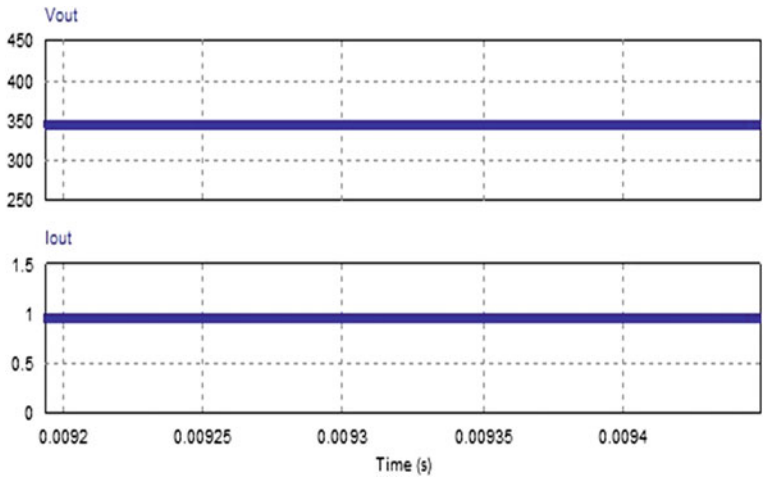


Fig. 6 Output voltage and current waveforms

5 Hardware Implementation

Hardware implementation of the proposed converter was done for a power level of 200 W. dSpace was used to generate the switching pulses. The pulses were fed to the switches via a driver board which provided isolation with the help of opto-couplers. Table 1 shows the various components used in the hardware implementation and their values.

Table 1 Parameters for hardware implementation

Components	Values/Part number	Components	Values
Switches	P55nf06	Leakage inductor	1.7 μH
Load	200 W	Input capacitor	20 μF
Transformer turns ratio	1:5	Output capacitor	20 μF
Boost inductor	1000 μH	Frequency	100 kHz

Fig. 7 Hardware setup

Figure 7 shows the complete hardware setup in the lab. Switching pulses are designed using Simulink on the computer which is interfaced with the dSpace unit. Input to the converter is provided using a programmable power supply which can simulate variations in supply and all other real-time situations. Measurements for voltage and current are done using probes and the output is viewed on a digital storage oscilloscope. A set of bulbs is used as load.

Figure 8 shows the screenshots from the digital storage oscilloscope showing the switching pulses as generated by the dSpace unit and Fig. 9 shows the switching pulses as obtained at the output of the driver board.

Screenshots from the digital storage oscilloscope showing the input current, voltage, and output voltage in steady state are shown in Fig. 10. The output voltage is 350 V and the input voltage is 12 V.

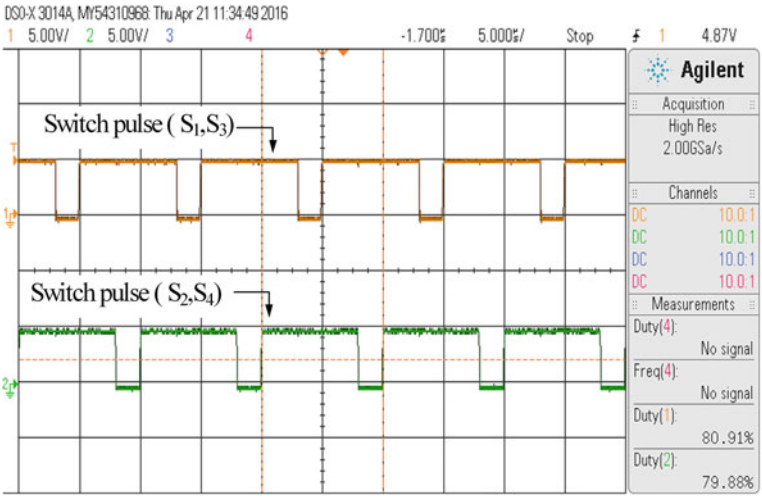


Fig. 8 Switching pulses obtained from dSpace unit

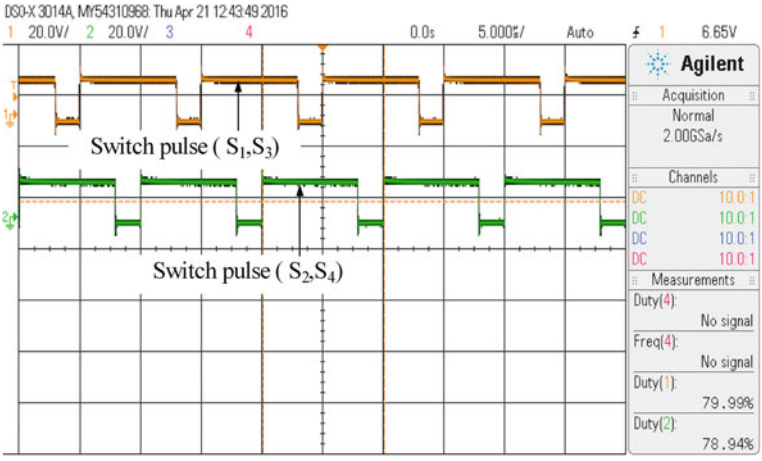


Fig. 9 Switching pulses obtained from the driver board

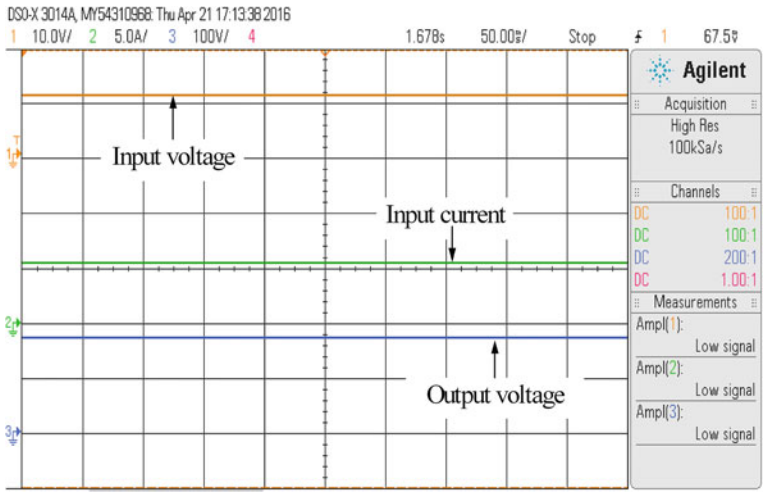


Fig. 10 Steady-state input voltage, input current, and output voltage

6 Conclusion

The proposed converter was simulated using P-Sim software as per the designed specifications and a hardware model was also developed to iron out any problems that might occur in real-time operation. ZCS was obtained on the input side and ZVS was obtained on the output side. This helped tremendously to reduce the switching losses and improve efficiency. It was also seen that ZCS and ZVS are more effective at reducing switching losses than passive snubber circuits and using active clamps because the former uses less components and is also more efficient. Using this converter, integration of renewable energy sources like fuel cells and solar PVs into day-to-day activities will be easier. The converter also has other versatile uses as it can be connected to a DC grid for micro-grid and smart grid applications.

References

1. Larminie, J.E., Dicks, A.: Fuel Cell Systems Explained. Wiley, New York (2002)
2. Li, W., He, X.: Review of non-isolated high-step-up DC/DC converter in photovoltaic grid-connected application. IEEE Trans. Ind. Electron. **58**(4), 1239–1250 (2011)
3. Feng, X.G., Liu, J.J., Lee, F.C.: Impedance specifications for stable dc distributed power systems. IEEE Trans. Power Electron. **17**(2), 157–162 (2002)
4. Chung, H.S., Ioinovici, A., Cheung, W.L.: Generalized structure of bi-directional switched-capacitor DC/DC converters. IEEE Trans. Circuits Syst. I, Fundam. Theor. Appl. **50**, 743–753 (2003)

5. Inaba, C.Y., Konishi, Y., Nakaoka, M.: High frequency PWM controlled step-up chopper type DC–DC power converters with reduced peak switch voltage stress. Proc. Inst. Elect. Eng. Elect. Power Appl. **151**(1), 47–52 (2004)
6. Wai, R.J., Duan, R.Y.: High-efficiency bidirectional converter for power sources with great voltage diversity. IEEE Trans. Power Electron. **22**(5), 1986–1996 (2007)
7. Chen, S.M., Liang, T.J., Yang, L.S., Chen, J.F.: A safety enhanced high step up DC–DC converter for AC photovoltaic module application. IEEE Trans. Power Electron. **27**(4), 1809–1817 (2012)

An Energy-Efficient and Reliable Depth-Based Routing Protocol for Underwater Wireless Sensor Network (ER-DBR)

S. Neelavathy Pari, M. Sathish and K. Arumugam

Abstract Underwater sensor network (USN) has a wide range of aquatic application that is totally different from terrestrial sensor network. The nodes of USN have a peculiar characteristics like float mobility, limited bandwidth and energy, signal and link quality, routing challenges and its cost and high error probability. By this nature, USN degrades the performance in terms of throughput and lifetime. This paper presents the link quality, routing path issue built on depth-based routing techniques to overcome the shortages in the existing work. Triangular metric-based routing is a geometric combination of packet reception probability (PRP), signal-to-noise ratio (SNR) and link quality indication (LQI) that is used to select the next forwarding node with reliability, which in turn reduces the routing cost. Moreover, it makes the very less energy consumption and improves the network lifetime. This method overcomes the unnecessary overlapping and repairs the link failure during network operation. The simulation results show that the proposed work reduces the cost of the route and improves the network lifetime by consuming less energy.

Keywords Underwater sensor networks · Energy consumption
Remaining energy · Depth-based routing protocol · Triangular metric

S. Neelavathy Pari (✉) · M. Sathish (✉) · K. Arumugam
Madras Institute of Technology, Chennai, India
e-mail: neela_pari@yahoo.com

M. Sathish
e-mail: sathish.sai91@gmail.com

K. Arumugam
e-mail: sixf08@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_45

1 Introduction

Underwater wireless sensor networks (UWSNs) are suitable for various application scenarios in environmental, military areas, pollution monitoring, disasters prevention which impacts tsunami alert, offshore exploration, navigation, gas/oil spills detection and tactical surveillance [1]. Underwater wireless sensor network is quite different from the terrestrial wireless sensor networks. The main difference is using sound signals as communication medium for UWSNs. This is because of radio less frequency in underwater. The frequency signals transmit long distance only at low frequencies that need high antennas and spectral power density [2, 3]. Acoustic waves never hurt from this high attenuation, but are influenced by vibrations and prone to failures due to corrosion. The acoustic signals have featured less bandwidth and significantly high end-to-end delay as underwater sensor nodes are randomly deployed. Underwater sensor network involves some of the better challenges. Bandwidth availability (i.e. <100 kHz) scatters and prone failures, bad link availability and limited energy spectrum levels. Because of the informed particular challenges in type, these protocols proposed for terrestrial networks cannot access the UWSNs. Basically, the routing protocols for UWSNs can be divided into energy efficient, position information free, localization information required and cross-layer design protocol. Moreover, the localization is not efficient because of these movements of sensor nodes and random topology of underwater environment. Localization-free protocols are much recommended by scientific communities. In this phase, we introduce a location information protocol for UWSNs (named ERDBR), by taking into account triangular metrics packet reception probability (PRP), signal to noise ratio (SNR), link quality indication (LQI) rather than previous protocols that consider separate routing metrics (Depth, Remaining energy). The quality of information is used for selecting the neighbour node who have more reliability from all the selected candidate nodes. The remaining energy of nodes is optimized to equalize the energy consumption around all sensors. In ERDBR, the triangular metrics are analysed and provide recommendation for suitable forwarding node between all the one hop neighbours. During the data transmission time, the nodes which are very close to the sink nodes are selected to forward the packets.

2 Related Works

To our knowledge, only two protocols [4, 5] in UWSNs measure the Link Quality in their sending process which is based on calculating ETX (Expected Transmission Count) between source node and next forward node. All of these protocols either utilize full location information provided by GPS (location-based) [4] or use partial information provided by Sink Node (Location-free Beacon based) [5]. Hitherto, to our knowledge, on one have been used Link Quality [6] in depth routing protocols. For that purpose, our proposed protocol is the first depth routing protocol that

measures the Link Quality. In [7], DBR uses the depth of the neighbour nodes as a routing protocol metric. The sender node broadcasting the packet includes its own depth of the data packet. It depends upon received packets, the received nodes compare the value of its node ID with chosen ID of the node that interconnect with the packet. Therefore, only the nodes that matche its node ID with the selected node ID that embedded with the packets accept the data packets while is discarded by all remaining nodes. The operation is significantly occurring again until data packets reach one of the best nodes. Then, the data packets are directly accessed to one of the sinks. It allows a minimum number of nodes to forward the data packets, the node having the highest remaining energy from hello packet format among its neighbours has zero holding time, while in all other neighbours forwarding nodes hold the data packet for a particular time.

3 Network Architecture

Figure 1 shows UWSNs' architecture used in most of related works. In this figure, all sink nodes are deployed at water surface connected to each other by radio frequency links. Normal sensor nodes are randomly placed under water surface from high to low at various depths. It is accepted that, sink nodes are utilized with sound wave links (exchanging information with UWSNs) and radio link (communication with sinks and data centre). Sensor nodes send the message from sender node to the receiver by relaying the data packets through sensor nodes placed near to sink. More precisely, the sensor nodes placed at bottom of deployment region (higher depth) forward the message by moving the data packet through sensor nodes placed at top of deployment region (lower depth). By next information, the sensor nodes are capable to be used at various depths by exchange information. However, due to the nodes movement with water current, there is a high chance to increase void regions. Hence, in this void region, communication becomes a big question mark, as there nodes will not be in the position to transfer or receive the packets.

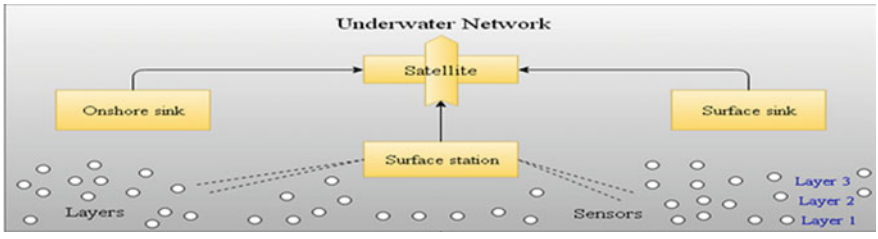


Fig. 1 Architecture of underwater sensor network

3.1 Link Quality Metrics

Link quality estimator is one of the best criteria that have direct impact on the performance of minimizing the energy consumption, maximizing delivery ratio and throughput. The triangular metric [6] is taken into account out of more link quality analysis approximation that have not been measured yet in UWSNs. On the other hand, many link quality analysis approximations have been proposed in the literature of UWSN, i.e. ETX [8], WMEWMA [9] and RNP. These metrics only consider (PRP) delivery ratio for calculating the link quality which did not obtain stability and full reliable link. Therefore, these metrics cannot obtain high link quality between nodes. An important advantage of the triangular metric is that it can obtain fast assessment, reliable estimation and minimized traffic overhead.

The triangular metric is a mathematically merging of the cogency of PRP, SNR and LQI. The triangular metric further is a combination of PRP [10, 11], LQI [12, 13] and SNR [14] in order to guarantee reliable and fast link quality estimation by calculating mean LQI and mean SNR.

The formal equation of the triangular metric can be described as n packets with m successfully received packets where $(0 < m \leq n)$. The SNR and LQI for each successfully transmitted packet i are indicated by snr_i and lqi_i. The sender node broadcasts 10 probe packets in specific time to its neighbour nodes. After receiving the packets, the responding nodes determine mean SNR_i and mean LQI_i using the following equations:

$$\overline{\text{SNR}} = \frac{\sum_{k=1}^{m} \text{snr}_k}{n} \tag{1}$$

$$\overline{\text{LQI}} = \frac{\sum_{k=1}^{m} \text{lqi}_k}{n}. \tag{2}$$

The receiver node then calculates the distance to the origin (distance of hypotenuse using Pythagorean theorem from Fig. 2) characterized by a point ($\overline{\text{LQI}}$, SNR) and the origin (0, 0) using the following equation based on Eqs. (1) and (2):

$$\Delta d = \sqrt{\overline{\text{SNR}}^2 + \overline{\text{LQI}}^2}. \tag{3}$$

Based on the calculated distance, the reviver node estimates the link quality for the link between sender and receiver nodes on the base of large distance, the best link quality. In our proposed protocol, each node computes the link quality based on the triangular metric and then exchanges the link quality information among its neighbours. Table 1 illustrates the triangular metric-based link selection (very good link, good link, intermediate link, poor link).

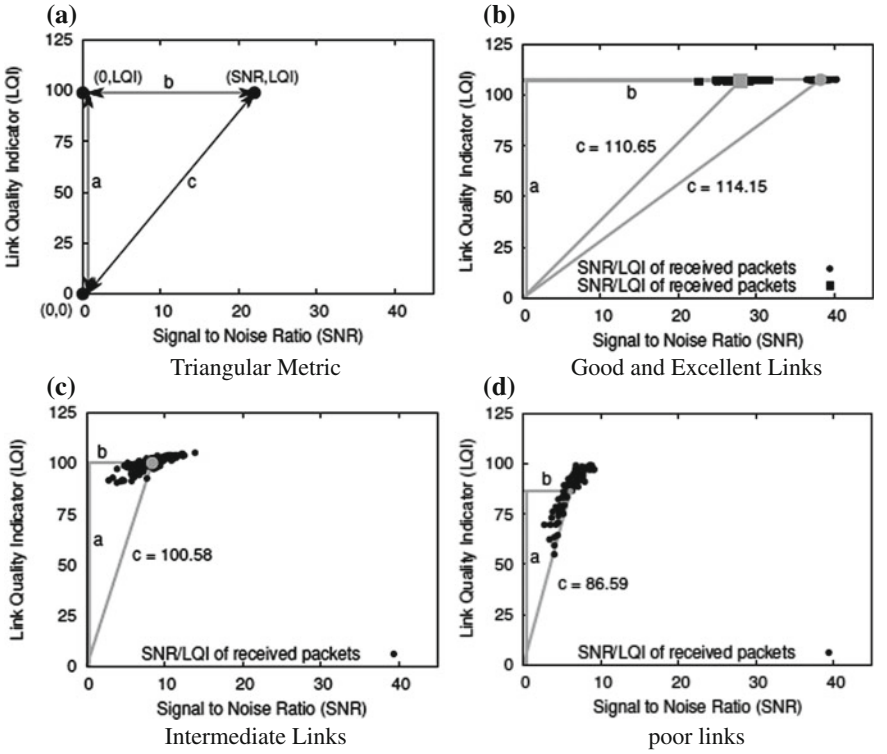


Fig. 2 **a** Triangular metric with comparison of LQI and SNR. **b** It reduces with low-quality links. **c**, **d** It cannot tolerant with high PRP

Table 1 Triangular metric-based link selection (very good, good, intermediate, poor)

Link category	Metric			
	SNR	LQI	PRP	Triangular calculation
Excellent link	>25	>100	1	>104
Good link	10–25	95–100	0.70–1	95–104
Intermediate link	5–10	85–95	0.30–0.70	85–95
Poor link	0–5	0–85	0–0.30	0–85

3.2 Neighbour Knowledge Collection Phase

In this section, each sensor node computes the distance based on the triangular metric and share depth and remaining energy among neighbours. This knowledge can help in selecting the best neighbour nodes as a forwarder during forwarding phase, i.e. if a sensor node have data packets to send to the sink node, then depth,

residual energy and the distance have been used to select the next-neighbour nodes to forward the data packets to the sink.

The process of this section is as follows. Each sensor node broadcasts a Hello packet to its one hop neighbour nodes. This Hello packet contains depth of the node, remaining energy and the distance of the triangular metric links towards its neighbours. To compute the distance, each node broadcasts a less amount of packets with very small size packets containing transmitting nodes' ID towards its neighbour nodes and then compute distance based on the triangular metric as mentioned in the previous section. Figure 3 shows the Hello packet format. After receiving the Hello packets, underwater sensor nodes store depth, remaining energy and distance for the sensor nodes that have smaller depth. It is reported that it is not required to store information for all sensor nodes; this is because the data routing starts from bottom (higher depth) to up (lower depth) until reaching sink node. Therefore, sensor nodes only save details about sensor nodes that have smaller depth, which avoid saving huge amount of data. In UWSNs, updating the depth information is not significance because the underwater sensor nodes are occupying at the identical depth with horizontal direction movements, and the vertical direction movements are mostly negligible [15]. However, the remaining energy for each underwater sensor node is changed with an interval time due to distinct functions, i.e. transmitting, receiving, forwarding and processing. Therefore, remaining energy for all of underwater sensor nodes needs to get modified and updated. In our proposed protocol, employ a distributed approach, each sensor node checks its remaining energy information on an interval basis. We set a system parameter as a threshold value and compare it with the difference between the current and existing remaining energy; if the remaining energy value is larger than the threshold, this underwater sensor node broadcasts Hello packets to its one-hop neighbour nodes including the updated remaining energy. This approach helps in keeping all nodes updated remaining energy information which leads to balance the energy between sensor nodes and sinks to decrease the consuming energy and increase the network lifetime.

At the end of this section, each sensor node becomes aware of their neighbours' information, their depth, remaining energy and distance of the triangular metric link towards neighbour nodes.

Fig. 3 Format of Hello packet

3.3 Data Forwarding Phase

This section describes packet transmission between sender node and sink node. The next-neighbour forwarding node should be immediate distance to the sink, with high remaining energy and good link quality will have a least cost. Rest of the nodes that have sudden distance to the sink support to forward the data. However, and different from [13] that deliberated minimum cost based on remaining energy and ETX, calculate the route cost based on remaining energy and link quality to choose the next forwarding node. Therefore, the route cost can be calculated between two nodes (x, y) using Eq. (4):

$$\text{Route Cost}(x, y) = (1 - \frac{\text{Res}_y}{\text{Res}_{\max}}) + (1 - \frac{\Delta d_{(x,y)}}{\Delta d_{\max}}), \tag{4}$$

where Res_y is the standard value of the remaining energy of node y, $\text{Res}_{\max}$ is a total energy value of a node, $\Delta d_{\max}$ is a maximum distance parameter value and set according to the conditions, i.e. choose the max Δd after simulating different underwater scenarios, $\Delta d_{(x,y)}$ is the link quality value of the link that computed between sender and forwarder nodes x, y. This equation calculates the route cost based on two different metrics, that is, remaining energy and quality of the link. Based on Eq. (4), it is expected that the node that placed at lower depth than sender with higher remaining energy and best quality of the link will have least route cost. Thus, this node will be chosen as a next forwarding node to send data packets. Process of data forwarding is as follows. The sender node first retrieves all neighbour's information from the neighbour information table and computes route cost based on Eq. (4). The sender node then selects the nodes that have minimum routing cost. The further process is that the sender node embeds the ID of the chosen node with the data packets. It depends upon the received packets; the received nodes compare the value of its node ID with chosen ID of the node that interconnect with the packet. Therefore, only the nodes that match its node ID with the selected node ID that embedded with the packets accept the data packets while they are discarded by all remaining nodes. The operation is significantly occurring again until data packets reach one of the best nodes. Then, the data packets are directly accessed to one of the sinks. The sender nodes try to transmit the data packets with best link quality, but the link quality in UWSNs is not in steady state [14]. Therefore, it is possible that the data packets might not reach its destination/next forwarding node because of dropping of packets. Our proposed protocol utilizes an implicit acknowledgment, that is, neighbour nodes overhear the data packets that transmitted by next forwarding node. Hence, neighbour nodes buffer the packets for an accurate time (i.e. in our simulation scenario we set 1 s) and upon overhearing the identical data packets from its receiving node, the forwarding node eliminates the data packets from its buffer. Otherwise, retransmission mechanisms have been applied to retransmit the data packets again.

4 Performance Evaluation

4.1 Simulation Scenarios

In this section, an explanation of the simulation setup to simulate the algorithms is done using Aqua-Sim. Aqua-Sim is an underwater supportive package attached in NS-2 and works in parallel with Communication Management Unit (CMU) used to analyse the performance of the ERDBR protocol. This Aqua-sim 3 dimension is used to simulate the 3D underwater architecture. Radio range is set 250 m. Moreover, it supports different numbers of underwater wireless sensor nodes (25–400) in 3-D area size of 1250 m × 1250 m × 1250 m. Different numbers of sink are set based on the number of nodes (3–7) deployed on water surface in order to receive the packet from underwater sensor nodes via sound waves and forward it to the super nodes via radio signals. The initial energy of sensor nodes is set to 100 J. In addition, the amount of total energy reduction in terms of transmission, receiving and idle is considered equal to 2W, 0.75W and 10 MW, respectively. The results have been averaged from 50 iterations to increase the accuracy of the simulation results. Table 2 illustrates the simulation set up parameters used in this study.

4.2 Results and Study

4.2.1 Packet Delivery Ratio (PDR)

The packet delivery ratio of DBR and ERDBR in a random network topology is shown in Fig. 4. In the proposed methodology, the redundant transmissions of

Table 2 Simulation scenario

Simulation parameter	Value
Network topology	Random and grid (100 m)
Deployment area	1250 m × 1250 m × 1250 m
Number of sinks	3–7
Number of nodes	25–400
Transmission range	250 m
MAC protocol	Broadcast MAC
Initial energy	100 J
Communication medium	Acoustic waves
Bandwidth	10 kbps
Signal velocity	1500 m/s
Node movement	0–3 m/s
Energy consumption	2 W, 0.75 W and 10 MW
Data packet size	64 byte
Hello packet interval	100 s
Simulation time	1500 s
Number of runs	50

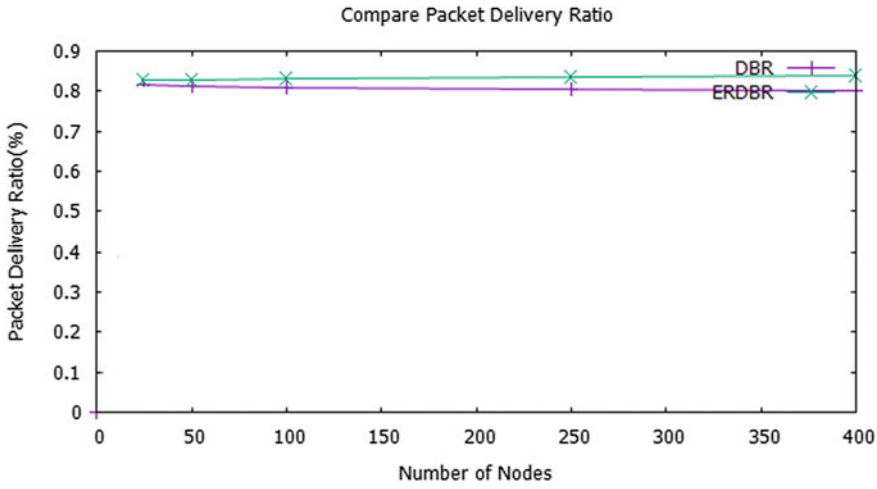


Fig. 4 Comparison of packet delivery ratio (DBR, ERDBR)

packets are minimized by the forwarding node. Suppose the packets are not successfully received to the sink node, it has to be decided which forwarding node takes the authority to retransmit the packets. Moreover, the packet loss is significantly less, so improve the ratio of packets.

In the graphical representation between nodes versus PDR, when the number of nodes incremented from 25 to 400 nodes, ERDBR has increased the performance by 2.73%.

4.2.2 End-to-End Delay

The End-to-End delay of DBR and ERDBR in a random network topology is shown in Fig. 5. Therefore, every node in this work tunes the packets for an accurate time in terms of the depth variance with the previous node. In ERDBR, the second highest remaining energy node forwards the message. The transmitting sensor does not have an enough time to push the packets and less delay with low propagation. This method decreases the delay around 43%.

4.2.3 Energy Consumption

Figure 6 shows the comparison of energy consumption in random network topology. DBR causes more energy consumption in 25–400 nodes which keep on increasing. If the number of nodes is increasing, most of the nodes are involved in transmitting, receiving, forwarding and processing; therefore overall consumption of energy also increases. In contrast, in ERDBR, the energy consumption is lower

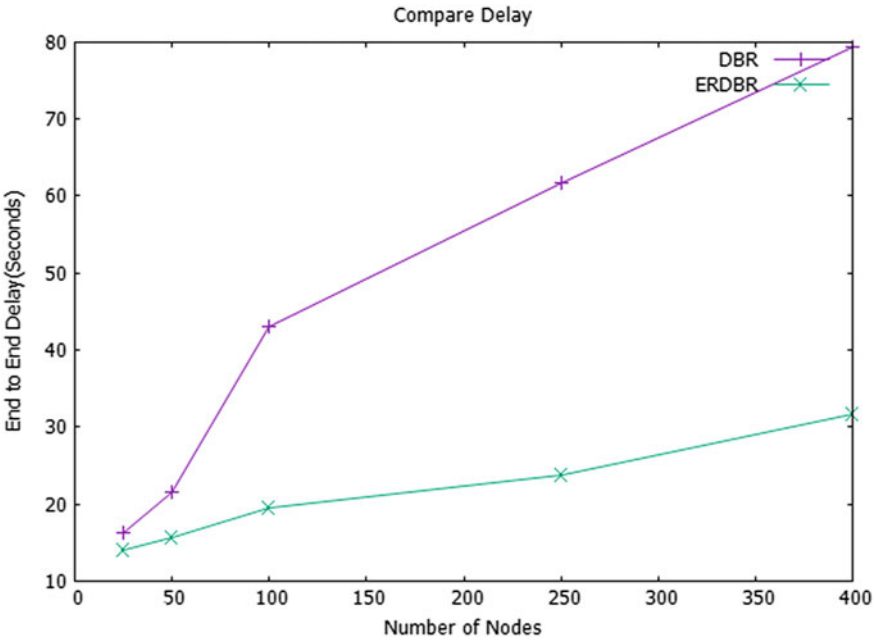


Fig. 5 Comparison of end-to-end delay (DBR, ERDBR)

than DBR, because ERDBR allows a minimum number of nodes to forward the data packets; the node having the highest remaining energy from Hello packet format among its neighbours has zero holding time, while in all other neighbours forwarding nodes hold the data packet for a particular time. Moreover, in ERDBR, increasing number of nodes cannot affect the energy consumption. This is the reason why only single neighbour node is used to forward in all categories. This work significantly upgrades the consumption of energy around 24.81%.

4.2.4 Network Lifetime

Figure 7 describes the graphical view of remaining energy in random network topology. In addition, DBR forwards the data after performing lower level depth analysis; this helps to reduce energy consumption. But ERDBR, using triangular metric, allows to minimize the number of nodes to forward data packets and inessential data packets are reduced, increasing network lifetime. This work significantly improves the lifetime of network around 37.5%.

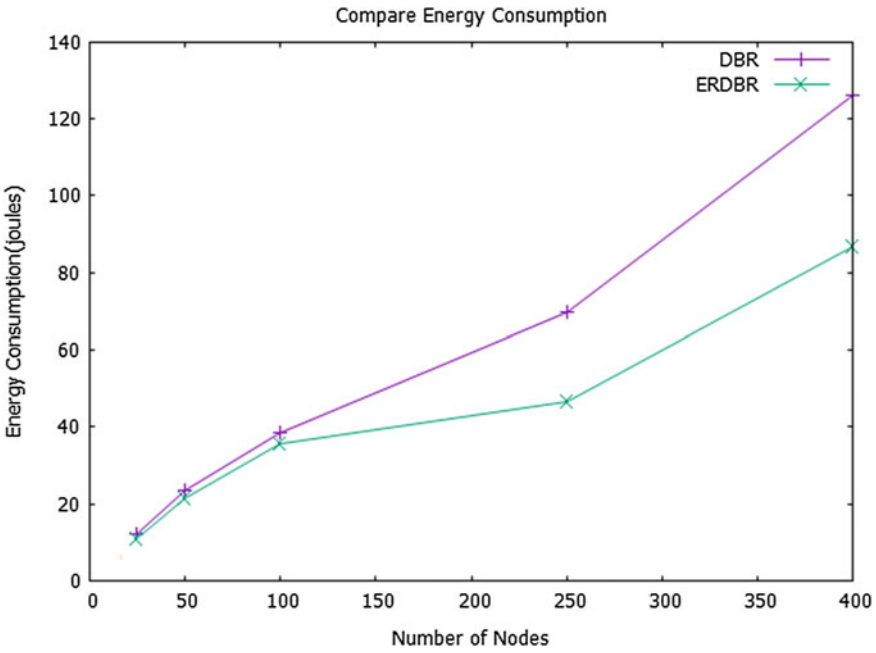


Fig. 6 Comparison of energy consumption (DBR, ERDBR)

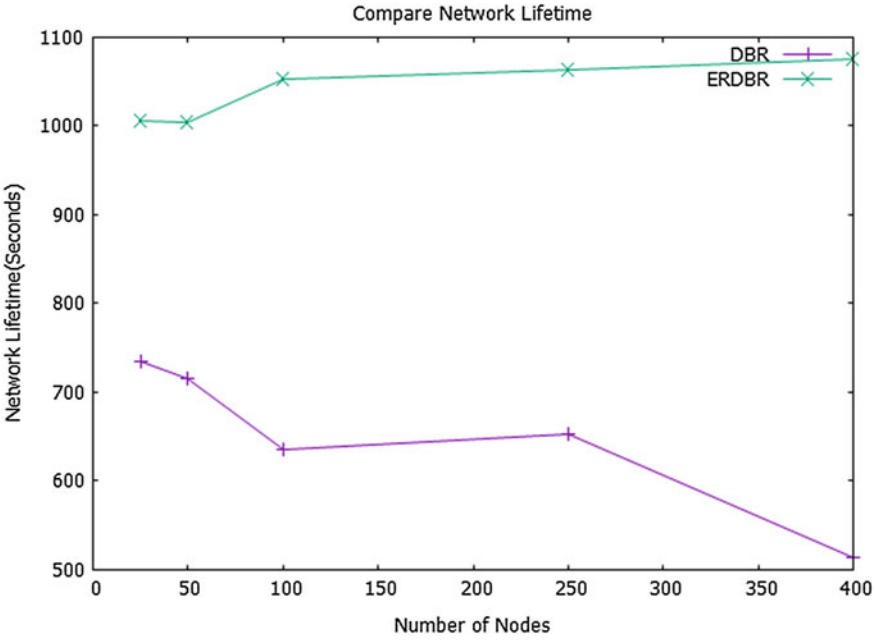


Fig. 7 Comparison of network lifetime (DBR, ERDBR)

5 Conclusion

The proposed method gives a novel solution using triangular metrics (PRP, SNR, LQI) to improve the route cost, reduce energy consumption and increase link quality. ERDBR works in various phases, namely, link quality metrics phase, neighbour knowledge collection phase and data forwarding phase. Link quality metrics phase is a combination of PRP, LQI and SNR in order to guarantee reliable and best link quality estimation by calculating mean LQI and mean SNR. During neighbour knowledge collection phase the distance based on the triangular metric shares depth of the node and remaining energy among neighbours. The data forwarding phase is to minimize the route cost among neighbours. Using the novel solution, we observed a 43% decrease in end–to-end delay, 24.81% reduce in energy consumption, 2.73% increase in packet delivery ratio and 37.5% increase in network lifetime. In future work, void aware data packet forwarding algorithm can be introduced to identify the real and logical void nodes and avoid the void nodes in forwarding process.

References

1. Shin, D., Hwang, D., Kim, D.: DFR: an efficient directional flooding-based routing protocol in underwater sensor networks. Wireless Commun. Mobile Comput. **12**(17), 1517–1527 (2012)
2. Wahid, A., Lee, S., Kim, D.: A reliable and energy-efficient routing protocol for underwater wireless sensor networks. Int. J. Commun Syst **27**(10), 2048–2062 (2014)
3. Boano, C.A., Zúniga, M.A., Voigt, T., Willig, A., Römer, K.: The Triangle Metric: Fast Link Quality Estimation for Mobile Wireless Sensor Networks. In: (Eds.): The Triangle Metric: Fast Link Quality Estimation For Mobile Wireless Sensor Networks (IEEE edn.). pp. 1–7 (2010)
4. De Couto, D.S., Aguayo, D., Bicket, J., Morris, R.: A high-throughput path metric for multi-hop wireless routing. Wireless Netw. **11**(4), 419–434 (2005)
5. Woo, A., Tong, T., Culler, D.: Taming the underlying challenges of reliable multihop routing in sensor networks. In: (Eds.) Taming the Underlying Challenges of Reliable Multihop Routing in Sensor Networks (ACM edn.). pp. 14–27 (2003)
6. Zhou, A., Wang, B., Sun, X., You, X., Sun, H., Li, T.: SLQE: an improved link quality estimation based on four-bit LQE. Int. J. Future Gener. Commun. Network. **8**(1), 149–160 (2015)
7. Yan, H., Shi, Z., Cui, J.H.: DBR: Depth-based routing for underwater sensor networks. In: Proceedings of the IFIP Networking'08 Conference, Singapore, pp. 72–86, (2008)
8. Sang, L., Arora, A., Zhang, H.: On link asymmetry and one-way estimation in wireless sensor networks. ACM Trans. Sensor Netw. (TOSN) **6**(2), 12 (2010)
9. Boano, C.A., Voigt, T., Dunkels, A., Osterlind, F., Tsiftes, N., Mottola, L., Suárez, P.: Exploiting the LQI Variance for Rapid Channel Quality Assessment. In: (Eds.): Exploiting the LQI Variance for Rapid Channel Quality Assessment. (IEEE Computer Society, edn.). pp. 369–370 (2009)
10. Polastre, J., Szewczyk, R., Culler, D.: Telos: Enabling Ultra-Low Power Wireless Research. In: (Eds.) Telos: Enabling Ultra-Low Power Wireless Research (IEEE edn.). pp. 364–369 (2005)

11. Sehgal, A., Cernea, D., Birk, A.: Modeling Underwater Acoustic Communications for Multi-robot Missions in a Robotics Simulator. In: (Eds.) Modeling Underwater Acoustic Communications for Multi-robot Missions in a Robotics Simulator (IEEE edn.). pp. 1–6 (2010)
12. Nicolaou, N., See, A., Xie, P., Cui, J.-H., Maggiorini, D.: Improving the Robustness of Location-Based Routing for Underwater Sensor Networks. In: (Eds.) Book Improving the Robustness of Location-Based Routing for Underwater Sensor Networks (IEEE edn.). pp. 1–6 (2007)
13. Wahid, A., Kim, D.: An energy efficient localization-free routing protocol for underwater wireless sensor networks. Int. J. Distrib. Sens. Networks (2012)
14. Dhurandher, S.K., Obaidat, M.S., Gupta, M.: Providing reliable and link stability-base geocasting model in underwater environment. Int. J. Commun. Syst. **25**, 356–375 (2012). doi:10.1002/dac.1245
15. Wafta, M.K., Selman, S., Denkilkian, H.: UW-MAC: an underwater sensor network MAC protocol. Int. J. Commun. Syst. **23**, 485–506 (2010). doi:10.1002/dac.1086

Adaptive PI Control of STATCOM for Stability Improvement of Power System

Rubi Kumari and Chitrangada Roy

Abstract The power system today has become a very complicated network with thousands of generating stations, distribution and load centres which are interconnected through power transmission lines. So, the sudden increase of load in order to meet the demand leads to voltage instability in the power system. For overbear the steady-state control difficulties in power systems, Flexible Alternating Current Transmission Systems (FACTS) controllers came into use. Among various FACTS controllers, Static Shunt Compensators shortly termed as STATCOM are efficient enough to provides instantaneous requirement of reactive power support to maintain stability of voltage in the power system. The STATCOM with proportional integral (PI) controllers act as a trail-and-error approach because the PI controller parameters are not fixed. This paper proposes a new control method where PI controllers will self-adjust their control parameters at the time of any disturbances or variation in the load so that the performance of the power system will match the desired response, despite of any change in the operating conditions. The projected work was enforced in MATLAB/SIMULINK.

Keywords Static synchronous compensator (STATCOM) · State-space vector pulse width modulation (SVPWM) · Flexible alternating current transmission system (FACTS) · Voltage source converter (VSC)

R. Kumari · C. Roy (✉)
Department of Electrical & Electronics Engineering, Sikkim Manipal Institute of Technology, Rangpo, India
e-mail: roychitrangada@gmail.com

R. Kumari
e-mail: rubi09kumari@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_46

1 Introduction

A power system is subdivided into four parts, i.e. generation from various power plants, transmission through overhead and underground transmission networks, distribution which is done by the various substation and utilization, i.e. use of the power by the consumer. The chances of voltage collapse increases when the demand suddenly increases than the daily requirements. Voltage stability and reactive power compensation are the two main aspects of a single activity that needs to be considered in the power system. Voltage stability can be controlled either by absorbing or delivering the required amount of reactive power to the power system [1].

Based on the rapid development of power electronics technology, Flexible Alternating Current Transmission System (FACTS) controllers came into use for improving the efficiency of the transmission networks [2]. Due to recent development in FACTS techniques, it became possible to improve the power quality and decrease the voltage instability problems in the power system. Among various FACTS controllers, STATCOM proved to be the best one because it provides instantaneous, quick and effective reactive power for stability of voltage in the power system [3].

This paper mainly focuses on various controls design methods in the STATCOM [4]. First, the results of the STATCOM model with the PI controllers were checked. The PI controller gains acted as a trial-and-error at the time of disturbances which affected the performance and efficiency. Thus, in order to achieve fast, highly efficient and better outcomes of the power system in different functioning situations STATCOM with Adaptive PI controller has been implemented [5].

2 Designing of the Test System

The three-phase test system has been shown in Fig. 1. The generation voltage is 11 kV at 50 Hz. The length of three-phase 33 kV pi-section line is 50 km. The receiving end comprises of two RL loads of 1 MW at 0.8 power factor lagging each. The transient time given to the three-phase breaker is 0.6 s and at that instant another RL load of 4.25 MW at 0.8 power factor lagging is introduced to the system.

3 STATCOM Controller Design

A STATCOM is defined as the Voltage Source Converter (VSC) which generates and absorbs the required amount of the reactive power to the transmission system. The three-phase equivalent circuit of the STATCOM has been exhibited in Fig. 2.

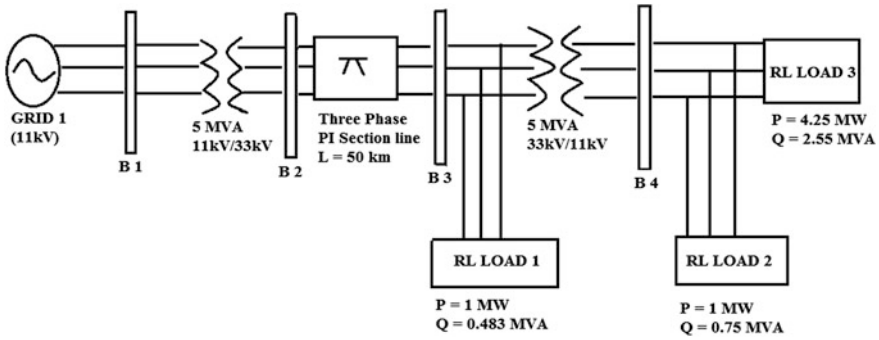


Fig. 1 Block diagram representation of the three-phase test system

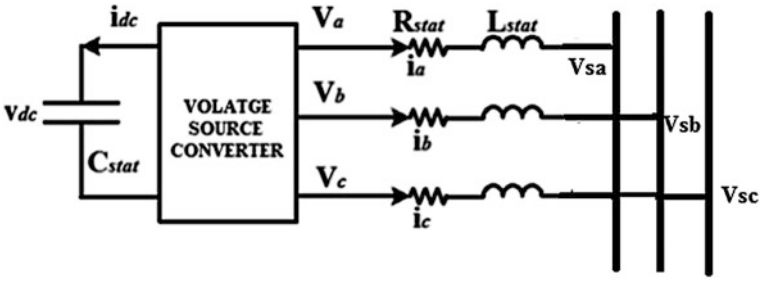


Fig. 2 STATCOM equivalent model

The STATCOM model contains a Direct Current (DC) link capacitor so that only exchange of reactive power should take place, a VSC, three resistors which has been denoted as R_{stat}, three inductors denoted as L_{stat}. The R_{stat} represents conduction losses of the transformer which has been connected in series with the Alternating Current (AC) lines, whereas the (L_{stat}) inductor represents the filter leakage inductances [6]. (V_a, V_b, V_c) are the STATCOM output voltage (V_{sa}, V_{sb}, V_{sc}) are the three-phase transmission line voltage and (i_a, i_b, i_c) are the transmission line current.

The voltage has been transformed from *d-q* frame to the stationary frame by Clark's Transformation method. Equations (1) and (2) represent the STATCOM voltage after conversion in terms of *d-q*:

$$v_d = R_{\text{stat}} i_d + L_{\text{stat}} \frac{\mathrm{d}i_d}{\mathrm{d}t} - \omega_e L_{\text{stat}} i_q + v_{sd} \tag{1}$$

$$v_q = R_{\text{stat}} i_q + L_{\text{stat}} \frac{\mathrm{d}i_q}{\mathrm{d}t} + \omega_e L_{\text{stat}} i_d + v_{sq} \tag{2}$$

where (v_d, v_q) are the *d-q* components of STATCOM voltage, (i_d, i_q) are transmission line current and (v_{sd}, v_{sq}) is the output voltage of the transmission network. The power losses in the system have been neglected for better simplification. So, the AC and DC side power balance will result in:

$$P_{\mathrm{dc}} = P_{\mathrm{ac}} \tag{3}$$

$$v_{\mathrm{dc}} i_{\mathrm{dc}} = v_a i_a + v_b i_b + v_c i_c \tag{4}$$

$$C_{\mathrm{stat}} v_{\mathrm{dc}} \frac{\mathrm{d}v_{\mathrm{dc}}}{\mathrm{d}t} = \frac{3}{2}(v_{sd} i_d + v_{sq} i_q) \tag{5}$$

where v_{dc} denotes the STATCOM's Direct Current (DC) link voltage and i_{dc} is the DC link current of the STATCOM. Considering v_{sq} being zero for right rotating alignment. DC link voltage can be obtained from Eq. (6).

$$\frac{\mathrm{d}v_{\mathrm{dc}}}{\mathrm{d}t} = \frac{3}{2}\frac{v_{sd} i_d}{C_{\mathrm{stat}} v_{\mathrm{dc}}} \tag{6}$$

The reactive power generated by the STATCOM can be calculated using Eq. (7)

$$Q_{\mathrm{stat}} = \frac{3}{2} v_{sd} i_q \tag{7}$$

According to Fig. 3, it consists of two Proportional Integral (PI) controller loops. The inside PI control loop is the current control loop which controls the '*d*' and '*q*' elements of the STATCOM currents (i_q and i_d), and giving current references ($i*_d$, $i*_q$) as the error signal on comparison for VSC. The outer part denotes the voltage control loop to which the reference current is fed and compared with its actual values thus generating reference voltage ($v*_d$, $v*_q$). The error signal generated is further compared with the actual voltages. The State-Space Vector PWM technique has been used to generate pulses to drive the Voltage Source Converter of STATCOM [7].

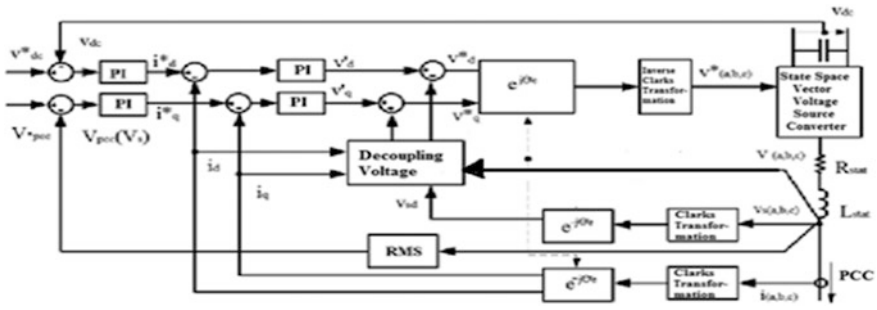


Fig. 3 Block representation of the STATCOM PI controller

4 Adaptive PI Control for STATCOM

4.1 Concept Behind the Adaptive PI Control for STATCOM

As discussed earlier, the PI controllers were used in the STATCOM model but the trial-and-error approach of the PI control gain parameters affected the overall output and efficiency of the STATCOM which was not feasible. The situation went worse if there was any change in the operating conditions of the transmission system. Thus, the STATCOM controller was unable to perform at the time of requirements. Therefore, for more efficient and adaptable system an Adaptive PI control method was implemented over here in the STATCOM model to increase the voltage regulation in the transmission networks. The Adaptive PI control method was able to self-adjust the control parameters itself under different disturbances such as sudden increase of the load, voltage fluctuation, faults and many more in the power system (in this case sudden increase of load was considered). Thus, any modification in a system will not affect the power system *f* the voltage such as instability of the voltage, poor performance of the system and many more. Thus this will make the STATCOM an adaptive device because of which STATCOM will provide dynamic performance in various operating conditions.

4.2 Designing of the Adaptive PI Controller for STATCOM

The block representation of the Adaptive PI controller of STATCOM has been shown in Fig. 4. In the outer block (voltage control block), the measured voltage $V_m(t)$ has been compared with the reference voltage denoted as $V_{\text{ref}}(t)$, and the K_{p_V}, K_{i_V} are adjusted so that the measured voltage matches the reference voltage

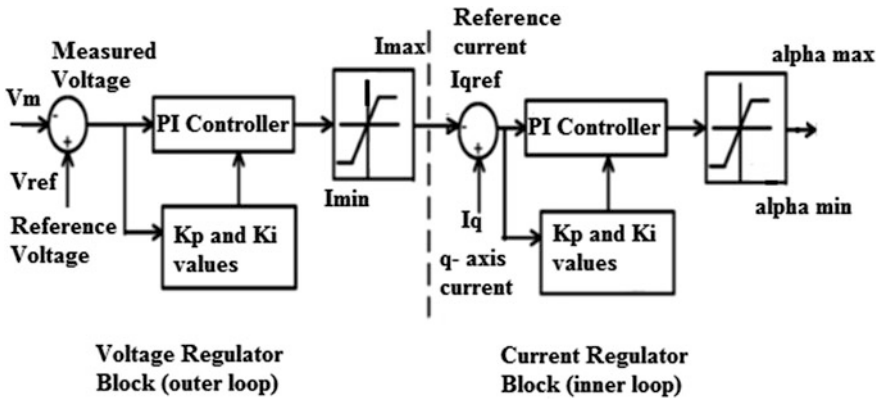


Fig. 4 Block representation of the adaptive PI control

and generates an error signal as q-axis reference current (I_{qref}) which was compared with the actual value of the q-axis current (I_q). The inner loop (current control block), I_{qref} was compared with the original value of the q-axis current (I_q) and based on the error signal obtained K_{p_I} and K_{i_I} has been adjusted. Further an angle (alpha) was determined and based on the angle STATCOM will do reactive power compensation into the system for voltage stability.

The calculated voltage $V_m(t)$ can be calculated from STATCOM output voltage (V_d and V_q) obtained in Eqs. (1) and (2):

$$V_m(t) = \sqrt{V_d^2(t) + V_q^2(t)} \tag{8}$$

Based on the calculated voltage, i.e. $V_m(t)$, the reference voltage $V_{\text{ref}}(t)$ was calculated:

$$V_{\text{ref}}(t) = V_{ss} - (V_{ss} - V_m(t))\mathrm{e}^{-t/\tau} \tag{9}$$

When the system operates in the normal condition, the parameters of the K_{p_V} and K_{i_V} will have no effect and STATCOM would not do reactive power injection or absorption in the system to maintain the voltage stability. But when there will be any disturbance in the power system, then $V_{\text{ref}}(t) = V_{ss} - (V_{ss} - V_m(t))\mathrm{e}^{(-t/\tau)}$ the control gain parameters, i.e. K_{p_V} and K_{i_V} will adjust itself and thus the STATCOM would inject the required reactive compensation so that voltage stability in the transmission networks will increase. The error between the reference voltage $V_{\text{ref}}(t)$ and the calculated voltage $V_m(t)$ has been denoted $\Delta V(t)$ [6]. Forward–Euler method was used to get the mathematical modelling of the proposed system the following equation has been obtained [6].

$$\Delta V(t)K_{p\_V}(t) + K_{i\_V}(t)\int_{t}^{t+Ts} \Delta V(t)\mathrm{d}t = I_{\text{qref}}(t + T_S) \tag{10}$$

where T_S = Sample Time

$$y(t) = y(t - T_S) + K_{i\_V}(t - T_S)T_S x\, \Delta V(t - T_S) \tag{11}$$

where

$$y(t) = K_{i\_V}(t)\int_{t}^{t+Ts} \Delta V(t)\mathrm{d}t \tag{12a}$$

$$y(t - T_S) = K_{i\_V}(t - T_S)\int_{t}^{t+Ts} \Delta V(t - T_S)\mathrm{d}t \tag{12b}$$

Considering $y(t - T_S) = I_{\text{qref}}(t)$, we rewrite Eq. (10) as follows:

$$\begin{aligned}\Delta V(t)K_{p\_V}(t) + K_{i\_V}(t)\int_{t}^{t+Ts}\Delta V(t)d - K_{i\_V}(t - T_S)\int_{t}^{t+Ts}\Delta V(t - Ts)\mathrm{d}t \\ = I_{\text{qref}}(t + T_S) - I_{\text{qref}}(t)\end{aligned} \tag{13}$$

For very short-time duration, we considered $K_{i\_V}(t) = K_{i\_V}(t - T_S)$. Hence, Eq. (13) was rewritten as:

$$\Delta V(t)K_{p\_V}(t) + K_{i\_V}(t)\int_{t}^{t+Ts} A\mathrm{d}t = I_{\text{qref}}(t + T_S) - I_{\text{qref}}(t) \tag{14}$$

where, $A = \Delta V\,(t)\; -\; \Delta V\,(t\; -\; T_S)$.

Based on Eq. (17), we determine the ideal response ratio $((I_{\text{qref}}(t + T_S\; -\; I_{\text{qref}}(t))/\,(\Delta V\,(t))$, and thus the ideal ratio $(K_{i\_V}(\mathrm{t}))/K_{p\_V}(\mathrm{t}))$ the desired $K_{p\_V}(\mathrm{t})$ and $K_{i\_V}(\mathrm{t})$ has been solved.

Assuming the ideal response, we get:

$$I_{\text{qref}}(t + T_S) - I_{\text{qref}}(t) = R \times \Delta V(t) \tag{15}$$

The system was considered stable and the delay time at which the system will become stable was considered to be 5τ. Since $I_{\text{qref}}(t_0) = 0$ based on Eqs. (13) and (8) can be rewritten as:

$$\Delta V(t_0)K_{p\_V}(t_0) + K_{i\_V}(t_0)\int_{t}^{t+Ts}\Delta V(t)\mathrm{d}t = R\; \times \Delta V(t_0) \tag{16}$$

where

t_0 is change in the operating condition.

$$K_{i\_V}(t_0) = \frac{R \times \Delta\, V(t_0)}{\int_t^{t+Ts}\Delta V(t)\mathrm{d}t} \tag{17}$$

Now, the ratio $mv = (K_{i\_V}(t_0))/(K_{p\_V}(t_0))$ is the ideal ratio of the values of $K_{p\_V}(t)$ and $K_{i\_V}(t)$ after the disturbance had occurred (in this case change of load).

Thus, Eq. (15) was rewritten as:

$$I_{\text{qref}}(t + 5\,\tau) - I_{\text{qref}}(t) = k_V V(t_0) \tag{18}$$

Here, k_V was considered as the steady and ideal ratio $(I_{\text{qref}}(t + T_S)) -$ $I_{\text{qref}}(t))/\,(\Delta V\,(t))$.

The rating of the STATCOM ($\Delta V_{\max}$) was obtained as:

$$\frac{\Delta V(t_0)}{\Delta V_{\max}} = k_V \times \frac{\Delta V(t_0) Kp\_V(t_0) + Ki\_V(t_0) \int_{t_0}^{t_0+5\tau} \Delta V(t)\mathrm{d}t}{R} \tag{19}$$

Based on (16), (18) and (19), k_V was calculated by:

$$k_V = \frac{R \times \Delta V(t_0)}{\left(\Delta V(t_0) K_{p\_V}(t_0) + K_{i\_V}(t_0) \int_{t_0}^{t_0+5\tau} \Delta V(t)\mathrm{d}t\right) \Delta V\max} \tag{20}$$

For exact calculation of the PI Control gains on the basis of Eq. (14) we can get:

$$\Delta V(t) K_{p\_V}(t) + m_V K_{p\_V}(t) \int_{t}^{t+Ts} A(t)\mathrm{d}t = k_V \times \Delta V(t) \tag{21}$$

Therefore, $K_{p\_V}(t)$ and $K_{i\_V}(t)$ were derived using equations shown above:

$$K_{p\_V}(t) = \frac{k_V \times \Delta V(t)}{\left(\Delta V(t) + m_V \int_t^{t+Ts} A(t)\mathrm{d}t\right)} \tag{22}$$

$$K_{i\_V}(t) = m_V K_{p\_V}(t) \tag{23}$$

Therefore, based on (22) and (23), $K_{p\_V}(t)$ and $K_{i\_V}(t)$ was adjusted automatically. A similar process was used to obtain the expression of current regulator PI gains:

$$K_{p\_I}(t) = \frac{k_i \times \Delta I_q(t)}{\left(\Delta I_q(t) + m_I \int_t^{t+Ts} B(t)\mathrm{d}t\right)} \tag{24}$$

$$K_{i\_I}(t) = m_I K_{p\_I}(t) \tag{25}$$

where, $\Delta I_q(t)$ is the error between I_{qref} and I_q, m_I means the ideal ratio of $K_{p\_I}(t)$ and K_{i_I} (t) after change in the operating condition and B is equivalent to $\Delta I_q(t) - \Delta I_q(t - T_S)$.

5 Results and Discussion

In this paper, the effect of sudden load variation on a three-phase test system has been observed under three conditions. First, the behaviour of the test system has been observed without STATCOM, Second with PI controller-based STATCOM and finally in presence of Adaptive controller-based STATCOM.

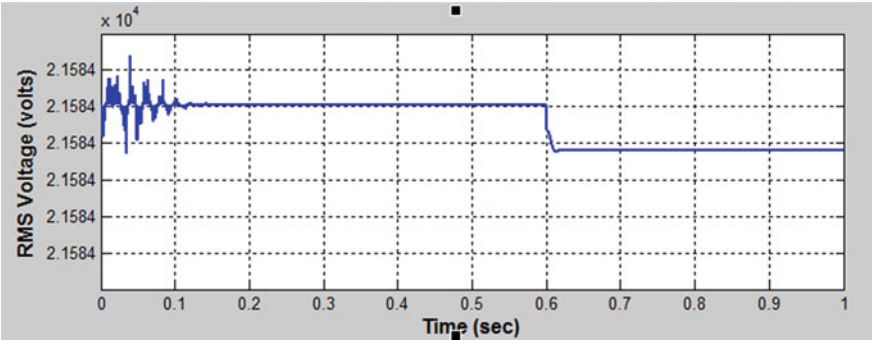


Fig. 5 RMS voltage of the transmission line at bus no. 3 without the STATCOM

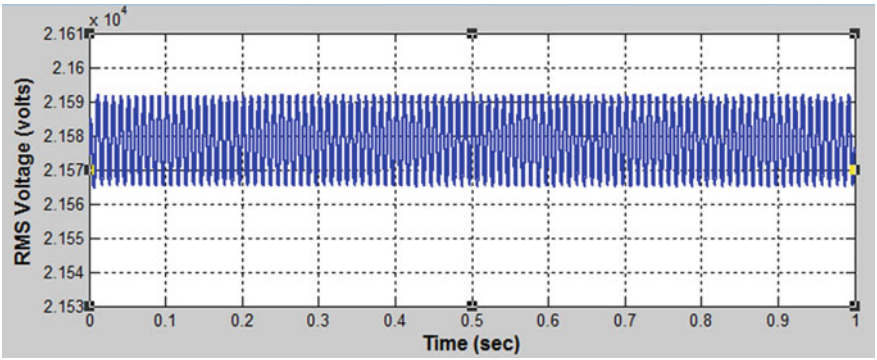


Fig. 6 RMS voltage of the transmission line system at bus no. 3 with normal PI controller-based STATCOM

In absence of compensating device, a voltage dip at 0.6 s was observed due to change in load at bus no. 3 as shown in Fig. 5.

After connecting STATCOM to the three-phase test system, it was observed that the voltage recovered and came back to its nominal value. The distortion occurring in the voltage profile is due to the random selection of the control parameters (PI gains) of STATCOM model in Fig. 6.

The distorted RMS voltage profile was improved by applying the proposed model of the Adaptive PI Controller for STATCOM which has been shown in Fig. 7. With an Adaptive PI Control of the STATCOM model the PI control parameters were adjusted automatically under sudden load variation.

Figure 8a shows the active power of the three-phase transmission test system. The fluctuation in active power at 0.6 s ensures more losses and instability of the power system due to sudden load change. In Fig. 8b, it was observed that in presence of the shunt compensator STATCOM active power recovered and came back to its nominal value but there were distortion in the profile due to the random selection of the control parameters (PI gains) in the STATCOM model.

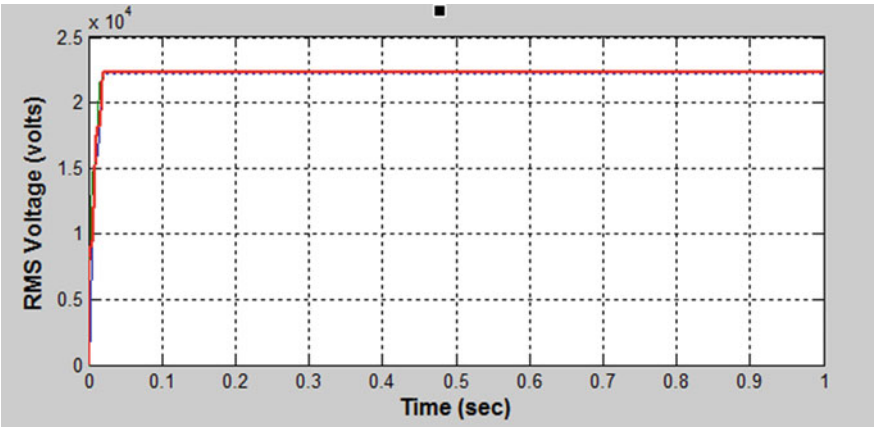


Fig. 7 RMS voltage at bus no. 3 with the adaptive PI controller of the STATCOM

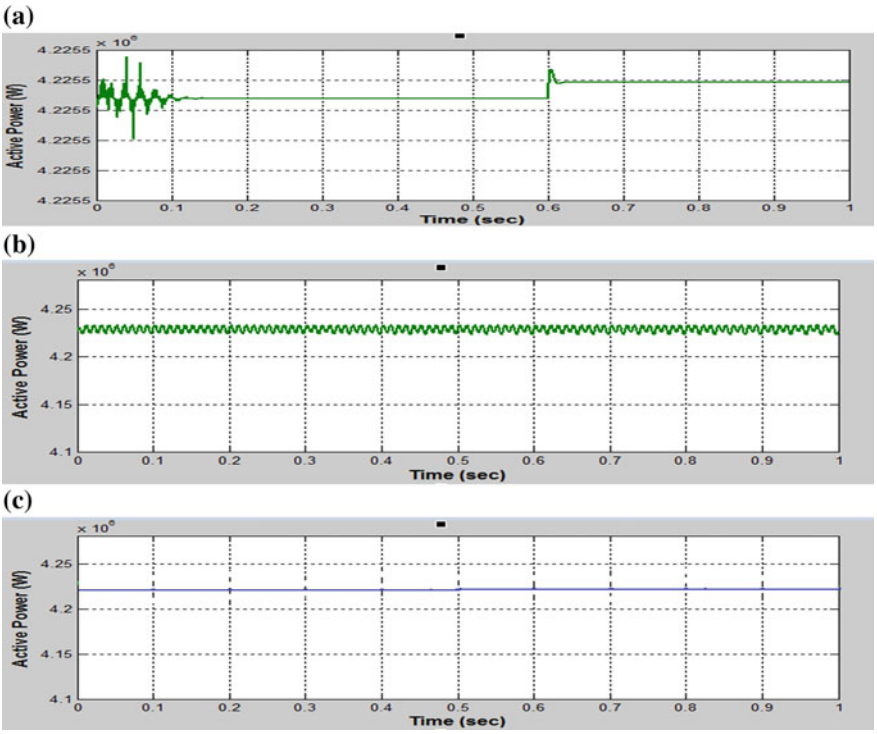


Fig. 8 Transmission line's active power **a** without STATCOM, **b** with the STATCOM model, **c** with the adaptive PI controller of STATCOM model

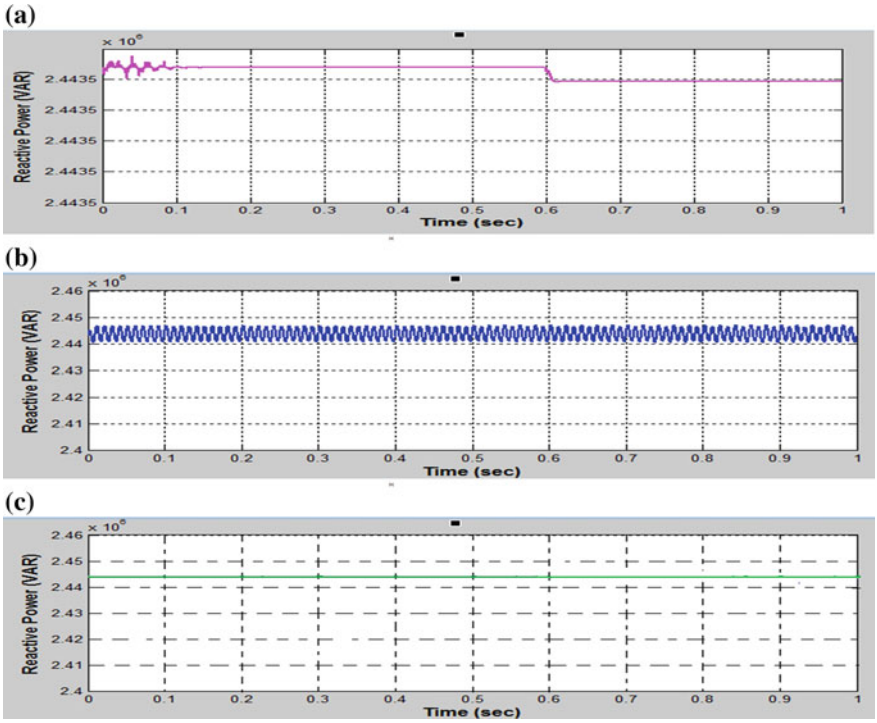


Fig. 9 Transmission line's reactive power **a** without the STATCOM model, **b** with STATCOM, **c** with the adaptive PI controller of STATCOM

Figure 8c shows that active power of the transmission line has been stabilized with the controlling action of adaptive PI Controller of STATCOM.

Figure 9a shows the reactive power of the three-phase transmission test system. Sudden change in load condition causes voltage to fall and current to increase which results in consumption of the reactive power by the system. After connecting STATCOM to the three-phase test system, the reactive power recovers but the graph has some distortions. Further, the distorted output has been improved by applying the proposed model of the Adaptive model of the Proportional Integral Controller for STATCOM because the PI control parameters were automatically adjusted under various changes occurring in the three-phase transmission line.

6 Conclusion

This paper explains about the implementation of new control method, i.e. Adaptive PI Control for STATCOM model for improvement of voltage stability in the power system. In this paper, the simulation results of the behaviour of

three-phase test system without the STATCOM, with the STATCOM and with Adaptive PI Control has been observed. The results obtained shows that that three-phase test system model in presence of STATCOM improves stability of the power system by improving voltage profile but it has been observed that the voltage profile has distortions due to the hit and trial approach of the control parameters (PI gains) in the STATCOM model, whereas, the three-phase test system model with Adaptive PI Controller shows almost smooth voltage profile which ensures negligible distortion in voltage value. Therefore, adaptive controller-based STATCOM model with requisite control action improves stability of AC system.

References

1. Jaswani, M., Bharti, S., Dubey, S.P.: A study of reactive power compensation in transmission system. Int. J. Adv. Eng. Res. Stud/IV/II/Jan.–March **351**, 353 (2015)
2. Hingorani, N.G., Gyugyi, L.: Understanding FACTS: Concepts and Technology of Flexible AC Transmission Systems. Wiley-IEEE press (2000)
3. Ajitha, A., Mutharasan, A., Dhal, P.K.: Power quality improvement using unified power flow controller in matrix converters for WECS. Int. J. Appl. Eng. Res. **10**(76), (2015)
4. SajediHir, M., Hoseinpoor, Y., MosadeghArdabili, P., Peerzade, T.: Analysis and simulation of a STATCOM for a midpoint voltage regulation of a transmission line. Aus. J. Basic Appl. Sci. (2011). ISSN: 1991-8178
5. Xu, Y., Li, F.: Adaptive PI control of STATCOM for voltage regulation. IEEE Trans. Power Delivery **29**(3), 1002–1011 (2014)
6. Tapia, A., Tapia, G., Ostolaza, J.X., Saenz, J.R.: Modeling and control of a wind turbine driven doubly fed induction generator. IEEE Trans. Energy Convers. **18**(2), 194–204 (2003)
7. Iqbal, A., Lamine, A., Ashraf, I.: MATLAB/SIMULINK model of space vector PWM for three-phase voltage source inverter. In: Proceedings of the 41st International Universities Power Engineering Conference (vol. 3, pp. 1096–1100). IEEE (2006)

Defect Detection in Power Electronic Circuits by Artificial Neural Network Using Discrete Wavelet Analysis

Dibyendu Khan, Sankhadip Saha, Shiladitya Saha and Subhrodipto Basu Choudhury

Abstract Power electronics occupies a major section of industrial drives and systems in terms of power converter and nonlinear circuits for running and controlling three-phase or single-phase machine. Three-phase controlled rectifier and inverter are the most important analog circuit in power electronics. These circuits have also gained immense importance in modern grid-connected system synchronized with renewable energy sources. In this context, it requires maximum attention for smooth operation of these devices at minimum recovery time during faulty condition. And hence detection of faulty component during running condition becomes extremely important. Considering these particulars, this paper presents a proficient defect-oriented parametric test method for two power electronic circuits like three-phase rectifier and inverter based on artificial neural network using discrete wavelet decomposition as preprocessor for feature extraction. Two types of feed forward neural network such as BPMLP and PNN are employed here for fault event detection. Results are found to be very promising with utmost of 99.95%.

Keywords Power electronic circuit · Fault detection · Wavelet transform BPMLP · PNN

D. Khan (✉) · S. Saha · S. Saha · S.B. Choudhury
Department of Electrical Engineering, Netaji Subhash Engineering College, Kolkata, India
e-mail: dibyendukhan001@gmail.com

S. Saha
e-mail: imsankhadip@gmail.com

S. Saha
e-mail: shiladityasaha282@gmail.com

S.B. Choudhury
e-mail: bumbadit@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_47

1 Introduction

With the advancement of automation technology, device condition monitoring for fault detection is now an essential criterion for smooth and efficient operation in the industry. Since power electronic circuit topology is used everywhere, condition monitoring for fault event detection also becomes very important for quick recovery as well as replacement of faulty components as quick as possible. IC Technology Both electrical and electronic circuits are subjected to several disturbances whose presence may damage the circuits. So, the preventive measures are needed to be taken to protect the power electronic circuits. Technically speaking, this type of disturbances may damage the doping concentration of semiconductor devices used in power electronic circuits. Industry requires a fail-safe operation of various vital power electronic circuits, and hence this necessitates the way to detect the type of faults that usually occurs in the circuit. Most of the common types of faults in power electronic circuits are short circuit fault and open circuit fault which may occur due to break of thyristor or MOSFET or IGBT. The main fault detection methods of circuit elements are spectrum analysis method, terminal voltage and current detection method, dictionary library diagnose method which require substantial amount of time and expert knowhow. In [1], authors attempts to detect the type of fault by using classification methodologies. They use artificial neural network to classify the fault. Wavelet decomposition technique is used to extract features and also to reduce the dimension of features matrix to train the neural network so that the fault category can be recognized in future. This method achieves a classification accuracy of 98%. Coming years witness method out forth on classification of faults in nonlinear circuits [2]. Wavelet transformation technique is used to extract some relevant features pertaining to distinct fault occurring in electronic circuit. The detection methodology classifies the fault with an accuracy of 90%. In [3], fault detection is employed in controlled rectifier by employing Support Vector Machine (SVM). They use two types of features as the average voltage of the output voltage waveform and area under the voltage signal to train the support vector machine. This method classified the fault with acceptable accuracy. They used two types of features as the average voltage of the output voltage waveform and area under the voltage signal to train the support vector machine. This method classified the fault with accuracy of 95%. In [4], fractional wavelet transform (FWT) is used to extract features. These features are fed to fuzzy-based support vector machine to train using maximum cluster distance by Kernel Fuzzy C-means (KFCM). It reaches a fault classification accuracy of 98%. S-transform is used in [5] for feature extraction in power electronic circuit. Support vector machine (SVM) was employed to detect the type of fault occurring in power electronic circuit. They also checked their classification accuracy using principal component analysis (PCA). The method has classification accuracy of 97%. In [6], authors use SVM method to classify the fault of grid-connected T-type rectifier with unity power factor. It has a classification accuracy of 98%.

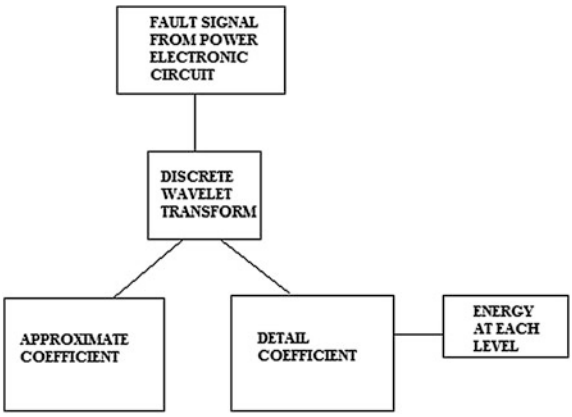


Fig. 1 Feature extraction using DWT

2 Feature Extraction Using Discrete Wavelet Transform

Modern simulation tool is used to set up an electronic circuit. Here a specific application of rectifier and inverter is used to show that fault due to sudden opening and closing of electronic switches can be detected and preventive measures can be taken. Earlier attempt by researchers uses several feature extraction techniques like Fast Fourier transform (FFT), S-transform (ST) and wavelet transform (WT), etc. This paper presents a new technique of discrete wavelet transform (DWT) to extract relevant and distinct features suitable to classify the fault event. It has been observed that there is better classification accuracy on increasing the level of discrete wavelet decomposition. Wavelet decomposition uses the concept of mother wavelet on which the fault signal is decomposed. There are several mother wavelets but in this research 'db4' mother wavelet is used. The fault signal has been decomposed into twelve levels and at each level energy for that level is extracted. At each level, detailed level and approximate level coefficients are decomposed. Combined energy of both approximate and detailed level are also computed. Thus, each signal has twelve different features pertaining to twelve levels. The method of decomposition and feature extraction technique is given in Fig. 1.

3 Fault Classification Techniques

The features extracted from fault signals being distinct they can be easily classified. Classification is required in order to gather some knowledge about the type of fault. Classification is helpful as they help us to take preventive measures on occurrence of a specific fault and hence to protect electrical instruments from hazards. Several methods are used to classify the fault. Here two different classification methods are employed to distinguish different type of fault. Two types of neural network—

multilayer perceptron and probabilistic neural network (PNN), are applied here. Multilayer perceptron also known as artificial neural network (ANN) is a family of cognitive learning feed forward model which is employed to predict a certain outcome. ANN is dependent on a large number input functions. ANN model is layered structure consisting of input layer, hidden layer consisting of neurons and the last output layer. All the layers are interconnected with each other, however they avoid intra connection. The connections have numeric weights that can be tuned based on experience, making neural nets adaptive to inputs and capable of learning. Neural network is a statistical feed forward model used for classification purposes. The term "neural network" usually refers to models employed in statistics, cognitive psychology and artificial intelligence.

3.1 Multilayer Perception (MLP)

Multilayer perceptron is anticipated for soft computation simulated by neural network in the field of machine learning. It estimates functions which depend on huge number of unidentified inputs. Hence MLP is a neural network used to plot input data set into the output dataset. The MLP configuration has three neuron layers, which are input layer, transitional layer and hidden or output layer correspondingly. Every single neuron of the layers is connected with others but not with itself (Fig. 2).

3.2 Probabilistic Neural Network (PNN)

Probabilistic neural network is another class of neural network which is based on kernel function. PNN has four layers, namely, input layer, pattern layer, summation layer and output layer. With context to real time electrical disturbance classification

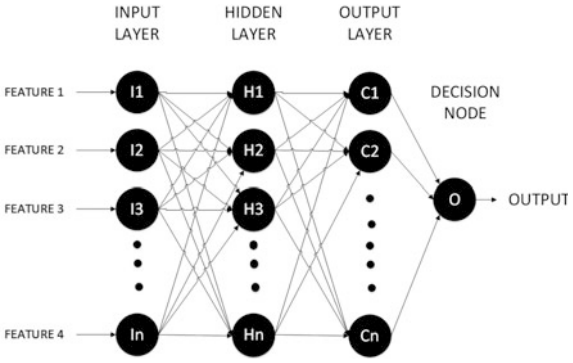


Fig. 2 Artificial neural network

PNN has been found to be more effective than conventional error back propagation-based neural networks. In order to assign a feature vector $f \in F_m$, amongst predefined classes, the conditional density P (f|Ck) of each class Ck is projected since it represents the improbability associated to a class attribution. They are combined according to Bayes theorem that makes optimal decision. Conditional density estimation is achieved by implementation of Parzen window. It can be viewed as a sphere of influence $p(s, x)$ around each sample, i.e. input point s and to add them up for each of the k classes at the summation layer using the expression $P\ (x|C) = p(s, x)$, $p\ (s, x) = \exp\ (-\|x - s\|2/2s\ 2)$, where the only complimentary parameter is the width (σ) of the Gaussians.

4 Results and Analysis

In order to validate the fault detection scheme, two power converter circuits are experimentally tested using MATLAB simulation, i.e. the first one is the three-phase rectifier circuit and the second is the three-phase inverter. Totally, 13 classes of signal are considered in this work, out of which one represents the normal class, i.e. the healthy signal and the remaining twelve fault classes includes six short circuit faults and six open circuit faults for each case under consideration. Both the converter circuit is constructed using power MOSFET. A three-phase full bridge-controlled rectifier and three-phase full bridge-controlled inverter is shown in Figs. 3 and 4 individually. Simulated fault is created by opening or connecting the two terminals of a particular MOSFET for the open circuit and the short circuit fault, respectively. In case of rectifier circuit, random samples are generated by varying the three-phase ac source from its base value, i.e. 100 V_{ac} in the range of

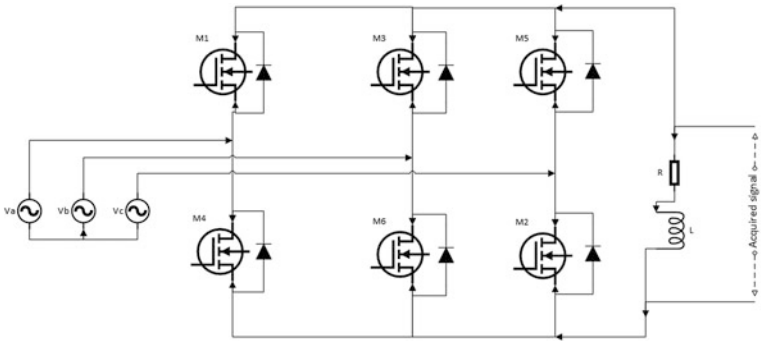


Fig. 3 Three-phase full bridge-controlled rectifier

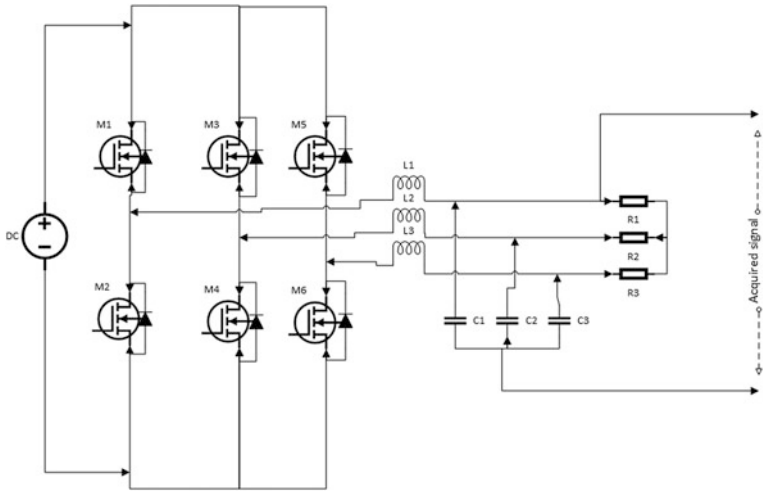


Fig. 4 Three-phase full bridge-controlled inverter

95–105 V_{ac}. The same range is also considered for the inverter dc source. Figure 5 reflects the 2-D plot of every class including normal condition and fault conditions. For both the cases, training to testing data ratio is 60:40. Thus, 780 samples are used for training and 520 samples are used for testing purpose. Since injection of noise into the signal in real time condition is an inescapable fact, so the performance of the proposed scheme is judged with the different level of noise contamination in the signal. In this respect, samples are generated using 60, 50, 40, 30 and 20 dB white Gaussian noises. Amongst the daubechies family of wavelets, 'db_4' is used here with 12 level of decomposition considering the 5 kHz sampling frequency. Energy, as a feature, is computed for 12 detailed coefficients at each level of decomposition. Feed forward based multilayer perceptron, trained with the back-propagation algorithm based on the Levenberg–Marquardt algorithm, is implemented here to train the feed forward neural network with mean square error as performance criteria for the network. Input neurons of BPMLP signify the number of features whereas output of MLP represents the 12-fault class or event. Number of neurons in the hidden layer of the network is optimized and found to be 10 by trial and error for best performance. The above algorithm is coded in MATLAB simulation environment. Table 1 displays the comparison of the results for each fault cases according to the classifier.

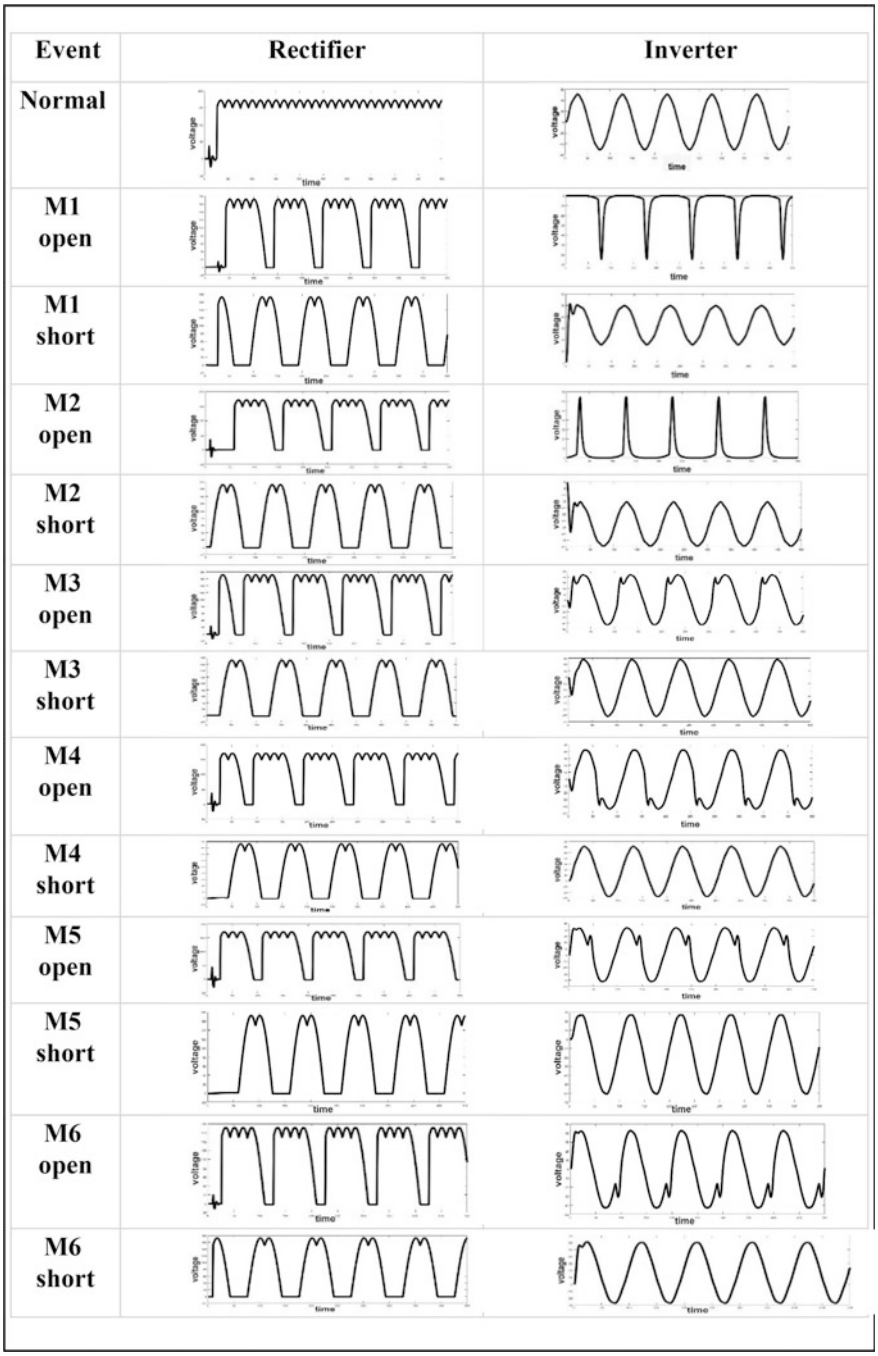


Fig. 5 Voltage waveforms for different fault conditions

Table 1 Classification result for the tested signals

Event	Classification performance				
	Classifier	50 dB	40 dB	30 dB	20 dB
Normal	BP-MLP	100	99.81	99.00	97.00
	PNN	100	99.62	98.99	98.00
T1 open	BP-MLP	99.98	99.70	98.88	97.21
	PNN	100	99.80	98.78	96.56
T1 short	BP-MLP	99.82	99.72	98.50	97.50
	PNN	100	99.75	98.89	97.05
T2 open	BP-MLP	99.98	99.55	98.01	97.62
	PNN	99.90	99.72	99.00	96.98
T2 short	BP-MLP	99.92	99.60	98.50	97.64
	PNN	99.89	99.71	97.67	96.45
T3 open	BP-MLP	99.90	99.60	98.01	97.89
	PNN	99.95	99.55	98.05	97.56
T3 short	BP-MLP	99.98	99.67	98.00	97.02
	PNN	100	99.01	99.01	97.01
T4 open	BP-MLP	99.95	99.65	98.55	97.00
	PNN	100	99.32	97.56	97.00
T4 short	BP-MLP	99.95	99.72	98.23	97.05
	PNN	99.92	99.50	97.99	96.87
T5 open	BP-MLP	99.98	99.70	98.56	97.06
	PNN	99.95	99.51	98.59	96.77
T5 short	BP-MLP	99.97	99.67	98.23	97.08
	PNN	99.98	99.32	98.23	97.06
T6 open	BP-MLP	99.98	99.65	98.50	97.64
	PNN	99.87	99.60	98.56	97.69
T6 short	BP-MLP	99.99	99.55	98.50	97.72
	PNN	99.91	99.45	98.78	97.60
All event	BP-MLP	99.95	99.66	98.42	97.34
	PNN	99.95	99.52	98.46	97.12

5 Conclusion

This paper focuses on the intelligent detection of faulty circuit component using complex signal processing method like discrete wavelet transform (DWT) and artificial neural network as detection technique. Simulation results show superior classification performance for immediate and efficient faulty event detection. It is also found that significance performance is achieved with respect to noisy condition. This is because of selection of proper wavelet using ‘db4’ due to the fact that scaling function of ‘db4’ approximately resembles the faulty waveform during transient response. The same fault detection scheme can be utilized for other power

electronic converter circuits. On the other hand, various statistical machine learning techniques like support vector machine, extreme learning machine and decision trees may be applied as classifier to reduce the training time of the neural network.

References

1. Stopjakova, V., Malosek, P., Matej, M., Nagy, V., Margala, M.: Defect detection in analog and mixed circuits by neural networks and wavelet analysis. IEEE Trans. Reliab. **54**(3), 441–448 (2005)
2. Shirong, Y., Gangju, C., Yongle, X.: Wavelet neural network based fault diagnosis in non-linear analog circuits. J. Syst. Eng. Electron. **17**(3), 521–526 (2006)
3. Hong-da, L., Wen-jie, Y., Hai, L., Dian, H.: Fault diagnosis method in controlled retifier based on support vector machine,. In: Second WRI Global Conference on Intelligent Systems. pp. 235–238 (2010)
4. Luo, H., Wang, Y., Cui, J.: A SVDD approach of fuzzy classification for analog circuit fault diagnosis with FWT as preprocessor. Expert Syst. Appl. **38**, 10554–10561 (2011)
5. Wang, R., Zhan, Y., Zhou, H.: Application of S transform in fault diagnosis of power electronics circuits. Scientia Iranica D **3**, 721–726 (2012)
6. Lee, J.S., Lee, K.B.: An open-switch fault detection method and tolerance controls based on SVM in a grid-connected T-type rectifier with unity power factor. IEEE Trans. Ind. Electron. **61**(12), 7092–7104 (2014)

Stability of Two-Dimensional Systems Using Single Square Matrix

P. Ramesh and K. Vasudevan

Abstract This article presents a new and easy unified way to investigate the stability of 2-D linear systems. The 2-D characteristics equation is regenerate into a similar one-dimensional characteristic polynomial. Using the coefficient of the equal one-dimensional characteristic polynomial, a new technique had proposed to create a single square matrix to check the sufficient conditions for stability analysis. To determine the stability square matrix should have the positive inner wise for all determinants starting from the middle elements and continuing outward up to the integrated matrix are positive. The illustrative examples prove the simplicity and application of the suggested method.

Keywords Necessary condition · Sufficient condition · Inner determinants
Linear discrete systems · Square matrix · Two-dimensional (2-D)

1 Introduction

The aspire of 2-D algorithmic numerical filters has received the attention of the many analysis employees [1], because of their wide application in many areas of aerial and satellite image graphs, Communication and geo physics, Medical X-rays and digital pictures in pattern recognition applications. A class of two-dimensional systems can

P. Ramesh (✉)
Department of EEE, University College of Engineering,
Anna University, Ramanthapuram, Tamil Nadu, India
e-mail: rameshucermd@gmail.com

K. Vasudevan (✉)
Department of EEE, Sriram Engineering College,
Chennai, Tamil Nadu, India
e-mail: vasudevank1978@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_48

be effectively implemented using recursive structure. For a given response characteristic, recursive digital filters have less hardware requirements. But the stability constrains related to design of such filters may be a major drawbacks [2]. The reason is that incorporation stability constrains in the design stage is computationally very difficult and hence it would be extremely desirable to have technique by which the stability problem could be separated from the design problem. The stability of the designed filter is guaranteed by stabilization. Some real-time systems are inherently unstable and to stabilize the unstable physical system, a controller can be designed.

Thus the stability analysis and stabilization are the most vital and necessary tasks that ought to be considered in linear system dissection and purport. The system analyzer and designer must have a simple procedure to analyze stability of the given system, among the various algorithms. In this paper, we proposed a direct and straightforward technique to check the sufficient conditions for stability of 2-D characteristics polynomial by the formation of single square matrix [S] and also the inner determinants were determined by the Jury inner methodology to check the stability, which is helpful for numerical testing of stability and for the design of linear systems together with one necessary condition [3, 4].

2 Literature Survey

The stability dissection is that the eminently significant check that should be thought about in LTIDS inquiry and purport. So that stability perception is extremely vital. Therefore several analyses have been conducted to establish the stability in previous couple of years. Several theorems have proposed for characteristics roots of matrix lie within the unit circle, new method has proposed to avoid bilinear transformation to get fullers theorem directly with less computational significance were discussed in [4]. Bistriz [5] had introduced the efficient stability task a look at that involves real univariate polynomials and real numeric solely, It conjointly test the doubling degree technique within the development of 2-D stability tests were discussed in [6]. The attainable root locations of 2-D polynomials were projected in [7] have proved the essential necessitate of obtained from the polynomial and additionally obtained the stability inside the unit circle. A replacement methodology to reason the stability margin of 2-D continuous systems was provided in [8, 9].

For finding the stability of 2-D filters, a new simple procedure were proposed compared to huang's and shanks method by avoiding the bilinear transformation components of huang's method [10]. The obtained results in [11] evidenced that double bilinear transformation does not conserve the stability in either direction. The algorithm in [12] analyze the positive definiteness of an absolute quadratic form was expressed in terms of inner wise range. The imperative and tolerable conditions are used to form the inner determinant matrix mentioned in [13].

References [14, 15] have revealed new procedure to determine whether bivariate polynomial had no zeros in the closed exterior of the unit circle with low count of operations. Reference [16] shows a procedure to test the stability of finite assortment of real in variant polynomials by a particular changed form of single dimensional stability obtained by telepolation of two-dimensional tabulation tests. The suitable distinctions between the one and two-dimensional test cases were given in [17]. The stability of 2-D recursive filters in the frequency domain has discussed in [18] and simplified version of shanks stability theorem were derived. The reduction method [19] which reduces nonlinearity from m-D equation to 1-D equation, stability of 1-D is ample for stability of m-D system. This method provides less number of prohibitive conditions. In [20] a new modified form of criterion for asymptotic stability of two- dimensional system using Roesser model were developed. In [21] stability robustness analysis performed in the space of markov parameters using corner points for positive definiteness which reduces the more computational tasks. In [22] a new algorithm was proposed to obtain the root distribution of a polynomial with respect to unit circle in z-plane.

3 Existing Method

The two-dimensional (2-D) linear systems [10] in transfer function form as follows:

$$H(Z_1, Z_2) = \frac{A(Z_1, Z_2)}{B(Z_1, Z_2)} \tag{1}$$

where A and B non-cancellable polynomials in Z_1 and Z_2.

Regularly, the stability condition is expressible by the accompanying two conditions on a two variable polynomial [23] $B\ (s_1, s_2)$ as

(a) $B(s_1, 1) \neq 0 \quad \mathrm{Re}\, s_1 \geq 0$
(b) $B(s_1, s_2) \neq 0 \quad s_1 = jw, \mathrm{Re}\, s_2 \geq 0$

and the discrete case given [24] as

$$B(z_1, 0) \neq 0 \quad |z_1| \geq 1$$

$$B(z_1, z_2) \neq 0 \quad |z_1| = 1, |z_2| \geq 1$$

Testing the condition (a) for stability checking of a variable polynomial with real coefficients is simple. To check conditions of (b) involves a lot of complications involves to test the stability of a one-variable polynomial with complex coefficients

[25]. To avoid more complication of the above said method, we proposed a new method to check the sufficient condition in stability analysis of two-dimensional system (2-D) as follows.

4 Proposed Method

In general the following form can also be chosen:

$$B(Z_1, Z_2) = T_0(Z_1)Z_2^n + T_1(Z_1)Z_2^{n-1} \cdots + T_n(Z_1) = 0 \tag{2}$$

The reciprocals of Z_1 and Z_2 are $\left(\frac{1}{Z_1}\right)$ and $\left(\frac{1}{Z_2}\right)$ respectively, which is utilized in such a way, so that the Eq. (2) is rewritten as:

$$B\left(\frac{1}{Z_1}, \frac{1}{Z_2}\right) = T_0\left(\frac{1}{Z_1}\right)\left(\frac{1}{Z_2}\right)^n + T_1\left(\frac{1}{Z_1}\right)\left(\frac{1}{Z_2}\right)^{n-1} \cdots + T_n\left(\frac{1}{Z_1}\right) = 0 \tag{3}$$

Again equation is represented as

$$\begin{aligned} M(Z_1, Z_2) \quad &= F(x) = 0 \\ &Z_1 = Z_2 = x \end{aligned} \tag{4}$$

Let

$$F(x) = a_n x_n + a_{n-1} x_{n-1} + \cdots + a_0 = 0 \tag{5}$$

The postulate indispensable conditions for stability were established as follows: When 'n' is even:

(i) $f(1) > 0$
(ii) $f(-1) > 0$ and
(iii) $\left|\frac{a_0}{a_n}\right| < 1$

When 'n' is odd:

(i) $f(1) > 0$
(ii) $f(-1) < 0$ and
(iii) $\left|\frac{a_0}{a_n}\right| < 1$

The Jury sufficient test is carried out as follows:

Utilizing the coefficients of $f(x)$ two triangular matrices were formed by left and right shifting the coefficient

$$[t_1] = \begin{pmatrix} a_n & a_{n-1} & a_{n-2} & . & . & . & a_0 \\ 0 & a_n & a_{n-2} & . & . & . & . \\ 0 & 0 & a_n & . & . & . & . \\ 0 & 0 & 0 & a_n & . & . & . \\ . & . & . & . & . & . & . \\ . & . & . & . & . & . & . \\ . & . & . & . & . & . & a_n \end{pmatrix} \tag{6}$$

$$[t_2] = \begin{pmatrix} a_n & a_{n-1} & a_{n-2} & . & . & . & a_0 \\ a_{n-1} & a_{n-2} & a_{n-3} & . & . & . & 0 \\ a_{n-2} & a_{n-3} & 0 & . & . & . & 0 \\ . & . & . & . & . & . & 0 \\ . & . & . & . & . & . & 0 \\ . & . & . & . & . & . & 0 \\ a_0 & 0 & 0 & . & . & . & 0 \end{pmatrix} \tag{7}$$

From (t_1) and (t_2), we construct $[S_1]$ by adding (t_1) and (t_2) and we construct $[S_2]$ subtracting (t_1) and (t_2).

$$[S_1] = [t_1] + [t_2] \tag{8}$$

$$[S_2] = [t_1] - [t_2] \tag{9}$$

For the system to be absolutely stable, $[S_1]$ and $[S_2]$ must be positive inner wise, with all the determinants from the middle element(s) and continuing out wards to the entire matrix are positive Jury [11]. This method consumes more arithmetic operations and time, computational cost also very high. Hence, we go to following proposed method to test the sufficient condition of the given system by direct formation of Single Square matrix [S].

Proposed method to check the sufficient condition:

Consider the following one-dimensional characteristic equation.

$$a_4z^4 + a_3z^3 + a_2z^2 + a_1z + a_0 = 0$$

$$[S] = \begin{bmatrix} a_4 & a_3 & a_2 & a_1 & a_0 \\ a_3 & a_4 + a_2 & a_3 + a_1 & a_2 + a_0 & a_1 \\ a_2 & a_1 & a_0 + a_4 & a_3 & a_2 \\ a_1 & a_0 & 0 & a_4 & a_3 \\ a_0 & 0 & 0 & 0 & a_4 \end{bmatrix}$$

The above single square matrix [S] has formed to check the sufficient condition of the given system which has formed as follows: In the fifth column, the coefficient

of the characteristics is entered in ascending order. First, column was formed by entering the coefficient in descending order, The second row has formed by adding alternate coefficient of the first row. The fourth column and second has formed by one shifting up word by fifth and first column, respectively, and third was formed by two shifting upward the fifth column and first column. The single square matrix [S] should be positive inner wise for all the determinants beginning from the centre elements and continuing outward up to the entire matrix were positive

5 Illustrations

Example 1:

$$B(Z_1Z_2) = 1 + 0.5Z_2 + 0.25Z_2^2 + 0.5 + 0.25Z_2Z_1 + 0.25Z_1^2$$

Equivalent one-dimensional characteristic equation by inverting variables Z_1 and Z_2 and equate $Z_1 = Z_2 = X$

$$F(X) = 1.5X^2 + 0.5X + 0.75$$

Necessary condition:

$$F(1) = 1.5 + 0.5 + 0.75 = 2.75 > 0 \quad \text{(Satisfied)}$$
$$F(-1) = 1.5 - 0.5 + 0.75 = 1.75 > 0 \quad \text{(Satisfied)}$$

Sufficient test by Jury method:

$$F(X) = 1.5x^2 + 0.5x + 0.75 = 0$$

$$X = \begin{bmatrix} 1.5 & 0.5 \\ 0 & 1.5 \end{bmatrix}$$
$$Y = \begin{bmatrix} 0.5 & 0.75 \\ 0.75 & 0 \end{bmatrix}$$

$$[X + Y] = \begin{bmatrix} 2 & 1.25 \\ 0.75 & 1.5 \end{bmatrix}$$
$$[X - Y] = \begin{bmatrix} 1 & 0.25 \\ 0.75 & 1.5 \end{bmatrix}$$

$$X + Y = 2.0625 > 0 \quad \text{(Satisfied)}$$
$$X - Y = 1.3125 > 0 \quad \text{(Satisfied)}$$

System is stable.

Proposed method for sufficient test:

$$\begin{bmatrix} 1.5 & 0.5 & 0.75 \\ 0.5 & 2.25 & 0.5 \\ 0.75 & 0 & 1.5 \end{bmatrix}$$

$$\nabla_1 = 2.25 > 0 \quad \text{(Satisfied)}$$
$$\nabla_3 = 3.609 > 0 \quad \text{(Satisfied)}$$

The proposed method to test sufficient conditions which consumes less arithmetic operation compare to Jury sufficient condition [11] test. The given system fulfills one and the other imperative and tolerable conditions. Consequently the given system is stable.

Example 2:

$$B(Z_1Z_2) = \left(12 + 10Z_1 + 2Z_1^2\right) + \left(6 + 5Z_1Z_1^2\right)Z_2$$

Equivalent one-dimensional characteristic equation by inverting variables Z_1 and Z_2 and equate $Z_1 = Z_2 = X$

$$F(X) = 12X^3 + 16X^2 + 7X + 1$$

Necessary condition:

$$F(1) = 12 + 16 + 7 + 1 = 36 > 0 \quad \text{(Satisfied)}$$
$$F(-1) = -12 + 16 + 7 + 1 = -2 < 0 \quad \text{(Satisfied)}$$

Sufficient test by Jury method:

$$F(x) = 12x^3 + 16x^2 + 7x + 1 = 0$$

$$X = \begin{bmatrix} 12 & 14 \\ 0 & 12 \end{bmatrix}$$
$$Y = \begin{bmatrix} 7 & 1 \\ 1 & 0 \end{bmatrix}$$

$$[X+Y] = \begin{bmatrix} 19 & 17 \\ 1 & 12 \end{bmatrix}$$
$$[X-Y] = \begin{bmatrix} 5 & 15 \\ 1 & 12 \end{bmatrix}$$

$$X+Y = 211 > 0 \quad \text{(Satisfied)}$$
$$X-Y = 12 > 0 \quad \text{(Satisfied)}$$

System is stable.

Proposed method to test the sufficient conditions:

$$\begin{bmatrix} 12 & 16 & 7 & 1 \\ 16 & 19 & 17 & 7 \\ 7 & 1 & 12 & 16 \\ 1 & 0 & 0 & 12 \end{bmatrix}$$

$$\nabla_2 = 211 > 0 \quad \text{(Satisfied)}$$
$$\nabla_4 = 5400 > 0 \quad \text{(Satisfied)}$$

The disposed system fulfills the pair mandatory and plentiful conditions. Consequently the given system is stable, also the proposed method to test the sufficient conditions which consumes less arithmetic operation compared to Jury [11] method.

Example 3:

$$D(Z_1, Z_2) = 1 - 1.2Z_2 + 0.3Z_2^2 - 1.5Z_1 + 1.8Z_1Z_2 - 0.75Z_1Z_2^2 + 0.6Z_1^2 - 0.72Z_1^2Z_2 + 0.29Z_1^2Z_2^2$$

Equivalent one-dimensional characteristic equation by inverting variables Z_1 and Z_2 and equate $Z_1 = Z_2 = X$

$$F(X) = X^4 - 2.7X^3 + 2.7X^2 - 1.47X + 0.29$$

Necessary condition:

$$F(1) = 1 - 2.7 + 2.7 - 1.47 + 0.29 = -0.18 < 0 \quad \text{(Not satisfied)}$$
$$F(-1) = 1 + 2.7 + 2.7 + 1.47 + 0.29 = 8.16 > 0 \quad \text{(Satisfied)}$$

Sufficient test by Jury method:

$$F(X) = x^4 - 2.7x^3 + 2.7x^2 - 1.47x + 0.29 = 0$$

$$X = \begin{bmatrix} 1 & -2.7 & 2.7 \\ 0 & 1 & -2.7 \\ 0 & 0 & 1 \end{bmatrix}$$

$$Y = \begin{bmatrix} 2.7 & -1.47 & 0.29 \\ -1.47 & 0.29 & 0 \\ 0.29 & 0 & 0 \end{bmatrix}$$

$$X + Y = \begin{bmatrix} 3.7 & -4.17 & 2.99 \\ -1.47 & 1.29 & -2.7 \\ 0.29 & 0 & 1 \end{bmatrix}$$

$$X - Y = \begin{bmatrix} 1.7 & -1.23 & 2.41 \\ -1.47 & 0.71 & -2.7 \\ 0.29 & 0 & 1 \end{bmatrix}$$

$$X + Y = 0.789 > 0 \quad \text{(Satisfied)}$$
$$X - Y = -0 > 0 \quad \text{(Not satisfied)}$$

System is unstable.

Proposed method to test the sufficient conditions:

$$\begin{bmatrix} 1 & -2.7 & 2.7 & -1.47 & 0.29 \\ -2.7 & 3.7 & -4.17 & 2.99 & -1.47 \\ 2.7 & -1.47 & 1.29 & -2.7 & 2.7 \\ -1.47 & 0.29 & 0 & 1 & -2.7 \\ 0.29 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\nabla_1 = 1.29 > 0 \quad \text{(Satisfied)}$$
$$\nabla_3 = 0.790 > 0 \quad \text{(Satisfied)}$$
$$\nabla_5 = -0.197 < 0 \quad \text{(Not satiesfied)}$$

The inured system not satisfied the twain crucial and acceptable conditions. Hence the given system is unstable, also the proposed method to test the sufficient conditions which is very simple compared to Jury test [11].

6 Conclusion

A new stability test of two-dimensional linear systems has been presented in this paper. Various approaches to test stability of 2-D system have been studied. The proposed strategy used to check the adequate condition to find the stability of 2-D linear system using single square matrix [S], which is exponentially straightforward and expends less number of arithmetic operations and reduced computational costs when contrasted with jury [11] proposed techniques for analyze the stability in 2-D linear systems.

References

1. Prasad, K.P., Reddy, P.S.: Method for designing stable 2-D digital filters. IET Electron. Lett., 385–386 (1997)
2. Ramesh, P.: Stability analysis of multi-dimensional linear system and root distribution using sign criterion with real co-efficient. Circ. Syst., 100–109 (2016)
3. Ramesh, P.: Stability analysis of multi-dimensional linear time invariant discrete system within the unity shifted unit circle. Circ. Syst., 709–717 (2016)
4. Jury, E.I., Gutman, S.: On the stability of the a matrix inside the unit circle. In: IEEE Transaction on Automatic Control, pp. 533–535 (1975)
5. Bistriz, Y.: Immediate and telepolation-based procedures to test stability of continuous-Discrete bi-variate Polynomials. IEEE Trans. Circ. Syst. **3**, 293–296 (2004)
6. Bisttritz, Y.: Testing stability of 2-D discrete systems by a set of real 1-D stability tests. IEEE Trans. Circ. Syst. I Regul. Pap. **51**(7), 1312–1320 (2004)
7. Khargoneker, P.P., Bruce Lee, E.: Further results on possible root locations of 2-D polynomials. IEEE Trans. Circ. Syst. **33**(5), 566–569 (1986)
8. Mastorakis, N.E.: A method for computing the 2-D stability margin. IEEE Trans. Circ. Syst. II, Anal. Digit. Signal Process. **45**(3), 376–378 (1998)
9. Anderson, B.D.O., Jury, E.I.: A simplified Schur–Cohn test. IEEE Trans. Autom. Control **31**, 157–163 (1973)
10. Anderson, B.D.O., Jury, E.I.: Stability test for two-dimensional recursive filter. IEEE Trans. Audio Electro Acoustics **21**, 366–372 (1973)
11. Jury, E.I., Bauer, P.: On the stability of two-dimensional continuous systems. IEEE Trans. Circ. Syst. **35**(12), 1487–1500 (1988)
12. Bose, N.K., Jury, E.I.: Inner algorithm to test for positive definiteness of arbitrary binary forms. IEEE Trans. Autom. Control, 169–170 (1975)
13. Jury, E.I.: "Inners" approach to some problems of system theory. IEEE Trans. Autom. Control **16**(3), 223–240 (1971)
14. Bistritz, Y.: Stability testing of 2-D Discrete linear systems by telepolation of an immittance—type tabular test. IEEE Trans. Circ. Syst. I: Fundam. Theor. Appl. **48**(7), 840–846 (2001)
15. Ahmed, A.: On the stability of two-dimensionaldiscrete systems. IEEE Trans. Autom. Control **25**(3), 551–552 (1980)
16. Jury, E.I.: A note on the analytical absolute stability test. In: Proceeding of the IEEE, pp. 823–824 (1970)
17. Goodman, D.: Some stability properties of two-dimensional linear shift-invariant digital filters. IEEE Trans. Circ. Syst. **24**(4), 201–208 (1977)
18. Huang, T.S.: Stability of two-dimensional recursive filters. IEEE Trans. Audio Electro Acoust. **20**(2), 158–163 (1972)

19. Bauer, P., Jury, E.I.: Stability analysis of multi-dimensional (M-D) direct realization digital filters under the influence of nonlinearities. IEEE Trans. Acoust. Speech Signal Process. **36** (11), 1770–1780 (1988)
20. Singh, V.: New approach to stability of 2-D discrete systems with state saturation. Sci. Direct Signal Process. **92**, 240–247 (2012)
21. Katbab, A., Jury, E.I., Mansour, M.: On robust Schur property of discrete time polynomials. IEEE Trans. Circ. Syst. I: Fundam. Theor. Appl. **39**(6), 467–470 (1992)
22. Kamat, P.S., Zwass, M.: On zero location with respect to the unit circle of discrte-time linear systems polynomials. Proc. IEEE **73**(11), 1686–1687 (1985)
23. Zhang, C.: The application of 2-D numerical inversion of laplace transform. In: IEEE 9th International Conference on Signal Processing (2008)
24. Najim, M.: A slice based 3-D Schur Cohn stability criterion. In: IEEE International Conference on Acoustics Speech and Signal Processing (ICASSP 07) (2007)
25. Jury, E.I.: Stability tests for one-two and multi-dimensional linear system. In: IET Proceedings of the Institution of Electrical Engineers, vol. 124, pp. 1237–1240 (1977)

Multidimensional Linear Discrete System Stability Analysis Using Single Square Matrix

P. Ramesh and K. Vasudevan

Abstract This paper reviews to search out the stability of multidimensional linear time invariant discrete system; the system, which is portrayed within the forms of the individual characteristic equation. Besides an equivalent one-dimensional equation is created from the multidimensional characteristic equation, a replacement method has planned for construction single square matrix using the coefficient of equivalent one-dimensional characteristic equation and determinants were evaluated using Jury's idea. The proposed procedure for construction of single square matrix is compared to Jury's matrix formation that is incredibly simple and direct and consumes less arithmetic operations. This approach is delineated utilizing numerous numerical illustrations.

Keywords Characteristics equation · Coefficient · Multidimensional Single square matrix · Sufficient conditions

1 Introduction

In recent years, multidimensional (m-D) digital filters is receiving appreciable attention in sight of the emerging widespread applications, such as digital filtering, image processing, video processing, seismic processing, bio-medical signal processing, control, etc. There are various general testing strategy accessible in the literature [1]. In advanced control system, the stability assumes a truly definitive part inside the execution of the system. Hence, system stability ought to be considered though determinant the system performance as to various design criteria

P. Ramesh (✉)
Department of EEE, University College of Engineering, Anna University, Ramanathapuram, Tamil Nadu, India
e-mail: rameshucermd@gmail.com

K. Vasudevan
Department of EEE, Sriram Engineering College, Chennai, Tamil Nadu, India
e-mail: vasudevank1978@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_49

along these lines this paper is intended to build up another plan for the analysis, design and stabilization of multidimensional linear time invariant discrete system using the terribly efficient changed Jury's inner wise determinant criterion referred in Jury [2] together with ample condition by the formation single square matrix [*S*] and necessary condition was utilized in the stability analysis of multidimensional linear discrete system. The objective of this paper to concentrate on growing new mathematical technique, for the stability analysis of class of multidimensional linear time invariant discrete systems and to enhance the performance to bring out the ability of adjusted Jury's internal astute determinant foundation for stability investigation.

2 Literature Survey

System stability is the vital necessities in the linear discrete systems. Stability field has been analyzed by several specialists within the last century or a lot of Jury in [1] examined the conversion of multidimensional systems into single-dimensional for numerous applications. Also a new technique discussed in [3] explains the sign definiteness of forms necessary in stability studies. This positive definiteness of arbitrary quadratic structures that is communicated as far as a calculation utilizing internal wide networks. Tests exhibited in [4] determined an *s*-area scattering Hurwitz polynomials. These tests based on inner matrices which reduce the complexity of test procedure. Bose and Kamat Proposed an era of various multi variable polynomials by utilizing a limited number of multivariable framework augmentations took after by decrease of these polynomial [5].

Bose and Modarressi have given a constructive rule that is incredibly efficient for calculation of determinants of huge matrices with multivariable polynomial entries [6]. Serban and Najim in [7] explained the Schur–Cohn rule for testing bounded-input bounded-output (BIBO) stability in *N* variables. The cluster of authors targeted on efficient polynomial time algorithmic programme for computing determinant of a matrix [8]. Additionally on recurrent applications of extended hermite or Schur–Cohn formulation and uses sturm's theorem to search out the content of a system of polynomial in equalities during a single indeterminate it reduces the computations [9]. Bistriz talked the efficient stability test that is changed than Jury test [10]. The test procedure introduced by Jury clarifies the stability utilizing Routh table. Later, it is then changed in 1961 that is comparable to Routh table and extremely straightforward for hand computation for any order linear discrete systems was demonstrated in [11].

Had proposed an approach named as pseudo Routh section polynomials used to get low level of Routh table [12]. The strategy explores on [13] gave the propelled technique for finding out powerful stability utilizing bilinear change made a way to deal with *n*-dimensional stability testing, which is more proficient neighbourhood energy testing strategy [14]. Disclosed the procedure using a Schur–Cohn matrix that significantly simplifies the test procedure [4]. The criterion in [15] was

supported slice functions mechanisms and a recent n-dimensional extension of single-dimensional Schur coefficient associated to a polynomial, reviewed some geometrical properties of the stability domain of recursive filters that were redefined for specific categories of filters [16]. These commitments towards multidimensional straight move invariant advanced channels have prompted a few investigates in related field. Jury also introduced an associate efficient algorithmic rule that compute the determinant of polynomial matrix [1]. A critical result lead to reveal that stability drawback of multidimensional system was tackled as an optimization problem [17].

A neutral network was projected as an answer for this problem. Inner of square matrix was introduced by Jury for stability analysis using necessary and comfortable condition for the systems. Disclosed that the asymptotic stability of a category of linear time invariant system [18]. A association between positive inner wise and positive definite symmetric matrices for stability of linear discrete system that is proven in [2] had recommended that are to clone of critical constraints obtained from polynomial getting stability among unit circle directly simplifies the considerable use of bilinear transformation on the A matrix [19].

The strategies described in [20] were advanced for finding out powerful stability of discrete systems depends on use of bilinear transformation. In [8], an algorithmic programme is presented that computes the determinant of a polynomial matrix using quick Fourier rework from a view point of polynomial interpolation. The group of author well-tried the sufficient conditions that are straightforward enough to use for the stability tests using quick Fourier transform [21]. Novel stability criterion for multidimensional digital and analogue filters with rational transfer functions was given in [22]. The execution technique in [23] for stability check for single-dimensional advanced digital filter was reached out to multidimensional case that is verified using PC programme.

3 Existing Method

Stability Conditions for Multidimensional LTI System

The transfer function operate [24] of multidimensional digital systems is described as follows,

$$H(z_1, z_2, \ldots z_n) = \frac{A(z_1, z_2, z_3, \ldots z_n)}{B(z_1, z_2, z_3, \ldots z_n)} \tag{1}$$

The stability conditions are expressible for the continuous and discrete cases as follows: [19–25],

(i) Continuous case: $B\ (s_1, s_2, \ldots, s_n)$ [26]

$$\begin{aligned}
&B(s_1, 0, \ldots, 0) \neq && \operatorname{Re} s_1 \geq 0\\
&B(0, s_2, 0, \ldots) \neq && \operatorname{Re} s_2 \geq 0\\
&B(0, 0, s_3, 0, \ldots) \neq 0 && \operatorname{Re} s_3 \geq 0.\\
&\cdot\\
&B(s_1, s_2, \ldots, s_n) \neq 0\\
&B(s_1, s_2, \ldots, s_n) \neq 0 && \operatorname{Re}[s_1] = \operatorname{Re}[s_2] = \cdots = \operatorname{Re}[s_n] = 0
\end{aligned}$$

(ii) Discrete case: $B(z_1, z_2, \ldots, z_n)$

$$\begin{aligned}
&B(z_1, 1, 1, \ldots 1) \neq 0 && |z_1| \geq 1\\
&B(-1, z_1, 1, \ldots 1) \neq 0 && |z_2| \geq 1.\\
&\cdot\\
&B(-1, 1, 1, \ldots, z_n) \neq 0 && |z_n| \geq 1\\
&B(z_1, z_2, \ldots, z_n) \neq |z_1| = |z_2| = \cdots = |z_n| = 1
\end{aligned}$$

The testing of the last conditions, for each continuous and discrete case is incredibly troublesome that involves additional computations [25].

4 Proposed Method

The previously mentioned necessary conditions and one sufficient condition may be rewritten using reciprocal z_i, $(i = 1, 2, \ldots n)$ such that, the degree of x depends on the degree of the variables Z and this can be formulated as equation:

$$\begin{aligned}
B\left(\frac{1}{z_1}, \frac{1}{z_2}, \ldots \frac{1}{z_n}\right) = T_0\left(\frac{1}{z_1}, \frac{1}{z_2}, \frac{1}{z_3}, \ldots\right)\left(\frac{1}{z_n}\right)^n + T_1\left(\frac{1}{z_1}, \frac{1}{z_2}, \frac{1}{z_3}, \ldots\right)\left(\frac{1}{z_n}\right)^{n-1}\\
+ \cdots T_n\left(\frac{1}{Z_1}\right) = 0
\end{aligned} \tag{2}$$

(or) after simplification the above equation becomes

$$M(Z_1, Z_2, Z_3 \ldots Z_n)\left|\begin{array}{l} = F(x) = 0\\ (Z_k) = x\\ (k = 1, 2 \ldots n)\end{array}\right. \tag{3}$$

Thus, the $F(x) = 0$ can be handled by the proposed algebraic test which is given below.

Let

$$F(x) = a_n x_n + a_{n-1} x_{n-1} + \cdots + a_0 = 0 \tag{4}$$

then the generalised necessary conditions for stability can be formed as given below:

If 'n' is even:

(i) $f(1) > 0$
(ii) $f(-1) > 0$ and
(iii) $\left|\frac{a_0}{a_n}\right| < 1$

If 'n' is odd:

(i) $f(1) > 0$
(ii) $f(-1) < 0$ and
(iii) $\left|\frac{a_0}{a_n}\right| < 1$

The Jury sufficient test is carried out as follows:

Utilizing the coefficients of $f(x)$ two triangular matrices is composed by left and right movings of the coefficient

$$[A_1] = \begin{pmatrix} a_n & a_{n-1} & a_{n-2} & . & . & . & a_n \\ 0 & a_n & a_{n-2} & . & . & . & . \\ 0 & 0 & a_n & . & . & . & . \\ 0 & 0 & 0 & a_n & . & . & . \\ . & . & . & . & . & . & . \\ . & . & . & . & . & . & . \\ . & . & . & . & . & . & a_n \end{pmatrix} \tag{5}$$

$$[A_2] = \begin{pmatrix} a_n & a_{n-1} & a_{n-2} & . & . & . & a_0 \\ a_{n-1} & a_{n-2} & a_{n-3} & . & . & . & 0 \\ a_{n-2} & a_{n-3} & 0 & . & . & . & 0 \\ . & . & . & . & . & . & 0 \\ . & . & . & . & . & . & 0 \\ . & . & . & . & . & . & 0 \\ a_0 & 0 & 0 & . & . & . & 0 \end{pmatrix} \tag{6}$$

From (A_1) and (A_2), we construct $[I_1]$ by adding (A_1) and (A_2) and we construct $[I_2]$ subtracting (A_1) and (A_2).

$$[I_1] = [A_1] + [A_2] \tag{7}$$

$$[I_2] = [A_1] - [A_2] \tag{8}$$

For the system to be absolutely stable, $[I_1]$ and $[I_2]$ must be positive inner wise. The aforementioned square matrix S is claimed to be positive inner wise with all the determinants with the middle element(s) and continuing out wards up to the entire matrix are positive Jury [27]. This method consumes more arithmetic operations and time, computational cost also very high. Hence we go to following proposed method to test the sufficient condition of the given system by direct formation of Single Square matrix [S].

Proposed method to check the sufficient condition:

Consider the following one-dimensional characteristic equation

$$a_5 z^5 + a_4 z^4 + a_3 z^3 + a_2 z^2 + a_1 z + a_0$$

$$[S] = \begin{bmatrix} a_5 & a_4 & a_3 & a_2 & a_1 & a_0 \\ a_4 & a_5 + a_3 & a_4 + a_2 & a_3 + a_1 & a_2 + a_0 & a_1 \\ a_3 & a_2 & a_1 + a_5 & a_4 + a_0 & a_3 & a_2 \\ a_2 & a_1 & a_0 & a_5 & a_4 & a_3 \\ a_1 & a_0 & 0 & 0 & a_5 & a_4 \\ a_0 & 0 & 0 & 0 & 0 & a_5 \end{bmatrix} \tag{9}$$

From the given 1-D characteristics equation all the coefficients from a_n to a_0 entered within the initial row of matrix [S]. The first column of matrix [S] is made by getting into the coefficient from a_{n-1} (n = 5, 4, 3…1) to a_0 equally the last column of matrix [S] is formed by getting into the characteristics equation coefficients from a_{n+1} to a_n (n = 1, 2, 3…5). Then the second row of the matrix is made by adding the alternate coefficients of the first row of the matrix[S]. The [(n − 1) + 1] where (n = 5) column is made by one shifting the (n + 1) column and insert '0' in first and eliminate a_n. Equally second column is made by one shift towards the top of the first column and insert '0' in first and eliminate a_0.

The [(n − 2) + 1] wherever n = 5 fourth column of matrix is made by two shifts towards top of the (n + 1) column, insert two '0's' first and eliminate a_{n-1}, a_n, equally third column is made by the two shift the towards top of the first column and insert '0's' in first and eliminate a_1, a_0. Equally the remaining columns were formed in [(n + 1) * (n + 1)] single square matrix. The simple shift and elimination operation has concerned the formation of single square matrix [S]. The square matrix [S] is claimed to be positive inner wise once all the determinants beginning with the centre elements and proceeding outward up to the complete matrix are positive. The planned methodology for forming single square matrix [S] that consumes less arithmetic operations and time compared to Jury methodology.

5 Illustrations

Example 1:

$$B(Z_1Z_2Z_3) = 6Z_1^2Z_2Z_3 + 6Z_1^2Z_3 + 4Z_1^2Z_2 + 6Z_1Z_2Z_3 + 14Z_1Z_3 + 4Z_2Z_3 + 4Z_1^2 + 2Z_1Z_2 + 4Z_3 + 10Z_1 + 2Z_2 + 2$$

Equivalent one-dimensional characteristic equation by inverting variables Z_1, Z_2 and Z_3 and equate $Z_1 = Z_2 = Z_3 = X$.

$$F(X) = 2X^4 + 16X^3 + 24X^2 + 16X + 6$$

Necessary condition:

$$F(1) = 2 + 16 + 24 + 16 + 6 = 64 > 0 \quad \text{(satisfied)}$$
$$F(-1) = -2 - 16 + 24 - 16 + 6 = 0 \quad \text{(Not satisfied)}$$

Sufficient test by Jury method:

One-dimensional characteristic equation:

$$f(x) = 2x^4 + 16x^3 + 24x^2 + 10x + 6 = 0$$

$$X = \begin{bmatrix} 2 & 16 & 24 \\ 0 & 2 & 16 \\ 0 & 0 & 2 \end{bmatrix},$$

$$Y = \begin{bmatrix} 24 & 16 & 6 \\ 16 & 6 & 0 \\ 6 & 0 & 0 \end{bmatrix}$$

$$X + Y = \begin{bmatrix} 26 & 32 & 30 \\ 16 & 8 & 16 \\ 6 & 0 & 2 \end{bmatrix} = 1024 > 0 \quad \text{(Satisfied)}$$

$$X - Y = \begin{bmatrix} 22 & 0 & 18 \\ 16 & 4 & 16 \\ 6 & 0 & 2 \end{bmatrix} = -256 < 0 \quad \text{(Not satisfied)}$$

System is unstable.

Proposed method for sufficient test:

$$\begin{bmatrix} 2 & 16 & 24 & 16 & 6 \\ 16 & 26 & 32 & 30 & 16 \\ 24 & 16 & 8 & 16 & 24 \\ 16 & 6 & 0 & 2 & 16 \\ 6 & 0 & 0 & 0 & 2 \end{bmatrix}$$

$\nabla_1 = 8 > 0$ (Satisfied)
$\nabla_3 = 1024 > 0$ (Satisfied)
$\nabla_5 = 0$ (Not satiesfied)

The given system not satisfied the both necessary and sufficient conditions. Hence the given system is unstable.

Example 2:

$$B(Z_1Z_2Z_3) = 1 + Z_1 + Z_1Z_2 + Z_1Z_3 + 5Z_1Z_2Z_3$$

Equivalent one-dimensional characteristic equation by inverting variables Z_1, Z_2 and Z_3 and equate $Z_1 = Z_2 = Z_3 = X$.

$$F(X) = X^3 + X^2 + 2X + 5$$

Necessary condition:

$$F(1) = 1 + 1 + 2 + 5 = 9 > 0 \quad \text{(Satisfied)}$$
$$F(-1) = -1 + 1 - 2 + 5 = 3 < 0 \quad \text{(Not satisfied)}$$

Sufficient test by Jury method:

One-dimensional characteristic equation:

$$f(x) = x^3 + x^2 + 2x + 5 = 0$$

$$X = \begin{bmatrix} 1 & 1 \\ 0 & 1 \end{bmatrix},$$
$$Y = \begin{bmatrix} -2 & 5 \\ 5 & 0 \end{bmatrix}$$

$$X+Y=\begin{bmatrix}3 & 6\\ 5 & 1\end{bmatrix}=-27<0 \quad \text{(Not satisfied)}$$
$$X-Y=\begin{bmatrix}1 & 4\\ 5 & 1\end{bmatrix}=-19<0 \quad \text{(Not satisfied)}$$

System is unstable.

Proposed method for sufficient test:

$$\begin{bmatrix}1 & 1 & 2 & 5\\ 1 & 3 & 6 & 2\\ 2 & 5 & 1 & 1\\ 5 & 0 & 0 & 1\end{bmatrix}$$

$$\nabla_2=-27<0 \quad \text{(Not satisfied)}$$
$$\nabla_4=567>0 \quad \text{(Satisfied)}$$

The given system does not satisfied the both necessary and sufficient conditions, therefore the given system is unstable.

Example 3:

$$Q(S_1,S_2,S_3)=6S_1^3S_2S_3+6S_1^2S_3+6S_1S_2S_3+S_1S_3+2S_1S_2+S_1^2+S_1+4S_3+1$$

Equivalent one-dimensional characteristic equation by inverting variables S_1, S_2 and S_3 and equate $S_1=S_2=S_3=X$

$$F(X)=X^5+5X^4+4X^3+2X^2+6$$

Necessary condition:

$$F(1)=1+5+4+2=18>0 \quad \text{(Satisfied)}$$
$$F(-1)=-1+5-4+2+6=8>0 \quad \text{(Satisfied)}$$

Proposed method for sufficient test:

$$\begin{bmatrix} 1 & 5 & 4 & 2 & 0 & 6 \\ 5 & 5 & 7 & 4 & 8 & 0 \\ 4 & 2 & 1 & 11 & 4 & 2 \\ 2 & 0 & 6 & 1 & 5 & 4 \\ 0 & 6 & 0 & 0 & 1 & 5 \\ 6 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

$$\nabla_2 = 65 > 0 \quad \text{(Satisfied)}$$
$$\nabla_4 = 231 > 0 \quad \text{(Satisfied)}$$
$$\nabla_6 = 96336 \quad \text{(Satiesfied)}$$

The given system satisfied both necessary and comfortable conditions, therefore the given system is unstable.

6 Conclusion

The procedure is projected in this paper with suitable examples to examine the stability of multidimensional characteristics polynomial using single square matrix [*S*] and projected methodology is incredibly straightforward and direct compared to Jury methodology.

References

1. Jury, E.I.: Stability of multi-dimensional scalar and matrix polynomials. Proc. IEEE **66**(9), 1018–1047 (1978)
2. Jury, E.I.: Inners—approach to some problems of systems theory. IEEE Trans. Autom. Control. **16**(3), 223–240 (1971)
3. Bose, N.K., Jury, E.I.: Inner algorithm to test for positive definiteness of arbitrary binary forms. IEEE Trans. Autom. Control. **20**(1), 169–170 (1975)
4. Karivaratharajan, P., Reddy, H.C.: A test procedure for 2-D discrete scattering Hurwitz polynomials. IEEE Trans. Acoust. Speech Signal Process. **37**(1), 118–120 (1989)
5. Bose, N.K., Kamat, P.S.: Algorithms for stability test of multi-dimensional filters. IEEE Trans. Acoust. Signal Process. **22**(5), 307–314 (1974)
6. Bose, N.K., Modarressi, A.K.: General procedure for multivariable possibility test with control applications. IEEE Trans. Autom. Control. 696–701 (1976)
7. Serban, I., Najim, M.: Multidimensional systems: BIBO stability test based on functional schur coefficients. IEEE Trans. Signal Process. **55**(11), 5277–5285 (2007)
8. Kurosawa, K., Yamada, I., Yokokawa, T., Tsujji, S.: A fast stability for multidimensional systems. In: IEEE International Symposium on Circuits and Systems, Tokyo Institute of Technology, Tokyo, Japan, vol. 152, pp. 579–582 (1993)

9. Bose, N.K., Jury, E.I.: Positivity and stability test for multidimensional filters (discrete–continuous). IEEE Trans. Acoust. Speech Signal Process. **22**(3), 174–180 (1974)
10. Bistriz, Y.: Critical stability constraints for discrete—time linear systems. IEEE Trans. Circuits Syst. II Express Briefs **52**(2), 95–99 (2006)
11. Jury, E.I., Blanchard, J.: A stability test for linear discrete systems in table form. Proc. IRF. **21**, 1947–1948 (1961)
12. Sivanandam, S.N., Deepa, S.N.: Linear system design using Routh column polynomials. Songklanakarin J. Sci. Technol. **29**(6), 1651–1659 (2007)
13. Bose, N.K, Zeheb, E.: Khantonov's theorem and stability test of multidimensional digital filters. Proc. IEEE Electr. Circuits Syst. **133**(4), 187–190 (1986)
14. Bose, N.K.: Implementation of a new stability test for 2-D filters. IEEE Trans. Acoust. Speech. Signal Proc. **27**(1), 1–4 (1979)
15. Serban, I., Najim, M.: A slice based 3-D Schur Cohn stability criterion. In: IEEE International Conference on Acoustics, Speech and Signal Processing. vol. 13, pp. 1405–1408 (2007)
16. Benidir, M.: Sufficient conditions for the stability of multi-dimensional recursive digital filters. In: International Conference on Acoustics, Speech and Signal Processing, pp. 2885–2888 (1991)
17. Mastorakis, N.E., Mladenoy, V.M., Swamy, M.N.S.: Neural network for checking the stability of multi-dimensional system. In: IEEE Proceeding of the Ninth Symposium on Neural Networks. Belgrde, Serbia, pp. 89–94 (2008)
18. De la sen, M.: Stability criteria for linear time invariant systems with point delays based on one dimensional Routh–Hurwitz tests. Appl. Math. Comput. **187**, 1199–1207 (2007)
19. Jury, E.I., Gutman, S.: On the stability of the a matrix inside the unit circle. IEEE Trans. Autom. Control. **20**(4), 533–535 (1975)
20. Bose, N.K., Zeheb, E.: Kharitonov's theorem and stability test of multi-dimensional digital filters. Proc. IEEE Electron. Circ. Syst. **133**(4), 187–190 (1986)
21. Hertz, D., Zeheb, E.: Sufficient conditions for stability of multi-dimensional discrete systems. Proc. IEEE **72**(2), 226 (1984)
22. Strintzis, M.G.: Test of stability of multi-dimensional filters. IEEE Trans. Circ. Syst. **24**(8), 432–437 (1997)
23. Sivanandam, S.N., Sivakumar, D.: A new algebraic test procedure for stability analysis of multi-dimensional shift invariant digital filters. In: Proceedings of IEEE Region 10 International Conferences on Electrical and Electronic Technology, Vol. 1, pp. 33–38 (2001)
24. Ramesh, P.: Certain algebraic test for analyzing aperiodic stability of two dimensional linear discrete systems. Circuits Syst. **7**(6), 718–725 (2016)
25. Jury, E.I.: Stability tests for one-two and multi-dimensional linear systems. In: IET Proceedings of the Institution of Electrical Engineers, vol. 124, pp. 1237–1240 (1977)
26. Zhang, C.: The application of 2-D numerical inversion of laplace transform. In: IEEE 9th International Conference on Signal Processing (2008)
27. Jury, E.I., Bauer, P.: On the stability of two-dimensional continuous systems. IEEE Trans. Circuits Syst. **35**(12), 1487–1500 (1988)

Detection of Static Air-Gap Eccentricity in Three-Phase Squirrel Cage Induction Motor Through Stator Current and Vibration Analysis

S. Bindu and Vinod V. Thomas

Abstract Three-phase squirrel cage induction motor being a core component of industrial drives needs fault detection strategies which can detect internal faults in very early stage of its development. This can result in enormous financial saving in industries. Simulation studies with suitable mathematical models helps in identification of fault signatures in the diagnostic signal. The work presented in this paper addresses the issue of detection of incipient static eccentricity faults. Modelling of motor with static eccentricity fault is done and characteristic signatures were identified in frequency spectrum of stator current. These components were also identified in the vibration spectrum, by conducting a practical experimentation in three-phase squirrel cage induction motor with fabricated static eccentricity. The results validates the modelling approach and also demonstrates the suitability of vibration and stator current signal for the diagnosis of incipient static eccentricity faults.

Keywords Air-gap eccentricity · Motor current signature analysis
Vibration analysis · Three-phase squirrel cage induction motor

1 Introduction

A huge amount of world's generating capacity is consumed by induction motor drives [1]. Induction motor drives are the major assets in process and energy industries. The asset management of electrical drives requires reliable condition monitoring, diagnostics and maintenance strategies. Static eccentricity is an internal fault in which position of minimum air-gap is fixed in space. In practical situations, inherent level of air-gap eccentricity always present due to manufacturing tolerances. Abnormal level of air-gap eccentricity has to be identified before leading to

S. Bindu (✉) · V.V. Thomas
Manipal Institute of Technology, Manipal University, Manipal, India
e-mail: bindu.s@manipal.edu

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_50

secondary defects. The work presented here focuses on experimentation based on stator current and vibration analyses to diagnose static eccentricity in three-phase induction motor.

2 Diagnosis of Air-Gap Eccentricity

Industrial case studies show that air-gap eccentricity occurs due to incorrect onsite installation of large motors and during re-installation following a repair or overhaul. Thermal bowing of the shaft can cause dynamic eccentricity. Air-gap eccentricity level of 25–30% is considered to be severe in large motors. A catastrophic failure can occur if the eccentricity is at a level such that the resultant unbalanced magnetic pull causes stator to rotor rubs [1, 2].

No single diagnostic signal exist which is able to detect probable faults in induction motors completely. Vibration and Stator Current and Temperature are the easily sensible diagnostic signals but each of these signals alone can detect only some specific faults. A general and reliable diagnostic system cannot depend only on a single signal. Non-invasive condition monitoring techniques are the key requirement in many industrial applications [3–6].

3 Static Eccentricity Modelling

Conventional direct and quadrature axis model is a model suitable for dynamic analysis of induction motor. Since this modelling strategy is available in many literatures [7], this part is not elaborated here. To incorporate static eccentricity, developed model is modified as per the following approach. Air-gap length is variable with respect to rotor position in static eccentricity conditions and this deviation reflects in the stator to rotor mutual inductance. Static eccentricity is present if there is a shift in the rotational centre of rotor from the geometric centre of stator bore. Such an eccentricity is maximum at one place and minimum at diametrically opposite place in the air gap [8, 9].

A coordinate system deliberated here has its origin lies at the geometric centre of the stator bore 'O' as given in Fig. 1. For healthy motor air-gap length is constant and is given by:

$$l_g = r_s - r_r \tag{1}$$

where r_s and r_r are the stator bore radius and rotor radius, respectively.

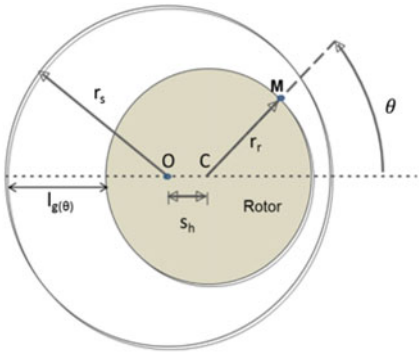


Fig. 1 Schematic diagram of static air-gap eccentricity

If static eccentricity exists, rotor shifts towards one side and air-gap remains non-uniform. Let S_h be the shifted rotor centre 'C' from 'O'. Let 'M' be a point on the outer surface of rotor. Distance of 'M' from the origin $r_1(\theta)$ can be written as

$$r_1^2(\theta) = (r_r \sin\theta)^2 + (s_h + r_r \cos\theta)^2 \tag{2}$$

Therefore, air-gap at any point 'M' is given by

$$l_g(\theta) = r_s - r_1(\theta) \tag{3}$$

Let 'A' be the cross-sectional area of the path followed by flux, length of flux path is same as air-gap length. Reluctance 'S' is given by

$$S(\theta) = l_g(\theta)/(\mu A) \tag{4}$$

where 'μ' is the permeability of medium. Cross-sectional area of the path followed by flux can be considered as constant, and hence reluctance is proportional to air-gap length. Hence, permeance of air-gap is inversely proportional to the air-gap length. 'l_g' is the fixed air-gap length of healthy motor, whereas for faulty motor it is slip dependant. Since mutual inductance between stator and rotor windings is proportional to permeance it can be written as:

$$L_{sr}(\theta) = L_{sr} * (l_g/l_g(\theta)) \tag{5}$$

where '$L_{sr}(\theta)$' is the mutual inductance between rotor and stator of faulty machine and 'L_{sr}' is that of healthy machine. To incorporate air-gap eccentricity in the conventional model, mutual inductance between rotor and stator is replaced by rotor position dependent mutual inductance '$L_{sr}(\theta)$'.

4 Simulation Results and Analyses

Simulation of the dynamic model in DQ frame of a 3hp motor is conducted in MATLAB® platform. Speed and torque responses as well as stator current response in time and frequency domain were observed and analyzed, at different load conditions.

The healthy machine current spectrum shows only fundamental component at 60 Hz as given in Fig. 2. Frequency spectrum of stator current of machine with eccentricity contains slip dependent frequency components and is presented in Fig. 3. Frequencies are matching with characteristic frequencies for eccentricity f_c, given in Eq. (6)

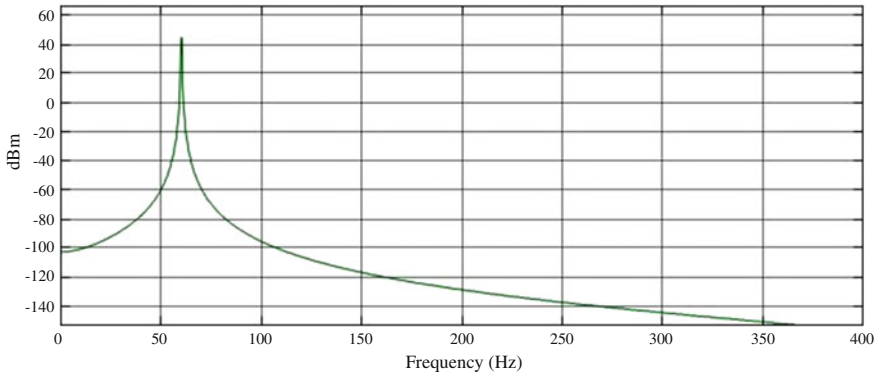


Fig. 2 Stator current spectrum of healthy machine

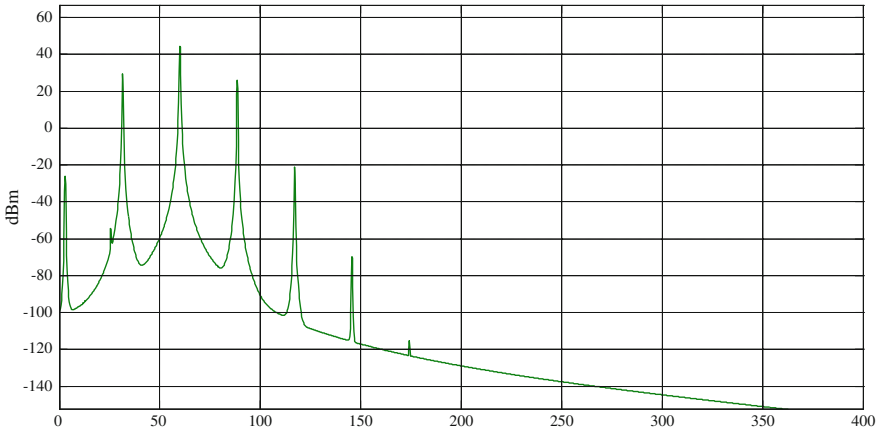


Fig. 3 Frequency spectrum of stator current at 50% static eccentricicty

Table 1 Frequency components in stator current spectrum at 50% static eccentricity

Slip	Characteristic frequency components (Hz)						
		$f - 2f_r$	$f - f_r$	$f + f_r$	$f + 2f_r$	$f + 3f_r$	$f + 4f_r$
0.0235	Expected	1.46	30.7	89.3	118.6	147.9	177.2
	Observed	1.41	30.7	89.3	118.6	147.9	177.2
0.0483	Expected	2.86	31.5	88.5	117.1	145.6	174.1
	Observed	2.89	31.4	88.5	117.1	145.6	174.2

$$f_c = f_s \pm m f_r \tag{6}$$

where f_s is the supply frequency and m is an integer given by m = 1, 2, 3, … and $f_r = f_s(1 - s)/p$, where p is the number of pole pairs and s is the slip.

The spectrum components are presented in Table 1.

The model of three-phase induction motor with static eccentricity fault used here is a modified form of DQ model, which showed expected stator current spectrum. So this model has proven its suitability for air-gap eccentricity studies. This model follows a simple approach which has less computational load compared to multiple coupled circuit approach [10]. In faulty condition, with static eccentricity speed and torque oscillations were observed. These oscillations are increasing with increase in percentage of eccentricity.

5 Motor Current Signature Analysis: Results and Discussion

To create non-uniform air-gap length rotor centre is shifted from geometric centre of the bore. This is achieved by making phosphor bronze ring around the bearing with non-uniform thickness as given in Fig. 4. Stator current spectrum was observed at

Fig. 4 End cap of the machine with fabricated air-gap eccentricity

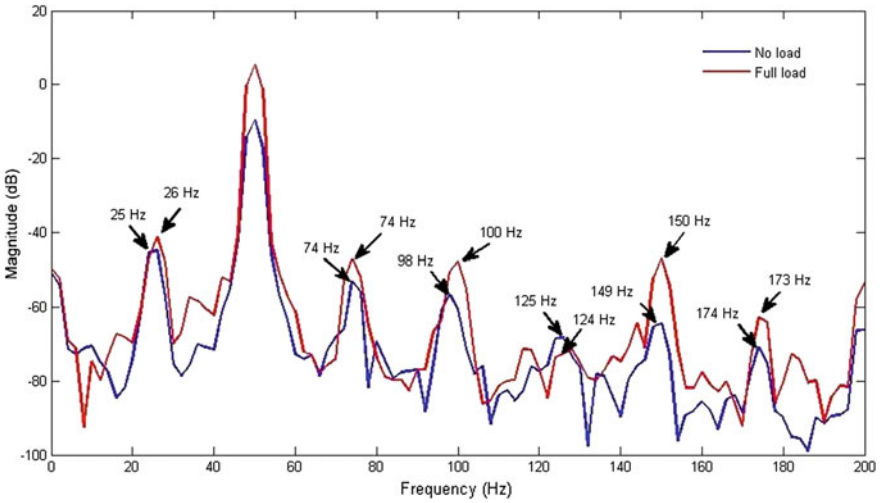


Fig. 5 Frequency spectrum of stator current at two different rotor speeds at 50% static eccentricity

Table 2 Characteristic frequency components in the frequency spectrum of stator current at two different slips at 50% static eccentricity

Slip		$f - f_r$	$f + f_r$	$f + 2f_r$	$f + 3f_r$	$f + 4f_r$	$f + 5f_r$
0.0093	Expected	25.2	74.7	99.5	124.3	149.0	173.8
	Observed	25.0	75.0	99.0	125.0	150.0	174.0
0.0600	Expected	26.5	73.5	97.0	120.5	144.0	167.5
	Observed	26.0	74.0	98.0	122.0	148.0	168.0

different load conditions by making use of LABVIEW® data acquisition and processing platform. Slip dependent frequency components as per Eq. (6) were observed as presented in Fig. 5 and Table 2, which validates the simulation results.

6 Vibration Analysis: Results and Discussion

All electric machines generate noise and vibration, and the analysis of the produced noise and vibration can provide information on the condition of the machine. After introducing the fault, tests were conducted using vibration sensor (triple axis accelerometer). The characteristic frequency components as per Eq. (6) are also identified in vibration spectrum, which is given in Fig. 6. Both vibration and stator current spectra give the slip dependent characteristic components of static eccentricity as given in Eq. (6).

Both experimentation results validates the simulation approach by the presence of same components in the spectra.

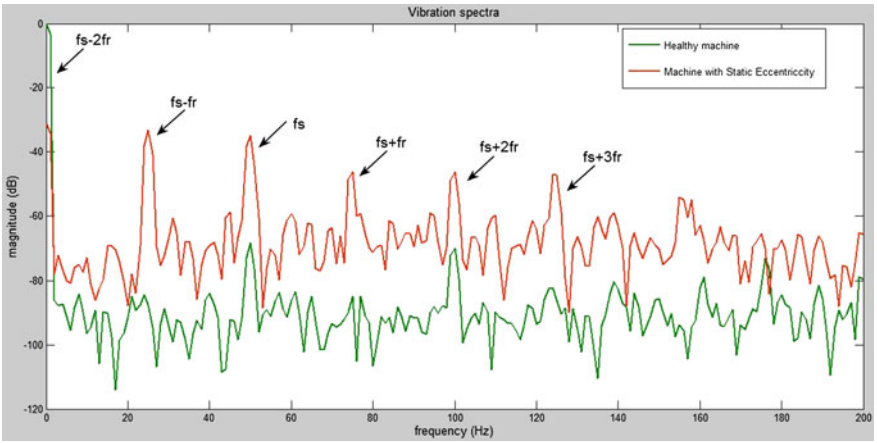


Fig. 6 Characteristic frequency components in vibration spectrum corresponding to healthy machine and machine with 50% static eccentricity

7 Conclusion

The model developed is a novel approach for reliable diagnosis of static eccentricity. The simulation results provide a stator current spectrum which exhibits air-gap eccentricity characteristic frequencies. The experimental results noticeably indicate the difference in the characteristic signatures with slip. To incorporate dynamic, mixed or inclined eccentricity and other internal faults in the proposed model, further investigation has to be conducted. Further analyses with appropriate models, experimentation and signature extraction using advanced signal processing tools will aid in emerging condition monitoring systems which is clever in detecting internal faults at incipient stage.

References

1. Zhang, P., Du, Y., Habetler, T.G., Lu, B.: A survey of condition monitoring and protection methods for medium-voltage induction motors. IEEE Trans. Ind. Appl. **47**, 34–46 (2011)
2. Thomas, V.V., Vasudevan, K., Kumar, V.J.: Online cage rotor fault detection using air-gap torque spectra. IEEE Trans. Energy Convers. **18**, 265–270 (2003)
3. Hyun, D., Hong, J., Lee, S.B., Kim, K., Wiedenbrug, E.J., Teska, M., Nandi, S., Chelvan, I. T.: Automated monitoring of air gap eccentricity, for inverter-fed induction motors under standstill conditions. IEEE Trans. Ind. Appl. **47**, 1257–1266 (2011)
4. Thomas, V.V., Bindu, S.: Non-invasive techniques for fault diagnoses of induction machines. In: Proceedings of Third International Engineering Symposium (2013)
5. Bindu, S., Thomas, V.V.: Diagnoses of internal faults of three phase squirrel cage induction motor—a review. In: Proceedings of ICAECT-2014, pp. 48–54, (2014)

6. Huang, X., Habetler, T.G., Harley, R.G.: Detection of rotor eccentricity faults in a closed-loop drive-connected induction motor using an artificial neural network. IEEE Trans. Power Electron. **22**, 1552–1559 (2007)
7. Krishnan, R.: Electric Motor Drives: Modelling, Analysis and Control, Pearson (2011)
8. Kamal, V.A., Giri, K.: Mathematical modelling of dynamic induction motor and performance analysis with bearing fault. Proc. Int. J. Innov. Technol. Res. **1**, 336–340 (2013)
9. Kamal, A., Giri, V.K.: Detection of bearing fault in three phase induction motor using wavelet. VSRD J. Electr. Electron. Commun. Eng. **3** (2013)
10. Luo, X., Liao, Y., Toliat, H.A., El-Antably, A., Lipo, T.A.: Multiple coupled circuit modeling of induction machines. IEEE Trans. Ind. Appl. **31**, 311–318 (1995)

Analysis of Three Phase Inverter Using Different PWM Techniques

Ayesha Firdous, Mohammed Imran and Mahboob Shaik

Abstract There are many inverter topologies in which cascaded inverter have some advantages compared to other multilevel inverters such as reduced harmonics but they have drawbacks also such as many heat losses, more switches, high cost. But in this new configuration which is developed in this project overcome all these disadvantages. In this project four different pulse width modulation techniques are used, they are In Phase disposition, Phase Opposition disposition, Overlap Carrier disposition, and Frequency Varying disposition methods. This paper discusses new configuration with 10 power switches and four DC sources. The proposed configuration includes many advantages compared to existing configurations the advantages are very less cost, less switching losses, less harmonics, and greater efficiency at output. The circuit is built in matlab software and results are verified to select the best Pulse width modulation technique which has reduced Total Harmonic Distortion in output. In order to make the output voltage more sinusoidal and reduce the THD, LC Filter is used.

Keywords Different multilevel inverters · Different pulse width modulation methods · FFT analysis

A. Firdous (✉) · M. Imran · M. Shaik
Electrical Engineering Department, Muffakham Jah College of Engineering, Hyderabad 500034, India
e-mail: ayeshafirdous2016@gmail.com

M. Imran
e-mail: imraneed@mjcollege.ac.in

M. Shaik
e-mail: mahaboobeed@mjcollege.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_51

Table 1 Switches for each phase for different inverters for 13 level

S.No.	Configuration	Switches for each phase for 13 level inverter	Conducting switches for each phase
1	Diode clamped	24	5
2	Capacitor clamped	24	5
3	Ten switch type	10	5

1 Introduction

Nowadays electronic devices are very important and play a very crucial role for control of electric power and conversion from AC to DC and vice versa [1]. Inverters can be three phase or single phase inverters. Single phase inverters which are bipolar produce staircase waveform which includes many harmonics. Due to these drawbacks multilevel inverters are implemented [2]. Thirteen level inverter which has very reduced THD percentage will be discussed. Different PWM techniques are used gating pulses. Those PWM techniques are In Phase Disposition, Phase Opposition, Overlap Carriers, and Frequency Varying PWM techniques [3]. In comparison other topologies, the discussed inverter have reduced switches [4]. This project deals with one phase of inverter with 10 switches and 4 DC sources for obtaining 13 level inverter output. Similarly three phase output can be obtained by interconnecting the three single phases to load which is star connected with common earth. The proposed configuration have many advantages, i.e., reduced cost reduced harmonics, pure sine output, reduced gate control, very less heating losses. Below table shows different multilevel Inverters compared with proposed techniques for number of components for phase. In this project LC filter is used to get pure sine wave with very low THD value. The LC filter attenuates ripples in the output voltage due to switching (Table 1).

2 Proposed Method with Working

The new 13 level inverter has ten switches and four sources which are DC for each phase as shown in Fig. 1. The combination of four DC sources $V_{dc,}$ $2V_{dc,}$ $V_{dc,}$ and $2V_{dc}$ which are connected in series with which thirteen level output voltage in each cycle can be produced. For every mode five switches operates simultaneously.

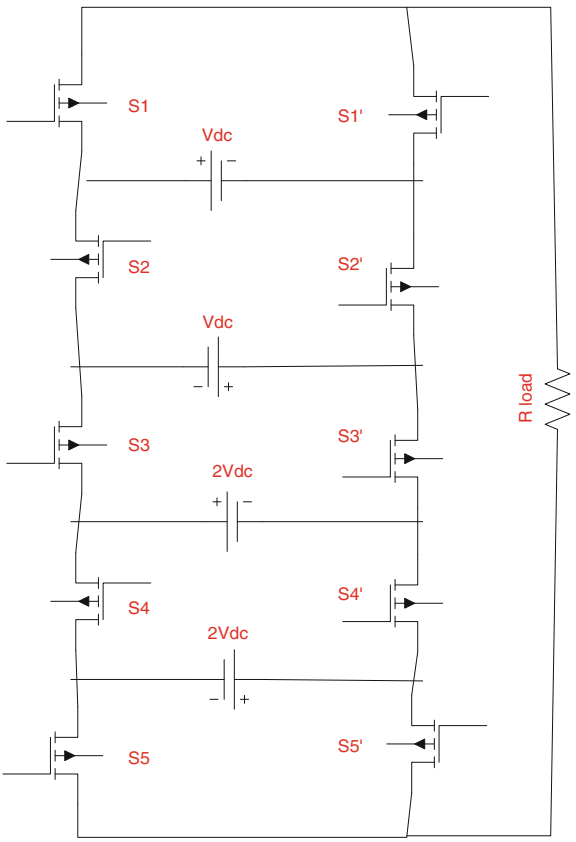


Fig. 1 Implemented circuit diagram for one phase of 13 level

Table 2 Operation of switches in 13-level inverter

Voltage at output	$S1$	$S2$	$S3$	$S4$	$S5$	$S1'$	$S2'$	$S3'$	$S4'$	$S5'$
$6V_{dc}$	1	0	1	0	1	0	1	0	1	0
$5V_{dc}$	0	0	1	0	1	1	1	0	1	0
$4V_{dc}$	1	1	1	0	1	0	0	0	1	0
$3V_{dc}$	1	0	0	0	1	0	1	1	1	0
$2V_{dc}$	1	1	1	0	0	0	0	0	1	1
V_{dc}	1	0	0	0	0	0	1	1	1	1
0	0	0	0	0	0	1	1	1	1	1
$-V_{dc}$	0	1	1	1	1	1	0	0	0	0
$-2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$-3V_{dc}$	0	1	1	1	0	1	0	0	0	1
$-4V_{dc}$	0	0	0	1	0	1	1	1	0	1
$-5V_{dc}$	1	1	0	1	0	0	0	1	0	1
$-6V_{dc}$	0	1	0	1	0	1	0	1	0	1

By turning on the switches *S*l, *S*2′, *S*3′, and *S*4′, *S*5 together we get $+V_{dc}$ voltage for 13 level inverter. In the same manner other dc voltages are obtained as in Table 2.

3 Modulation Techniques

For controlling the problems at output voltage we should have good pulse width modulation method. Out of all the pulse width modulation methods, sinusoidal method is used in this project.

3.1 In Phase Disposition Level-Shift PWM Technique

In this technique the carrier waves are shifted in levels. The carrier signals are of same amplitude of 1 V. These carrier waves are compared with reference wave as shown in Fig. 2.

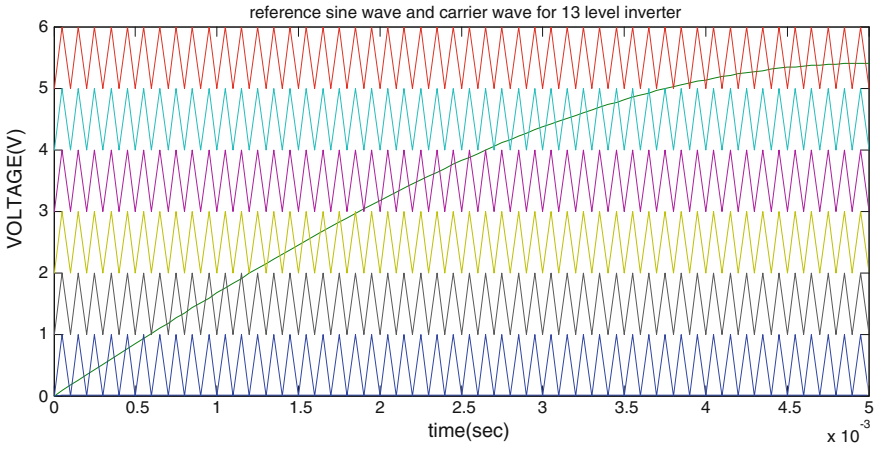


Fig. 2 Comparison of sine wave and carrier wave for IPD–PWM technique

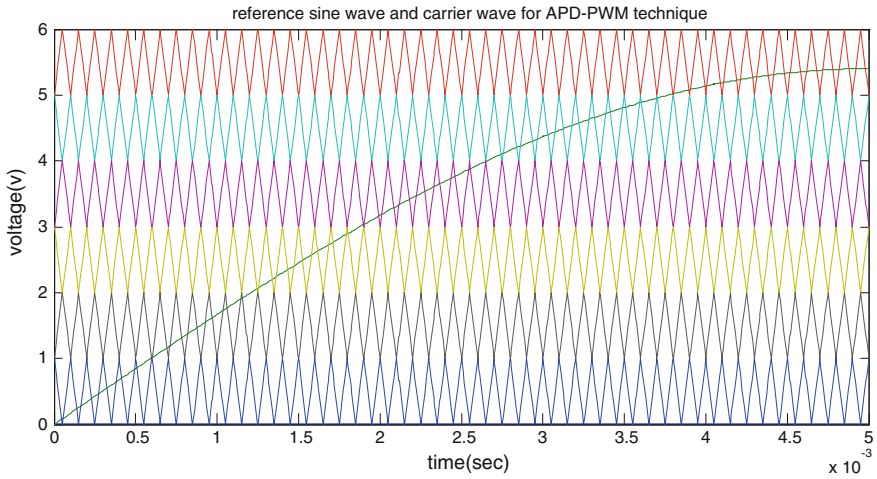


Fig. 3 Comparison of sine wave and carrier wave for APD–PWM technique

3.2 Phase Opposition Level-Shift PWM Technique

In this technique the generated gating pulses are shown in Fig. 3.

3.3 Carrier Overlap PWM Technique

In this technique carrier signals are having same amplitude and frequency but the carrier signals overlap each other. These carrier signals are compared with sine wave, which is at fundamental frequency to get the gate pulses as shown in Fig. 4.

3.4 Variable Frequency PWM Technique

In this technique the carrier signals are of different frequency but having same amplitude as shown in Fig. 5.

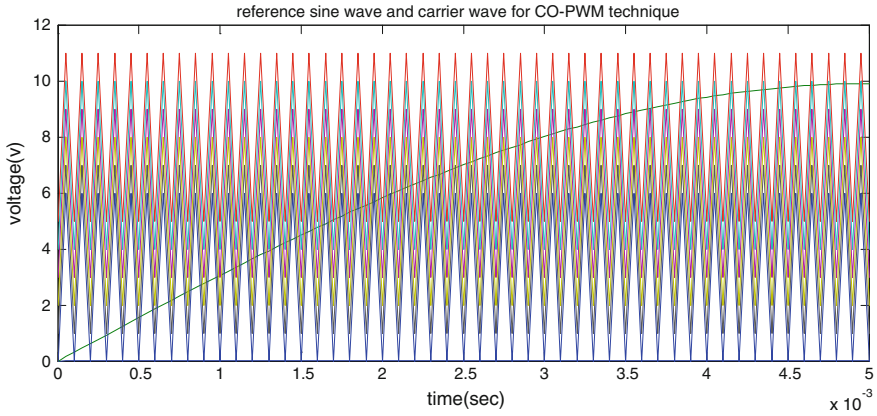


Fig. 4 Comparison of sine wave and carrier wave for CO–PWM technique

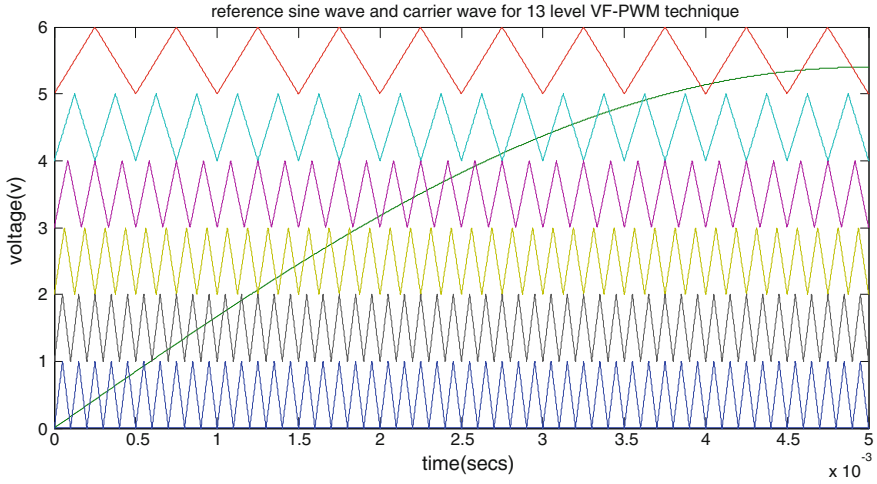


Fig. 5 Comparison of sine wave and carrier wave for VF–PWM technique

4 Results Obtained After Simulation

Different pulse width modulation techniques are used in this project for getting the three phase output using MATLAB software. The load which is used is in star connection.

$$\text{Load resistance} = 50\,\Omega$$

4.1 *Output Voltage Waveforms for 13 Level Inverter Using IPD–PWM Technique*

Three phase waveform of output voltage for 13 level using IPD–PWM method for the time period 20 ms and amplitude of 180 V is shown in Fig. 6a and FFT analysis is given in Fig. 6b.

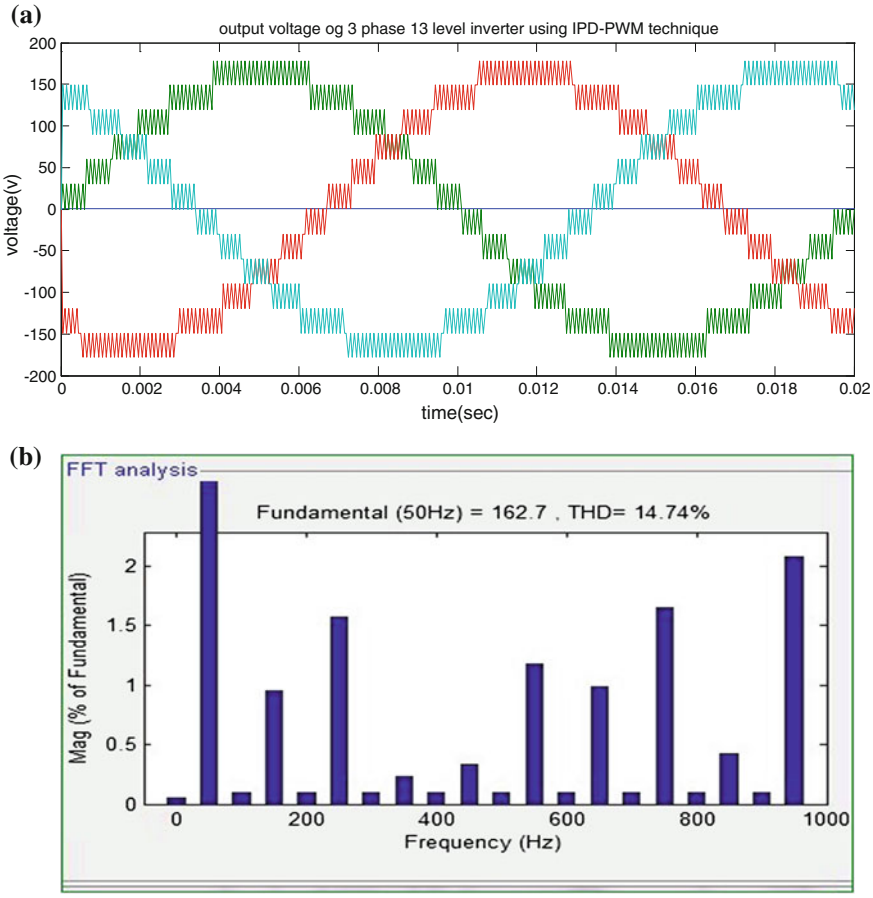


Fig. 6 **a** Obtained three phase waveform for output voltage for 13 level using IPD–PWM method **b** FFT analysis for 13 level inverter

4.2 *Output Voltage Waveforms for 13 Level Inverter with PO–PWM Method*

Figure 7a, b gives the three phase output voltage and fast fourier analysis of 13 level inverter using APD–PWM method at 0.02 s and 180 V and simultaneously [5].

4.3 *Output Voltage Waveforms for 13 Level Inverter Using CO–PWM Technique*

Figure 8a, b shows the three phase output voltage and FFT analysis obtained which are at time period of 20 ms and amplitude of 180 V. From the above discussions its observed that this method contains more THD compared to other two techniques. The pulses in this method overlap each other [6].

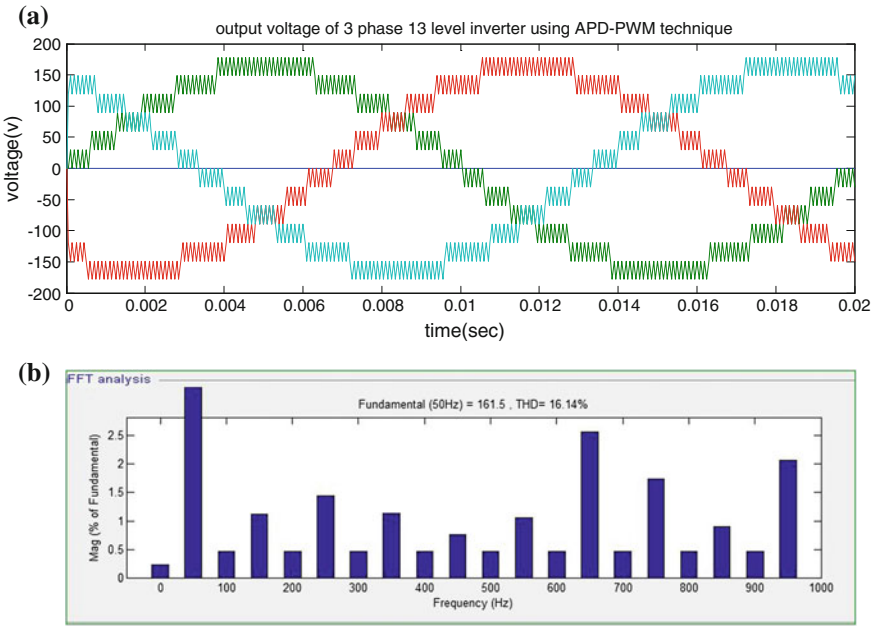


Fig. 7 **a** Obtained three phase waveform for output voltage for 13 level using APD–PWM method **b** FFT analysis for 13 level inverter

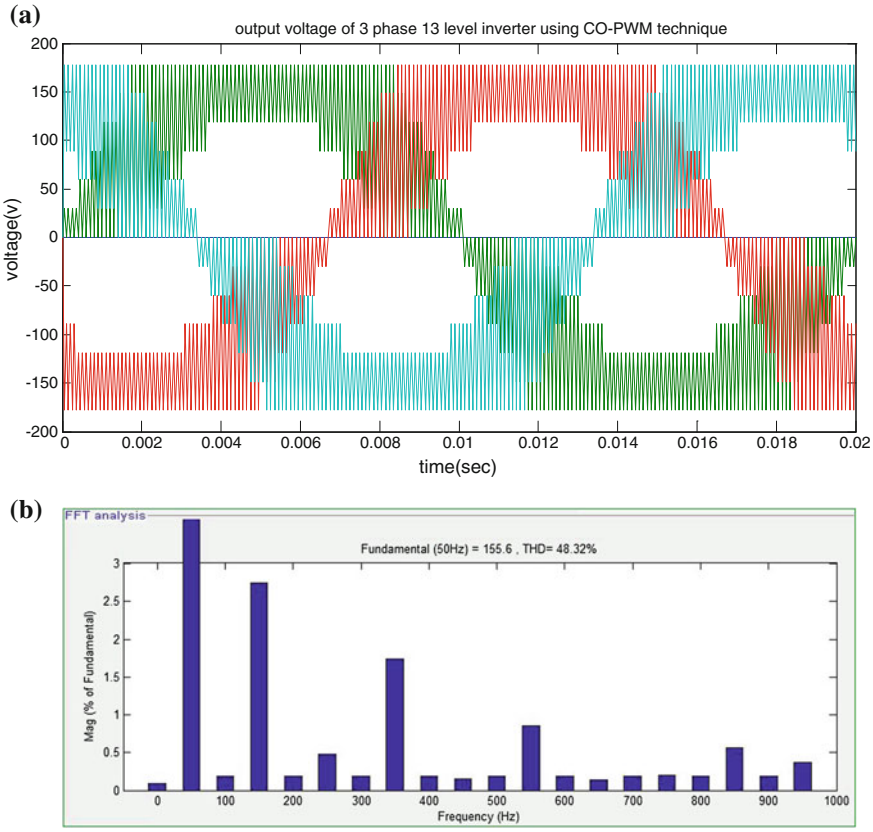


Fig. 8 **a** Obtained three phase waveform for output voltage for 13 level using CO–PWM method **b** FFT analysis for 13 level inverter

4.4 Output Voltage Waveforms for 13 Level Inverter for VF–PWM Method

Figure 9a shows the three phase output voltage obtained at time period of 20 ms and amplitude of 180 V and Fig. 9b gives the FFT analysis of the above three phase waveform using VF–PWM method. The THD of this method is very low 12.51 compared to all other three methods [7].

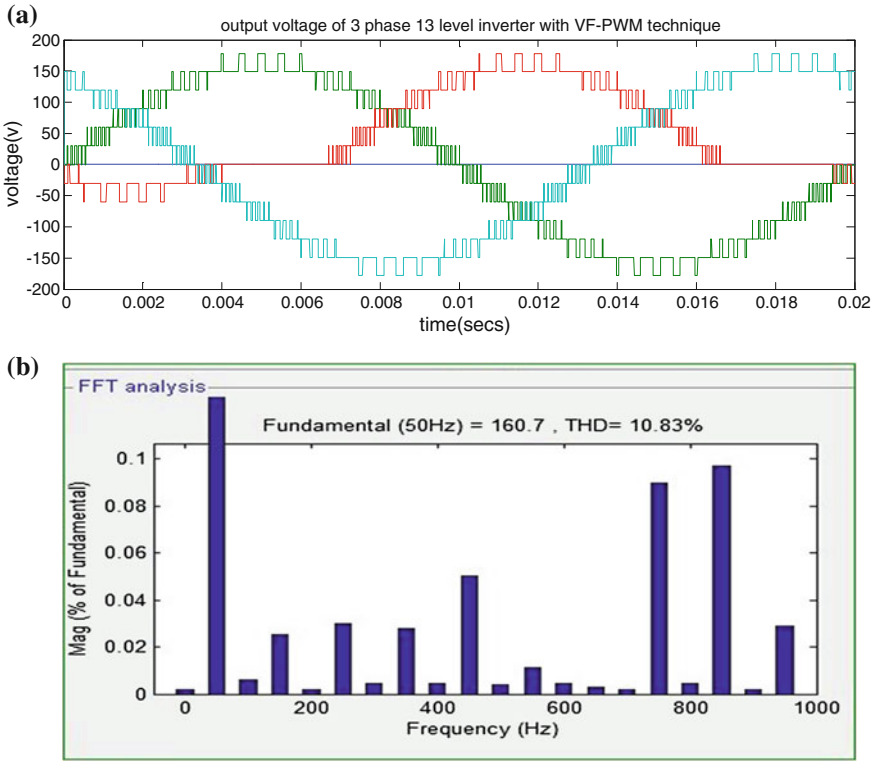


Fig. 9 **a** Obtained three phase waveform for output voltage for 13 level using VF–PWM method **b** FFT analysis for 13 level inverter

4.5 Output Voltage Waveforms for 13 Level Inverter Using Frequency Varying Technique Using Filter

The obtained pure sinusoidal waveforms are three phase output voltage waves using LC filter at time period of 0.2 ms and 180 V amplitude which is shown in Fig. 10a and FFT analysis is shown in Fig. 10b [8].

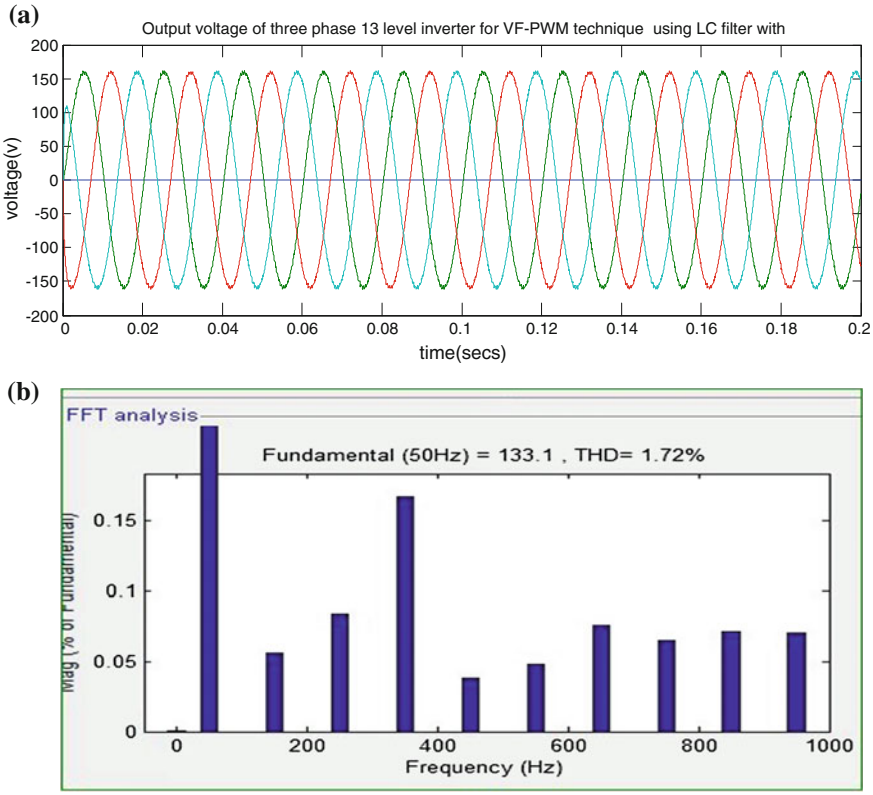


Fig. 10 **a** Obtained three phase waveform for output voltage for 13 level using VF–PWM method with LC filter **b**. FFT analysis for 13 level inverter using VF–PWM method using LC filter

Table for THD for 13 level inverter with various PWM methods

S. No.	Pulse width modulation techniques	% of THD for 13 level inverter
1	IPD–PWM technique	15.18
2	APD–PWM technique	16.14
3	CO–PWM technique	48.32
4	VF–PWM techniques	10.83
5	VF–PWM with LC Filter	1.72

5 Conclusion

In this paper a new configuration of thirteen level inverter by reducing switches is done. Various pulse width modulation techniques have been simulated and compared using MATLAB. From the obtained simulation results, its observed that VF–

PWM produces less harmonics compared to other techniques. This PWM technique is the best PWM technique for inverter switching compared to other three techniques. In this PWM method, inductance is used in series with output voltage to reduce THD of 1.72% and obtain pure sine wave.

References

1. Singh, M.D., Khanchandani, K.B.: Inverters (Chap. 9). In: Power Electronics, 2nd edn., pp. 536–592 (2015)
2. Bimbhra, P.S.: Fourier Analysis. In: Power Electronics, 4th edn., pp. 691–698 (2006)
3. Baker, R.H., Bannister, L.H.: Electric power converter. U.S. Patent 3 867 643, Feb 1975
4. Rashid, M.H.: Types of Inverters. Power Electronics, Circuits, Devices, and Applications, 3rd edn., pp. 408–419
5. Khomfoi, S., Tolbert, L.M.: Multilevel Power Converters (Chap. 17). In: Power Electronics Handbook. 2nd edn., Elsevier, Amsterdam, ISBN 978-0-12-088479-7, pp. 451–482 (2007)
6. Gupta, K.K., Jain, S.: Topology for multilevel inverters to attain maximum number of levels from given DC sources. lET Power Electron. **5**(4), 435–446 (2012)
7. Sen, P.C.: Principles of Electrical Machines Power Electronics. 3rd edn, Wiley, New York (2013) ©2014
8. Holmes, D.G., Lipo, T.A.: Pulse Width Modulation For Power Converters, Wiley, New York (2003)

A State-of-the-Art Review on Synchrophasor Applications to Power Network Protection

M.S. Prabhu and Paresh Kumar Nayak

Abstract The demand for electricity supply has been increased many folds over the last few decades. However, the growth in the electric infrastructure has not been increased accordingly due to deregulation of the energy markets, economic and environmental reasons. In present days, power networks are most often operated closer to their stability limit to fulfill the growing electricity demand. As a result, the security and safety of the power system today is at risk. Investigation on large blackouts in the recent past show that maintaining system reliability and integrity becomes more and more difficult due to reduced transmission capacity margins and increased stress on the system. Under the stressed operating condition, the widely-used distance relaying based transmission line protection schemes are susceptible to maloperation. The use of series-compensated and multiterminal lines is another concern for the distance protection scheme. At the same time, the present advancements in the wide-area measurement systems (WAMS) using synchrophasors has shown potential for ensuring improved protection for different power networks operating even at critical conditions. In this paper, the authors first investigate the limitations of existing distance relays while protecting different power networks during stressed operating conditions. Then, an extensive review is made on the application of synchrophasor based WAMS technology for reliable power system protection. The objective of the present study is mainly to bring the attention of the researchers from academic institutions, industries and utility grid on the possible applications of synchrophasors based WAMS technology for ensuring improved protection to today's power system.

Keywords Distance relay · Multiterminal line · Series compensation
Synchrophasor · WAMS · Wide-area backup protection

M.S. Prabhu (✉) · P.K. Nayak
Department of Electrical Engineering, IIT (ISM) Dhanbad, Dhanbad 826004, India
e-mail: msprabhuceg@gmail.com

P.K. Nayak
e-mail: pareshkumar.nayak@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_52

1 Introduction

The power utilities today are most often forced to operate transmission lines closer to their stability limits to fulfill the ever-increasing electricity demand, the economical, environmental and the recent regulatory requirements. Such operating conditions cause power networks more susceptible to disturbances and protection schemes, an integral part of the power system, are under more scrutiny. Even with new generation protection schemes, the power system today is not free from blackouts. Investigations on large disturbances reveal that maloperation of protection schemes in a power system plays important role in triggering cascaded tripping [1]. Although complete immunity from such catastrophic failure is not easy to achieve, new developments on transmission line protection employing numerical relays [2] show promising signs that cascading system outages can be minimized. Recent developments in communication and information technologies have drawn attention for the use of synchrophasors based WAMS for reliable power system protection [3–5].

The protection of transmission lines in a complex power network is a very challenging task. A variety of scheme is employed in practice for protecting power networks. Among them, digital distance relaying based scheme is the preferable one. It computes the apparent impedance by using the measured voltage and current signals. The scheme operates when the computed impedance falls within a preset value. It has typically three zones of protections, namely, zone-1, zone-2, and zone-3. In this scheme, primary protection is provided by zone-1. Zone-2 and zone-3 provide the backup protection to adjacent sections of the protected line [6].

The limitation of building new transmission lines due to right-of-restrictions demands optimal utilization of existing lines. The installation of series-capacitors in the existing lines is an alternative solution for fulfilling the above needs. However, the installation of series-capacitors in the existing lines creates problem to distance relaying based protection schemes [7, 8]. The installation of metal oxide varistor (MOV) for providing protection to the series devices complicates the problem further.

Multiterminal lines are used in some cases both in transmission and subtransmission levels due to various technical reasons. Among the different configurations, three-terminal line configuration is the most preferred one. However, the existing protection schemes including the distance relays find difficulty in protecting such lines [9, 10].

Zone-3 provides backup protection to the longest line of the neighboring section. However, the use of only local measurements by zone-3 element makes it susceptible to stressed power system operating conditions. Zone-3 maloperation under such situation plays an important role in initiating the cascade tripping [11]. For example, the Northeast blackout in 2003 [12] and the recent 2012 blackouts in India

[13] were initiated due to zone-3 maloperation under overload and power swing conditions. Moreover, the growing complexity of power system configuration creates problems in coordinating several backup zones and may induce hidden failures [14]. In the recent years, synchrophasors based WAMS has shown potential to provide more reliable network protection [15]. Significant research has been reported in the last decade to improve the performance of existing protection schemes using such technology. In this paper, firstly, a brief discussion on the architecture of the synchrophasor base WAMS technology is provided. Then, in the second step, a representative survey on the available applications of synchrophasor based WAMS technology for reliable power system protection is carried out and is presented in the following sections.

2 Wide-Area Phasor Measurement Technology

Synchrophasor provides phasor values of the time domain voltage and current signals measured at different locations of a power system. These phasors are time stamped to the universally used global positioning system (GPS). The complete setup used for providing synchronized phasors are called phasor measurement unit (PMU). The schematic of a typical PMU is shown in Fig. 1. The detail on PMU technology is provided in [16].

The PMUs in a WAMS are installed at selected locations of the power system where the measurements are carried out. The synchronized phasor data are collected at the phasor data concentrators (PDCs) and passed on to the central computer system (CCS) through communication medium. The analysis of data at the central computer center provides the real-time view of the whole power system. The data is refreshed at each one-cycle interval of power frequency. The schematic diagram of PMUs based WAMS technology is shown in Fig. 2 [16].

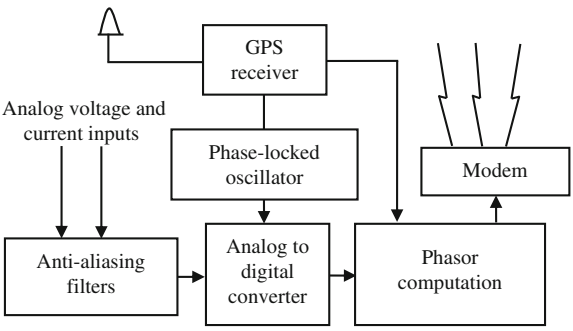


Fig. 1 Schematic of a typical phasor measurement unit

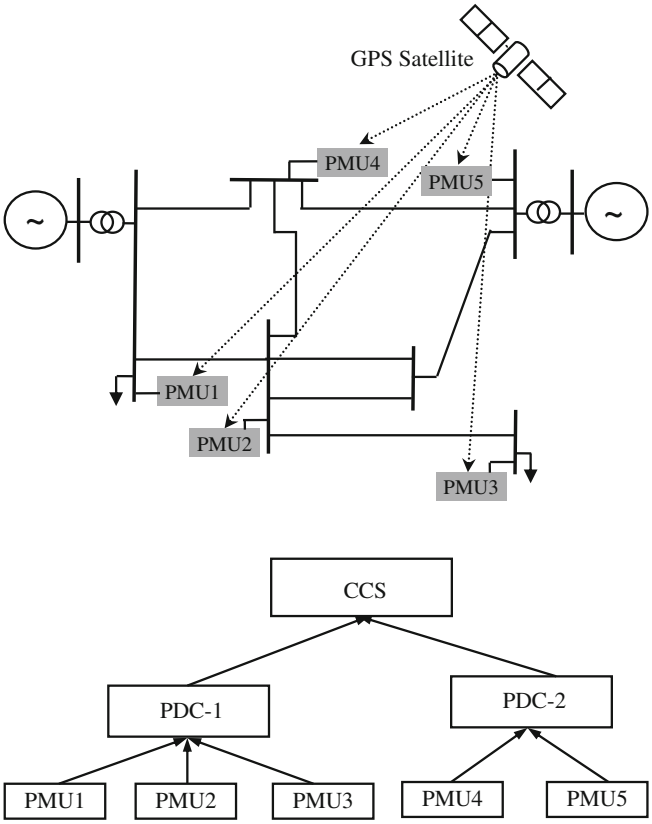


Fig. 2 Schematic diagram of a typical wide-area measurement system

3 Review on Synchrophasor Application for Improved Protection of Power Networks

Today, PMUs based WAMS technology is matured enough for applying into power system for accomplishing improved real time monitoring, control, and protection task. A brief review on the overall applications of such technology is provided in [17]. In the present work, we have made an extensive review on the applications of synchrophasors based WAMS technology to overcome the limitations of distance relaying based protection schemes applied to different power networks at different operating conditions.

3.1 Protection of Series-Compensated Transmission Lines Using Synchrophasors

The installation of series-capacitors into an existing transmission line increases its power transfer capability. Power system stability improvement, improved voltage regulation, loss reduction and flexible control of the power flow are some of the other benefits of series compensation [18–22]. However, the installation of series capacitors and the protection devices (the metal oxide varistors (MOVs) and/or air-gap) of the series-capacitors makes the line protection more complex. The various phenomena such as voltage and/or current inversion, additional transients caused due to the operation of the air-gap, subharmonic oscillations in the voltage and current waveforms etc., are seen in such lines during a fault condition. These above phenomena are dependent on various factors such as the type of faults, location of faults, inception angle of the fault, level of compensation etc. Because of the above reasons, the existing distance relaying scheme using only local information find difficulty for protecting such lines [23–25]. To overcome the limitations of distance relaying based protection scheme, recently synchrophasor data in WAMS environment are utilized by many researchers for exploring enhanced protection to such lines. The detailed review on the available synchrophasor based protection schemes applied to series-compensated lines is provided below.

A fault location algorithm is proposed in [26] for a series-compensated line using synchrophasor measurements from both ends of the line. The scheme does not require the modeling and mode of operation of the series device for voltage drop calculation as is done in the traditional fault location algorithms. This helps the method to eliminate the fault location errors as is seen in the traditional fault location algorithms. The scheme operates in two steps. First one is called prelocation step and the second one is called correction step. Prelocation step is used to compute the voltage drop and the correction step is used to estimate the location of the fault. It is claimed that the design and implementation of the scheme is very easy as the method is independent of the operating mode of the series capacitor. However, the algorithm assumes that the impedance of the fault is a pure resistance and the fault type is known. Another technique is reported in [27] for estimating the location of the fault in a line possessing series compensation. The scheme utilizes voltage and current samples at both ends of the line for locating the fault. It is claimed that the method gives a stable performance for a wide variety of fault resistances, source impedances and fault inception angles. The method neither needs modeling nor knowledge on the operating mode of the series device for accomplishing the location estimation task.

A fault location algorithm is reported in [28] for a double-circuit possessing series compensation. In this scheme, the voltage phasor of the local terminal and the current phasors of both ends are utilized for estimating the location of the fault. In this scheme, also, the model of the series capacitor is not required like traditional fault location algorithms. The algorithm works in three steps. The fault classification task is accomplished in the first step using synchrophasor data. Then, the

scheme uses two criteria for fault location. First, the fault point voltages and currents are represented in terms of the two ends of the line voltages and currents and then the location of the fault is estimated. The performance of the scheme is independent of source impedances, mutual coupling and fault path resistance. However, the computational burden of the scheme is high.

3.2 *Protection of Multi-terminal Transmission Lines Using Synchrophasors*

Distance relaying based protection schemes, using only local information faces underreaching and overreaching problems when used for the protection of multi-terminal lines. In order to improve the performance of distance protection schemes on the above issues, communication assisted or unit protection schemes are employed for protecting such lines. Permissive overreaching transfer trip (POTT), direct underreaching transfer trip (DUTT) and directional comparison blocking (DCB) are the three most widely used communication assisted protection schemes. However, POTT and DCB based protection schemes are susceptible to maloperation during power swing [10]. Recently, synchrophasor assisted unit protection schemes are proposed for providing improved protection to such lines. The detailed review on the available multiterminal line protection schemes using synchrophasors data is provided below [29–35].

Voltage and current phasors at all ends of a multiterminal line are used in [29] for locating faults in any branch of the multiterminal line configuration. The technique has used voltage differences of different ends and then gradually shortens a multiterminal line to a two-end line configuration containing the faulted branch. Then, the fault location task is accomplished by using a reactive power based method. In [30], a precise fault location algorithm is proposed by utilizing the voltage and current phasors of the synchrophasors placed only at the two ends of the three-terminal line. The technique works in two steps. In the first step, the faulted branch is identified and in the second step, the location of the fault is estimated on the faulted branch. The superimposed components of the phasor values of voltages and currents are used for identifying the faulted branch. The superimposed component of positive-sequence voltages and currents and postfault positive-sequence voltage and current are used for estimating the location of the fault on the faulted branch.

In [31], a technique is proposed for estimating the fault location in a multiterminal line and is based on simple circuit principles. The scheme utilizes phasor values of voltage and current provided by the synchrophasors placed at all terminals of the multiterminal line for identifying the faulted section. The location of the fault is estimated by using only voltage phasors before and after a fault. It is claimed that the scheme performs equally for both transposed and untransposed transmission lines. The performance of the scheme is not affected significantly by CT errors,

prefault conditions, and fault resistance. However, the scheme needs the calculation of exact source impedance for determining the correct location of the fault. Another fault location technique is proposed in [32] by using synchronized currents from three ends of a three-terminal line along with the voltage from the terminal where the fault algorithm is executed. The method forms three subroutines by using currents from three ends of the three-terminal line along with the local voltage to identify the faulted line section. The location estimation error is claimed to be less than 0.2%. However, the computational burden of the scheme is high as it requires Newton-Raphson iterative operation for accomplishing the fault location task.

Fault location estimation task is performed in the N-terminal transmission line in [33] using synchronized measurements of voltage and current from all terminals. The scheme is applicable to short and long lines, nonhomogeneous lines, and double circuit lines. The error is claimed to be less than 1% under various fault conditions. However, the scheme requires the calculation of $(N - 1)$ two-terminal indices for performance evaluation which increases the computational burden. Another method is proposed in [34] for locating a fault in a three-terminal line using three end voltages and currents. In this method, a two-end fault location technique is extended to a three-end technique. The scheme has the ability to discriminate internal faults from external faults as well as locating the fault. The computational burden is less as the scheme neither requires fault type selection nor iterative operations like [32]. However, the method exhibits poor performance for untransposed lines.

A synchrophasor assisted three-terminal transmission line protection scheme is proposed in [35]. Here, the scheme first computes the tee-point positive-sequence voltage by utilizing the three-end voltage and current. The one-cycle superimposed components of the voltage are estimated at the tee-point is and is compared with the one-cycle superimposed components of the terminal voltage for discriminating internal faults from external faults. The scheme can also able to detect faults occurring during power swing condition.

3.3 Synchrophasors Assisted Wide-Area Backup Protection

The wide-area backup protection (WABP) scheme based on faulted line identification (FLI) is proposed by many researchers in the recent years. It is claimed by the researchers that a more secured and faster backup protection can be achieved using this technique. Because in this scheme coordination among different backup zones is not required like in a three-stepped distance protection scheme. Different WABP schemes based on FLI are reported in [36–41].

A WABP is reported in [36] which operate in two steps. In the first step, the positive-sequence voltages are estimated at selected substations of the power system and the minimum of them is used for identifying the bus nearest to the fault. Once the faulted substation bus is identified, then the current angles for all lines connecting to the faulted substation bus are utilized for faulted line identification.

However, the scheme shows poor performance for detecting high resistance faults. In [37], a two agent-based backup protection scheme built on the low latency communication network is proposed. A supervised zone-3 backup protection is reported in [38] by utilizing the information from a synchrophasor based state estimator. A WABP scheme is reported in [39], where the fault voltages and currents are utilized for faulted line identification. Based on the network topology and PMU placement technique, protection correlation regions (PCRs) are obtained by using the subsets of buses. Then current differential principle is employed in each PCR for faulted line identification.

A WABP scheme is proposed in [40] which operates mainly in two parts. In the first part, the fault incident bus (FIB) is identified by utilizing the sequence voltages at different buses in the power system. Once the FIB is identified, then the fault component voltage at the other terminal of the line is calculated by utilizing the measured voltage and current phasors at the local end. The ratio of the calculated values and the measured values of the voltage phasors are utilized for faulted line identification. An adaptive WABP scheme is proposed in [41], where the fault detection and the location task is accomplished by using the information from minimum number of PMUs placed at selected locations. First, according to PMU placement and system topology, backup protection zones (BPZs) are created by using the subsets of lines and buses. The zero and positive-sequence currents are utilized together for determining the faulted BPZ. Then, the voltages and currents of the faulted BPZ are used for fault identification and location estimation.

The performances of all the aforementioned WABP schemes are not tested for transmission lines possessing series-compensation. A WABP scheme applicable to both series-compensated and normal transmission lines is proposed in [42]. The scheme operates in two steps. In the first step, magnitudes of sequence voltages at different buses are computed and compared for faulted bus identification. Once the faulted bus is identified, the sign of the angle between sequence voltages and currents are used for identifying the faulted line. The reported WABP scheme is also evaluated for faults occurring under power swing condition.

4 Conclusion

The limitations of distance relaying based protection schemes for different power networks such as series-compensated and multiterminal transmission lines are discussed first in this paper. Then, the limitations of zone-3 backup protection of the distance relay using only local information during stressed operating conditions are discussed. The alternative solutions to the above-mentioned problems of distance relaying scheme protecting different power networks operating at various critical conditions are explored using synchrophasor assisted WAMS technology. The detailed review, merits, and demerits of available schemes protecting transmission lines using synchrophasor technology are carried out in this paper. The authors

believe that the contents of the presented paper will be useful to both academic researchers and practicing engineers for further study on the application of synchrophasor based WAMS technology for reliable power system protection.

References

1. IEEE Power System Relay Committee: Performance of relaying during wide area stressed conditions. Available: www.pes-psrc.org (2008)
2. Kumar, J., Venkata, S., Damborg, M.: Adaptive transmission protection: concepts and computational issues. IEEE Trans. Power Del. **4**(1), 177–185 (1989)
3. De La Ree, J., Centeno, V., Thorp, J.S., Phadke, A.G.: Synchronized phasor measurement applications in power systems. IEEE Trans. Smart Grid **1**, 20–27 (2010)
4. Martin, K., Hamai, D., Adamiak, M., Anderson, S., Begovic, M., Benmouyal, G., Brunello, G., Burger, J., Cai, J., Dickerson, B., Gharpure, V., Kennedy, B., Karlsson, D., Phadke, A.G., Salj, J., Skendzic, V., Sperr, J., Song, Y., Huntley, C., Kasztenny, B., Price, E.: Exploring the IEEE standard c37. 118–2005 synchrophasors for power systems. IEEE Trans. Power Del. **23**, 1805–1811 (2008)
5. Phadke, A., Thorp, J.: Communication needs for wide area measurement applications. In: Critical Infrastructure (CRIS), IEEE, 5th International Conference, pp. 1–7, Beijing, China (2010)
6. Horowitz, S.H., Phadke, A.G.: Power System Relaying, vol. 22. Wiley, New York (2008)
7. Novosel, D., Phadke, A.G., Saha, M.M., Lindahl, S.: Problems and solutions for microprocessor protection of series compensated lines. In: Developments in Power System Protection, IET, Sixth International Conference (Conf. Publ. No. 434), pp. 18–23 (1997)
8. Altuve, H.J., Mooney, J.B., Alexander, G.E.: Advances in series-compensated line protection. In: Proceedings of the 35th Annual Western Protective Relay Conference, Spokane, WA (2008)
9. IEEE Power system relaying committee: Protection aspects of multiterminal lines, IEEE Publication No. 79 TH0056-2-PWR (1979)
10. NERC technical document prepared by the system protection and control task force of the NERC planning committee: The complexity of protecting three-terminal transmission lines (2006)
11. Horowitz, S., Phadke, A.G.: Third zone revisited. IEEE Trans. Power Del. **21**, 23–29 (2006)
12. NERC: NERC recommendations to August 14, 2003 blackout-prevent and mitigate the impacts of future cascading blackouts (2003)
13. Report of the enquiry committee on grid disturbance in northern region on 30th July 2012 and in northern, eastern and north-eastern region on 31st July 2012. Technical Report, Power Grid, New Delhi, India, Aug. 2012. Available: www.powermin.nic.in/pdf/GRID-ENQ-REP-16-8-12.pdf
14. Phadke, A.G., Thorp, J.S.: Expose hidden failures to prevent cascading outages [in power systems]. IEEE Comput. Appl. Power **9**, 20–23 (1996)
15. Xiao, J., Wen, F., Chung, C.Y., Wong, K.P.: Wide-area protection and its applications—a bibliographical survey. In: 2006 IEEE PES Power Systems Conference and Exposition, pp. 1388–1397 (2006)
16. Phadke, A.G., Thorp, J.S.: Synchronized Phasor Measurements and their Applications. Springer, Berlin (2008)
17. Aminifar, F., Fotuhi-Firuzabad, M., Safdarian, A., Davoudi, A., Shahidehpour, M.: Synchrophasor measurement technology in power systems: Panorama and state-of-the-art. IEEE Access **2**, 1607–1628 (2015)

18. Coursol, M., Nguyen, C.T., Lord, R., Do, X.D.: Modeling mov-protected series capacitors for short-circuit studies. IEEE Trans. Power Del. **8**, 448–453 (1993)
19. Saha, M.M., Kasztenny, B., Rosolowski, E., Izykowski, J.: First zone algorithm for protection of series compensated lines. IEEE Trans. Power Del. **16**, 200–207 (2001)
20. Kasztenny, B.: Distance protection of series compensated lines—problems and solutions. In: Proceedings of the 28th Annual Western Protective Relay Conference, Spokane, WA (2001)
21. Sidhu, T.S., Khederzadeh, M.: Series compensated line protection enhancement by modified pilot relaying schemes. IEEE Trans. Power Del. **21**, 1191–1198 (2006)
22. Nayak, P.K., Pradhan, A.K., Bajpai, P.: A fault detection technique for the series-compensated line during power swing. IEEE Trans. Power Del. **28**, 714–722 (2013)
23. Grunbaum, R., Strömberg, G., Wikström, K.: On the impact of series compensation on line protection and TRV. Relay Protection and Substation Automation of Modern Power Systems, Moscow/Cheboksary (2007)
24. Gajbhiye, R.K., Gopi, B., Kulkarni, P., Soman, S.: Computationally efficient methodology for analysis of faulted power systems with series-compensated transmission lines: a phase coordinate approach. IEEE Trans. Power Del. **23**, 873–880 (2008)
25. Parikh, U.B., Das, B., Maheshwari, R.P.: Combined wavelet-SVM technique for fault zone detection in a series compensated transmission line. IEEE Trans. Power Del. **23**, 1789–1794 (2008)
26. Yu, C.S., Liu, C.W., Yu, S.L., Jiang, J.A.: A new pmu-based fault location algorithm for series compensated lines. IEEE Trans. Power Del. **17**, 33–46 (2002)
27. Sadeh, J., Adinehzadeh, A.: Accurate fault location algorithm for transmission line in the presence of series connected facts devices. Int. J. Electr. Power Energy Syst. **32**, 323–328 (2010)
28. Apostolopoulos, C., Korres, G.: Accurate fault location algorithm for double-circuit series compensated lines using a limited number of two-end synchronized measurements. Int. J. Electr. Power Energy Syst. **42**, 495–507 (2012)
29. Abe, M., Otsuzuki, N., Emura, T., Takeuchi, M.: Development of a new fault location system for multi-terminal single transmission lines. IEEE Trans. Power Del. **10**, 159–168 (1995)
30. Lin, Y.H., Liu, C.W., Yu, C.S.: A new fault locator for three-terminal transmission lines using two-terminal synchronized voltage and current phasors. IEEE Trans. Power Del. **17**, 452–459 (2002)
31. Brahma, S.M.: Fault location scheme for a multi-terminal transmission line using synchronized voltage measurements. IEEE Trans. Power Del. **20**, 1325–1331 (2005)
32. Izykowski, J., Rosolowski, E., Saha, M.M., Fulczyk, M., Balcerek, P.: A fault-location method for application with current differential relays of three-terminal lines. IEEE Trans. Power Del. **22**, 2099–2107 (2007)
33. Liu, C.W., Lien, K.P., Chen, C.S., Jiang, J.A.: A universal fault location technique for n-terminal transmission lines. IEEE Trans. Power Del. **23**, 1366–1373 (2008)
34. Lin, T.C., Lin, P.Y., Liu, C.W.: An algorithm for locating faults in three-terminal multisection nonhomogeneous transmission lines using synchrophasor measurements. IEEE Trans. Smart Grid **5**, 38–50 (2014)
35. Nayak, P.K., Pradhan, A.K., Bajpai, P.: A three-terminal line protection scheme immune to power swing. IEEE Trans. Power Del. (2015). doi:10.1109/TPWRD.2014.2387873
36. Eissa, M., Masoud, M.E., Elanwar, M.M.M.: A novel back up wide area protection technique for power transmission grids using phasor measurement unit. IEEE Trans. Power Del. **25**, 270–278 (2010)
37. Lin, H., Sambamoorthy, S., Shukla, S., Thorp, J., Mili, L.: Ad-hoc vs. supervisory wide area backup relay protection validated on power/network co-simulation platform. In: Proceedings of the 17th Power Systems Computation Conference (2011)
38. Navalkar, P.V., Soman, S.A.: Secure remote backup protection of transmission lines using synchrophasors. IEEE Trans. Power Del. **26**, 87–96 (2011)

39. Ma, J., Li, J., Thorp, J.S., Arana, A.J., Yang, Q., Phadke, A.G.: A fault steady state component-based wide area backup protection algorithm. IEEE Trans. Smart Grid **2**, 468–475 (2011)
40. He, Z., Zhang, Z., Chen, W., Malik, O.P., Yin, X.: Wide-area backup protection algorithm based on fault component voltage distribution. IEEE Trans. Power Del. **26**, 2752–2760 (2011)
41. Neyestanaki, M.K., Ranjbar, A.M.: An adaptive PMU-based wide area backup protection scheme for power transmission lines. IEEE Trans. Smart grid **6**, 1550–1559 (2015)
42. Nayak, P.K., Pradhan, A.K., Bajpai, P.: Wide-area measurement-based backup protection for power network with series compensation. IEEE Trans. Power Del. **29**, 1970–1977 (2014)

Performance Analysis of Current-Mode Interconnect System in Presence of Process, Voltage, and Temperature Variations

Yash Agrawal, Rutu Parekh and Rajeevan Chandel

Abstract The present paper analyzes process, voltage and temperature variation effects in current-mode (CM) interconnect system. CM signaling is considered as one of the advanced signaling schemes and effective in achieving high performance in integrated circuits. The impact of variability has been accessed using technology scaling, parametric and process corner analyses. It is analyzed that FF process corner model is the fastest while SS model results in least power dissipation in the circuit. Parametric sensitivity analysis reveals that variation in threshold voltage and supply voltage dominantly impacts the propagation delay and power dissipation, respectively, in the system. The variability effects in CM interconnect system are analyzed for scaled technology nodes from 130 to 32 nm. SPICE is used for simulative analyses.

Keywords Current-mode signaling · On-chip interconnects · Process, voltage and temperature (PVT) · Variability

1 Introduction

The advancements in nanofabrication of integrated circuit (IC) technology have made feasible the fabrication of billions of transistors on a single chip. This has led to compactness of ICs with increased functionality on the same chip area. However,

Y. Agrawal (✉) · R. Parekh
VLSI & Embedded Systems Research Group, Dhirubhai Ambani Institute of Information and Communication Technology, Ganghinagar 382007, Gujarat, India
e-mail: yash_agrawal@daiict.ac.in

R. Parekh
e-mail: rutu_parekh@daiict.ac.in

R. Chandel
Department of Electronics & Communication Engineering, National Institute of Technology, Hamirpur 177005, Himachal Pradesh, India
e-mail: rchandel@nith.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_53

at miniaturized technology nodes, process, voltage, and temperature (PVT) induced variations have aggravate effect and become a major concern in achieving sustainable outputs [1]. Thus, comprehending and analyzing PVT variation effects have become an important design check in ICs.

On-chip interconnects constitute a significant portion of an IC. Interconnects dominantly impact the circuit performance namely power dissipation, delay, crosstalk and noise in the circuit. To mitigate these non-ideal effects, various circuit levels, architectural and signaling schemes have been investigated [2]. Among the various techniques investigated so far, current-mode (CM) signaling scheme for on-chip interconnects has been examined as one of the effective measures to achieve high performance in a circuit [3, 4]. Unlike conventional voltage-mode signaling scheme, CM signaling scheme has smaller impedance termination. This is achieved by using specialized CM receivers [4]. The interconnects using CM signaling scheme possess lesser delay, higher throughput, smaller energy dissipation and lower electrostatic induced damages of MOSFETs. This makes CM interconnect system aptly suitable for IC designs.

At nanoscale dimensions, the physical parameters of the interconnect are vulnerable to variations due to finite limitations of current lithography, etching and other state-of-the-art fabrication processes [1, 5]. The variations in interconnect dimensions affect the parasitic electrical parameters of the interconnect viz. resistance, inductance, and capacitance. This in turn affects the overall performance of system. The effect of PVT variations in conventional voltage-mode interconnect system has been investigated by many researchers [1, 2, 5]. However, the same has been relatively less explored for advanced on-chip current-mode interconnect system. Consequently, this has been enthrallingly and comprehensively analyzed in the current research paper. The rest of the paper is constituted as follow. Section 2 introduces CM interconnect system model. The effect of variability in CM interconnect system has been analyzed and presented in Sect. 3. Finally, the concluding remarks are made in Sect. 4.

2 Current-Mode Interconnect System

The schematic of CM interconnect system is shown in Fig. 1. The driver is realized by practical CMOS inverter. The interconnect is modeled by distributed resistance (R_{dis}), inductance (L_{dis}) and capacitance (C_{dis}) parasitic elements. The interconnect parasitics are evaluated using [6].

The receiver in CM interconnect system is of low impedance value. This is modeled and equivalently presented by load capacitance (C_L) and resistance (R_L) that are configured in parallel at the receiver-end [7]. The low impedance termination in CM interconnect system reduces the voltage swing over interconnects. This causes fast charging and discharging of parasitic interconnect node capacitances. Thereby the overall circuit delay is reduced.

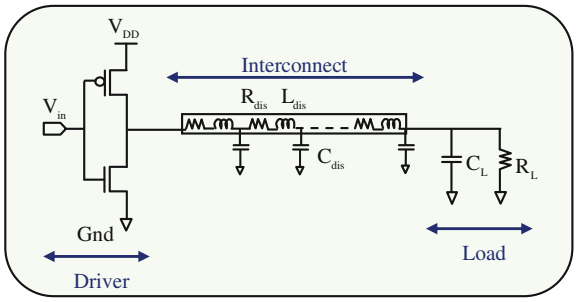


Fig. 1 Schematic of current-mode interconnect system

3 Variability Analysis in Current-Mode Interconnect System

This section details the effect of technology scaling, process corner variations and parameter sensitivity analyses for on-chip CM interconnect system. The device and interconnect dimensions are as per ITRS [8]. The interconnect parasitics viz. R_{dis}, L_{dis}, and C_{dis} are 3.18 MΩ/m, 1.48 μH/m, and 21.8 pF/m, respectively. The value of load impedance R_L and C_L are 1 kΩ and 0.5 fF, respectively [3]. Interconnect length is 10 mm. The technology is varied from 32 to 130 nm. The analyses have been carried out using Tanner SPICE EDA tool [9].

3.1 Impact of Temperature and Technology Scaling

In pursuit to improve the performance and enhance the functionality of a system, transistor density in an IC increases. This is due to feasibility of down scaling MOS transistor dimensions, while global interconnects undergo reverse scaling. In current-mode logic designs, most of the ON switching operation occurs during saturation mode [10]. The current (I_{DS}) in n-channel MOS transistor in the saturation mode is presented in (1) [11]

$$I_{DS} = \left(\frac{1}{2}\right)\mu_{eff}\left(\frac{\varepsilon_{ox}}{T_{ox}}\right)\left(\frac{W}{L_{eff}}\right)(V_{GS} - V_{th})^{\alpha} \tag{1}$$

where V_{GS} represents gate to source voltage and V_{th} depicts threshold voltage of NMOS transistor. α is velocity saturation index. The value of α is 1.3 and 2 for short and long channel devices, respectively [10]. ε_{ox} is dielectric constant. T_{ox} denotes gate oxide thickness. μ_{eff} is the effective mobility of charge carriers. W and and L_{eff} are channel width and effective channel length, respectively.

In [10], it is analyzed that current in shorter channel devices is lesser than longer ones in CM logic designs. This is because of short channel effects which consequence in saturation of carrier velocity in the MOS devices. It is further investigated

that saturation current reduces for short channel devices. This implies that current decreases with the down scaling of technology. This in turn, affects the overall performance of the CM interconnect system. Thus technology scaling has a prominent effect on VLSI circuit performance.

Temperature is another parameter that significantly impacts the performance of electronic circuits. This is particularly because the effective mobility of charge carriers and MOSFET threshold voltage are temperature dependent [12]. Effective mobility is dependent on temperature (T) and is given in (2) as [1, 5, 10]

$$\mu_{\text{eff}}(T) = \mu(T_{\text{r}})(T/T_{\text{r}})^{-\kappa_1} \tag{2}$$

where T_{r} is room temperature in Kelvin. κ_1 is technology-dependent constant parameter. It ranges from 1.2 to 2. It can be examined from (2) that effective mobility has negative correlation with temperature. It is well proven that current is directly proportional to the effective mobility [1, 10, 12]. Thus it can be envisaged that as temperature increases, effective mobility decreases. This in turn decreases current in the circuit. The smaller current decreases the switching speed and power dissipation in the circuit. The variations in effective mobility directly impact current in the circuit.

The threshold voltage of NMOS is given in (3) as [12]

$$V_{\text{th}} = \left(\phi_{\text{ms}} - \frac{Q_{\text{ss}}}{C_{\text{ox}}}\right) + \frac{\sqrt{2\varepsilon_{\text{s}} q N_A (2\phi_B)}}{C_{\text{ox}}} + (2\phi_B) \tag{3}$$

where ϕ_{ms} is metal (or polysilicon) to semiconductor work function difference, Q_{ss} represents density of oxide charge, N_A denotes concentration of dopants in substrate, q is the charge on electron, ε_s is dielectric constant of the substrate, C_{ox} is oxide charge per unit area ($=\varepsilon_{\text{ox}}/T_{\text{ox}}$). ϕ_B is Fermi potential difference and is defined in (4) as

$$\phi_{\text{B}} = \frac{kT}{q} \ln\left(\frac{N_{\text{A}}}{n_i}\right) \tag{4}$$

where k denotes Boltzmann constant and n_i represents intrinsic carrier concentration of silicon. Thus V_{th} is much dependent on temperature.

Consequently, temperature is an important variable for analyzing electronic circuits. Thus, the effect of technology scaling and temperature variations on the performance of CM interconnect system is analyzed using driver-interconnect-load model and presented in Figs. 2 and 3, respectively. The technology is scaled from 130 to 32 nm and temperature is varied from −25 to 125 °C.

Figure 2 shows the variation of propagation delay with temperature at varying technology nodes. It is seen that as technology is scaled down, propagation delay in CM interconnect system increases. For instance, at a temperature of 25 °C, the propagation delay is 0.54 ns for 130 nm technology node. However this increases to 1.1 ns for 32 nm technology node. In CM interconnect system, the signal

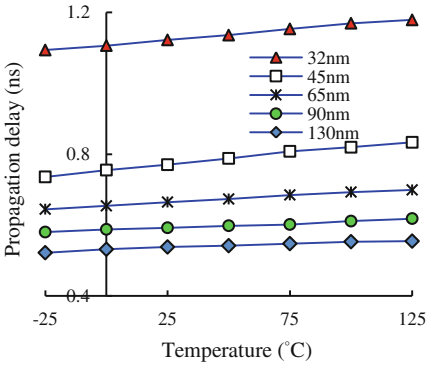


Fig. 2 Variation in propagation delay with scaling of technology nodes

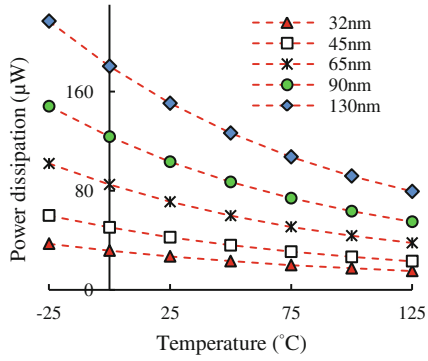


Fig. 3 Variation in power dissipation with scaling of technology nodes

propagation delay is function of current. As the technology is scaled down, the current through both the device and interconnect decreases due to smaller value of supply voltage. This in turn escalates the circuit latency. However, it can be observed that the delay variation is quite nominal with temperature for any technology node. For example, in case of 130 and 32 nm technology nodes, the variation in delay is less than 3 and 5%, respectively, as temperature rises from −25 to 125 °C.

The variation in power dissipation at varying technology nodes is presented in Fig. 3. It is observed that as technology shrinks, power dissipation decreases. It is analyzed that power dissipation is nearly 5.5 times lesser for 32 nm technology node as compared to 130 nm at 25 °C. The lower power dissipation is because of smaller voltage and current at smaller technology nodes. This causes smaller I^2R losses in the circuit. Also it is seen that as temperature increases, power dissipation decreases for all the technology nodes. For example, in 90 nm technology node, the power dissipation decreases from 148.1 to 54.8 μW as temperature increases from −25 to 125 °C. The decrease in power dissipation is because of enhanced scattering and lower current at higher temperatures.

3.2 Process Corner Analysis

In a CMOS technology, the characteristics of NMOS and PMOS transistors may vary due to fluctuations in the fabrication processes. Depending on the characteristics of transistors, different process corners are formed and categorized as Slow-NMOS Slow-PMOS (SS), Slow-NMOS Fast-PMOS (SF), Fast-NMOS Slow-PMOS (FS) and Fast-NMOS Fast-PMOS (FF). MOSFETs with lower threshold voltage are fast while slow MOSFETs have a higher threshold, compared to the nominal or typical threshold voltage value corresponding to a technology node. These variations consequence from the fabrication fluctuations. It is considered that the Typical-NMOS Typical-PMOS (TT) case has no variation effects. The analysis of process corners facilitates to estimate the best and the worst case performance of the system.

Figures 4 and 5 depict propagation delay and power dissipation, respectively, for different process corners for 32 nm technology node. From the figures it is seen that SS process corner model has maximum propagation delay, while decreases sequentially in FS, TT, SF and FF models. It is investigated that FS, TT, SF and FF models, respectively, are 0.56, 1, 2.3 and 3% faster than SS model at 75 °C. In SS model, both the transistors (i.e., NMOS and PMOS) are slow. Consequently, this takes more time to charge and discharge the interconnect node capacitances. This increases the latency in the circuit. On the other hand, power dissipation is least in SS model. Higher threshold voltage in slow transistors, leads to lesser short circuit power dissipation [11]. The power dissipation increases sequentially in FS, TT, SF and FF models. It is analyzed that SS model has nearly 17, 48, 90 and 112% lesser power dissipation than FS, TT, SF and FF models, respectively. The analyses reveal a trade-off between power dissipation and propagation delay. It can be envisaged that for high speed applications FF model is the best, whereas SS model is advantageous for low power applications.

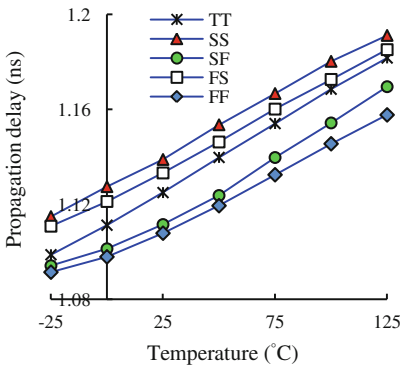


Fig. 4 Variation in propagation delay for different process corners

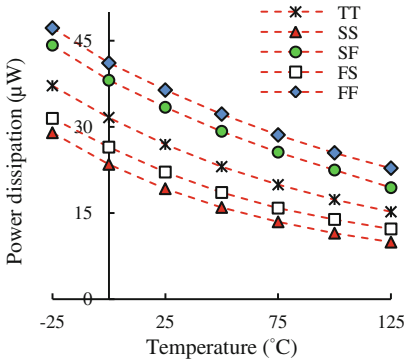


Fig. 5 Variation in power dissipation for different process corners

3.3 Parametric Sensitivity Analysis

In this section, the effect of individual parameter variations is analyzed. Four important parameters are considered viz. threshold voltage (V_{th}), oxide thickness (T_{ox}), effective gate length (L_{eff}) and supply voltage (V_{DD}). Each of the four parameters is varied individually by $\pm 3\sigma$, while all the other parameters are kept constant at their nominal value. The $\pm 3\sigma$ variations incorporate the worst case shift and cover nearly 99.7% variation of the parameter under the Gaussian curve [12].

The effect of variations in V_{th}, T_{ox}, L_{eff} and V_{DD} on CM interconnect system performance is presented in Fig. 6a–d, respectively. The performance metrics are propagation delay and power dissipation. The analyses are performed at 25 °C and the technology nodes are varied from 130 to 32 nm. It is seen from the figure that the impact of variations on propagation delay for 3σ variation in V_{th}, T_{ox}, L_{eff} and V_{DD} are nearly 11.5, 8.1, 7.9 and 6.5%, respectively, for 45 nm technology node. These variations in power dissipation are almost 7.3, 3, 9.9 and 30%, respectively. The analyses suggest that propagation delay is most affected by variation in V_{th} parameter, while fluctuations in V_{DD} affect power dissipation the most. It is also analyzed that as technology is scaled down from 130 to 32 nm, the variation in propagation delay increases by 76% with fluctuations in V_{th}. This increase is nearly 70% for fluctuation in T_{ox} parameter. However, in case of fluctuations in L_{eff}, the variation in propagation delay decreases by 44%. The variation in V_{DD} also shows decrease in propagation delay up to 57%. This suggests that V_{th} and T_{ox} fluctuations affect propagation delay more prominently at smaller technology nodes. Similarly, it is investigated that incase of power dissipation, the impact of variations in L_{eff} and V_{DD} becomes very dominant at lower technology nodes.

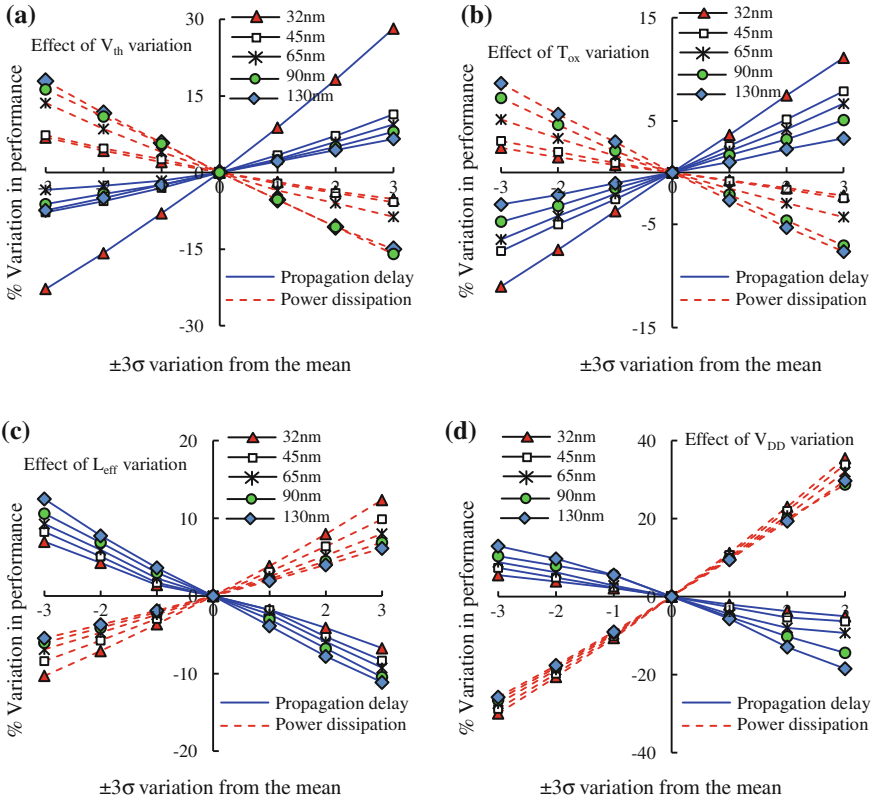


Fig. 6 Parametric sensitivity analysis with variations in **a** threshold voltage (V_{th}), **b** oxide thickness (T_{ox}), **c** effective gate length (L_{eff}) and **d** supply voltage (V_{DD}) in current-mode interconnect system

4 Conclusion

The paper presents the impact of process, voltage and temperature variation effects in current-mode interconnect system. The effect of technology scaling, process corner and parametric sensitivity variations are analyzed. It is investigated that as technology is scaled down, the propagation delay increases while power dissipation decreases in CM interconnect system. It is also observed that process corners severely affect the performance of the system. The SS model results in least power dissipation in the circuit while FF model is good for high speed applications as it offers smallest latency in the circuit. The effects of variations in V_{th}, T_{ox}, L_{eff} and V_{DD} have varying impact on propagation delay and power dissipation in the circuit. It is inferred that fluctuation in V_{th} affects propagation delay the most while V_{DD} fluctuations dominantly controls the power dissipation in the system. The various analyses in the paper reveal the impact of variability in CM interconnect system.

The present research shall be highly helpful in understanding variability effects and consequently manufacturing robust designs for current-mode interconnect system in nanometer regimes.

References

1. Unsal, O.S., Tschanz, J.W., Bowman, K., De, V., Vera, X., Gonzlez, A., Ergin, O.: Impact of parameter variations on circuits and microarchitecture. IEEE Micro **26**(6), 30–39 (2006)
2. Achar, R., Nakhla, M.S.: Simulation of high speed interconnects. Proc. IEEE **89**(5), 693–728 (2001)
3. Agrawal, Y., Chandel, R.: Crosstalk analysis of current-mode signalling-coupled RLC interconnects using FDTD technique. IETE Tech. Rev. **33**(2), 148–159 (2016)
4. Yuan, F.: CMOS current mode circuits for data communication. Springer, New York (2007)
5. Shoaran, M., Tajalli, A., Alioto, M., Schmid, A., Leblebici, Y.: Analysis and characterization of variability in subthreshold source coupled logic circuits. IEEE Trans. Circuits Syst. **62**(2), 458–467 (2015)
6. Predictive Technology Models. Available: http://ptm.asu.edu (2016)
7. Tunna, S., Nigussie, E., Isoaho, J., Tenhunen, H.: Modeling of energy dissipation in RLC current mode signaling. IEEE Trans. Very Large Scale Integr. Syst. **20**(6), 1146–1151 (2011)
8. International Technology Roadmap for Semiconductors. Available: http://public.itrs.net (2013)
9. Tanner EDA tools for SPICE simulation. Available: http://www.tannereda.com (2016)
10. Anis, M., Allam, M., Elmasry, M.: Impact of technology scaling on CMOS logic styles. IEEE Trans. Circuits Syst. **49**(8), 577–588 (2002)
11. Sakurai, T., Newton, A.R.: Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas. IEEE J. Solid-State Circuits **25**, 584–594 (1990)
12. Kang, S.M., Leblebici, Y.: CMOS Digit. Integr. Circuits. TMH, New Delhi (2003)

LMP Difference Approach for Management of Transmission Congestion

Divya Asija, K.M. Soni, S.K. Sinha and Vinod Kumar Yadav

Abstract This paper deals with new methodology for optimal placement of Distributed Generator (DG) to improve congestion in the transmission system. The proposed approach is based on LMP and LMP difference method to formulate priority list of buses. Based on priority list congested zones are formed and Distributed Generators are placed at potential location to analyze the status of the system. Loading condition is also studied. In this work, the simulation studies on IEEE 14 bus system is found to be competent to find the best location of DG for management of transmission system congestion.

Keywords Distributed generator · Locational marginal price · Congestion Social welfare · Weighting factors

1 Introduction

In this new era, power system has been restructured from vertically integrated system to unbundled electric system. Restructuring brings the several changes by introducing electricity as commodity and deregulated power supply. Competitive market has participation from several buyers for low cost generators thereby creating intensified congestion in the linked corridors. Congestion in the system results in unrestricted loss of load which has to be avoided for reliability and security.

D. Asija (✉) · K.M. Soni · S.K. Sinha
Amity University, Noida, Uttar Pradesh, India
e-mail: divyaasija83@gmail.com

K.M. Soni
e-mail: kmsoni@amity.edu

S.K. Sinha
e-mail: sksinha6@amity.edu

V.K. Yadav
Gautam Buddha University, Greater Noida, Uttar Pradesh, India
e-mail: vinod@gbu.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_54

Congestion management is done to decide the priority based transactions providing acceptable level of reliability and system security. In the current state of deregulated power system reliability and security of the network is of major concern which eventually enforce for the congestion management.

Literature Review

For mitigating congestion, Independent System Operator (ISO) mainly focuses on two major techniques non charge-free technique and charge-free technique [1]. Non charge-free technique involves generation re-dispatch and load curtailment. Charge-free technique is under the control of transmission system operator not involving Generation and Distribution Company. It includes network reconfiguration, installation of phase shifter, transformer taps, and utilization of series flexible AC transmission system devices. The above mentioned congestion management techniques exploit diverse techniques such as generation rescheduling [2], line flow sensitivity [3], voltage stability [4], installation of facts devices [5–7], network reconfiguration [8], relative electrical distance [9], expert system approach [7, 8, 10, 11], usage of Sen Transformer [12], zones and clustering [15, 16], power loss improvement [12, 13] and location of dispersed generator [10, 13, 14, 15].

In the proposed system the DGs have been used at the load side. DGs are small scale generators installed at consumer end for incrementing power system generating capacity. DG is considered as a good alternative for improving congestion in view of the fact that it itself acts as negative load thus reducing the higher payoff due to excess load [8]. Congestion cost diminishes with the installation of DG as it limits the expansion of transmission and high consumer demand by providing highly secure and reliable electricity. DGs supply the local load and remove the congestion from the transmission corridors thereby lowering the location marginal price (LMP) and nodal congestion price (NCP) for optimal power flow. The location of DG should be done with due consideration to provide maximum benefit. Improper placement may sometimes result in jeopardizing the system reliability and efficiency by augmenting the network congestion.

This paper is planned in the following manner: Sect. 2 presents the formulation of problem for congestion management. Section 3 deals with LMP and LMP difference method. Section 4 presents the simulation studies and result. Section 5 explains the conclusion related with the proposed system.

2 Problem Formulation

In these section nodal prices of electricity has been evaluated by optimal power flow (OPF) formulation to evaluate the price energy (NCP or LMP) with the objectives of social welfare maximization and network security. Optimal power flow (OPF) algorithm uses interior point nonlinear method to simultaneously optimize the multiple objectives. Social welfare is basically the benefit to the

negotiator and it is the difference of total cost incurred by the consumer minus the total cost of supplier. The inputs to the OPF routine are generation and demand offers. At the base level OPF routine evaluates the generation dispatch, load demand, and nodal prices. The placement of DG is optimal when it meets the load demand at a lesser price by redistributing the power flow over the transmission lines. DG owner will place the DG in the network to achieve maximum revenue. Maximum revenue is generated when the location of DG is optimum to have lower LMP and NCP. DG is situated at a place to conciliate both objectives having different weightage level.

The main contribution of this paper is removal of congestion from the transmission network with the enhancement of social benefit factor and security of the system. LMP difference method is used to find the priority ranking based congestion zones. The DG will be placed at higher priority location in the transmission network which meets the load demand at lesser price thereby reducing the congestion in the network.

2.1 Optimal Power Flow Formulation

The objective function without DG comprises of quadratic profit curve submitted by consumer or distributed company, DISCO minus the quadratic offer curve of the supplier or generation company, GENCO. The ultimate goal is to minimize the function F having weighting factors as wt_1 for social welfare and wt_2 for network security.

$$\text{Min.}F = -wt_1\left[\sum_{i=1}^{n}\left(C_{\text{d}i}P_{\text{d}i} - C_{\text{s}i}P_{\text{s}i}\right)\right] - wt_2\lambda_{\text{c}} \tag{1}$$

(Objective function without the installation of DG)

$$\left.\begin{aligned} &0 < wt_1 < 1, \\ &0 < wt_2 < 1 \\ &wt_1 = 1 - wt_2 \end{aligned}\right\} \tag{2}$$

(wt_1 is weight factor for social welfare and wt_2 is for network security)

$$C_{\text{d}i}P_{\text{d}i} = x_{\text{d}i} + y_{\text{d}i}P_{\text{d}i} - z_{\text{d}i}\left(P_{\text{d}i}^2\right) \tag{3}$$

(Consumer benefit function)

$$C_{\text{s}i}P_{\text{s}i} = x_{\text{s}i} + y_{\text{s}i}P_{\text{s}i} + z_{\text{s}i}\left(P_{si}^2\right) \tag{4}$$

(Supplier offer function)

$$\text{s.t.} \quad f(P_S, P_D, Q_G, \theta, V) = 0 \tag{5}$$

(Power flow equation)

$$f(P_s, P_d, Q_{gc}, \theta_c, V_c, \lambda_c) = 0 \tag{6}$$

(Power flow equation for max. load)

$$\lambda_{cmin} \leq \lambda_c \leq \lambda_{cmax} \tag{7}$$

(Loading Range)

$$0 \leq P_S \leq P_{Smax} \tag{8}$$

(Generator supply bid)

$$0 \leq P_D \leq P_{Dmax} \tag{9}$$

(Consumer demand bid)

$$\left.\begin{aligned} I_{ab}(\theta, V) &\leq I_{abmax} \\ I_{ba}(\theta, V) &\leq I_{bamax} \\ I_{ab}(\theta_c, V_c) &\leq I_{abmax} \\ I_{ba}(\theta_c, V_c) &\leq I_{bamax} \end{aligned}\right\} \tag{10}$$

(Thermal limits)

$$\left.\begin{aligned} Q_{g\,min} \leq Q_g &\leq Q_{g\,max} \\ Q_{g\,min} \leq Q_{gc} &\leq Q_{g\,max} \end{aligned}\right\} \tag{11}$$

(Generator Q limits)

$$\left.\begin{aligned} V_{lower} \leq V &\leq V_{higher} \\ V_{lower} \leq V_c &\leq V_{higher} \end{aligned}\right\} \tag{12}$$

(Voltage security limits)
The objective function with inclusion of DG is as follows:

$$\text{Min.}F = -wt_1 \left[\sum_{i=1}^{n} \left(C_{di} P_{di} - C_{si} P_{si} - C_{dg_i} P_{dg_i} \right) \right] - wt_2 \lambda_c \tag{13}$$

DG offer function is represented as

$$C_{\mathrm{dg}_i} P_{\mathrm{dg}_i} = x_{\mathrm{dg}_i} + y_{\mathrm{dg}_i} P_{\mathrm{dg}_i} + z_{\mathrm{dg}_i} \left(P_{\mathrm{dg}_i}^2 \right) \tag{14}$$

where

C_{s} is the supply cost (\$/MWh)
C_{d} is the demand cost (\$/MWh) minimum
$C_{\mathrm{dg}i}$ is the supply cost of distributed generator (\$/MWh)
$P_{\mathrm{s}i}$ is the generated output power of unit i (MW)
$P_{\mathrm{d}i}$ is the power demand by consumer of unit i (MW)
$P_{\mathrm{dg}i}$ is the generated output power form distributed generator for unit i (MW)
Q_{g} is the reactive power output of unit i (MVar)
λ_{c} is the critical loading parameter
I is the total generating units
J is the total consumer units
N is the total transmission lines
μ_i is 1 for online unit i

In the above problem formulation, the congestion management problem has been resolved by installation of DG at optimum location thereby maximizing objectives of social welfare and network security.

3 LMP Difference Method

3.1 Locational Marginal Price

Location Marginal Price imitates the true marginal cost of production taking into account all operational and physical constraints of the system. It is calculated as the cost of allocating the subsequent increment of load at every location. Under normal operating conditions the value of LMP is same at all locations but when congestion occurs in the transmission network it differs. In a bilateral market, higher LMP gives the indication that demand is higher than the generation at that node. Injection of active power at the node having higher LMP will further accomplish the objective of social welfare maximization. DG is the source of active power and best suited to improve the system performance.

3.2 LMP Difference

LMP difference method finds the difference of LMPs of two nodes where transmission line is connected. The value of LMP difference is highest in case of congested line as

compared to other lines. Therefore it directly indicates the prioritized location for placement of DG. LMP difference method is more reliable as compared to highest LMP method which sometimes leads to further increment in congestion.

LMP difference equation:

$$\Delta \mathrm{LMP}_{x \to y} = \mathrm{LMP}_x - \mathrm{LMP}_y; \quad x \text{ and } y = 1, 2 \ldots N \tag{15}$$

where $\Delta \mathrm{LMP}_{x \to y}$ is the LMPs difference of transmission line from bus x to bus y and N is the total number of buses. Equation (15) will deliver the optimum location for placement of DG. The placement of DG at optimum location would improve the LMP difference.

4 Simulation and Results

System performance is analyzed and discussed after DG installation for two distinct objectives of social welfare and network security maximization with different weighting factors. The proposed design is tested on IEEE 14 bus system. It is modified by installation of DG at the high priority location. In the proposed modified IEEE 14 bus system the DG is located at bus 14 with higher LMP method (Fig. 1).

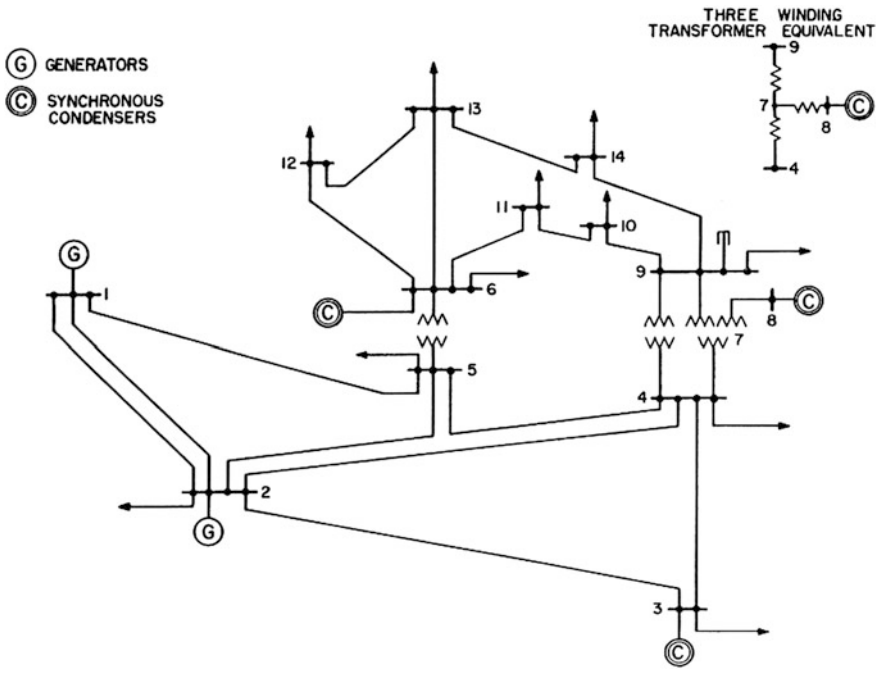


Fig. 1 Single line diagram of IEEE 14 bus system

Supplier and consumer bids data entered into the system to find the optimum power flow as shown by Table 1.

Table 1 shows the cost parameters having quadratic coefficients for the conventional generator connected in the base system and the distributed generator whose incremental cost is comparable to conventional generator in the modified system. In the modified system distributed generator will supply only the real power.

In order to have optimal placement of DG, the congestion management problem is first considered for IEEE 14 bus standard system using optimal power flow which comprises of both genco and disco functions. Results obtained are shown in Fig. 2. It is clear from the figure that bus no. 14 is having the highest NCP of 0.9631512 $/MWh and LMP of 8.8082221 $/MWh. contrary to load which is highest at node 3 having 0.9420 p.u. load. Therefore congestion is not load dependent it is directly related to the transmission capacity of the line. Consequently, bus no. 14 is considered as the desired location for placement of DG as per highest LMP. DG placement will further mitigate congestion from the transmission line.

Table 1 Cost parameters of conventional and distributed generators

Generator type	Bus number	x ($/h)	y ($/MWh)	z ($/MW^{2}h)
Conventional	1	0	20	0.0430293
Conventional	2	0	20	0.25
Conventional	3	0	40	0.01
Conventional	6	0	40	0.01
Conventional	8	0	40	0.01
Distributed	14	0	20	0.25

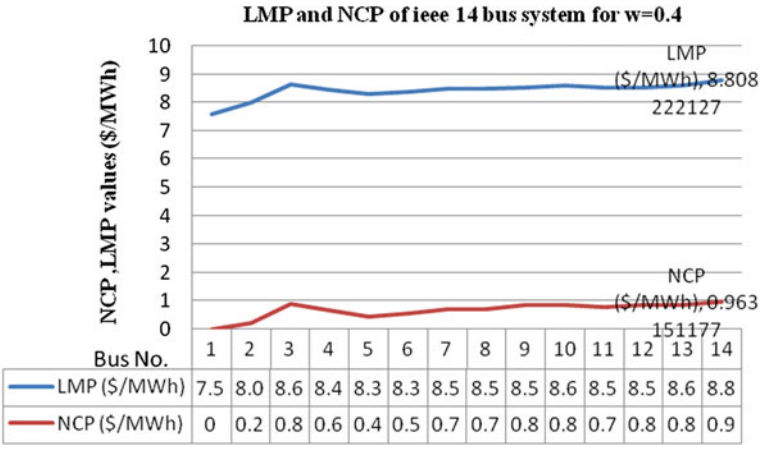


Fig. 2 LMP and NCP for IEEE 14 bus standard system

Table 2 Priority ranking for DG placement

Priority ranking	Transmission line No.	Transmission line from *x* to *y* bus	LMP difference
1	6	3 to 4	0.18
2	7	4 to 5	0.15
3	15	10 to 11	0.07
4	14	7 to 8	−8.52E−12
5	16	7 to 9	−0.0321

Table 3 Loading condition after DG placement

Maximum loading condition at optimum DG locations			
DG at bus no. 14 with LMP method		DG at bus no. 4 with LMP difference method	
Lambda (p.u.)	0.18732	Lambda (p.u.)	0.23643
Max. loading condition (MW)	307.9734	Max. loading condition (MW)	422.5383
Min. loading condition (MW)	48.588	Min. loading condition (MW)	80.7987

Table 2 shows the priority ranking for DG placement based on highest LMP difference technique. The transmission line having higher LMP difference has been placed on top. Table shows that line no. 6 is having highest LMP difference which is connected between bus 3 and 4. Since bus 3 is the generator bus, it is not considered as potential location for placement of DG. At generator bus the load demand should be greater then only it can be considered as one of the optimal location for placement of DG otherwise next sub-optimal location is considered. Bus 4 is considered as next possible location for placement of DG to relieve congestion. Bus 14 has been considered as optimal location for DG placement as per highest LMP method but it has got very less LMP difference as per Table 2.

Table 3 shows the effect of placement of DG in accordance with the two techniques of LMP and LMP difference on the loading condition of the system. The loading factor lambda increased from 0.18732 to 0.23463 p.u. resulting in increment of maximum loading condition by 114.5649 MW. Thus LMP difference technique gives better optimum location.

5 Conclusion

Results obtained from LMP and LMP difference techniques with different weighting factors are exploited to find the candidate node for installation of DG at most favorable location. DG having incremental cost equivalent to conventional

generator cost is installed. Comparative analysis after DG placement in accordance with LMP and LMP difference techniques shows that loading factor has been increased when DG is placed at bus 4. Therefore it is concluded that LMP difference technique is best suited to find the optimum location of DG for congestion management and higher system efficiency.

References

1. Pillay, A., Karthikeyan, S.P., Kothari, D.P..: Congestion management in power systems—a review. Int. J. Electr. Power Energy Syst. **70**, 83–90 (2015)
2. Dutta, S., Singh, S.P.: Optimal rescheduling of generators for congestion management based on particle swarm optimization. IEEE Trans. Power Syst. **23**(4), 1560–1569 (2008)
3. Jibiki, T., Sakakibara, E., Iwamoto, S.: Line flow sensitivities of line reactances for congestion management. IEEE Power Eng. Soc. Gen. Meet. **1**, 1–6 (2007)
4. Conejo, A.J., Milano, F., García-Bertrand, R.: Congestion management ensuring voltage stability. IEEE Trans. Power Syst. **21**(1), 357–364 (2006)
5. Saravanan, M., Slochanal, S.M.R., Venkatesh, P., Abraham, J.P.S.: Application of particle swarm optimization technique for optimal location of FACTS devices considering cost of installation and system loadability. Electr. Power Syst. Res. **77**(3–4), 276–283 (2007)
6. Acharya, N., Mithulananthan, N.: Locating series FACTS devices for congestion management in deregulated electricity markets. Electr. Power Syst. Res. **77**(3–4), 352–360 (2007)
7. Bhattacharyya, B., Gupta, V.K.: Fuzzy based evolutionary algorithm for reactive power optimization with FACTS devices. Int. J. Electr. Power Energy Syst. **61**, 39–47 (2014)
8. Granelli, G., Montagna, M., Zanellini, F., Bresesti, P., Vailati, R., Innorta, M.: Optimal network reconfiguration for congestion management by deterministic and genetic algorithms. Electr. Power Syst. Res. **76**(6–7), 549–556 (2006)
9. Yesuratnam, G., Thukaram, D.: Congestion management in open access based on relative electrical distances using voltage stability criteria. Electr. Power Syst. Res. **77**(12), 1608–1618 (2007)
10. Mithulananthan, N., Oo, T., Van Phu, L.: Distributed generator placement in power distribution system using genetic algorithm to reduce losses. Thammasat Int. J. Sci. Technol. **9**(3), 55–62 (2004)
11. Muneender, E., Vinod Kumar, D.M.: Optimal real and reactive power dispatch for zonal congestion management problem for multi congestion case using adaptive fuzzy PSO. In: IEEE Region 10 Annual International Conference, Proceedings/TENCON (2009)
12. Sen, K.K., Sen, M.L.: Comparison of the 'Sen' transformer with the unified power flow controller. IEEE Trans. Power Delivery. **18**(4), 1523–1533 (2013)
13. Dulau, L.I., Abrudean, M., Bica, D.: Optimal location of a distributed generator for power losses improvement. Procedia Technol. **22**, 734–739 (2016)
14. Gautam, D., Nadarajah, M.: Influence of distributed generation on congestion and LMP in competitive electricity market. World Acad. Sci. Eng. Technol. **39**(3), 822–829 (2009)
15. Sultana, S., Roy, P.K.: Krill herd algorithm for optimal location of distributed generator in radial distribution system. Appl. Soft Comput. J. **40**, 391–404 (2016)
16. Daganzo, C.F., Lehe, L.J.: Distance-dependent congestion pricing for downtown zones. Transport. Res. Part B: Met. **75**, 89–99 (2015)

Optimal Allocation of DG in the Radial Distribution Network Using Bat Optimization Algorithm

T. Yuvaraj, K.R. Devabalaji and K. Ravi

Abstract In the present era, the optimal allocation of Distributed Generation (DG) at the distribution end is becoming significant due to environmental and economic issues, to deduce the power loss and also to improve the voltages between the buses. In this paper authors focused to address the optimal sitting and sizing of DGs in the distribution networks by using nature inspired Bat Algorithm (BA). In addition in this study, two different kinds of DGs have been considered. The main aim of the present work is to reduce the network real power losses. The location and sizing of different types of DGs can be determined by implementing BA. Further, to verify the effectiveness of the proposed method, IEEE 33-bus RDS is chosen. The obtained results of the proposed method is compared with other optimization based techniques. The simulation results specify that allocation of DGs in the RDS can significantly decrease the network power losses.

Keywords Distributed generation (DG) · Bat algorithm (BA)
Radial distribution network (RDS)

1 Introduction

Distribution networks have the highest rate of power loss in power system which has been approximated in the studies about 13% [1, 2]. Hence many efforts have been taken to decrease the power loss in the RDS. The optimal placement of DG has valid effect on decreasing network losses and improving the voltages between the each bus in the distribution networks. The term "Distributed" or "Dispersed"

T. Yuvaraj (✉) · K.R. Devabalaji · K. Ravi
School of Electrical Engineering, VIT University, Vellore, India
e-mail: yuvaraj4252@gmail.com

K.R. Devabalaji
e-mail: eeedevabalaji@gmail.com

K. Ravi
e-mail: k.ravi@vit.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_55

Generation (DG) is used to define as small level power generation that is directly linked to the electric distribution systems.

Distributed Generation consists of synchronous and induction generators, fuel cells, solar photovoltaic installations, combustion and reciprocating engines, micro turbines, wind turbines and other small power generation sources. There are several reasons for a consumer to place a DG in the distribution system. The power supply to the consumers is generated by DG for peak saving or emergency generation or standby purpose. The installation cost of DGs are usually less in compare with construction of new power plants and distribution and transmission lines. The installation of DG exhibits numerous advantages over conventional generations such as power quality, high reliable energy related solutions, economic and environmental friendly [3, 4].

The problem of optimal allocation of DGs in the RDS is become a big challenging task for power system engineers. Till now the numbers of research works have been carried out for optimum allocation of DG in RDS using various optimization algorithms. Bee Colony Algorithm [5], PSO and Monte Carlo simulation [6], GA [7], Honey Bee Mating Optimization Algorithm [8], Quasi-oppositional teaching learning based optimization [9], Backtracking search optimization algorithm [10] have been considered for DG allocation in RDS with different objective function.

In this paper an efficient methodology proposed by considering drawbacks exists in the other optimization techniques to determine the optimal allocation for DG in the RDS for reduction of power loss and bus voltage profile enhancement. Recently developed bio-inspired Bat Algorithm is used to identify the candidate DG location and amount of kW/kVAr injection in the RDS. In the proposed method different types of DG models are considered and analyzed for reduction of power loss and enhancement of bus voltage profile.

2 Power Flow Analysis

Radial distribution networks have high resistance to reactance (R/X) ratio. Therefore traditional load flow studies such as Newton Raphson, fast decoupled and Gauss-Seidal load flow solution methods are not appropriate for finding the voltages between the buses and line flows in the RDS.

The Distribution power flow solution is one of the most efficient methods for load flow analysis of RDS [11]. The main feature of this power flow study is that there is no difficulty of convergence in the solution of radial distribution networks with high ratio of resistance to reactance. The Model radial distribution system is depicted in Fig. 1.

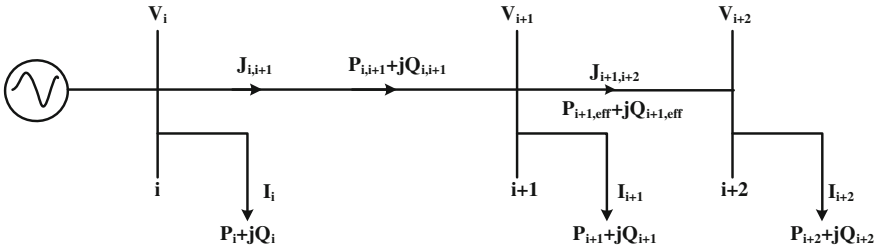


Fig. 1 Model radial distribution system

The equivalent current injection at bus i can be calculate using Eq. (1).

$$I_i = \left(\frac{P_i + jQ_i}{V_i}\right)^* \tag{1}$$

where the P_i and Q_i are represented the loads of the active and reactive powers at bus i, respectively.

From Fig. 1, the branch current $J_{i,i+1}$ between the buses i and $i + 1$ can be computed by using KCL, which is given by

$$J_{i,i+1} = I_{i+1} + I_{i+2} \tag{2}$$

By using the Bus Injected to BIBC, the above equation is derived in matrix format

$$[J] = [\text{BIBC}][I] \tag{3}$$

where BIBC is Branch Current matrix. From Fig. 1, the bus $i + 1$ voltage can be calculated by using Kirchhoff's voltage law, which can be expressed as

$$V_{i+1} = V_i - J_{i,i+1}(R_{i,i+1} + jX_{i,i+1}) \tag{4}$$

where $X_{i,i+1}$ and $R_{i,i+1}$ are the Reactance and Resistance of the line segment between buses i and $i + 1$, respectively. The computation of the real $\left(P_{\text{Loss}(i,i+1)}\right)$ and reactive power loss in the line segment between buses i and $i + 1$ are listed as follows:

$$P_{L(i,i+1)} = \left(\frac{P_{i,i+1}^2 + Q_{i,i+1}^2}{\left|V_{i,i+1}\right|^2}\right) * R_{i,i+1} \tag{5}$$

By considering the all line losses in each bus, we can calculate the total active power losses P_{TL}.

$$P_{\mathrm{TL}} = \sum_{t=1}^{nb} P_{L(i,i+1)} \tag{6}$$

2.1 Objective of the Problem

The objective of the present work is adapted to reduce the total active power loss of the RDS. The objective function can be formulated as

$$\text{Minimize } (F) = \text{Min } (P_{\mathrm{TL}}) \tag{7}$$

3 Bat Algorithm

Nowadays, nature inspired algorithms play a major role in distribution system optimization. Xin-Sha Yang developed a nature inspired algorithm known as bat algorithm in the year of 2010 [12, 13]. Echolocation behavior is the main tool of bat algorithm. Bats are alluring animals, these are only the mammals having wings and innovative echolocation ability to find their prey. Generally it radiates a sound signal named echolocation to sense the objects nearby them and identify their technique even in the night times.

Based on the BA idealization rules, the step by step execution of BA for the proposed DG allocation work is described in the following steps.

Step 1: First, initialize the system bus and load data.
Step 2: Find out the uncompensated system losses, and voltage between the buses with help of distribution load flow.
Step 3: The different types of DG placement can be done by using bat algorithm.
Step 4: Set the minimum and maximum bounds for the constraints, bat algorithm control parameters (pulse frequency, pulse rates and loudness) and maximum no of iteration.
Step 5: Randomly produce the first bat population in the possible area. Each bat indicates an encouraging optimal size for DG in the RDS.
Step 6: Calculate the fitness (objective) function. In this step, the predictable value of the power losses and the voltage values can be determined by using Direct Load Flow method for each solution or bat.
Step 7: Pick the finest bat in the population (minimum objective function value).
Step 8: Update the bat population.
Step 9: Run the power flow again and note down the power losses and voltages for updated population.

Step 10: Verify the termination criterion. Terminate the algorithm, if the objective function reaches to minimum value otherwise go to step number 5.
Step 11: Display the optimal solutions.

To achieve the objective the above steps have been followed to entire optimization process.

4 Results and Discussion for IEEE 33-Bus

To verify the effectiveness of the proposed method, the implementation steps of proposed algorithm and other optimization algorithms have been coded using MTALAB, by considering various test conditions. To verify this; a standard IEEE 33-bus test system is considered and two types of DG models (Type-I and Type-II) also taken into consideration. The base case power losses and voltage between each bus is obtained by using direct distribution load flow method.

4.1 IEEE 33-Bus System

Here in this case, active and reactive loads of medium scale 33-bus system is given as 3.72 MW and 2.3 MVAr respectively. The bus and line data have been obtained from [14]. The uncompensated system active power loss and minimum voltage are 210.98 kW and 0.9037 respectively. In the present work; Type I and II DGs have been taken for the consideration. The 33-bus system schematic diagram is depicted in Fig. 2.

In this test system, three DGs (Type-I or Type-II) are optimally located in 13th, 24th and 30th buses. The optimum allocation of the different kinds of DGs are obtained by using bat optimization algorithm. The simulation results obtained by implementing this method are given in Table 1, that depicts the candidate locations, sizes of the DGs, real power loss, minimum voltage between the buses and minimum VSI values. Voltage profile of comparison of 33-bus network is shown in Fig. 3. From Table 1 and Fig. 3, it can be noted that Type-II DG placement is more beneficial as the power loss decrease and bus voltage profile enhancement than the

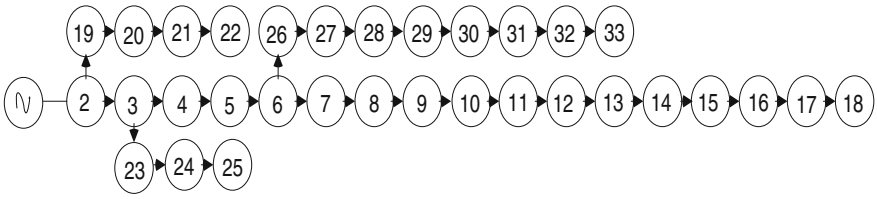


Fig. 2 Schematic diagram of IEEE 33-bus system

Table 1 Comparison and performance of 33-bus test system

DG type	Method	DG location and size (kW)	Power factor	P_{Loss} (kW)	% Reduction in P_{Loss}	V_{min} (p.u)
Type-I DG	Base case	–	–	210.98	–	0.9037
	BSA [10]	632(12) 487(28) 550(31)	Unity	89.05	57.8	–
	QOTLBO [9]	880.8(12) 1059.2(24) 1071.4(29)	Unity	74.1	64.9	–
	Proposed method	720(13) 1020(24) 980(30)	Unity	73.4	65.2	0.9628
Type-II DG	BSA [10]	632(12) 487(28) 550(31)	0.86 0.71 0.70	29.65	85.97	–
	Proposed method	720(13) 1020(24) 980(30)	0.896 0.897 0.720	12.35	94.15	0.9879

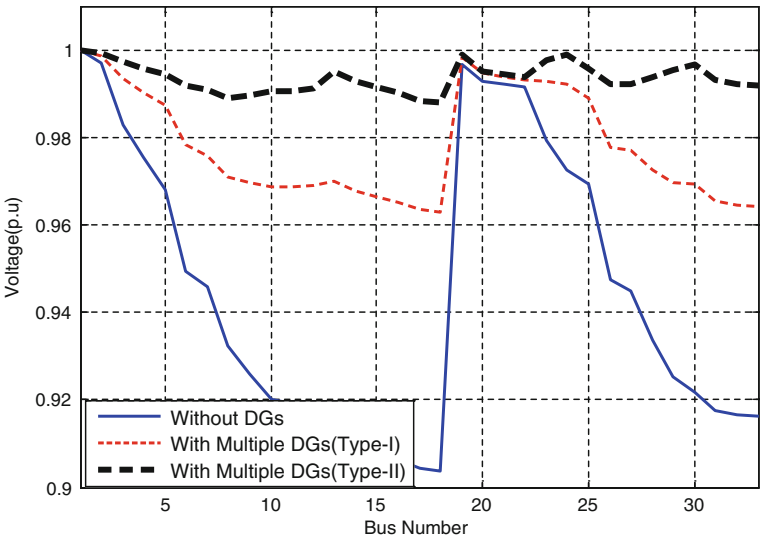


Fig. 3 Comparison of voltage profile for 33-bus network

Type-I DG placement. To validate the effectiveness of the present optimization approach, it is compared with the other algorithms such as BSA [10], and QOTLBO [9]. The obtained simulation values are presented in Table 1. From the examining the Table 1 clearly, it can be confirm that, the proposed method gives better results in terms of power loss reduction and bus voltage improvement.

5 Conclusion

From the literature and work carried out it is understood that optimal allocation of DGs is one of the major issues in the RDS. It is important to place the DGs at candidate locations with optimal kW and kVAr to ensure the maximum benefits of the system. Different types of DG candidate placements and sizing is determined by implementing BA to achieve the objective function in the RDS. The benchmark 33-bus test system has been considered for analysis in the present work. The results presented in result section shows the effectiveness of the present work in finding best locations. Further, the BA can be recommended as a talented nature inspired algorithm to resolve difficult problems in the engineering fields for the upcoming researchers.

References

1. EI-Fergany, A.A.: Optimal capacitor allocations using evolutionary algorithms. IET Gener. Transm. Distrib. 593–601 (2013)
2. Yuvaraj, T., Ravi, K., Devabalaji, K.R.: Optimal allocation of DG and DSTATCOM in radial distribution system using cuckoo search optimization algorithm. Modelling and Simulation in Engineering (2017). Article in Press. doi:10.1155/2017/2857926
3. Willis, H.L., Scott, W.G.: Distributed Power Generation: Planning and Evaluation. Marcel Dekker, New York (2000)
4. Ackerman, T., Anderson, G., Soder, L.: Distributed generation: a definition. Electr. Power Syst. Res. **57**, 195–204 (2001)
5. Abu-mouti, F.S., EI-Hawary, M.E.: Optimal distributed generated generation allocation. IEEE Transpower Deliv. **26**, 2090–2101 (2011)
6. Abdi, S., Afshar, K.: Application of IPSO-monte carlo for optimal distributed generation allocation and size. Int. J. Elect. Power Energy Syst. **44**(1), 786–797 (2013)
7. Mardaneh, M., Gharehpetian, G.B.: Siting and sizing of DG units using GA and OPF based technique. In: Proceedings of IEEE Region 10 TENCON Conference, vol. 3. pp. 331–334 (2004)
8. Niknam, T.: A new HBMO algorithm for multi objective daily volt/var control in distribution system considering Distributed Generators. Appl. Energy, 778–788 (2010)
9. Sultana, S., Roy, P.K.: Multi-objective quasi oppositional teaching learning based optimization for optimal location of distributed generator in radial distribution. Int. J. Elect. Power Energy Syst. **63**, 534–545 (2014)
10. El-Fergany, A.: Optimal allocation of multi-type distributed generators using backtracking search optimization algorithm. Int. J. Elect. Power Energy Syst. **64**, 1197–1205 (2015)
11. Teng, J.H.: A direct approach for distribution system load flow solutions. IEEE Trans. Power Deliv. **18**(3), 882–887 (2003)
12. Yang, X.S.: A new meta heuristic bat-Inspired algorithm. In: Gonzalez, J.R., et al. (eds.) Nature Inspired Cooperative Strategies for Optimization (NISCO 2010). Studies in Computational Intelligence, pp. 65–74. Springer, Berlin (2010)
13. Yuvaraj, T., Ravi, K., Devabalaji, K.R.: DSTATCOM allocation in distribution networks considering load variations using bat algorithm. Ain Shams Eng. J. (2015). Article in Press. doi:10.1016/j.asej.2015.08.006
14. Sahoo, N.C., Prasad, K.: A fuzzy genetic approach for network reconfiguration to enhance voltage stability in radial distribution systems. Energy Convers. Manag. **47**, 3288–3306 (2006)

Smart Controlling of Appliances in Power-Line Communication Using LabVIEW

Deepthi P. Kulkarni, H.B. Bhuvaneswari and B. Kalyan Ram

Abstract Power-line communication is an efficient energy-controlled networking technology, which is used in Smart Grid, Smart Cities, Smart Buildings and smart home applications. This technology is very efficient, low cost, requires no rewiring, making the installation system very simple in any smart home applications. More energy management technologies are in progress in various countries due to demand in increased power consumption with limited natural resources. Automating equipment will lead to efficient energy management with huge saving on the monthly electricity tariff. One of the drawbacks of the existing PLC systems in a very challenging communication environment is the use of high-frequency carrier wave which tends to cause noise and interference in the power line and thus needs improvement. This paper presents a new, simple, cost-effective approach which eliminates use of high-frequency carrier wave to reduce the wastage of power in the domestic energy consumption. Here, automation of two loads for lighting application using LabVIEW by sending the data bits using NI myDAQ controller is demonstrated. The system developed uses firing angle controller to trigger the TRIAC at different firing angles to automate the two loads.

Keywords Automation · NI myDAQ · op-amp · Power-line communication LabVIEW

D.P. Kulkarni
Jain University, Kanakapura, India
e-mail: deepthipk91@gmail.com

H.B. Bhuvaneswari (✉)
ACS College of Engineering, Bengaluru, India
e-mail: hbbhuvana@gmail.com

B. Kalyan Ram
BITS, Pilani, Goa, India
e-mail: kalyanb.ram@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_56

1 Introduction

Optimized energy management to use less power and save money is the main requirement to meet the current energy crisis [1]. Making low-carbon economy and achieving sustainable development by promoting renewable energy sources, which has become the consensus of international community [2]. Thus, many laws have been introduced recently with respect to energy crisis and environmental awareness due to increased power consumption and exhausted natural resources [3].

Automation plays a key role in saving energy consumed by the household in peak hours by enabling people to turn off appliances at will, remotely. Home automation systems increase the level of comfort, emotion, security and energy management in our home as we can control the devices through mobile phones, touch pads, PCs and/or handheld remotes by eliminating manual switches. This will reduce the human error of leaving the appliances ON even when not in use. Smart Home uses ICT to connect and control alliances in all subsystems in a Home Area Network (HAN) to achieve energy management and remote monitoring [4]. Smart controlling of appliances will turn down the appliances automatically when not in use and thus save energy.

Households' account for a great share of overall energy consumption to obtain great energy savings [5]. Power line is one of the most economical communication technology used throughout the world in many home-automated buildings as there are a number of electrical appliances run on electricity.

2 Power-Line Communication (PLC)

PLC supports low speed and high speed transmission by transmitting data, video, and audio information on common power line [6]. Some of the broad range applications of PLC are Internet access, remote metering/engineering, command and control of home devices for Smart Grid/Cities/Buildings [7, 8]. In home-control PLC device, digital signals are used to modulate a carrier wave into the household wiring at the transmitter whereas the same is decoded at the receiver.

PLC is more affordable and portable (plug-n-play type) as it uses the existing electrical wiring for communication and thus reduces rewiring, which leads to less cost also. Energy usage and CO_2 emission can also be reduced using PLC [9].

The applicability of the PLC technology has been widely investigated in recent years using various modulation techniques and power line modems which are used for the data transfer over power line and some constraints like impedance variation, signal loss, noise and attenuation have been discussed [10–13]. Signal repeaters if used can increase the cost and complexity. Thus, these limitations provide a motivation to develop a new system for PLC which may not require a high frequency carrier modulation technique that is proposed in this work.

This paper implements a simple, home energy intelligent system with an effective scheme to reduce the wastage of power for two loads for lighting applications, which can be extended to many more applications/loads. Here, a simple design for PLC is proposed which uses a TRIAC firing angle control method to generate a code and send one bit data at a time over the power line, thus eliminating the use of high-frequency carrier wave. This system is designed using NI myDAQ (acts as a controller) which will encode the data over the power line at transmitting end and then decode it at the receiving end to control two lighting appliances remotely.

3 Hardware and Software Tools

NI myDAQ with software are used as tools. That is NI Multisim is used for simulating electrical circuits and LabVIEW tool is used for graphical programming.

3.1 NI LabView

The steps involved in creating a LabVIEW program are as follows:

(a) Launch a LabVIEW VI.
(b) Creating controls for user in the front panel.
(c) Creating a block diagram using function palette.
(d) Executing the VI.

3.2 NI Multisim

Circuit simulation involves various steps such as

(a) Creating a new file.
(b) Placing the components and wiring them.
(c) Simulating the circuits.

4 System Architecture, Results and Discussion

Proposed Power-line communication system consists of two major parts: (a) Encoding system and (b) Decoding system. Encoding system includes a TRAIC firing angle controller circuit which is used to generate code, to be sent on the

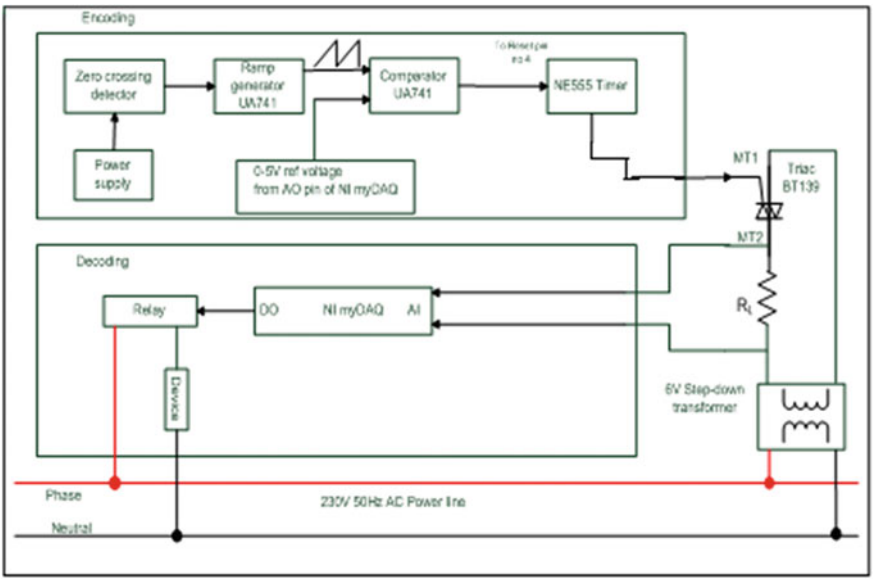


Fig. 1 Block diagram of Power-line communication

power line. Decoding system shall detect the code generated, decodes it and thus, switches the appliances. The block diagram of PLC is as shown as Fig. 1.

4.1 Encoding System

The Encoding system consists of power supply with a zero crossing detector (ZCD), ramp generator, comparator and a timer circuit to trigger the TRIAC. Further the Encoding system defines the duration for which the code is required to be transmitted. The receiving system would respond based on the time synchronized code accordingly.

(a) **Power Supply along with Zero Crossing Detectors (ZCD)**

The power supply unit consists of a step-down transformer which is used to step-down the AC voltage from 230 to 15 V which forms the power supply unit for the ZCD. The ZCD is realized by using two IN4007 diodes and a transistor 2N222 as shown in Fig. 2. Circuits are simulated using NI multisim and simulated output waveforms of rectifier and ZCD are a shown in Figs. 3 and 4 respectively. A full wave rectified output of 15 V amplitude with a pulse output of 5 V amplitude for every 10 ms at 50 Hz frequency has been obtained.

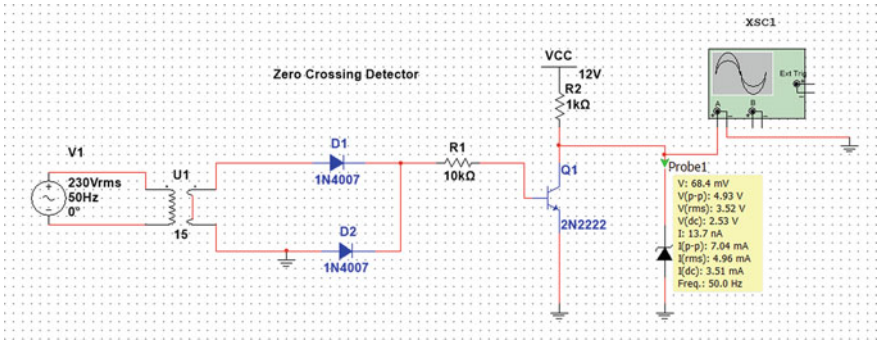


Fig. 2 Simulation circuit of power supply and ZCD

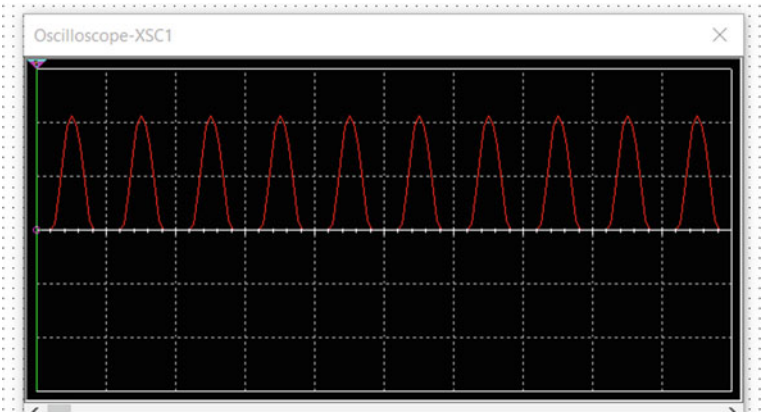


Fig. 3 Full wave rectified output

(b) **Ramp Generator and Comparator**

Ramp generator is realized using operational amplifier (μA741) which is configured as voltage follower. The output of ZCD is connected to a zener diode so that the transistor 2N2222 acts as a constant current source for the amplifier. The output of the transistor is connected to non-inverting terminal of op-amp. A power supply voltage of ±12 V is applied as $+V_{CC}$ and $-V_{EE}$ to the op-amp.

The comparator circuit is realized using op-amp μA741. Figure 5 represents simulation circuit of ramp generator along with comparator. Analog Output pin of NI myDAC provides the reference voltage of (0–5) V DC applied to the non-inverting of op-amp (pin 3 of the IC) is compared with a ramp voltage. Figure 6 shows the ramp waveform of +5 V obtained as the output of ramp generator, which is applied to the inverting terminal of op-amp. Comparator will

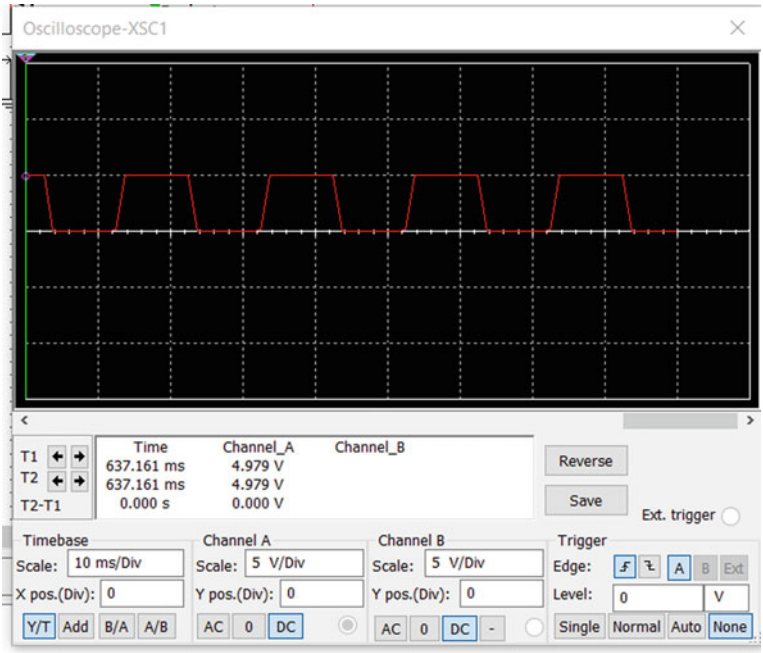


Fig. 4 Zero crossing output

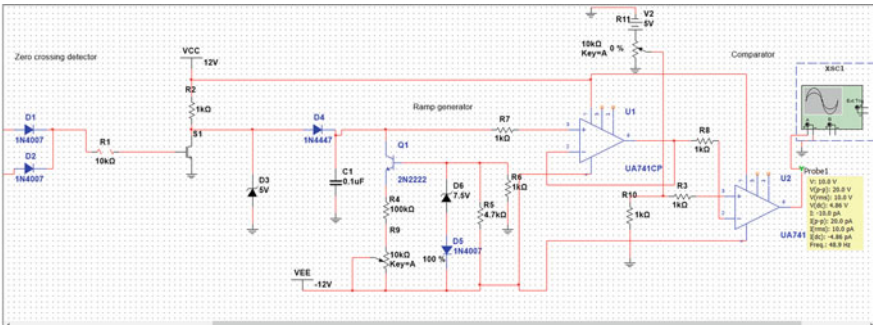


Fig. 5 Simulation circuit with ramp generator and comparator

compare these two signals and provides a pulse output only for that period when the ramp voltage is higher than the set reference voltage as shown in Fig. 7. Comparator provides a 5 V pulse output whose duty cycle can be varied by varying the reference voltage level as shown in Table 1. One such waveform for 90% duty cycle is shown in Fig. 8.

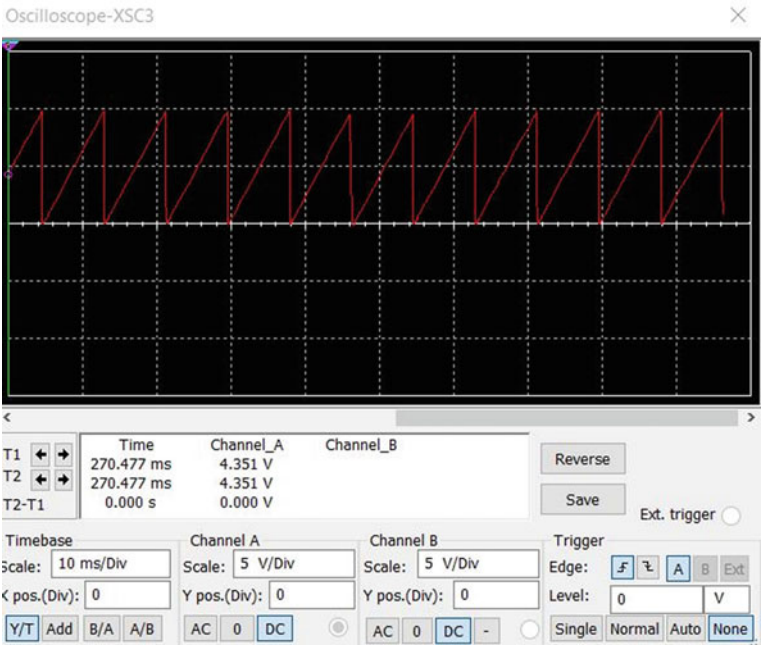


Fig. 6 Simulated output of ramp generator

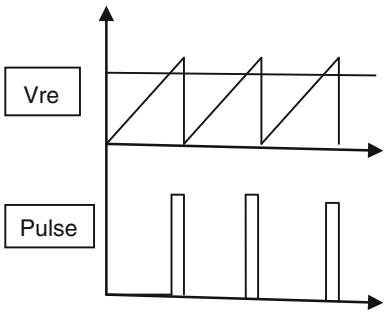


Fig. 7 Expected output of comparator

Table 1 Comparator output

Reference voltage (V)	Duty cycle (%)
0	0
2.5	50
3.5	70
5	100

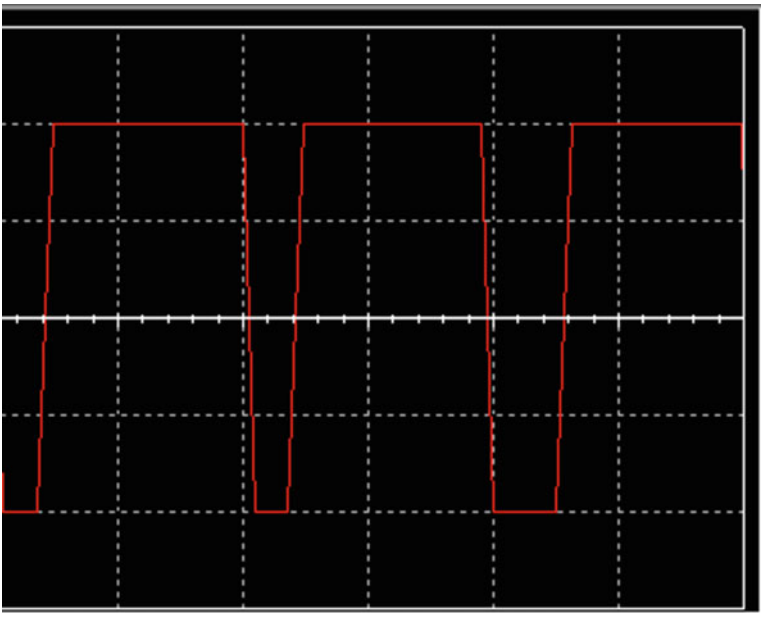


Fig. 8 Comparator output with 90% duty cycle

(c) Final Simulated Circuit of Encoding System

The final block of an encoding system is a NE 555 timer as shown in Fig. 9. Here, the timer works as Pulse width modulator in astable multi-vibrator mode. Here, charging of capacitor takes place through the resistors 'R_1' and 'R_2' where as 'R_2' discharges between 1/3 V_{CC} and 2/3 V_{CC} only. Thus, duty cycle can be varied by adjusting the ratio of these resistors. The output trains of pulses obtained at the

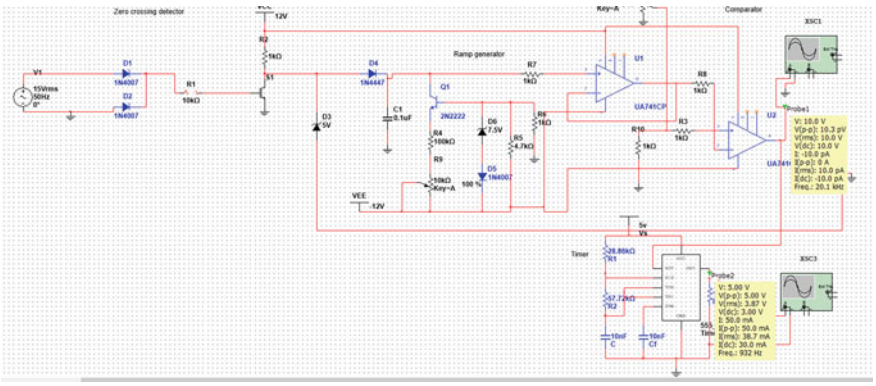


Fig. 9 Simulation circuit with 555 timer

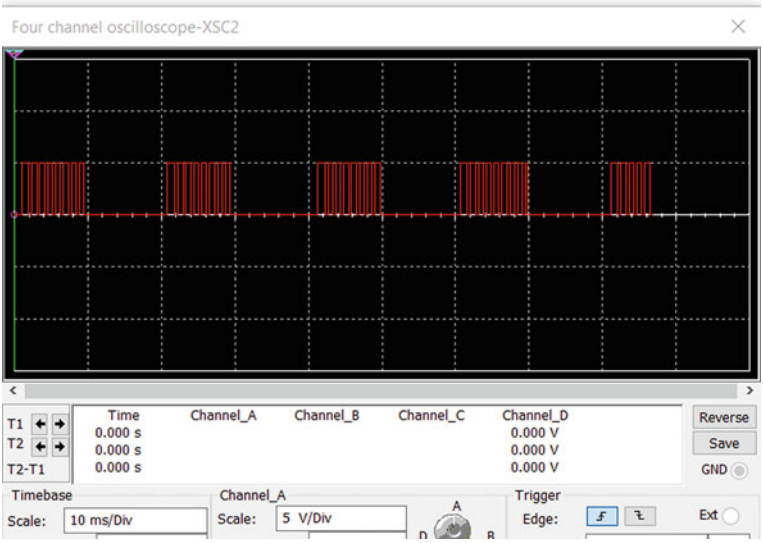


Fig. 10 Simulated PWM output. Waveform of 555 timer

output of timer is as shown in Fig. 10. PWM output with 5 V, 1 kHz has been obtained.

(d) **Hardware Implementation of Encoding System**

The feasibility of the proposed system is verified by implementing the prototype for the encoding part of PLC which is as shown in Fig. 11a. Final output of encoding system was captured using NI myDAQ and LabVIEW which is as shown in Fig. 11b.

Output of the encoding system is used to trigger the TRIAC BT139 (600 V, 14 A) at two different firing angles '$\alpha 1$' and '$\alpha 2$' to turn on the devices between 0°

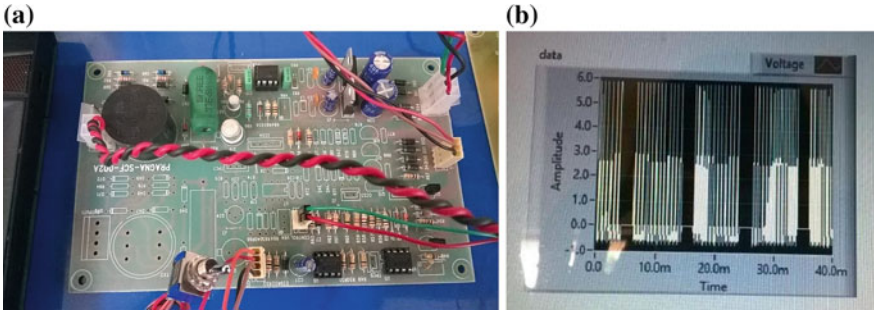


Fig. 11 **a** Printed circuit board of encoding system for TRIAC firing. **b** Final output waveform of encoding system

and 180°. Variation of Duty cycle along with triggering angle is as shown in Table 2. Figure 12 shows the complete hardware set up of TRIAC firing angle controller along with firing angles of TRIAC.

Table 2 Variation of DC voltage, duty cycle and triggering angle 'α'

DC voltage (V)	Duty cycle (%)	Firing angle 'α' (°)
0	0	0
2.5	50	90
3.5	70	126
5	100	180

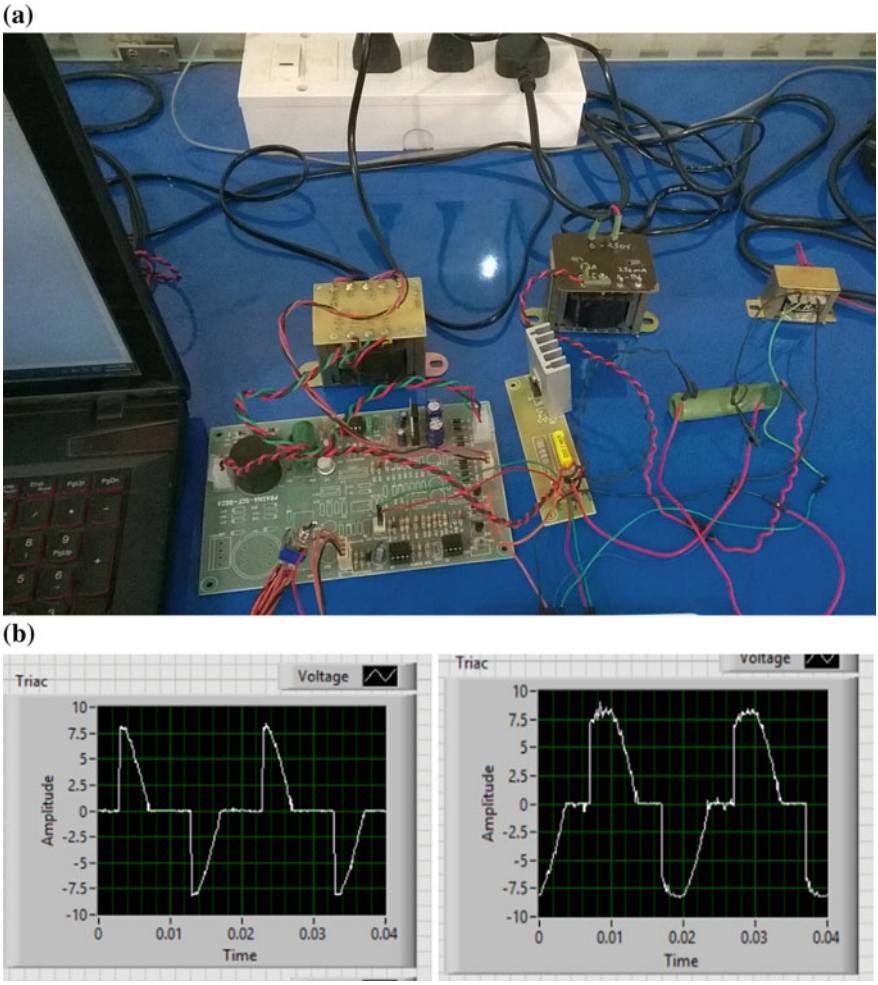


Fig. 12 **a** Hardware set up of TRIAC firing angle controller. **b** TRAIC firing at 90° and 126° respectively

4.2 Decoding System

The voltage variations across the load resistance 'R_L' of TRIAC is fed to the Analog input of the NI myDAQ which detects the code generated. LabVIEW programming tool is used to decode this data. The LabVIEW code processes the data acquired and activated the digital output pin accordingly. A program is written in LabVIEW which will detect the phase angle at which the TRIAC was triggered. The phase angle acts as a command to activate the digital output pin of myDAQ which in turn activates the relay. Thus, each phase angle acts as unique address of the devices to be operated. A step-down transformer is used to reduce the AC voltage from 230 to 8 V to bias the TRIAC.

Phase Detection Using LabVIEW Programming:

NI myDAQ is used to acquire the output waveform of the load resistance connected to the TRIAC. A LabVIEW program is developed to detect the phase/firing angle, which act as a address code to switch the relay, which in turn switch the devices. Figure 13 represents the graphical program developed using LabVIEW for phase detection.

The Algorithm for firing angle detection and decoding is given below.

- Acquire 10 ms segment of the AC sine wave and the voltage waveform of the load resistance connected to the TRIAC using "Split 1D" array block. (NI myDAQ sampling frequency is set to 10 kHz.)
- Both waveforms are made absolute to remove the negative cycle using "Absolute value" block.

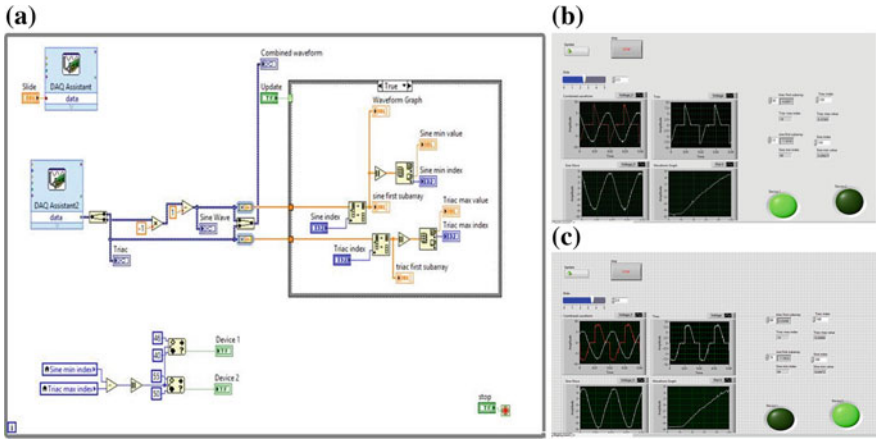


Fig. 13 **a** LabVIEW graphical program for firing angle detection. **b**, **c** Simulated results for device 1 and 2 at 90° and 126° respectively

- The minimum index value of AC sine wave is acquired using "Array max and min" block. (It gives the zero crossing point of the sine wave.)
- The maximum index value of the voltage waveform of load resistance is acquired using "Array Maximum and Minimum values".
- Firing angle of the TRIAC is given by the difference between the maximum and minimum value.

In this project, two devices are selected to demonstrate the switching. Device 1 turns ON when TRAIC is triggered at 90° and Device 2 turns ON when TRAIC is triggered at 126°. A user interface is created to demonstrate controlling of two lights using LabVIEW graphical programming. The results of which are shown in Fig. 14.

5 Conclusion

This paper successfully proposes a simple, practical, cost effective, automation system based on Power-line Communication for smart controlling of lights in which the use of high frequency carrier wave has been eliminated. Elimination of use of high frequency carrier wave greatly reduces the chance of noise interference in the power line which is normally designed to carry only 50/60 Hz signal. The designed smart system uses laptop/PC which eliminates the use of manual switches to drive only two loads. Though the prototype is under development, the most important feature of our project, i.e. to send the data over power lines which have been accomplished fulfils the prime requirement of the project. The system design can be further simplified/updated by using Arduino board and Simulink model to control the TRIAC firing angle. The appliances can be controlled remotely by implementing the current system with a Wi-Fi shield. Our idea can deliver clear benefits about resource utilization, energy conservation and cost reduction to users.

References

1. Son, Y.S., Pulkkinen, T., Moon, K.D., Kim, C..: Home energy management system based on power line communication. IEEE Trans. Consum. Electron. **56**(3) (2010)
2. Gungor, V.C., Sahin, D., Kocak, T., Ergut, S., Buccella, C., Cecati, C., Hancke, G.P.: Smart grid technologies: communication technologies and standards. IEEE Trans. Industr. Inf. **7**, 529–539 (2011)
3. Ju, S.H., Lim, Y.H., Choi, M.S., Baek, J.M., Lee, S.Y.: An efficient home energy management system based on automatic meter reading. In: IEEE International Symposium on Power Line Communications and its Applications (ISPLC), pp. 479–484 (2011)
4. Lung, K.C.: The design and implementation of a home automation network system using power line communication. M.A. thesis, National Cheng Kung University, Taiwan, July 2006
5. D'Alessandro, S., Tonello, A.M., Monacchi, A., Elmenreich, W.: Home energy management systems: design guidelines for the communication infrastructure. In: IEEE International Energy Conference, pp. 805–812 (2014)

6. Zhai, Z.: Discussion and analysis about transmission mode of electric power communication. Telecommun. Electric Power Syst. **27**, 61–63 (2006)
7. Mahoor, M., Najafaabadi, T.A., Salmasi, F.R.: A smart street lighting control system for optimization of energy consumption and lamp life. In: The 22nd Iranian Conference on Electrical Engineering, Shahid Beheshti University, pp. 1290–1294 (2014)
8. Dange, H.V., Gondi, V.K.: Power line communication based home automation and electricity distribution system. Process In: Automation, Control and Computing (PACC) International Conference, IEEE, pp. 1–6, Coimbatore (2011)
9. Li-jun, Q., Zi-zheng, S., Feng, J.: Intelligent Streetlight Energy-saving System Based on Lon Works Power Line Communication Technology. IEEE, pp. 663–667 (2011)
10. Peng, S.C., Dai, L.S., Su, T.H.: The design of smart electrical outlet for smart home base on PLC. In: International Conference on Intelligent Green Building and Smart Grid (IGBSG), pp. 1–4 (2014)
11. Shwehdi, M.H., Khan, A.Z.: A power line data communication interface using spread spectrum technology in home automation. IEEE Trans. Power Deliv. **11**, 1232–1237 (1996)
12. Ping, Y., Heng-Ming, Y.: A Practical intelligent home system based on power line communication. In: 2nd International Conference on Power Electronics Systems and Applications, Hong Kong. IEEE, pp. 273–276 (2006)
13. Pandi Jothi, M., Selvam C., Ramakrishnan, S.: Implementation and testing of power line communication network for lamp control application. In: IEEE International Conference on Advanced Communication Control and Computing Technologies, Ramanathapuram, pp. 974–978 (2014)

Modelling and Analytical Study of Linear Induction Motor and Its Air Gap Flux Measurement at Different Slip

Prasenjit D. Wakode, Mohd Tariq, T.K. Bhattacharya and C. Bharatiraja

Abstract The paper presents a complete modelling and analysis of the Linear Induction Motor (LIM). The dimensions of the different parts of LIM prototype are given in the paper. The main air gap flux component, i.e. *Y* components (magnetic flux density distribution $B_y(x, t)$ is calculated using the theoretical equations and compared with the MATLAB®/Simulink-based results. The analysis of the primary winding is also presented in the paper and it is traced from the flux density when only phase "*A*" is energized.

Keywords Linear induction motor · Air gap flux · Slip · Magnetic flux density distribution · Windings

1 Introduction

The rotary induction motor produces the rotational motion but for applications such as transportation and in electric traction system where a translation motion is required a Linear Induction Motor (LIM) can be used as it offers many advantages. The LIM is the advanced version of rotary induction motor which gives a linear translational motion instead of the rotational motion [1]. The stator is cut axially

P.D. Wakode
Bharat Heavy Electrical Limited, Bhopal, India
e-mail: prasenjit926@gmail.com

M. Tariq (✉)
School of Electrical and Electronic Engineering, Nanyang Technological University, Singapore, Singapore
e-mail: tariq.iitkgp@gmail.com

P.D. Wakode · M. Tariq · T.K. Bhattacharya
Department of Electrical Engineering, Indian Institute of Technology, Kharagpur, India

C. Bharatiraja
Department of EEE, SRM University, Kattankulathur, Chennai, India

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_57

and spread out flat. In this type of motor, the stator and rotor are called primary and secondary respectively. The secondary of the linear induction motor consists of a flat aluminium conductor with a ferromagnetic core.

The main application of the LIM is in transportation and in electric traction system. For example, in a traction system the primary is mounted on the vehicle/train and the secondary is laid on the railway track. In many countries the transportation network is based on LIM [2, 3]. Other applications of induction motor beside transportation are in railway engines, self-excited induction generators for distributed generation in rural areas, etc. [4–6]. LIM, can provide a levitation effect. Hence, they are mainly used in where contactless force is required, where low maintenance is desirable, or where the duty cycle is low. The properties mentioned above make the LIM to be used often in maglev propulsion, as in the Japanese Linimo magnetic levitation train line near Nagoya [7].

In literature, the analysis of the LIM is presented along with the experimental results in [8] while the effect of the conductor reactance, resistance and the construction of the secondary structure on the performance of the LIM is given in [9, 10]. In some of the analysis presented in the literature, attraction force and transverse edge effect of LIM is also given. The analysis and measurement of the Air Gap Flux is very important and essential with respect to the machine as it helps to know the characteristics of the machine. Despite all the researches related to the LIM as discussed above gives a detail analysis of the LIM, its performance, its application, etc., but the research related to the measurement of the air gap flux at different slips is missing in the literature. Henceforth, the authors have taken this opportunity to explore this area and report the interesting finding as mentioned in the subsequent section of the paper.

2 Specification and Measurements of Single-Sided Linear Induction Motor (LIM) Dimensions

The short primary flat type single-sided LIM prototype used for experimental test has the structure and parameters as shown in Fig. 1 and Table 1 respectively. The figure shows the different parts of LIM and their dimensions and the directions assumed along X, Y and Z axes are also mentioned. Figure 1 shows the longitudinal direction view whereas Fig. 2 shows the transverse direction view.

As shown in Fig. 1, the primary iron core has slots and teeth so as to accommodate windings in it. It is made up CRGO laminations (as in the case of transformer or induction motor). The half path of the air gap flux is completed through this. The core also increases the amount of flux created by the mmf applied by the windings. The back iron at the secondary part actually acts as a return path for the air gap flux, i.e. the flux produced by the primary emerges out of primary core travels through the air gap and then returns back to the air back towards primary part. This return path is provided by the secondary back iron. The secondary back

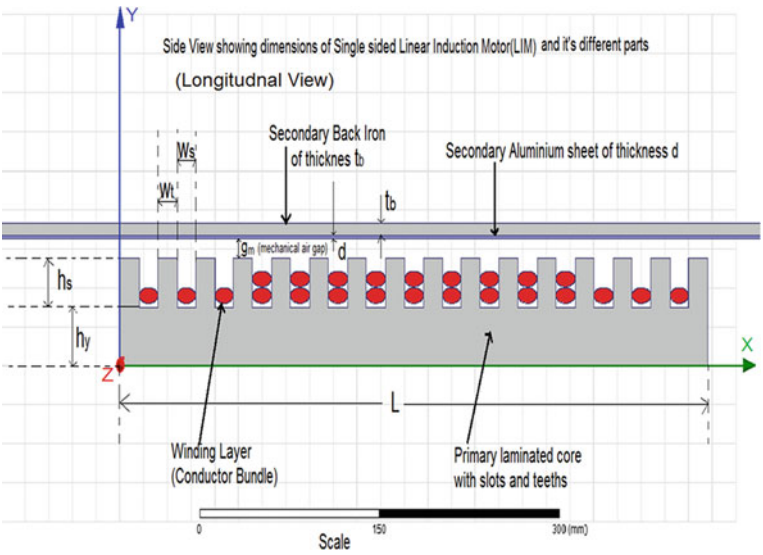


Fig. 1 LIM longitudinal side view showing different parts

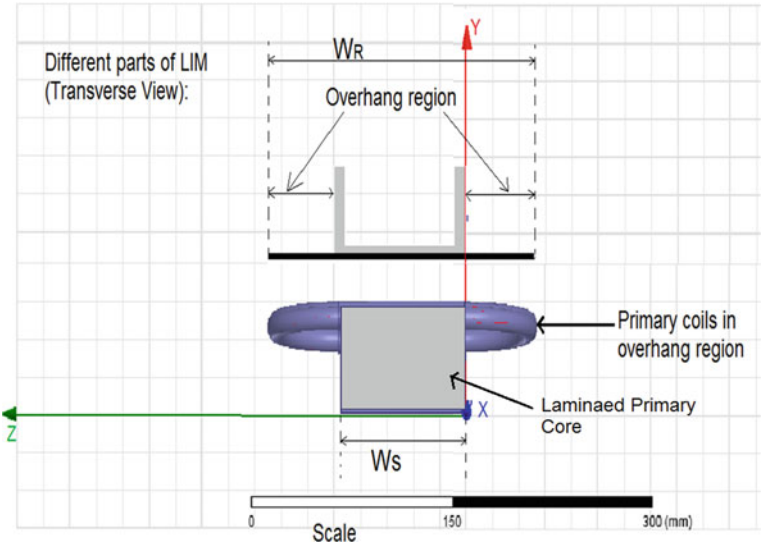


Fig. 2 LIM transverse side view showing different parts

Table 1 LIM dimensions of different parts

(a) LIM primary laminated core:	
Length of the LIM primary laminated core: L	48.6 cm
Width of the LIM primary laminated core: W_s	9.5 cm
Number of teeth and slots	15 slots and 16 teeth
Width of a slot on primary: w_s	1.6 cm
Width of the tooth or projection on primary: w_t	1.6 cm
(b) LIM primary laminated core:	
Width of secondary aluminium sheet: w_R	19.8 cm
Thickness of secondary aluminium sheet: d	2 mm
Thickness of secondary back iron : t_b	6 mm
Width of secondary back iron: W_B	10 cm
Width of overhang (OH) part of aluminium sheet: W_{OH}	4.85 cm

iron increases the air gap flux by providing the return path to it thereby reducing the leakage flux. Hence, the secondary back iron increases the propulsion force developed by LIM.

If secondary back iron is not there and only aluminium plate is only there, then the propulsion force still will be developed but it will be very less due to large leakage flux. If there is only back iron and no aluminium sheet, then the iron of primary core and back iron will have strong force of attraction, hence no propulsion force will be developed. The back iron used in the LIM prototype is of about 8 mm thickness.

The secondary aluminium plate is made up of a paramagnetic material like aluminium. The aluminium sheet carries the induced eddy currents due to the AC air gap flux crossing it. This is the key part in LIM structure. The aluminium sheet is analogous to the short-circuited copper bars by end rings as in case of rotor of squirrel cage rotor. The eddy current induced in the aluminium sheet gives rise to secondary flux and the interaction the primary and secondary flux produces the propulsion force. The iron–iron attraction is reduced by this aluminium plate hence the more amount of horizontal thrust is developed.

3 Analysis of Windings of LIM Primary

The LIM windings of phase *A* are as shown in Fig. 3. This winding is traced from the Flux density when only phase *A* is energized and observed finding the *Y* component of flux density as shown by CRO. The winding of each phase is in such a way as to obtain the opposite poles one after another as denoted by dot and cross in Fig. 3. So, the 3-phase windings are connected in the following manner as shown in Fig. 4. (FINISH ends *X*, *Y*, *Z* are joined together to get a neutral N terminal to form a star-connected 3-phase winding.)

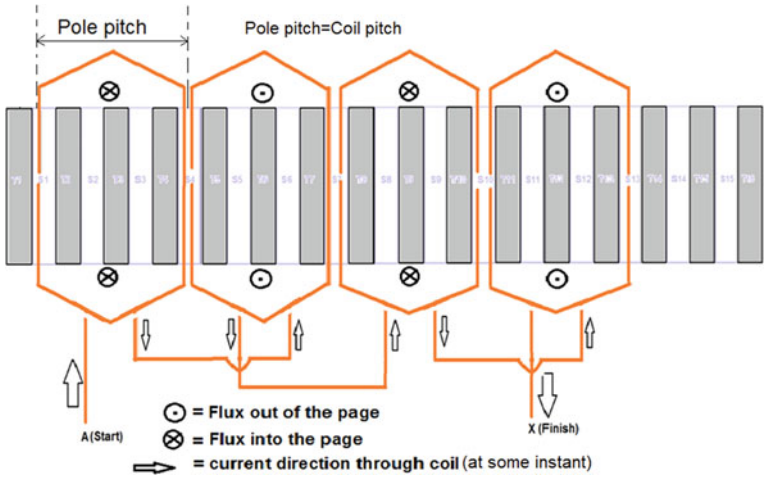


Fig. 3 LIM primary winding of only one phase

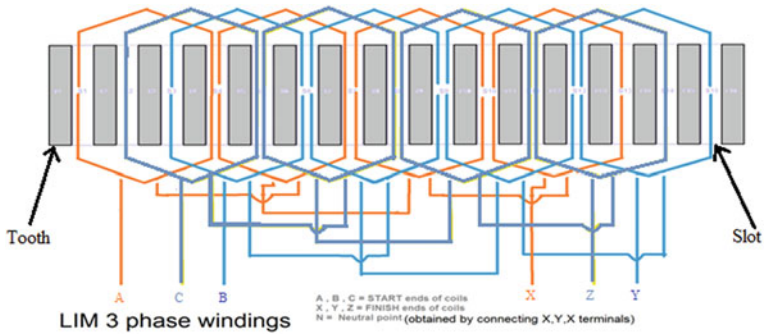


Fig. 4 LIM 3 phase primary windings with their respective ends

By observing the actual physical windings and flux pattern produced by it, it can be concluded that the coil pitch of winding is same as the pole pitch. Hence, it is a full-pitched coil. The length of pole pitch is equal to the length of the 3 slot pitches. Also, at both the ends, 3 slots of LIM carry the single-layered winding and the 9 slots carry the double-layered windings.

The LIM primary part is provided with wheels which run on a rail put under the secondary part as shown in Fig. 5. So in this case the primary is the moving member. The LIM secondary has the length of 4 m and at each end, the buffers are located so that LIM will hit the buffers when it reaches one of the ends.

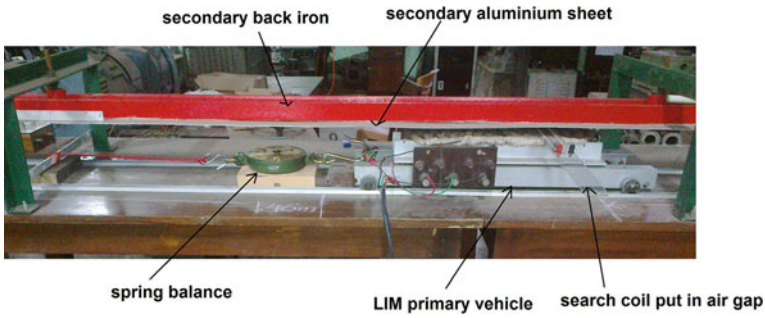


Fig. 5 Actual LIM prototype used for experiments (at blocked rotor condition)

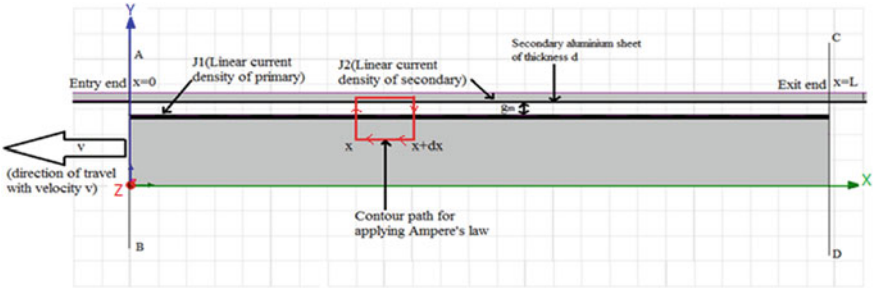


Fig. 6 LIM primary and secondary equivalent current sheets assumption for air gap flux density's *Y*-component derivation

4 Air Gap Flux Measurement

The study and analysis of the air gap flux measurement is essential keeping in view the fact that the physical cutting and opening by unrolling of the cylindrical/annular structure of Induction motor to develop LIM gives rise to some additional effects and phenomena which are simply not present in the cylindrical structure of induction motor.

Let us assume that the LIM is moving in the left direction as shown in Fig. 6. As per the assumed direction of movement of LIM, the line *A–B* marks the entry end and line *C–D* marks the exit end of LIM. As LIM is moving continuously, hence from the entry end the new unmagnetized secondary material is always entering the magnetic field of air gap and from the exit end the secondary material which is magnetized due to being in the air gap region of flux is continuously leaving the air gap flux region. The secondary material is leaving the exit end after being in the air gap magnetic field for the time $Tv = L/v$ (s), where L = Length of LIM primary (m), v = speed of LIM travel (m/s). Hence, the flux at entry end *A–B* and at exit end *C–D* need not be the same.

The induction motor has a cylindrical structure hence there are no definite 'beginnings' or 'endings' of its structure but in case of LIM, there are definite entry and exit ends with different magnetic profiles at these ends. Hence, the quantities such as magnetic flux, secondary sheet current density, forces on secondary, etc., are different at these two ends.

Due to open magnetic structure and large air gaps than the induction motor, the magnetic reluctances in case of LIM are more than that of induction motor.

Boundary conditions used for flux density calculation:

$$Az(x) \quad \text{at } x = 0, \text{ i.e. } Az(0) = 0 \text{ and } Az(x) \text{ at } x = L \text{ i.e. } Az(L) = 0$$

4.1 Calculation of Magnetic Flux Density Distribution $B_y(x, t)$

Let the linear current density in primary windings be

$$j_1(x,t) = J_1 \cdot \cos\left(wt - \frac{\pi \cdot x}{\tau}\right) \text{ (A/m)} \tag{1}$$

At any time "t" and at a point on primary winding at a distance "x" on measured from entry end. Let, $k = \frac{\pi}{\tau}$ (/m)is the wave number.

Using Ampere's circuital law to the contour as shown in Fig. 6 and we get expression for B_y in (2) as a function of time t and longitudinal distance x as follows:

$$B_y(x,t) = \text{Real}\{B_y(x) \cdot e^{j\omega t}\}$$

$$\begin{aligned} B_y(x) &= \delta \cdot C1 \cdot e^{-\delta x} - \gamma \cdot D1 \cdot e^{+\gamma x} + j \cdot \frac{\widehat{J}_1 \cdot \frac{\mu_o}{g_e} \cdot e^{-j \cdot k \cdot x}}{k \cdot (1 + j \cdot s \cdot G)} \quad \text{(tesla)} \\ &= B_y f(x) + B_y b(x) + B_y o(x) \end{aligned} \tag{2}$$

where, forward travelling-attenuated magnetic field due to entry end effect,

$$B_y f(x) = \delta \cdot C1 \cdot e^{-\delta x}$$

Backward travelling-attenuated magnetic field due to exit end effect,

$$B_y b(x) = -\gamma \cdot D1 \cdot e^{+\gamma x}$$

Synchronously travelling magnetic field in forward direction,

$$B_y o(x) = j.\frac{\widehat{J}_1 \cdot \frac{\mu_o}{g_e} \cdot \mathrm{e}^{-j.k.x}}{k \cdot (1 + j \cdot s \cdot G)}$$

where, Imaginary number, $j = \sqrt{-1}$.

Wave number (/m), $k = \pi/\tau$.

Primary linear current density peak value

$$J1 = \frac{\sqrt{2} \cdot N1 \cdot m \cdot Kw \cdot Is}{\tau P_e}(A/m). \tag{3}$$

P_e equivalent number of primary pole pairs, $P_e = \frac{(2P-1)^2}{4P-3+\frac{c}{mq}}$

Is Primary RMS phase current (A);

f Primary supply frequency (Hz)

Kw Primary winding factor

μ_o Permeability of air = 4 $\pi \times 10^{-7}$ H/m

Effective 'Goodness factor', G;

$$G = \frac{2f \cdot \tau^2 \cdot \mu_0 \cdot \sigma_e \cdot d}{\pi \cdot g_e} \tag{4}$$

Slip, $s = \frac{v_s - v}{v_s}$ where, v_s = synchronous speed$\left(\frac{m}{s}\right) = 2f\tau$, v = LIM speed (m/s). From the boundary conditions $Az(0) = Az(L) = 0$, we get following coefficients,

$$C_1 = \frac{-J1 \cdot \mu_o / g_e}{k^2(1 + jsG)(\mathrm{e}^{\gamma L} - \mathrm{e}^{-\delta L})}\left(\mathrm{e}^{\gamma L} - \mathrm{e}^{-jkl}\right) \tag{5}$$

$$D_1 = \frac{-J1 \cdot \mu_o / g_e}{k^2(1 + jsG)(\mathrm{e}^{\gamma L} - \mathrm{e}^{-\delta L})}\left(-\mathrm{e}^{-\delta L} + \mathrm{e}^{-jkl}\right) \tag{6}$$

Attenuation constant for forward travelling wave (/m)

$$\delta = -\frac{k(1-s)G}{2} + \sqrt{\left(\frac{k(1-s)G}{2}\right)^2 + j \cdot Gk^2}$$

Attenuation constant for backward travelling wave (/m)

$$\gamma = +\frac{k(1-s)G}{2} + \sqrt{\left(\frac{k(1-s)G}{2}\right)^2 + j \cdot Gk^2}$$

Effective air gap 'g_e' determination:

Equivalent air gap (m): $g_e = g_o \cdot Kcg$

Length of magnetic path in Y direction in air gap: $g_o = g_m + d$

Modified Carter's coefficient: $Kcg = \frac{Kc\cdot(g_m+d)g_m+d^2-d\cdot g_m}{g_m^2+d^2}$

Carter's coefficient: $Kc = \frac{(w_s+w_t)}{(w_s+w_t)-\gamma 1\cdot g_o}$

$$\gamma 1 = \frac{4}{\pi}\left\{\frac{w_s}{2\cdot g_o}\cdot\tan^{-1}\left(\frac{w_s}{2g_o}\right) - \ln\sqrt{1+\left(\frac{w_s}{2g_o}\right)^2}\right\} \tag{7}$$

Effective volume resistivity of secondary sheet σ_e determination:

Equivalent volume conductivity of secondary aluminium sheet because of transverse edge effects is given by $\sigma_e = \sigma \cdot K_{RN}$

Volume resistivity of secondary aluminium sheet at T °C, $\rho = 2.826 \times 10^{-8}(1 + 0.0038 * (T - 20))$ (Ω m). T °C is high when aluminium sheet becomes hot.

Conductivity of secondary aluminium sheet $\sigma = 1/\rho$.

Russel–Norsworthy constant, $K_{RN} = 1 - \frac{2}{kW_s}\left\{\frac{\tan h\left(\frac{kW_s}{2}\right)}{1+\tan h\left(\frac{kW_s}{2}\right)\tan h\left(\frac{k(W_R-W_s)}{2}\right)}\right\}$

From Eq. 2 of $B_y(x, t)$ at blocked rotor, i.e. slip, $s = 1$, supply frequency 50 Hz, line current Is = 12 A, mechanical air gap of $g_m = 1$ cm, temperature of aluminium as T = 85 °C as it also gets hot during flux measurement and considering the equivalent pole pairs Pe = 2.286, we get the following $B_y(x, t)$ as a function of distance from entry end, i.e. x at $t = 0$ as shown in Fig. 7.

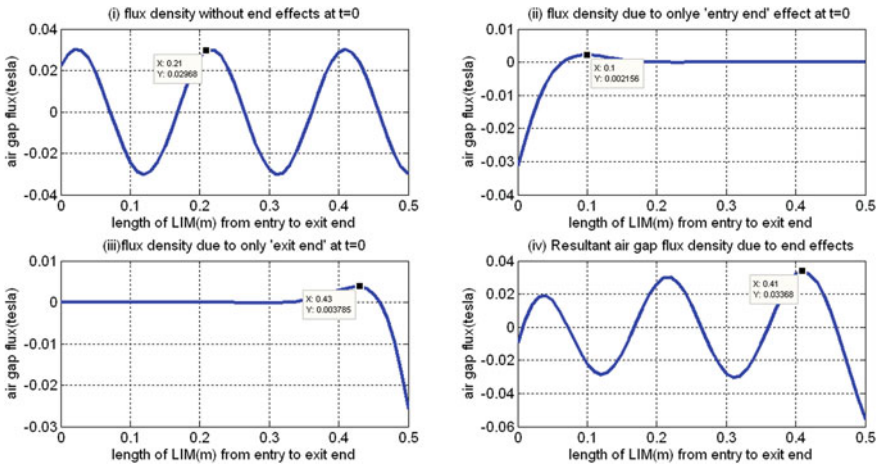


Fig. 7 MATLAB calculated resultant $B_y(x, t)$ wave with all its components as per Eq. (2) at $t = 0$, slip $s = 1, f = 50$ Hz, $Iph = 10$ A with 1 cm air gap, temperature of secondary aluminium sheet as 85 °C

5 Results and Discussions

The results are shown in Figs. 7, 8 and 9. It can be observed from the Figs. 7 and 9 that at the end regions, the resultant wave in Fig. 9 has much more flux density as compared to the experimentally measured maximum air gap flux density distribution. This is because in the derivation of Eq. (2), the primary current density is assumed to be same throughout LIM length, but in case of actual LIM, the 3 end slots at each end are filled with single-layered windings, hence current density at these end regions is less than that compared to the mid region where slots are filled with double-layered windings. It is also observed that the forward travelling wave due to entry end reduces the resultant flux density at the entry end. This is called

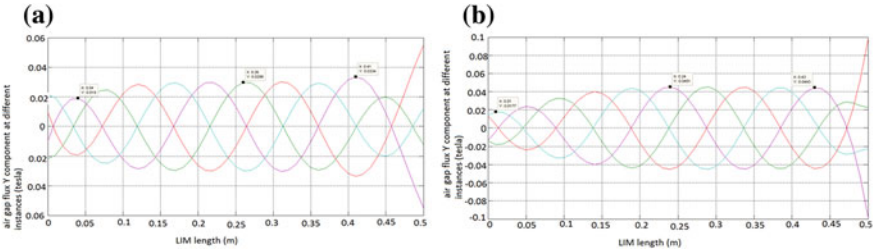


Fig. 8 **a** Resultant air gap flux density when 3 phase supply is given to LIM at supply frequency f = 50 Hz, *Iph* = 10 A at 'Blocked rotor' condition and secondary aluminium temp. = 85 °C, air gap = 1 cm **b**. Resultant air gap flux density when 3 phase supply is given to LIM at supply frequency f = 50 Hz, *Iph* = 10 A at slip s = 0.03 and secondary aluminium temperature = 30 °C at air gap = 1 cm

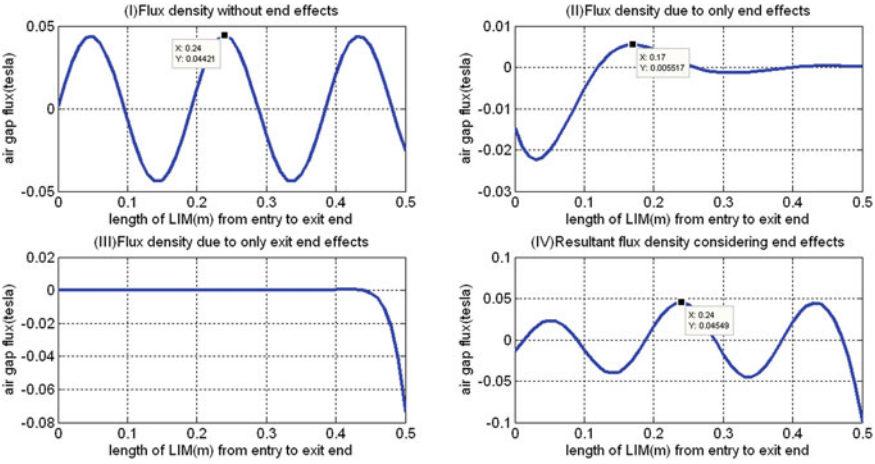


Fig. 9 MATLAB calculated resultant $B_y(x, t)$ wave with all its components as per Eq. (2) at t = 0, slip s = 0.03, aluminium temperature 30 °C

'entry end' effect. The backward travelling wave due to exit end has an effect of increasing the resultant air gap flux at the exit end. This is called the 'exit end' effect. The reduction of air gap flux at entry end due to forward travelling wave is more prominent than the effect of addition of flux due to the exit end wave as can be observed from Fig. 8a, b. The entry end effect becomes more prominent as the speed of LIM is increasing as can be observed from Fig. 9.

6 Conclusion

In this paper, the modelling and analysis of LIM has been done. The analysis was required keeping in mind the tremendous application, LIM is having in transport nowadays. Detail discussion of the experimental setup has been given in the paper along with its merit and demerit. Maximum air gap flux density Y component Bmax (tesla) for different conditions such as without and with the exit and end effects and at blocked rotor condition and at slip = 0.03 has been presented and discussed for better understanding of the subject.

References

1. Gong, J., Gillonand, F., Zhong, H.: Optimal Design of a Linear Induction Motor for Traction Application, pp. 251–258. Springer, Berlin (2016)
2. Lv, G., Liu, Z., Sun, S.: Analysis of torques in single-side linear induction motor with transverse asymmetry for linear metro. IEEE Trans. Energy Convers. **31**(1), 165–173 (2016)
3. Hellinger, R., Mnich, P.: Linear motor-powered transportation: history, present status, and future outlook. Proc. IEEE **97**(11), 1892–1900 (2009)
4. Tariq, M., Yuvarajan, S.: Modeling and analysis of self excited induction generator with electronic load controller supplying static loads. Can. J. Electr. Electron. Eng. **4**(1), 9–13 (2013)
5. Tariq, M., Yuvarajan, S., Wakode, P.: Digital simulation of electronic load controller with reduced THD for self-excited induction generator. IUP J. Electr. Electron. Eng. **6**(4), 36 (2013)
6. Tariq, M., Yuvarajan, S.: Simulink based modeling, analysis and simulation of self excited induction generator for use in remote areas. IU-J. Electr. Electron. Eng. **13**(1), 1623–1628 (2013)
7. Jacek, G.F., Piech, Z.J., Tomczuk, B.: Linear Synchronous Motors: Transportation and Automation Systems. CRC press (2016)
8. Wakode, P.D., Tariq, M., Bhattacharya, T.K.: Experimental analysis of linear induction motor under variable voltage variable frequency (VVVF) power supply. Trans. Environ. Electr. Eng. **1**(2) (2016)
9. Lee, B.-J., Koo, D.H., Cho, Y.-H.: Investigation of linear induction motor according to secondary conductor structure. IEEE Trans. Magn. **45**(6), 2839–2842 (2009)
10. Lv, G., Liu, Z., Sun, S.: Analysis of forces in single-side linear induction motor with lateral displacement for linear metro. IET Electr. Power Appl. **10**(1), 1–8 (2016)

Model Predictive Current Control of Single-Phase 13-Level Transistor-Clamped H-Bridge Based Cascaded Multilevel Inverter

K. Rameshkumar, V. Indragandhi, Geetha Mani and Padmanaban Sanjeevikumar

Abstract The manuscript presents a Model Predictive type Current Control (MPCC) of single-phase 13-level Transistor-Clamped H-Bridge (TCHB) based cascaded Multi Level Inverter (MLI) for improving power quality. The objective of the MPCC is to regulate the inverter output current by using 15 switches and 14 voltage vectors. The working condition of the MPCC strategy is investigated using steady state condition, transient state condition, variation of input frequency and variation of sampling time through simulations with RL load. The results show that the MPCC schemes perform well for all operating conditions and the inverter delivers a good quality of load voltage and load current with less harmonic components value. The inverter model and MPCC algorithm is implemented by using MATLAB software.

Keywords Cost function · Multi-level inverter · Predictive current control Sampling time · Total harmonic distortion

K. Rameshkumar (✉) · V. Indragandhi · G. Mani
School of Electrical Engineering, Vellore Institute of Technology (VIT) University, Vellore, Tamil Nadu, India
e-mail: rameshvel.k@gmail.com

V. Indragandhi
e-mail: indragandhi.v@vit.ac.in

G. Mani
e-mail: geethamani@gmail.com

P. Sanjeevikumar
Department of Electrical and Electronics Engineering, University of Johannesburg, Auckland Park, Johannesburg, South Africa
e-mail: sanjeevi_12@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_58

1 Introduction

Multilevel Inverter (MLI) has become more significant interest among the researchers in recent years due to its significant performance. Different MLI topologies which are used such as MLI with neutral-point-clamped, MLI with diode clamped, cascaded H-bridge and flying capacitor MLI. On comparing with all other types of MLI, the cascaded H-bridge MLI has an advantages like its high reliability, modular structure, extendibility, enhanced fault capability and easy to alter the number of levels with minimum changes [1]. Nowadays, the TCHB based cascaded MLI inverter topology has more attention amongst researchers due to its simple methodology to increase levels of output by delivering different voltage levels by utilizing the capacitors arranged in a sequence manner. The traditional methods for control of MLI inverter uses multicarrier PWM control technique [2], hysteresis current control [3], Space Vector Modulation (SVM) [4], feed-forward SVM [5] and in [6] new modulation scheme is used to produce the gating signals.

Amongst the various control approaches utilized in power electronics, Model Predictive Control (MPC) strategy has increased level of popularity due to many advantages like good dynamic performance, improved current quality and the MPCC of converters has been extensively studied in the last decade and found some application in power converters like three phase two-level inverter [7], two-level inverter with four-leg inverter operating under balanced, unbalanced and nonlinear loading conditions were analyzed [8, 9] and this control techniques are also implemented on single-phase nine-level inverter [10], grid connected flying capacitor inverter [11], Three phase nested Neutral Point-Clamped (NPC) converter [12], three phase four-leg NPC converters [13–15], multilevel diode clamped inverter [16], multilevel cascaded H-bridge inverters [17], and grid connected cascaded H-bridge inverters [18], asymmetric flying capacitor converter [19] and direct matrix converter [20].

From the above references, by considering MPCC technique for single phase, three phase inverter and three phases MLI under several conditions is discussed. The analysis of single phase 13-level TCHB cascaded based MLI with MPCC for several conditions is not being described yet. So in this manuscript the MPCC technique has been applied to the single phase 13-level TCHB cascaded based MLI to analyze the steady state, transient state conditions, supply frequency variation and sampling time varying conditions. This manuscript is systematized as follows. In Sect. 2, the inverter model is presented. In Sect. 3, description of the MPCC strategy with algorithm is presented. In Sect. 4, simulation outcomes are discussed. Finally Sect. 5 concludes the work.

2 Inverter Modelling

A representation of a single phase model 13-level TCHB depends on cascaded MLI connected to the RL load is shown in Fig. 1. Three independent DC energy sources are consider in this study and three H-bridge sections and equal number of bidirectional switches to the bridge sections are used to generate a required voltage level on its output terminals. This MLI operation includes switching states with count of 14, which is alters from S_1 to S_{14}.

Then the voltage vector V_i can be derived from the MLI supply voltage V_{dc} and switching state S_i by

$$V_i = V_{dc}(S_{i4} - S_{i2}) * \left\{\frac{1}{2}S_{i5} + |S_{i1} - S_{i2}| \cdot |S_{i3} - S_{i4}|\right\} \tag{1}$$

where V_i, S_i are MLI voltage vectors and switching states of inverter respectively with $i = 1, 2 \ldots 14$.

The vector representation of inverter load current can be represented by

$$v = Ri + L\, \mathrm{d}i/\mathrm{d}t \tag{2}$$

In the above equation the L, R and v are the load inductance, load resistance and voltage vector by the MLI.

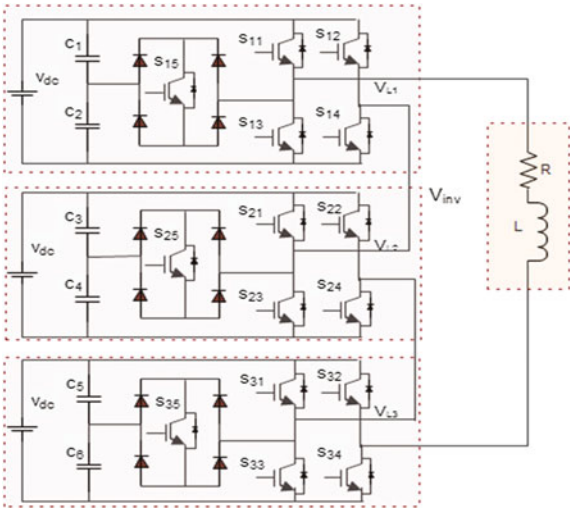


Fig. 1 Single-phase 13-level TCHB based cascaded MLI

3 Model Predictive Current Strategy

The MPCC scheme of MLI is presented in Fig. 2. Discrete system model, switching states and load current of MLI are taken to find out the upcoming variable performances to be regulated.

The system derivative $\frac{di}{dt}$ from Euler equation can be represented by

$$\frac{di}{dt} = \frac{i(k) - i(k-1)}{T_S} \tag{3}$$

Equation (3) is substituted in Eq. (2) the voltage vector can be represented by

$$v = Ri + L\frac{i(k) - i(k-1)}{T_S} \tag{4}$$

The inverter measured output current at the time of k is expressed by

$$i(k) = \frac{1}{RT_S + L} + [Li(k-1) + T_S v(k)] \tag{5}$$

Then the load current $i(k)$ is shifted in single step advance $i(k+1)$ and the predicted output current can be expressed by

$$i_p(k+1) = \frac{1}{RT_S + L} + [Li(k) + T_S v(k+1)] \tag{6}$$

In which $v(k+1)$ load voltage vector, and $i(k)$ is the monitored load current at the instant of k.

The most significant purpose of MPCC is to reduce the error among the references and a forecasted output load current which is defined as cost function or quality function (g). So in order to attain that objective, the inverter switching state

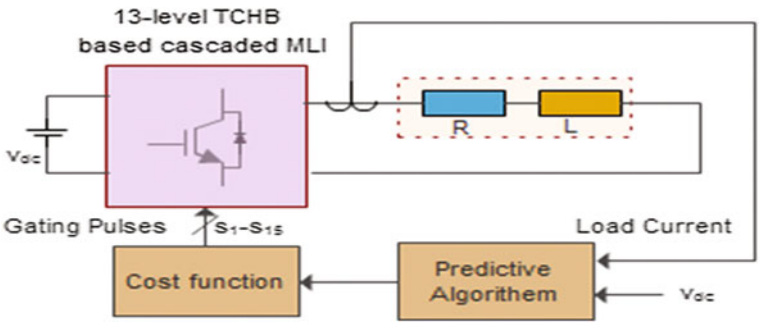


Fig. 2 Block diagram of MPCC of MLI

which is going to reduce 'g' is chosen and given at the time of next sampling instant.

In the subsequent sampling instant the difference among the reference load current and the predicted current of the load can be represented by

$$g = (i_{\text{Ref}}(k+1) - i_p(k+1)) \tag{7}$$

For computational simplicity absolute error is used in this manuscript. Other methods can be used to identify the cost functions such as error squared and it's represented as follows

$$g = (i_{\text{Ref}}(k+1) - i_p(k+1))^2 \tag{8}$$

Finally lowest of 'g' is selected and corresponding switching pulses is given as a gate pulse of the inverter. The detailed algorithm for control of MLI is as follows.

3.1 MPCC Algorithm for Inverter

The MPCC algorithm is implemented in MATLAB embedded function block. The functional block operates in the discrete update technique based on sampling time defined for the algorithm. The parameters used in this algorithm are shown in parameter initialization step, and each parameters are initialized with specific values (step 1). In step 2 the voltage vectors are estimated by using input supply voltage and 14 possible switching state and also the load current of inverter at specific value of (k + 1) are predicted by substituting eight voltage vectors and measured load current. The cost functions are calculated by relating the predicted current of load with the current reference as indicated in step 3. In step 4 cost function optimization is implemented. At last the switching state gives lowest 'g' which is selected and given to the MLI, as shown in step 5.

1. **Parameter initialization**
   Load Resistance = 150 Ω,
   Load inductance = 160 mH.
   Sampling frequency = 10 kHz
   Cost function at initial (g) = inf.
   Voltage vector at initial = V_1, and Switching state = S_1
2. **Voltage vector and load current prediction**
   $V_i = V_{\text{dc}}(S_{i4} - S_{i2}) * \left\{\frac{1}{2}S_5 + |S_{i1} - S_{i2}| \cdot |S_{i3} - S_{i4}|\right\} * /$ by using supply voltage and switching state $(S_1 - S_{14}) * /$
   Prediction of current at next instant
   $i_p(k+1) = \frac{1}{RT_S + L} + [L.i(k) + T_S v(k+1) /*$ considering inverter load current and voltage vector $(v_1 - v_{14})$*/

3. **Calculate '*g*' value**
   $g_{\text{value}} = (i_{\text{Ref}}(k+1) - i_p(k+1))$/* by using reference current and load current */
4. **Cost function optimization**

   If ($g < g_{\text{opt}}$) /*Optimum '*g*' and choice of choosing the switching state*/
   Updating optimal cost function and switching state

$$g_{\text{opt}} = g;$$
$$x_{\text{opt}} = i;$$

5. **Optimum switching state**
   $S_a = S(x_{\text{opt}}, 1)$; /*optimal switching state is given to inverter*/
   $S_b = S(x_{\text{opt}}, 2)$;
   $S_c = S(x_{\text{opt}}, 3)$;
   The optimal switching pulse obtained is given to the inverter.

4 Simulation Results

The operation of MPCC based Single-Phase 13-level TCHB based MLI under four different analysis has been taken and simulated in MATLAB/Simulink software. The parameters for inverter and load are indicated in Table 1. The reference current is defined manually. The concepts of MPCC and inverter model are discussed previously.

4.1 Steady State Analysis

In this analysis the MPCC technique is applied to the MLI with constant load and reference condition. Here the reference current amplitude is fixed as 2 A and inverter DC-Link voltage to be maintained at 120 V for each level. Figure 3

Table 1 Inverter and load parameters

Parameters	Value
Input voltage V	360 V (120 V for each level)
Frequency	50 Hz
Sampling time (T_s)	100 μs
Load resistance	160 Ω
Load inductance	160 mH
DC-link capacitor value	3300 μF

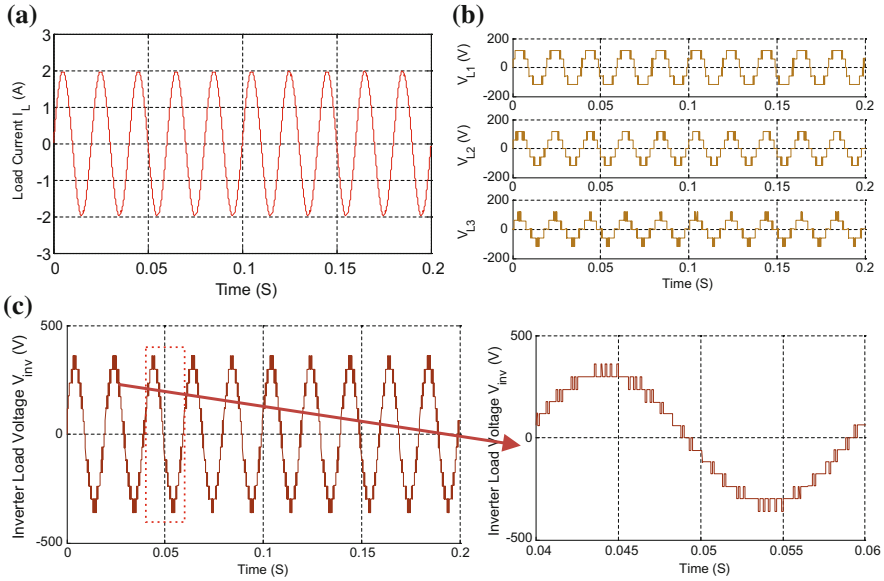


Fig. 3 Illustrates the simulation results concerning steady state response. **a** Load current, **b** inverter voltage at each level and **c** inverter load voltage

illustrates the simulated outcome of the load current, resultant output voltage 'V_{inv}' and voltage at each level (V_{L1}, V_{L2}, V_{L3}).

4.2 Transient State Response

In transient state condition, two different conditions are evaluated. In the first condition the reference current amplitude increases from 0 to 2 A at 0.04 s and consecutively current reference decreases from 2 to 1.5 A at 0.12 s with R = 160 Ω, L = 160 mH which is shown in Fig. 4.

In the second condition the current reference amplitude is fixed by 2 A with frequency of 50 Hz and the load resistance value changes from 150 to 165 Ω at 0.04 s and consecutively loads resistance changes from 165 to 175 Ω at 0.12 s that is depicted in Fig. 5. The result shows that the measured output current tracks its reference current instantly without any under or overshoot.

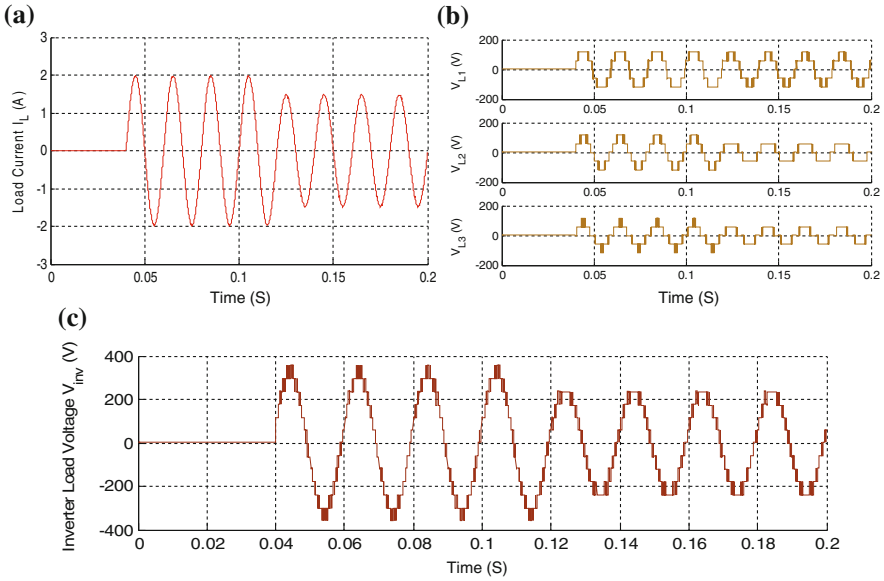


Fig. 4 Illustrates the simulation results concerning transient response of **a** load current, **b** inverter voltage at each level and **c** inverter load voltage

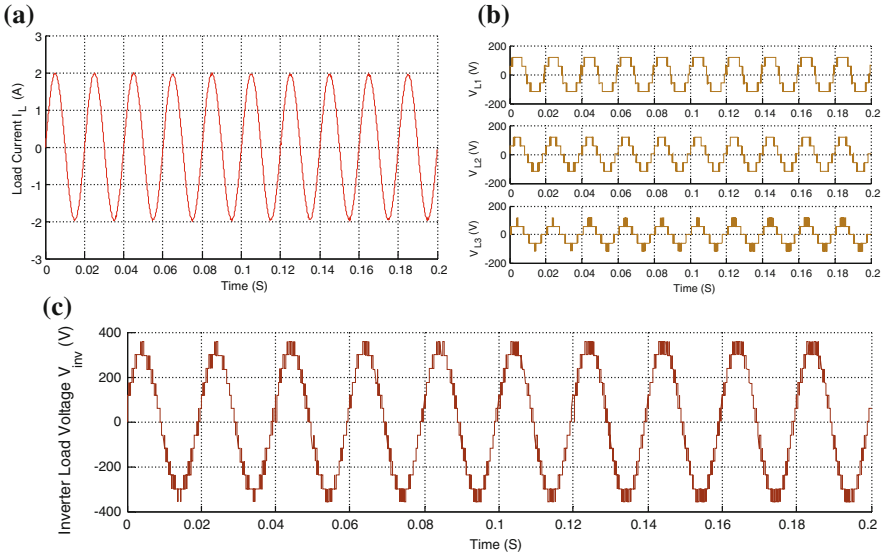


Fig. 5 Illustrates the simulation results concerning transient response of **a** load current, **b** inverter load voltage at each level and **c** inverter load voltage

4.3 Examination with Supply Frequency Variations

In this examination the reference current frequency changes from 50–100 Hz at 0.04 s and consecutively reference current frequency changes from 100 to 20 Hz at 0.11 s with R = 160 Ω, L = 160 mH. Figure 6 clearly shows that the load current tracks the reference with no overshoot.

4.4 Examination with Sampling Time Variations

The examination is tested by varying the sampling time, in that the output current and voltage THD varies according to the sampling time variation. The FFT analysis for inverter output current and voltage is given in Figs. 7 and 8. When the sampling time was set as 50 µs the THD shows 0.42% for current; 9.92% for voltage. However while increasing the sampling period from 100, 150 and 200 the THD for load current and load voltage also increases gradually as shown in Table 2.

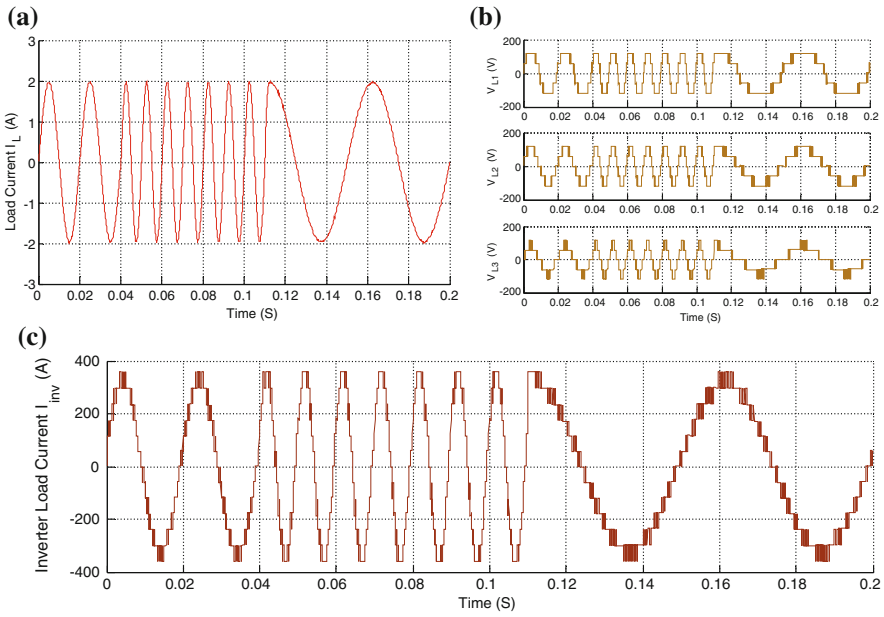


Fig. 6 Illustrates the simulation results concerning transient response of **a** load current, **b** inverter load voltage at each level and **c** inverter load voltage

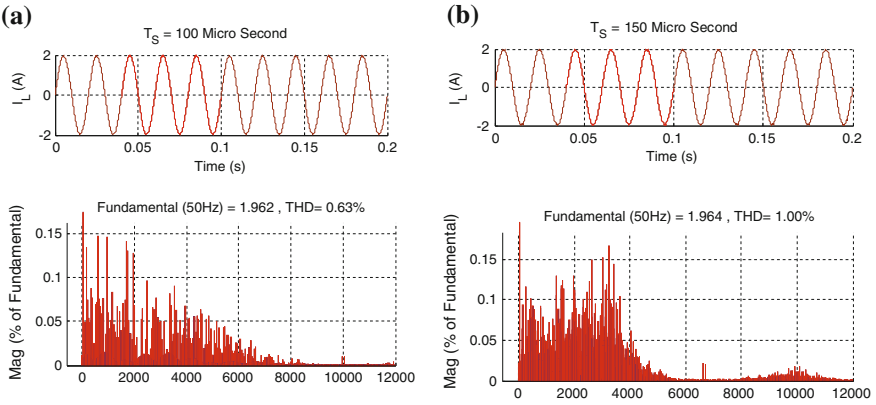


Fig. 7 THD for the load current with the sampling time of **a** 100 µs and **b** 150 µs

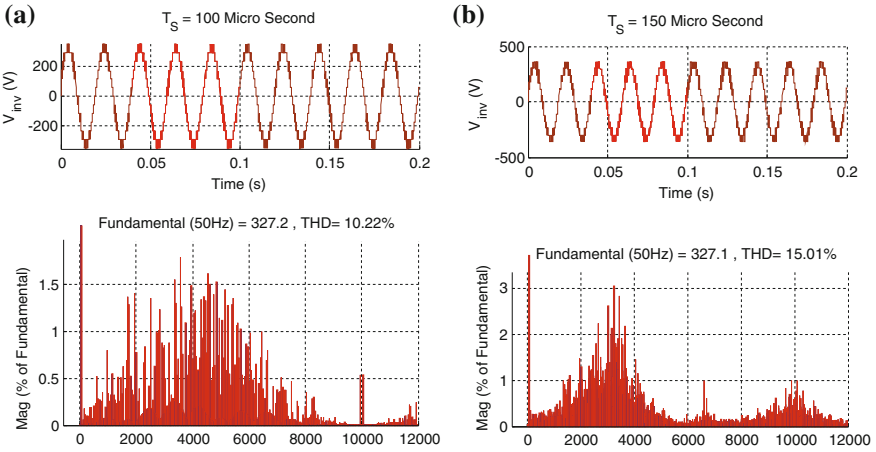


Fig. 8 THD for the load voltage with the sampling time of **a** 100 µs and **b** 150 µs

Table 2 THD for load current and load voltage with different sampling time

Sampling time T_s (µs)	THD %	
	Load current	Load voltage
50	0.42	9.92
100	0.63	10.22
150	1.0	15.01
200	2.2	32.74

5 Conclusion

The MPCC of single-phase 13-level TCHB based cascaded MLI was designed and analyzed with MATLAB Simulink model. And also, the performance indices i.e., steady state, transient state conditions, variation of reference current frequency and sampling time are exhibited with corresponding simulation results. It is proved that this control technique is simple and easy to exhibit in real time and straightforwardly prolonged to other type of converters with various applications, though it does not have a complex design and any modulating stages.

References

1. Halim, W.A., Rahim, N.A., Azri, M.: Selective harmonic elimination for a single-phase 13-level TCHB based cascaded multilevel inverter using FPGA. J. Power Electr. **14**, 488–498 (2014)
2. McGrath, B.P., Holmes, D.G.: Multicarrier PWM strategies for multilevel inverters. IEEE Trans. Industr. Electr. **49**, 858–867 (2002)
3. Shukla, A., Ghosh, A., Joshi, A.: Hysteresis current control operation of flying capacitor multilevel inverter and its application in shunt compensation of distribution systems. IEEE Trans. Power Deliv. **22**, 396–405 (2007)
4. Celanovic, N., Boroyevich, D.: A fast space-vector modulation algorithm for multilevel three-phase converters. IEEE Trans. Ind. Appl. **37**, 637–641 (2001)
5. Leon, J.I., Vazquez, S., Watson, A.J., Franquelo, L.G., Carrasco, J.M.: Feed-forward space vector modulation for single-phase multilevel cascaded converters with any DC voltage ratio. IEEE Trans. Industr. Electr. **56**, 315–325 (2009)
6. Rodríguez, J., Pontt, J., Correa, P., Silva, C.: A new modulation method to reduce common-mode voltages in multilevel inverters. IEEE Trans. Industr. Electr. **51**, 834–839 (2004)
7. Rodríguez, J., Pontt, J., Silva, C.A., Correa, P., Lezana, P., Cortes, P., Ammann, U.: Predictive current control of a voltage source inverter. IEEE Trans. Ind. Electr. **54**, 495–503 (2007)
8. Yaramasu, V., Rivera, M., Wu, B., Rodríguez, J.: Model predictive current control of two-level four-leg inverters—Part I: Concept, algorithm and simulation analysis. IEEE Trans. Power Electr. **28**, 3459–3468 (2013)
9. Rivera, M., Yaramasu, V., Rodríguez, J., Wu, B.: Model predictive current control of two-level four-leg inverters—Part II: Experimental implementation and validation. IEEE Trans. Power Electr. **28**, 3469–3478 (2013)
10. Kakosimos, P., Pavlou, K., Kladas, A., Manias, S.: A single-phase nine-level inverter for renewable energy systems employing model predictive control. Energy Convers. Manag. **89**, 427–437 (2015)
11. Trabelsi, M., Ghazi, K.A., Emadi, N.A., Brahim, L.B.: A weighted real-time predictive controller for a grid connected flying capacitors inverter. Electr. Power Energy Syst. **49**, 322–332 (2013)
12. Narimani, M., Wu, B., Yaramasu, V., Cheng, Z., Zargari, N.R.: Finite control-set model predictive control (FCS-MPC) of nested neutral point-clamped (NNPC) converter. IEEE Trans. Power Electr. **30**, 7262–7269 (2015)

13. Yaramasu, V., Rivera, M., Narimani, M., Wu, B., Rodríguez, J.: Finite state model-based predictive current control with two-step horizon for four-leg NPC converters. J. Power Electr. **14**, 1178–1188 (2014)
14. Vargas, R., Cortes, P., Ammann, U., Rodríguez, J., Pontt, J.: Predictive control of a three-phase neutral-point-clamped inverter. IEEE Trans. Ind. Electr. **54**, 2697–2705 (2007)
15. Yaramasua, V., Riverab, M., Narimania, M., Wu, B., Rodríguez, J.: High performance operation for a four-leg NPC inverter with two-sample-ahead predictive control strategy. Electr. Power Syst. Res. **123**, 31–39 (2015)
16. Yaramasu, V., Wu, B., Rivera, M., Narimani, M., Kouro, S., Rodríguez, J.: Generalized approach for predictive control with common-mode voltage mitigation in multilevel diode-clamped converters. IET Power Electr. **8**, 1440–1450 (2015)
17. Cortes, P., Wilson, A., Kouro, S., Rodríguez, J., Abu-Rub, H.: Model predictive control of multilevel cascaded H-bridge inverters. IEEE Trans. Ind. Electr. **57**, 2691–2699 (2010)
18. Han, J., Li, C., Yang, T., Han, J.: Simplified finite set model predictive control strategy of grid-connected cascade H-bridge converter. J. Control Sci. Eng. (2016)
19. Lezana, P., Aguilera, R., Quevedo, D.: Model predictive control of an asymmetric flying capacitor converter. IEEE Trans. Ind. Electr. **56**, 1839–1846 (2009)
20. Rivera, M., Rojas, C., Rodridguez, J., Wheeler, P., Wu, B., Espinoza, J.: Predictive current control with input filter resonance mitigation for a direct matrix converter. IEEE Trans. Power Electr. **26**, 2794–2803 (2011)

3-to-8 Decoder Implementation Using Single Electron Threshold Logic (SE-TL) for Low Power Computing

Arpita Ghosh and S.K. Sarkar

Abstract The reduction in power consumption for the computing devices requires the basic fundamental circuits to be realized with low power consuming technologies. This work mainly describes the design and implementation issues of one of the basic computing circuits, a 3:8 decoder, using single electron threshold logic. The single electron tunneling through a junction reduces energy consumption and the comparison of weighted sum with the threshold value gives the threshold logic approach.

Keywords Single electron tunneling · Threshold logic · 3:8 decoder SIMON · Power consumption

1 Introduction

The continuous technological upgradation demands higher packing density and low power consumptive devices. But due to the limitations of conventional MOS technology from the scaling point of view further reduction in its dimension has become almost impossible after a certain limit. The solution is in the form of different technologies for providing the desired results. Among them one of the emerging technologies is single-electron tunneling technology [1, 2]. It allows much higher packing density than the conventional MOS as well as very low power consumption. The different logical circuits can be implemented using this technology.

A. Ghosh (✉)
RCCIIT, Kolkata, India
e-mail: arpita161@gmail.com

S.K. Sarkar
Jadavpur University, Kolkata, India
e-mail: su_sircir@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_59

The low power computing devices are nowadays in high demand. If the single-electron tunneling is used along with the threshold logic [3–5] concept then as a result a very small-sized device with very low power consumption and high speed can be designed. Already several works have been done on the design of basic logic gates, multiplexer, programmable logic array [5], adder, subtractor but so far no work has been reported on the design of 3:8 decoder circuit.

This work explains the different design parameters, inputs, output conditions for the proposed 3:8 single electron threshold logic decoder circuit. The simulated waveforms for the input and out are presented to verify the logical results. Further the power consumption of the circuit is discussed in this paper.

2 3:8 Decoder Implementation

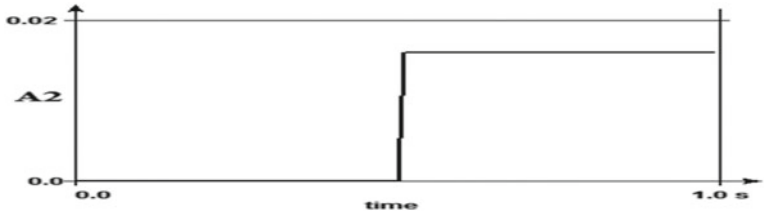
In threshold logic, generally the output logic is determined by the comparing the threshold value with the summation of all the weighted sums. If the threshold value is greater than the summation value then the logical output is considered to be 1 and if it is less than that then the output logic level is considered to be logic 0. Using the concept of the threshold logic gate the different basic gates can be designed such as AND, OR, NAND, NOR, NOT, etc. The single-electron tunneling uses the concept of controlled tunneling of a single or few numbers of electrons through a tunnel junction. The logical level determination using threshold logic and single electron tunneling technology is known as the single electron threshold logic (SE-TL) approach.

The decoder circuit is one of the important basic circuits of any complicated computational system. The design of the 3:8 decoder circuits using the SE-TL circuit is elaborated throughout the work.

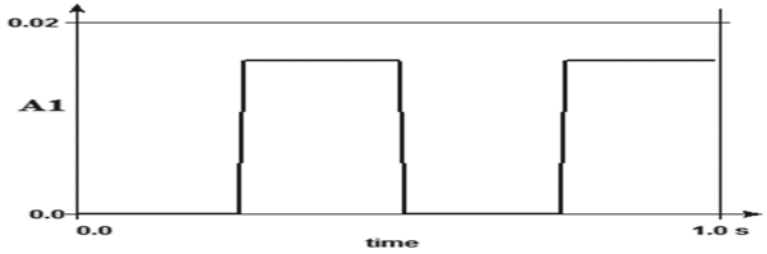
The circuit implementation requires three input signals. Figure 1a–c shows the input signal $A2$, $A1$, and $A0$ respectively. The complete circuit implementation and simulation is done in SIMON [6, 7, 8] platform. The proposed circuit design is shown in Fig. 2. Here, totally 8 numbers of three-input buffered AND gates are required and three extra buffers are needed for inverting the inputs. Total 52 tunnel junctions and 95 capacitors are required for the proposed circuit.

3 Result Verification

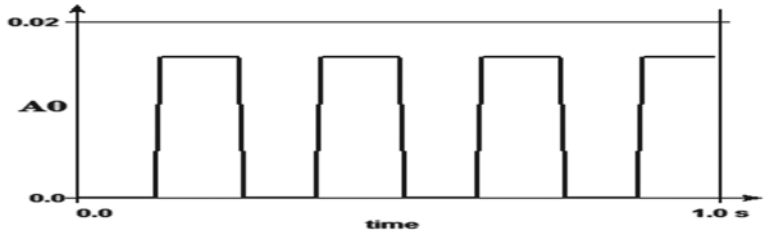
The simulated outputs are verified with the truth table of 3:8 decoder shown in Table 1.



(a)



(b)



(c)

Fig. 1 Input signal waveforms for **a** $A2$, **b** $A1$ and **c** $A0$

Corresponding to the given three input signals ($A2$, $A1$, $A0$) the different output signal waveforms ($Z0$, $Z1$, $Z2$, $Z3$, $Z4$, $Z5$, $Z6$, $Z7$) are shown in the Fig. 3a–h respectively. Here the logic high voltage level is 0.016 V and logic 0 is 0 V as the power supply voltage considered for the circuit design is 16 mV. The output $Z0$ is at logic high when $A0$, $A1$ and $A2$ are at logic low $\left(Z0 = \overline{A2} \cdot \overline{A1} \cdot \overline{A0}\right)$ and when all the inputs are at logic high the output $Z7$ is also logic high $(Z7 = A2 \cdot A1 \cdot A0)$, shown in Fig. 3a, h respectively. The other output signals are $Z1 = \overline{A2} \cdot \overline{A1} \cdot A0$, $Z2 = \overline{A2} \cdot A1 \cdot \overline{A0}$, $Z3 = \overline{A2} \cdot A1 \cdot A0$, $Z4 = A2 \cdot \overline{A1} \cdot \overline{A0}$, $Z5 = A2 \cdot \overline{A1} \cdot A0$ and $Z6 = A2 \cdot A1 \cdot \overline{A0}$.

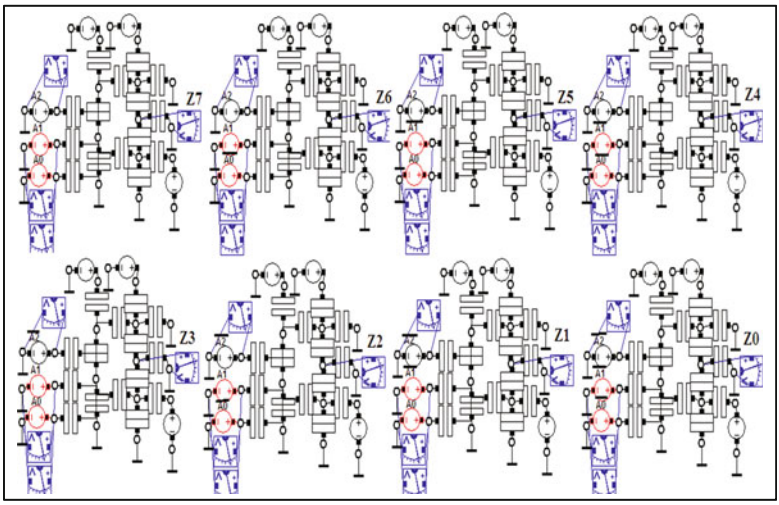


Fig. 2 SE-TL based 3:8 decoder

Table 1 Truth table for 3:8 decoder

Inputs			Outputs							
*A*2	*A*1	*A*0	*Z*7	*Z*6	*Z*5	*Z*4	*Z*3	*Z*2	*Z*1	*Z*0
L	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*L*	*H*
L	*L*	*H*	*L*	*L*	*L*	*L*	*L*	*L*	*H*	*L*
L	*H*	*L*	*L*	*L*	*L*	*L*	*L*	*H*	*L*	*L*
L	*H*	*H*	*L*	*L*	*L*	*L*	*H*	*L*	*L*	*L*
H	*L*	*L*	*L*	*L*	*L*	*H*	*L*	*L*	*L*	*L*
H	*L*	*H*	*L*	*L*	*H*	*L*	*L*	*L*	*L*	*L*
H	*H*	*L*	*L*	*H*	*L*	*L*	*L*	*L*	*L*	*L*
H	*H*	*H*	*H*	*L*	*L*	*L*	*L*	*L*	*L*	*L*

4 Power Consumption

The energy consumption of the AND gate is 11.14 meV and there are totally 8 AND gates. The power consumption of the complete circuit is 62 pW, which is much lower than the MOS-based same circuit. Implementation of the same circuit using MOS consumes power in the range of μW.

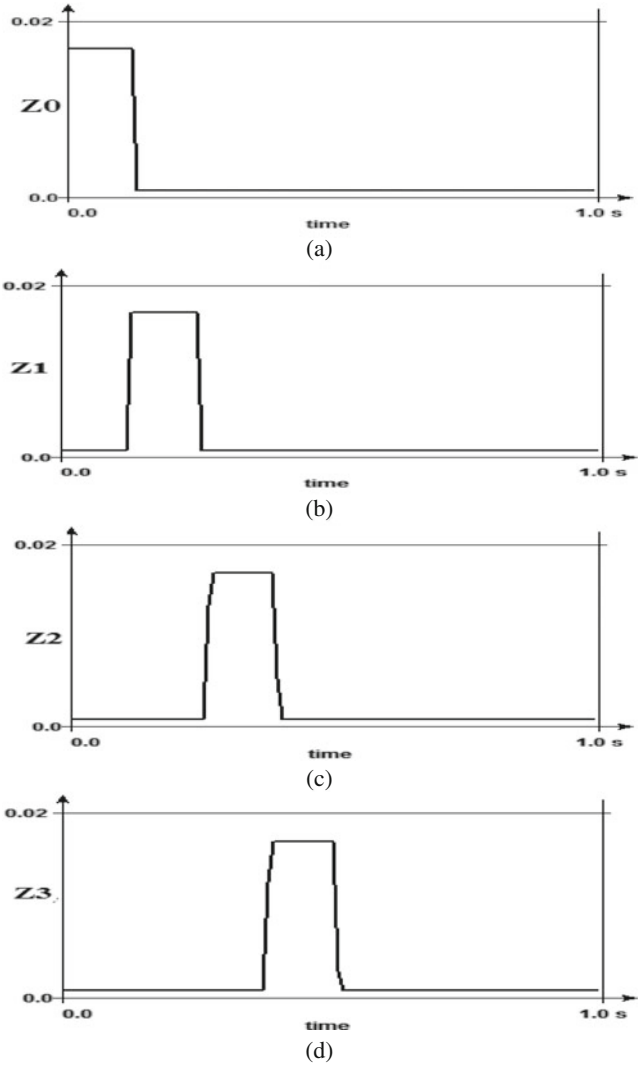
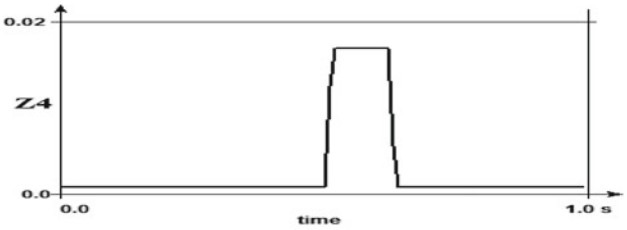
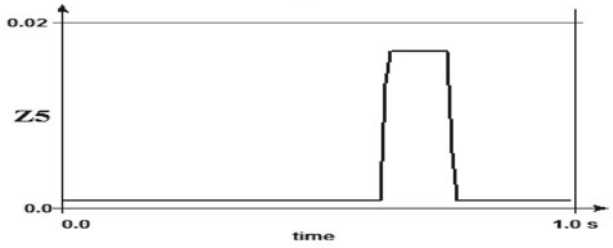


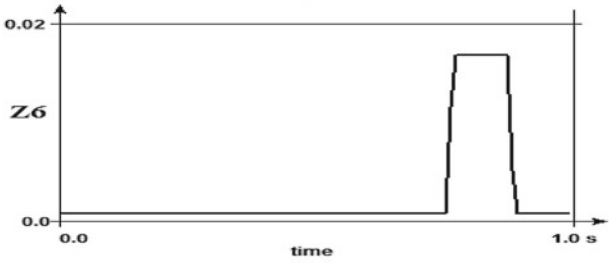
Fig. 3 The output waveforms for **a** *Z*0, **b** *Z*1, **c** *Z*2, **d** *Z*3, **e** *Z*4, **f** *Z*5, **g** *Z*6, **h** Z7



(e)



(f)



(g)

(h)

Fig. 3 (continued)

5 Conclusion

In this complete work, a single electron threshold logic-based 3:8 decoder circuit is proposed. The power consumption of the designed circuit is in the pW range which is much lower than conventional MOS based same circuit. Due to the use of single electron tunneling technology the size of the decoder is also small. The logical

justification of the circuit is done using the simulated input output waveforms. So the presented circuit proves itself to be eligible for the low power computing system.

References

1. Likharev, K: Single-electron devices and their application. Proc. IEEE **87**(4), 606–632 (1999)
2. Lageweg, C., Cotofana, S., Vassiliadis, S.: Buffer design trade-offs for single electron logic gates. In: Proceedings of 2005 5th IEEE Conference on Nanotechnology, Nagoya, Japan, July 2000
3. Ghosh, A., Jain, A., Singh, N.B., Sarkar, S.K.: A comparative study of single electron threshold logic-based and SET-MOS hybrid based half subtractor. In: Computational Advancement in Communication Circuits and Systems. Lecture Notes in Electrical Engineering, vol. 335, pp. 367–373
4. Fernandez Ramos, J., Hidalgo Lopez, J.A., Martin, M.J., Tejero, J.C., Gago, A.: A threshold logic gate based on clocked couple inverters. Int. J. Electron. **84**(4), 371–382 (1998)
5. Ghosh, A., Jain, A., Singh, N.B., Sarkar, S.K.: Reliability aspects and performance analysis of single electron threshold logic based programmable logic array. J. Comput. Theoret. Nanosci. **12**(9), 2405–2414(10) (2015)
6. Thuslim, A.F., Kanan, V.: The novel design method of 3–8 decoder. IOSR J. Electron. Commun. Eng. **10**(2), ver-1, 92–95 (2015)
7. Ghosh, A., Jain, A., Sarkar, S.K.: Design and simulation of single electron threshold logic gate based programmable logic array. Proc. Technol. **10**, 866–874 (2013)
8. Wasshuber, C.: SIMON-A simulator for single-electron tunnel devices and circuits. IEEE Trans. Comput. Aided Des. Integr. Circ. Syst. **16**, 937–944 (1997)

Parallel Investigation of Different Task Schedulers at Greencloud for Energy Consumption in Datacenters

S. Aarthee and R. Prabakaran

Abstract Energy consumption in datacenters depends upon its workload in execution of processes in which the resources are handled by the processors. In datacenters, the consumed energy leads to reducing the operational cost from that the organization can save money to improve the economy and also enhances the quality of life with green environment. In this paper, we compared different task schedulers namely Green Scheduler (Consolidation based scheduler), Round Robin Scheduler, Random Scheduler, Heterogeneous Energy-efficient Resource allocation Optimizing Scheduler, Datacenter Energy-efficient Network-aware Scheduler—RandDENS, BestDENS for datacenters energy consumption on computing resources in Greencloud simulation environment. The simulation results are obtained through energy management by datacenter topology with three-tier high-speed architecture and Dynamic Voltage Frequency Scaling in virtualization.

Keywords Energy efficiency · Task schedulers · Cloud computing
Green Scheduler · Datacenters

Abbreviations

DVFS	Dynamic voltage frequency scaling
HEROS	Heterogeneous energy-efficient resource allocation optimizing scheduler
DENS	Datacenter energy-efficient network-aware scheduler
DPM	Dynamic power management

S. Aarthee (✉) · R. Prabakaran
Department of Information and Communication Engineering, Anna University, BIT Campus, Tiruchirappalli, Tamil Nadu, India
e-mail: aartheerenu@gmail.com

R. Prabakaran
e-mail: hiprabakaran@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_60

1 Introduction

Cloud Computing technology exploits the idea of sharing the computing resources in global cloud space instead of having personal devices without installation of software or local servers for accessing their personal and business files to handle web applications over the Internet. It allows better efficient computing by centralized data storage, data processing, and bandwidth in data communication. There is a general subscription model named pay-as-you-go which is designed mainly for business organizations, which can easily add or remove services and usually will only pay for used services or resources. Figure 1 shows that cloud computing technology is having five essential characteristics for handling the services, four deployment models for accessing the services and three service models which hold the services. Although the components of cloud computing is more efficient than conventional server solutions and it promises on green cloud computing which lies with locating energy consumed datacenters and utilizing renewable energy sources.

Virtualization is associated with the technology of cloud computing which allows numerous virtual machines to be run on a single-host physical server [1]. Earlier to the development of virtualization, each server computes only the dedicated given task or job; it maintained performance and reliability of a dedicated server over resource efficiency and energy efficiency. The virtual machines are inaccessible from one another and it will take full dominance of host physical server

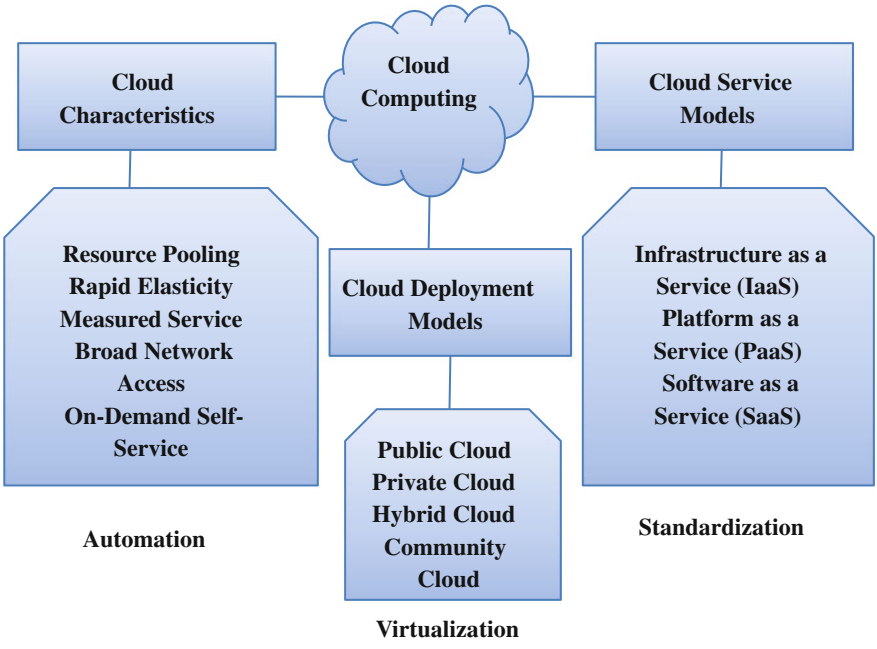


Fig. 1 Components of cloud computing

in computing the resources. If any one of the virtual machine crashes, the other virtual machines will run without any interruption. Every virtual machine is independent to each other. Power is the primary cost associated with operating datacenters which derives power from coal and other renewable sources. Hydroelectric power provides green energy and there comes the concept of Greencloud to maintain the standard computation resources with lower energy consumption. In the direction of a Green Cloud, the cloud computing provides energy-efficient method for addressing the shared resources with lower energy consumption.

2 Energy Efficiency in Datacenters

The most important criteria on utilizing the energy are by interconnection of datacenters and network equipments. The subsidiary energy is wasted as heat energy, usage of air-conditioning systems, and in power distribution system [2]. The Greencloud has three components for energy consumption such as computational energy, communicational energy, and finally the energy related to the physical host infrastructure of a datacenter. Efficiency of datacenter is characterized in relation to the performance delivered per watt. It has been calculated by two metrics that are [3]:

1. Power Usage Effectiveness (PUE)
2. Data Center Infrastructure Efficiency (DCiE)

2.1 Power Usage Effectiveness (PUE) Calculation

It is a measurement of efficient usage of energy in datacenter; specifically, utilizing energy by the computing IT equipment in contradiction to cooling devices. PUE is the ratio of total amount of energy used by a datacenter facility or the effective usage of electrical power to the energy delivered to computing equipment [4].

$$\text{PUE} = \frac{\text{Total Facility Power Load/Energy}}{\text{IT Equipment Power Load/Energy}} \tag{1}$$

- First, Total Facility Power Load is measured at the amount of datacenters used to execute the computing resources which includes the internal components like coolers or chillers, security equipment, Computer Room Air-Conditioning units, Uninterruptible Power Supply, PDUs, lighting and monitoring equipment required to provide services to the IT equipment power load.
- Second, measurement in IT equipment power loads which is determined to carried out after all the switching and conditioning operations.

Equation (1) determines the efficiency of processing datacenter. The lower number is 1, which determines the enhanced efficiency in datacenter. PUE generally ranges from 1 to 3 score value which means of constant energy utilization which does not cause higher carbon emissions, so the quality of life with green environment can be maintained. The reciprocal of PUE expressed is as a percentage is known as the Data Center infrastructure Efficiency and is represented by the Eq. (2),

$$\mathrm{DCiE}(\%) = \frac{1}{\mathrm{PUE}} \tag{2}$$

Both PUE and DCiE describes that the total consumed energy gets distributed to the computing servers. The two main approaches for consuming energy in computing servers are Dynamic Voltage Frequency Scaling and Dynamic Power Management [5]. The DVFS scheme adjusts the power of CPU by performance level according to the existing power load. On converse, the DPM scheme performs power down in computing servers which is an incredible energy-efficient technique. However, if there is a necessity to power up the server, a substantial amount of energy consumption is attained compared to the DVFS scheme [6].

3 Working Principle of Task Schedulers

(a) **Green Scheduler**:

The Green Scheduler consolidates the virtual machines in the cloud environment in which few servers as possible as are used and the unused or idle servers are shut down. The controller in datacenter dynamically analyzes the cloud and turns on servers as needed for computing the resources, turns off idle servers, deploys virtual machines and migrates virtual machines in order to free up servers [7]. The general suggestion is to use as few servers as possible while maintaining the optimum load per server for energy efficiency. An optimum load (ex. 80%) for servers can be defined and the controller will respect this value by always trying to maintain as many virtual machines on a server for fulfilling the 80% server load. For example, on a server with 10 GB memory and 1 GHz CPU, the virtual machines deployed should cumulatively request 0.8% of the CPU and memory (0.8 GHz CPU and 8 GB memory).

(b) **Round Robin Scheduler**:

It is worked by job process and network schedulers in computing servers. Each process is assigned by the time slices in equal fraction called quantum and it executes all the processes in circular order without priority.

(c) **HEROS Scheduler**:

The HEROS methodology allocates tasks to the dedicated server with maximum score. This score is calculated by decision functions such as establishing server selection and the functionality of datacenters communication (potential function for communication).

(d) **Random Scheduler**:

This scheduler uses the random ticket for selecting the next process to get executed. The allocation of tickets is not necessarily to be uniform. The priority of process selection is decided, depends upon the number of tickets granted by the scheduler to that particular process.

(e) **RandDENS and BestDENS**:

It has the modifications of the Datacenter Energy-efficient Network-aware Scheduler (DENS) with random and best-fit server selection options [1].

The round robin scheduler does not have any priority to the tasks and took equal period of time to execute the different type of tasks. In random scheduler, the random tickets are generated and it is not assure of executing all tasks. In HEROS scheduler, the score will differ depending upon the task handled by the datacenter and the score table need to be maintained properly. The RandDENS and BestDENS use the best-fit server selection randomly and it has no such considerations for idle servers. All these limitations can be overcome by Green Scheduler.

4 Results and Discussion

Greencloud simulator [8] is a packet-level simulator for communications between datacenters in energy-aware cloud computing. It offers a comprehensive modeling for energy consumption by the datacenter IT equipment such as computing servers, energy management by hosts initialization, network switches, virtualization and datacenter topology such as topology parameters, network links, and task description. Greencloud helps to provide novel solutions in resource scheduling, monitoring, workload allocation, optimization of communication protocols and network infrastructures. The Greencloud simulator is an extension of NS2, a Network Simulator [9]. Greencloud simulator supports the quality of life for sustainable eco-cloud computing environments. It also offers a thorough examination of workload distributions in executing the tasks by the task schedulers. The energy efficiency in various parameters of task schedulers is to be considered for comparison and to find the best task scheduler for executing the task in the efficient

manner on consuming the server energy. For the purpose of analyzing the results in server energy consumption, the same number of tasks is assigned to datacenters and processed the tasks inside virtual machine with different task schedulers. Energy efficiency in server energy and total energy by datacenter is compared with different task schedulers. The bandwidth in the core and aggregation parts of the network in switches is mainly improved by three-tier high-speed architecture.

The parameters of datacenter topology and energy management with its values are represented in the Table 1. A total task carried by the datacenter is 465,199. Out of which 177,360 tasks executed by the HEROS scheduler are failed by servers. HEROS scheduler cannot able to process the entire tasks; there are few occurrences in tasks failure at its execution. Switch Energy (core), Switch Energy (aggregation), and Switch Energy (access) are equally emitting the energy capacity as 1033.4, 458.5 and 1375.7 Wh by all task schedulers. There is the difference in server energy by task schedulers. The BestDENS task scheduler obtained 3347.3 Wh server energy which is comparatively lesser than the other considered task schedulers but the numbers of tasks failed by servers due to BestDENS scheduler is 209,758. In Green task Scheduler, none of the tasks is failed by the server and it has the server energy of 3784.9 Wh. This server energy value is lesser than Round Robin Scheduler, Random Scheduler and RandDENS Scheduler, in that case all the tasks are executed by the servers and there is no task failure in these servers. The simulation results for various parameters are shown in the Table 2. With these servers energy values in executing with datacenter parameters, it can be easily identified that, the best task scheduler for energy efficiency in datacenters is Green Scheduler. The graphical representation of server's energy consumption and energy summary by Green Scheduler are shown in the Figs. 2 and 3 for clear understanding of energy management.

Table 1 Datacenter topology parameters and network links with its values

Input	
Parameter	Value
Datacenter architecture	Three-Tier high-speed (3Ths)
Switches (core)	2
Switches (aggregation)	4
Switches (access)	256
Servers	1536
task.mips	300,000
task.memory	1,000,000
task.storage	300,000
task.size	8500
task.output size	250,000

Table 2 Result comparison on server energy by different task schedulers

Output Parameters	Scheduler					
	Green	Round Robin	HEROS	Random	Rand DENS	Best DENS
Average load/server	0.3	0.3	0.2	0.3	0.3	0.2
Datacenter load	34.7	34.8	22.5	34.9	34.9	19.1
Total tasks	465,199	465,199	465,199	465,199	465,199	465,199
Average tasks/server	302.9	302.9	302.9	302.9	302.9	302.9
Tasks failed by servers	0	0	177,360	0	0	209,758
Total energy (Wh)	6652.5	6656.1	6308.9	6658.7	6658.6	6214.9
Switch energy (core) (Wh)	1033.4	1033.4	1033.4	1033.4	1033.4	1033.4
Switch energy (agg.) (Wh)	458.5	458.5	458.5	458.5	458.5	458.5
Switch energy (access) (Wh)	1375.7	1375.7	1375.8	1375.7	1375.7	1375.7
Server energy (Wh)	3784.9	3788.5	3441.2	3791.1	3791.0	3347.3

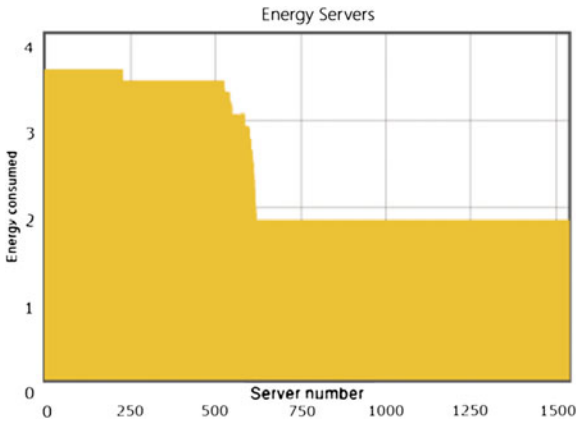


Fig. 2 Energy consumption

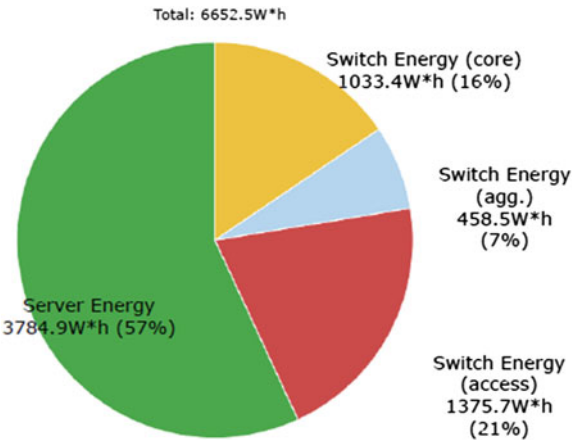


Fig. 3 Energy summary

5 Conclusion

Here, the server's energy utilization in computing the resources with different task schedulers is compared and analyzed the outcome. By the simulation results, it can be clearly virtualized that the BestDENS (combination of energy efficiency and network awareness) methodology of task scheduler consumes the energy in data-center compared to other discussed task schedulers but the major problem is that the few number of task failures by servers are occurred. This drawback can be over-come by Green Scheduler with the energy consumption of 3784.9 Wh without any task failures by the servers compared to Round Robin Scheduler, Random Scheduler and RandDENS Scheduler; in these schedulers there is no tasks failures happened by the servers.

References

1. Kliazovich, D., Bouvry, P., Khan, S.U.: DENS: Datacenter Energy-Efficient Network-Aware Scheduling. Springer, Berlin (2011)
2. Kliazovich, D., Bouvry, P., Khan, S.U.: GreenCloud: A Packet-Level Simulator of Energy-Aware Cloud Computing Data Centers. Springer, Berlin (2010)
3. Rawson, A., Pfleuger, J., Cader, T.: Green grid data center power efficiency metrics: PUE and DCIE. The Green Grid White Paper #6 (2008)
4. Raghavendra, R., Ranganathan, P., Talwar, V., Wang, Z., Zhu, X.: No power struggles: coordinated multi-level power management for the data center. APLOS (2008)
5. Chen, G., He, W., Liu, J., Nath, S., Rigas, L., Xiao, L., Zhao, F.,: Energy-aware server provisioning and load dispatching for connection-intensive internet services. In: USENIX Symposium on Networked Systems Design and Implementation, USENIX Association, USA (2008)

6. Li, B., Li, J., Huai, J., Wo, T., Li, Q., Zhong, L.: EnaCloud: an energy-saving application live placement approach for cloud computing environments. In: IEEE International Conference on Cloud Computing, India (2009)
7. Verma, A., Dasgupta, G., Nayak, T., De, P., Kothari, R.: Server workload analysis for power minimization using consolidation. In: USENIX Annual Technical Conference (2009)
8. Kliazovich, D., Bouvry, P., Khan, S.U.: GreenCloud: a packet-level simulator of energy-aware cloud computing data centers. J. Supercomput. **62**(3), 1263–1283 (2012)
9. The Network Simulator NS2. http://www.isi.edu/nsnam/ns/
10. Berl, A., Gelenbe, E., Di Girolamo, M., Giuliani, G., De Meer, H., Quan Dang, M., Pentikousis, K.: Energy-efficient cloud computing. Comput. J. (2009)

Distributed Energy Generation—Is It the Way of the Future?

Mujahid Tabassum, Saad Bin Abul Kashem and Kuruvilla Mathew

Abstract This research topic consists of the advantages of distributed energy generation, the different methods used to generate the energy (e.g. photovoltaic panel and wind turbine), how to store the energy (e.g. battery) and how it will be achieved. Other topics that are discussed are cost factor and performance of each method. Furthermore, differences between the traditional transmission and distribution grid are compared. Lastly, the implementation of a smart grid is discussed to show that "green power" can provide a significant environmental benefit.

Keywords DEG · Solar · Wind turbines · Smart grid · Power transmission Renewable energy · Sustainable

1 Introduction

Nowadays, with the increasing world population, there is an increasing demand for electrical energy in many countries. With the current delivery system, consumers in certain regions are facing unpredicted blackouts and periodic electricity cuts. In addition, industries in those areas are not getting the consistent high power that they need. The two main causes for this problem are first, due to insufficient capacity of power generation as the system that was designed years back is not able to meet today's world demand. Second, the existing power distribution system has become old and therefore cannot carry the high load of power needed by the population. A remedy to this problem is distributed energy generation (DEG) system. Compared to conventional ways, where power plants are centralised and large unit,

M. Tabassum · S.B.A. Kashem (✉) · K. Mathew
Swinburne University of Technology Sarawak Campus, Kuching, Malaysia
e-mail: skashem@swinburne.edu.my

M. Tabassum
e-mail: mtabassum@swinburne.edu.my

K. Mathew
e-mail: kmathew@swinburne.edu.my

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_61

DEG is the generation of electrical energy, and sometimes also thermal energy, at the point of consumption. This is done by making use of small-scale power generation technologies such as photovoltaic panel and wind turbine. This system also involves the storage of the generated energy, for example, a battery. Lastly, it comprises of an advanced energy distribution system where other devices are synchronised to make the system more reliable and stable. In all, DEG means that houses or single buildings can be entirely self-supporting in terms of electrical and heat energy. While decentralisation of energy production seems to be verbalised by threats like being vulnerable to complicated systems, it can also be observed as "the world of possibilities", regarding power redistribution. This article describes in detail how DEG is indeed the way of the future. First, why a distributed energy system is important will be discussed, followed by the disadvantages of the traditional transmission and distribution system. Finally, the article will concluded that a DEG system is a good choice regarding sustainable development.

2 Why DEG?

The traditional method to power domestic and industrial needs is to use a central power plant, which supplies electricity to the grid in every region where electricity is needed. Usually, the central power plants are either located near to residential areas and industrial zones, or near to the place where the resources are obtained to generate electricity. Examples of the latter are dams or rivers for hydroelectric power plants or docks for transporting heavy loads of coal and heavy fuel oil. Consequently, after generating electricity, the load is supplied to the traditional grid for distribution to the end users. The process of distribution costs a lot depending on the distance of transmission. However, at that time it was economically sensible to do so, as the cost of electricity production was more than transmission cost. This is because the technology was not so advance at that time. Nowadays, there is a different concept about the financial side. In cases where the power plants are far away from the end users, the cost of transmission is costing more than the production of electricity. This is due to the new advanced technologies that are available at the present time [1]. Moreover, it is also noticed that the production efficiency no longer depends on the generation capacity of a power plant. However, it will be more profitable if instead of one big power plant, several smaller power plants are made closer to the regions of demand [2]. The new advanced technology mentioned above involves the use of renewable energies, where the production cost is much cheaper. Renewable source of energy implies free resource such as the sun and wind. This explains the cheaper production costs. What also makes the generation of electricity cheaper is the shorter transmission distance as the power plants are located nearer to sites on demand. With the proper technology and ecological knowledge, by setting up DEG plants at the point of use or close to the point of use will result in low production cost. Concerning transmission, the cost will be reduced to a minimum. Also, the longer the transmission distance, the larger is the power

lost. Lastly, in many countries, the government is encouraging the use of smart meters, which allows two-way communication between the metre and the central system. Using this, the consumer can be paid by the electricity provider for supplying electricity to the grid in case the consumer produces extra electricity (for example, if the consumer has PV installed on his/her house). Ultimately, using renewable resources will cause very little or no damages to our environment [3]. Therefore, as mentioned earlier that the government in many countries is encouraging this system, DEG is becoming an increasingly used technology in many developing and developed countries and is thus becoming the way of the future.

3 Why Not the Old System?

The usual big central power plant requires a large area of land, which previously might be occupied by forests. Therefore, constructing a power plant there means the destruction of the natural habitat of animals living there. In the case of the hydroelectric power plant, damming rivers will destroy the wildlife and other natural resources. Moreover, by having hydropower plants can decrease the level of dissolved oxygen in the water, which can cause harm to the river habitats [4]. The traditional transmission and distribution system is considered to be the weakest link in the whole power grid. The average values of power losses at the different steps are listed below:

- 1–2%: step-up transformer from generator to line of transmission
- 2–4%: resistance in transmission line
- 1–2%: step-down transformer from line of transmission to network distribution
- 4–6%: distribution network to the end users [5]

The total for all the losses sums between 8 and 15%. In numbers, it does not seem to be much, but when put in perspective, that amount of power could be used to supply lots of consumers. Usually, a lot of land is required to construct power plants and they are available in a remote area far from inhabited places. Therefore, the distance between the production of electricity and point of use is very long, which makes the high amount of power loss. (The longer the distance, the higher is the power loss.)

As seen in Fig. 1, derived from the Ref. [6], in the US for the year 2013, coal has the biggest percentage in the type of electricity generation and is the single biggest air polluter there. Burning coal causes lots of problems such as smog and acid rain, which consequently leads to global warming.

These facts, summarises why the old traditional system of electricity production and transmission is not sustainable and therefore needs to be changed to Distributed Energy Generation where environmental damages are kept to a minimum or zero.

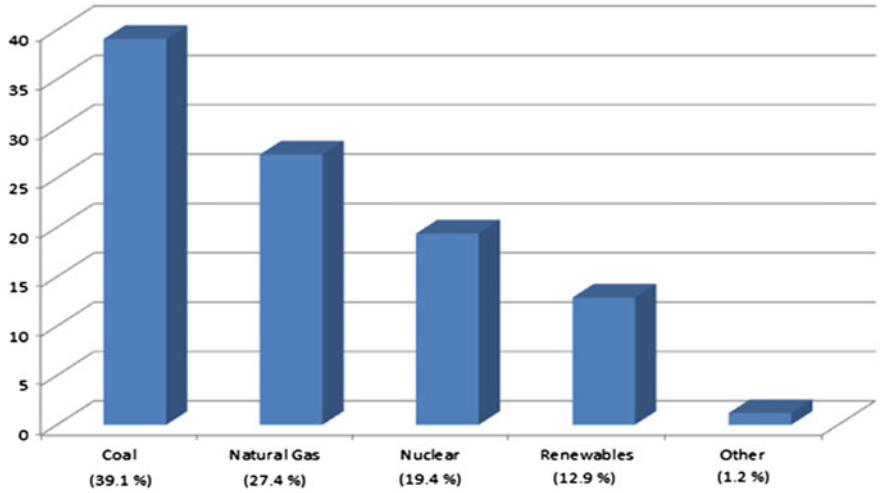


Fig. 1 US 2013 electricity generation by type

4 Approach

In order to prove whether Distributed Energy Generation is the way of the future, an analysis is made to compare consumers' demand criteria to DEG systems' supply criteria. This will make sure that the DEG systems will be able to solve the problems facing by the traditional ways of electricity production and distribution. The average domestic consumption is obtained to estimate the electricity usage of a household.

Table 1 shows that the estimated total peak power in kW for an average home is around 4.652. Please note that in different countries, the power consumption will vary.

5 Types of DEG Resources

Usually, DEG systems are small-scale power generation plants which produce electrical power in a range starting from 1 kW (suitable for home) to 1000 kW (suitable for medium or large industry). As calculated in the previous section, the estimated total peak power is 4.652 kW. Therefore, a 5 kW DEG system will be sufficient to power this house. However, even if the total peak power exceeded the rated DEG system power, and if the house is still connected to the grid, then electricity can be taken from the grid. By making use of smart meters, as mentioned above, during an off-peak time, extra electrical power can be supplied to the grid. Lastly, even though DEG is not restricted in using only renewable resources to

Table 1 Average peak power in a household

Appliances	No. of appliances in the house	Rated power (kW)	Est. total peak power (kW)
Room air conditioner	2	1.1	2.2
Microwave	1	1.5	1.5
Computer/laptop	2	0.12	0.24
Ceiling fan	2	0.1	0.2
LCD TV	1	0.213	0.213
Lights CFL bulb (100 W equivalent)	8	0.03	0.24
Refrigerator	1	0.059	0.059
Total			4.652

generate electricity, in order to make DEG the way of the future, it should make use of renewable energies only so as to become a major solution in the future. Following are some of the renewable energies that are currently in practice in some developed countries.

5.1 Photovoltaic (PV) Panel

Solar power is one of the most commonly used renewable energies. The photovoltaic panel is the device which is used to convert the solar energy into direct current (DC) electricity by making use of semiconducting materials that exhibit the PV effect. In photovoltaic effect, electric current is created by a physical and chemical phenomenon upon exposure to light. Afterwards, a step-up transformer is used to boost up the voltage to 110/240 V, as required according to the country. This happens in the case where the PV power system is connected to the grid. Connecting to the grid is more advantageous for extra electrical power because it can be sent to the grid using smart meters. Usually, the solar panels, which are composed of several solar cells, are placed on the roof of houses for domestic application [7].

The growth of solar photovoltaic is significantly increased and the capacity has reached at least 177 GW worldwide by 2014. Germany produces the largest amount of solar power in the world by contributing more than 7% of its national electricity demands.

In this year, China is expected to take the lead from Germany so as to become the world's largest solar power producer [8]. However, those figures are for solar power generated by power stations. Therefore, to promote Distributed Energy Generation, projects like "The Solar Settlement", a sustainable housing community project in Germany, which is mentioned earlier, should be encouraged by governments of all developed and developing countries. Moving to the economics, some calculations are done based on an average American home.

Using the above data, the area required to set up the system will be 33.45 m^2. The results which are obtained using 'Solar Simplified Calculator' are shown in Tables 2 and 3 [9].

Therefore, if encouraged and helped by the government, this DEG system will indeed change the traditional power generation system and become the way of the future. Also, the biggest benefit of this system is that the sun is a never-ending source of energy and that solar panels have a very long lifespan. Thus, once an individual invests on solar panels, he/she will benefit from it for a lifetime and save lots of money on electricity cost after the payback period.

5.2 Small Wind Turbine

This is a wind turbine, which is used for microgeneration, which is different from the large wind turbines found in wind farms. The turbines are smaller and thus producing less power output.

The size is usually between 2.1 and 7.6 m in diameter and electrical power produced is between 300 and 10,000 W. Some small wind turbines are as light as 16 kg, therefore allowing it to be sensitive to minor wind and has a quick response to wind gusts. To set up a DEG system, it is usually mounted on the top of the house, just like a television antenna. Small wind turbines come both in the traditional horizontal axis and in the vertical axis as well [10]. Medium size wind turbines are suitable to be installed in factories as their required load is bigger.

Depending on the estimated total peak power of a household (e.g. As calculated in Table 1), the appropriate specification of the wind turbine can be chosen as displayed in Table 4.

Even though the required peak power does not meet the standard power rating for a household (in case the consumer set up a very small wind turbine), since the system is connected to the grid, electrical power can be taken from both the grid and the wind turbine. Obviously, the current generated from the wind turbine will pass through an inverter to transform it to alternating current first.

A great advantage of this DEG system compared to solar power DEG is that the wind can be present even at night while the sun is only during the day. Therefore, at off-peak hours electricity can be supplied to the grid by using the smart metre.

By installing smaller, easy to install and easy to maintain wind turbine on rooftops compared to the big one in wind farms, the problem of power transmission loss is eliminated as usual wind farms are located far from residential areas. At the same time, that area of land is saved where the wind farm would be built.

The power produced by the wind energy depends on several factors, as shown in the formula below

Table 2 Solar cost and savings

Cost after all incentives and taxes	$16,100.00
System cost without incentives	$25,000.00
First year savings	$678.99
Average annual savings	$869.93
Saving over 25 years	$21,748.13

Table 3 Financial metrics

Metric	With incentives	Without incentives
Lifetime return on investment	35%	−13%
First year return on investment	4%	3%
Net present value of system	$−4432.20	$−13,332.20

Table 4 Wind turbine size class

Wind turbine size classes						
	Rotor diameter		Swept area		Standard power rating[a]	
	m	~ft	m^2	~ft^2	kW	kW
Micro	0.5–1.25	2–4	0.2–1.2	2–13	0.04	0.25
Mini	1.25–3	4–10	1.2–7.1	13–76	0.25	1.4
House hold	3–10	10–33	7–79	76–845	1.4	1.6
					Typical manufacturer power rating	
Small commercial	10–20	33–66	79–314	640–3400	25	100
Medium commercial	20–50	66–164	314–1963	3400–21,100	100	1000
Large commercial	50–100	164–328	1963–7854	21,100–84,500	1000	3000

[a]Std. power rating for micro, mini, and house hold-size wind turbines = swept area × 200 W/m^2

$$P = 0.5 \cdot \rho \cdot A \cdot C_{\mathrm{p}} \cdot w^3 \cdot \eta_{\mathrm{g}} \cdot \eta_b(\mathrm{W})$$

where ρ is the air density (kg/m^3), A is the rotor swept area (m^2), C_{p} is the coefficient of performance, w is the wind speed (m/s), η_{g} is the generator efficiency and η_b is the gearbox efficiency. The Evans R9000 has been received the UK's Microgeneration Certificate. It is a 3-bladed 5.5 m diameter upwind wind turbine, which comes with a tail fin. So as observed from the graph above, it can produce a maximum constant power of 5 kW when the wind speed is above 13 m/s. Moving on to the cost of this type of DEG, buying and installing a system which is large

enough to power an entire home will cost around $30,000. However, the price has a range between $10,000 and $70,000 depending on the specification. Very small off-grid turbines usually cost $4000 to $9000. Concerning the payback period, it takes around 6–30 years [11]. To promote wind energy DEG systems, the US government has been offering grants of 30% since March 2009 for installing small wind energy systems [11].

5.3 Current Strategies and Future of DEG

At the present time, there are some strategies that are being developed to implement DEG systems efficiently, such as Smart Grid. A smart grid involves the use of Information and Communication Technology (ICT) along with a controller into the electrical transmission and distribution of electrical power to the end user. It is mentioned above that smart meters allow a two-way communication between the metre and the central system. So as to make efficient use of the DEG power and the power from the grid, it is important to have a good management between the demands and supply of power. Therefore, by having a smart grid, imbalances in the supply and demand will be monitored and in case faults are detected, they will be corrected in a real-time 'self-healing' process which will improve the distribution of electrical power. Furthermore, the smart grid will make sure that maximum electrical energy is used for the DEG system. In all, we can say that smart grid increases the reliability of electricity supply and increases the efficiency of the energy infrastructure.

5.4 Comparison and Discussion

As discussed earlier, one of the main disadvantages of the traditional power distribution system is the power loss during transmission. Therefore, the power must be produced at very high voltages and step down to the level the consumer needs it. Every time the voltage level is changed, there are more energy losses, for example in terms of heat. As seen in the picture below, when the electrical power leaves the generation plant, it is transmitted at 400,000 V and by the time that it reaches a household, the voltage has been stepped down at least 4 times to 230 V. Therefore, by having a DEG system, large amount of electrical power is saved.

6 Conclusion

Distributed energy generation, as discussed previously has lots of benefits, can, therefore, help to alleviate lots of critical problems that we are facing concerning the grid such as replacing the thousands of kilometres of new high voltage transmission lines. DEG is a sensible idea in today's world, especially when we know that the fossil fuel is depleting. As a remedy, renewable energies must be used as they are free and will always be available. While there are some factors that encourage economies of scale—e.g. large turbines are more efficient than smaller ones—DEG will be advantageous in many situations. Using DEG systems, electrical power is supplied almost directly to the consumer and the grid become gradually a kind of peer-to-peer power network where a surplus of power is redistributed to areas of energy deficit. Thus, the grid acts more as a load balancer than a 1-way power pipeline from a few huge thermoelectric plants to the mass of consumers.

References

1. US Department of Energy: The Potential Benefits of Distributed Generation and Rate-Related Issues That May Impede Their Expansion. Available at: https://www.ferc.gov/legal/fed-sta/exp-study.pdf (2007). Accessed 5 May 2015
2. Takahashi, K.: Policy Options to Support Distributed Resources. Available at: http://ceep.udel.edu/wp-content/uploads/2013/08/2005_es_policy_options_distributed-resources11.pdf (2005). Accessed 1 May 2015
3. Distributed Energy: Distributed Generation Systems: A New Paradigm for Sustainable Energy (2015)
4. Society, N.: Hydropower Facts, Hydropower Information—National Geographic. National Geographic. Available at: http://environment.nationalgeographic.com/environment/global-warming/hydropower-profile/ (2015). Accessed 13 May 2015
5. Schneider Electric Blog, How big are Power line losses?—Schneider Electric Blog. Available at: https://blog.schneider-electric.com/energy-management-energy-efficiency/2013/03/25/how-big-are-power-line-losses/ (2013). Accessed 13 May 2015
6. Union of Concerned Scientists: Coal generates 44% of our electricity, and is the single biggest air polluter in the U.S. Available at: http://www.ucsusa.org/clean_energy/coalvswind/c01.html#.VVIpUPmqpBc (2015). Accessed 13 May 2015
7. Ellen MacArthur Foundation: Vauban: a pioneering sustainable community in Germany. Available at: http://www.ellenmacarthurfoundation.org/circular-economy/explore-more/initiatives-around-the-world/vauban-a-pioneering-sustainable-community-in-germany (2015). Accessed 5 May 2015
8. Ayre, J., Ayre, J., China's National Energy Administration: 17.8 GW of New Solar PV in 2015 (~20% Increase). CleanTechnica. Available at: https://cleantechnica.com/2015/03/19/chinas-national-energy-administration-17-8-gw-new-solar-pv-2015/ (2015). Accessed 5 May 2015
9. Solarsimplified.org: Solar Investment Calculator. Available at: http://solarsimplified.org/solar-resources/calculate-your-solar-savings (2015). Accessed 5 May 2015

10. Google Books: Wind Energy Basics: Wind turbine Kits and Supplies. Available at: http://www.windgenkits.com/faq.htm (2015). Accessed 4 May 2015
11. Windenergyfoundation.org. Wind Power Your Home. Available at: http://www.windenergyfoundation.org/wind-at-work/wind-consumers/wind-power-your-home (2015). Accessed 2 May 2015

Impact of Distance on the Harmonic Active Power and Energy Metering at the Load

K.S.V. Phani Kumar and S. Venkateshwarlu

Abstract A nonlinear load connected to the system draws non-sinusoidal currents, leading to generation of harmonics of *n*th order. The active power developed by the load, combines with the fundamental active power being consumed by the load and effectively reduces the overall value of active power. When this active power is measured by the energy meter over time, there would be loss to the power distribution company and unplanned power deficiency in the system. The effect of the factors like electrical distance from the source, the type and combination of linear and nonlinear loads is studied in this paper. MATLAB-based simulation is executed on a three-phase system using Thyristor and IGBT-based switches and the results shall be analyzed.

Keywords Harmonic active power (HAP) · Fundamental active power (FAP) Nonlinear load harmonics · Energy meter · Rectifier loads

1 Introduction

The loads in the power system are now the major concern for the distribution companies. Over a decade ago the percentage of nonlinear loads was comparatively less but with the intervention of the electronic equipment into the loads the nonlinearity in the power is hence introduced into the system. Low-Voltage (LV) single-phase nonlinear loads mainly include switched mode power for fans, personal computers, laptops, electronic chokes (with ballast technology), LED bulbs, etc. The single/three-phase Medium Voltage (MV) loads include inverter-based air conditioners, adjustable speed drives (both AC and DC), lighting systems

K.S.V. Phani Kumar (✉) · S. Venkateshwarlu
Electrical and Electronics Engineering Department, CVR College of Engineering, Ibrahimpatnam, Hyderabad, Telangana, India
e-mail: phani5016@gmail.com

S. Venkateshwarlu
e-mail: svip123@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_62

with T12 and high intensity discharge lamps which need ballast of electronic type, arcing and welding devices, etc. This nonlinearity leads to the generation of 'harmonics' which is considered as a pollutant to the quality of power being supplied. The current supplied to these nonlinear loads is not in proportion to the voltage being supplied and distorted from the actual expected sinusoidal wave shape. The harmonic index 'Total Harmonic Distortion' (THD) is the measure of the quality of the waveform for both current and voltage at the Point of Common Coupling (PCC). In literature, [1] has tabulated the effects of domestic and commercial loads indicating the percentage THD, the percentage of the nth harmonic to the fundamental and the True Power Factor (TPF). In [2] the results of the survey done on LV and MV distribution networks is presented with the detailed study of the THD and the specific harmonic that is present in the voltage. Some corrective strategies are also mentioned so as to reduce the effect of harmonics at the PCC. The authors in [3] have particularly focused on the harmonics being injected from a building having many computers. The impact of the current harmonics injected due to the SMPS is studied and the effects on the power distribution system were discussed in detail. The impact of widespread utilization of Compact Fluorescent Lamps (CFL) bulbs was studied in [4]. The results show that depending on the Power Factor (PF) of the lamp used, the harmonics injected in the system is varied proportionally. The authors in paper [5] have studied the harmonic components of domestic appliances like Electronic Fan Regulator, Laptop, Fan Regulator, LCD Projector. The results show the dominance of the current harmonics and the voltage waveform is also distorted significantly because of it. Papers [6–8] show the significance of harmonics generated because of a rectifier-based circuit in the load. The discussion about the various compensation techniques is considered to be beyond the scope of the paper. Section 13 of [9] discusses the examples of large industrial plant at MV level, several users on a single distribution feeder with and without the introduction of the filters in the system. The distance between the source and the harmonic source is taken as a defined value in terms of impedance and the Per-Unit (PU) of the current is found out for the fundamental and nth harmonic in comparison with the IEEE 519 standard values. Annexure A of [10] measures the current and voltage phasor values at the terminals of a nonlinear load drawing a defined active power. The tabulation A-1 shows that the harmonic active power calculated in that case is negative (i.e. power is injected into the PCC).

There is an ambiguity about the power that is measured by the energy meters placed at the load end, as the measured energy is the product of total power consumed in kilo-watt-hour and time. This total power is the summation of the fundamental power that is drawn from the source and also the harmonic power. The IEEE standard 1459-2010 [10] clearly states that the different types of active power as Fundamental Active Power (FAP) denoted by P_1 and the Harmonic Active Power (HAP) or the non-fundamental active power denoted by P_H. For a three-phase or single-phase system the active power measured (P) is mathematically written as in Eq. (1)

$$P = P_1 + P_H \tag{1}$$

The FAP is expressed as

$$P_1 = V_1 I_1 \cos \varnothing_1 \tag{2}$$

The HAP is further defined as

$$P_H = V_0 I_0 + \sum_{h \neq 1}^{n} V_h I_h \cos \varnothing_h \tag{3}$$

where V_0 and I_0 are the direct voltage and the direct current terms, $V_1 \angle \alpha_1$ and $I_1 \angle \beta_1$ are the fundamental components of voltage and current, $V_h \angle \alpha_h$ and $I_h \angle \beta_h$ are the harmonic voltage and harmonic current terms, $\emptyset_h$ corresponds to the angle $(\beta_h - \alpha_h)$, where $h = 2$ to n.

The total active power considered was $P = 4072.716$ W while the fundamental component of the power was 4085.72 W, calculated using Eq. (2). This difference would be accounted to HAP calculated using Eq. (3). Normally the fundamental component of power is the power used to do the useful work. The energy meter would record the total active power and hence the error of 12.96 W goes unrecorded, but consumed. So, for the customer who has a predominantly nonlinear load gets lesser number of electric units billed.

Article [11] highlights the impact of the nonlinear load and also elaborates the impact on the linear loads connected to the feeder. But the influence of the distance from the source was not studied. This paper focuses on the impact of nonlinear load, in terms of the difference between the total active load and the fundamental component of the active load, as the electrical distance between load and the source is changing.

In this paper, the impact of the nonlinear loads on the system is studied as well as impact of change in electrical distance between the source and the loads is analyzed, for the loads having rectifier circuits with thyristor/IGBT as the switching devices, in Sects. 2 and 3 respectively. This analysis helps in planning the placement of the power generation station in the given control area, particularly when there is a microgrid scenario and sensitive loads are connected to the feeders.

2 Impact of a Thyristor-Based Rectifier Connected to the System

A three-phase thyristor-based controlled rectifier is designed to handle a simple resistive heating type a load. To control the power output of rectifier, a six-pulse mode of triggering is employed. The system considered is shown in Fig. 1.

The MATLAB model of it is shown in Fig. 2.

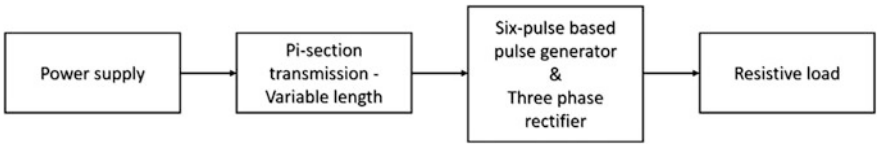


Fig. 1 System's block diagram representation

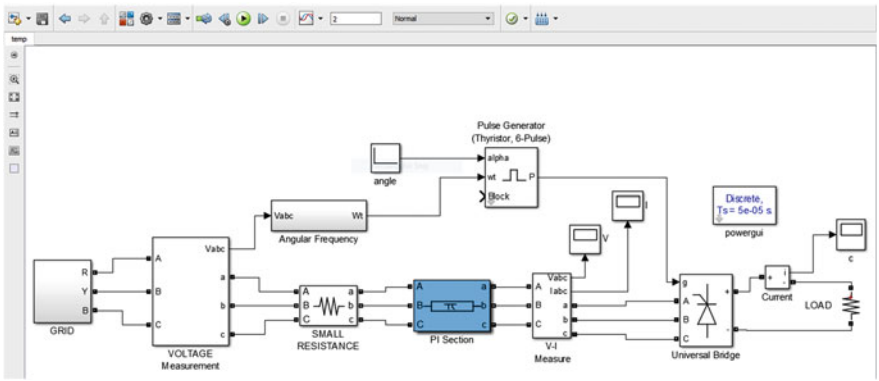


Fig. 2 MATLAB model of the system considered in Fig. 1

The system shown in Fig. 2 shall be analyzed for the following cases:

1. The pi-section transmission length remaining constant at 20 km and the firing angle is varied from 0° to 90° for R load and RL load (motor equivalent).
2. The firing angle is varied from 0° to 90° and the transmission line length is varied from 1025 km.

2.1 Case 1

As the firing angle is varied, the harmonic active power drawn by the load is calculated using Eq. (1) by extracting the harmonic contents of voltage and current waveforms measured during the simulation through Fourier transformation technique. It is observed that 5th and 7th harmonics are predominant and contribute about 95% of the total harmonic active power. The magnitude of current decreases as the angle increases because the conduction is reduced and hence there is a proportional raise in the voltage to maintain the power to the load. Due to the presence of the transmission system, the harmonics in current are now induced into the voltage waveform. A similar kind of a characteristic is observed when a RL load is present in the system. The readings are noted for a triggering phase angle step

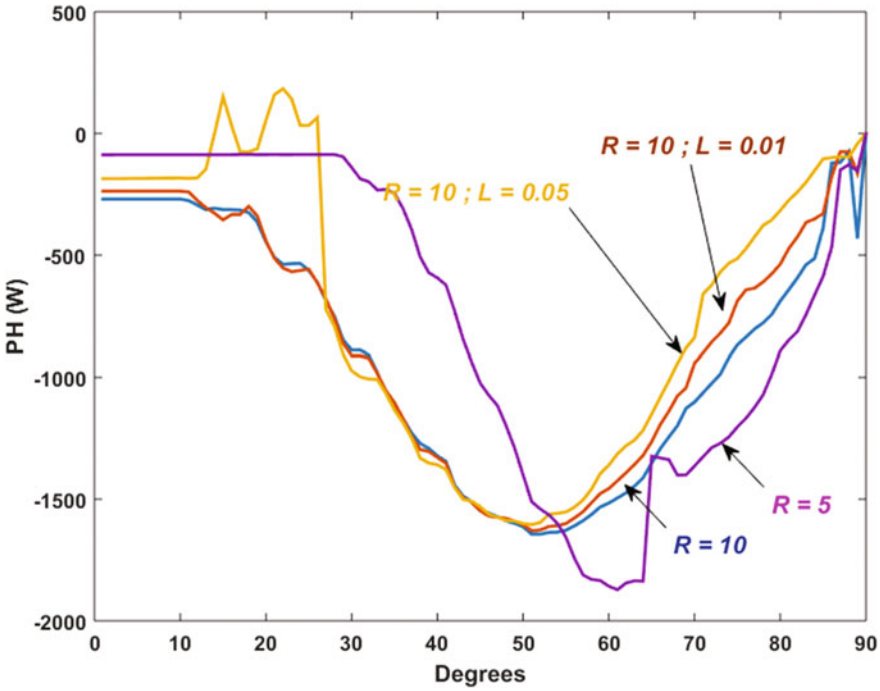


Fig. 3 Variation of HAP for change in load and change in firing pulse phase angle delay

delay of 0.1°. Figure 3 shows the combined results of variation of the firing angle and the load (R and RL). It can be understood that as the load is increasing, the HAP variation is predominant at higher firing angles. The increase in the HAP can be accounted for higher THD contents and until 50° of firing angle variation. The slope of the graph now changes. This is because, the actual power consumed by the load is decreasing and hence the HAP magnitude also decreases.

2.2 Case 2

Similar kind of analysis is done by considering the pi-section length to be changing while the resistance of the load is kept constant at 10 Ω. The results are shown in Fig. 4. It can be observed that closer the load is to the source, more is the HAP.

Consider an example of $R = 10\ \Omega$, pi-section length is 20 km, firing pulse is 40°. The HAP value is −1400 W. So, when there is an energy meter connected at the PCC the total reading for 1 h would be the sum of fundamental power drawn (FAP = 9500 W) and the HAP, which is 8100 W. If the tariff is calculated for 1 h operation of the load, at the rate of ₹5.00 per unit, the total number of units recorded is 8.100 * 5 = ₹40.5/h, while the actual cost is 9.500 * 5 = ₹47.50. A net loss of

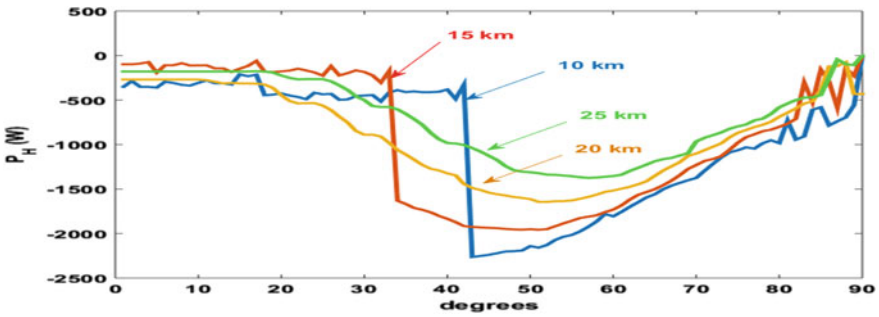


Fig. 4 Variation of HAP for change in transmission line length and constant load (R = 10 Ω)

₹7.00 per hour is encountered by the distribution company because of the existence of nonlinear loads. This loss would reduce proportionally as the distance of the load to the source is increasing. It can be analyzed from the data that operation of the thyristor-based rectifier is desirable for firing angles between 0° and 30°, irrespective of the location of the load from the source.

3 Impact of a IGBT-Based Rectifier Connected to the System

A power system model shown in Fig. 5 is considered and the load subsystem is modelled as shown in Fig. 6.

This system is analyzed for the transmission line length varying from 0 to 20 km. The FAP drawn by the load is calculated and compared to the TAP or called the 'effective' power measured at the terminals of the load, at each step of transmission line length. This is shown in Fig. 7.

The energy meter connected at the load terminals located at 2 km from the source would read the TAP of 104.2 kW while the actual consumed FAP is

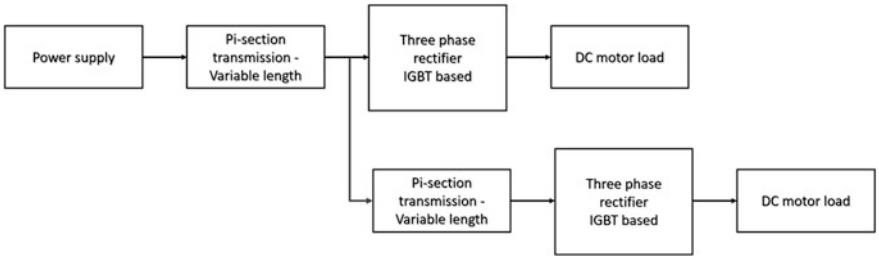


Fig. 5 Block diagram representation of system considered

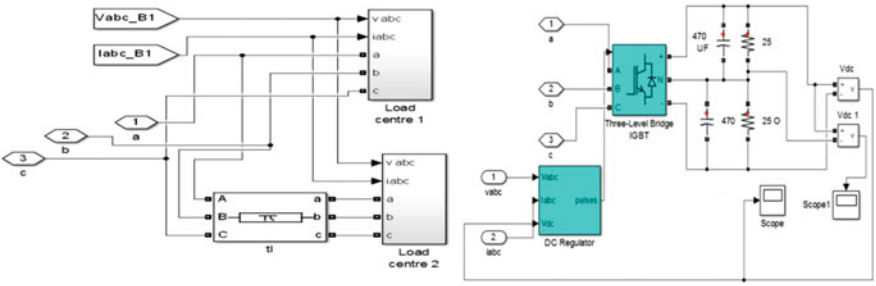


Fig. 6 MATLAB model of the system and the load considered

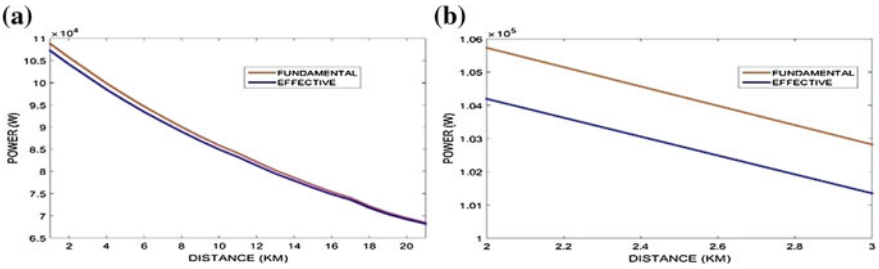


Fig. 7 **a** Variation of fundamental and effective active power as the distance is varying from 0 to 20 km. **b** Zoomed between 2 and 3 km

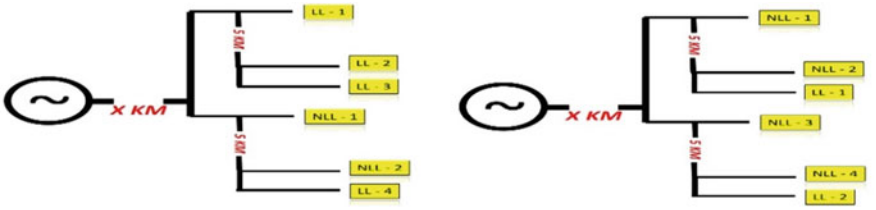


Fig. 8 **a** Two-third number of linear loads with distance '*x*' from source. **b** Two-third number of nonlinear loads with distance '*x*' from source

105.8 kW. Considering the tariff to be ₹5.00/kWh, for an hour, the loss of revenue to the distribution company would be (105.8 − 104.2) * ₹5 * 1 h = ₹8.0/h. It can be observed from Fig. 8a that as distance increases, the loss of revenue would reduce significantly to around ₹0.5/h, as (i) the overall power delivered is reduced and (ii) the difference between the FAP and HAP is reduced.

3.1 *Considering a Combination of Linear and Nonlinear Loads in the System*

A total of six loads are considered to be connected to the system the combination of the loads is considered in the following two ways

1. 4 linear loads, 2 nonlinear loads
2. 2 linear loads, 4 nonlinear loads

The line diagram of the systems considered are shown in Fig. 8a, b.

The actual FAP and the HAP in the two cases are shown in Fig. 9a, b.

For analyzing the error in the calculation of the TAP in both the cases, a sample at 1.7 km is considered. Figure 9 is now zoomed into the respective axes and is shown in Fig. 10. For the two-third linear load case corresponding to Fig. 10a, the loss in the

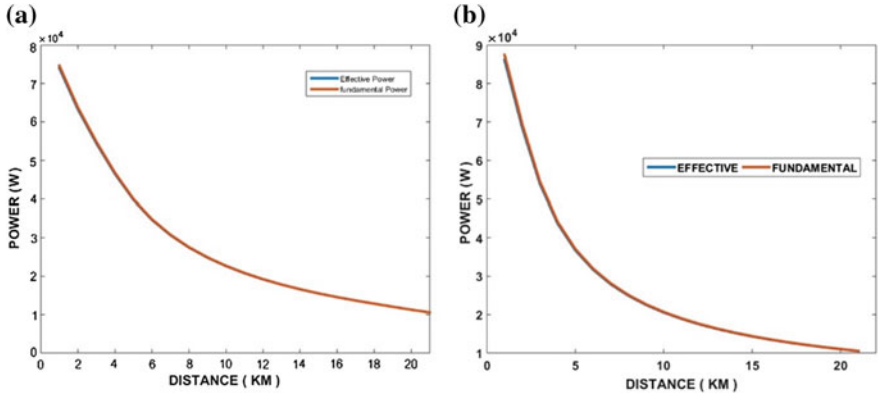


Fig. 9 **a** Variation of HAP for two-third number of linear loads with distance '*x*' from source. **b** Variation of HAP for two-third number of nonlinear loads with distance '*x*' from source

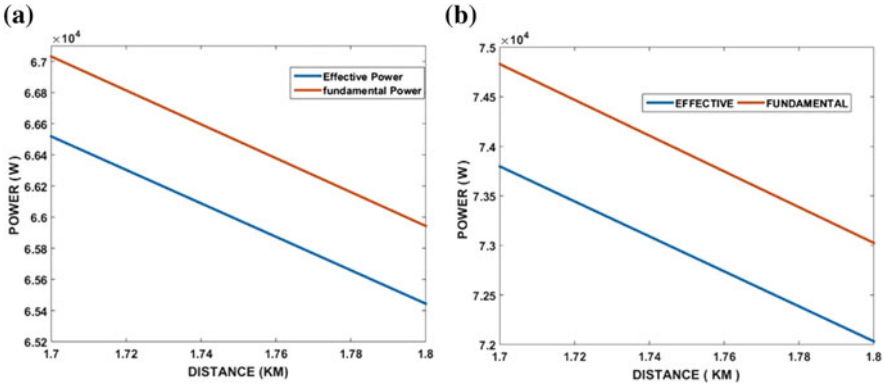


Fig. 10 **a**, **b** are magnified versions of Fig. 9 between 1.7 and 1.8 km of distance

revenue can be calculated using the values (6.705 − 6.6525) * 5 * 1 = ₹2.652/h. For the two-third nonlinear load case corresponding to Fig. 10b, the loss in the revenue can be calculated using the values (7.48214 − 7.378572) * 5 * 1 = ₹5.1784/h.

4 Conclusion

The simulation results for the effect of distance and the type of switch used in a nonlinear load are studied in terms of the load generated harmonic active power and the fundamental active power drawn by the load. It is observed that as the distance of the load from the source is reduced, there is a significant increase in the current drawn and hence the error of the energy meter is increased. This error increases with the concentration of nonlinear load connected to the system. Three-phase rectifier circuits are used as loads and a MATLAB-based simulation is carried out to arrive at the conclusions.

References

1. Priyadharshini, A., Devarajan, N., Uma, R., Anitt, R.: Survey of harmonics in non linear loads. Int. J. Recent Technol. Eng. **1**, 92–97 (2012)
2. Bompard, C.V.E., Carpaneto, E., Napoh, R., Ribaldone, P.: Survey of harmonic distortion in Lv and Mv networks: results and corrective strategies. CIRD **482**, 18–21 (2001)
3. Chan, M.-Y., Lee, K.K., Fung, M.W.: A case study survey of harmonic currents generated from a computer centre in an office building. Archit. Sci. Rev. **50**(3), 274–280 (2007)
4. Sharma, H., Sunderman, W.G., Gaikwad, A.: Harmonic impacts of widespread use of CFL lamps on distribution systems. pp. 1–5 (2011)
5. Bhonsle, D.C.: Harmonic pollution survey and simulation of passive filter using MATLAB. **1** (2), 230–236 (2011)
6. Yildiz, A.B., Unverdi, E.: Simplified harmonic model for full wave diode rectifier circuits. J. Control. Electron. Comput. Commun. **55**(4), 399–404 (2014)
7. Kim, S., Enjeti, P., Rendusara, D., Pitel, I.J.: A new method to improve THD and reduce harmonics generated by a three phase diode rectifier type utility interface. In: Industry Applications Society Annual Meeting, pp. 1071–1077 (1994)
8. Meza, J.C., Samra, A.H.: A new technique to reduce line-current harmonics generated by a three-phase bridge rectifier. In: Southeastcon '98 Proceedings, pp. 354–359 (1998)
9. IEEE, Recommended Practices and Requirements for Harmonic Control in Electrical Power Systems (1993)
10. Ru, D.: IEEE Standard Definitions for the Measurement of Electric Power Quantities Under Sinusoidal, Nonsinusoidal, Balanced, or Unbalanced Conditions, pp. 1459–2010 (2010)
11. Jhalora, S.: Harmonics in power system and metering, pp. 1–3. Secure Meters (2000)

Generation System Reliability Assessment Incorporating Photovoltaic Energy

K. Shivarama Krishna and K. Sathish Kumar

Abstract The reliability assessment of generation system including photovoltaic energy has been described in this article. In general, the reliability analysis of power system can be done at three Hierarchical Levels, but here the reliability analysis of power system is performed at generation level. Therefore the reliability is accomplished at Hierarchical Level-I (HL-I). The intermittent nature of solar irradiance and failure rate of the components have been considered for the development of photovoltaic system. The annual solar data has been considered, in which the generation from the photovoltaic system is made into different states using Fuzzy C-Means clustering method. In addition, the Markov process has been implemented not only to obtain the probability of the photovoltaic model but also its frequency and duration for all the specified states. Finally, the Recursive Algorithm is used to evaluate the indices of the reliability for Roy Billinton Test System including photovoltaic unit.

Keywords Fuzzy C-means · Markov process · Photovoltaic system
Reliability assessment · Recursive algorithm · Reliability indices

1 Introduction

With the deployment of renewable energies like wind, photovoltaic, biomass, tidal and ocean thermal energy, the environmental pollution as well as the carbon-dioxide emissions will decrease to great extent compared to the conventional energy sources. In rural areas, to improve the reliability, renewable energies such as wind and solar energy plays not only dominant role but also they are environmental friendly [1–3].

K. Shivarama Krishna (✉) · K. Sathish Kumar
School of Electrical Engineering, VIT University, Vellore, Tamil Nadu 632014, India
e-mail: shivaram.kvs@gmail.com

K. Sathish Kumar
e-mail: ksathishkumar@vit.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_63

The reliability assessment of power system is very necessary. Generally, the power system consists of generation, transmission and distribution level, the reliability can be performed at individual or combination of the above mentioned three levels. The reliability assessment of a given power system network requires historical data, component failures, outage data and availability of the resources at particular location. The reliability analysis can be done using analytical, simulation and hybrid method [4]. Each of the aforementioned methods has their own advantages and limitations. Depending on the requirement, the power system engineer has to select any one of the above methods for reliability assessment. The authors presented the reliability analysis of power system incorporating large-scale wind farm [5]. The authors described the reliability assessment of power system with wind farm for Brazilian sites [6]. The authors proposed reliability assessment of photovoltaic system which is grid connected and is simulated in fault environment [7]. In the proposed work, the reliability indices were measured using recursive algorithm for RBTS incorporating photovoltaic energy.

2 Photovoltaic Farm Generation

The solar output power is calculated using the following Eq. (1)

$$P_{\mathrm{PV}} = E * A_{\mathrm{S}} * N_{\mathrm{S}} * \eta \tag{1}$$

where,

A_{S} Represents the single module area
E Represents the mean solar irradiation
N_{S} Defines the number of solar modules and
η Defines the efficiency

The PV farm of 20 MW capacity has been developed including the failure percentage of the equipment's and intermittent nature of solar irradiation. The annual hourly solar irradiation is depicted in Fig. 1.

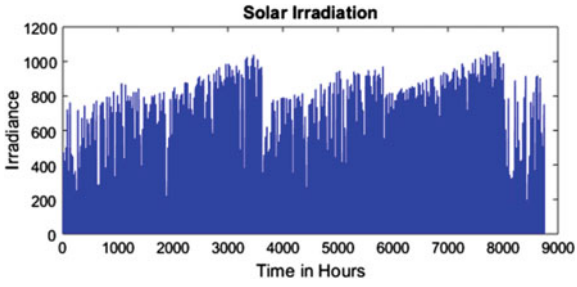


Fig. 1 Annual hourly solar irradiance

Table 1 Repair and failure rate of the components

Components	Repair rate	Failure rate
DC/AC converter	50	0.5
DC/DC converter	219	0.01
Solar panel	219	0.004

The repair rate and failure rate of the photovoltaic components such as converters and solar panels are obtained from the military standard hand book [8] shown in Table 1.

3 Fuzzy C-Means (FCM) Clustering Method

The FCM clustering method has been employed to obtain required number of different clusters, which is described [9] in the below function $J(U, V)$ that is given in the following Eq. (2):

$$J[U, V] = \sum_{i=1}^{M} \sum_{c=1}^{C} [\mu_c[i]]^m \|X_i - X_c\|^2, \tag{2}$$

where,

M Defines number of the data
C Defines the cluster number
V_C Represents cth cluster centre vector
X_i Represents the cluster of ith data vector

The value of m lies in the range of 1 and infinity.

In the proposed work, the output power generated from the photovoltaic system is divided into 15 states using the following Eqs. (3–5).

The membership functions matrix was approximated using Eq. (3)

$$U^{(k)} = \left[\mu_c(i)^{(k)}\right] €R^{C\times N} \tag{3}$$

where 'k' denotes the iterative index and the initial value of k is zero.

The cluster c and the value of its center is calculated using Eq. (4)

$$V_C = \frac{\sum_{i=1}^{M} \left(\left(\mu_c(i)^{(k)}\right)^m X_i\right)}{\sum_{i=1}^{M} \left(\mu_c(i)^{(k)}\right)^m}, \quad 1 \le c \le C \;\; 1 \le i \le M. \tag{4}$$

The value of $\mu_c(i)^{(k)}$ is updated for all X_i, $i = 1, \ldots M$

$$\mu_c(i)^{(k)} = \frac{1}{\sum_{j=1}^{C}\left[\frac{||X_i - V_c||}{||X_i - V_j||}\right]^{\frac{2}{m-1}}}, \tag{5}$$

If the value of $||\mu_c(i)^{(k)} - \mu_c(i)^{(k-1)}|| < \varepsilon$, the process is ended, otherwise the process is repeated from Eq. (4).

4 Markov Models

Markov 4-state model, and its transition among the states is shown in Fig. 2. It is used to find the transition rate, probability of the specified number of generation states [10, 11].

In Fig. 2 markov process for four-state model was depicted, in which P_1, P_2, P_3 and P_4 denote the generation states, whereas $\varnothing_{12}$, $\varnothing_{13}$, $\varnothing_{14}$, $\varnothing_{23}$, $\varnothing_{24}$, and $\varnothing_{34}$ denote the transition between the four states. These values are calculated using the following Eqs. (6–9).

$$\phi_{ij,i\neq j} = \frac{[n_{ij}]}{N_i} \tag{6}$$

where

i Represents the row of the state and
j Represents the column of the state

The number of samples available in the same state is given by Eq. (7)

$$\varnothing_{ii} = 1 - \sum \varnothing_{ij,i\neq j} \tag{7}$$

The probability of each state is measured using the following Eq. (8)

$$\alpha_N . \sum_{j=1, j\neq N}^{N} \{\varnothing_{ij}\} = \sum_{j=1, j\neq N}^{N} \{\alpha_j . \varnothing_{j1}\} \tag{8}$$

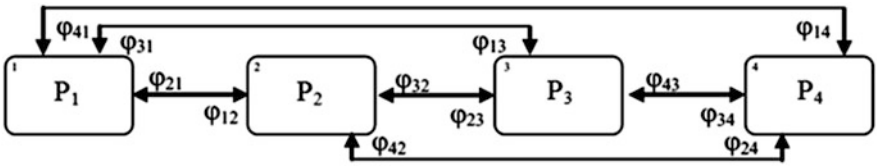


Fig. 2 General markov 4-state model

The summation of the probability of each row is equal to 1 which is given by the below Eq. (9)

$$\sum_{i=1}^{N} \alpha_i = 1 \tag{9}$$

The frequency of each state is calculated using the following Eq. (10)

$$f_i = \alpha_i . \sum_{j=1, j\neq i}^{N} \{\varnothing_{ij}\}, \quad i = 1, \ldots N \tag{10}$$

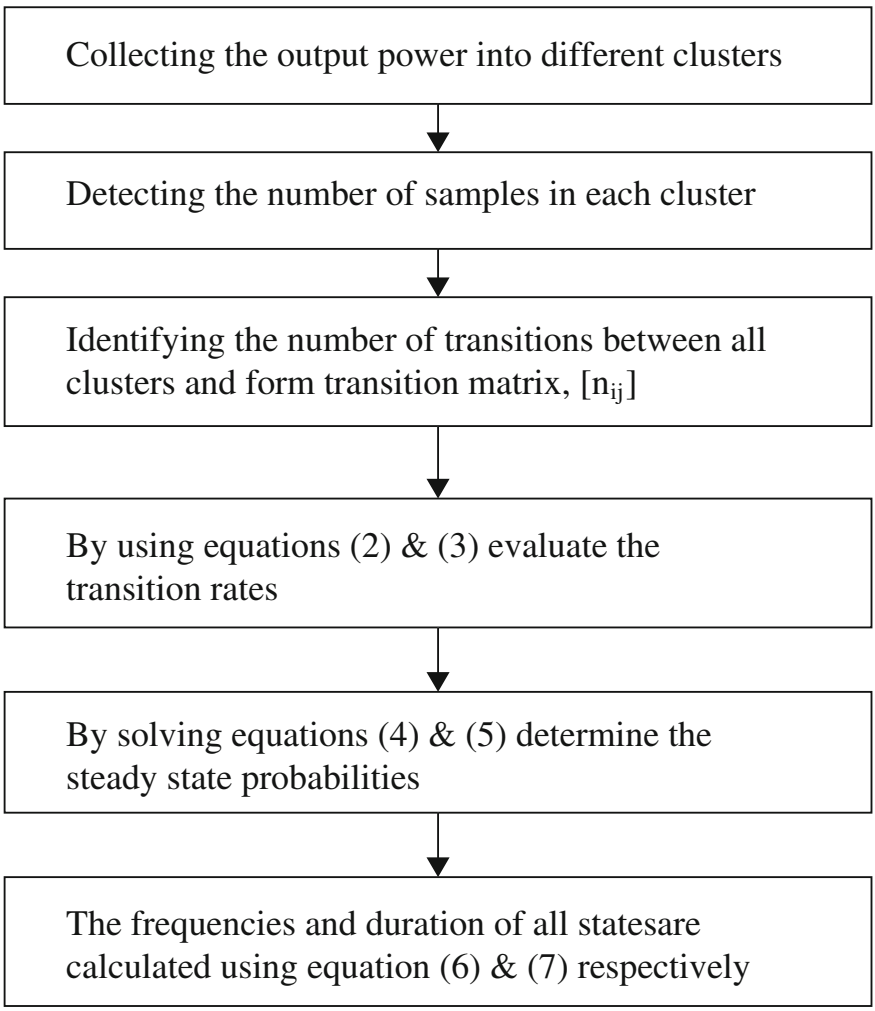


Fig. 3 Flow chart of markov model

Table 2 Probability, frequency and duration of generation state

States	Generation (MW)	Probability	Frequency	Duration
1	0.0057	0.5329	0.0417	12.789
2	1.7095	0.0179	0.0175	1.0261
3	3.5211	0.0159	0.0152	1.0451
4	5.1685	0.0158	0.0152	1.0376
5	7.0268	0.0162	0.0161	1.0071
6	8.5527	0.0142	0.014	1.0081
7	10.1112	0.0215	0.0211	1.0162
8	11.6965	0.0192	0.0187	1.0244
9	13.0754	0.0161	0.0154	1.0444
10	14.2746	0.0164	0.0158	1.0435
11	15.4333	0.0183	0.0175	1.0458
12	16.605	0.0202	0.0193	1.0473
13	17.7785	0.0196	0.0186	1.0552
14	18.8214	0.0184	0.0177	1.0387
15	19.9915	0.2376	0.0387	6.1386

The duration of each state is calculated using the following Eq. (11)

$$d_i = 1/\left[\sum_{j=1, j\neq i}^{N} \{\varnothing_{ij}\}\right], \quad i = 1, \ldots N \tag{11}$$

The flowchart describes the steps to measure the probability and frequency of each state which is shown in the following Fig. 3.

The 15-state PV model has been obtained, the frequency, probability, and duration of these states were displayed in Table 2.

5 Recursive Algorithm and Reliability Assessment

Recursive algorithm is used to calculate the cumulative probability using the following Eqs. (12 and 13). The main advantage of the recursive algorithm is a multi-state model can be added to existing network. The existing network may be generation, transmission, distribution level that can be either individual or combination of these three levels. In addition, the existing network or the test system which has been considered can be multi-state or single state model. In the proposed work, the developed photovoltaic system is added to the RBTS system by including the repair rate and failure percentage of the equipment, reliability indices of the multi-state model were calculated.

Table 3 Reliability indices

Case	LOLE	LOLP
Case I	4.5395	0.01257
Case II	2.7514	0.00621

$$P[Y] = [1 - V]P^1[Y] + [V]P^1[Y - D] \tag{12}$$

$$P[Y] = \sum_{i=1}^{n} P_i P'[Y - D_i] \tag{13}$$

where,

V	Represents the forced outage rate
D	Represents the unit capacity and
$P[Y]$ and $P^1[Y]$	Represent the cumulative probabilities

The Roy Billinton Test System (RBTS) has 11 generating units, in which the generating capacity and load model are 240 and 185 MW respectively [12]. Two cases are taken for reliability analysis.

Case 1: RBTS
Case 2: RBTS with 20 MW PV farm

The recursive algorithm which is used to calculate the reliability indices such as Loss of Load Expectation and Loss of Load Probability for the above two cases are shown in Table 3.

6 Conclusion

The proposed work reduces the Loss of Load Probability and Loss of Load Expectation with the help of recursive algorithm. Multi-state photovoltaic model is added to the RBTS and the reliability indices have been measured using recursive algorithm. The output power generated from the photovoltaic system is divided into specified number of states using Fuzzy C-Means clustering method. Markov process is implemented which not only calculates the frequency, probability and duration of the photovoltaic farm but also reduces the computation time. The reliability indices of the RBTS and the RBTS with photovoltaic system have been measured. The key advantage of this work is adding the photovoltaic system to the RBTS for improving the reliability. The achieved results prove that adding PV farm to the RBTS increases the reliability of the system.

References

1. Paliwal, P., Patidar, N.P., Nema, R.K.: Planning of grid integrated distributed generators: a review of technology, objectives and techniques. Renew. Sustain. Energy Rev. **40**, 557–570 (2014)
2. Krishna, K.S., Kumar, K.S.: A review on hybrid renewable energy systems. Renew. Sustain. Energy Rev. **52**, 907–916 (2014)
3. Krishna, K.S., Kumar, K.S., Edward, J.B., Balachandar, M: Design and analysis of grid connected Wind/PV hybrid system. In: Proceedings of the International Congress on Information and Communication Technology, Springer, Singapore, pp. 555–566 (2016)
4. Zhou, P., Jin, R.Y., Fan, L.W.: Reliability and economic evaluation of power system with renewables: a review. Renew. Sustain. Energy Rev. **58**, 537–547 (2016)
5. Zhang, S., Li, G., Zhou, M: Adequacy evaluation of wind farm integration in power generation and transmission systems. In: International Conference on Sustainable Power Generation and Supply, IEEE, pp. 1–7 (2009)
6. Leite, A.P., Borges, C.L., Falcao, D.M.: Probabilistic wind farms generation model for reliability studies applied to brazilian sites. IEEE Trans. Power Syst. **21**(4), 1493–1501 (2006)
7. Cai, B., Liu, Y., Ma, Y., Huang, L., Liu, Z.: A framework for the reliability evaluation of grid-connected photovoltaic systems in the presence of intermittent faults. Energy **93**, 1308–1320 (2015)
8. United States of America: Department of Defense: Military Handbook: Reliability Prediction of Electronic Equipment: MIL-HDBK-217F. Department of defense (1991)
9. Bezdek, J.C., Ehrlich, R., Full, W.: FCM: The fuzzy c-means clustering algorithm. Comput. Geosci. **10**(2–3), 191–203 (1984)
10. Manco, T., Testa, A.: A markovian approach to model power availability of a wind turbine. In: Power Tech, IEEE Lausanne, pp. 1256–1261 (2007)
11. Shamshad, A., Bawadi, M.A., Hussin, W.W., Majid, T.A., Sanusi, S.A.M.: First and second order markov chain models for synthetic generation of wind speed time series. Energy **30**(5), 693–708 (2005)
12. Billinton, R., Kumar, S., Chowdhury, N., Chu, K., Debnath, K., Goel, L., Oteng-Adjei, J.: A reliability test system for educational purposes-basic data. IEEE Trans. Power Syst. **4**(3), 1238–1244 (1989)

Design Study for a 5 GW Base Load Power Drawn from Satellite Solar Power Station

Deepak Kumar and Kalpana Chaudhary

Abstract In this work, satellite solar power station as base load plant model estimated analysis has performed. SSPS base load power plant for 5 GW model has investigated, and its feasibility prospects are studied. The SSPS essential components sizes have estimated for 5 GW power productions on the ground. A microwave power transmission with high beam efficiency approach is adopted in this work and beam energy effect on transmitting antenna size has examined.

Keywords Microwave · Power · Antenna · Rectenna · Satellite solar power station

1 Introduction

There is imperativeness crisis around the globe [1]. The possibility augmentation in the quantities of tenants in developing countries like "India" requires an exponential addition in the usage of essentialness, sustenance, resources. This way the condition in developing countries is falling apart due to nonappearance of essentialness resources. In India, power plants for the most part in perspective of conventional resources which give 80% of the total fundamental essentialness supply. This kind of electrical imperativeness transform technique has overall issues like an unsafe environment harming, physiological change and a quick decrease of fossil storehouse [2]. With time, India is gaining industrialized and computerized, so more electrical power need than other essentialness outlines.

We are scanning for ecologically well-disposed power imperativeness headways which do not release carbon dioxide into the air, or they are renewable. Natural

D. Kumar (✉) · K. Chaudhary
Department of Electrical Engineering, Indian Institute of Technology (BHU) Varanasi, Varanasi 221005, India
e-mail: Deepak.rs.eee14@iitbhu.ac.in

K. Chaudhary
e-mail: kchaudhary.eee@iitbhu.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_64

Sun-based imperativeness; hydropower essentialness, wind imperativeness, and other renewable essentialness are reliable essentialness source [1, 2]. The Sun-based imperativeness is flawless essentialness. Sun-based imperativeness falling on the Earth each hour is adequate to give world essentialness yearly demand. Consequently, research is in advance of the time for growing modifies capability from natural Sun obtainable enlightenment and heat to electrical power [1–5]. There are moreover price related, and site condition issues in commercializing Sun influenced energy plants. Sun accessible radiance reduces while coming to the Earth. It cripples on shady or stormy days furthermore daylight is missing at evening time [2].

2 Overview of SSPS

In a satellite solar power station, space satellite collects Sun irradiance and photovoltaic transform it into electrical energy [1]. This electrical power changes into the microwave and transmitting that microwave power remotely to receiving antenna on the Earth. The receiving antenna associated rectifiers turn over microwave power back to electrical power [4]. This way, the space energy is available on the earth to supply in the commercial grid after appropriate dispensation [1–3]. Consequently, it is apposite to supplant routine wellsprings of imperativeness. In many aspects, SSPS rides over terrestrial Sun situated power due to unobstructed and undistorted daylight irradiance available in space. On the Earth-based solar framework, the SSPS has added three-cover increases in power accessibility. Regardless, SSPS has some development troubles and major cost-related issues to execute [3].

2.1 SSPS as a Base Load Power

There is an essential of the base load power plant as shown in Fig. 1, for the developing imperativeness sustainability [2]. Natural daylight-based power is brilliant for unpredictable power use, yet it is not sensible for base load power. On another side, the upside of SSPS is it can be utilized for base load demand. There is a necessity of large size rectenna on the Earth to gain power from space. The rectenna mounted ground is free for agriculture and diverse purposes [1].

SSPS Power cost could be viable or less costly than other essentialness sources. With the advancement to lessen the satellite dispatch cost and supplementary technology improvements, SSPS is feasible in coming future. An inventive advance in radio wave innovation is going on around the world in this direction [1, 2].

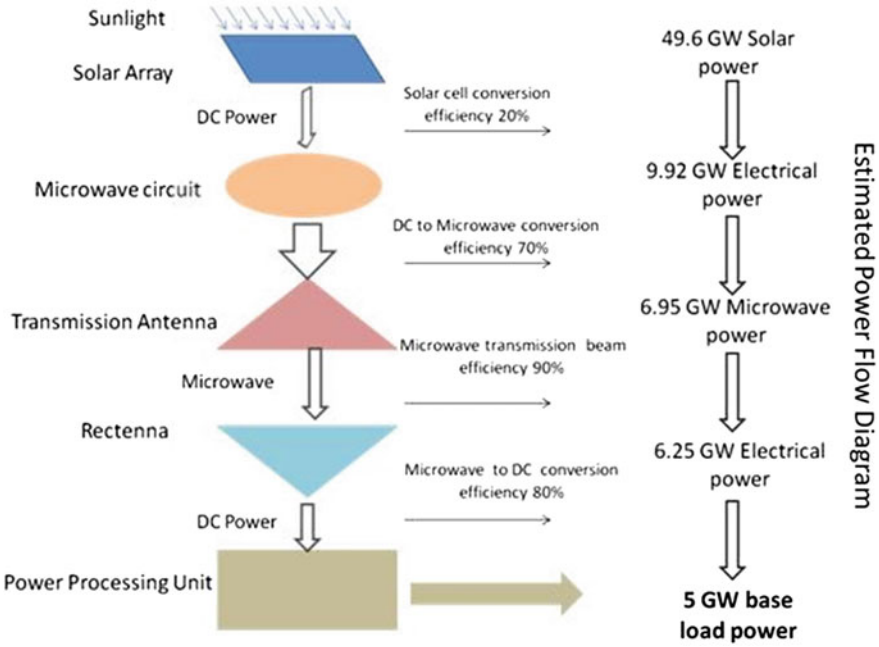


Fig. 1 A 5 GW SSPS base load plant model [1]

3 History of SSPS

SSPS advancement is in the creating stage. Diverse space workplaces are looking at and reported SSPS as a sustainable imperativeness source. In any case, there are various mechanical challenges and preservationist issues in SSPS application. The deep research was performed by NASA-DOE in the USA and gave reference model of SSPS [2]. In spite of the way that in 1997, the Fresh-Look-SSPS thought was a change in SSPS reference design. It gave "Sun Tower," SSPS to have a couple of innovative approaches for managing to diminish SSPS operation and life cycle cost. In 2001, Japanese aeronautics examination association (JAXA) demonstrated 5.8 GHz 5 GW SSPS model using microwave development [6]. The preferred frequency 5.8 GHz is noticeable all around decreasing system dimension. The SSPS application in base load and non-base load power plant, a relative study, and examination were performed by "European space investigates office" in 2005. The study examined SSPS and land-based Sun arranged thermal with hydrogen stockpiling. It completes up, for far-reaching size (more than 5 GW), SSPS is conceivable and cost-related identical with land-based influence plant [5, 6].

4 SSPS Microwave Power Transmission Effects on the Atmosphere and Space

For the considered SSPS base load plant, the microwave transmission impacts in the space and environment must study. The microwave Power disaster on account of normal climatic ingestion over the partition from a geostationary hover to the ground is thought to be underneath 2% [7]. Along these lines, it is an insignificant condition in an air space if microwave arrangement prosperity and security purpose of repression is associated. At lower frequencies diminishing is more progressive in the atmosphere and at higher frequency ionosphere correspondence is more effectual. Radio waves are experiencing ionosphere diminished due to digestion as shown in Fig. 2. This wonder is called ohmic warming [7]. In subordinate level ionosphere, the higher electron density is accessible making more ohmic warming. Unfortunately, electron warming estimation on account of high power microwaves is not available in the written work, and merely speculative results had been presented. High-power microwave in space causes plasma waves. The reason behind plasma wave period is through full participation. Plasma Precariousness creates discretionary EM waves; these assistant waves support have electron warming effect and electron density irregularity [7, 8].

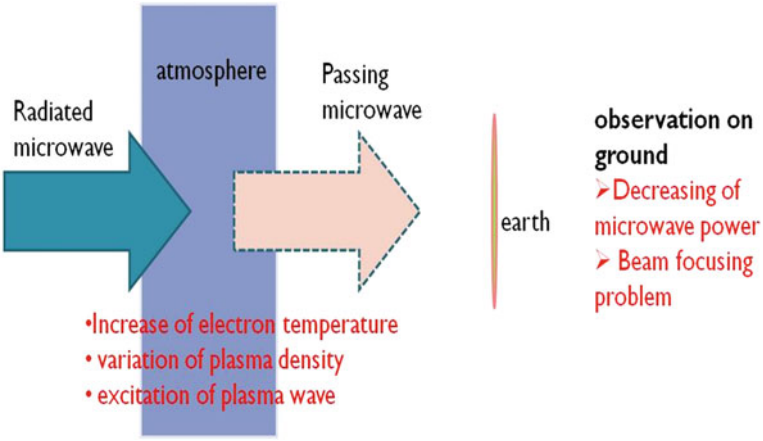


Fig. 2 Microwave transmission impact in space [8]

5 Estimation of 5 GW SSPS Base Plant Model

The consideration of SSPS 5 GW base load power has established in this work. In this condition, 5 GW of electrical imperativeness is offered on earth is acknowledged. There is ground rectenna yield electrical power; consider rectenna efficiency 80%. Therefore, 6.25 GW of microwave power is required on the ground rectenna site to convey this much electrical yield. The microwave compels of 6.25 GW on the ground transmitted from space satellite transmitting antenna. Assuming beam capability of 87%, the required microwave power at transmitting antenna is 6.95 GW. In space satellite, there is DC to microwave change units are available to change over DC power into the microwave. In this manner, required DC power is 9.92 GW for DC to microwave change efficiency 70%. Photovoltaic are used to change over Sun-based imperativeness into DC power in space. Photovoltaic have Sun situated essentialness to DC power transform adequacy of 20%. Therefore, 49.6 GW of Sun arranged imperativeness required at the space end. In this work, we consider 5 SSPS module of 1 GW power that collectively provides, 5 GW of electrical essentialness available on the earth.

5.1 SSPS Size Estimation

The photovoltaic array size required making 10 GW DC power yield is around 50 km^2 (5 km × 10 km). There is an unsavory estimation of photovoltaic array size need. To establish rectenna measurement, we have to consider microwave power density existing on the rectenna site. There is a microwave power density limit for human prosperity and security. The microwave presentation security limit picked by agencies is 10 mW/cm^2 [7].

Considering normal microwave power flux density at rectenna = 100 W/m^2 for 1 GW unit.

$$100\,\mathrm{W/m^2} \times \text{Rectenna area} = 1.25\,\mathrm{GW}$$

Therefore, rectenna diameter = 4 km (approximate size). However, we require 6 km diameter around considering Gaussian distribution.

5.2 Microwave Power Transmission

This work is to consider the transmission of 1.44 GW of microwave vitality from geostationary circle to the Earth for 1 GW base load control. The separation in between is 36,000 km.

Friis transmission equation [9]

$$\frac{P_r}{P_t} = G_t G_r \left(\frac{\lambda}{4\pi D}\right)^2 \tag{1}$$

where G_t, G_r are the antenna gains, λ is the wavelength, and D is the distance between the antennas [9].

For microwave power transmission, Friis condition has commonly used. While applying the above Friis transmission condition, to send 5 GW microwave power from Geo partition to the Earth. The found out microwave power got on the earth surface is low 1.5 MW. In fact, notwithstanding for this circumstance, we consider high gain and directivity of transmitting and receiving antenna. For this situation to assemble 5 GW microwave power, the rectenna measure essential is 1000 km. The above situation is not reliable in a veritable case. Along these lines here we made a conclusion; The Friis transmission condition is not reliable for the circumstance [9–11]. Besides, it is merely applicable to the far field condition.

Transformed Friis transmission condition in near field condition [10]

$$\frac{P_r}{P_t} = \frac{A_t A_r}{\lambda^2 D^2} = \tau^2 \tag{2}$$

In the transformed transmission equation, one can look at getting power is greater than the broadcasting power for $\tau > 1$. These unfeasible conditions raise in light of the way that $D < 2d_t^2/\lambda$, this is the nearby field or Fresnel zone condition. In the nearby field condition

Beam Efficiency [10]

$$\eta = 1 - e^{-\tau^2} \tag{3}$$

For this circumstance, the beam profitability is varying in the range 80–90%; in this way, the estimation of τ gets the opportunity to be more than one [10].

$$\tau = \frac{\sqrt{A_t A_r}}{\lambda D} \tag{4}$$

6 Results and Discussion

In SSPS, transmit power from geo to the Earth; near field condition is kept up. Since in the near field condition, the transmitting antenna estimate relies on upon the frequency utilized. Concerning the higher frequency, the transmitting antenna dimension prerequisite declines. Hence, acknowledgment of higher frequency power transmission SSPS is financially beneficial, notwithstanding, there

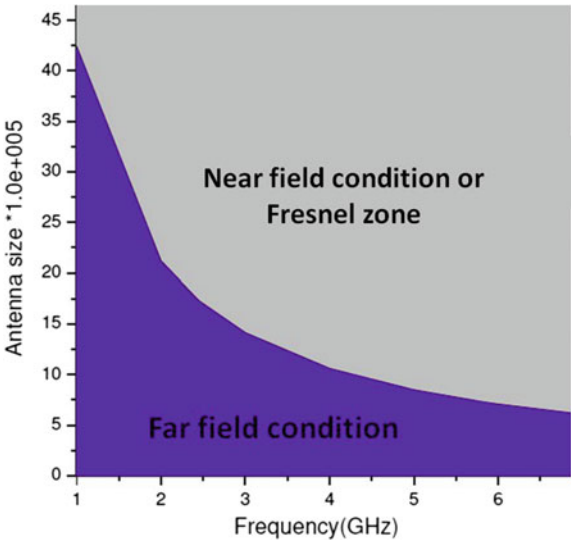


Fig. 3 Antenna size variation with frequency and near field region

are certain points of confinement in a practical situation [8]. In this way, frequency 2.45 and 5.8 are a predominant choice. Figure 3 illustrates near field operation region with frequency.

The microwave beam effectiveness is a significant feature in power transmission. For the state of exchange given power, the beam productivity, the receiving antenna estimate, the separation between and frequency will choose the transmitting antenna measure necessity [9]. In this work, one SSPS unit of 1 GW has considered and the rectenna effective area calculated values is 1×10^7 m^2. The transmitting antenna estimates deviation with the beam proficiency appears in Fig. 4. Figure 4

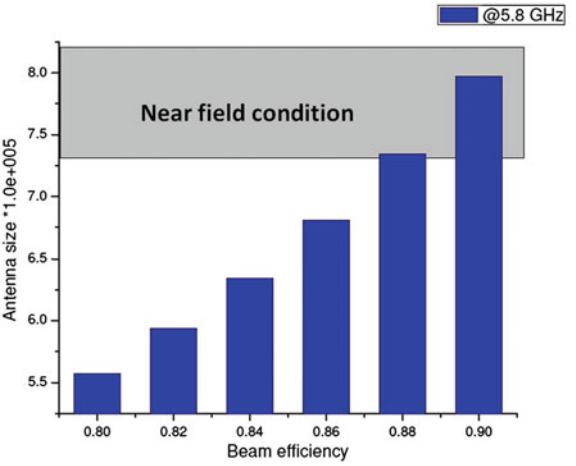


Fig. 4 Antenna size variation with beam efficiency

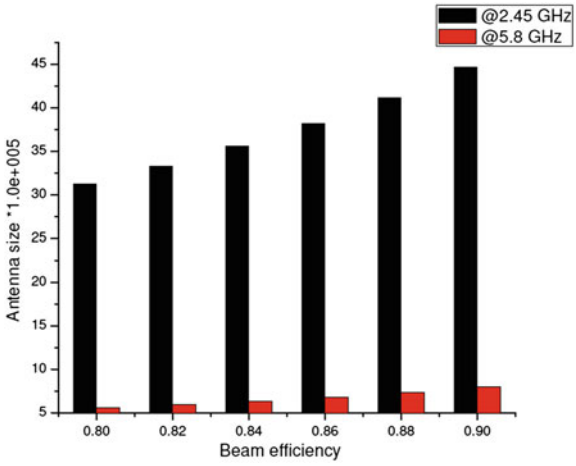


Fig. 5 Antenna size at 2.45 and 5.8 GHz

demonstrates the worthy esteem for transmitting reception apparatus measure that falls in the near field region. A comparison result for frequency 2.45 and 5.8 GHz appears in Fig. 5.

7 Conclusion

In this work, satellite solar power station as base load plant evaluated investigation has performed. For the ground section, the rectenna evaluated measure kept more than computed estimate considering Gaussian distribution. Space fragment photovoltaic size evaluated for continuous power supply of 5 GW on the ground. A microwave power transmission with high beam effectiveness approach embraced in this work and diverse ways conferred. The beam productivity is the critical parameter for choosing transmitting antenna measure. The regularly utilized Friis transmission condition for remote power transmission is not any more legitimate in this work as it lies in near field condition. For near field condition; transmitting antenna measure estimation utilizing reformed friis transmission condition gives exact results. The frequency 2.45 and 5.8, which is in the environmental window, is broadly decided for examination investigation. Along these lines, it has observed that 5.8 GHz frequency has cost-benefit more than 2.45 GHz in satellite solar power station.

References

1. Brown, W.C.: Satellite power stations, a new source of energy. IEEE Spectrum **10**(3), 38–47 (1973)
2. Brown, W.C.: The history of power transmission by radio waves. IEEE Transactions on Microwave Theory and Techniques, MTT-32, pp. 1230–1242 (1984)
3. Bodson, B.: COTA system transmits power wirelessly at up to 30 feet, Gizmag, 29 Sept 2013
4. Rappaport, T.S.: Wireless Communications: Principles and Practice (Chap. 4), 2nd edn. Prentice-Hall, Upper Saddle River (2002)
5. Varshney, L.R.: Transporting information and energy simultaneously. In: Proceedings of IEEE ISIT'08, Toronto, Canada, pp. 1612–1616 (2008)
6. Shoki, H.: Issues and initiatives for practical deployment of wireless power transfer technologies in Japan. Proc. IEEE **101**(6), 1312–1320 (2013)
7. Brown, W.C.: Beamed microwave power transmission and its application to space. IEEE Trans. Microwave Theory Tech. **40**(6), 1239–1250 (1992)
8. Shinohara, N.: Wireless Power Transfer via Radio waves, ISTE/Wiley (2014)
9. Friis, H.T.: A note on a simple transmission formula. Proc. IRE **34**, 254–256 (1946)
10. Hogg, D.: Fun with the Friis transmission equation. IEEE Antennas Propag. Mag. **35**, 33–35 (1993)
11. Ju, H., Zhang, R.: Throughput maximization in wireless powered communication networks. IEEE Trans. Comm. **13**(1), 418–428 (2014)

Reduction of Fault Detection Time by Using Fast S-Transform (FST)

P. Mahalakshmi, Ritwik Dhawan, Archit Srivastava and A. Sharmila

Abstract The target of this paper is to diminish the computational time of separation handing-off of transmission line utilizing Fast S-transform (FST). Separate transferring may require a quicker and more accurate estimation of the phasor of the fault current and voltage signals, which are utilized to register clear hindrance for creating the stumbling signal in case when a fault occurs. Customary S-transform is reversible time–frequency unearthly limitation procedure that integrates the components of wavelet and brief time Fourier transformation. The working (handling) time of traditional S-transform is large and in this manner, not appropriate for applications like advanced assurance of transmission lines. FST decreases the computational weight by using down examining. So FST can unquestionably supplant the current DFT construct calculation for with respect to line computerized separate handing-off undertaking in expansive power transmission organizing.

Keywords Fast S-transform · Transmission lines · Conventional S-transform Phasor · Apparent impedance · Distance relaying

1 Introduction

The S-transform has a few zones of uses including therapeutic imaging, for example, directing inconsistencies in the heart, and distinguishing variations from the norm in mind tumors, and in addition identifying aggravations in power

P. Mahalakshmi · R. Dhawan · A. Srivastava · A. Sharmila (✉)
School of Electrical Engineering, VIT University, Vellore, Tamil Nadu, India
e-mail: asharmila@vit.ac.in

P. Mahalakshmi
e-mail: pmahalakshmi@vit.ac.in

R. Dhawan
e-mail: ritwik.professionalid@gmail.com

A. Srivastava
e-mail: a.srivastava2014@vit.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_65

systems, watching wind designs, recognizing gravitational waves, and checking sound and acoustic examples [1]. The S-transform is a recurrence change that is utilized to examine the recurrence substance of nonstationary signs. By utilizing a dynamic recurrence determination indistinguishable to the wavelet transform, it enhances the execution of the short-time Fourier transform. Dissimilar to the wavelet, in any case, the S-transform keeps up an unmistakable relationship to the Fourier range. Quick S-transform calculation was designed in 2010. It diminishes the computational time and assets by no less than four requests of size. Most vital issue in the computerized handing-off is to extricate the major recurrence flag, rapidly and precisely [2]. The blame flag is typically mixed of principal recurrence part, music, and a rotting dc segment. The goal of the advanced channels is to extricate just the basic recurrence by sifting all other undesirable signs. The time consistent and extended rotting DC are obscure and connected with the fault resistance, fault position, and the fault occurrence time [3]. The most well-known estimation of phasor calculations are the full-and half-cycle DFT-based calculations. It is notable that full-cycle DFT channels have preferable recurrence reactions over half-cycle DFT channels, in light of the fact that the principal takes out all music, though the last do not take out even music [4].

2 Materials and Methods

Quick S-transform-based separation transferring in transmission line was used to build up a quick and successful handing-off calculation for ensuring transmission lines utilizing FST. FST is utilized for estimation of phasor (extent and stage), which is proficiently contrasted with routine S-Transform. Further, evident impedance is registered utilizing individual voltage and current phasor for stumbling choice. The created separate transferring calculation is tried for various blame conditions with expansive varieties in working conditions and, observed to be exact and solid in basic leadership inside one cycle from the blame commencement. By stifling the rotting DC segment for computerized defensive transfers displays another versatile phasor estimation calculation for advanced defensive relaying. The calculation is totally safe to an exponentially rotting dc part paying little mind to its underlying extent and time consistent. The calculation is basically planned for current flags and enhances greatness of impedance estimations. The new method depends on the recursive full-period Fourier channel with a different versatile capacity which permits intensive dismissal of the dc flag segment [5]. The introduced calculation performs superior to known measuring methods including the computerized imitate sifting comprehensively utilized as a part of today's transfers. We are presenting here the s-Charm DF method, for estimating selected harmonics in noisy fault signals. A detailed study has been carried out on the behaviour of the proposed algorithm to guarantee its stability and accuracy in the case of noisy signals.

2.1 S-Transform

The traditional S-transform [4] is defined as:

$$S(\tau,f) = \int_{-\infty}^{+\infty} x(t).w(t-\tau,\zeta).e^{-i2\pi ft}$$

The above equation is using the continuous in time signal to compute the transform, but in FST it uses the discrete in time signal. So, the number of points to be transformed are reduced there by computational time is reduced. To convert the continuous signal to discrete signal we have to use a window with a sampling time T. For more accuracy the T has to be increased but increase in T leads to increase in cost of the hardware. So, optimal T has to be chosen.

To understand the S-change, the window work must fulfill:

$$\int_{-\infty}^{+\infty} w(t-\tau,\zeta)d\tau = 1.$$

The conventional S-transform has following discrete version:

$$S\left(jT,\frac{n}{NT}\right) = \sum_{k=0}^{N-1} x(kT)w(kT,\zeta)\exp^{-(i2\pi nk/N)}$$

Whereas and $f = n/NT$ and $x\ (kT)$, k [0, 1, … N − 1] is the series of discrete time having a sampling interval of 'T'.

For higher frequencies, the window width diminishes bringing down the recurrence determination and for lower frequencies the same window width becomes quite high and along these lines, bringing down the time determination. Accordingly, the uniform examining does not mirror the adjustment in determination.

2.2 Fast S-Transform Algorithm

1. Let the signal be $X(n/NT)$.
   Find out its Fourier transform [6, 7].
2. Calculate the Kernel Functions

$$\psi^{+} = e^{(-i2\pi kn/N)} \quad \text{and} \quad \psi^{-} = e^{(i2\pi kn/N)}$$

3. Find out the window functions w (kT, n/NT).

$$\text{For } n = \left[\frac{N}{2}, \frac{N}{4}, \frac{N}{8}, \ldots 4, 2, 1\right]$$

4. Register the band-pass channel $X(k)$ and apply backwards Fourier change to get $x'(t)$.
5. At long last process the changed specimens for each point "j" in $x'(t)$.

$$S\left(jT, \frac{3n}{4NT}\right) = \sum_{k=0}^{N-1} x'(kT) \cdot w\left(kT - T, \left|\frac{3n}{4NT}\right|\right) \cdot \psi^{+}\left(kT, \left|\frac{3n}{4NT}\right|\right)$$

$$S\left(jT, \frac{-3n}{4NT}\right) = \sum_{k=0}^{N-1} x'(kT) \cdot w\left(kT - T, \left|\frac{3n}{4NT}\right|\right) \cdot \psi^{-}\left(kT, \left|\frac{3n}{4NT}\right|\right)$$

6. End of the process.

2.3 Initial Test System

To analyze the fault we need a fault signal, we are using Simulink model to create a fault. In practical cases, a fault signal consists of fundamental component, harmonics, and noise. To make the situation more practical, we are adding a noise to the fault generated in the Simulink model. We take that signal and sample it and find its frequency spectrum to check the frequencies present in it. Then, we pass the signal to an anti-aliasing low-pass filter to filter the unwanted components [8]. Then, apply **Phasor estimation (Measurement)** to find the magnitude and phase of the signal.

2.4 Phasor Measurement (Estimation)

In general, the relay uses the DSP processor to process. So the inputs must be discrete so the continuous signal is sampled and sent to the DSP processor through a sampling window at a specific rate of sampling. To estimate the magnitude from the samples accurately we use some algorithms. This process of estimation is known as phasor estimation (Measurement) which is shown in Fig. 1.

Test the nonstop voltage or current flag. The figure indicates 12 focuses per cycle (the examining rate is 12 × 50 = 600 Hz). Utilize Discrete Fourier Series (DFS/DFT) strategy to process the size and period of the flag (i.e., applying DFS equation). Compute greatness and stage for every period of the 3-stage amount utilizing one time of information diminishes the impact of estimation clamour.

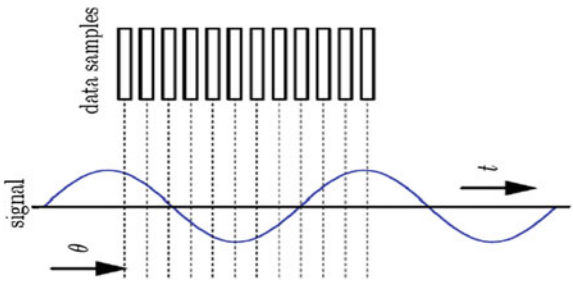


Fig. 1 Schematic of phasor estimation

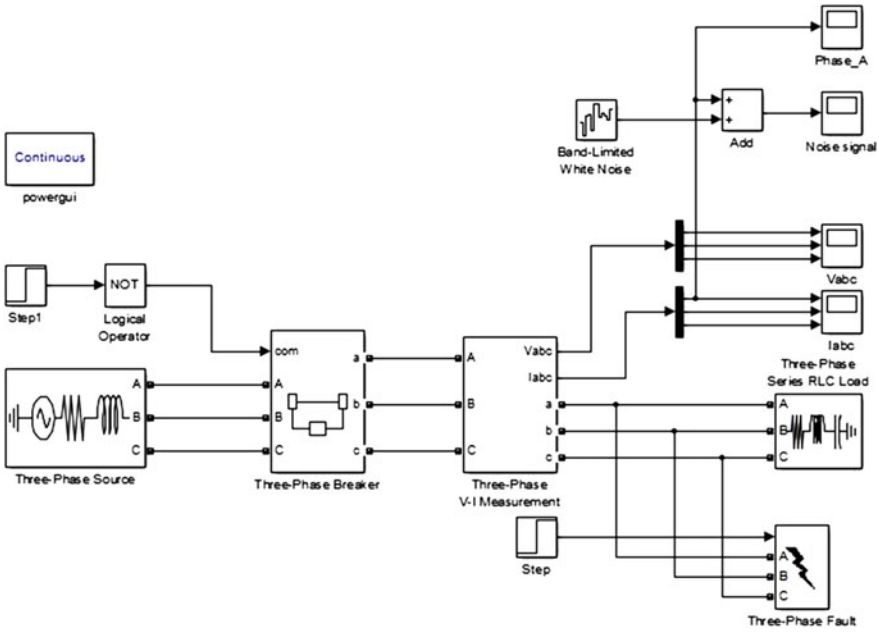


Fig. 2 Schematic showing the initial system to generate fault with noise

3 Results and Discussion

Almost all the PMU's are using DFT to estimate the magnitude and phase of the fault signal which consumes much time and the computational burden is also high. So, we planned to estimate the phasor using the FST. A quick S-Transform calculation was imagined in 2010. It diminishes the computational time and assets by no less than four requests of size and is accessible to the examination group under an open source permit (Fig. 2).

If we observe the output of the estimations of the algorithms in Fig. 3 we can clearly see that conventional S-transform is taking more time to settle at some particular point but where as the DFT is taking less time when comparing to

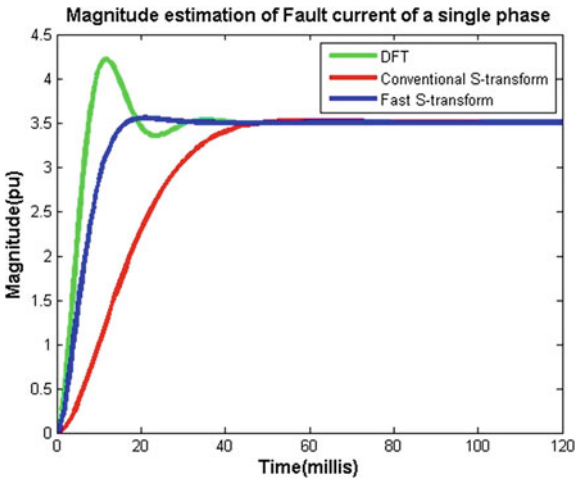


Fig. 3 The output of the algorithms

conventional S-transform but there is a spike in that which increases the magnitude of the fault which may cause malfunction of circuit breaker (C.B) during normal condition. So overcoming these demerits we can find the FST algorithm which has no spike and taking less time comparing to both DFT and Conventional transform.

4 Conclusion

The major outcome of the project is to reduce the computational time in digital relays by implementing the new algorithm. In addition to that, we eliminate the harmonic components present in the noise signal and suppress the DC components which are present in the signal [9]. Finally, using our method we combine all of these algorithms to get the faster relay than the relays which have been already developed using the old and classic algorithms.

References

1. Phadke, A.G., Hlibka, T., Ibrahim, M.: A digital computer system or EHV substations: analysis and field tests. IEEE Trans. Power Apparatus Syst. PAS **95**(1), 290–301 (1976)
2. Brown, R., Zhu, H., Mitchell, J.R.: Distributed vector processing of a new local multi-scale Fourier transform for medical imaging applications. IEEE Trans. Med. Imaging. **24**(5) (2005)
3. Schweitzer, E.O., Hou, D.: Filtering for protective relays. Schweitzer Engineering Laboratories, Pullman, USA, Technical Report (1993)
4. Samantaray, S.R.: Fast S-transform based distance relaying in transmission line. Electr. Power Syst. Res. (2013)
5. Rosolowski, E.: Adaptive measuring algorithm suppressing a decaying DC component for digital protective relays. Electr. Power Syst. Res. **60**(2), 99–105 (2001)

6. Liang, F., Jeyasuryal, B.: Transmission line distance protection using wavelet transform algorithm. IEEE Trans. Power Deliv. **19**(2), 545–553 (2004)
7. Osman, A., Malik, O.: Protection of parallel transmission lines using wavelet transform. IEEE Trans. Power Deliv. **19**(1), 49–55 (2004)
8. Feilat, E.A.: An artificial neural network approach for three-zone distance protection. Int. J. Model. Simul. (2005)
9. Sidhu, T.S.: A New Filtering Technique to Eliminate Decaying Dc and Harmonics for Power System Phasor Estimation. IEEE Power India Conference (2006)

Low-Voltage Low-Power FGMOS-Based Current Conveyor III

Charu Rana, Neelofer Afzal, Dinesh Prasad and Anu

Abstract A new realization of high-performance third-generation current conveyor (CCIII) is proposed in this paper. FGMOS technique is utilized to implement low-voltage CCIII. The inherited features of the proposed block are low supply-voltage, low-power dissipation, and high-output impedance at terminal *Z*. The circuit is simulated in SPICE using 0.13 μm CMOS technology.

Keywords CMOS · FGMOS · Current conveyor · Power dissipation

1 Introduction

The downscaling of the technology and increase in the number of components on the chip have motivated researchers to develop low-voltage, low-power area. Analog circuits with low voltage and low power are required to prolong the battery life of battery operated applications. The threshold voltage of lower technologies hinders the development of low-voltage analog signal processing blocks which furthers prevent the lowering of power dissipation. Several techniques such as MOSFET in subthreshold region, bulk-driven MOSFET, floating gate MOSFET exist to lower the supply voltage. The effective threshold voltage of FGMOSFET

C. Rana (✉) · N. Afzal · D. Prasad · Anu
Jamia Millia Islamia, New Delhi, India
e-mail: Charurana707@gmail.com

N. Afzal
e-mail: neelofar.afzal@yahoo.com

D. Prasad
e-mail: dprasad@jmia.ac.in

Anu
e-mail: anu47@gmail.com

C. Rana
The NorthCap University, Gurgaon, India

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_66

can be reduced by applying a voltage at one of the input terminals through capacitance with large value. Thus, it can operate at low supply voltages. The realization of third-generation current conveyor is mentioned in [1–3], where it is designed using MOSFETs. The features of CCIII are high accuracy, high linearity, and wide bandwidth. Various applications have been realized using CCIII such as current mode filters [4, 5], immittance [6], buffer [8], current mirrors [8, 9], all pass networks [10–16], and receivers [17]. All these applications utilize CCIII as current pass network. In this paper, CCIII is implemented using FGMOS technique for low-voltage operation. The above applications can also be made to work at low-voltage by using FGMOS CCIII instead of MOSFET CCIII. Several other active elements of analog signal processing can also be designed, such as Op Amp, OTA, Trans-conductors, class AB output stage for CMOS Op-Amps, differential voltage current conveyor.

2 Floating Gate MOSFET and Self-cascode Structure

2.1 Floating Gate MOSFET

Floating gate MOSFET is a low-voltage analog design technique. It has a floating gate with n number of inputs. Two layers of polysilicon are used to form first and secondary gates. Figure 1 shows the symbol of FGMOSFET considering all capacitances and connections.

The capacitance of FGMOSFET can be given as a sum of all capacitances C_i where $i = [1, N]$ including capacitance at floating gate and parasitic capacitance present in the MOSFET. The voltage at floating gate is VFG and expressed as (2) after assuming that there is isolation at floating gate and V_i are the inputs voltages and QFG is amount of charge trapped in FGMOS while fabricating it.

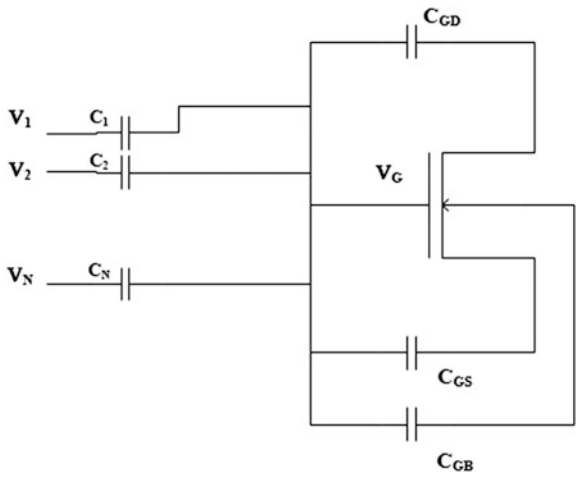


Fig. 1 Symbol of floating gate MOSFET

$$C_{\mathrm{T}} = C_{\mathrm{GD}} + C_{\mathrm{GS}} + C_{\mathrm{GB}} + \sum_{i=1}^{N} C_i \tag{1}$$

$$V_{\mathrm{FG}} = \sum_{i=1}^{N} \frac{C_i}{C_{\mathrm{T}}} + \frac{C_{\mathrm{GS}} V_{\mathrm{S}}}{C_{\mathrm{T}}} + \frac{C_{\mathrm{GS}} V_{\mathrm{D}}}{C_{\mathrm{T}}} + \frac{Q_{\mathrm{FG}}}{C_{\mathrm{T}}} \tag{2}$$

The current ID of FGMOS transistor is expressed as

$$I_{\mathrm{D}} = \frac{\mu \mathrm{C}_{\mathrm{ox}} W}{2L} \left(\sum_{i=1}^{N} \frac{C_i V_i S}{C_{\mathrm{T}}} + \frac{C_{\mathrm{GD}} V_{\mathrm{DS}}}{C_{\mathrm{T}}} + \frac{C_{\mathrm{GB}} V_{\mathrm{BS}}}{C_{\mathrm{T}}} + \frac{Q_{\mathrm{FG}}}{C_{\mathrm{T}}} - V_{\mathrm{T}} \right)^2 \tag{3}$$

where W is the width and L is the length of FGMOS, V_{T} is the threshold voltage, V_{S}, V_{D}, V_{B} are voltages at source, drain and bulk terminals.

2.2 Self-cascode Structure

Single composite transistor is basically a transistor consisting of two transistors and can also be called as self-cascode structure [18]. Figure 2 shows the self-cascode structure, a single input source along with *dc* bias voltage is connected to gates of $M1$ and $M2$. The aspect ratio of $M2$ is kept larger than of $M1$ so that $M1$ is operating in linear region and $M2$ in saturation mode resulting in high gain. The drain to source voltage is quite small of $M1$, so this structure can be represented by a composite transistor.

The condition is $|V_{\mathrm{TH}}M2| - |V_{\mathrm{TH}}M1| \geq |V_{\mathrm{DS}}\mathrm{sat}M2|$ to give high rout. The effective transconductance and output impedance of a self-cascode structure can be given as

$$\mathrm{gm}_{\mathrm{eff}} = \mathrm{gm}_1 \tag{4}$$

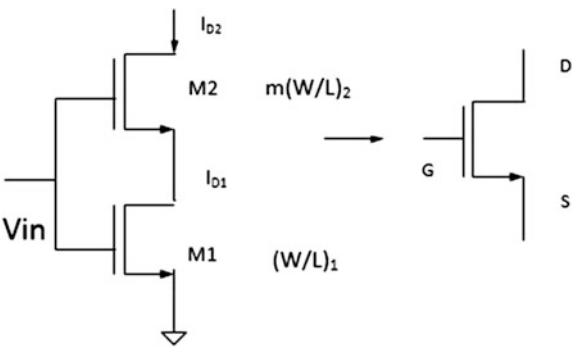


Fig. 2 Self-cascode structure

$$\begin{aligned} \mathrm{ro_{eff}} &= \mathrm{gm_2} * \mathrm{ro_2} * \mathrm{ro_1} - \mathrm{ro_2} * \mathrm{ro_1} \approx (\mathrm{gm_2} * \mathrm{ro_1} - 1) * \mathrm{ro_2} \\ \mathrm{ro_{eff}} &= (\mathrm{m} * \mathrm{gm_1} * \mathrm{ro_1} - 1) * \mathrm{ro_2} = (m - 1) * \mathrm{ro_2} \end{aligned} \tag{5}$$

where m is ratio of $(\mathrm{W/L})_2$ to $(\mathrm{W/L})_1$.

3 FGMOS-Based CCIII

The relationship among terminal voltages and currents of CCIII shown in Fig. 1 are given below

$$\begin{bmatrix} I_y \\ V_x \\ I_{z+} \\ I_{z-} \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & -1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_y \\ I_x \\ V_{z+} \\ V_{z-} \end{bmatrix}$$

According to the ideal conditions, (+1) voltage gain between terminals X and Y, (−1) current gain between X and Y terminals, (+1) current gain between terminals X and Z+ and (−1) current gain between X and Z−.

Figure 2 shows floating gate MOSFET-based third-generation current conveyor. It consists of four current mirrors: $M5$–$M7$, $M6$–$M8$, $M13$–$M15$, and $M14$–$M16$ and the output stage composite transistors $M21$–$M22$ and $M23$–$M24$ transfer the currents in terminals X and Y to Z+ and Z−. Simplicity is the major advantage of current conveyor III. As the main function of current conveyor III is to copy current from X terminal to Z+ terminal and Y terminal to Z− terminal, four current mirrors are utilized to transfer the currents.

The output resistance of conventional CCIII without using FGMOS is given as

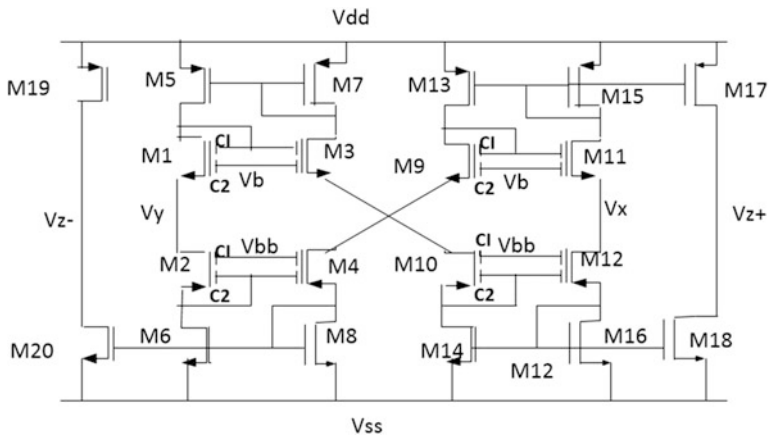


Fig. 3 FGMOS-based CCIII

$$\mathrm{ro}_{z+} = \mathrm{ro}_{21} || \mathrm{ro}_{22} \tag{6}$$

where ro_i is output resistance of ith transistor.

Between the terminals X and Z+ and Y and $Z-$, composite transistors are used in current mirrors $M17$–$M18$ and $M19$–$M20$ which are self-cascode transistors connected in stack form. The output resistance of self-cascode transistor [18] is (Fig. 3)

$$\mathrm{ro} = (m-1) * \mathrm{ro}_1 \tag{7}$$

So, the output resistance at terminal Z+ of FGMOS-based CCIII can be expressed as

$$\mathrm{ro}_{z+} = (m-1) * \mathrm{ro}_{21} || m * \mathrm{ro}_{21} \tag{8}$$

$$\mathrm{ro}_{z+} = (m-1) * (\mathrm{ro}_{21} || \mathrm{ro}_{21}) \tag{9}$$

where the value of m is more than 1.

It can see that the output resistance achieved after using self-cascode structures at Z+ and $Z-$ terminals in FGMOS-based CCIII is higher than the conventional CCIII.

4 Simulation Results and Comparison

The proposed FGMOS-based CCIII is simulated in SPICE program using 0.13 µm technology. The aspect ratios of all NMOS transistors and PMOS transistors selected are 100:1 and 200:1, respectively. The voltage supply used for proper operation is ±1 V. The DC characteristics of proposed FGMOS-based CCIII are observed. The relationship between V_x with respect to V_y is shown in Fig. 4 with the input connected at terminal Y. The voltage at terminal X by connecting a resistance

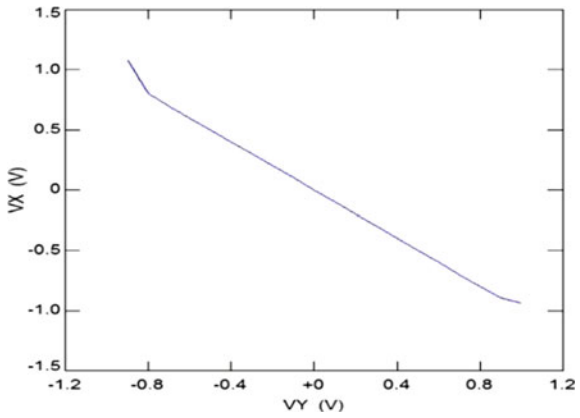


Fig. 4 Relationship between V_x and V_y

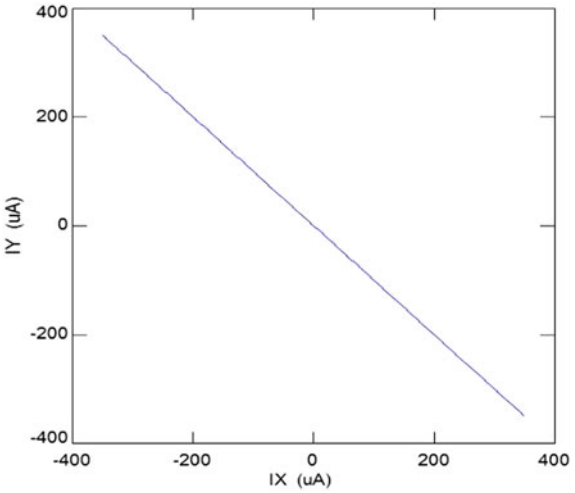


Fig. 5 Relationship between I_x and I_y

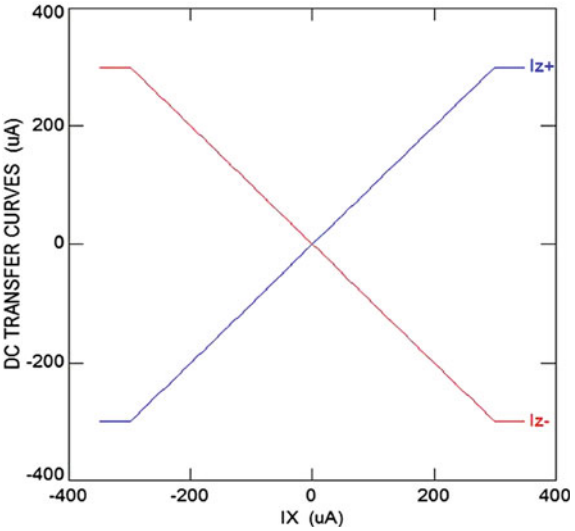


Fig. 6 Relationship between I_{z+}, I_{z-}, and I_x

at this terminal keeping terminal Z grounded. The variation in current at terminal Y with respect to current at X terminal is shown in Fig. 5. The plot of currents at terminal Z; I_{z+} with respect to I_x and I_{z-} with respect to I_x is shown in Fig. 6. The frequency response of current follower for $I_y - I_x$ is given in Fig. 7 and the bandwidth achieved is 89 MHz. Similarly, the frequency response of current followers such as I_{z+} with respect to I_x and I_{z-} with respect to I_x are shown in Fig. 8 and their respective bandwidths are 81.5 MHz for $Z+$ and $Z-$.

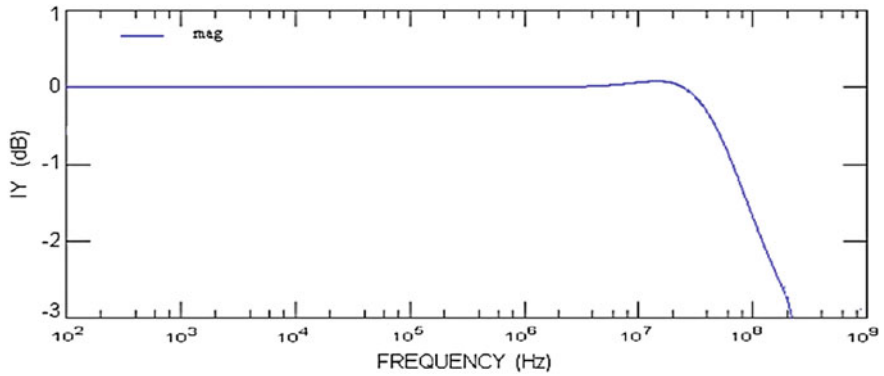


Fig. 7 The frequency response of I_y/I_x

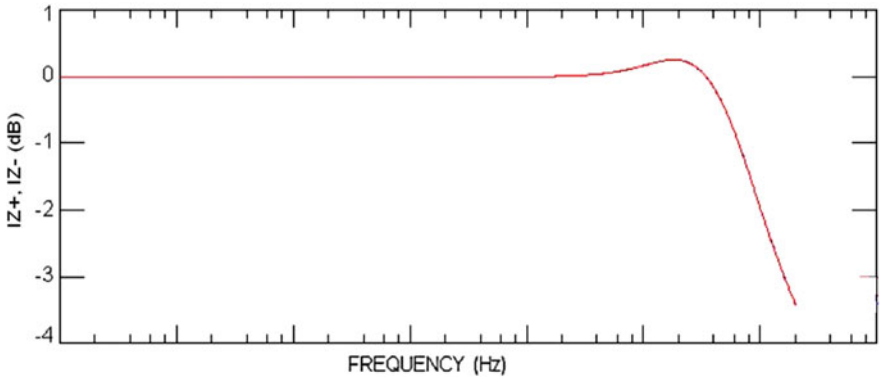


Fig. 8 The frequency response of I_{z+}/I_x and I_{z-}/I_x

Table 1 Comparison of FGMOS-based CCIII with conventional CCIII

Parameter	Conventional CCIII	Proposed FGMOS CCIII
Supply voltage (V)	±2	±1
Linear range $V_X - V_Y$	−0.55–0.6 V	−0.8–0.8
Linear range $I_{Z+} - I_X$	0.8–0.8 mA	−0.3–0.3 mA
Linear range $I_Z - I_X$	0.71–0.75 mA	0.3–(−0.3) mA
I_x/I_y 3 dB	306 MHz	89 MHz
I_{z+}/I_x f 3 dB	106 MHz	81.5 MHz
I_{z-}/I_x f 3 dB	83 MHz	81.5 MHz
Output resistance at $Z+$	18.2 kΩ	6 GΩ
Output resistance at $Z-$	18.2 kΩ	6.1 GΩ
Power dissipation	880 μW	412 μW

Table 1 shows the comparison of proposed CCIII with existing third-generation current conveyors. It can be seen that the voltage supply of proposed CCIII is less than other reported literature. The power dissipation of the proposed circuit is 412 μW. The output impedances measured at terminal $Z+$ and $Z-$ are 6 and 6.1 GΩ. Self-cascode structure utilized in the circuit increased the output impedance at Z terminal. The frequency response of current follower and voltage follower are also compared.

5 Conclusion

A new low-voltage low-power third-generation current conveyor (CCIII) is proposed in this paper. FGMOS technique is used to design this simple CCIII for low-power operation. The power dissipation of FGMOS CCIII measured is 412 μW at voltage supply of ±1 V. The self-cascode structure enhanced the output impedance of Z terminal up to 6 GΩ. This block is suitable for low-voltage analog signal-processing applications.

References

1. Sedra, A., Smith, K.: A second-generation current conveyor and its applications. IEEE Trans. Circuit Theory **17**, 132–133 (1979)
2. Sedra, A., Roberts, G.: The current conveyor: history, progress and new results. IEE Proc. G1 **37**, 78–87 (1990)
3. Fabre, A.: Third generation current conveyor: a new helpful active element. Electron. Lett. **33**, 338–339 (1995)
4. Horng, J.-W., Weng, R.-M., Lee, M.-H., Chang, C.-W.: Universal active current filter using two multiple current output OTAs and one CCIII. Int. J. Electron. **87**, 241–247 (1997)
5. Abuelmaatti, M.T., Alzaher, H.A.: Multi-function active-only current-mode filter with three inputs and one output. Int. J. Electron. **85**, 431–435 (1998)
6. Wang, H.-Y., Lee, C.-T.: Systematic synthesis of R-L and C-D immittances using single CCIII. Int. J. Electron. **8**, 293–301 (2000)
7. Chow, H.-C., Feng, W.-S.: New symmetrical buffer design for VLSI application. Int. J. Electron. **88**, 779–797 (2001)
8. Kuntman, H., Cicekoglu, O., Ozoguz, S.: A modified third generation current conveyor, its characteristic and applications. Frequenz **56**, 47–54 (2002)
9. Zeki, A., Kuntman, H.: Accurate and high output impedance current mirror suitable for CMOS current output stages. Electron. Lett. **33**, 1042–1043 (1997)
10. Pal, K.: Realisation of current conveyor all-pass network. Int. J. Electron. **50**, 165–168 (1981)
11. Higashimura, M., Fukui, Y.: Realization of all-pass networks using a current conveyor. Int. J. Electron. **65**, 249–250 (1988)
12. Higashimura, M., Fukui, Y.: Realization of current mode all pass networks using a current conveyor. IEEE Trans. Circuits Syst. **37**, 660–661 (1990)
13. Soliman, A.M.: Generation of current conveyor based all-pass filters from op-amp based circuits. IEEE Trans. Circuits Syst. II **44**, 324–330 (1997)

14. Cicekoglu, O., Kuntman, H., Berk, S.: All-pass filters using a single current conveyor. Int. J. Electron. **86**, 947–955 (1999)
15. Khan, I., Maheshwari, S.: Simple first order all-pass section using a single CCII. Int. J. Electron. **87**, 303–306 (2000)
16. Toker, A., Ozoguz, S., Cicekoglu, O., Acar, C.: Current-mode all pass filters using current differencing buffered amplifier and a new high-Q bandpass filter configuration. IEEE Trans. Circuits Syst. II **47**, 949–954 (2000)
17. Rudell, G.W., Ou, J.J., Cho, T.B., Chien, G., Brianti, F., Weldon, J.A., Grey, P.A.: 1.9-GHz wide-band IF double conversion CMOS receiver for cordless telephone applications. IEEE J. Solid-State Circuits **32**, 2071–2088 (1997)
18. Comer, D.J., Petrie, C.: The utility of the composite cascade in analog CMOS design. Int. J. Electron. **91**, 491–498 (2004)

Single-Precision Floating Point Matrix Multiplier Using Low-Power Arithmetic Circuits

Soumya Gargave, Yash Agrawal and Rutu Parekh

Abstract This paper presents a single-precision floating point (IEEE 754 standard) matrix multiplier module. This is constructed using subblocks, which include floating point adder and floating point multiplier. These subblocks are designed to achieve the goal of low power consumption. Different architectures of subblocks are compared on the basis of energy-delay product. Design and simulations have been performed for 180 and 45 nm technology node. Simulation results show that design of floating point matrix multiplier is better at 45 nm than 180 nm technology node in terms of lesser delay by 43% and energy-delay product by 97.86% at 1 V. Also, 45 nm technology cells occupy only 6.25% of the area as compared to 180 nm cells.

Keywords Arithmetic and logic circuits · Energy-delay product (EDP)
Floating point multiplication · Low-voltage low-power design
Matrix multiplier · Simulation

1 Introduction

Technology advances brought together large number of devices on a small silicon area, thereby increasing power density on a chip. Low-power designs of these devices are therefore needed to prolong lifetime of a chip as well as the battery. One way to reduce power of a bigger module is to reduce power dissipation at subblocks

S. Gargave · Y. Agrawal · R. Parekh (✉)
VLSI & Embedded Systems Group, Dhirubhai Ambani Institute
of Information and Communication Technology,
Ganghinagar 382007, Gujarat, India
e-mail: rutu_parekh@daiict.ac.in

S. Gargave
e-mail: soumyagargave@gmail.com

Y. Agrawal
e-mail: yash_agrawal@daiict.ac.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_67

level. This requires implementation of judicial design strategies and architectures to obtain the best result for any application. Matrix multiplication unit is used in digital signal processing applications such as, digital imaging, signal processing, computer graphics, and multimedia. So, it is very crucial that it occupies less area, works fast, and consumes low power. IEEE standard 754 floating point (FP) is a representation for real numbers on computers. The goal of this paper is to present a low-power design for FP matrix multiplier. Paper publications in this area have been limited to building algorithm [1, 2] and subblocks required for floating point matrix multipliers, which include floating point multiplier [3] and floating point adder [4]. The circuit level simulation of designs at 180 and 45 nm technology nodes is performed using low-voltage and low-power design techniques in Virtuoso-Cadence environment.

The rest of the paper is organized as follows. Section 2 presents architecture of FP matrix multiplier along with its subblocks like multiplexer, FP multiplier, FP adder, and register. Section 3 presents the simulation results and comparison of delay, power, and energy-delay product (EDP) at 180 and 45 nm node for low-power design. Finally, conclusion is drawn in Sect. 4.

2 Matrix Multiplier Implementation

FP matrix multiplication is performed basically in two steps, FP multiplication and FP addition. In this paper, power is reduced by reusing the adder architecture to perform addition one after the other [1, 2]. This is an efficient technique to reduce power consumption by breaking the main circuit in partially sequential and partially parallel parts. Matrix multiplication operation is performed as follows:

$$\begin{bmatrix} X_{11} & X_{12} & X_{13} & X_{14} \\ X_{21} & X_{22} & X_{23} & X_{24} \\ X_{31} & X_{32} & X_{33} & X_{34} \\ X_{41} & X_{42} & X_{43} & X_{44} \end{bmatrix} \times \begin{bmatrix} Y_{11} & Y_{12} & Y_{13} & Y_{14} \\ Y_{21} & Y_{22} & Y_{23} & Y_{24} \\ Y_{31} & Y_{32} & Y_{33} & Y_{34} \\ Y_{41} & Y_{42} & Y_{43} & Y_{44} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & Z_{13} & Z_{14} \\ Z_{21} & Z_{22} & Z_{23} & Z_{24} \\ Z_{31} & Z_{32} & Z_{33} & Z_{34} \\ Z_{41} & Z_{42} & Z_{43} & Z_{44} \end{bmatrix}, \tag{1}$$

where

$$Z_{11} = X_{11}Y_{11} + X_{12}Y_{21} + X_{13}Y_{31} + X_{14}Y_{41}, \tag{2}$$

$$Z_{12} = X_{11}Y_{12} + X_{12}Y_{22} + X_{13}Y_{32} + X_{14}Y_{42}, \tag{3}$$

and so on…

The block diagram of FP matrix multiplier along with its subblocks is shown in Fig. 1a–e. Figure 1a depicts the 4 × 4 matrix multiplier. Figure 1b shows operation of each cell of the matrix multiplier. It comprises of 4:1 MUX, FP multiplier, FP adder, and memory register. The circuit diagram of 4:1 MUX is presented in

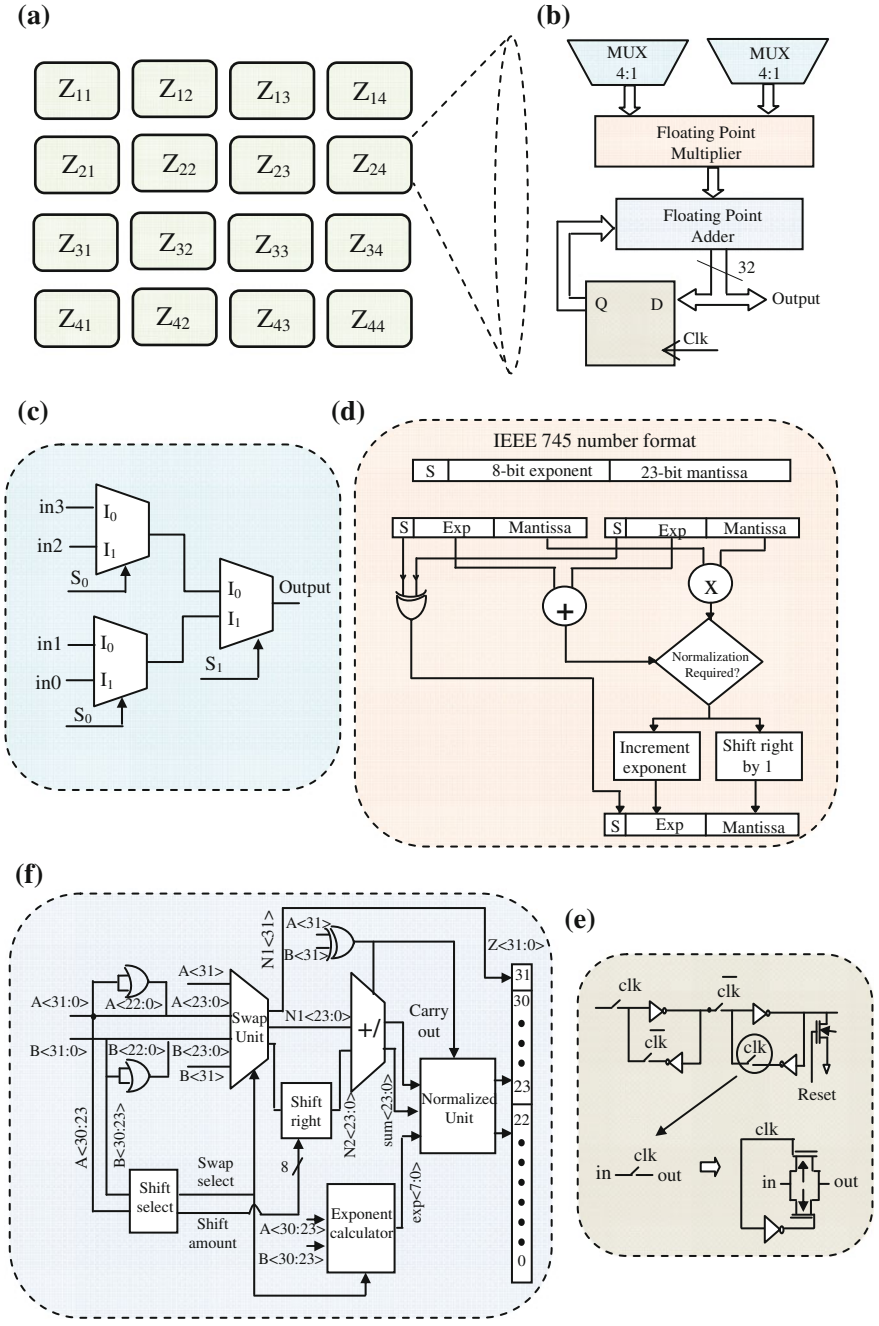


Fig. 1 Representation of FP matrix multiplier and its subblocks. **a** Architecture of 4 × 4 FP matrix multiplier. **b** FP matrix multiplier block diagram. **c** MUX schematic. **d** FP multiplier block diagram. **e** FP adder block diagram. **f** 1-bit register circuit

Fig. 1c. MUX selects the inputs of the two matrices to be multiplied. These are 4:1 MUX for matrices of size 4×4. Each MUX gives output as a 32-bit single-precision floating point number. These are inputs to the floating point multiplier unit.

The FP multiplier unit has three subparts as shown in Fig. 1d. Floating point multiplication [3] is done in three steps: sign calculation, exponent calculation, and mantissa calculation. The multiplier unit used for mantissa calculation is the slowest path as it has to perform operation on 24 bits (23 bits mantissa and 1 bit normalizing bit). So, in order to make this subblock fast, different architectures of multipliers have been studied. FP multiplier can be implemented using several designs as divide and conquer multiplier [5], Wallace tree multiplier [6], and Barun multiplier [5]. Divide and conquer multiplier is used mostly in FPGAs, as this leads to fast calculation. However, this comes at the expense of more hardware. Wallace tree multiplier has less number of bits in each level, but delay is not evenly distributed. So, it may cause glitches. Also, the tree structure uses a lot of interconnection; therefore uses a lot more area. Barun multiplier shown in Fig. 2 offers evenly distributed delay for the inputs of a full adder and it can be extended to multiply higher number of bits. Based on the simulation results presented in Sect. 3 for all the above three multipliers, it has been inferred that Barun multiplier offers lesser EDP. Consequently, this is incorporated in the present low-power FP matrix multiplier design.

The basic block in FP matrix multiplier is a full adder. Different architectures of full adder like 17-T, 14-T, 10-T have been discussed in [7]. The 17-T adder proves to be the best architecture in terms of power, delay, and power-delay product. A 17-T adder was made using pass transistor logic, but there is a probability of getting wrong logic at the output. For example, say when $a = b = 0$ the output at

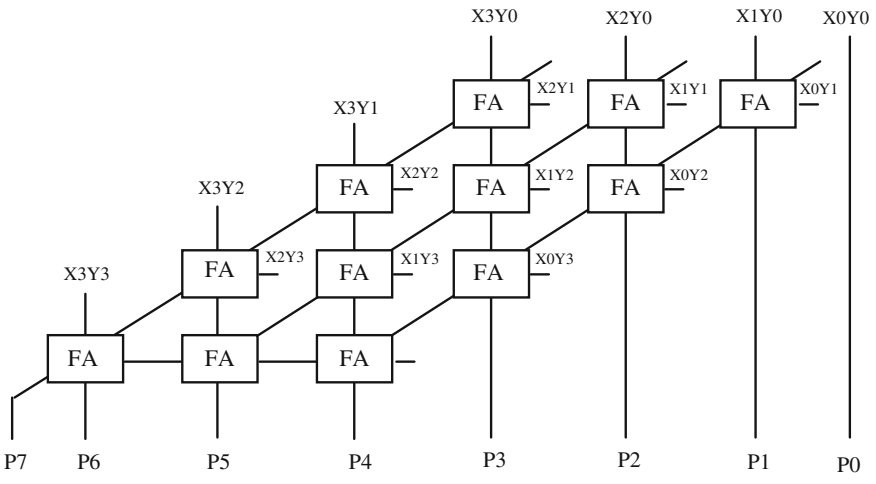


Fig. 2 Barun multiplier

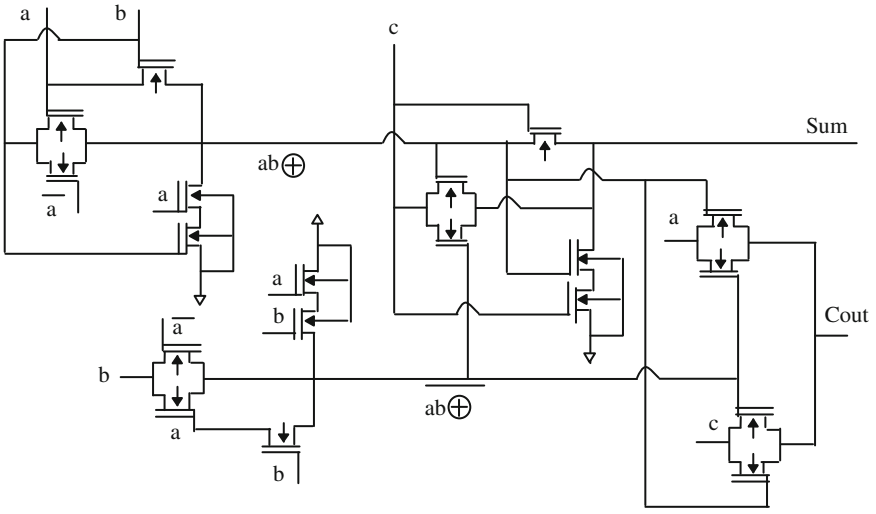


Fig. 3 Proposed full adder

$a \oplus b$ is V_{tp} and that at Ex-NOR is $V_{dd} - V_{tn}$. This problem increases when adders are cascaded as inputs a and b can be output of any previous adder. So, modified 17T architecture is proposed here and used in this work. This is shown in Fig. 3. In this, transmission gate is used instead of pass transistor which transfers full logic.

The addition of two FP numbers is the trickiest part. The algorithm for FP addition is taken from [4] and block diagram for the same is shown in Fig. 1e. FP adder performs addition of partial products, as shown in Eqs. (2) and (3). First, there is a need to make exponent of both the operands equal in order to perform addition. According to Fig. 1e, if $|B_{exp}| > |A_{exp}|$ ($B_{exp} = B\langle 30:23\rangle$ and $A_{exp} = A\langle 30:23\rangle$), then swapping of the numbers is required, which implies that the signal swap select = 1. The mantissa of smaller number (A) is shifted right by the shift amount to make exponent of both equal and then added to or subtracted from other number, as per the signs of the two numbers. Normalizing unit normalizes the output to IEEE 754 format again.

A 32-bit register stores the value of the adder block, such that it can be added again to the new multiplied value. Figure 1f shows the circuit diagram of 1-bit register.

Power of the FP matrix multiplier in the present design is reduced by,

(1) Using multiplier module with sleep transistor logic.
(2) Reducing the bit width for the floating point multiplier input from 24 to 12 bits [8]. This method is called *bit truncation*.

The inputs to the multiplier in Fig. 1d are of 24 bits, so after multiplication output is of 48 bits. But as this output needs to be fitted in FP format again, rounding has to be done. This requires more power. Consequently to reduce power,

bit truncation is used in which inputs are reduced to 12 bits, giving output of 24 bits. This can be effectively used in most of the applications like sensors, image processing, etc., where limited accuracy can be tolerated.

3 Simulation Results

Simulations are performed on circuits made using UMC 180 nm and gpdk 45 nm technology node library in Cadence Virtuoso, so as to compare low-power designs of both technologies in terms of EDP. Figure 4a shows the comparison of EDP for different multiplier architectures. It is evident from the figure that Braun multiplier is best in terms of lower EDP and minimum energy-delay point is observed at 1 V. So, this multiplier is built again using 45 nm technology cells and compared under same conditions with 180 nm circuit. It is clear from Fig. 4b that the best case (1 V) value of 45 nm circuit is lower than the best case (1 V) value of 180 nm circuit.

The functionality of FP multiplier and adder units have been analyzed. It has been investigated that FP multiplier discussed here has an improvement of 61.9% in EDP with respect to [9] (904.2E−21 J) and FP adder has an improvement of 94.8% in power with respect to [10] (5.6 mW). For logic and functionality verification, single element of the FP matrix multiplier is implemented and presented below. Using Eq. (2), the first element of the output matrix is computed as:

$$Z_{11} = X_{11}Y_{11} + X_{12}Y_{21} + X_{13}Y_{31} + X_{14}Y_{41},$$

Let,

$$X_{11} = -16.23998,\ X_{12} = -12.55799,\ X_{13} = 1.26839,\ X_{14} = 1.26839,$$
$$Y_{11} = -12.2398,\ Y_{21} = 0.01246,\ Y_{31} = 124.8939,\ \text{and}\ Y_{41} = 0.01246.$$

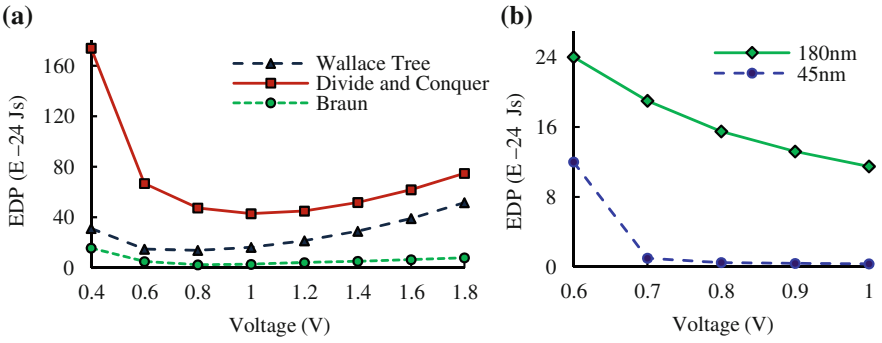


Fig. 4 **a** EDP of different multipliers at 180 nm technology node. **b** EDP comparison of Barun multiplier at 180 and 45 nm technology nodes

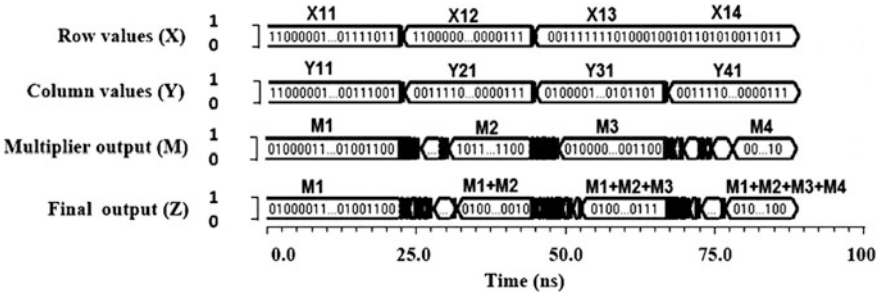


Fig. 5 Simulation table for floating point matrix multiplier

Here X_{11}, X_{12}, X_{13}, and X_{14} are the inputs to MUX1, which is first element in Fig. 1b. These comprise row vector. While Y_{11}, Y_{21}, Y_{31}, and Y_{41} are the inputs to MUX2, these comprise column vector. $M1$ ($X_{11} \times Y_{11}$), $M2$ ($X_{12} \times Y_{21}$), $M3$ ($X_{13} \times Y_{31}$), and $M4$ ($X_{14} \times Y_{41}$) are corresponding products of the row and column values. Z is the final output, which is $M1 + M2 + M3 + M4$. The output from the simulator ADE-XL of virtuoso is shown in Fig. 5. Table 1 shows the simulated result of a single element Z (equals to $M1 + M2 + M3 + M4$) for floating point matrix multiplier. It is analyzed that the error between desired and simulated output is 0.044% which is because of rounding the product of multiplication to 24 bits as in FP multiplication algorithm. Table 2 presents power, delay, and EDP obtained from the simulation results of FP matrix multiplier at 180 nm for normal voltage of 1.8 V and low-power design at 1 V. The same FP matrix multiplier circuit is implemented for 45 nm technology node. Table 3 compares the results for 180 and 45 nm technology at 1 V.

Table 1 Output of first element of floating point matrix multiplier (180 nm)

Quantity	Decimal value	32-bit floating point binary value
Desired output	357.0476	0 10000111 01100101000011000011000
Simulated output	356.89	0 10000111 01100100111000111101100

Table 2 Simulation results of floating point matrix multiplier at 180 nm

Parameters	At 1.8 V	At 1 V
Total power (mW)	5.006	0.805
Static power (μW)	145.2	48.09
Dynamic power (mW)	4.8608	0.757
Delay (ns)	55.6478	91.8
EDP (Js)	15.5E−18	6.783E−18

Table 3 Comparison of logic circuits at 180 and 45 nm at supply of 1 V

Logic circuit	Technology (nm)	Delay (ns)	Static power (μW)	Dynamic power (μW)	Total power (μW)	EDP (Js)
Braun multiplier	180	2.4249	0.798	1.286	2.084	12.25E−24
	45	0.7651	0.001	0.752	0.0762	0.045E−24
FP multiplier	180	7.9722	9.619	68.711	78.33	4.96E−21
	45	2.0788	0.0126	3.8904	3.903	0.017E−21
FP adder	180	25.323	17.7	401.8	419.5	269E−21
	45	14.084	0.7347	9.4553	10.19	2.02E−21
FP matrix multiplier	180	91.8	48.0932	757.2068	805.3	6.786E−18
	45	52.32	0.0672	52.7728	52.32	0.145E−18

4 Conclusion

The floating point matrix multiplier operating at low voltages is designed and simulated at 180 and 45 nm technology nodes. Various parameters like propagation delay, power dissipation, and energy-delay product have been studied. Based on the study, it is concluded that best performance (in terms of EDP) is achieved by fixing supply voltage to 1 V at 180 nm node. The FP matrix multiplier circuits made by using 45 nm technology reduce delay by 43%, power by 93.44%, and EDP by 97.86% as compared to circuits made at 180 nm technology cells at 1 V. In addition, the 45 nm technology cell occupies only 6.25% of the area as compared to 180 nm cells.

References

1. Lin, R.: A reconfigurable low-power high-performance matrix multiplier design. In: Proceedings of IEEE Symposium Quality Electronic Design, pp. 1–8 (2000)
2. Saha, P., Banerjee, A., Bhattacharyya, P., Dandapat, A.: Improved matrix multiplier design for high-speed digital signal processing applications. IET Circuits Devices Syst. **8**, 27–37 (2014)
3. Al-Ashrafy, M., Salem, A., Anis, W.: An efficient implementation of floating point multiplier. In: Proceedings of Saudi International Conference Electronics, Communications and Photonics, pp. 1–5 (2011)
4. Loucas, L., Cook, T.A., Johnson, W.H.: Implementation of IEEE single precision floating point addition and multiplication on FPGAs. In: Proceedings of IEEE Symposium FPGAs for Custom Computing Machines, pp. 107–116 (1996)

5. Belkacemi, S., Benkrid, K., Crookes, D., Benkrid, A.: Design and implementation of a high performance matrix multiplier core for Xilinx Virtex FPGAs. IEEE International Workshop on Computer Architectures for Machine Perception, pp. 156–159 (2003)
6. Gupta, J., Grover, A., Wadhwa, G.K., Grover, N.: Multipliers using low power adder cells using 180 nm technology. In: Proceedings of IEEE International Symposium Computational and Business Intelligence, pp. 3–6 (2013)
7. Yeo, K., Roy, K.: Low-Voltage, Low-Power VLSI Subsystems (Chapter 3). McGraw-Hill, pp. 63–89 (2005)
8. Tong, J.Y.F., Nagle, D., Rutenbar, R.A.: Reducing power by optimizing the necessary precision/range of floating-point arithmetic. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. **8**, 273–286 (2000)
9. Sivanantham, S.: Design of low power floating-point multiplier with reduced switching activity in deep submicron technology. Int. J. Appl. Eng. Res. **8**, 851–859 (2013)
10. Gilani, S.Z., Kim, N.S., Schulte, M.: Energy-efficient floating-point arithmetic for software-defined radio architectures. In: Proceedings of IEEE International Conference on Application-Specific Systems, Architectures and Processors, pp. 122–129 (2011)

Monitoring Real and Reactive Power in a Transmission Network Using Generalized Unified Power Flow Controller

Raja Reddy Duvvuru, B. Venkata Prasanth and V. Ganesh

Abstract The generalized UPFC has been treated as voltage source dependent converter. This paper explains a complete model of 48-pulse GTO voltage source converter, here four 12-pulse converters are used to form a single 48-pulse converter. Main objective of using GUPFC is to control the reactive and real power through transmission line. GUPFC contains single shunt converter as well as two series converters, the two devices operate as VSC. Here, shunt converter acts like a static synchronous compensator (STATCOM) which is used for injecting current into the line, also the device regulates bus voltage. The two series converters act like SSSC which is used for injecting the voltage into the line. Based upon current control strategy, the shunt and series controllers are operated. Results are carried out by MATLAB/Simulink software.

Keywords 48-pulse gate turn off device · Generalized unified PFC
Active compensation · System stability

1 Introduction

Among all switching devices, GTO device have very elevated power managing capacity so that they are widely used in controlling the active and reactive power. Here, voltage source converter technology is adopted in the converters. GUPFC

R.R. Duvvuru (✉)
Department of Electrical Power Engineering, JNTU University, Anantapur, Anantapur, India
e-mail: rajajntuacep@gmail.com

B. Venkata Prasanth
QIS College of Engineering and Technology, Ongole, India
e-mail: venkataprasanthb@gmail.com

V. Ganesh
Department of Electrical and Electronics Engineering, JNTUA College of Engineering, Pulivendula, Pulivendula, India
e-mail: ganivg@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_68

consists of two series and a single shunt converter, so that GUPFC is treated as a three converter controller. A common DC link is used to connect both the converters, the real and reactive power is exchanged among the converters through this link. Mainly, the FACTS devices are used in controlling the bus voltages, line impedances and the load angles of the transmission line [1]. Among the FACTS devices, this GUPFC is used in monitoring five power system parameters such as real and reactive powers, bus voltages at both ends and provides reactive power compensation. Power quality devices are used for providing reactive power compensation. Here, a complete model of 48-pulse gate turn off VSC is used four 12-pulse converters form a single 48-pulse converter. The 48-pulse VSC produces less harmonic distortion because when the pulse number increases harmonics gets reduced and also minimizes the power quality problems when compared with other converters such as (6, 12, 24 and 36) pulse. The THD in output voltage of a converter can be tentatively minimized without increasing the order of bridges. The projected arrangement requires only one injected transformer, so that fact does not exist. Also, by reducing number of transformers the total cost can be minimized. The 48-pulse VSC consists of an auxiliary circuit and a double-bridge converter. For the main bridges, the converter operates at primary frequency, and for the auxiliary circuit, the converters operate four times the primary frequency. The voltage across the main bridges drops to zero when the DC voltage is injected through the line. Due to this reason, switching losses in the converter become very high. These features are essential for high voltage applications.

2 Modelling of GUPFC

Both the shunt and series controllers in the GUPFC are operated as the voltage source converters. Interline power flow controller (IPFC) related to FACTS family can be treated as voltage source converter. The circuit designing of IPFC is done in MATLAB [2]. Suitable representation of GUPFC is given in Fig. 1.

For regulating real power in the line, the reactive voltage which is introduced by each VSC is monitored. Simultaneous operation of VSC's is needed here when one VSC is monitoring the DC voltage then the other VSC's must regulate the reactive power that flows in transmission lines. This reactive power flow is regulated by introducing the real voltage within the line. Here, shunt device acts like a static-synchronous compensator (STATCOM) used for injecting the current into the transmission line and also it regulates bus voltage. Two series converters act like a SSSC used for injecting the voltage into the line. Based on decoupled current control stratagem, both shunt and series controllers are operated [3, 4].

Here, a complete model of 48-pulse gate turn off VSC is used four 12-pulse converters to form a single 48-pulse converter. The 48-pulse VSC produces less harmonic distortion because when the pulse number increases harmonics gets reduced and also minimizes the power quality problems when compared with other converters such as (6, 12, 24, and 36) pulse.

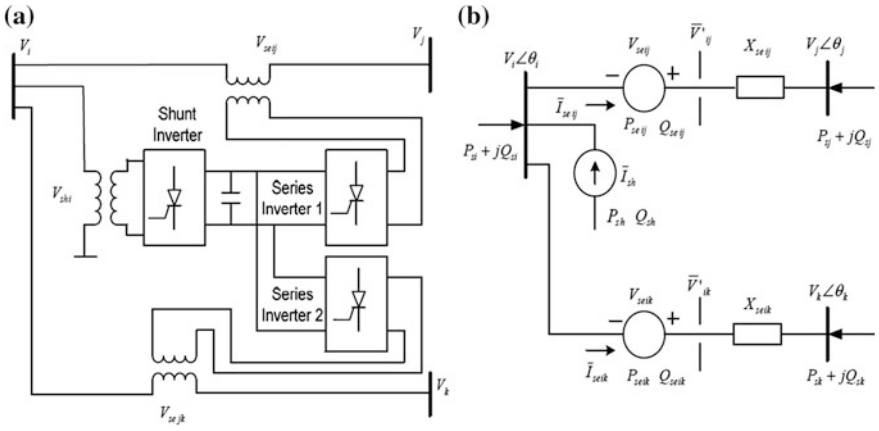


Fig. 1 (**a**) Suitable model of GUPFC converters. (**b**) Equivalent model of GUPFC

3 GUPFC with 48-Pulse GTO Base VSC

The equivalent shunt circuit diagram comprises of a three-phase gate turn off thyristor, and a transformer provided by single-leakage reactance, capacitor which is placed at DC side. The reactive power substitution among the shunt converter and the line exists due to the voltage variation across transformer. En route for pickup system voltage profile, the voltage along the line is monitored this is the main duty of shunt piece of equipment. The primary purpose of shunt converter is controlling the magnitude of bus voltages by captivating or producing the reactive power. Through the transformer leakage reactance, the reactive power can be transmitted by keeping the voltage across secondary within the phase of primary voltage of the transformer.

The corresponding figure of the GUPFC is represented in Fig. 2, which is implemented in making changes in UPFC circuit diagram [5]; where V_p is the output voltage of the transformer, L_p, L_c is the leakage inductances and R_p, R_c are the resistances related to particular transformers. The shunt converter acts as an inductor, when the voltage across the secondary side is less than system voltage. Similarly shunt converter acts as a capacitor in the opposite way as mentioned in above. Here, when the converter acts as a inductor the converter absorbs the reactive power, and vice versa. Due to the losses occurred in the inverter, the voltage across every bus leads the voltage across the inverter with a minute angle during the stable region.

Mainly, there are three methods in eliminating the harmonics from the system caused to switching operations. They are as follows: eliminating harmonics by providing magnetic coupling, by adopting PWM switching techniques, by using multilevel converter configurations, by using four 12-pulse converters, a single 48-pulse converter is formed. Among all the harmonics third harmonic is the most dangerous harmonics so by increasing the number of pulses, lower order harmonics

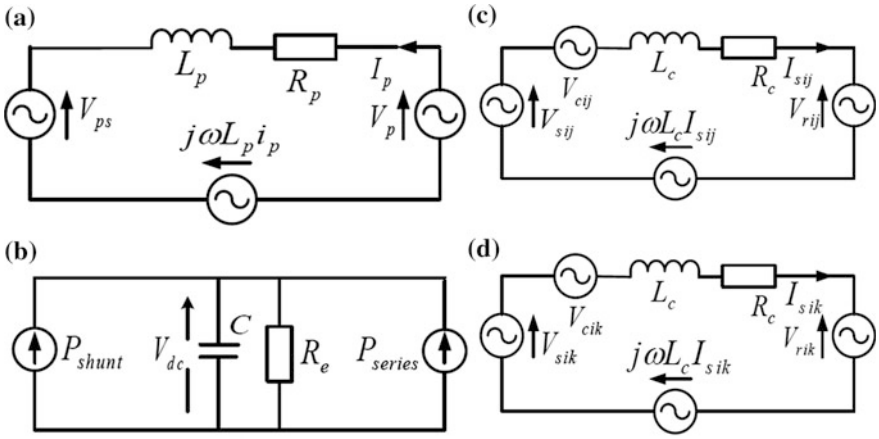


Fig. 2 Corresponding figure for Generalized Unified PFC, **a** shunt device **b** power flow in AC and DC **c** and **d** series device

can be easily nullified compared to 60-pulse converter [6]. The 48-pulse voltage source converter produces less harmonic distortion because when the pulse number increases harmonics gets reduced and also minimizes the power quality problems when compared with other converters such as (6, 12, 24 and 36) pulse. Here, the shunt device acts like STATCOM used for injecting the current into line, in addition it controls the bus voltage. The two series converters act as a SSSC used for injecting the voltage into the line.

4 GUPFC-Simulation Model

In this paper, a novel model using 48-pulse Simulink model of the generalized UPFC is shown. The model is simulated using MATLAB/Simulink, this entire procedure depends upon the decoupled current control approach method *using* d-component as well as q-component currents in series VSC, shunt voltage source converter.

4.1 A Brief Justification on the Grid

GUPFC is connected in transmission line (500 kV, 100 MVA) AC grid network. In these, modelling of GUPFC 48-pulse GTO and its decoupled current control method for shunt voltage source converter and control scheme of two series voltage source converters is done by MATLAB/Simulation. Figure 3 illustrates single line representation of GUPFC grid network. In these, network 500 kV voltage source,

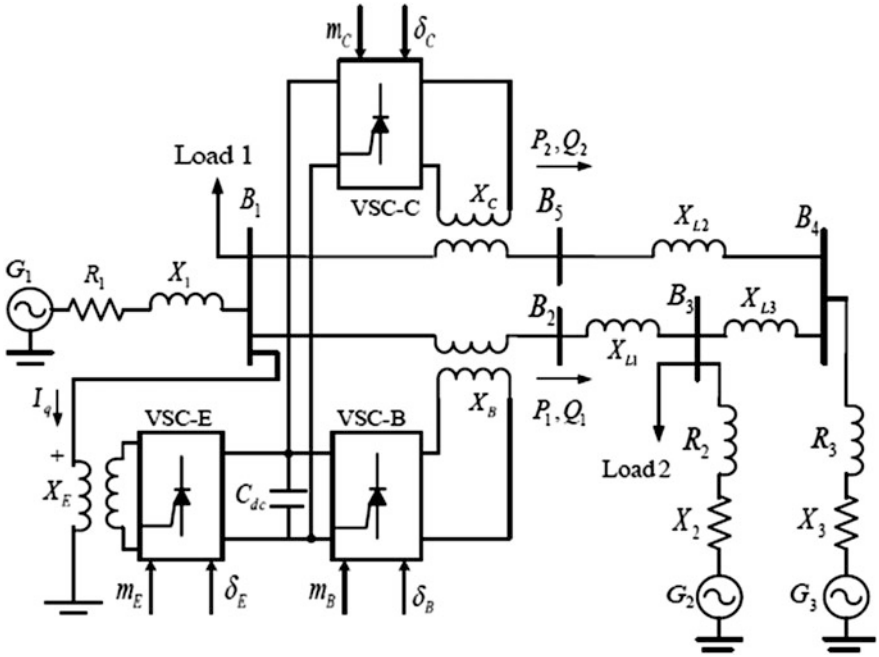


Fig. 3 Three-bus system with GUPFC at bus B2 and B5

8500 MVA with inject load of 300 MW at bus B1, 6500 MVA with inject load of 200 MW at bus B3 and 9000 MVA at bus B4 are used.

Generalized UPFC modelling is employed to regulate ability of the power that surges through a 500 kV-transmission system. Generalized unified power flow controller device placed next to load side, connecting 500 kV buses 1, 5, is employed for changeable real power passing during the course of bus 2, 5 and regulating the voltage by the side of bus 1. It contains 3–100 MVA, 3-level, 48-pulse gate turn off thyristors, one of the converter is related to shunt at bus 1, the two convertors are related in series among buses 1, 2, along with buses 1, 5. Power between the series and shunt converters is able to exchange the course of a DC bus.

The Simulink diagram of GUPFC model by considering reference power and voltage values is capable of modifying by using generalized unified power flow controller-graphic user interface block. GUPFC model is operated at three modes, the shunt-converter is operated same as STATCOM. Three-stage shunt converters operate by the side of fixed conduction angle (sigma $\sigma = 180 - 7.5 = 172.5°$), hence generate a quasi-sinusoidal 48-pulse voltage step wave form. The major harmonics are 47 and 49. During the operation of GUPFC, the amount of voltage that is introduced by two series converters will change by modifying the value of σ, subsequently high harmonic content will be created in the shunt converter. At the same time, 48-pulse waveform is produced by series converter when its function is analogous in the direction of SSSC mode.

In these network, the power that is flowing throughout the buses B5 and B2 during a period of zero voltage is produced from two series converters; where as in GUPFC mode, both phase angle and magnitude and injected voltages of two series converters could be adjusted, which in turn allows the monitoring of real power in addition to reactive power. Generalized unified PFC convenient area is achieved by maintaining the maximum value of introduced voltage is (0.1 pu) and by varying the phase angle from 0 to 360°. The generalized UPFC tool consists of complete 48-pulse VSC representation that is linked with the electrical grid system with a suitable coupled transformer. Controlling the voltage across the various buses is done by decoupled current control method. The 48-pulse voltage source converter produces a lesser amount of harmonics and in turn decreases the troubles in power quality compared to the additional converters. This results in smallest amount of effective overloading and harmonic instability problems and also corrects performance calculation of voltage, reactive power and active power flowing through line and evaluates the stability circumstances.

4.2 48-Pulse GTO-Based VSC

This converter was designed with four 12-pulse gate turn off converters, with a phase shift of 7.5° starting from every converter, which presents the whole act performed by 48-pulse converter. By adopting symmetrical shift principle 7.5° is presented in a subsequent manner, −3.75° phase shift is provided on both the transformers that are coupled, +3.75° is given for first 20 four-pulse converter and to the next converter and extra phase winding is provided with a phase shift of −3.75°. A 48-pulse converter is made up of four matching 12-pulse gate turn off converters. Figure 3 shows a bus model of the 48-pulse gate turn off converter representation for shunt voltage source converter, this concept is analysed from 36-pulse gate turn off thyristor model. The same mode can be established for series VSC. The 48-pulse GTO device used in HV appliances, by using these converter there is no need of using the ac filters for reducing harmonics present on ac side.

5 Simulation Results

Under various circumstances, the series converters insist for more amount of power, a capacitor rating of 2500 pF is utilized. First the shunt VSC device is intended and response of the converter was examined during the starting periods. Previous to starting the method, the DC link capacitor is supposed to charge to its initial values. Figure 4 represents the simulation results obtained by the shunt model during starting periods. Figures 5 and 6 represent the waveforms formed by using generalized unified PFC in controlling the power. After observing results produced by

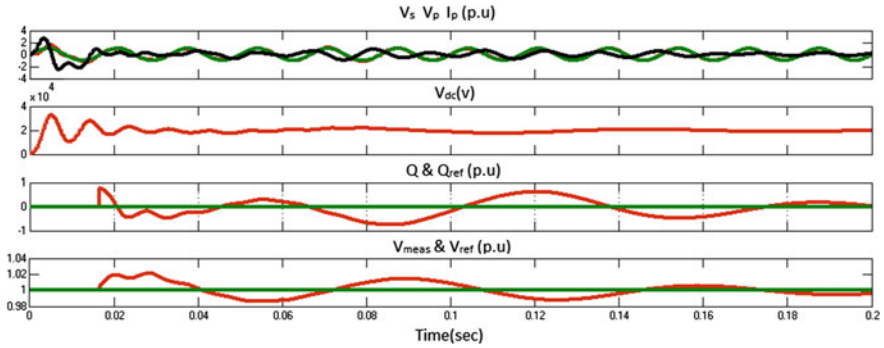


Fig. 4 Generalized UPFC shunt converter operating at Q_{ref} = 0.4 pu; 0.5 pu

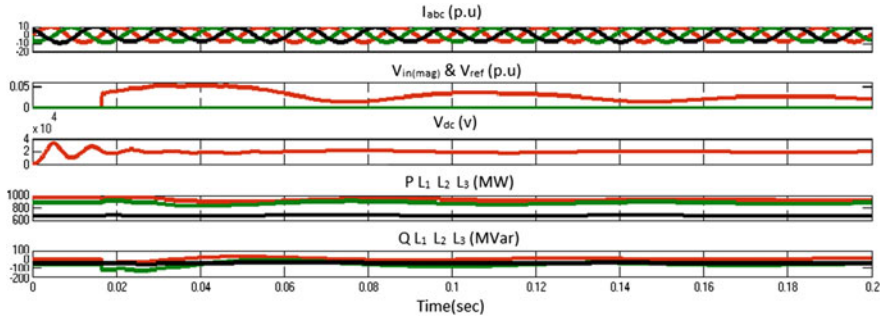


Fig. 5 Generalized UPFC converter operating at P_{ref} = 8.8 pu; 10 pu, Q_{ref} = −0.7 pu; 0.7 pu

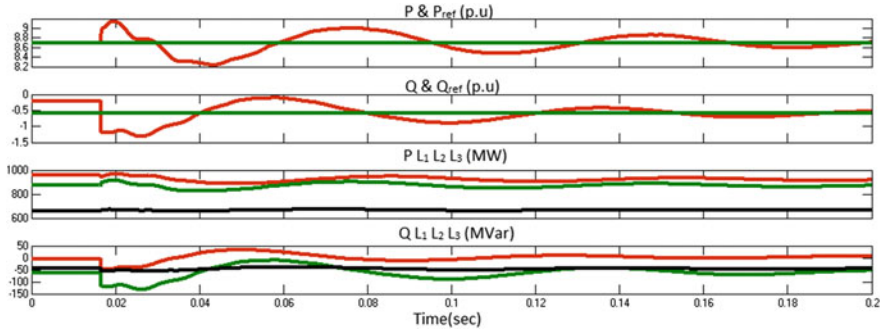


Fig. 6 Generalized UPFC converter operating active and reactive power at P_{ref} = 8.8 pu; 10 pu and Q_{ref} = −0.7 pu; 0.7 pu

shunt converter, the response of series converter taking place at 0.25 s, the real power and reactive power values are brought back to normal ideal values and both the powers are totally monitored using generalized unified power flow controller.

6 Conclusion

This manuscript proposes a complete representation consisting 48-pulse voltage source based device which builds up generalized unified power flow controller FACTS devices. A coupling transformer is to connect all these 48-pulse VSC flow models towards grid system. By using some current control strategies, these cascade models are authorized for managing real, reactive power compensation. Some control methods employs current control method to certify controllability, reduced oscillatory behaviour and system instability. The 48-pulse VSC based device produces less harmonic distortion because when the pulse number increases, harmonics gets reduced and also minimizes the power quality problems when compared with other converters such as (6, 12, 24 and 36) pulse. The entire model of a GUPFC has been obtained in the synchronous reference frame and the control schemes of two converters are shown. The results that are shown validate the presentation of generalized unified PFC in monitoring the real as well as reactive power.

References

1. Hingorani, N.G., Gyugyi, L.: Understanding FACTS, concepts and technology of flexible AC transmission systems. IEEE Press, Pscataway (2000)
2. Reddy, B.S.R., Rani, A.P.U.: Modeling and digital simulation of interline power flow controller system. Int. J. Comput. Electr. Eng. **2**(3), 441–446 (2010)
3. Sharaf, A.M., El-Moursi, M.S.: Novel controllers for the 48-pulse VSC STATCOM and SSSC for voltage regulation and reactive power compensation. IEEE Trans. Power Syst. **20**(4), 1985–1997 (2005)
4. Sharaf, A.M., Norouzi, A.H.: Two control schemes to enhance the dynamic performance of the STATCOM and SSSC. IEEE Trans. Power Deliv. **20**(1), 435–442 (2005)
5. Agelidis, V.G., Xu, L.: Flying capacitor multilevel PWM converter based UPFC. IEE Proc. Electr. Power Appl. **149**(4), 304–310 (2002)
6. Z. Xu, J. Zhang, W. Pan: Novel configuration of 60-pulse voltage source converter for STATCOM application. Int. J. Emerg. Electr. Power Syst. **8**(5), Article 7 (2007)

Improvement of Power System Security Under Single Line Critical Contingency Condition by Optimal Placement of Multiple TCSCs

Pallavi Choudekar, Sanjay Sinha and Anwar Siddiqui

Abstract Transmission congestion occurs in a power system due to increase in load demand. This mainly occurs in restructured power system because of restrictions of transmission line capacity. Due to this power system does not remain in secure condition. Ranking of contingency is done using performance index and critical contingency is found. In this paper, placement of multiple TCSCs for reducing transmission line congestion under single line critical contingency condition is done. Optimal location for placement of TCSCs is found out by using sensitivity analysis. By placing two TCSCs, there is reduction in line loading, improvement in voltage profile and reduction in reactive power loss, thus keeping power system in secure condition under critical contingency. Proposed work is carried out on IEEE 14 bus test system using MATLAB.

Keywords Performance index · Critical contingency · Sensitivity analysis
Active power performance index · Voltage performance index

1 Introduction

Transmission line congestion is a severe problem in deregulated power system. Every buyer of electricity wants to get electricity at lower prices from the sellers and as a result of this, transmission line gets overloaded and line congestion occurs

P. Choudekar (✉) · S. Sinha
Amity University, Noida, Uttar Pradesh, India
e-mail: pallaveech@gmail.com

S. Sinha
e-mail: sinha.sanjay66@gmail.com

A. Siddiqui
Jamia Millia Islamia, New Delhi, India
e-mail: anshsi@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_69

in deregulated power systems. Effects of congestion are increase in losses, reduction in system stability and security and making generation pattern uneconomical. Utilization of available power capacity of transmission line is done by installing FACTS devices. By using FACTS devices power loss in heavily loaded lines gets reduced and they increase system loadability and stability of power system is improved.

Some of the works done in this area of research have been highlighted below: Congestion management using transmission congestion distribution factor has been studied and identification of congestion zones is done and congestion is reduced in those zones [1]. Installation of TCSC and reduction in LMPs in the congested lines and maximization of social welfare has been discussed [2]. Multi-objective congestion management gives more accurate results than conventional single objective solution [3]. Differential evolution algorithm is applied for improving power system security under single line outage for reducing congestion and reducing bus voltage deviations [4]. PSO–TVAC is used for optimally placing TCSC for congestion management [5]. Contingencies are ranked using real power flow performance index and line outage distribution factor and TCSC is placed at optimal location for reducing line overloading [6]. Management of congestion using Bee Colony Optimization and cost minimization is also done [7]. In reference [8] congestion relief and voltage stability enhancement in unbundled electricity market has been discussed using multiple FACTS devices. Congestion cost reduction using FACTS devices has been presented in [9]. Sensitivity-based approaches are studied and developed for finding best location of TCSC and its effect on outage of a line to relieve congestion [10]. TCSC optimal location to reduce line overloading under contingencies has been discussed in [11, 12].

Main contribution of the paper are finding of critical contingency (single line outage) by using performance index and determination of congested lines in IEEE 14 bus system. Under this critical line critical line outage condition by placement of TCSCs transmission line congestion is reduced and all transmission line loading are within their rated capacity.

The remaining paper is organized as follows: Sect. 2 gives ranking of critical contingency and in Sect. 3 mathematical model of TCSC is described. Section 4 gives methods to find optimal location of TCSC under critical contingency. Section 5 gives simulation results and discussions for placement of TCSC under critical contingency for congestion management. In Sect. 6 conclusions are drawn from the results obtained.

2 Critical Contingency Ranking

Single line contingency is created in IEEE 14 bus system and most severe contingency is found out by calculating performance index.

Higher the performance index, most severe is the contingency. Performance index is composed of two components.

Active Power Performance Index (PI_P)—This index is useful in finding line overloading

$$PI_P = \sum_{l=1}^{N_l} (W/2n)\left(P_l/P_l^{\max}\right)^{2n} \tag{1}$$

where,

P_l Power flow of line l
$P_l^{\max}$ Rated capacity of line l
N_l Number of transmission lines
W Weighting factor = 1
n Penalty function = 1
$P_1^{\max}$ $(V_m/V_n)/X$
V_m Voltage at bus m
V_n Voltage at bus n
X Transmission line reactance which is connected between bus m and bus n.

Voltage Performance Index (PI_V)—This index is used to find out bus voltage violations.

$$PI_V = \sum_{m=1}^{N_B} (W/2n)\left[\left(|V_m| - \left|V_m^{sp}\right|\right)/\Delta V_m^{\lim}\right]^{2n} \tag{2}$$

$|V_m|$ Magnitude of voltage at bus m
$\left|V_m^{sp}\right|$ Magnitude of voltage specified at bus m
$\Delta V_m^{\lim}$ Limit of voltage violation
n Penalty function
N_B Number of buses
W Real non negative weighting factor = 1

$$\text{Overall Performance index (OPI)} = PI_P + PI_V \tag{3}$$

Outage of transmission line is done one by one and for each line outage load flow is carried out using Newton Raphson method and overall performance index is calculated. OPI is arranged in descending order and line contingency corresponding to highest OPI is severe contingency. Under this critical contingency condition power flow through each line can be observed and it can be seen that three lines gets congested (line 10, line 11, and line 12). Congestion of these three lines can be reduced by placement of TCSCs at optimal location.

From Table 1 it is clear that line 8 outage is critical single line contingency as it has highest overall performance index.

Table 1 Overall performance index for contingency ranking

Bus	Bus	Outage of line	PI_P	PI_V	OPI
1	2	1	11.96615	5.144207	17.11036
1	5	2	11.80216	5.06687	16.86903
2	3	3	11.63671	5.17993	16.81664
2	4	4	11.50231	5.170382	16.67269
2	5	5	11.2733	5.099176	16.37248
3	4	6	11.19228	5.176676	16.36895
4	5	7	12.13195	5.566142	17.69809
6	11	8	8.340626	45.65425	**53.99488**
6	12	9	11.56421	4.909991	16.4742
6	13	10	11.94986	5.053949	17.00381
7	9	11	14.94654	8.528648	23.47519
9	10	12	15.75971	9.252322	25.01203
9	14	13	11.49032	5.033894	16.52422
10	11	14	7.902068	23.40086	31.30293
12	13	15	11.09736	5.250127	16.34748
13	14	16	11.29966	5.649689	16.94935

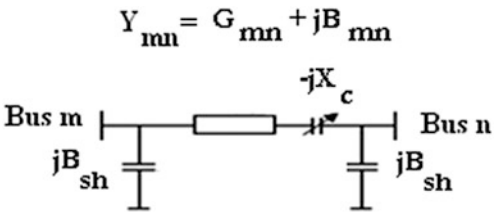


Fig. 1 Transmission line model with TCSC

3 Mathematical Modelling of TCSC

Modelling when TCSC in series with transmission line

A transmission line connected between buses m and n with admittance Y_{mn} is considered in π model. Consider a TCSC with steady state static reactance $-jX_c$ connected in between buses m and n as shown in Fig. 1. The voltages at the buses m and n are $V_m\angle\delta_m$ and $V_n\angle\delta_n$, respectively, and $\delta_{mn} = \delta_m - \delta_n$.

When TCSC is connected in series with transmission line, the real and reactive power flows from bus m to bus n are P_{mn} and Q_{mn}, respectively. These are given by

$$P_{mn} = V_m^2 G_{mn} - V_m V_n (G_{mn}\cos\delta_{mn} + B_{mn}\sin\delta_{mn}) \tag{4}$$

$$Q_{mn} = -V_m^2 (B_{mn} + B_{sh}) - V_m V_n (G_{mn}\sin\delta_{mn} - B_{mn}\cos\delta_{mn}). \tag{5}$$

Similarly, the real and reactive power flows from bus n to bus m are P_{nm} and Q_{nm} respectively. These are given by

$$P_{nm} = V_n^2 G_{mn} - V_m V_n (G_{mn} \cos \delta_{mn} - B_{mn} \sin \delta_{mn}) \tag{6}$$

$$Q_{nm} = -V_n^2 (B_{mn} + B_{sh}) + V_m V_n (G_{mn} \sin \delta_{mn} + B_{mn} \cos \delta_{mn}). \tag{7}$$

where,

$$G_{mn} = \frac{r_{mn}}{r_{mn}^2 + (x_{mn} - x_c)^2} \tag{8}$$

$$B_{mn} = \frac{-(x_{mn} - x_c)}{r_{mn}^2 + (x_{mn} - x_c)^2}. \tag{9}$$

4 Optimal Location of TCSC

Method used for optimal location of TCSC is described in this section.
Sensitivity-based method
Sensitivity index-based technique is used to identify sensitive lines to reduce the reactive power loss, to increase the stability, and to intensify the voltage profile by placing TCSCs.

Reactive power loss sensitivity index (b): It is considered as the partial derivative of the reactive power loss of transmission line with respect to the compensated capacitive reactance (X_{cm}) of the transmission line, it is given by

$$b = \frac{\partial Q}{\partial x_{cm}} = \left(V_m^2 + V_n^2 - 2V_m V_n \cos \delta_{ij}\right) \frac{(r_{mn}^2 - x_{mn}^2)}{(r_{mn}^2 + x_{mn}^2)^2}, \tag{10}$$

where $\delta_{mn} = \delta_m - \delta_n$ and $(r_{mn} + jx_{mn})$ is the impedance of the line before compensation.

TCSC is located in the line which has most positive reactive power loss sensitivity index.

Table 2 shows values of sensitivity index obtained under critical contingency condition (line 8 outage). Optimal location for placing TCSCs are between line 9 to line 10, line 10 to line 11, and line 12 to line 13.

Table 2 Sensitivity index

Bus	Bus	Line	*B*	Bus	Bus	Line	*b*
1	2	1	−1.77979	7	9	11	−1.99644
1	5	2	−1.91977	9	10	12	**−0.7835**
2	3	3	−2.06931	9	14	13	−1.21338
2	4	4	−1.70897	10	11	14	**−0.3973**
2	5	5	−1.73199	12	13	15	**0.21709**
3	4	6	−1.51232	13	14	16	−1.24356
4	5	7	−1.71905	5	6	17	−2.19437
6	11	8	−0.71446	4	9	18	−1.97469
6	12	9	−1.40236	4	7	19	−2.09942
6	13	10	−1.30986	7	8	20	−2.24408

Table 3 Percentage loading under critical contingency condition

Percentage loading of line	Under critical contingency	TCSC placed in line 12 (9–10)	TCSC placed in line 15 (12–13)	TCSC placed in line 12 (9–10) and line 15 (12–13)
12	199	***63***	110	**26.98**
11	137	161	145	**46.56**
10	103	112	***99***	**68.03**

There is significant change in percentage loading by placement of TCSCs, numbers in bold indicates percentage loading under 100%

5 Simulation Results and Discussion

Under critical contingency condition (line 8 outage) three transmission lines (line 10, line 11, line 12) gets overloaded and effect of placement of TCSCs in relieving the transmission lines from overload can be seen.

Optimal location is found out in Sect. 4. From Table 3 it can be seen that if only one TCSC is placed at optimal location and it relieves overloading of only one transmission line, loading of line 10 is reduced from 103 to 99% and other two transmission lines (line 12 and line 11) remains in overloaded condition. But if two TCSCs are placed congestion of all three lines is removed. Loading of line 10 is reduced from 103 to 68.03%, loading of line 12 is reduced from 199 to 26.98% and loading of line 11 is reduced from 137 to 46.56%.

Effect of placement of two TCSCs at optimal location can be seen on improvement in voltage profile and reduction in reactive power loss from following Figs. 2 and 3, respectively.

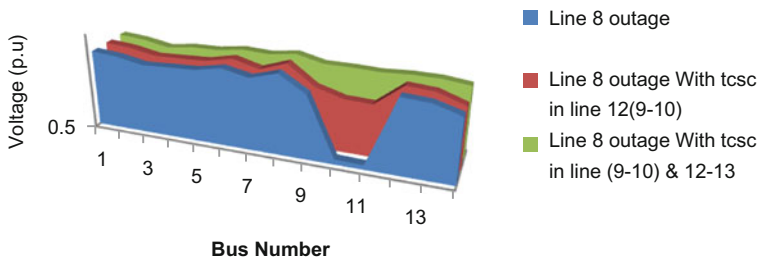


Fig. 2 Voltage profile of buses

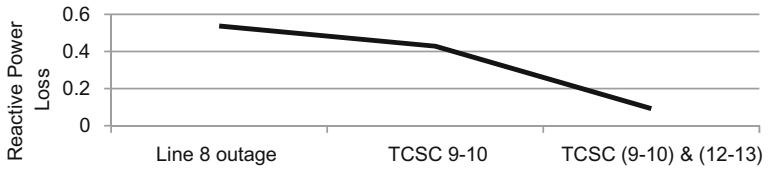


Fig. 3 Reactive power loss

6 Conclusion

Placement of two TCSCs under critical contingency condition is discussed in this paper. Sensitivity-based approach is used for finding optimal location of TCSCs. If we place only one TCSC, congestion of only one line gets removed that is loading of line 10 reduced by 4% and other two lines are still congested. Congestion of all three lines gets removed if we place two TCSCs, loading of line 10 gets reduced by 34.97%, reduction in loading of line 11 by 90.44%, and reduction in line loading of line 12 by 172.02%. Apart from reducing line overloading in critical contingency, reactive power loss of the system and voltage profile have also improved. Results obtained by placing two TCSCs are better than obtained by placing one TCSC.

References

1. Kumar, A., Srivastava, S.C., Singh, S.N.: A zonal congestion management approach using ac transmission congestion distribution factors. Electr. Power Syst. Res. **72**(1), 85–93 (2004)
2. Acharya, N., Mithulananthan, N.: Influence of TCSC on congestion and spot price in electricity market with bilateral contract. Electr. Power Syst. Res. **77**(8), 1010–1018 (2007)
3. Esmaili, M., Shayanfar, H.A., Moslemi, R.: Locating series FACTS devices for multi-objective congestion management improving voltage and transient stability. Eur. J. Oper. Res. **236**(2), 763–773 (2014)
4. Rashed, G.I., Sun, Y.: Optimal placement of Thyristor controlled series compensation for enhancing power system security based on computational intelligence techniques. Procedia Eng. **15**, 908–914 (2011)

5. Mandala, M., Gupta, C.P.: Optimal placement of TCSC for transmission congestion management using hybrid optimization approach. In: International Conference on IT Convergence and Security (ICITCS), pp. 1–5 (2013)
6. Sayyed, A.L., Gadge, P.M., Sheikh, R.U.: Contingency analysis and improvement of power system security by locating series FACTS Devices "TCSC and TCPAR" at optimal location. IOSR J. Electr. Electron. Eng. (IOSR-JEEE). 19–27 (2014)
7. Rahim, M.A., Musirin, I., Abidin, I.Z., Othman, M.M.: Contingency based congestion management and cost minimization using bee colony optimization technique. In: PECon2010—2010 IEEE International Conference on Power and Energy, pp. 891–896 (2010)
8. Lu, Y., Abur, A.: Static security enhancement via optimal utilization of thyristor-controlled series capacitors. IEEE Trans. Power Syst. **17**(2), 324–329 (2002)
9. Kumar, A., Sekhar, C.: Congestion management with FACTS devices in deregulated electricity markets ensuring loadability limit. Int. J. Electr. Power Energy Syst. **46**(1), 258–273 (2013)
10. Besharat, H., Taher, S.A.: Congestion management by determining optimal location of TCSC in deregulated power systems. Int. J. Electr. Power Energy Syst. **30**(10), 563–568 (2008)
11. Wibowo, R.S., Yorino, N., Eghbal, M., Zoka, Y., Sasaki, Y.: FACTS devices allocation with control coordination considering congestion relief and voltage stability. IEEE Trans. Power Syst. **26**(4), 2302–2310 (2011)
12. Singh, S.N., David, A.K.: Optimal location of FACTS devices for congestion management. Electr. Power Syst. Res. **58**(2), 71–79 (2001)

DXCCII-Based First Order Voltage-Mode All-Pass Filter

Ashok Kumar, Ajay Kumar Kushwaha and Sajal K. Paul

Abstract In this article, a new design for realizing voltage-mode (VM) first order all-pass filter (APF) using single dual-X second generation current conveyor (DXCCII), one capacitor, one grounded resistor and one NMOS transistor operating in triode region is presented. The proposed circuit is analyzed for non-ideality presence due to voltage and current tracking errors and also due to parasitic components of the DXCCII to check the effect on functionality of proposed all-pass filter. PSPICE simulation and AD844 analogue IC-based experimental results are included to verify the proposed theory of the circuit.

Keywords Voltage mode · APF · DXCCII · Analogue building block (ABB) Current feedback operational amplifier (CFOA)

1 Introduction

An APF finds wide applications in analogue signal processing circuits. It produces delay of 90° to the applied input waveform while keeping its amplitude constant over the frequency range. In recent years, current mode (CM) circuits using different current conveyor blocks are receiving great attention due to their advantages such as high slew rate, low power consumption, wider signal bandwidth, wide dynamic range and great linearity. Taking into account all these advantages of CM circuits a number of VM and CM first order APF circuits are reported using different high performance active building blocks (ABBs) in the literature [1–6]. Most of the reported circuits employ large number of active and passive compo-

A. Kumar · A.K. Kushwaha · S.K. Paul (✉)
Indian Institute of Technology (ISM), Dhanbad, Dhanbad, India
e-mail: sajalkpaul@rediffmail.com

A. Kumar
e-mail: ashok1987.in@gmail.com

A.K. Kushwaha
e-mail: ajay.igecsagar@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_70

nents with complex passive component matching constraints. The APFs employing second generation current conveyor (CCII) in [1, 2] have floating resistor and employ three or more number of passive elements. The APF circuits reported in [3, 4] has advantage of using grounded resistor but these circuits employ two ABBs and use three or more passive components. In the APF circuit (Fig. 1b) of [5], a passive resistor is replaced by MOS-based electronic resistor and employs grounded capacitor, but uses two active building blocks. Single DXCCII-based APF is reported in [6] but uses three passive elements.

In this article, a new first order VM APF is realized using one DXCCII, one floating capacitor, one resistor and one NMOS transistor working in triode region. In the proposed filter realization simple resistor matching is required. It may be noted that the present integrated circuit (IC) technologies are capable to mach resistors with precision better than 0.1% [7] and these new technologies also offers the feasible designing of floating capacitor as a double poly (poly1-poly2) or metal-insulator-metal (MIM) Capacitor [8]. The proposed theory and results are validated using SPICE simulations and performance of the APF circuit is also experimentally verified through commercially available current feedback operational amplifier (CFOAs) AD844 ICs.

2 The DXCCII

The symbol of DXCCII [9] and its internal CMOS structure is given in Fig. 1. It is a combination of regular CCII and inverting current conveyor (ICCII). It has two X ports (X_n and X_p) with current conveying to the respected Z ports (Z_n and Z_p). As

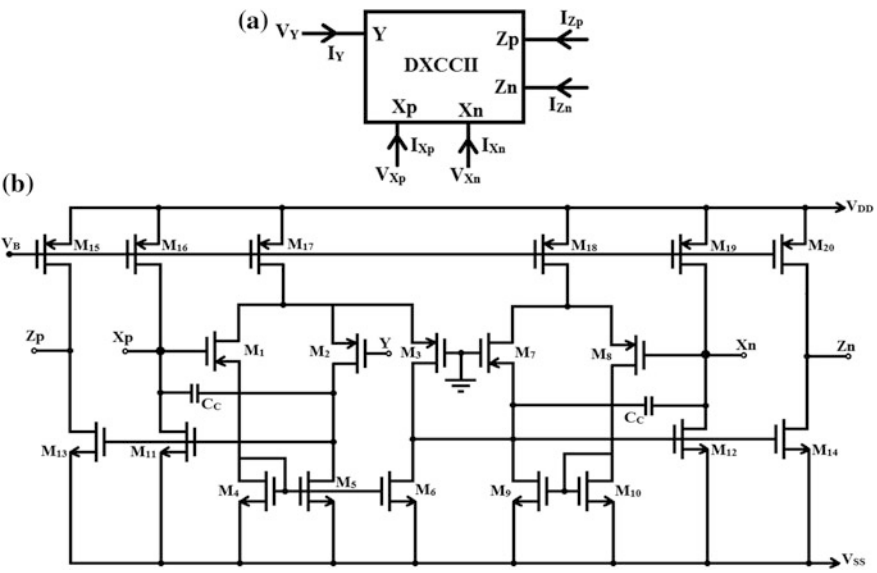


Fig. 1 DXCCII **a** symbol **b** CMOS structure

in all CCII topologies, Y and Z ports are high input impedance while X port is low impedance. The ideal equation of the DXCCII can be present by the given matrix

$$\begin{bmatrix} I_Y \\ V_{Xp} \\ V_{Xn} \\ I_{Zp} \\ I_{Zn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_Y \\ I_{Xp} \\ I_{Xn} \end{bmatrix}. \tag{1}$$

3 Proposed Filter Circuit

The proposed first order VM APF using single DXCCII, one capacitor, and one grounded resistor is given in Fig. 2. The analyzing the circuit of Fig. 2 results transfer function expressed as

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{S - 2/CR_M}{S + 1/RC}, \tag{2}$$

where R_M is MOS resistance and can be expressed as

$$R_M = \left[\mu_n C_{\text{ox}} \left(\frac{W}{L}\right)(V_G - V_T)\right]^{-1}.$$

Considering $R_M = 2R$, (2) reduces to

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{S - 1/RC}{S + 1/RC}. \tag{3}$$

The all-pass filter exhibited from (3) has pole frequency

$$\omega_o = \frac{1}{RC}. \tag{4}$$

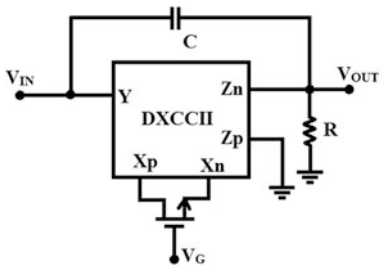


Fig. 2 The proposed VM APF

The phase of the APF is computed as

$$\angle\phi = \pi - 2\tan^{-1}\omega RC. \tag{5}$$

The pole-ω_o sensitivities for the filters of (2) with respect to components can be expressed as

$$S_{R,C}^{\omega_o} = -1 \quad \text{and} \quad S_{R_M}^{\omega_o} = 0. \tag{6}$$

From (6), it is found that passive components sensitivities of pole-ω_o are small and maximum magnitude is unity.

4 Non-ideal Analysis

The DXCCII introduces non-ideality due to deviation of voltage (current) transfer gain and also due to development of parasitic components. Discussion of both the types of non-ideality on all-pass filter is discussed in this section.

4.1 Voltage (Current) Transfer Non-ideality

The matrix equation defining a non-ideal DXCCII due to voltage (current) transfer may be given as

$$\begin{bmatrix} I_Y \\ V_{Xp} \\ V_{Xn} \\ I_{Zp} \\ I_{Zn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta_p & 0 & 0 \\ -\beta_n & 0 & 0 \\ 0 & \alpha_p & 0 \\ 0 & 0 & \alpha_n \end{bmatrix} \begin{bmatrix} V_Y \\ I_{Xp} \\ I_{Xn} \end{bmatrix}, \tag{7}$$

where $\beta_p\,(\beta_n)$ are the voltage transfer gains from the Y port to $X_p\,(X_n)$ ports and $\alpha_p\,(\alpha_n)$ are the current transfer gains from the $X_p\,(X_n)$ port to the $Z_p\,(Z_n)$ ports (ideally, there voltage and current transfer gains are unity in magnitude).

The analyzation the circuit of Fig. 2 using (7) gives the following non-ideal transfer function.

$$\frac{V_{\text{OUT}}}{V_{\text{IN}}} = \frac{\left(S - \frac{\alpha_n(\beta_p + \beta_n)}{CR_M}\right)}{\left(S + \frac{1}{RC}\right)} \tag{8}$$

It is clearly shown that the all-pass filter is affected by non-ideality of DXCCII, however its intensity depends on the deviation of voltage transfer gain β_p (β_n) and current transfer gain (α_n) from ideal value.

4.2 Parasitic Components Non-ideality

Effect of parasitic involved with DXCCII current conveyor is discussed. The parasitic associated with the DXCCII is given in Fig. 3. The various parasites involved with the DXCCII are as follows: a small parasitic resistances R_{Xp} and R_{Xn} at X_p and X_n ports respectively, parasitic $(C_Y//R_Y)$ at Y port and parasitic $(C_{Zp}//R_{Zp})$ and $(C_{Zn}//R_{Zn})$ at Z_p and Z_n ports, respectively.

Practically it is assumed that external resistance has much smaller value than the parasitic resistance at the Y, Z_p and Z_n ports of the DXCCII, hence input voltage at Y port will be approximately same as that of source signal.

The transfer function obtained using above approximation is as

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = \left(\frac{C}{C + C_{Zn}}\right)\left(\frac{S - 2/CR'_M}{S + 1/R'(C + C_{Zn})}\right), \tag{9}$$

where $R'_M = \left(R_M - R_{Xp} - R_{Xn}\right)$ and $R' = R//R_{Zn}$.

The (9) clearly indicates that the all-pass filter will be affected due to parasites. However, the effect of parasites may be neglected if

(i) R_M is adjusted to a value which is considerably greater than R_{Xp} and R_{Xn} such that $R'_M \cong R_M$.
(ii) if R is adjusted to a value such that $R//R_{Zn} \cong R$, as $R_{Zn} \gg R$ and
(iii) the external capacitor C is taken much higher than C_{Zn} such that $C + C_{Zn} \cong C$.

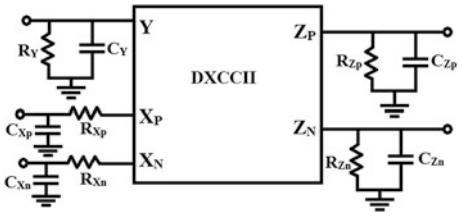


Fig. 3 Parasitic model of the DXCCII

Table 1 MOSFET dimensions of the DXCCII

MOS transistors	$W/L(\mu m)$
M_1, M_2, M_4, M_5, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{20}	2/0.25
M_3, M_6, M_7, M_8, M_9, M_{10}	4/0.25
M_{11}, M_{12}, M_{13}, M_{14}	16/0.25

5 PSPICE Simulation Results and Discussion

To validate the proposed theory, the first order VM APF in Fig. 2 is simulated by SPICE programme uses 0.25 µm TSMC level-three technology parameters. The aspect ratio of the MOSFETs is given in Table 1. The DC power supply voltages are taken as $V_{DD} = -V_{SS} = 1.25\,V$, $V_B = -0.3\,V$. Aspect ratio of triode MOS is W/L = 0.5 µm/0.25 µm and gate voltage is kept at 1.08 V. The proposed all-pass is designed for a pole frequency f_0 = 2.36 MHz taking C = 45 pF, R = 1.5 KΩ and triode MOS resistance 3 KΩ. The phase and magnitude responses of APF are shown in Fig. 4. The transient response of the proposed APF shown in Fig. 5 is acquired by applying a sine wave of 100 mV amplitude at 2.36 MHz. The output

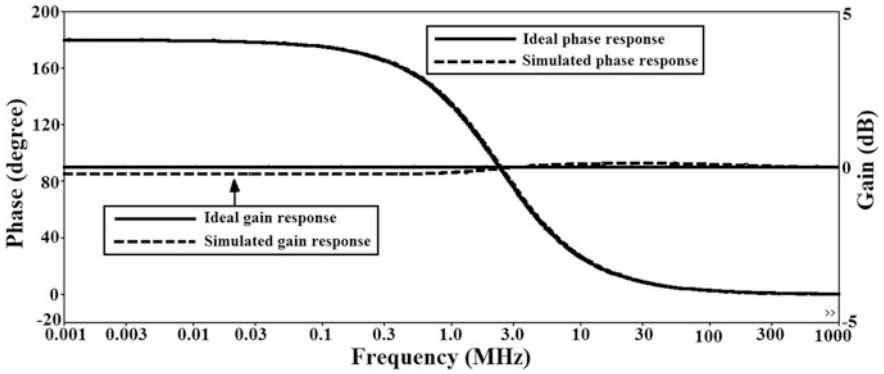


Fig. 4 Phase and gain responses of APF

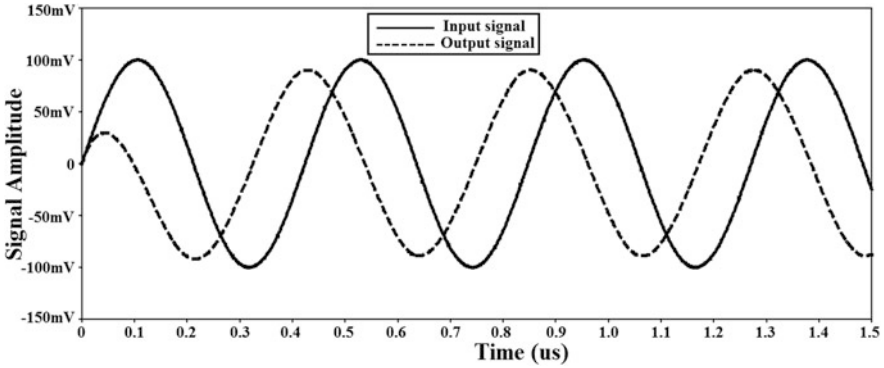


Fig. 5 Time-domain response of the proposed APF

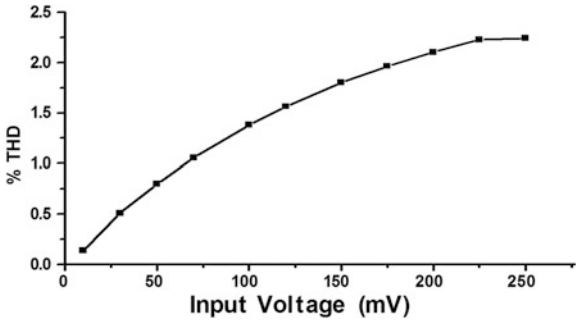


Fig. 6 %THD variation of APF with input voltage signal at 2.36 MHz

phase shift is 89°, which corresponds effectively with the theoretical value of 90°. The %THD of VM APF for a wide range of signal amplitude is presented in Fig. 6 and is found below 2.3% upto an amplitude of 250 mV.

6 Experimental Results and Discussion of the Proposed APF

The behaviour of the APF circuit is experimentally demonstrated using a hardware commercially available ICs. Commercially available CFOAs (AD844s) is employ to implement DXCCII [10]. As exhibit in Fig. 7, four AD844 ICs and two passive resistor are used for designing a DXCCII. The proposed all-pass filter is assembled on a bread board using IC AD844, $C = 2$ nF (series combination of 1 nF) and $R = 680\ \Omega$ for a pole frequency of 117.1 kHz. The DC power supplies are taken as ± 10 V.

Transient response of the APF circuit is presented in Fig. 8 with a 89.6° phase difference between the applied sinusoidal input and resultant output signal waveforms. Figure 9 shows the phase quadrature relationship between the input and output signals in *X*-*Y* mode, which confirms about 90° phase shift between the voltage input and resultant output signal. The measured frequency found to be is 108.7 kHz which is closed to the designed value of 117.1 kHz. The deviations of

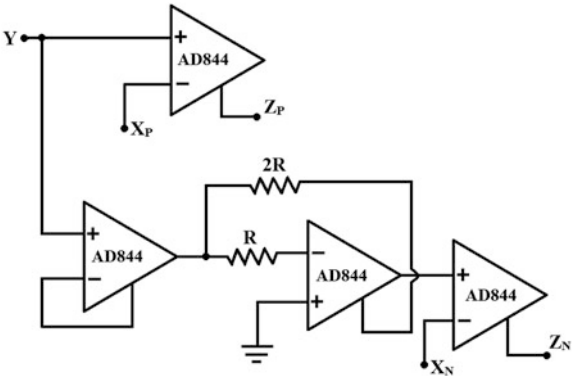


Fig. 7 DXCCII realization using AD844

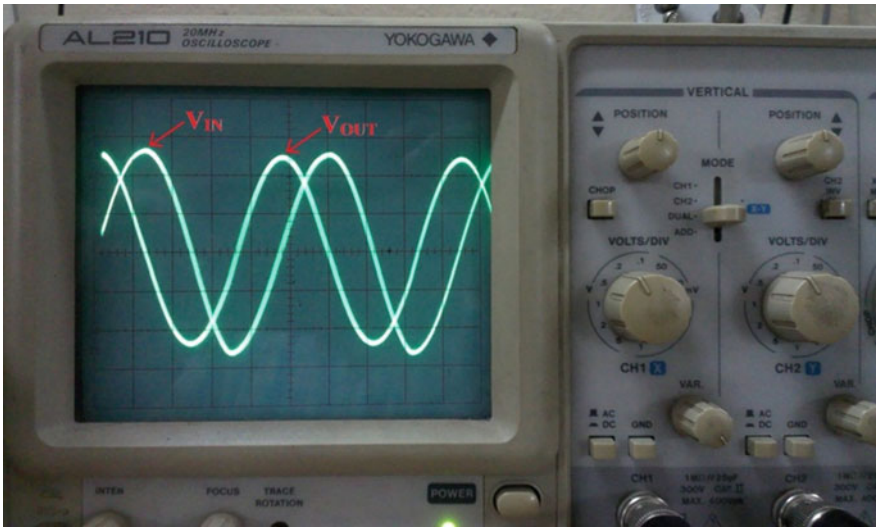


Fig. 8 Experimental quadrature signals of proposed APF (horizontal and vertical scales are 2 μs/div and 0.2 V/div, respectively)

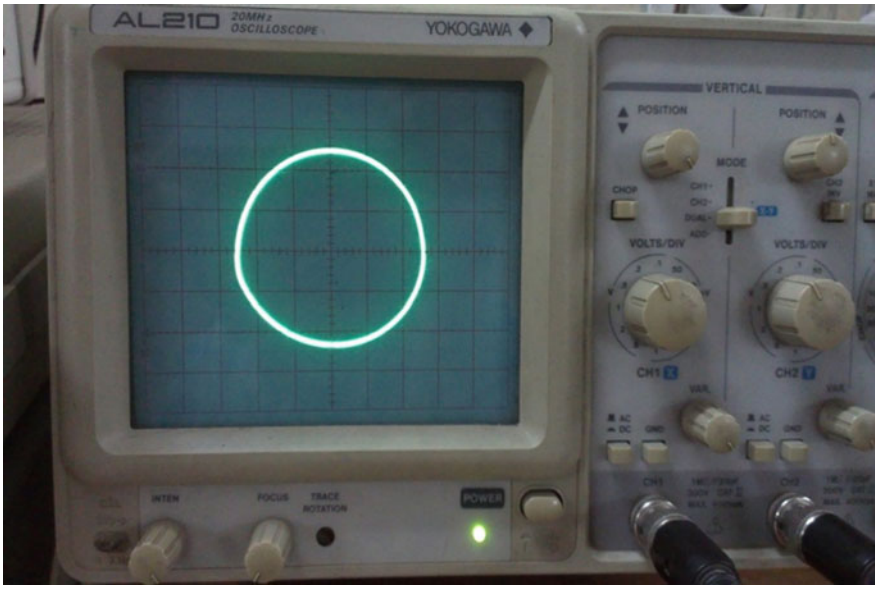


Fig. 9 Lissajous figure of APF in *X-Y* mode (horizontal and vertical scales are 0.2 V/div)

the experimental pole frequency may be attributed due to the parasitic associated with IC AD844 and passive component tolerance of 2 and 5% for capacitor and resistor respectively, used for circuit designing.

7 Conclusion

A first order VM APF using one DXCCII, one capacitor, resistor and NMOS each has been presented. Proposed filter employs less number of active and passive elements. Calculated %THD is found very low for wide range of applied signal amplitude. Active and passive sensitivities are found small and unity in magnitude. The PSPICE simulation results agree well with the predicted theory. Prototype circuit is implemented using commercially available CFOA IC AD844s to verify the theoretical results.

References

1. Higashimura, M., Fukui, Y.: Realization of current mode all-pass networks using a current conveyor. IEEE Trans. Circuits Syst. **37**, 660–661 (1990)
2. Pandey, N., Paul, S.K.: All-pass filters based on CCII– and CCCII–. Int. J. Electron. **91**, 485–489 (2004)
3. Ibrahim, M.A., Minaei, S., Yuce, E.: All-pass sections with high gain opportunity. Radioengineering **20**, 3–9 (2011)
4. Maheshwari, S.: High input impedance voltage-mode first-order all-pass sections. Int. J. Circuit Theory Appl. **36**, 511–522 (2008)
5. Metin, B., Pal, K., Cicekoglu, O.: All-pass filters using DDCC- and MOSFET-based electronic resistor. Int. J. Circuit Theory Appl. **39**, 881–891 (2011)
6. Minaei, S., Yuce, E.: Unity/variable-gain voltage-mode/current-mode first-order all-pass filters using single Dual-X second-generation current conveyor. IETE J. Res. **56**, 305–312 (2010)
7. Gray, P.R., Meyer, R.G.: Analysis and Design of Analog Integrated Circuits, pp. 451–452. Wiley, New York (1993)
8. Baker, R.J., Li, H.W., Boyce, D.E.: CMOS Circuit Design, Layout, and Simulation (Chapter 7). IEEE Press, New York (1998)
9. Zeki, A., Toker, A.: The dual-X current conveyor (DXCCII): a new active device for tunable continuous-time filters. Int. J. Electron. **89**, 913–923 (2002)
10. Maheshwari, S., Ansari, M.S.: Catalog of realizations for DXCCII using commercially available ICs and applications. Radioengineering **21**, 281–289 (2012)

Performance Analysis of High Power Brushless DC Motor Drive

R. Babu Ashok and B. Mahesh Kumar

Abstract Brushless motors are replacing most of the conventional application that were driven by induction motors in recent times. This is majorly due to the advancement and the proliferation of control techniques for the operation of such machines. The critical choice in electric vehicle applications is on the capability of motoring and generative characteristics. These types of machines are viable candidate as with its extended constant power range operation replacing the conventional multi-gear transmission. However, the major challenges in such type of machines is twofold, one with the cogging force generated in the operation mainly due to the magnetic orientation of the machine and the second one due to the switching ripple significantly increase the ripple content in the machine. In this paper, the performance of the 5 kW BLDC machine used for electric vehicle operation is reported in terms of torque and current characteristics.

Keywords BLDC · Dual magnetic circuit · Generative · Electric vehicle
Motor constant square density

1 Introduction

Three phase Brushless DC machine (BLDC) is finding major applications in recent times for commercial and industrial applications. However, the presence of cogging torque heavily due to the rotational magnetic forces is a daunting challenging. Cogging is addressed in two ways one with the machine design structure and through the control aspects the harmonic could be controlled. The lower the cogging torque produced, the better the torque performance of the motor. Thus,

R. Babu Ashok (✉) · B. Mahesh Kumar
Electrical & Electronics Engineering, Pondicherry Engineering College,
Pondicherry 605014, India
e-mail: babuashok69@gmail.com

B. Mahesh Kumar
e-mail: maheskumarpec@yahoo.co.in

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_71

reduction of cogging torque is critical for improved performance. BLDC motors work by exciting the 3 phase coil and when the magnet reaches the first phase, the second phase is excited and pulls the motor to the next phase. This process is repeated from phase 1 to other phase to produce a full revolution of the motor. The structure of brushless motors is quite similar to the permanent magnet synchronous motor. However, the sensor to detect the rotor position or magnetic poles to produce signals in order to control the electronic switches is required for its operation, commonly Hall sensor [1–8].

2 Design Challenges and Approach to Mitigate

2.1 Design Approaches

There are two ways to approach the reduction in cogging value and the ripple reduction. One way to mitigate the cogging is the structural approach in the magnetic circuit control design that can produce the reduced cogging value. The second approach is through the use of advanced control logic in the operational of the power electronic circuit that operates the machines. A number of parallel researches on both of the approaches are made in the literature.

2.2 Structural Variations

The idea of Integrated Permanent Magnet Hybrid Brushless Motor Drive is mainly focused and designed based on the requirement for EV application [9]. The major criteria of EV motor drives, namely high power density, high efficiency and wide speed range are being emphasized for designing the machine. However, the flexibility of the field control results in field weakening during high speed rotation. Hence, these design suitable only for constant power EV application. Consequent-Pole Permanent Magnet (CPPM) machine specialized in control of field weakening without demagnetizing the permanent magnets. The design structure provides a wide range of air gap flux linkage by cutting the magnetic flux generated from the armature conductor and built-in permanent magnet in the rotor. However, due to the extra iron losses caused by this flux configuration, the heat dissipation is high [10].

2.3 Switching Approaches

From the controller side the current pose major menace from motor side (speed and torque ripple) and converter side power quality issues [11]. The PQ converters are

broadly classified as. Unidirectional and Bi directional converters are further sub divided into Boost, Buck, Buck-Boost, multilevel and multi-pulse. These converters are multimillion dollar growing industry in the field of power electronics. Buck-Boost converter is preferred in this paper which is versatile for all applications and also owing to several advantages. This Buck-Boost is operated either in continuous conduction mode (CCM) or Discontinuous conduction mode (DCM) [12]. In CCM either load current or capacitor voltage is continuous. It requires two sensors one at supply voltage and the other at dc link voltage, matching for high power applications. DCM is generally preferred because it has only one sensor at dc link voltage hence cost effective four switches. Three phase inverter replaces six switch 3 phase Inverter. Moreover, the DC link voltage changes at fundamental frequency results in reduced switching losses. A reduced harmonic machine with reduced cogging and an additional filter design would make the drive to be more efficient. Filter size is inversely proportional to the order of the harmonics and the performance of the machine is first hand improved through design optimization [13].

3 Structural Configurations

The structure of the studied brushless DC motor is shown in Fig. 1. The motor torque can be expressed as shown in Eq. (1)

$$T = kIB \tag{1}$$

where

T Motor torque [Nm]
I Current in the conductors [A]
B Average flux density [T]
k Machine constant

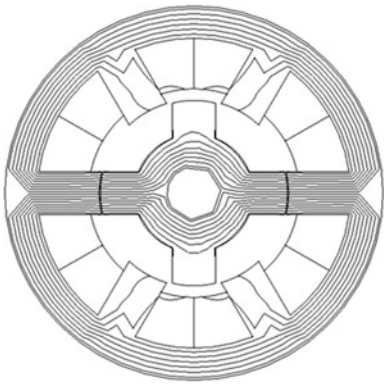


Fig. 1 Conventional BLDC machine (IPM configuration)

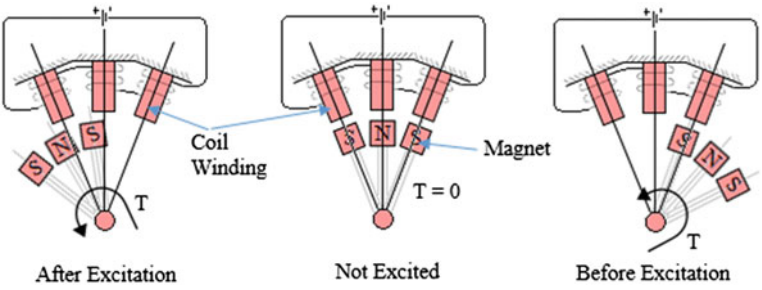


Fig. 2 Excitation as the rotor poles moves

Figure 2 shows the operating principles in the various positions of operation of the machine. Torque producing point is the resultant of air gap flux linkage, as it is the main factor to the rotation of the machine. To produce torque for the machine, first phase is injected current to generate magnetic flux linkage from the excited stator pole and permanent magnets. The rotor then rotates in the direction which minimizes the opposing air gap flux linkage. As the opposing air gap flux linkage for first phase is at minimum, the next phase is excited sequentially and continued operation. The position poles must be at unaligned position to avoid the effect of magnetic locking. Figure 3 shows the interaction position in the operation in the motoring and regenerating modes of operation. Figure 4 shows the inductance characteristics in both modes.

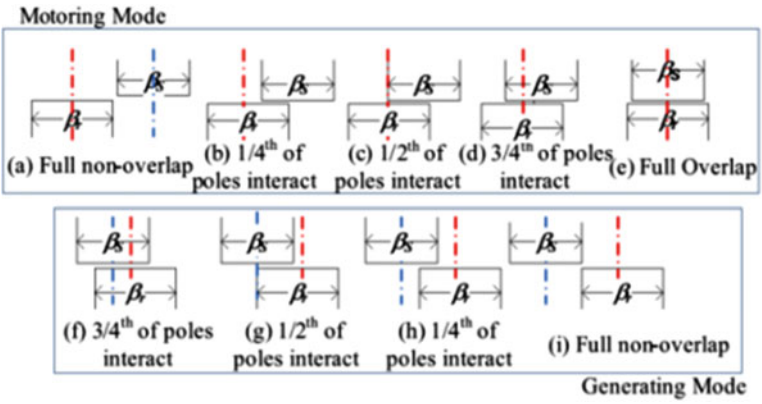


Fig. 3 Motoring and regenerating modes

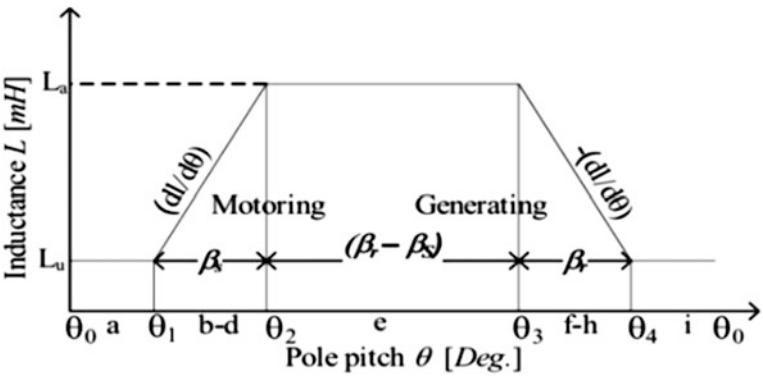


Fig. 4 Inductance profile for the entire operating range

4 Experimental Design

A 5 kW Electric Vehicle used for this research design. This machine is modelled in FEA, optimized for reduced cogging and then brought to MATLAB/SIMULINK to design the controller with reduced ripple. The approach used in this work is as shown in Fig. 5. The designed machine is optimized for structural variations so that the new variation in the machine design is derived. Using the real time simulation in-hardware loop the motor is modelled as a Simulink block in order to develop an appropriate controller. This method is the new approach and would bring the machine design and the power electronic systems together and thereby industry

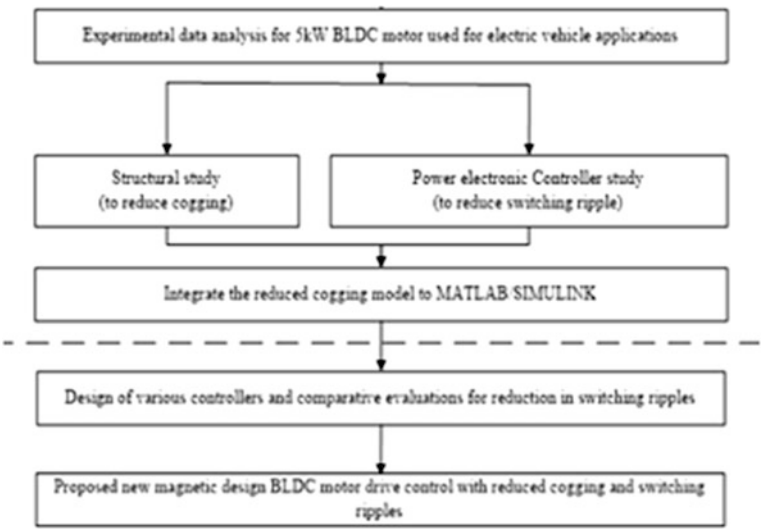


Fig. 5 Approach used in this research

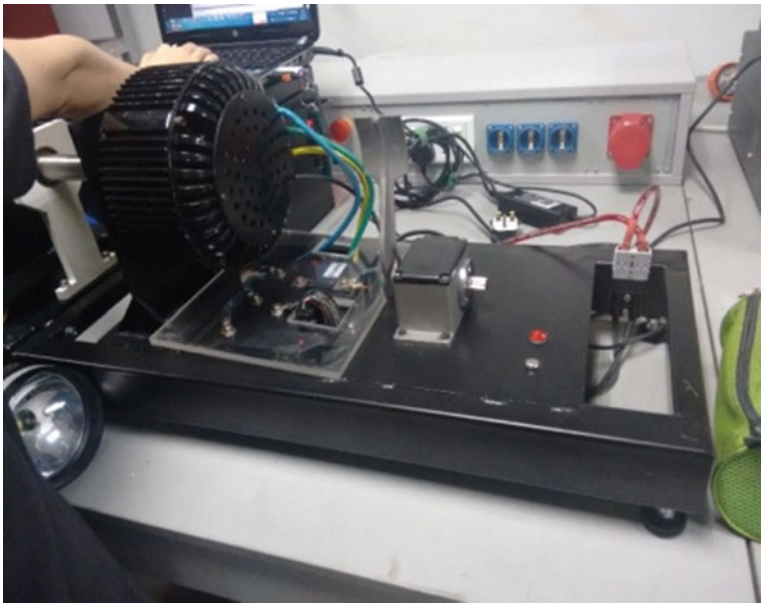


Fig. 6 5 kW experimental machine used for analysis

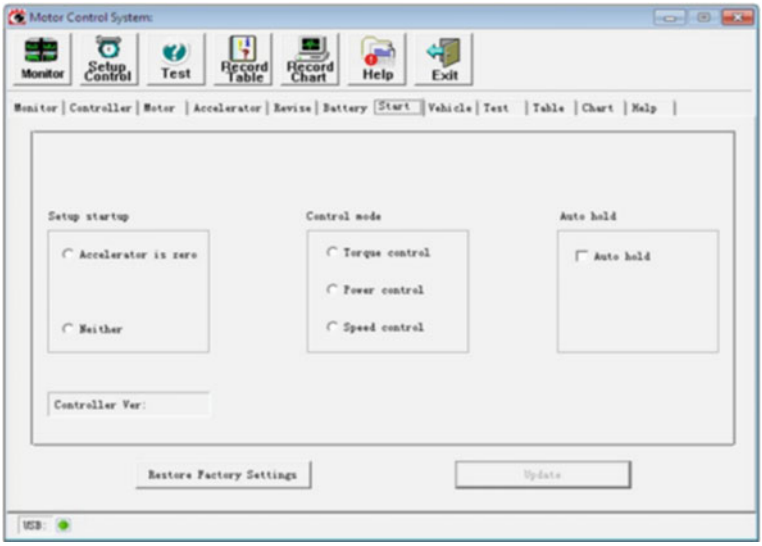


Fig. 7 Data logging interface for the experimental bed

specified machine can be developed. Figure 6 shows the practical experimental model used in this analysis. Figure 7 shows the operational interface used for data logging as shown in Fig. 8.

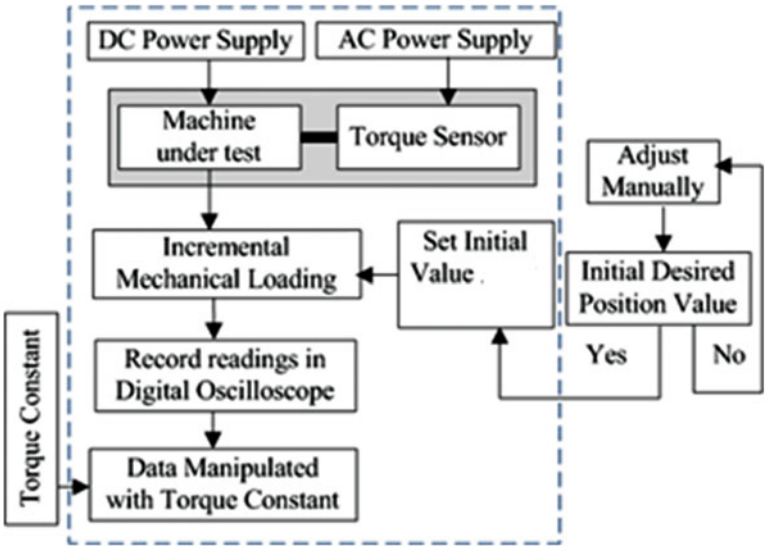


Fig. 8 Experimental procedure block diagram

5 Results and Discussions

The excitation state is based on the position of switches relative to that of the position of the rotor. Figure 9 shows the three phase drive circuit used in this analysis. Table 1 shows the measured electro-mechanical characteristic value of the experimentations.

Figure 10 shows the current variations with respect to the change in speed. As the speed reaches the rated values the current starts to stabilize and start drooping the voltage value and reduction in the operation of the machine. The maximum current is 80 A value and the voltage is 72 V for each of the inverter drive used for this machine in motoring mode. Figure 11 shows the torque characteristics of the machine as the machine is subjected for incremental load variations. This is required to find the torque values at each of the position to determine the operating torque under static conditions. Figure 12 shows the speed torque characteristics of the machine. As can be seen by 1000 rpm the machine is start drooping of torque, the point at which the power is stabilizing with respect to the load. This information is highly handy when the machine modelled later in the modelling tool need to be verified.

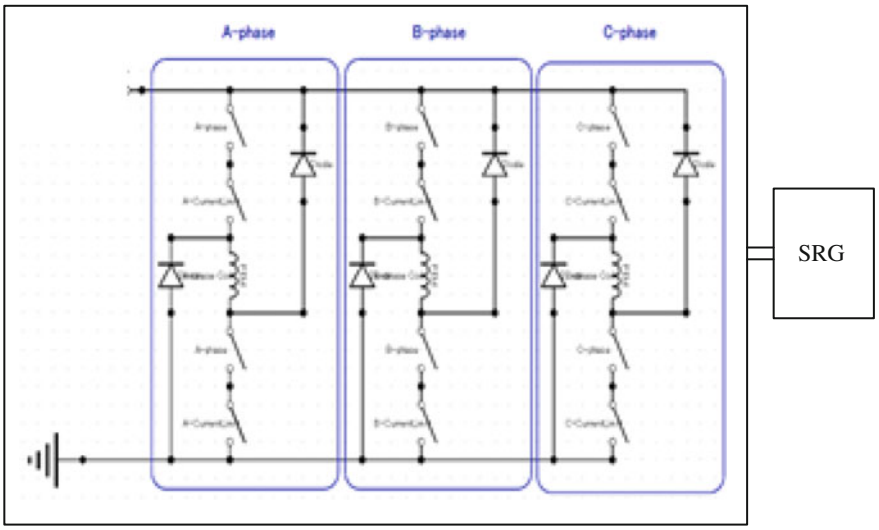


Fig. 9 Drive switching used

Table 1 Elecro-mechanical measured values

Speed (RPM)	Voltage (V)	Current (A)
0	48.0	0.1
563	47.6	2.1
1111	47.1	4.2
1538	47.6	6.0
2000	46.4	8.1
2500	45.8	11.2

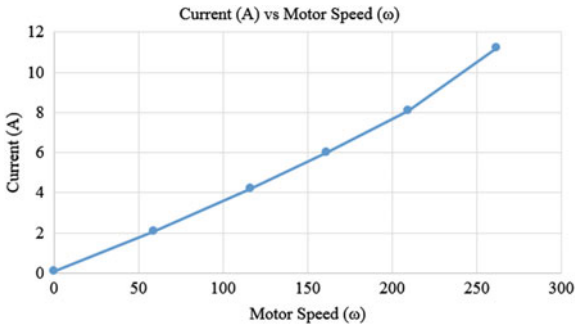


Fig. 10 Current speed characteristics

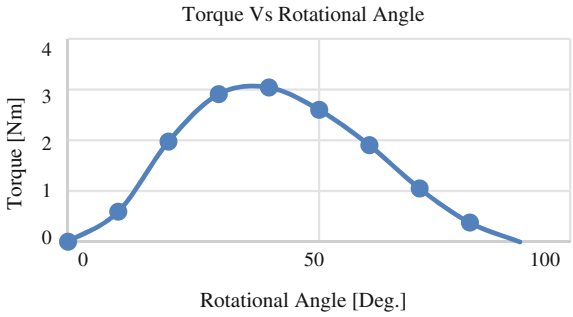


Fig. 11 Static torque characteristics

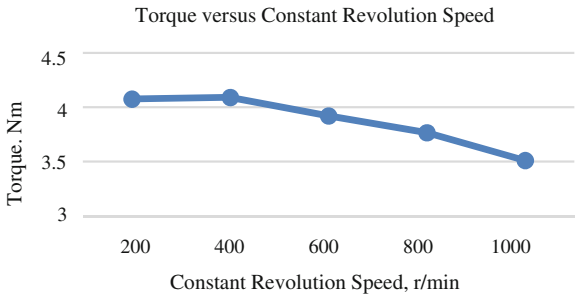


Fig. 12 Constant speed operating range characteristics

6 Conclusions

An integrated approach of FEA for cogging torque reduction with MATLAB/SIMULINK model for controller optimization approach is also introduced in this work and this is expected to be the future direction of research in modern electrical machine design. In order to develop an integrated approach of machine control for electric vehicle the BLDC machine is chosen. An experimental machine is tested for its operational characteristics and the results are presented in this work. A peak torque of 3.2 Nm under static conditions is setup. The table of data of the experimental design is to be evaluated with that of the machine model to be developed using the FEA tool which will be subsequently presented.

References

1. Aravind, C.V., Huai, H.P., Jagadeeswaran, A.: Design analysis of electrical machines through integrated numerical approach. J. Eng. Sci. Technol. 131–142 (2015) (Special Issue 1 on the fourth eureca 2015)
2. Lindstrom, J.: Development of an experimental permanent-magnet motor drive, vol. Licentiate, no. 312L (1999)

3. Jagadeeshwaran, A., Vijayshankar, S., Kannan, N., Aravind, C.V.: Limited angle BLDC for scan mirror application in space satellite system. IEEE Aerosp. Electron. Syst. Mag. **31**(6), 24–32 (2015). doi:10.1109/MAES.2016.160015
4. Seo, I.M., Kim, H.K., Hur, J.: Design and analysis of modified spoke type BLDC motor using a ferrite permanent-magnet. In: Electrical Machines and Systems (ICEMS), 2014 17th International Conference on, Hangzhou, pp. 1701–1705 (2014)
5. Anjum, Z., Aravind, C.V., Sulaiman, E., Shahrukh Adnan, K.: Application of halbach magnet array in designing a permanent magnet synchronous machine. Int. J. Control Theory Appl. **9** (5), 2835–2842 (2016)
6. Salehifar, M., Salehi Arashloo, R., Moreno-Eguilaz, M., Sala, V., Romeral, L.: Observer-based open transistor fault diagnosis and fault-tolerant control of five-phase permanent magnet motor drive for application in electric vehicles. IET Power Electron. **8**(1), 76–87 (2015)
7. Aravind Vaithilingam, C.: Design and development of double rotor switched reluctance motor using magnetic circuit analysis. Ph.D. thesis, University Putra Malaysia, Malaysia, pp. 40–186 (2013)
8. Aravind, C.V., Saja, A., Vijayshankar: Design evaluations of the double rotor switched reluctance machine. J Eng. Sci. Technol. 16–26 (2015) (Special Issue 1 on the fourth eureca 2015)
9. Chau, K.T., Zhang, D., Jiang, J.Z., Liu, C., Zhang, Y.: Design of a magnetic-geared outer-rotor permanent-magnet brushless motor for electric vehicles. IEEE Trans. Magn. **43**(6), 2504–2506 (2007)
10. Aravind, C., Kamalinni, S.T., Jagadeeswaran, A., Firdaus, R.: Design analysis of MAGLEV-VAWT with modified magnetic circuit generator. In: Electrical Energy Systems (ICEES), IEEE 2nd International Conference on, Chennai, 2014, pp. 82–86 (2014). doi:10.1109/ICEES.2014.6924146
11. Singh, B., Singh, S.: Single-phase power factor controller topologies for permanent magnet brushless dc motor drives. IET Power Electron. **3**(2), 147–175 (2010)
12. Motegi, S.I., Maeda, A.: A single-phase buck–boost PFC converter with output-voltage, ripple-reducing operation. Electr. Eng. **126**(2), 56–70 (1999)
13. Aravind, C.V., Kamalinni and Firdaus R.N: Design and development of a novel outer rotor internal permanent magnet synchronous generator. J. Eng. Sci. Technol. 60–70 (2015) (Special Issue in eureca 2014)

Design and Fabrication of Scale-Down Model of 620 MVA, 275 kV Transmission Line

Akash Deep Mukhia, Anwesh Gautam, Suyog Pradhan and Sandip Kumar Gupta

Abstract In this paper a 620 MVA, 275 kV and 400 km transmission line is scaled down to 0.5 kVA, 230 V and 400 km transmission line keeping the per unit values of actual system and scale-down system same. The current carrying capacity of the scale-down system is kept 3A and can be used where single-phase supply is available. The scale-down model of the actual system is fabricated using Pi model in sections of 50 km length. The result of fabricated model is also validated using Simulink simulation. The developed model can be used to determine the *ABCD* parameter of transmission line which is same for actual system and scale-down model. In future any kind of laboratory model of FACTS devices can be connected to the developed model for practical purposes and study the dynamic performance of transmission line.

Keywords Modeling of transmission line · Scale down model of transmission line · Short circuit test and open circuit test · *ABCD* parameter

1 Introduction

Transmission line is the backbone of power system, as transmission line is used to transmit the generated power from the place of generation to the place of consumption. Therefore it is of substantial importance for a power system engineer to

A.D. Mukhia · A. Gautam · S. Pradhan · S.K. Gupta (✉)
Electrical and Electronics Department, Sikkim Manipal University, Gangtok, Sikkim, India
e-mail: sandipgupta_nh@yahoo.co.in

A.D. Mukhia
e-mail: akashdeepmukhia@gmail.com

A. Gautam
e-mail: anvexg123@gmail.com

S. Pradhan
e-mail: suyogpradhan11@gmail.com

A. Garg et al. (eds.), *Advances in Power Systems and Energy Management*, Lecture Notes in Electrical Engineering 436,
https://doi.org/10.1007/978-981-10-4394-9_72

be thorough with mathematical modeling. The *ABCD* parameter of the transmission line provides the link between the supply and receiving end voltages and currents. *ABCD* parameters are extensively used for determining the performance analysis of a transmission line under different conditions. Chavan et al. [1] have developed the model of transmission line but the detailed modeling is not explained. In this paper the authors have provided the mathematical details of modeling of scale-down transmission line for laboratory purpose using per unit system. The authors have also depicted the application of per unit system in mathematical modeling and analysis. The developed model can be used for various transient and steady-state analysis related to transmission line. The developed model can be used for studying different VAR compensation technique and different FACTS devices can be connected to the developed model for analysis.

2 Parameter Estimation

To determine the values of resistance (R), inductance (L) and capacitance (C) of scale-down model of transmission line per unit values of R, L and C of actual system is determined from the provided data in the literature [2, 3]. Using the per unit values of the actual system and base impedance of scale-down model R, L and C values of scale-down model is determined and the calculation of which is given as follows:

Resistance of the actual system R is 0.0345 Ω/km.
Inductive reactance X_L of actual system is 0.323 Ω/km.
Shunt admittance Y_C of actual system is 9.52 μS/km.

$$R^{\text{actual}} = 0.034\ \Omega/\text{km}$$
$$X_L^{\text{actual}} = 0.323\ \Omega/\text{km}$$
$$X_L^{\text{actual}} = 2\Pi fL$$
$$L^{\text{actual}} = \frac{1}{2\Pi f} = \frac{0.323}{2 \times 3.14 \times 50} = 0.001\ \text{H/km}$$
$$Y_c^{\text{actual}} = 9.52\ \mu\text{S/km}$$
$$Y_c = \frac{1}{X_c}$$
$$X_c^{\text{actual}} = \frac{1}{Y_c} = \frac{1}{9.52 \times 10^{-6}} = 105042.0168\ \Omega/\text{km}$$
$$X_c^{\text{actual}} = \frac{1}{2\Pi fC}$$
$$C^{\text{actual}} = \frac{1}{2\Pi X_c} = \frac{1}{2 \times 3.14 \times 50 \times 105042.0168} = 30.30\ \mu\text{F/km}$$

Per unit values of actual system

$$R_{\text{pu}} = \frac{R^{\text{actual}}}{Z_{\text{base}}} = \frac{0.034}{121.975} = 2.824 \times 10^{-4}\text{pu}$$

$$X_{L\text{pu}} = \frac{X_L^{\text{actual}}}{Z_{\text{base}}} = \frac{0.323}{121.975} = 2.6 \times 10^{-3}\text{pu}$$

$$L_{\text{pu}} = \frac{L^{\text{actual}}}{Z_{\text{base}}} = \frac{0.001}{121.975} = 8.19840 \times 10^{-4}\text{pu}$$

$$Y_{C\text{pu}} = \frac{Y_C^{\text{actual}}}{\frac{1}{Z_{\text{base}}}} = \frac{9.52 \times 10^{-6}}{121.975} = 1.16 \times 10^{-3}$$

$$C_{\text{pu}} = \frac{C^{\text{actual}}}{Z_{\text{base}}} = \frac{30.30\ \mu\text{F}}{121.975} = 2.484 \times 10^{-10}\text{pu}$$

Parameter estimation of scale-down model.
Scale-down model is designed for single-phase system of 0.5 kVA, 230 V.
Base Impedance of scale down model

$$\begin{aligned} Z_{\text{base}}^{\text{Scale Down}} &= (\text{kV})^2/\text{MVA} \\ &= (0.23)^2/0.0005 \\ &= 105.8 \end{aligned}$$

$$\begin{aligned} \text{Scale down } R &= R_{\text{pu}} \times Z_{\text{base}}^{\text{Scale Down}} \\ &= 2.828 \times 10^{-4} \times 105.8 \\ &= 0.029\ \Omega/\text{km} \end{aligned}$$

$$\begin{aligned} \text{Scale Down } X_L &= X_{L\text{pu}} \times Z_{\text{base}}^{\text{Scale Down}} \\ &= 2.6480 \times 10^{-3} \times 105.8 \\ &= 0.280\ \Omega/\text{km} \end{aligned}$$

$$\begin{aligned} \text{Scale Down } Y_C &= Y_{C\text{pu}} \times \left(1/Z_{\text{base}}^{\text{Scale Down}}\right) \\ &= 1.16 \times 10^{-3} \times (1/105.8) \\ &= 10.964\ \mu\text{S/km} \end{aligned}$$

$$\begin{aligned} \text{Scale Down } L &= X_{L\text{pu}}/(2\Pi f) \\ &= 0.280/(2 \times 3.14 \times 50) \\ &= 0.891\ \text{mH/km} \end{aligned}$$

$$\begin{aligned} \text{Scale Down } X_C &= 1/Y_C \\ &= 91.20 \times 10^3\ \text{S/km} \end{aligned}$$

$$\begin{aligned}\text{Scale down } C &= 1/(2\Pi f X_C)\\ &= 1/(2 \times 3.14 \times 50 \times 91.20 \times 10^3\\ &= 34.920 \text{ nF/km}\end{aligned}$$

The above-calculated R, L and C value for scale-down model is per km value. The scale-down model that is designed is sectionalized into 8 pi section each of 50 km length, as per the requirement different length can be used total length of the line is 400 km. R, L and C values for 50 km are as follows:

$$\begin{aligned}R &= 0.029\ \Omega/\text{km} \times 50\,\text{km}\\ &= 1.45\ \Omega\end{aligned}$$

$$\begin{aligned}L &= 0.891 \times 10^{-3}\ \text{H/km} \times 50\ \text{km}\\ &= 44.55\ \text{mH}\end{aligned}$$

$$\begin{aligned}C &= 34.920\ \text{nF/km} \times 50\ \text{km}\\ &= 1.746\ \mu\text{F}\end{aligned}$$

3 Design and Fabrication of the Model

Actual system is rated 620 MVA, 275 kV and scale-down model is rated 0.5 kVA, 0.23 kV. Hence rated current (I) of actual system and rated current (I_{sd}) of scale-down model is calculated as follows:

$$I = \frac{620 \times 10^3\ \text{KVA}}{275\ \text{KV}} = 2254.5\ \text{A}.$$

$$I_{\text{sd}} = \frac{0.5\ \text{KVA}}{0.230\ \text{kV}} = 2.1739\ \text{A}$$

Hence the resistance, inductance and capacitance are selected based on the above current rating I_{sd}. In this design it is also observed that the value of X/R ratio for actual system and the scale-down model is almost same: $\frac{0.280}{0.029} = 9.6$.

4 Result and Simulation

A transmission line model is developed in Simulink using the calculated parameter value of R, L and C. $ABCD$ parameter is determined. Using

$$V_S = AV_R + BI_R$$
$$I_S = CV_R + DI_R$$

Open circuit and short circuit test was conducted to determine the *ABCD* parameter of the scale-down model of transmission line and the simulated and practical value was compared and it was almost same (Table 1).

Observation Table (From Simulation)

In Table 2 it can be seen that the sending end voltage is less than that of receiving end; this is because the capacitive charging current as it flows through the inductance of the line and as the length of the line increases the voltage at the end increases. This effect is known as Ferranti effect [4].

From open and short circuit test the *ABCD* parameter of the transmission line is calculated. Open circuit test gives the value of *A* and *D* and short circuit test gives

Table 1 Short circuit test

S. No.	Supply voltage (V_S)	Supply current (I_S)	Receiving voltage (V_S)	Receiving current (I_S)
1	50	1.78	0	1.78
2	60	2.13	0	2.13
3	65	2.31	0	2.31
4	70	2.49	0	2.49
5	75	2.65	0	2.67
6	80	2.85	0	2.85
7	85	3.02	0	3.02

Table 2 Open circuit test

S. No.	Supply voltage (V_S)	Supply current (I_S)	Receiving voltage (V_S)	Receiving current (I_S)
1	60	0.066	60.9	0
2	65	0.071	65.95	0
3	70	0.0769	71.03	0
4	75	0.082	76.14	0
5	80	0.088	81.15	0
6	85	0.0933	86.3	0

Fig. 1 Scale-down transmission line model

the value of B and C [5]. The following calculations are made with reference to the observation obtained for the Simulink simulation results (Fig. 1)

$$A = V_S/V_R = 60/60.9 = 0.98522$$

$$B = V_{S/}I_R = 60/2.1363 = 28.0859$$

$$C = I_S/V_R = 0.066/60.9 = 1.0837 \times 10^{-3}$$

$$D = I_S/I_R = 2.1363/2.1363 = 1$$

5 Conclusion

In this paper, the design and fabrication of scale-down model of transmission is discussed in detail and the application of the developed model to determine the *ABCD* parameter is also explained. Any kind of FACTS devices can be connected with the developed model to carry on more experiments related to transmission lines. The future work can be analysis of VAR compensation technique using the developed model [6].

References

1. Chavan, S.V., Patil, R.V., Kamble, S.S.: Hardware implementation of transmission line and its study using MATLAB. Int. J. Eng. Res. Technol. (IJERT). 2360–2363 (2014)
2. Murali, M., Pande, V.N., Gopalkrishnan, N.: Design, analysis, fabrication, and testing of laboratory model of transmission line. Electr. Power Compon. Syst. 1215–1224 (2015)
3. https://www.researchgate.net: Per unit value
4. Mali, B.N., Aglawe, P.M., Mane, S.A., Shakya, M.: Performance study of transmission line Ferranti effect and fault simulation model using MATLAB. Int. J. Innovative Res. Electr. Electron. Instrum. Control Eng. 49–52 (2016)
5. Emerole Kelechi, C., Chinedum, M.G.: A-B-C-D parameter model for two-port networks. Int. J. Adv. Eng. Res. Technol. (IJAERT). 234–239 (2015)
6. Mendoza-Araya, P., Munoz, J., Nolasco, J.C., Palma-Behnke, R.E.: Lab-scale TCR-based SVC system for education and DG application. IEEE Trans. Power Syst. 3–11 (2011)