Inductorless SiGe BiCMOS Optical Receiver Front End for 25 Gb/s Optical Links

Jingqiu Wang, Fujiang Lin, Liang Chen and Qiwei Song

Abstract A novel inductorless optical receiver analog front end (AFE) design is demonstrated to require less chip area and is suitable for both low cost and high-speed optical communication applications. The optimized transimpedance amplifier (TIA) has a differential regulated cascode (RGC) topology, with a novel zero-pole canceling technique. The proposed limiting amplifier (LA) using Cherry–Hooper topology and negative Miller capacitance broaden the bandwidth. Based on the IBM 7WL 0.18 μm SiGe BiCMOS process, the post-simulation results show a total transimpedance gain of 107.1 dBΩ and −3 dB bandwidth of 17 GHz. The chip consumes 132 mW power dissipation from a single 3.3 V supply and occupies the core area of only 110 × 340 μm^2.

Keywords SiGe BiCMOS · Optical receiver · Inductorless · Zero-pole canceling · Negative miller capacitance

1 Introduction

The required data traffic is rapidly increasing in the Internet, supercomputing, and data centers. For these applications, existing electrical communications face severe performance limitation due to signal integrity and jitter, density, cross-talk noises, and power dissipation. Fiber-optic techniques are gaining popularity as they can

J. Wang · F. Lin
School of Information Science and Technology, University of Science and Technology of China, Hefei 230026, China

J. Wang · L. Chen · Q. Song (✉)
National ASIC Design Engineering Center, Institute of Automation, Chinese Academy of Sciences, Beijing 100190, China
e-mail: sqw6307@tju.edu.cn

Q. Song
School of Electronic Information Engineering, Tianjin University, Tianjin 300072, China

Q. Liang et al. (eds.), *Communications, Signal Processing, and Systems*, Lecture Notes in Electrical Engineering 423,
https://doi.org/10.1007/978-981-10-3229-5_58

solve above problems. Furthermore, silicon photonics interconnect techniques are emerging as a major driving force because they can fabricated on bulk silicon platforms [1, 2].

An essential electronic building block is the optical receiver in optical links, and its performance can affect the whole optical interconnect systems. Transimpedance amplifier (TIA) and limiting amplifier (LA) are the two critical blocks in the optical receiver. Parasitic capacitances of transistors greatly reduce the bandwidth [3], several hybrid optical integration technologies such as inductive peaking and capacitive degeneration have been widely explored to demonstrate coherent wideband optical receivers [4]. Furthermore, we have realized SiGe BiCMOS RGC TIA with one on-chip spiral inductor, which achieves 20 Gb/s [5]. However, using inductors result in the chip size dramatically increases, also the magnetic cross talk increases through the inductors resulting in performance degradation of the clock and data recovery (CDR) [6]. Therefore, inductive peaking technology can be realized with active devices if the area is critical.

This letter present a fully inductorless differential SiGe BiCMOS optical receiver AFE tailored to IEEE 100 GBASE-LR4 standard for mid-to-long-range transmissions at a channel speed of 25 Gb/s. The IC comprises a TIA with a novel capacitive emitter degeneration technology, an equalizer, two-stage LA with negative Miller compensation and a f_T doubler buffer.

2 Proposed Circuit Implementation

2.1 Transimpedance Amplifier

The TIA is the first critical block in the optical receiver AFE. The main bandwidth restriction of a conventional TIA is usually at the input node due to the large parasitic photodiode capacitance. By modifying conventional common gate (CG) input stage to regulated cascade (RGC) or common gate feedforward topology containing negative feedback, very small input impedance can be obtained to relax the gain-bandwidth tradeoff at the input node [7]. The schematic of the proposed TIA circuit is shown in Fig. 1a. Obviously, this is a fully differential RGC input stage. However, unlike traditional structure, resistor R_{E1}, and capacitor C_{E1} can provide an extra zero for zero-pole canceling. There are two dominant poles in this fully differential, V_{out1} and V_{out2}, which will seriously reduce the stability and bandwidth of the amplifier. Fortunately, the two dominant poles can be canceled with zero by adjusting R_{E1} and C_{E1}. The new dominant pole is pushed to V_{in1} and V_{in2}. Because of this low input resistance characteristic of RGC topology, the bandwidth of the modified fully differential TIA will be higher. The detailed analysis of this TIA topology can be found in [5].

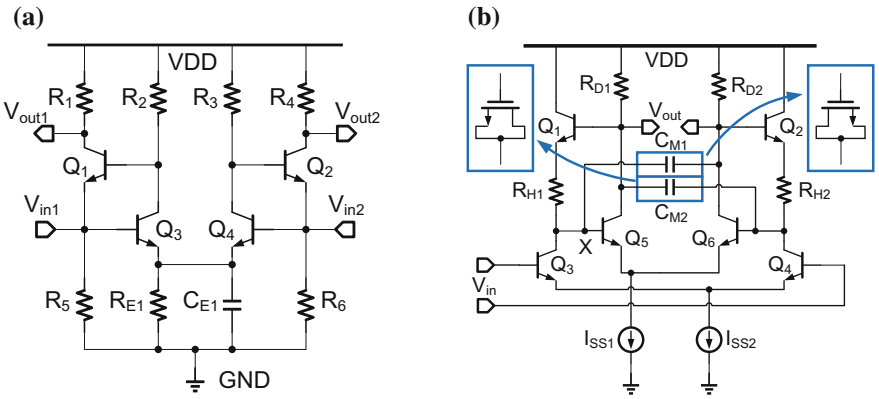

Fig. 1 Schematic of the proposed **a** TIA and **b** LA

2.2 *Limiting Amplifier*

A traditional LA is difficult to achieve high gain-bandwidth product (GBW) due to the identical cascaded gain cells topology [8]. Several circuit techniques have been proposed to enhance the bandwidth of LA in the past. Cherry–Hooper amplifier with emitter–follower feedback is widely used in LA and decision circuits in photoelectronic integrated receivers. Operation in wideband communication systems requires high slew rates and thus high tail current, so the power dissipation is rather high [9]. In our design, a modified Cherry–Hooper gain cells is introduced to achieve high GBW performance [10]. The LA is a combination of a modified Cherry–Hooper amplifier with negative Miller compensation. Figure 1b shows the schematic of the proposed LA.

The Q_1 (Q_2) and R_{D1} (R_{D2}) provide equivalent active inductor load to improve bandwidth, and the R_{H1} (R_{H2}) can achieve higher gain performance. It is assumed that the circuit is symmetrical, so that the small-signal parameters of Q_3 and Q_4 are equal. The base–collector capacitance of the transistor Q_3, $C_{\mu 3}$, was reflected to the base and collector of Q_3 using the Miller effect. Hence, the equivalent capacitance of node X, C_X, are the addition of $C_{\mu 3}$ reflected to the collector of Q_3, the base–emitter capacitance of Q_5, $C_{\pi 5}$ and the collector-buck capacitance of Q_3, C_{sub1}.

Obviously, C_X will create the dominate pole if the pole due to C_{in} and C_{out} is at a relatively high frequency. Thus, the conventional Cherry–Hooper LA topology cannot work in high speed communication systems. If we can weaken the effect of this pole, the bandwidth of the LA will be limited at higher frequencies. Fortunately, this supposition can be realized using negative Miller capacitance method. As shown in Fig. 1b, two capacitors are connected across the non-inverting nodes of the amplifier to cancel the some part of the amplifier's input capacitance. If a capacitance C_{M1} (C_{M2}) is connected across the non-inverting nodes of an amplifier, effective miller capacitance at the input of the amplifier becomes $-C_M$ (1−A),

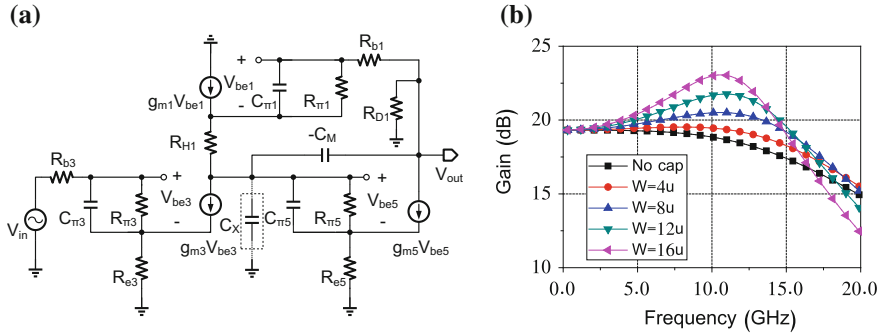

Fig. 2 **a** Small-signal differential-mode half circuit of the proposed LA. **b** Simulated frequency response with different values of W

where A is the gain between these non-inverting nodes. Figure 2a is the small-signal differential-mode half circuit of proposed LA. In order to save the area, C_{M1} and C_{M2} are realized by placing NMOS devices inside an N-well, thus providing a greater fraction of the gate-oxide capacitance. Efficiency of this method depends on the cutoff frequency of capacitors and their series resistances. Therefore, the new equivalent capacitance of node X, C_X, new, is given

By

$$\begin{aligned} C_{X,new} &= C_{\pi 5} + \left(1 - \frac{1}{A_3}\right) C_{\mu 3} + C_{sub3} + C_{\mu 5}(1 - A_5) + [-C_M(1 - A_5)], \\ &= C_X - C_M(1 - A_5) \end{aligned} \tag{1}$$

where A_3 and A_5 are the gains across $C_{\mu 3}$ and $C_{\mu 5}$, respectively, and are given by

$$A_3 = -\frac{g_{m3}(1 + R_H \cdot g_{m1})}{g_{m1}(1 + R_D \cdot g_{m5})} \tag{2}$$

$$A_5 = g_{m5} R_D \tag{3}$$

where g_{mn} is the transconductance of transistor n, $R_{\pi n}$ is the base–emitter resistance for a transistor n. Figure 2b shows the simulated frequency response of proposed LA with different values of channel width (W) of NMOS capacitor (the channel length of NMOS is fixed). It can be found that the −3 dB bandwidth of the proposed topology is 1.3 times than that without negative Miller NMOS capacitor.

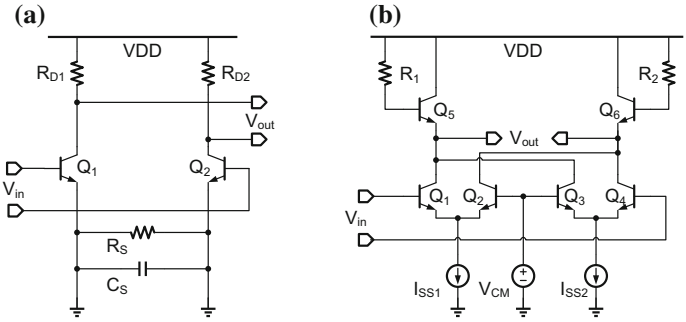

Fig. 3 **a** Schematic of the proposed EQ and **b** Buffer

2.3 Equalizer and Buffer

Figure 3a shows the schematic diagram of the equalizer (EQ) circuit includes the emitter degeneration resistor and capacitor to extend the bandwidth. The equivalent transconductance of the EQ is given by

$$G_m = \frac{g_m(R_s C_s + 1)}{R_s C_s + 1 + g_m R_s/2} \tag{4}$$

If the zero ($1/R_sC_s$) cancels the pole ($1/R_DC_L$) at the collector, the bandwidth of the EQ is extended. Where C_L represents the load capacitance of EQ's output. However, emitter degeneration may cause undesired gain peaking in the frequency response. Thus, the tradeoff between gain flat degree and bandwidth should be considered.

To drive the testing instruments with an input impedance of 50 Ω, an output buffer is included in the design. To deliver a single-ended voltage swing of 0.5 V, the buffer must steer 10 mA, which requires a tail current of 20 mA. This work employs a f_T doubler as the output buffer with active inductive peaking. Depicted in Fig. 5, the circuit exhibits an input capacitance roughly equal to half the base–emitter capacitance of Q_1 while provide the same transconductance as that of Q_1.

3 Layout and Simulation Results

In order to verify the effectiveness and feasibility of the proposed topology, we performed cadence simulation using IBM7WL 0.18 μm SiGe BiCMOS technology, which offers HBTs with a maximum transit frequency of 60 GHz. The chip layout is depicted in Fig. 4. Two on-chip 300 fF MIM capacitors are used to mimic the effect of the photodiode parasitic capacitance, and together with the parasitic capacitance of the input pad, the total input parasitic capacitance is about 0.35 pF.

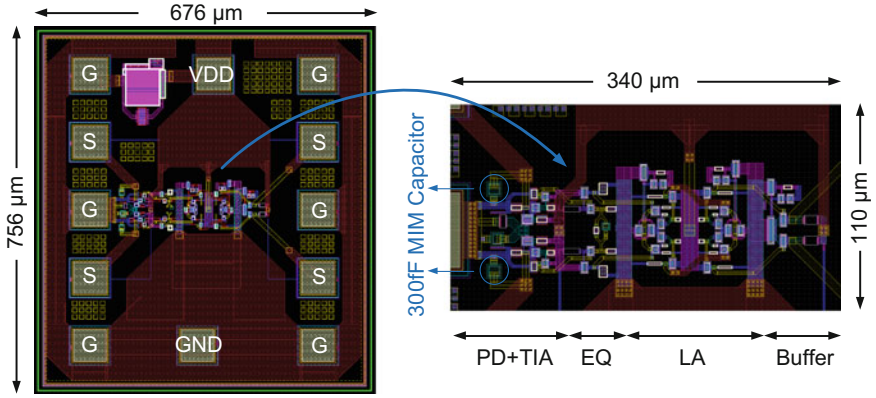

Fig. 4 Layout of the proposed optical receiver AFE

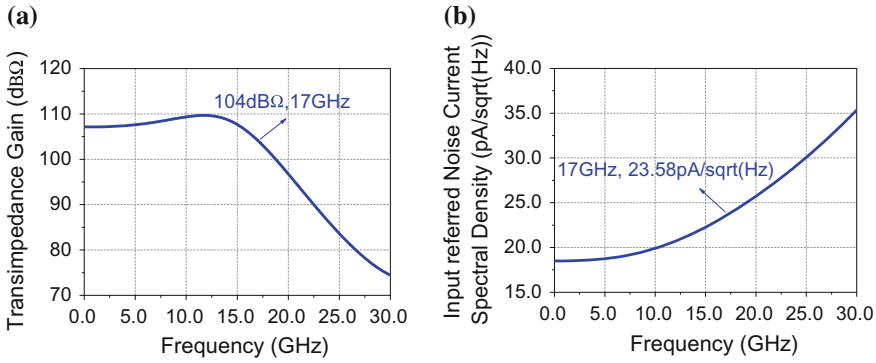

Fig. 5 Post-layout simulated **a** differential frequency response and **b** noise response

The size of the IC is 756 × 676 µm^2 due to the GSGSG differential probe, but the active area occupies only 340 × 110 µm^2. Figure 5a shows the post-layout simulated frequency response for the proposed optical receiver AFE exhibits a transimpedance gain of 107.1 dBΩ and bandwidth of 17.03 GHz. The receiver consumes 132 mW from 3.3 V supply. Figure 5b illustrates the post-layout simulated input noise current spectral density. The simulation results show an equivalent input noise current spectral density below 23.6 pA$\sqrt{\text{Hz}}$ up to 17.03 GHz. Figure 6 shows the post-layout simulated output eye diagram with 10 µApp input current as well as $2^{31}-1$ PRBS (pseudorandom binary sequence) NRZ (non-return-to-zero) input data.

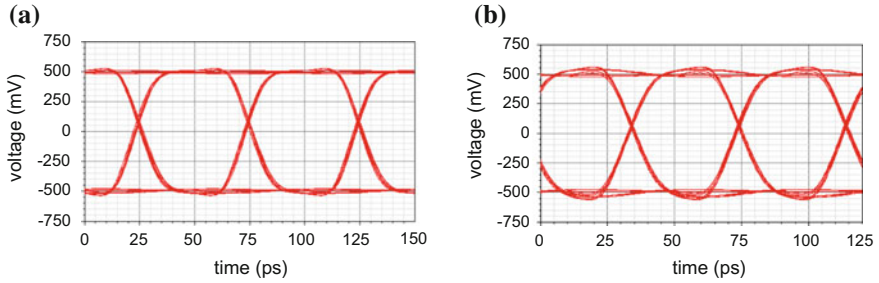

Fig. 6 Post-layout simulated eye diagram of the differential output with 10 μApp input current at **a** 20 Gb/s and **b** 25 Gb/s

4 Conclusion

This paper presents a novel inductorless fully differential optical receiver AFE. It is implemented in 0.18 μm SiGe BiCMOS technology which offers HBTs with a maximum transit frequency of 60 GHz. One of the innovations is the Cherry–Hopper LA with negative NMOS Miller capacitance significantly increases the bandwidth. It is observed that optical receiver AFE achieves a high transimpedance gain of 107 dBΩ over a high bandwidth of 17 GHz in the presence of a 300 fF photodiode capacitance which is sufficient for 25 Gb/s. The optical receiver AFE occupies 340 × 110 μm^2 (without PAD) and the power dissipation is 132 mW at a 3.3 V supply. Simulation results show that the optical receiver AFE is very proficient for applications in high speed optical transceivers.

References

1. J.-S. Youn, M.-J. Lee, K.-Y. Park, H. Rücker, W.-Y. Choi, A bandwidth adjustable integrated optical receiver with an on-chip silicon avalanche photodetector. IEICE Electron. Express. **8** (7), 404–409 (2011)
2. D. Li, G. Minoia, M. Repossi, D. Baldi, E. Temporiti, A. Mazzanti, F. Svelto, A low-noise design technique for high-speed CMOS optical receivers. IEEE J. Solid-State Circuits **49**(6), 1437–1447 (2014)
3. C. Li, S. Palermo, A low-power 26-GHz transformer-based regulated cascode SiGe BiCMOS transimpedance amplifier. IEEE J. Solid-State Circuits **48**(5), 1264–1275 (2013)
4. K. Park, B.C. Kim, B. Jung, W.-S. Oh, A 1–13 Gbps tunable optical receiver with supply voltage scaling. IEICE Electron. Express. **11**(18), 1–6 (2014)
5. Q. Song, L. Mao, S. Xie, Wideband SiGe BiCMOS transimpedance amplifier for 20 Gb/s optical links. IEICE Electron. Express. **12**(13), 1–8 (2015)
6. O. Momeni, H. Hashemi, E. Afshari, A 10-Gb/s Inductorless transimpedance amplifier. IEEE Trans. Circuits Syst.-II, Exp. Briefs **57**(12), 926–930 (2010)
7. Z. Lu, K.S. Yeo, J. Ma, M.A. Do, W.M. Lim, X. Chen, Broad-band design techniques for transimpedance amplifiers. IEEE Trans. Circuits Syst.-I, Reg. Papers **54**(3), 590–600 (2007)

8. F. Jiang, J. Chen, D. Wu, J. Wu, Z. Jin, X. Liu, A wide dynamic range transimpedance amplifier with high gain-bandwidth product for 10 Gb/s optical links, in *International Workshop on Microwave and Millimeter Wave Circuits and System Technology (MMWCST)*, vol. 1 (2012)
9. M. Maadani, M. Atarodi, A Low-area, 0.18 μm CMOS, 10 Gb/s optical receiver analog front end, in *IEEE International Symposium on Circuits and Systems* (2007), pp. 3904–3907
10. C.D. Holdenried, J.W. Haslett, M.W. Lynch, Analysis and design of HBT Cherry-Hooper amplifiers with emitter-follower feedback for optical communications. IEEE J. Solid-State Circuits **39**(11), 1959–1967 (2004)