Differential Voltage Controlled Ring Oscillators—A Review

Tripti Kackar, Shruti Suman and P.K. Ghosh

Abstract The differential ring voltage controlled oscillator (DRVCO) is a key component in various fields of communication and transmission systems with increased modularity and excellent controllability. This paper analyzes the different DRVCOs cell topologies and their performance have been interpreted in terms of frequency range, power consumption, phase noise and technology used, which allows the designers to opt the most suitable differential ring VCO for specific applications.

Keywords Voltage controlled oscillator (VCO) · Differential voltage controlled ring oscillator (DVCRO) · Delay stages

1 Introduction

Voltage controlled oscillator (VCO) is an essential block of electronic systems in which output frequency is linearly varied by input control voltage. The major applications of VCOs are optical transmission, clock generation, radio frequency integrated devices (RFID) transponders [1] and data recovery circuits and also in medical domains [2]. CMOS based ring VCOs are widely used as they have high tuning range. The design of circuits with enhanced speed, power and larger bandwidth is one of the greatest challenges for designers today. To successfully deal with it, the best choice is a ring VCO, because it generates multiple phases.

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The odd number of stages is connected such that the output of last stage is fed back to the input of first stage. In order to have sustained oscillations, it must satisfy necessary conditions i.e. the total phase shift around the loop must be 360° and the loop gain must be equal to unity as stated by Barkhausen. The advanced demands of VCO circuits comprise miniaturization, less power dissipation and lower phase noise. The frequency of oscillations for N stages can be given by Eq. (1) [3]:

$$f_{osc} = \frac{1}{2Nt_d} \tag{1}$$

where N is the total number of stages in a ring oscillator and t_d is the delay at each stage given by $t_d = C_{eq} * R_{eq}$. In general, VCOs has output frequency as an function of applied control voltage which can be given by Eq. (2) [4]:

$$f_{out} = F_o + K_{VCO} V_{Ctrl} \tag{2}$$

where F_o is the frequency of oscillations of VCO, K_{VCO} is the gain of the VCO which checks variation over control voltage (V_{Ctrl}) which is input to the VCO determining it's operating frequency. The ring VCOs can be categorised as single ended and differential configurations [5].

Figures 1 and 2 shows the simplified cascaded structures in ring form of basic types of VCOs for N number of stages. The differential ring oscillators are advantageous as they reject common mode noise and avoid usage of bypass and coupling capacitors together with high gain stability at high frequencies. Although single ended configurations consumes less area but are less efficient in terms of noise. The odd numbers of stages are well suited for single ended oscillators and will always oscillate whereas differential configurations can have both odd as well as even number stages. The differential configurations with even number of stages are useful for generating quadrature or multiphase outputs [6].

The objective of this paper is to analyze the records on differential VCOs using delay stage of each oscillator circuit. The remaining paper is categorized as:

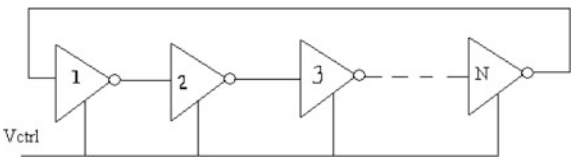

Fig. 1 Single ended ring VCO

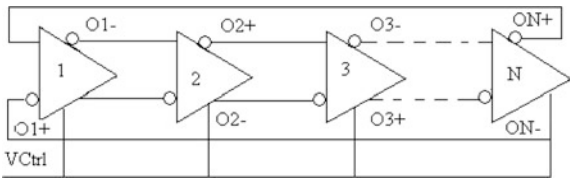

Fig. 2 Differential ring VCO

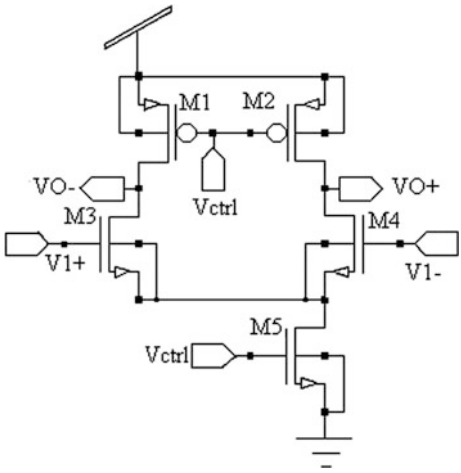

Fig. 3 Conventional delay cell for DRVCO

Section 2 focuses on fundamental basics of DVCRO. The improved versions of differential delay cells and results are summarized in Sect. 3. Section 4 finally gives future scope and conclusions.

2 Differential Voltage Controlled Ring Oscillator

The differential ring VCO in semiconductor industries is extensively used for all integrated circuit applications in differential mode of operation. The circuit designing is done generally based on ring oscillator topology with inverting and non-inverting stages which is helpful for low power consumption and closed loop structure with positive feedback enhances the speed of the design.

The schematic of conventional delay cell is shown in Fig. 3. Each delay stage comprises of two transistors as a load M1 and M2, two input transistors M3 and M4 and one current source transistor M5 is added at the tail. This delay cell network fails to satisfy the oscillations criterion at two stages due to hindered stability conditions and insufficient gain observed which is thereby, overcome with the help of positive feedback.

3 Different Delay Stages for Differential Voltage Controlled Ring Oscillator

There are several methods by which differential VCOs can be designed. The design perspectives are implemented in relevance with fundamental parameters. Few of the differential voltage controlled ring oscillators delay stages are briefly discussed as follows:

3.1 High Speed and Low Power Delay Cell

With the help of CMOS technology, the delay cell technique [7] gives wider band of frequencies for operation but also allows larger gain, linearity, spectral purity of signal in compensation with power and noise due to glitches and switching at the circuit nodes. The VCO is designed using fast slewing saturated differential delay cell [8] gives fast rise and fall times and leads to full switching operation. The average noise power P_n for any random process is expressed in Eq. (3):

$$P_n = \lim_{T\to\infty} \frac{1}{T} \int_{-T/2}^{T/2} v_n^2(t).dt \tag{3}$$

where V_n is the noise voltage given by $v_n^2(t) = 4\,KTR$. Here, K is the Boltzmann's constant, R is the resistance value and T is switching on time for each cycle which is defined in Eq. (4) as,

$$T = \frac{C_L V_{DD}}{I} \tag{4}$$

Here, C_L is the load capacitance at the output of each node, V_{DD} is the power supply voltage and I is the current in the device during operation. Hence, fundamental noise analysis done for ring oscillator yields average noise power as the function of time constant, delay at each stage and oscillation frequency.

The four-input differential delay cell is shown in Fig. 4. Firstly M9 and M10 forms differential input block, then pair of load transistors M2 and M3 forms latch block. Now the transistors M6 and M7 which is a controlled circuitry for CMOS latch stage to strengthen it resulting in decreases delay time. The acceleration block with transistors M1 and M4 are added to the load so as to generate negative skewed

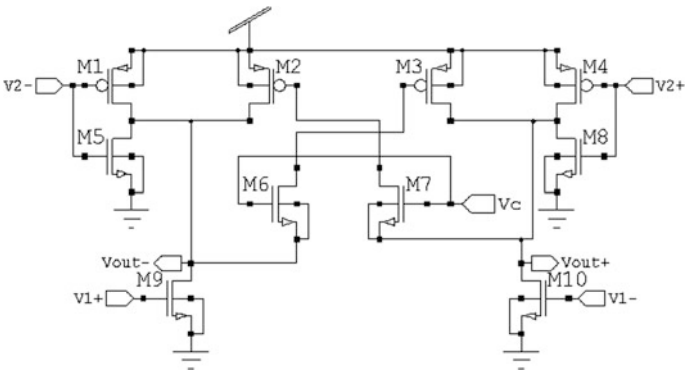

Fig. 4 Delay cell for high speed DRVCO

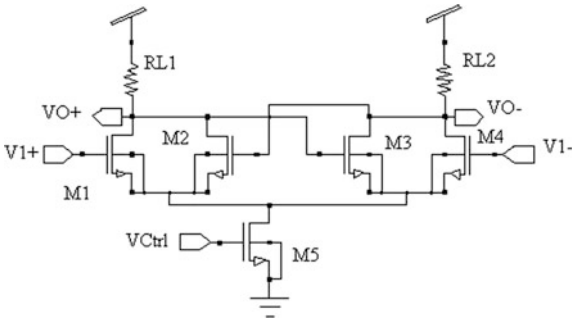

Fig. 5 Delay cell for low power DRVCO

signal which precharges the output nodes which ensures fast operation. This arrangement reduces rise time of the output as well as phase and supply noise. Similarly, transistors M5 and M8 NMOS are added to pre-discharge the output nodes decreasing fall time and achieves higher oscillation frequency, also hinders the frequency limitation problem.

The NMOS transistors provide positive feedback and sufficient delay to accomplish oscillatory criteria as shown in Fig. 5 [9]. The circuit can be best suited for optical communications applications as it exhibit good transient stability as shown in Eq. (5) and superior characteristics.

$$H(s = j\omega) \approx -\frac{G_o}{\left(1 + \frac{S}{\omega_o}\right)} \approx \frac{g_{m1R}}{1 - g_{m2R}} \tag{5}$$

where ω_o is the frequency at the pole, G_o is the open loop gain of the cell, g_{m1} and g_{m2} are the transconductance of transistor M1–M4 and M2–M3 respectively and R is the resistance of the symmetric load. The measured phase noise at 1 MHz offset is −141 decibels per hertz.

3.2 *Low Noise Multiloop Delay Cell*

In order to achieve the maximum desired frequency, the multiloop architecture using coarse and fine controls is reported in [10] as shown in Fig. 6. This can be done by adjusting positive feedback cross coupled pair of NMOS transistors M9 and M10. The phase noise and power spectral functions are determined using impulse sensitive function (ISF) and noise modulation functions (NMF). By varying the load PMOS using gate voltage of transistors M3 and M4 in ratio of M3 and M4 coarse tuning by control terminal V_c can be done and by changing the current in transistor M11 of latch network fine tuning using control V_F can be obtained. According to the linear time invariant theory, the phase noise can be closely stated as in Eq. (6) [11]:

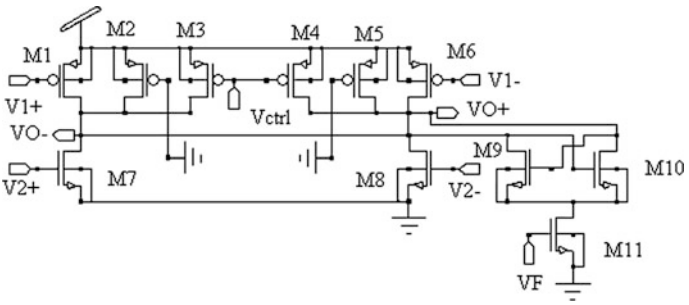

Fig. 6 Delay cell for low noise multiloop DRVCO

$$L(\Delta\omega) = 10\log\left[\frac{2KTF}{p}\left(1+\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right)\left(1+\frac{\Delta\omega 1/f3}{|\Delta\omega|}\right)\right] \tag{6}$$

where K is the Boltzmann's constant having value 1.38×10^{-23} J/K, P is the average signal power dissipated, T is the absolute temperature, F is fitting parameter for figure of noise, $\Delta\omega 1/f3$ is corner angular frequency between $1/f_3$ and $1/f_2$ components of flicker noise and Q is quality function of the oscillator which is expressed as given by Eq. (7):

$$Q = \frac{f_o}{2\Delta f_{-3db}} \tag{7}$$

When Q increases due to decrease in −3 db bandwidth represented by Δf_{-3db} results in sharpening of the peak in magnitude response. The measured phase noise at 1 MHz offset is −103.4 decibels per hertz.

3.3 Wide Bandwidth and Pseudo Differential Delay Cell

The day by day rise in demands for higher spectrum of frequencies allows devisers to explore new methods for adjusting the range requirements of the DVCRO systems. This delay cell as referred in [12] proposes a method for increasing the frequency of the CMOS ring VCOs. The approach of delay cell was implemented in which diode connected load M1 and M4 is used in differential pair in order to have large output swings as shown in Fig. 7. A control voltage (V_{Ctrl}) is applied such that it adjust the frequency of the oscillator by regulating the current in the transistor M7.

In pseudo differential delay cell [13] as shown in Fig. 8, input to the cell is given through CMOS differential push pull inverter. It also avoids the need of common

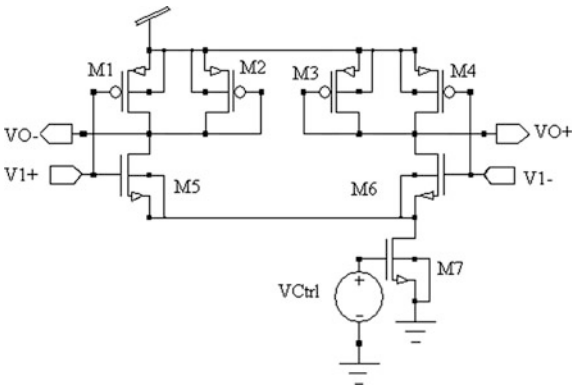

Fig. 7 Delay cell for wide bandwidth DRVCO

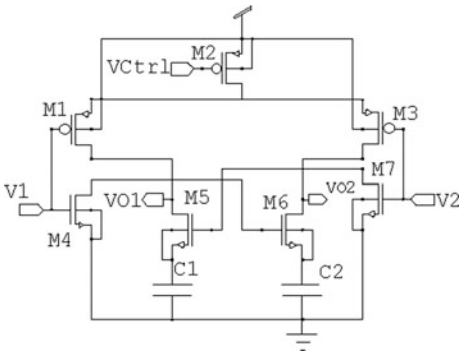

Fig. 8 Pseudo differential delay cell for DRVCO

tail transistor as a current source and gives fine frequency range. The operating frequency is obtained obtained as given by Eq. (8):

$$F_{osc} = \frac{\sqrt{3}}{2\Pi}\frac{\left(R_\lambda - g_{mp2}\right)}{C_T} = \frac{\sqrt{3}}{4\pi}\frac{\left(g_{mn1} + g_{mp1}\right)}{C_T} \tag{8}$$

where g_m the transconductance parameter of transistors for NMOS and PMOS, C_T is the total capacitance at the output node and R_λ is the resistance due to channel length modulation CLM effect. The delay cell design determining the best possible configuration for the ring oscillators having the least power consumption and precise delay with lesser sensitivity to the variations in the temperature and supply voltage for frequencies of GHz along with higher figure of merit. These Systems also realized with RFID transponders, WSN and 802.11 protocols thereby signify maximum data rate transfers at high speed process. The measured phase noise at 1 MHz offset is −162.4 decibels per hertz.

The results of different differential ring VCOs cells at different technology are shown in Table 1.

Table 1 Summary of simulated results

References	[7]	[9]	[10]	[12]	[13]
No. of transistors used in single delay stage	10	05	11	07	07
Power (mW)	12	1.09	60	1.09	2.47
Supply voltage (V)	2.5	1.8	1.5	1.2	1.5
Technology (μm)	0.25	0.18	0.13	0.5	0.18
Bandwidth (GHz)	0.85–2.1	1.6–2.6	7.3–7.86	1.6–2.6	0.5–2.54

4 Conclusions

The review of various differential ring VCOs delay stages has been presented in this paper, and finally concluded that the with the advancement in technology, there would always be the explosive requirement of efficient system devices in respect to the desired results, with tradeoffs between transistor sizing, frequency, speed, delay and power consumption of the circuits. The multiple feedback architectures are useful for low noise characteristics and maximum signal swings. The differential stages along with saturated load are providing the useful characteristics in terms of maximum frequency and low output phase noise. These characteristics of differential VCOs are explored when used at high frequencies at low power supply applications.

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