Modeling of Steady State and Transient State of the Power Electronic Distribution Transformer

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Abstract This research study presents a new type of power electronic distribution transformer (PEDT), aimed to overcome the disadvantages of the traditional electromagnetic distribution transformers. This new proposed model is named as power electronic distribution transformer incorporating power electronic converters in both primary and secondary sides, in addition to the high-frequency transformer. Moreover, the PEDT is capable of providing many advantages, such as power factor improvement, voltage sag/swell, reactive power compensation, harmonics elimination, self-protection and size reduction as compared to the conventional electromagnetic transformer. MATLAB/Simulink is used to simulate the proposed model. The simulation results show that the model is capable of offering an additional DC bus on the primary side as well as high power conversation ratios and power quality improvement.

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1 Introduction

The conventional electromagnetic distribution transformers have been widely used in the power distribution system as the essential equipments for voltage transformation and isolation. Also, it has high reliability and are simple to construct. However, the traditional transformer possesses the disadvantages like heavy weight, large size, the secondary voltage vary with the input voltage and the load, having no ability to control the voltage and current, lack the self-protection and not having an intelligent functions [1]. Although, the size of the transformer is proportional inversely with the operating frequency, the PEDT will be much smaller and more lightweight than the power distribution transformer due to high-frequency operation [2]. Different topologies of PET have been introduced in the last 3 decades. The first type of PEDT was introduced by Navy researchers in 1980 [3]. The PEDT comprised of an ac/ac buck converter as presents in Fig. 1. In 1995, the Electrical Power Research Institute (EPRI) continued the development of PET [4]. As a result, the prototypes were developed, but limited by the low voltage level, very high stress factor and also lack of magnetic isolation.

In 1996, the power electronic transformer based on the AC link was developed by [5, 6] as shown in Fig. 2. The size and the weight were reduced. However, no benefits were found in terms of power quality and control. The latest type of PEDT that has three stages (input stage, isolate and output stage) based on DC link has been introduced [7–13] as in Fig. 3. Nevertheless, this type consists of a large number of components due to the parallel and series connections, which result in lower efficiency and reliability.

In this paper, a new model of PEDT is proposed based on power electronic converters on both primary and secondary sides, in addition to the high frequency transformer. In fact, the proposed power electronic distribution transformer is environmentally friendly since no liquid dielectrics are used for cooling. PEDT can be prepared with an advanced communication interface which include diagnostics, smart metering and distance control features.
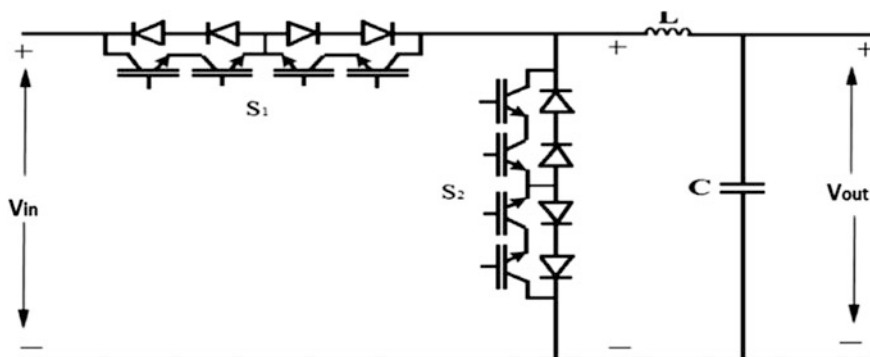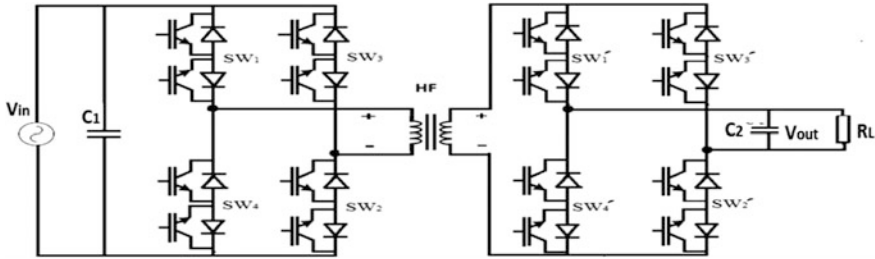

Fig. 1 AC/AC buck converter

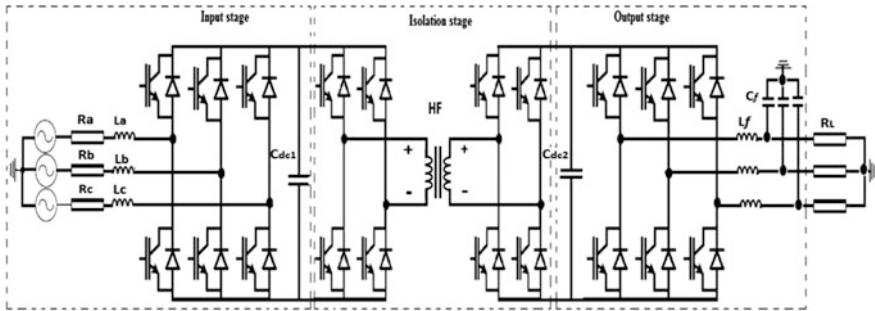**Fig. 2** High frequency transformer with AC link

Fig. 3 Power electronics transformer with DC link

2 Proposed Topology

Overall, the new proposed model of the power electronic distribution transformer has three stages as shown in Fig. 4. The first stage is an input stage comprised of a three-phase 3-level PWM converter, working as a rectifier to convert the AC grid voltage to DC one. The second stage is the isolation stage, which employs two converters, three-level, half-bridge converters connected to a high-frequency transformer (HFT), where the first converter modulates the DC voltage to high-frequency (HF) voltage and then pass it to HFT in order to reduce the high voltage to lower one with high-frequency and finally the second converter demodulates the HF voltage to DC voltage. While the third stage is output stage consists of 2-level three phase PWM converter, works as the inverter to convert the DC voltage to AC voltage. The aim of using three levels in the input stage and the middle stage is to reduce the semiconductor devices' stress ratio and improve the power quality of the grid. However, in the output stage, in the low voltage, it is more feasible to use a two-level three phase voltage source inverter than the three-level inverter, because it is cheaper and simpler.
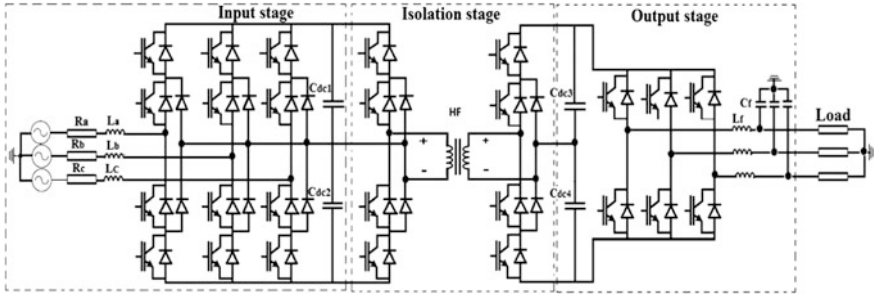
Fig. 4 The proposed topology of PEDT

2.1 The Input Stage Control

The aim of the input controller is to keep the DC-link voltage constant at the reference value and the input current and voltage purely sinusoidal. A *d-q* vector controller was used to lead the better performance and regulate the input current; the derivation of the mathematical model was presented in previously published research of [2]. The d-q mathematical model of the input stage is:

$$L_{E1} \frac{di_{E1d}}{dt} = \omega L_{E1} i_{E1q} + u_{1d} - u_{E1d} \tag{1}$$

$$L_{E1} \frac{di_{E1q}}{dt} = -\omega L_{E1} i_{E1d} + u_{1q} - u_{E1q} \tag{2}$$

where L_{E1} is the interface inductances, $I_{E1} = [i_{E1a}, \ i_{E1b}, \ i_{E1c}]$ is the line current vectors in the primary side, $u_{E1} = [u_{E1a}, \ u_{E1b}, \ u_{E1c}]$ is the AC terminal voltage vectors in the primary side, $u_1 = [u_{1a}; u_{1b}; u_{1c}]$ is input voltages in the primary and ω is the grid voltage synchronous angular.

The double closed-loop control design is based on Eqs. (1) and (2) which shows the current i_{ds} and i_{qs}. The three-level PWM rectifier output voltage was controlled using current i_{ds} and i_{qs}, where the voltage was assumed to be constant. The voltage instruction of the three-phase VSR current control in a synchronous rotating reference frame (d-q frame) will be:

$$v_d^* = -\left(k_{ip} + \frac{k_{iI}}{s}\right)(i_d^* - i_{ds}) + \omega L_{qs} + u_{ds} \tag{3}$$

$$v_q^* = -\left(k_{ip} + \frac{k_{iI}}{s}\right)(i_q^* - i_{qs}) - \omega L_{ds} + u_{qs} \tag{4}$$

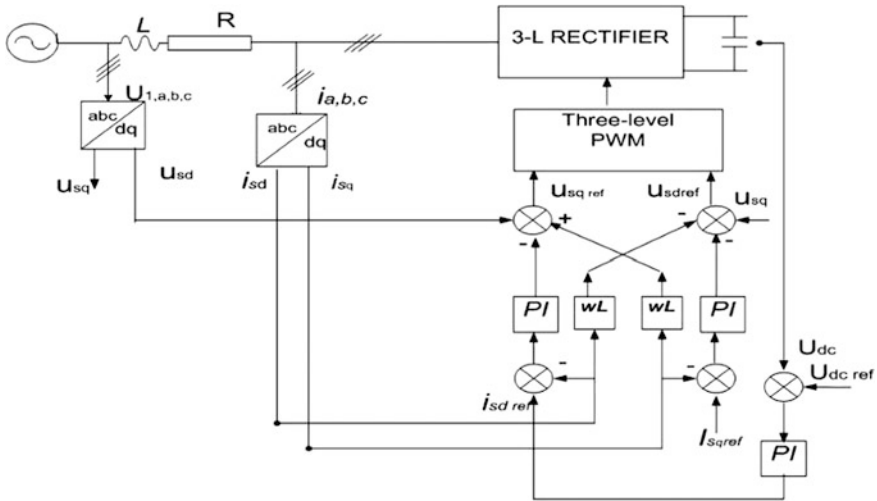where K_{iP} and K_{iI} are control confection.

Fig. 5 The input stage three-level PWM rectifier control system

The control of the input stage of PEDT is presented in Fig. 5. The rectifier output voltage was compared with the reference voltage, the error, then passed through the proportional integral controller to generate the reference value of i_d^*. The reactive current reference i_q^* is set at zero, this leads to unity power factor on the grid side. In the inner current loop, the input currents are converted into i_d and i_q reference frame. The component is compared with i_d^* and i_q^* the difference was formulated to wave signal by the proportional integral controller.

2.2 The Isolation Stage Control

In order to simplify the design control, an open loop PWM control is applied into the two single-phase, three-level converters. This control method provides an absorbing additional feature so that the synchronisation problem can easily be solved [14]. The simplified model of the middle stage can be presented as in Eq. (5).

$$V_{dc2} = \frac{1}{k} V_{dc1} \tag{5}$$

where V_{dc1} and V_{dc2} are the primary and secondary voltage for a high-frequency transformer and K is the transformation ratio.
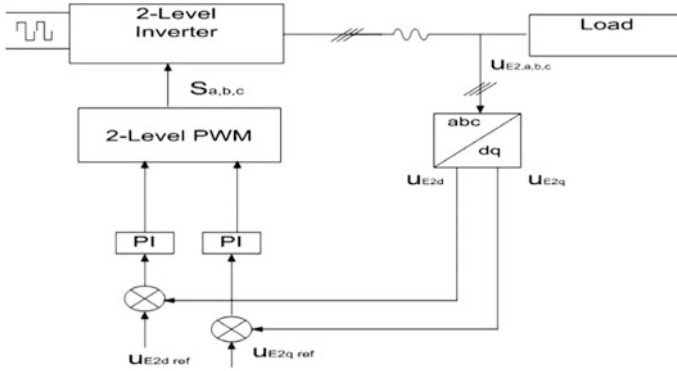
Fig. 6 Output stage control

2.3 *The Output Stage Control*

The function of output control of PEDT is to provide a constant output voltage and frequency to the end users, when the transient changes happen in the load or in the grid side. The control diagram of the output inverter is shown in Fig. 6. The d-q model of the output stage can be described through Eqs. (6) and (7) as follows.

$$L_{E2}\frac{di_{E2d}}{dt} = \omega L_{E2}i_{E2q} + u_{2d} - u_{E2d} \qquad (6)$$

$$L_{E2}\frac{di_{E2q}}{dt} = -\omega L_{E2}i_{E2d} + u_{2d} - u_{E2q} \qquad (7)$$

3 Simulation Result and Discussion

In this section, the input/output characteristics are investigated by using MATLAB/Simulink based on the mathematical model and the control strategy of PEDT. The simulation parameters are shown in Table 1.

The steady state characteristics, including input voltage, current, DC link voltage, HF transformer, primary and secondary voltage, load voltage and current are shown in Figs. 7, 8, 9, 10 and 11. Nevertheless, the input current is sinusoidal and unity power factor was nearly achieved as presented in Fig. 7. In Fig. 9, the single phase 3-level converter modulates the DC voltage into an HF square wave, whereas HF square wave was stepped down using HF transformer as shown in Fig. 10. And Fig. 11 shows the load voltage and current are in phase and the current is clearly sinusoidal and the output voltage of PEDT is 240 and found to be almost sinusoidal.

Table 1 Principal parameters

Parameters	Values
Capability	100 KVA
Input line to line voltage	11 kV
DC link capacitor C_1, C_2	40 μf
DC link capacitor C_3, C_4	7500 μf
Line frequency	50 Hz
Operating frequency	10 kHz
Input inductance	227 mH
Output filter inductance	3.5 mH
Output filter capacitance	680 μf
Load	50 Kw
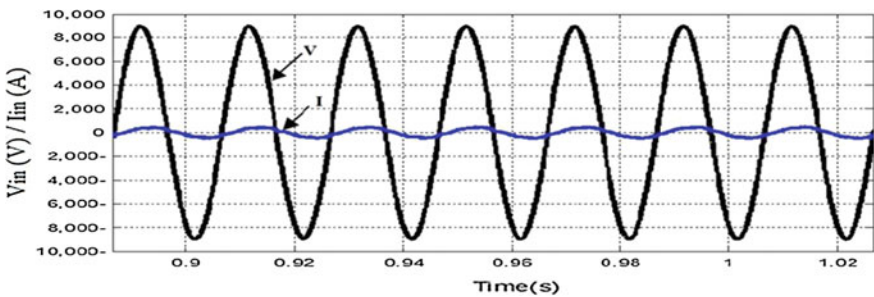
Fig. 7 Input voltage and current
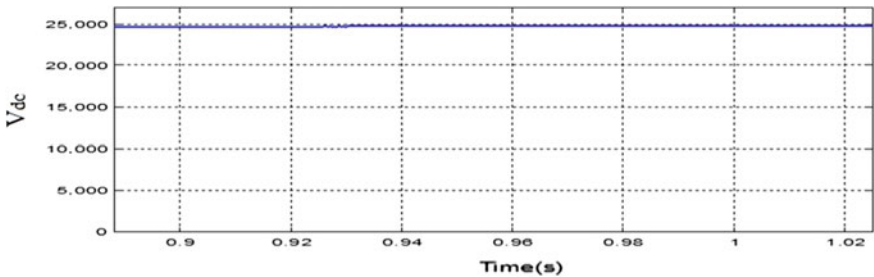
Fig. 8 High voltage DC Link PEDT

On the other hand, the proposed PEDT and the traditional transformer are identical in terms of electrical performance. However, the PEDT not only steps the voltage to a lower level, but also improves the power quality of the system that leads the PEDT to a wider range of applications. Table 2 summarises the steady state simulation result of the power electronic distribution transformer.

Additionally, in order to verify the effectiveness of the proposed PET against the power quality, the dynamic simulation such as voltage sag and voltage swell was
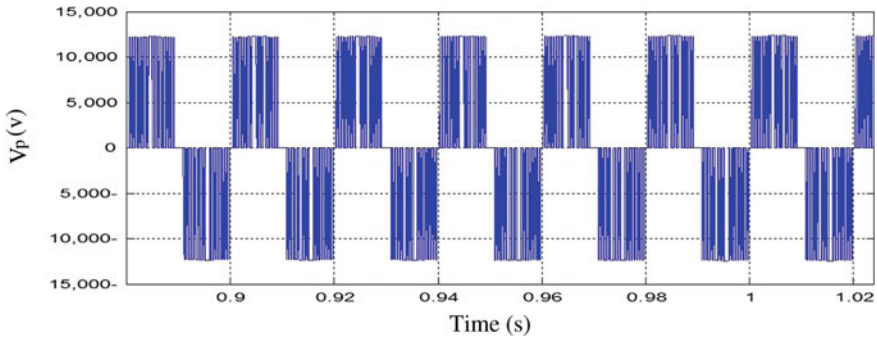
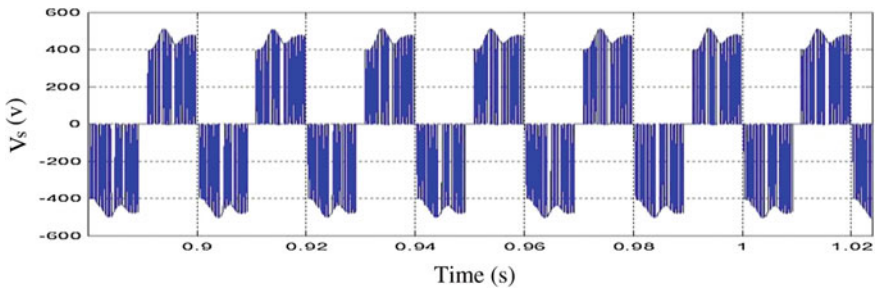**Fig. 9** The primary voltage of HF transformer

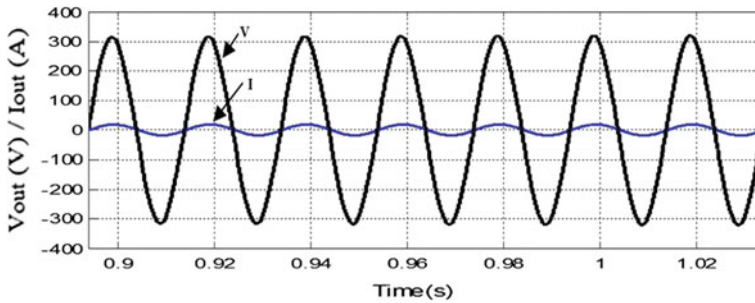**Fig. 10** The secondary voltage of HF transformer


Fig. 11 The output phase voltage of the PEDT

carried out. Figure 12 shows the three-phase grid voltage when there is 30 % voltage swell at starting time period from 0.92 s to the end time period of 0.94 s. Moreover, Fig. 13 shows the output voltage, at specified voltages, but no effect on the output voltage has been observed. Furthermore Fig. 14 shows the three-phase grid voltage when there is 30 % voltage sage between 0.92–0.94 s. As disclosed in Fig. 15, the PEDT prevent the secondary output voltage against voltage sag, infecting in the primary side of PEDT.

Table 2 Simulation result of PEDT

Parameters	Values
High voltage DC Link	24.8 kV
Primary voltage of HF transformer	12.5 kV
The secondary voltage of HF transformer	450 V
Output phase voltage of the proposed PET	240 V
Output frequency	50 Hz
The input power factor	0.9335
The output power factor	0.9848
THD in the grid side	2.23 %
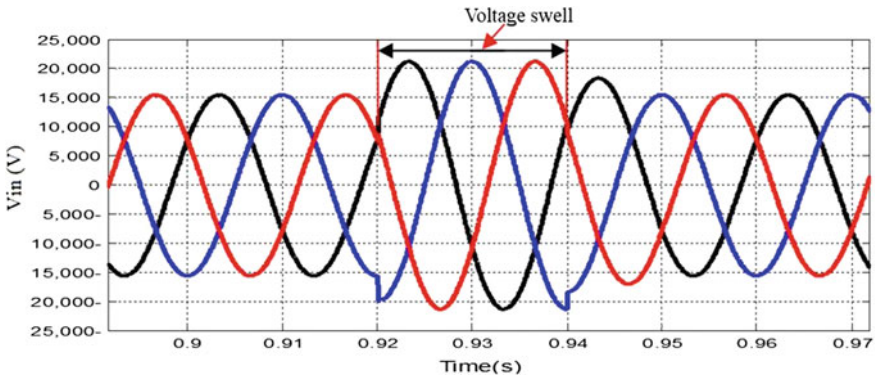
Fig. 12 Three phase input voltage under voltage swell
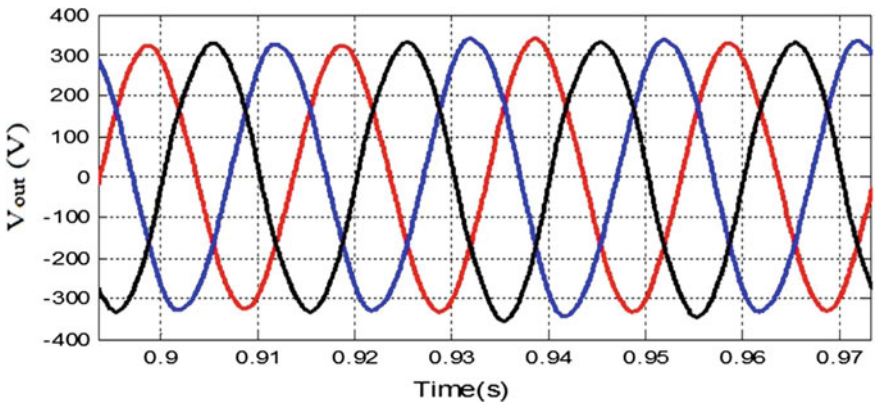
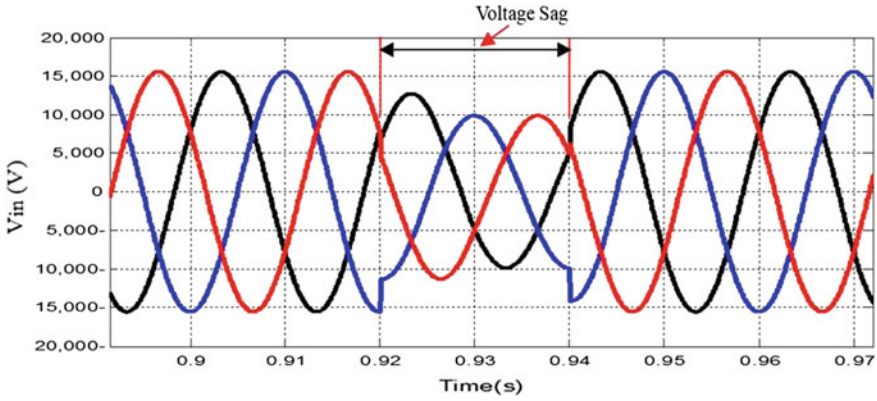
Fig. 13 Three phase output voltage under voltage swell

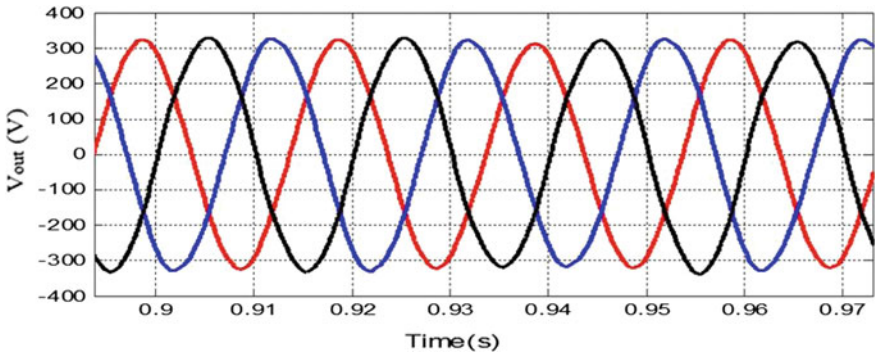**Fig. 14** Three phase input voltage under voltage sag

Fig. 15 Three phase output voltage under voltage sag

4   Conclusion

In this study, a new type of power electronic distribution transformer based on a three-level converter in the input stage and isolation stage has been proposed. This type of transformer has many advantages as compared to the traditional transformer, which is demonstrated in the simulation results. The pure sinusoidal waveforms for grid currents, nearly unity power factor and constant output voltage can be achieved by this PEDT. Accordingly, this PEDT not only steps down the voltage to a lower one, but also improves the power quality of a system, as shown in Table 2 the nearly unity PF, lower THD values on voltage and current is achieved and this model also offers a low voltage DC Bus. Besides that, the simulation results reveal that the disturbances affecting either the input or the output of the PET and do not propagate to the other side. This uncoupling effect is achieved by using the large capacitances such as DC link.

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