A Low Power Comparator Design for Analog-to-Digital Converter Using MTSCStack and DTTS Techniques

Pragash Mayar Krishnan and Mohd Tafir Mustaffa

Abstract This paper presents a low power comparator using Multi Threshold Super Cut-off Stack (MTSCStack) and Dual Threshold Transistor Stacking (DTTS) techniques using a 130 nm CMOS process technology. MTSCStack is proposed in order to decrease the leakage power in active mode and retaining the logic state of the comparator during the idle state. On the other hand, DTSS is proposed to decrease the leakage current with less impact on the delay. Based on the results, the total power consumption especially dynamic power has been reduced significantly by decreasing the VDD of the comparator. The static power and dynamic power of the post-layout proposed comparator is 797 pW and 17.55 μW respectively with delay of 1.08 ns.

Keywords MTSCStack · DTTS · Stacking · Dual threshold · Comparator · Low power

1 Introduction

Typically, power reduction techniques are mostly applied in the digital circuit instead of analog circuit [1]. This is because analog circuit are very complicated and complex. One of the rapidly growing building blocks of analogue circuit is flash analog-to-digital converter (ADC) which tends to be one of the most developed devices to be used in high speed and low power design. In flash ADC, the number of comparator increased exponentially as the resolution of the ADC is increases.

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Thus, low power and high speed comparator accuracy is important to deliver a good ADC performance [2].

Since the CMOS technology is shrinking, power consumption has been a major concern. Besides, high power consumption leads to high cost of packaging and cooling in order to minimize the heat dissipation from the circuit. This is because less power reduction techniques on analog circuit have been studied so far.

In this article, conventional comparator, comparator with reduced VDD, comparator with MTSCStack (Multi Threshold Super Cut-off Stack), comparator with DTTS (Dual Threshold Transistor Stacking) and the proposed comparator that combines all the three techniques (reduced VDD, MTSCStack and DTTS) have been designed and simulated in 0.13 μm CMOS process technology.

MTSCStack is proposed in order to decrease the leakage power in active mode and retaining the logic state of the comparator during the idle state [3]. Meanwhile, DTTS is proposed to decrease the leakage current with less impact on the delay [4].

Section 2 describes the design methodology. Section 3 discusses the parameters and power consumption of comparator on post layout simulation. Finally Sect. 4 concludes this work.

2 Circuit Design Methodology

2.1 Conventional and Reduced VDD Comparator

Figure 1 shows the schematic of conventional circuit that has been used and re-designed in this study. This conventional comparator circuit is chosen as it gives a high speed and moderate power consumption. Furthermore, the conventional comparator circuit can be also optimized easily due to its simple architecture.

The circuit has two stages with an output inverter. The first stage is NMOS differential pair (NM0 and NM1) which is driven by tail current transistor NM2. The reference voltage applied at transistor NM1 and the input voltage applied at transistor NM0. The range of input voltage of this conventional comparator is from 0 to 1.2 V. The reference voltage is set to 0.6 V. The bias voltage of the transistor gate NM2 which acts as the tail current transistor is 0.35 V. The transistors PM0 to PM2 are diode load to the differential pair because of the drain and the gate are shorted together. The second stage, PM3, a common source amplifier is used to contribute for the overall gain of the amplifier. The final stage consists of PM4 and NM5 which is the push-pull inverter acting as an output driver of the comparator [5]. Parametric analysis has been utilized to determine the general size of the NMOS and PMOS transistor size.

In addition, for the design of comparator with reduced VDD, the same exact circuit of Fig. 1 is used with the power supply reduced to 0.9 V.

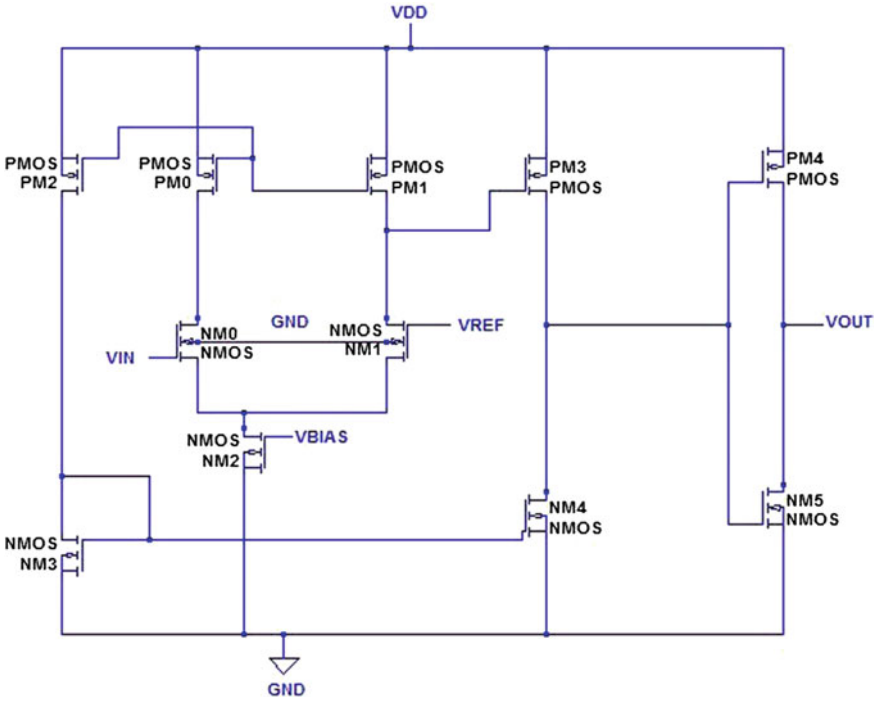

Fig. 1 Conventional comparator [5]

2.2 DTTS Comparator Design

Figure 2 shows the comparator schematic with DTTS technique. The DTTS is a technique that has both the benefits of Multi Threshold CMOS (MTCMOS) and stack transistor [4, 6]. DTTS is chosen because of its capability of reducing the leakage power and also giving less impact on the propagation delay of the comparator. The sleep transistor is built with high threshold voltage with reduced in size which is turned off during inactive state. The transistor is designed as high threshold voltage by increasing the body effect. Based on Eq. 1, by increasing the V_{SB}, the source bulk voltage, the threshold voltage of the transistor can be increased.

$$V_{TH} = V_{TO} + \gamma\sqrt{|V_{SB} + 2\varnothing_F|} - \sqrt{|2\varnothing_F|} \tag{1}$$

where

V_{TH} = threshold voltage, V_{SB} = source-to-body substrate bias

$2\varnothing_F$ = is the surface Fermi potential, V_{TO} = threshold voltage for zero substrate bias

The leakage current can be reduced by using high V_{TH} transistors during idle mode. From Eq. 2, it shows that by using high threshold voltage transistor the

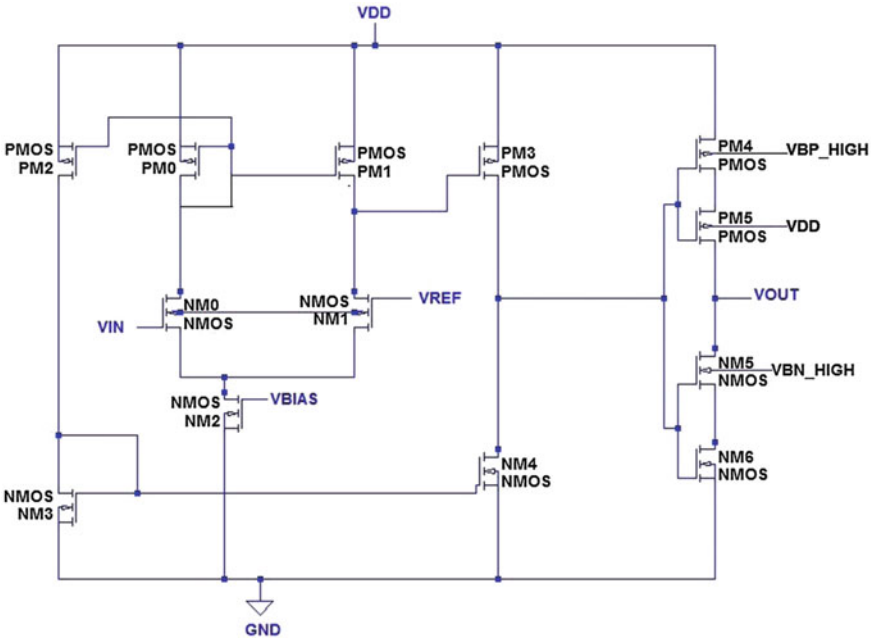

Fig. 2 Comparator with DTTS technique

sub-threshold leakage is reduced. This is because sub-threshold leakage is considered as major contribution of static power in circuit.

$$I_{SUB} = K(W/L)\, e^{(VGS - VTH)/(nVT)} \left(1 - e^{-VDS/VT}\right) \tag{2}$$

where

K = Boltzmann's constant (1.38×10^{-23} J/K), n = Technology parameter, W/L = width/length, V_{TH} = threshold voltage, V_{DS} = drain-source voltage, V_{GS} = gate-source voltage, V_T = thermal voltage

During active state, transistors PM4, PM5, NM5 and NM6 are 'ON' and 'OFF' in idle state. During idle state, there is no current flowing through the circuit. The leakage of two OFF transistors that in series used in DTTS is much lower than that of single transistor due to stack effect and design of high threshold voltage of sleep transistors.

The two extra transistors, PM4 and NM5 are used for implementing DTTS. The size of transistor PM4, PM5, NM5 and NM6 are divided into half compared to other transistors in the circuit. The sleep transistor PM4 and NM5 are designed as high threshold voltage in this circuit. This is done by applying different body biasing at the bulk of transistor PM4 and NM5.

2.3 MTSCStack Comparator Design

Figure 3 shows the circuit of comparator with MTSCStack approach. This technique is used due to its capability to decrease leakage power by shutting down the logic block during idle state. In addition, it also has the benefits of retaining the exact logic when the comparator goes idle. In this circuit, there are extra four transistors which consist of two PMOS transistors (PM5 and PM6) and two NMOS transistors (NM6 and NM7) compared to the conventional comparator.

The sleep signal is going low while the sleep bar signal goes high during active mode. Therefore, the sleep transistors PM5 and NM7 turned on where the circuit operates as normal. During this mode, the leakage power is reduced due to the stack effect.

The sleep signal is turned high during sleep mode and the sleep bar signal is turned low. As a result, all transistors are turned off except NM6 and PM6 that gives the circuit the ability to retain the logic states.

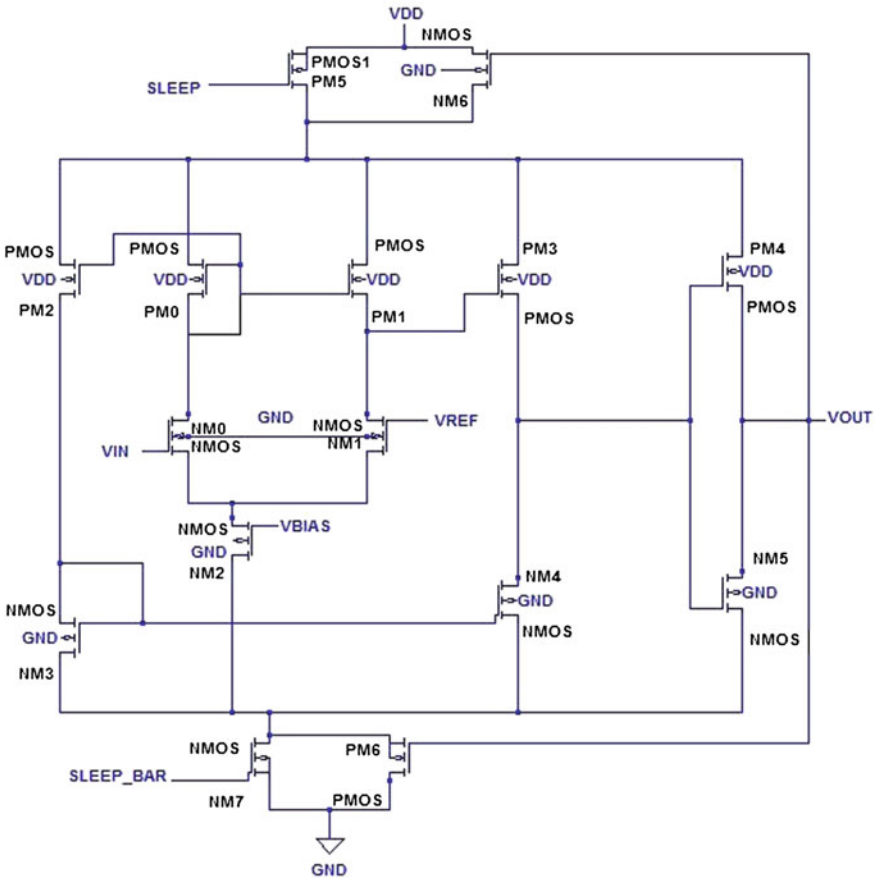

Fig. 3 Comparator with MTSCStack approach

From Eq. 2, it shows that V_{GS} affecting the amount of sub-threshold leakage. Hence, by using a slight negative gate voltage for sleep bar signal, the leakage can be reduced dramatically.

In order to maintain high value in ideal mode, NM6 transistor is designed in parallel to the PM5 sleep transistor as the only source of V_{DD}. Likewise, to maintain a low value in idle mode, PM6 transistor is designed in parallel to the NM7 sleep transistor as the source of GND. Thus, MTSCStack approach not only reducing the leakage power of the circuit but also help to retain the exact logic state of the circuit.

2.4 Proposed Comparator Design

Figure 4 shows the proposed comparator circuit using a combination of DTTS and MTSCStack techniques as well as reduced VDD. DTTS and MTSCStack

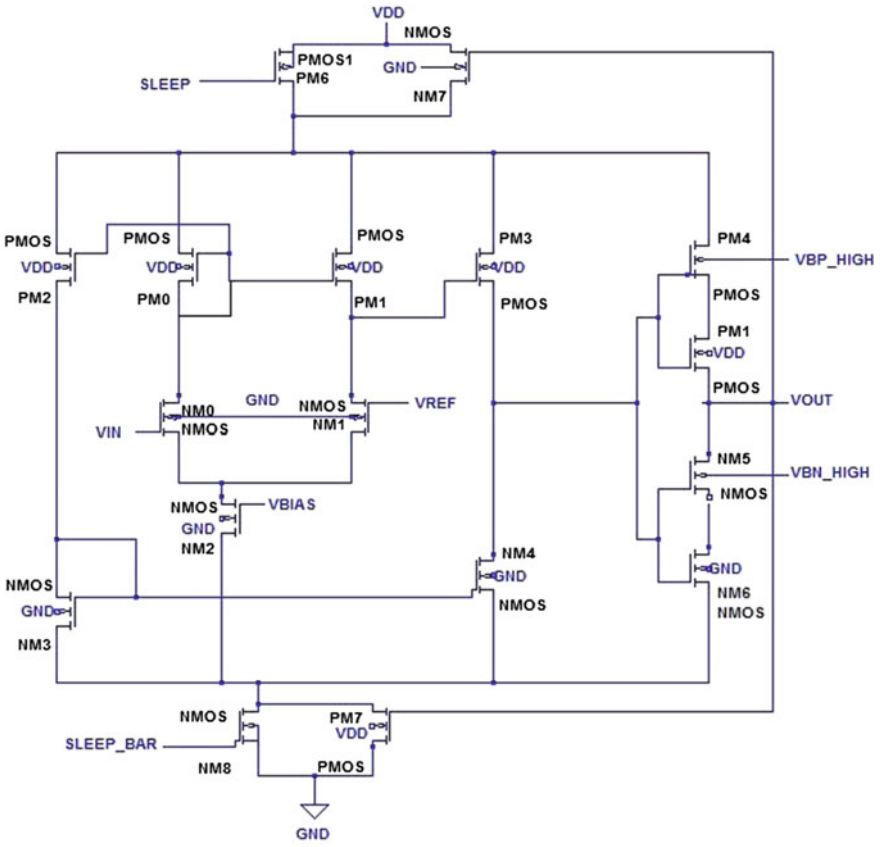

Fig. 4 Proposed comparator

Table 1 Transistor width and length of proposed comparator

Transistor	Length (nm)	Width (μm)
PM(0-1), NM(0-2)	200	2
PM(2-3), PM(6-7) NM(3-4), NM(7-8)	130	2
PM4-5, NM5-6	130	1

techniques are combined to see if the leakage power can be reduced even more compared to the use of only one single technique. Besides, $V_{DD} = 0.9$ V has been used in the proposed comparator circuit in order to reduce the total power consumption especially dynamic power of the comparator circuit.

In the proposed comparator, transistor NM8 and PM6 act as the sleeping transistors that will shut down the logic block during idle state while NM7 and PM7 are the transistor that tied parallel to sleep transistors to retain the exact logic state. Table 1 shows the transistor sizing for all the transistors used in the proposed comparator.

3 Simulations Results

Table 2 shows the total power, dynamic power and the static power consumption for conventional comparator, reduced V_{DD} conventional comparator, comparator with MTSCStack, comparator with DTTS and the proposed comparator. The comparator with MTSCStack technique shows the huge improvement in static power consumption compared to other techniques. This is because the entire transistor is turned off except transistor NM7 and PM7 to retain the logic state of the comparator.

From Table 2, it shows that proposed comparator managed to decrease up to 99.2 % in static power consumption. On the other hand, the percentage of static power reduction of comparator with MTSCStack techniques shows significant result compared to comparator with reduced V_{DD} and comparator with DTTS.

The layout drawn is shown in Fig. 5. The overall size of the comparator layout is 48 μm × 22 μm. Large area used for the layout due to one NMOS transistor is

Table 2 Power consumption of the comparator

Comparator	V_{DD}	V_{REF}	Static power	Dynamic power (μW)	Total power (μW)
Conventional comparator	1.2 V	0.6	88.40 nW	38.47	38.56
Comparator with reduced V_{DD}	0.9	0.45	40.65 nW	21.70	21.74
Comparator with MTSCStack	1.2 V	0.6	3.4 nW	48.07	48.07
Comparator with DTTS	1.2 V	0.6	80.20 nW	34.38	34.46
Proposed comparator	0.9	0.45	705 pW	16.84	16.84

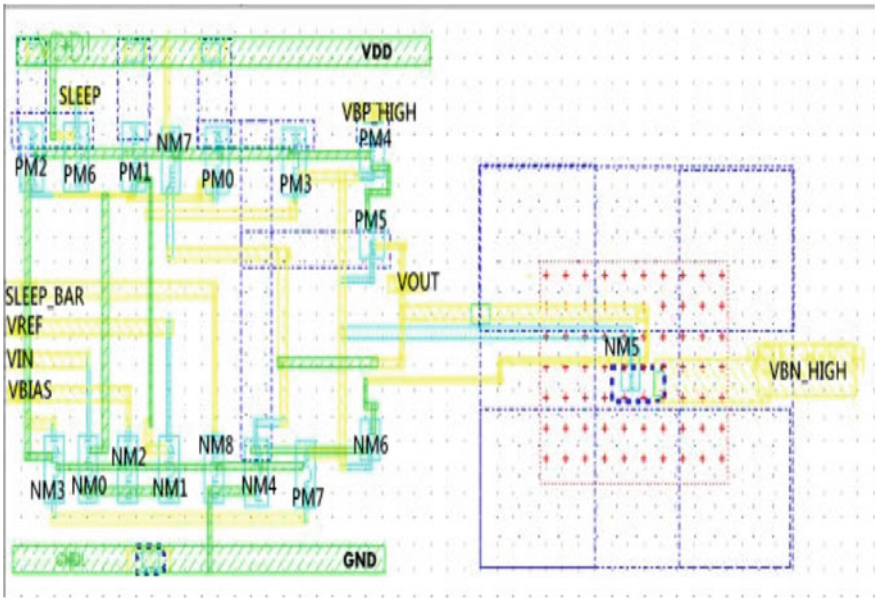

Fig. 5 Layout of proposed comparator

isolated for applying different body biasing as other body of the NMOS is tied to the ground. The transistor NM5 is isolated by placing Deep-nwell as a substrate isolator layer.

Table 3 shows the characteristic comparison between pre-layout and post-layout proposed comparator. It also shows that the offset, voltage gain and resolution of post-layout proposed comparator are similar with pre-layout proposed comparator. In contrast, the propagation delay and power consumption are slightly higher in post layout proposed comparator compared to pre-layout. The propagation delay increased from 0.78 to 1.08 ns. For the static power, result shows a slight increase of 92 pW while dynamic power is increased from 16.83 to 17.55 µW. This is because post-layout simulation includes the parasitic RC extraction. However, the parasitic RC extraction does not have big effect on the post-layout proposed comparator as the design is very small and there is no load capacitance.

Table 3 Power consumption of post-layout proposed comparator

Characteristic		Pre-layout	Post-layout
Output high/low voltage		880 mV/1.24 µV	880 mV/1.24 µV
Input high/low voltage		450 mV/432 mV	450 mV/432 mV
Offset/resolution		8.8 mV/18 mV	8.8 mV/18 mV
Gain/delay		49/0.78 ns	49/1.08 ns
Power consumption	Static	705 pW	797 pW
	Dynamic	16.83 µW	17.55 µW

4 Conclusion

This article discussed a proposed comparator with MTSCStack, DTTS with reduced VDD which shows a relatively high speed comparator with low power consumption. The dynamic and static power of the comparator in post-layout simulation is 17.55 μW and 797 pW respectively. The combination of MTSCStack and DTTS techniques shows a very significant result in reducing the static power of up to 99.2 %. This is a significant improvement especially for the circuit design that uses technology file in nanometer range. Besides that, MTSCStack technique provides ability to maintain the exact logic state in idle mode; while, DTTS technique reduces the static power without affecting other performance of the comparator such as delay. Also, it is shown that one of the best way of decreasing the power consumption for both static power and dynamic power is by reducing the supply voltage of the comparator.

Besides large reduction in power consumption, the proposed comparator has a very good performance on the resolution and offset. The offset of the comparator is only 8.8 mV while resolution is 18 mV. The delay of proposed comparator is higher compared to conventional circuit. However, delay is out of scope in this study. This is because as the power consumption of the comparator becomes smaller, the switching energy in comparator decreases. The low switching energy caused the delay to be increased.

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