Stability Criteria for Classical Digital Phase-Locked Loops

Siti Juliana Abu Bakar and Nur Syazreen Ahmad

Abstract A Classical Digital Phase-Locked Loop (CDPLL) is a hybrid system as it contains both analog and digital components. For a CDPLL with an XOR-gate phase detector (PD), it is useful to analyse its stability since its performance is affected by the nonlinear behavior of the PD. This paper presents the stability analysis of CDPLL in continuous and discrete-time domains. Four criteria are used, Circle and Popov for continuous-time domain, and Tsypkin and Jury-Lee for the discrete-time domain. Numerical examples are included to show the different stability margins provided by the aforementioned criteria.

Keywords Classical Digital Phase-Locked Loop ⋅ Popov ⋅ Circle ⋅ Tsypkin ⋅ Jury-Lee

1 Introduction

Phase locked-loop (PLL) has been widely used in communication systems and electronic applications particularly for clock generation, clock recovery and frequency synthesis [\[1,](#page-5-0) [2](#page-5-1)]. There are different types of PLLs such as analog PLL, classical digital PLL (CDPLL), all-digital PLL (ADPLL) and software PLL (SPLL) [\[3](#page-6-0)]. Each type is different based on the components integrated in the system.

A basic PLL can be easily constructed by using a phase detector (PD), a loop filter (LF) and a voltage controlled oscillator (VCO) [\[4\]](#page-6-1). Its fundamental operation is to synchronize the VCOs output frequency with the reference signals frequency which typically comes from an oscillator. The PD plays a very important role in comparing the frequencies and phases of the input and output signals as it needs to

S.J. Abu Bakar (✉) ⋅ N.S. Ahmad

School of Electrical and Electronic Engineering, Engineering Campus, Universiti Sains Malaysia, 14300 Penang, Malaysia e-mail: sjab15_eee017@student.usm.my

N.S. Ahmad e-mail: syazreen@usm.my

© Springer Science+Business Media Singapore 2017

427

H. Ibrahim et al. (eds.), *9th International Conference on Robotic, Vision, Signal Processing and Power Applications*, Lecture Notes in Electrical Engineering 398, DOI 10.1007/978-981-10-1721-6_46

adjust its action in order to ensure the differences are minimized. The LF is used to remove the high frequency components of the phase detector output and also the high frequency noise. When the two signals (reference signal and oscillators output signal) are equal in frequency, the error remains constant and the loop is said to be in a locked condition.

Although many applications are based on linearized models of PLL [\[5](#page-6-2), [6\]](#page-6-3), the approximation is not valid in general as the actual PLL is inherently nonlinear [\[7,](#page-6-4) [8\]](#page-6-5). This is mainly due to the behavior of the PD and the VCO. In this paper, the focus is on the CDPLL with an XOR-gate type PD. The PD is considered as the main source of nonlinearity and the VCO is assumed to be working in its linear range. It is therefore useful to analyze the stability of the system as its performance is affected by the nonlinearity. Since it is a hybrid system (i.e. the PD is digital while others are analog), the CDPLL can be modeled either in continuous-time or discrete-time domain with some limitations at high jitter frequency range [\[9](#page-6-6), [10\]](#page-6-7). Both models however can be generalized into a Lur'e system with sector bounded nonlinearity.

Various criteria have been developed to provide sufficient conditions for stability of Lur'e systems in both discrete and continuous-time domain [\[11\]](#page-6-8). For nonlinearities with sector-bound condition, the most common ones in continuous-time domain are circle and Popov criteria [\[12](#page-6-9)], and their discrete counterparts are Tsypkin and Jury-Lee respectively. In this note, these criteria will be used to analyze the stability of CDPLL. The results will also be compared to show different stability margins provided by the aforementioned criteria.

2 Preliminaries and PLL Basics

A basic block diagram of a PLL is shown in Fig. [1.](#page-1-0) The reference signal and the VCO output can be either in the form of square wave or sine wave. Without loss of generality, let the reference and VCO output signals be represented by [\[1\]](#page-5-0);

Fig. 1 Block diagram of a PLL [\[13](#page-6-10)]

$$
V_i(t) = A_1 \sin(-\omega_i t + \theta_i)
$$
 (1)

$$
V_o(t) = A_2 \cos \left(\omega_o t + \theta_o \right) \tag{2}
$$

respectively. When they pass through the PD, the output signal V_d can be calculated as $V_d(t) = -K_m A_1 A_2 \sin(-\omega_i t + \theta_i) \cos(-\omega_o t + \theta_o)$, where K_m is the gain of the mixer. Via trigonometric identity, we have

$$
V_d(t) = \frac{K_m A_1 A_2}{2} (\sin -[(\omega_i + \omega_o)t + \theta_i + \theta_o] + \sin[(\omega_i - \omega_o)t + \theta_i - \theta_o]).
$$
 (3)

By including a low pass filter, the high frequency component which is $sin[(\omega_i +$ ω_0)*t* + θ _i + θ _o] can be attenuated, leaving only low frequency component. Hence, the output of the PD can be written as $V_d(t) = K_d \sin[(\omega_i - \omega_o)t + \theta_i - \theta_o]$, where $K_d = (K_m A_1 A_2)/2$ is the gain in rad/V.

If the loop is locked, then $\omega_i = \omega_o$, and the output of the PD can be approximated by $V_d(t) \approx K_d \sin \theta_d$, where $\theta_d = \theta_i - \theta_o$ is the phase error. As for the VCO, the frequency at which it oscillates is determined by the output signal of the loop filter. The angular frequency is given by $\omega_2(t) = \omega_0 + K_0 V_f(t)$, where ω_0 is the center frequency of the VCO and K_0 is the VCO gain in rad $s^{-1}V^{-1}$. The phase of the VCO output is $\theta_o(t) = K_o \int_0^t V_f(t) dt$, which is equivalent to $\theta_o(s)/V_f(s) = K_o/s$ in Laplace domain. Due to this, the PLL will have at least one pole at the origin in the loop as illustrated in Fig. [1.](#page-1-0)

If the phase error is sufficiently small, then linear approximation can be used and the relationship between the input and output is given by $\theta_o(s)/\theta_i(s) = K_dK_oF(s)/\theta_i(s)$ $(s + K_d K_c F(s))$. In this case, the Nyquist criterion can be used to test the stability of the system. However if the phase error is large enough, linear approximation will no longer be valid.

For the purpose of stability analysis, the components in Fig. [1](#page-1-0) are rearranged as in Fig. [2](#page-2-0) where all linear components are placed in the forward path and the nonlinear component, denoted by ϕ , is placed in the feedback path. The nonlinearity function

Fig. 2 Rearrangement into linear and nonlinear components in phase space

 ϕ , which comes from the characteristic of the XOR-gate, belongs to the first and third quadrants of the plane as shown in Fig. [3](#page-3-0) [\[1](#page-5-0)]. Its input, represented by θ_d , is the phase difference between θ_i and θ_o .

3 Stability Analysis of CDPLL

Based on Fig. [2,](#page-2-0) the state space of the LTI block is given by $H \sim (A, B, C, 0)$ and the static, memoryless nonlinearity $\phi : \mathbb{R} \longrightarrow \mathbb{R}$ satisfies the sector condition:

$$
0 \le \frac{\phi(y)}{y} \le K, \qquad \forall y \ne 0 \tag{4}
$$

where $K > 0$ is the upper sector bound and $\phi(0) = 0$. Its slope bound can also be described as:

$$
-K \le \frac{\phi(y) - \phi(x)}{y - x} \le K, \qquad \forall y \ne x. \tag{5}
$$

The stability criteria suitable for such a system in both continuous and discrete-time settings are presented separately in the following subsections.

3.1 Continuous-Time Domain

Consider the feedback system as shown in Fig. [2,](#page-2-0) where the nonlinearity $\phi(y)$ is described as in [\(4\)](#page-3-1). The system is stable if:

$$
Re[G(j\omega) + K^{-1}] > 0, \qquad \forall \omega \in \mathbb{R}.
$$
 (6)

The condition in [\(6\)](#page-3-2) corresponds to the circle criterion which is applicable for Lur'e system with a nonlinearity that is sector-bounded, and possibly time-varying. If the nonlinearity is additionally static and time-invariant, then the condition:

$$
Re[(1+j\omega q)G(j\omega)] + K^{-1}] > 0, \qquad \forall \omega \in \mathbb{R}, \qquad q \in \mathbb{R}
$$
 (7)

is sufficient to provide the stability of the system. The condition [\(7\)](#page-4-0) corresponds to the Popov criterion where it reduces to circle criterion when $q = 0$ [\[14\]](#page-6-11).

3.2 Discrete-Time domain

In discrete-time domain, the loop filter and voltage controlled oscillator is combined together and transformed directly into *z*-domain via impulse invariant method [\[15](#page-6-12)]. Similar to the Circle criterion, its discrete-time counterpart namely Tsypkin criterion is stated as follows [\[16](#page-6-13)]:

$$
Re[G(z) + K^{-1}] > 0 \t\t \forall |z| = 1 \t\t (8)
$$

where $G(z)$ is the LTI system in discrete-time settings.

With regard to Popov criterion, one of its discrete-time counterparts suitable for such a system is as follows:

$$
Re[K^{-1} + (1 + (z - 1)n)G(z) - \frac{n}{2} | (z - 1)G(z)|^{2}] > 0 \qquad \forall |z| = 1 \tag{9}
$$

where $n \in \mathbb{R}$ [\[17\]](#page-6-14). Unlike Popov criterion, the condition derived in [\(9\)](#page-4-1) is also based on the slope restriction of ϕ , as described in [\(5\)](#page-3-3).

4 Numerical Examples

In this section, we analyze the maximum loop gain of CDPLL for which the system remains stable. This is also equivalent to searching for maximum sector/slope bound (i.e. *K*) of the system. For the first example, consider the feedback system in Fig. [2](#page-2-0) consisting of a third order Butterworth filter and a VCO, the corresponding continuous-time transfer function is given by:

$$
H_1(s) = \frac{1}{s} \left[\frac{1}{s^3/\omega_c^3 + 2s^2/\omega_c^2 + 2s/\omega_c + 1} \right]
$$
(10)

where $\omega_c = 10$ Hz is the cut-off frequency. The discrete-time model is obtained by transforming $H_1(s)$ into $H_1(z)$ via impulse invariant method with sampling time of 0.1 s. For the second example, the same feedback system is considered but with a fourth order Butterworth filter. The transfer function is then:

Stability criterion		Maximum gain K		
		$H_1(.)$	$H_2(.)$	
Continuous-time	Circle	2.0003	0.2959	
	Popov	5.5275	1.4161	
Discrete-time	Tsypkin	3.4592	3.0221	
	Jury-Lee	7.5093	5.7195	
Nyquist		7.5758	5.7471	

Table 1 Comparison results

$$
H_2(s) = \frac{1}{s} \left[\frac{1}{s^4/\omega_c^4 + 2.6132s^3/\omega_c^3 + 3.4143s^2/\omega_c^2 + 2.6132s/\omega_c + 1} \right] \tag{11}
$$

and the discrete-time model for $H_2(z)$ is obtained via the same method.

The results are compared in Table [1.](#page-5-2) For both examples, the result via linear approximation method (Nyquist criterion) is included to show the highest gain *K* that may be achieved. From the results, both examples show that the gain *K* obtained via Tsypkin and Jury-Lee criteria are higher compared to Circle and Popov criteria. The gain *K* for Jury-Lee is higher than Popov criterion due to the fact that the slope restriction of the nonlinearity is included in its derivation of criterion, making it less conservative than Popov criterion.

5 Conclusion

In this work, we have shown four different criteria (Circle, Popov, Tsypkin and Jury-Lee) which are suitable to analyze the stability of CDPLL when the nonlinearity is taken into account. As the CDPLL is considered as a hybrid system, it can be modeled either in *s*-domain or *z*-domain for stability analysis purposes. Based on the examples given, it is demonstrated that the discrete-time criteria can give much better stability margins as compared to their continuous-time counterparts. For future works, the result can be used to design the CDPLL such as the filter with certain performance specifications.

Acknowledgments This work was supported by FRGS (203/PELECT/6071267), Ministry of Education of Malaysia.

References

- 1. Abramovitch D (2002) Phase-locked loops: a control centric tutorial. In: Proceedings of the 2002 American control conference, vol 1, pp 1–15
- 2. Abramovitch DY (1990) Lyapunov redesign of analog phase-lock loops. IEEE Trans Commun 38:2197–2202
- 3. Wickert MA (2011) Phase-locked loops with applications, ECE 5675/4675 Lecture Notes
- 4. Best RE (1993) Phase-locked loops: theory, design, and applications. McGraw-Hill, New York
- 5. Li W, Meiners J (2000) Introduction to phase-locked loop system modeling. Analog Appl J 510
- 6. Hsieh GC, Hung JC (1996) Phase-locked loop techniques—a survey. IEEE Trans Ind Electron 43(6):609–615
- 7. Kuznetsov NV, Leonov GA, Yuldashev MV, Yuldashev RV (2014) Nonlinear analysis of classical phase-locked loops in signals phase space. In: IFAC proceedings volumes (IFAC-PapersOnline), vol 19, pp 8253–8258
- 8. Gardner FM (2005) Phaselock techniques, 3rd edn. Wiley, New York
- 9. Laboratories S (2010) Jitter attenuation—choosing the right phase-locked loop bandwidth, AN513 Rev 0.1 6/10
- 10. Lu J, Grung B, Anderson S, Rokhsaz S (2001) Discrete Z-domain analysis of high order phase locked loops. In: Proceedings of IEEE international symposium on circuits and systems, vol 1, pp 260–263
- 11. Park P, Kim SW (1998) A revisited Tsypkin criterion for discrete-time nonlinear Lur'e systems with monotonic sector-restrictions. Automatica 34:1417–1420
- 12. Wu NE (1998) Circle/Popov criteria in phaselock loop design. In: Proceedings of the 1998 American control conference, AACC. IEEE, Philadelphia, Pennsylvania, pp 3226–3228
- 13. Best RE (2003) Phase-locked loops: design, simulation, and applications, 5th edn. McGraw-Hill
- 14. Vidyasagar M (1993) Nonlinear systems analysis, 2nd edn. Prentice Hall, New York
- 15. Hein J, Scott J (1988) *Z*-Domain model for discrete-time PLL's. IEEE Trans Circuit Syst 35(11):1393–1400
- 16. Tsypkin YZ (1962) On the stability in the large of nonlinear sampled-data systems. Doklady Akademii Nauk SSSR 145:5255
- 17. Jury EI, Lee BW (1964) On the stability of a certain class of nonlinear sampled-data systems. IEEE Trans Autom Control 9:51–61