Chapter 9
Oscillator Design for Variability

9.1 Mixed-Mode Device and Circuit Simulation

To evaluate the physical insight into the Colpitts oscillator circuit operation, the mixed-mode device and circuit simulation using Sentaurus TCAD software [1] is adopted. In Sentaurus device simulation, Poisson's and continuity equations with drift-diffusion transport are implemented. The Shockley–Read–Hall carrier recombination, Auger recombination, and impact ionization models are used. The physical model for impact ionization used in this work is the University of Bologna impact ionization model, based on impact ionization data generated by the Boltzmann solver [2]. It covers a wide range of electric fields (50–600 kV/cm) and temperatures (300–700 K). It is calibrated against impact ionization measurements in the whole temperature range [3]. The low field mobility is calculated by Mathiessen's rule and incorporates the bulk and surface mobility. To account for lattice heating, Thermodynamic, Thermode, RecGenHeat, and AnalyticTEP models in Sentaurus are included. The thermodynamic model extends the drift-diffusion approach to account for electrothermal effects. A Thermode is a boundary where the Dirichlet boundary condition is set for the lattice. RecGenHeat includes generation–recombination heat sources. AnalyticTEP gives the analytical expression for thermoelectric power.

Figure 9.1 shows the Colpitts oscillator used in the mixed-mode device and circuit simulation [4]. The mixed-mode simulation provides the device physical insight and response in the practical circuit environment. In Sentaurus simulation, the MOSFET has the channel length of 65 nm and the channel width of 64 μm. The circuit parameters used are C_1 = 22 pF, C_2 = 27.2 pF, L_D = 0.15 nH, R_D = 2900 Ω, R_S = 40 Ω, V_G = 1.8 V, and V_{DD} = 3.3 V. The simulated oscillator output response from Sentaurus is displayed in Fig. 9.2. The oscillator has a sinusoidal oscillating

J.-S. Yuan, *CMOS RF Circuit Design for Reliability and Variability*,
SpringerBriefs in Reliability, DOI 10.1007/978-981-10-0884-9_9

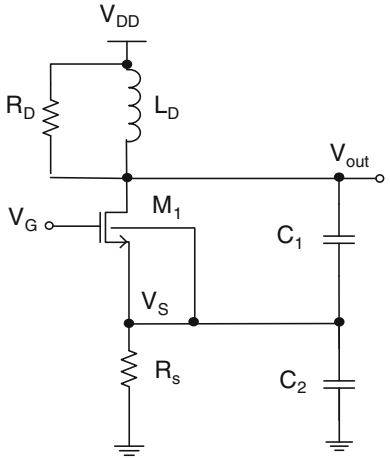

Fig. 9.1 Schematics of an oscillator used in the mixed-mode device and circuit simulation

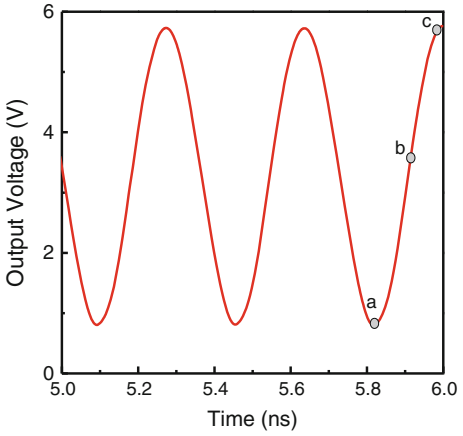

Fig. 9.2 Oscillator output response from mixed-mode device and circuit simulation (© IEEE)

output waveform from 0.5 to 2.9 V. To analyze the reliability effect on the Colpitts oscillator, gate-source voltage and drain-source voltage as a function of time are depicted in Fig. 9.3. Examining the voltage waveforms in Fig. 9.3, one can define three key points *a*, *b*, and *c* (i.e., the bottom, middle, and top of the output voltage) to probe impact ionization and self-heating at these three critical time points. The I.I. rates, electric field, and total current density from Sentaurus mixed-mode device and circuit simulation are plotted in Figs. 9.4, 9.5, and 9.6, respectively. Note that no lattice heating of the Colpitts oscillator was observed in mixed-mode device and circuit simulation (data not shown).

To investigate the physical insight into hot electron injection, impact ionization rates at the three different time points are shown in Fig. 9.4. At point *a* the drain-source voltage reaches the minimum and its corresponding electric field is low; however, the current density is very high due to large V_{GS} (see Fig. 9.5). At

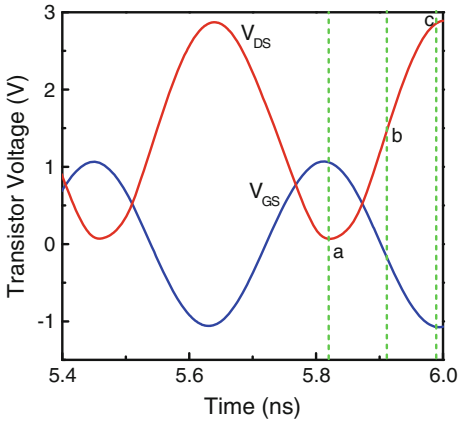

Fig. 9.3 Gate-source and drain-source voltages versus time (© IEEE)

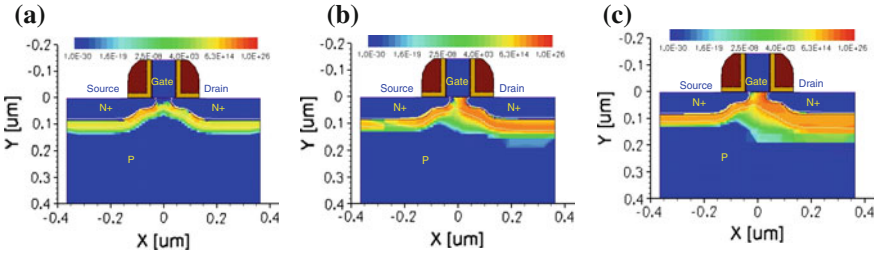

Fig. 9.4 Impact ionization rates at points *a*, *b*, and *c* in Fig. 9.2 (© IEEE)

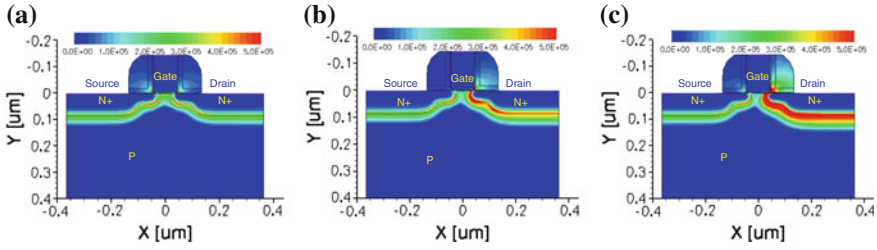

Fig. 9.5 Electric field at points *a*, *b*, and *c* in Fig. 9.2 (© IEEE)

point *c*, the I.I. rates are high because the drain-source voltage reaches the maximum. The impact ionization rates at point *b* are higher than those at points *a*. This is attributed to relatively high drain-source voltage and drain current density at point *b*, as indicated in Fig. 9.3. Higher drain current enhances I.I. generated carriers under high electric field. The peak impact ionization rates at points *b* and *c* reach $1 \times 10^{26}/\text{cm}^3/\text{s}$, a precursor of hot carrier effect. The hot electron reliability issue

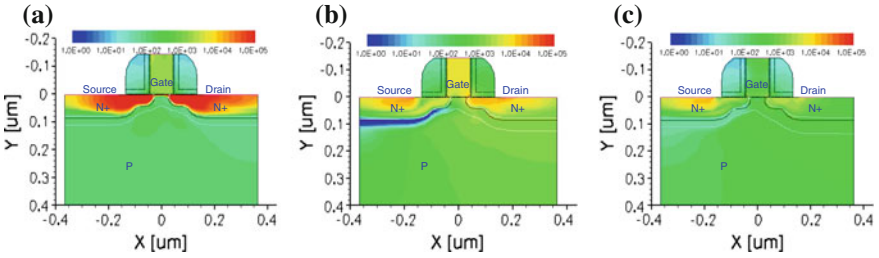

Fig. 9.6 Total current density at points *a*, *b*, and *c* in Fig. 9.2 (© IEEE)

becomes even more important when the channel length of the nMOSFET is decreasing and the supply voltage of the circuit is increasing.

The phase noise of Colpitts oscillator shown in Fig. 9.1 is analyzed for examining device parameter variations. The phase noise to account for MOS transistor parameter drift due to aging is expressed as [5]:

$$L(\Delta f) = 10\log\left(\frac{\bar{V}_n^2}{2\bar{V}_{\text{tank}}^2}\right) = 10\log\left\{\left[\left(\frac{\left|g_{m(1)}\right|^2 K_f}{4C_{\text{ox}}WL\Delta f} + \sum_{n=1}^{\infty}\left|g_{m(n-1)} + g_{m(n+1)}\right|^2 \times \frac{kT\gamma}{\bar{g}_m}\right)\alpha + \frac{kT}{R}\right]\left(\frac{Rf_0}{Q\Delta f A_S}\right)^2\right\} \tag{9.1}$$

where V_n is the output noise voltage, V_{tank} is the signal voltage of the oscillator output, $g_{m(n)}$ is the nth Fourier coefficients of transconductance, K_f is a process dependent constant on the order of 10^{-25} V^2F, f_0 is the center frequency, γ is a coefficient (about 2/3 for long-channel transistors and larger for submicron MOSFETs), $\bar{g}_m$ is the average transconductance of the transistor, α is the transfer parameter from nonlinear network port to linear network port ($\alpha = (1 - F)^2$, where $F = C_1/(C_1 + C_2)$), R is the parasitic resistance in the LC tank, Q is the quality factor of LC tank, and A_S is the amplitude of the AC voltage at the source of the transistor.

In (9.1) $\bar{g}_m = \beta A_S(\sin\theta - \theta\cos\theta)/\pi$, $\beta = \mu_{n0}C_{\text{ox}}W/L$, $\theta = \cos^{-1}[(V_T - V_G)/A_S\}$, $\beta = \mu_{n0}C_{\text{ox}}W/L$, $g_{m(n)} = g_{m(-n)}$, and

$$g_{m(n)} = \begin{cases} \beta A_S\left[\frac{(\sin\theta - \theta\cos\theta)}{\pi}\right] & \text{for } n = 0 \\ \beta A_S\left[\frac{(\theta - \sin\theta\cos\theta)}{\pi}\right] & \text{for } n = 1 \\ 2\beta A_S\left[\frac{\sin n\theta\cos\theta - n\cos\theta\sin\theta}{n(n^2-1)\pi}\right] & \text{for } n \geq 2 \end{cases} \tag{9.2}$$

The Colpitts oscillator shown in Fig. 9.1 has been simulated in ADS. To be consistent with the mixed-mode simulation condition, the same circuit element values used in mixed-mode simulation are also used in the ADS circuit simulation. The simulated output waveform as a function of time and its Spectral density versus

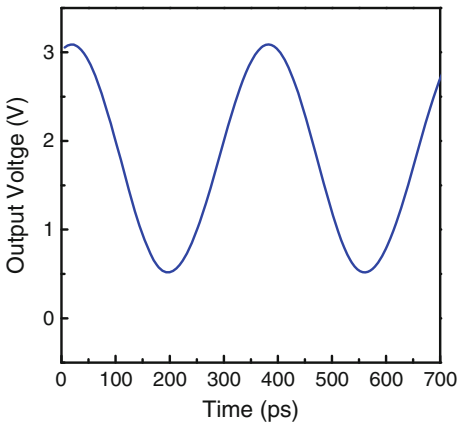

Fig. 9.7 Simulated output waveform versus time

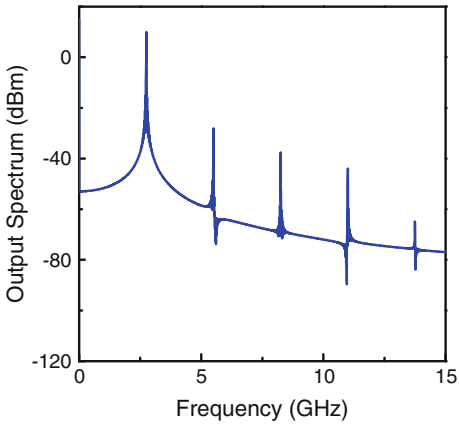

Fig. 9.8 Simulated output power spectrum characteristics

frequency are depicted in Figs. 9.7 and 9.8. The oscillation frequency measured from Fig. 9.7 is 2.4 GHz and its fundamental signal Spectral power is −4 dBm at 2.4 GHz. The phase noise predicted by the analytical equation in (9.1) is compared with that by the ADS simulation result in Fig. 9.9. In Fig. 9.9, the solid circles represent the model predictions and the solid line represents the ADS simulation. A good agreement between the model predictions and ADS simulation results before hot electron stress is obtained. The HCI effect on the phase noise is also displayed using K_f factor in (9.1). As seen in Fig. 9.9 the phase increases with increasing K_f factor, which is related to the interface quality or interface states between the SiO_2 and Si interface. Intuitively, the worse the process condition, the larger is the interface states. The longer the stress time, the larger is the interface trap density [6]. If the analytical equation on process and stress dependent K_f factor becomes available, Eq. (9.1) can account for more process and stress effects

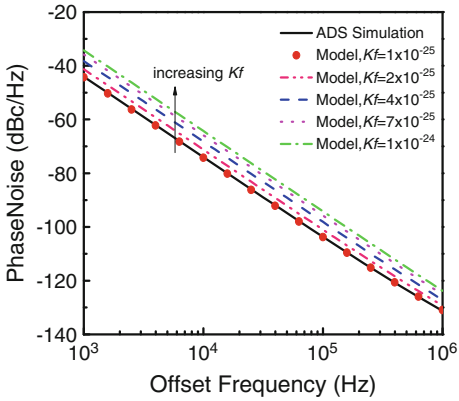

Fig. 9.9 Phase noise modeling versus offset frequency including K_f effect

inclusively. As hot carriers generate more interface states at the SiO_2 and Si interfacial layer, the K_f factor increases, thus the $1/f$ noise of the MOSFET and phase noise of the oscillator increase.

9.2 Process Variability and Adaptive Body Bias

RDF [7] remains the dominant source of statistical variability and is mainly caused by silicon dopant fluctuations during fabrication process. It becomes more severe as device size shrinks. LER [8], a random deviation of line edges from gate definition, does not scale with line width. PGG [9] is attributed to gate dielectric thickness variations which contribute to threshold voltage variation. All the above mentioned process variations cause fluctuation of threshold voltage, mobility, and oxide thickness, which in turn affect the device and circuit performance. Furthermore, reliability issue could widen the standard derivation of process variation in Gaussian distribution [10].

To further examine the process variation and reliability impact on Colpitts oscillator, Monte Carlo (MC) circuit simulation has been performed. In ADS, the Monte Carlo simulation assumes statistical variations (Gaussian distribution) of transistor model parameters such as the threshold voltage, mobility, and oxide thickness. After Monte Carlo simulations with a sample size of 1000, the phase noise variation is displayed in Fig. 9.10. In this histogram plot, the x-axis shows the phase noise distribution of the oscillator without body effect and y-axis displays the probability density of occurrence. The mean value of phase noise is −121 dBc/Hz and the standard deviation is 0.71 dBc/Hz. In Monte Carlo simulation, the initial values of V_{T0}, μ_0, and t_{ox} are 0.42 V, 491 cm^2/V s, and 1.85 nm, respectively. The statistical variations for V_{T0}, μ_0, and t_{ox} are set at ±10, ±5, and ±3 % from 65 nm technology node.

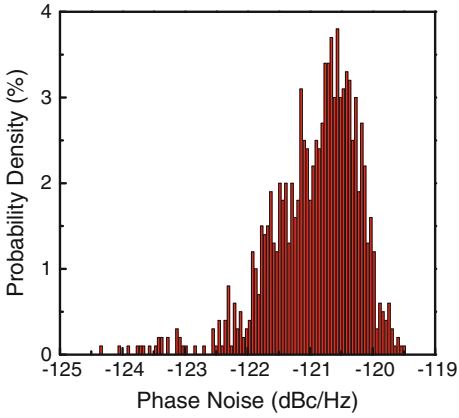

Fig. 9.10 Phase noise distribution @ $\Delta f = 400$ kHz (© IEEE)

To reduce the process variation effect on the Colpitts oscillator, an adaptive body bias scheme as shown in Fig. 9.11 is proposed. In Fig. 9.11, the body bias of $M1$ is determined by the adaptive body bias circuit in the dashed oval circle.

To account for the body bias effect, the threshold voltage of $M1$ can be written as

$$V_T = V_{T0} + \gamma_b \left(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F} \right) \tag{9.3}$$

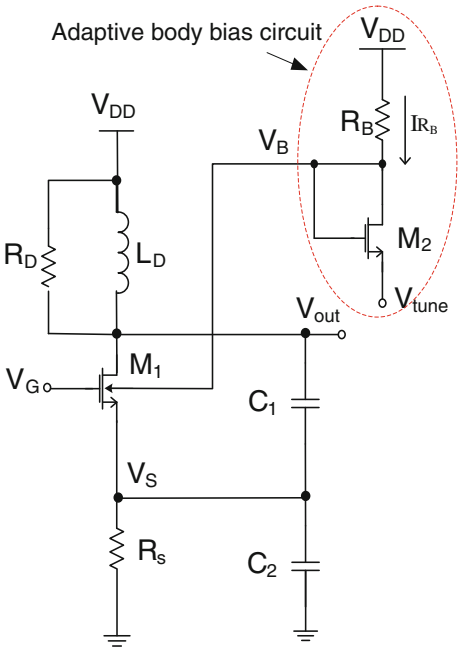

Fig. 9.11 Colpitts oscillator with adaptive body bias (© IEEE)

where V_{BS} is the body-source voltage. Note that the source voltage V_S in this circuit is not necessarily equal to zero, unlike the case of power amplifiers in Chap. 8.

The drain current of the MOSFET including the body bias effect can be approximated as

$$I_{DS} \approx \frac{\mu_{n0} C_{\mathrm{ox}} W}{2L[1 + \theta_1 (V_{GS} - V_T) + \theta_2 V_{\mathrm{BS}}]} (V_{GS} - V_T)^2 \tag{9.4}$$

The transconductance based on the derivative of drain current with respect to gate-source voltage is derived as

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\mu_{n0} C_{\mathrm{ox}} W}{2L} \frac{2(V_{GS} - V_T)(1 + \theta_2 V_{\mathrm{BS}}) + \theta_1 (V_{GS} - V_T)^2}{[1 + \theta_1 (V_{GS} - V_T) + \theta_2 V_{\mathrm{BS}}]^2} \tag{9.5}$$

The transconductance equation taking the body bias into account in (9.5) is then used in the phase noise prediction in (9.1) for the oscillator with an adaptive body bias.

The MC simulation result of the Colpitts oscillator including the body bias effect is shown in Fig. 9.12. In this histogram plot, the mean value of phase noise is −121 dBc/Hz and the standard deviation is 0.18 dBc/Hz. The phase noise is evaluated at the offset frequency of 400 kHz.

Comparing Figs. 9.10 and 9.12, the adaptive body bias clearly reduces the oscillator process sensitivity significantly. The use of adaptive body bias to reduce process variability effect on the Colpitts oscillator can be explained as follows: The threshold voltage shift including body bias effect can be expressed as

$$\Delta V_T = \Delta V_{T0} - \frac{\gamma_b \times \Delta V_{\mathrm{BS}}}{2\sqrt{2\phi_F - V_{\mathrm{BS}}}} \tag{9.6}$$

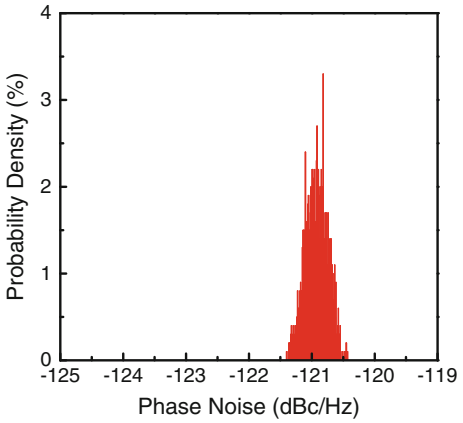

Fig. 9.12 Phase noise distribution using the adaptive body bias scheme (Δf is at 400 kHz) (© IEEE)

where ΔV_{T0} is the threshold voltage change resulting from process variations and ΔV_{BS} is produced due to current variation and the use of body bias circuit. The minus sign of the second term in (9.6) indicates that the body bias effect provides a compensation effect for threshold voltage variations from process uncertainties. Again, when the process variations increase the threshold voltage of M1 in Fig. 9.11, the body bias V_B to $M1$ increases due to less $I_{D2}R_B$ ohmic loss in the adaptive body bias circuit. This tends to decrease the V_{T} in $M1$ to compensate the initial increase in V_T. On the other hand, when process variability decreases the V_T in $M1$, the adaptive body bias circuit will decrease the V_B to $M1$. This in turn increases the V_T in $M1$ to compensate the initial decrease in V_T.

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