Chapter 8
Power Amplifier Design for Variability

It is clear that smaller feature size makes the MOSFET more sensitive to the process variations and stress-induced degradations. The circuit designer needs larger design margin to insure circuit robustness against such issues as yield and reliability. The process variability and reliability resilience design may reduce over design, while increase yield and circuit robustness. The resilient biasing technique aims to design reliable circuits capable of post-process adjustment and insensitive to the transistor parameter degradations over long-term stress effect.

Figure 8.1 shows a simplified variability and reliability resilient biasing design for the power amplifier, which introduces tunable adaptive body biasing.

The right branch of the circuit in Fig. 8.1 controls the body potential of the MOSFET $M1$. Thus, the threshold voltage of $M1$ can be adjusted by the body bias. The voltage source V_{tune} is used for post-fabrication calibration. During the long-term usage, both $M1$ and $M2$ are subject to similar reliability induced threshold voltage and electron mobility shifts. When the V_T of $M2$ increases, the branch current I_{R1} will decrease. The reduction in the branch current leads to an increase in the node voltage V_B. Therefore, the V_T of $M1$ will decrease due to combined reliability degradation and body effect. Similar mechanism applies to electron mobility degradation on both transistors. The drain current of $M1$ is thus more stable because of resilient biasing design scheme.

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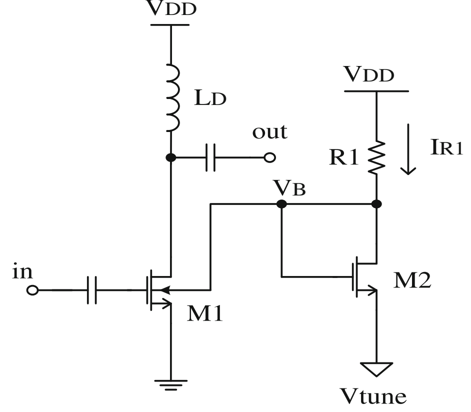


Fig. 8.1 Tunable adaptive body biasing (© IEEE)

8.1 Analytical Model and Equations

Again, using the approach laid out in Chap. 7, the V_T shift of $M1$ due to degradations of both $M1$ and $M2$ is given by

$$\delta V_T = \delta V_{T0} - \frac{\gamma \cdot \delta V_T'}{2\sqrt{2\phi_{\mathrm{FP}} - V_B}}\left(1 - \frac{1}{\sqrt{2\beta' R1(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V_T') + 1}}\right). \tag{8.1}$$

The mobility degradation results in a decrease in drain current also. The drain current of $M1$ is simplified as $I_D \approx \beta(V_{\mathrm{GS}} - V_T)^2/2$, where β variation due to mobility degradation is given by

$$\delta\beta = C_{\mathrm{ox}}\frac{W}{L}\delta\mu_n. \tag{8.2}$$

Clearly, β variation is linearly proportion to the electron mobility drift. The same relationship also applies to β'. The node voltage V_B fluctuation due to mobility degradation is simplified to $\delta V_B \approx \frac{\partial V_B}{\partial \beta'}\delta\beta'$. Using (8.2) $\frac{\partial V_B}{\partial \beta'}$ is derived below:

$$\begin{aligned}\frac{\partial V_B}{\partial \beta'} &= \frac{1}{(\beta' R1)^2}\left(\frac{2R1(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V_T')\beta' R1}{2\sqrt{2\beta' R1(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V_T') + 1}} - \sqrt{2\beta' R1(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V_T') + 1} \cdot R1\right)\\ &= \frac{\beta' R1^2(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V_T') - 2\beta' R1^2(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V_T') - R1'}{(\beta' R1)^2\sqrt{2\beta' R1(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V_T') + 1}}\\ &= \frac{-R1(\beta' R1(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V_T') + 1)}{(\beta' R1)^2\sqrt{2\beta' R1(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V_T') + 1}}.\end{aligned} \tag{8.3}$$

From the result in (8.3), one therefore finds δV_B as

$$\delta V_B = -\frac{R1(\beta' R1(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V'_T) + 1)}{(\beta' R1)^2 \sqrt{2\beta' R1(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V'_T) + 1}} \delta\beta'. \tag{8.4}$$

Assuming $\beta' R1(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V'_T) \gg 1$, (8.4) reduces to

$$\delta V_B \approx -\sqrt{\frac{V_{\mathrm{DD}} - V_{\mathrm{tune}} - V'_T}{2\beta'^3 R1}} \delta\beta'. \tag{8.5}$$

The threshold voltage variation in $M1$ due to body voltage fluctuation resulting from the mobility degradation in $M2$ is approximately as

$$\delta V_T \approx -\frac{\gamma \cdot \delta V_B}{2\sqrt{2\phi_{\mathrm{FP}} - V_B}}. \tag{8.6}$$

The drain current fluctuation subject to key transistor parametric drifts ($\delta\beta$ and δV_T) is given by

$$\delta I_D = \frac{\partial I_D}{\partial \beta}\delta\beta + \frac{\partial I_D}{\partial V_T}\delta V_T. \tag{8.7}$$

In the derivation of $\frac{\partial I_D}{\partial \beta}$ and $\frac{\partial I_D}{\partial V_T}$, a simple drain current equation $\left(I_D \approx \frac{\beta}{2}(V_{\mathrm{GS}} - V_T)^2\right)$ is used. The drain current variation is thus obtained as

$$\frac{\partial I_D}{\partial \beta} = \frac{1}{2}(V_{\mathrm{GS}} - V_T)^2. \tag{8.8}$$

$$\frac{\partial I_D}{\partial V_T} = -\beta(V_{\mathrm{GS}} - V_T) \tag{8.9}$$

Using (8.7), (8.8), and (8.9) one obtains

$$\delta I_D = \frac{1}{2}(V_{\mathrm{GS}} - V_T)^2\delta\beta - \beta(V_{\mathrm{GS}} - V_T)\delta V_T. \tag{8.10}$$

Combining (8.2), (8.8), and (8.10), the fluctuation of drain current of $M1$ is expressed below

$$\delta I_D = \frac{1}{2}(V_{\mathrm{GS}} - V_T)^2\delta\beta - \beta(V_{\mathrm{GS}} - V_T)\frac{\gamma\sqrt{\frac{V_{\mathrm{DD}} - V_{\mathrm{tune}} - V'_T}{2\beta'^3 R1}}\delta\beta'}{2\sqrt{2\phi_{\mathrm{FP}} - V_B}}. \tag{8.11}$$

Note that the variation $\delta\beta$ reflects the fluctuation resulting from the electron mobility degradation of $M1$. $\delta\beta'$represents the fluctuation caused by the electron mobility degradation of $M2$. The reduction of $M1$'s mobility will decrease the drain current in $M1$, while the reduction of $M2$'s mobility will increase the drain current in $M1$. To maximize the canceling effect, larger value of $R1$ as well as larger size of $M2$ are expected.

8.1.1 Tuning for Variability

The V_T shift of $M1$ due to V_tune change is described as follows. From (8.1) the body voltage values corresponding to the two different tuning voltages are determined by the equations in (8.12) and (8.13). Here, the $\mathrm{V_T}$ of $M2$ is supposed to be constant.

$$V_{B1} = V_{\mathrm{tune1}} + V_T' + \frac{\sqrt{2\beta R1(V_{\mathrm{DD}} - V_{\mathrm{tune1}} - V_T') + 1} - 1}{\beta R1} \tag{8.12}$$

$$V_{B2} = V_{\mathrm{tune2}} + V_T' + \frac{\sqrt{2\beta R1(V_{\mathrm{DD}} - V_{\mathrm{tune2}} - V_T') + 1} - 1}{\beta R1} \tag{8.13}$$

where V_{tune1} and V_{tune2} represent the two different tuning voltages.

The threshold voltage of $M1$ under the two different V_{tune} voltages can be written as:

$$V_{T1} = V_{T0} + \gamma_b\left(\sqrt{2\phi_F - V_{B1}} - \sqrt{2\phi_F}\right) \tag{8.14}$$

$$V_{T2} = V_{T0} + \gamma_b\left(\sqrt{2\phi_F - V_{B2}} - \sqrt{2\phi_F}\right). \tag{8.15}$$

The difference between two tuning voltage is marked as ΔV_T

$$\Delta V_T = V_{T2} - V_{T1}. \tag{8.16}$$

Combining (8.14) to (8.16), the sensitivity of V_T in $M1$ due to the tuning voltage of the circuit is derived as

$$\Delta V_T = \gamma_b\left(\sqrt{2\phi_F - V_{B2}} - \sqrt{2\phi_F - V_{B2}}\right). \tag{8.17}$$

A complete expression of (8.17) is complicated when substituting V_{B1} and V_{B2} with (8.12) and (8.13). Using (8.17) and the PTM 65 nm nMOSFET model parameters, the relationship between the threshold voltage and tuning voltage is calculated and plotted in Fig. 8.2.

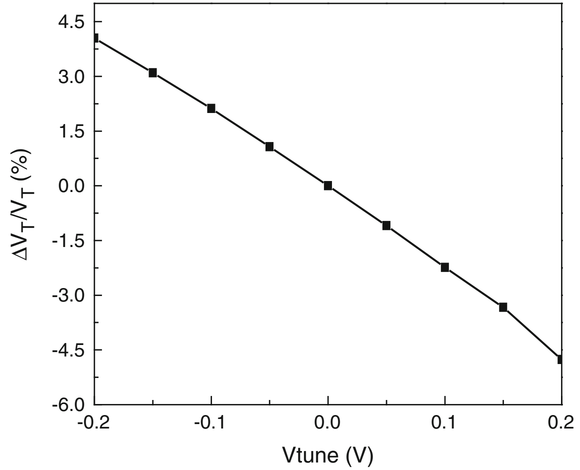


Fig. 8.2 Normalized ΔV_T versus V_{tune} (© IEEE)

The V_T of $M1$ decreases linearly from 4.05 to −4.76 % as Vtune increases from −0.2 to 0.2 V. This property can serve as post-fabrication calibration to compensate for the V_T deviation of $M1$ due to process variability.

Both the fabrication process-induced fluctuation and time-dependent degradation cause the MOSFET model parameter shifts. V_T is the most significant parameter for the MOSFET suffering from variability and reliability degradations. Static post-fabrication calibration and dynamic V_T adjustment are considered using the resilient biasing design. Figure 8.3 shows a 24 GHz class-AB PA topology. The resilient biasing is circled in this plot. The output matching network is tuned using ADS load-pull instrument to obtain the optimum value. The 65 nm NMOS transistors are modeled by the PTM equivalent BSIM4 model card. The transistor sizes, capacitor and inductor values, and supply voltage are given in this figure.

8.1.2 ADS Monte Carlo Simulation

The simulated P_{sat}, and η_{add} of the PA without resilient biasing are 10.28 dBm, 10.96 dBm, and 34.25 %, while the corresponding values of the resilient design shown reach 10.90 dBm, 11.22 dBm, and 34.59 %, respectively. The matching network remains the same between the two PA schematics. Figure 8.4 shows 20 overlapping samples of the output power and power-added efficiency variations due to process fluctuation [1]. It is observed from the Monte Carlo simulations that a 10 % of V_T spread (STD/Mean) will lead to 1.83 % P_{sat} spread and 1.05 % η_{add} spread. It is also seen from the simulation that the ±0.2 V and ±0.25 V V_{tune}

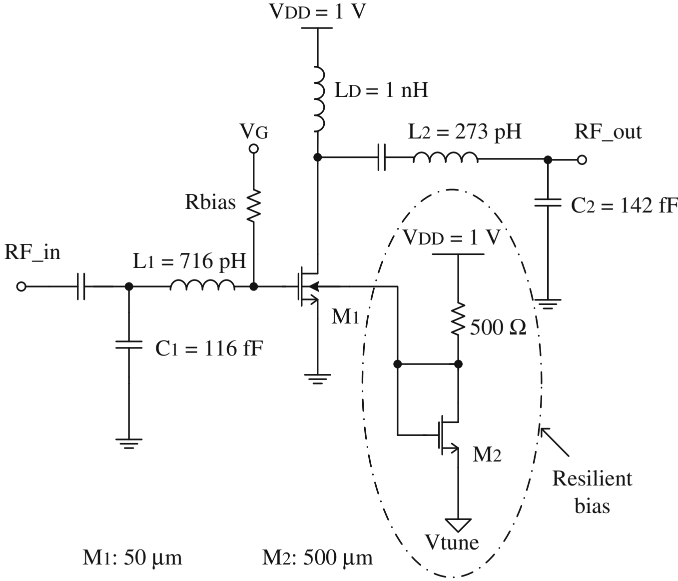


Fig. 8.3 Schematic of a 24 GHz class-AB power amplifier with resilient biasing (© IEEE)

correspond to the ±1.63 % and ±2.04 % P_{sat} deviation, respectively. So the spread fits into the compensation range of the ±0.25 V V_{tune} for post-process calibration.

The power amplifiers with and without resilient biasing technique are compared. Figure 8.5a shows normalized power-added efficiency to normalized threshold voltage variation. The resilient biasing reduces the sensitivity of normalized power-added efficiency significantly. For the normalized P_{sat} and P_{1dB} variations shown in Fig. 8.5b, the resilient biasing design reduces the sensitivity of P_{sat} and P_{1dB} against the threshold voltage shift dramatically, especially for the output power at the 1dB compression point (e.g., $\Delta P_{1dB}/P_{1dB}$ reduces from about −12 to −4 % at $\Delta V_T/V_T = 21$ %). So for reliability degradation induced dynamic V_T shift, the resilient biasing design helps improve the reliability of the PA by cutting the sensitivity by three to four times for the normalized output power at 1dB compression point and power-added efficiency.

The reliability degradation also reduces the electron mobility, which is another important parameter for drain current characteristic. Figure 8.6a shows normalized power-added efficiency versus normalized electron mobility reduction for PA with and without resilient biasing design. The resilient biasing scheme reduces the sensitivity of normalized power-added efficiency by 25 %. Figure 8.6b presents the normalized P_{sat} and P_{1dB} variations versus normalized mobility shift. The resilient design reduces the sensitivity of P_{sat} and P_{1dB} by 14.3 and 26.9 %, respectively. The resilient biasing design is obviously successful in reducing the power amplifier sensitivity against process variations and reliability degradations.

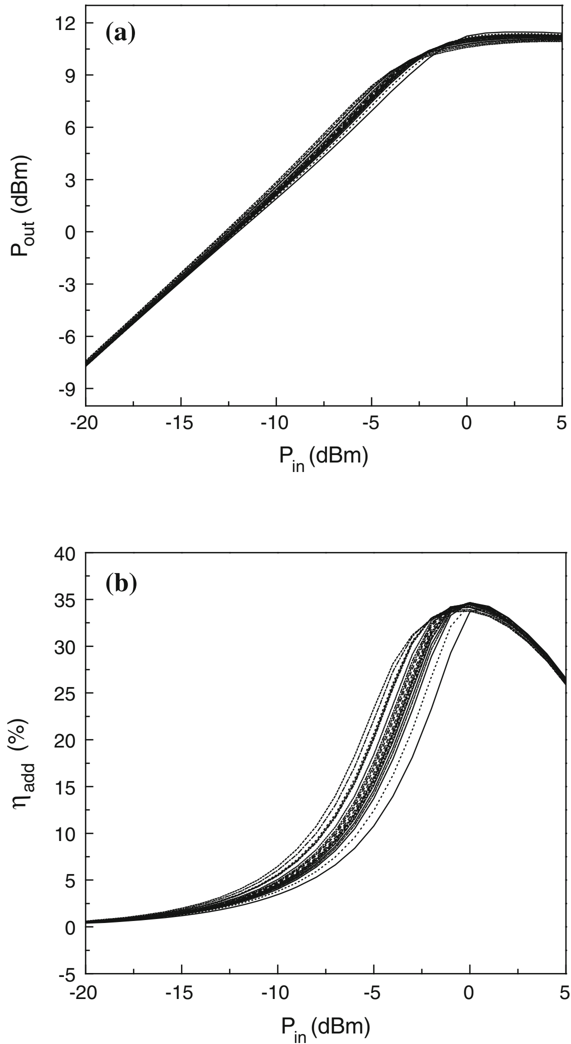


Fig. 8.4 PA performance fluctuation of **a** output power and **b** power-added efficiency versus input power (© IEEE)

8.2 Use of Current Source for Sensing Variability

An on-chip variability sensor using current source [2] is studied to detect process, supply voltage, and temperature (PVT) variations or even reliability degradation stemming from hot electron effect. The PVT variations yield a control signal from the designed current source. In Fig. 8.7, the current source circuit is made of n-channel transistors $M1$, $M2$, and $M3$. The transistor $M1$ and $M2$ have the same width and length and two times width of transistor $M3$. On the right branch in Fig. 8.1, a resistor R is used to set a control voltage V_{Ctrl}. The reference current I_{ref}

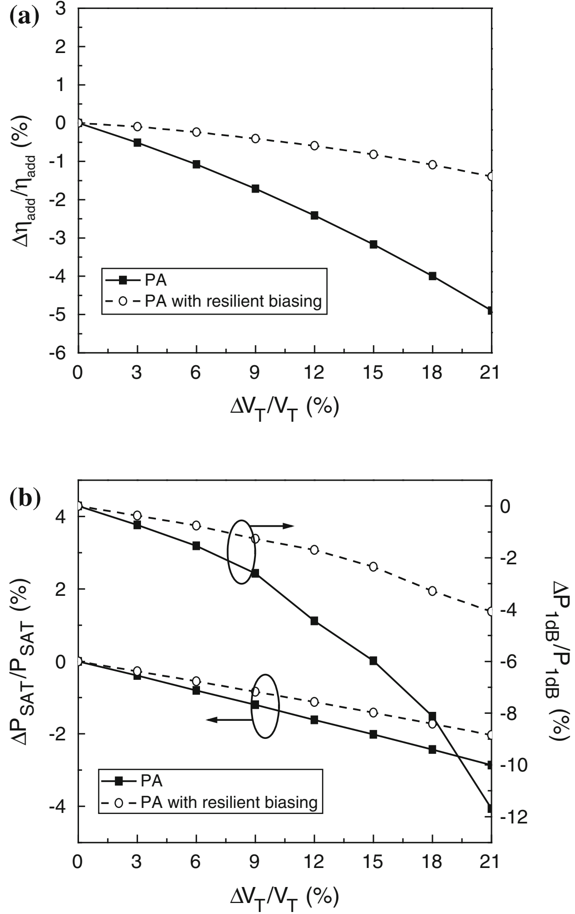


Fig. 8.5 Normalized **a** power-added efficiency variation and **b** P_{sat} and $P_{1\text{dB}}$ variation versus normalized threshold voltage shift (© IEEE)

is dependent on the PVT fluctuations. The Kirchhoff's current law to solve for V_{Ctrl} is given by

$$V_{\text{Ctrl}} = V_{\text{DD}} - I_{\text{ref}} R \tag{8.18}$$

and I_{ref} is the reference current and can be obtained as [3]

$$I_{\text{ref}} = \frac{(V_{\text{DD}} - V_{T1} - V_{T3})^2}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2} \tag{8.19}$$

where K_n is the transconductance factor ($K_n = \mu_n \varepsilon_{ox}/t_{ox}$). Subscript 1 and 3 represent the transistor $M1$ and $M3$, respectively.

Fig. 8.6 Normalized **a** power-added efficiency variation and **b** P_{sat} and P_{1dB} variation versus normalized mobility shift (© IEEE)

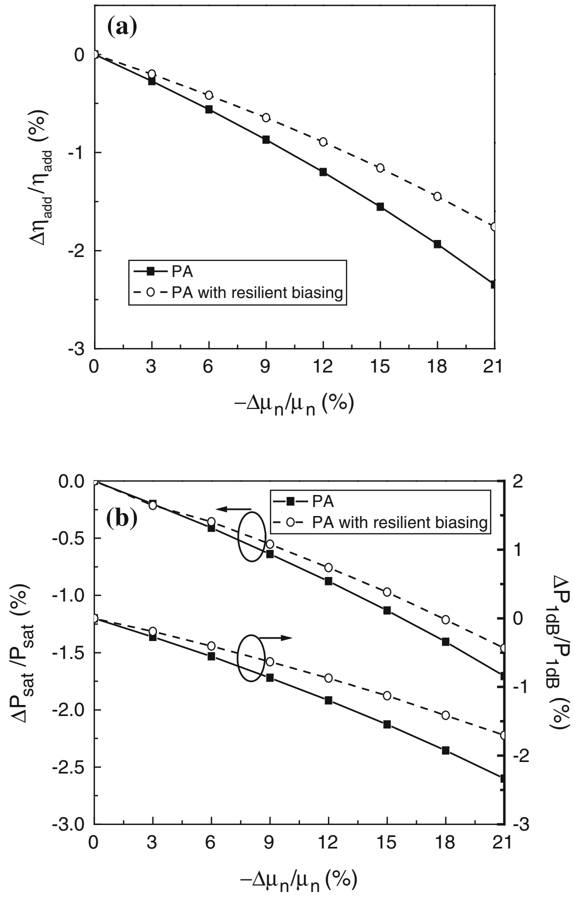
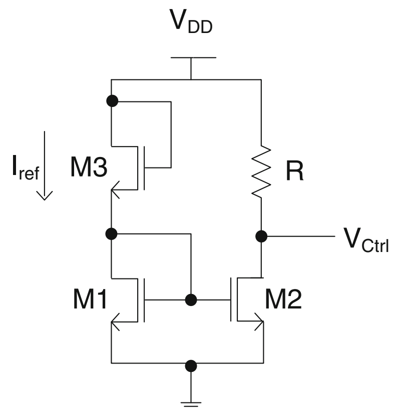


Fig. 8.7 Current source circuit schematic



The V_{Ctrl} shift because of supply voltage variation is derived using (8.18) and (8.19)

$$\frac{\partial V_{\mathrm{Ctrl}}}{\partial V_{\mathrm{DD}}} = 1 - \frac{2R(V_{\mathrm{DD}} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2} \tag{8.20}$$

The V_{Ctrl} shift due to mobility fluctuation is given by

$$\frac{\partial V_{\mathrm{Ctrl}}}{\partial \mu_n} = -\frac{\varepsilon_{\mathrm{ox}} R}{t_{\mathrm{ox}}} \frac{(V_{\mathrm{DD}} - V_{T1} - V_{T3})^2}{\left(\sqrt{\frac{2L_1}{W_1}} + \sqrt{\frac{2L_3}{W_3}}\right)^2} \tag{8.21}$$

Furthermore, the V_{Ctrl} shift resulting from fluctuation of the threshold voltage from $M1$ or $M3$ is

$$\frac{\partial V_{\mathrm{Ctrl}}}{\partial V_{T1,3}} = \frac{2R(V_{\mathrm{DD}} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2}. \tag{8.22}$$

Combing (8.20)–(8.22) yields the overall V_{Ctrl} variation as follows:

$$\begin{aligned}\Delta V_{\mathrm{Ctrl}} = &\left[1 - \frac{2R(V_{\mathrm{DD}} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2}\right] \Delta V_{\mathrm{DD}} - \left[\frac{\varepsilon_{\mathrm{ox}} R}{t_{\mathrm{ox}}} \frac{(V_{\mathrm{DD}} - V_{T1} - V_{T3})^2}{\left(\sqrt{\frac{2L_1}{W_1}} + \sqrt{\frac{2L_3}{W_3}}\right)^2}\right] \Delta \mu_n \\ &+ \left[\frac{2R(V_{\mathrm{DD}} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2}\right] \Delta V_{T1} + \left[\frac{2R(V_{\mathrm{DD}} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2}\right] \Delta V_{T3}\end{aligned} \tag{8.23}$$

8.3 Tuning for Variability

The sensitivity of the class AB PA is evaluated using Fig. 8.8. The PVT variations change behaviors of the PA and also degrade the performance. In the simulation, the PVT variations are given to the PA circuit. Adaptive body biasing is used to find a range of body biasing voltage (V_{ABB}) to compensate each variation.

V_{Ctrl} signal is efficiently transformed to an optimal body bias signal for power amplifier application. From a range of V_{ABB}, an operational amplifier is used as a voltage shifter and amplifier to adjust the V_{Ctrl} to meet a required V_{ABB}. Choosing appropriate size of resistor R_1 and R_2 using (8.31) provides a matched V_{ABB} for PA.

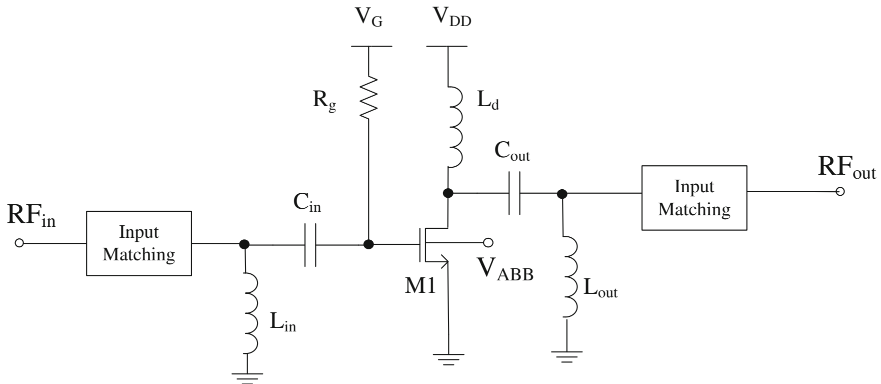


Fig. 8.8 A class AB PA with adaptive body biasing (© Elsevier)

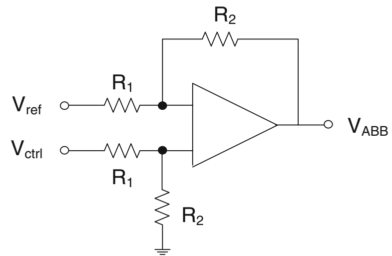


Fig. 8.9 Level shifting circuit

For example, for a reference voltage (V_{ref}) of 0.4 V, R_1 and R_2 can be designed at 500 Ω and 1500 Ω, respectively. (See Fig. 8.9)

$$V_{\text{ABB}} = \frac{R_2}{R_1}(V_{\text{Ctrl}} - V_{\text{ref}}) \tag{8.24}$$

Due to the body effect, the threshold voltage of the power amplifier transistor is described by the following expression

$$V_T = V_{T0} + \gamma_b\left(\sqrt{2\phi_F - V_{\text{ABB}}} - \sqrt{2\phi_F}\right) \tag{8.25}$$

The threshold voltage shift of the PA transistor is modeled by the fluctuation of V_{T0} and V_{ABB} as

$$\Delta V_T = \frac{\partial V_T}{\partial V_{T0}}\Delta V_{To} + \frac{\partial V_T}{\partial V_{\text{ABB}}}\Delta V_{\text{ABB}} = \Delta V_{T0} - \frac{\gamma}{2\sqrt{2\phi_F - V_{\text{ABB}}}}\Delta V_{\text{ABB}} \tag{8.26}$$

From (8.24), the V_{ABB} shift is given by

$$\Delta V_{\mathrm{ABB}} = \frac{\partial V_{\mathrm{ABB}}}{\partial V_{\mathrm{Ctrl}}} \Delta V_{\mathrm{Ctrl}} = \frac{R_2}{R_1} \Delta V_{\mathrm{Ctrl}} \tag{8.27}$$

Thus, the threshold voltage shift of the power amplifier input transistor due to PVT variations are summed as

$$\begin{aligned} \Delta V_T = {} & \Delta V_{T0} - \frac{\gamma_b R_2}{2R_1\sqrt{2\phi_F - V_{\mathrm{ABB}}}} \\ & \left\{ \left[1 - \frac{2R(V_{\mathrm{DD}} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2} \right] \Delta V_{\mathrm{DD}} - \left[\frac{\varepsilon_{\mathrm{ox}} R}{t_{\mathrm{ox}}} \frac{(V_{\mathrm{DD}} - V_{T1} - V_{T3})^2}{\left(\sqrt{\frac{2L_1}{W_1}} + \sqrt{\frac{2L_3}{W_3}}\right)^2} \right] \Delta \mu_n \right. \\ & \left. + \left[\frac{2R(V_{\mathrm{DD}} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2} \right] \Delta V_{T1} + \left[\frac{2R(V_{\mathrm{DD}} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2} \right] \Delta V_{T3} \right\} \end{aligned} \tag{8.28}$$

The drain current fluctuation subjects to key transistor parametric drifts $\Delta\mu_n$, ΔV_{GS} and ΔV_T can be modeled as

$$\Delta I_D = \frac{\partial I_D}{\partial \mu_n} \Delta \mu_n + \frac{\partial I_D}{\partial V_{\mathrm{GS}}} \Delta V_{\mathrm{GS}} + \frac{\partial I_D}{\partial V_T} \Delta V_T \tag{8.29}$$

Assume the $\mathrm{V_{GS}}$ shift is proportional to the fluctuation of V_{DD}.

$$\Delta V_{\mathrm{GS}} = \alpha \Delta V_{\mathrm{DD}} \tag{8.30}$$

where α is a fitting parameter.

Using (8.26)–(8.30) the fluctuation of drain current normalized to its fresh current is expressed as follows:

$$\begin{aligned} \frac{\Delta I_D}{I_D} = {} & \frac{\Delta \mu_n}{\mu_n} + \frac{2\alpha_{\mathrm{DD}}}{V_{\mathrm{GS}} - V_T} - \frac{2}{V_{\mathrm{GS}} - V_T} \left(\Delta V_{T0} - \frac{\gamma_b R_2}{2R_1\sqrt{2\varphi_F - V_{\mathrm{ABB}}}} \right. \\ & \left\{ \left[1 - \frac{2R(V_{\mathrm{DD}} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2} \right]_{\mathrm{DD}} - \left[\frac{\varepsilon_{\mathrm{ox}}}{t_{\mathrm{ox}}} \frac{2R(V_{\mathrm{DD}} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{W_1}} + \sqrt{\frac{2L_3}{W_3}}\right)^2} \right] \Delta \mu_n \right. \\ & \left.\left. + \left[\frac{2R(V_{\mathrm{DD}} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2} \right] \Delta V_{T1} + \left[\frac{2R(V_{\mathrm{DD}} - V_{T1} - V_{T3})}{\left(\sqrt{\frac{2L_1}{K_n W_1}} + \sqrt{\frac{2L_3}{K_n W_3}}\right)^2} \right]_{T3} \right\} \right) \end{aligned} \tag{8.31}$$

In the above equation, the terms beyond ΔV_{T0} represent the V_{DD}, mobility, and threshold voltage compensation effects. The normalized output power degradation is related to the normalized drain current degradation as follows [4]:

$$\frac{\Delta P_o}{P_o} \approx \frac{\Delta I_D}{I_D} \tag{8.32}$$

8.3.1 Circuit Simulation Results

The power amplifier with the current source compensation technique is compared with the PA without compensation using ADS simulation. For the process variation effect, the output power is evaluated against threshold voltage and mobility variations as shown in Figs. 8.10 and 8.11. It is clear from Figs. 8.10 and 8.11 that the power amplifier with adaptive body bias is more robust against threshold voltage variation (see Fig. 8.10) and mobility fluctuation (Fig. 8.11).

For the process variation effect, the output power of the PA has also been evaluated using different process corner models due to inter-die variations. The simulation result of the fast–fast, slow–slow, and nominal–nominal models is shown in Fig. 8.12. Clearly, the PA using the adaptive body bias compensation exhibits better stability against process variation effect.

Figures 8.13 and 8.14 show the output power of the power amplifier versus temperature variation and supply voltage change, respectively. As seen in Figs. 8.13 and 8.14 the output power of the PA using the adaptive body bias compensation technique demonstrates less sensitivity over temperature and V_{DD} variations.

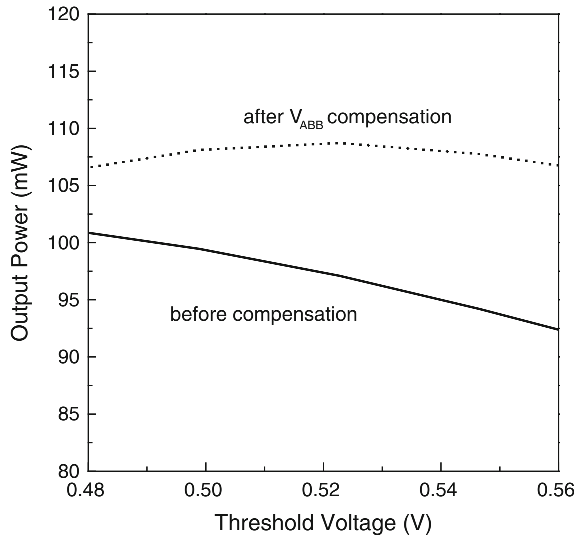


Fig. 8.10 Output power versus threshold voltage shift (© Elsevier)

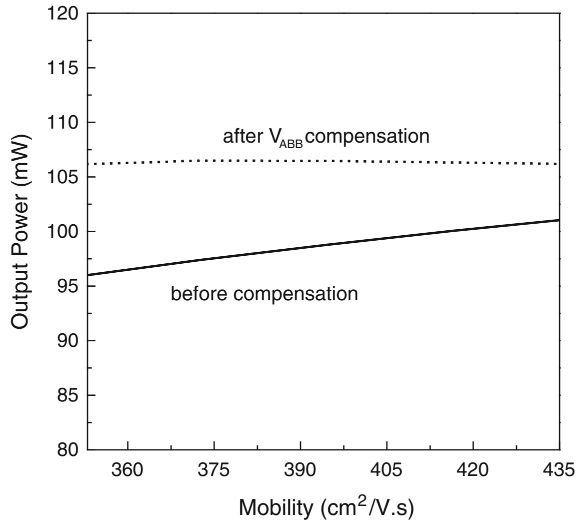


Fig. 8.11 Output power versus mobility variation (© Elsevier)

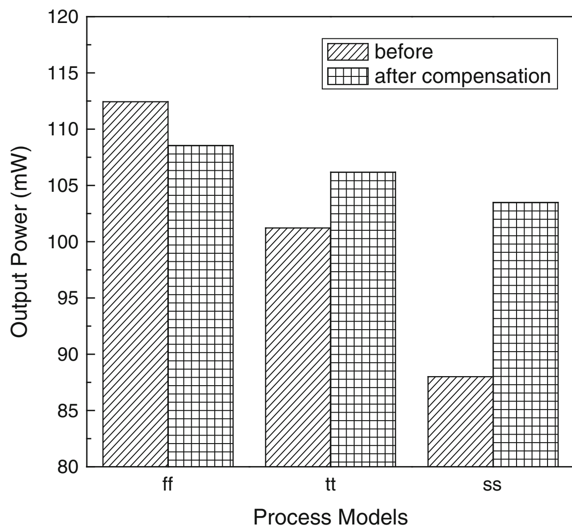


Fig. 8.12 Output power versus process corner models (© Elsevier)

In addition, the power-added efficiency of the power amplifier with or without adaptive body bias compensation is examined against semiconductor process variations effects. Figures 8.15 and 8.16 display the improvement of power-added efficiency of the PA with ABB compensation over that without adaptive body bias for the threshold voltage shift (see Fig. 8.15) and mobility variation (see Fig. 8.16).

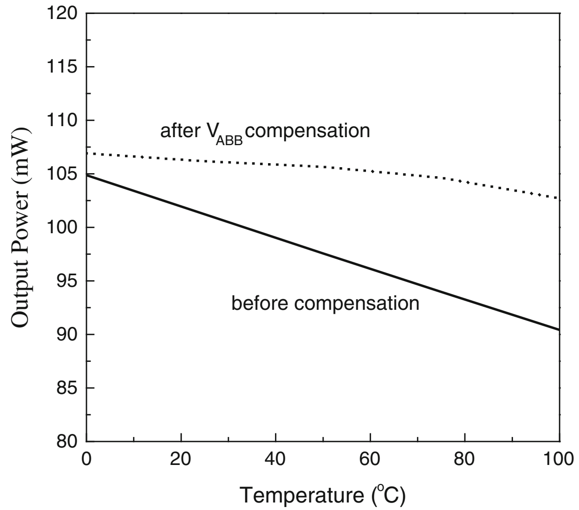


Fig. 8.13 Output power versus temperature (© Elsevier)

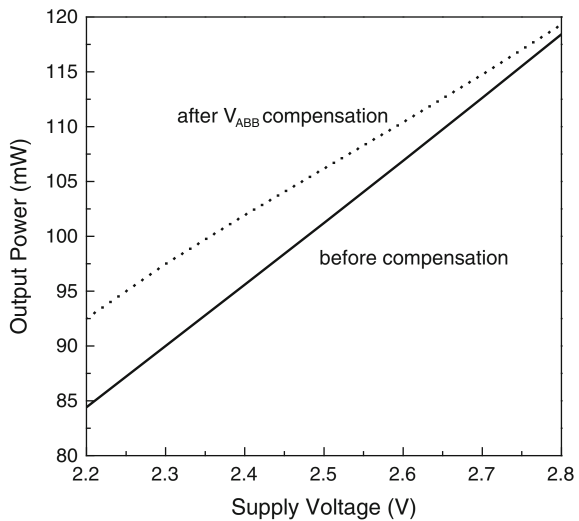


Fig. 8.14 Output power versus supply voltage (© Elsevier)

For the process corner models the power-added efficiency of the PA with ABB compensation shows less process sensitivity, as evidenced by the plot in Fig. 8.17.

Then, the power-added efficiency is compared against temperature and supply voltage variations. The power-added efficiency is getting better for the PA with ABB compensation as shown in Figs. 8.18 and 8.19.

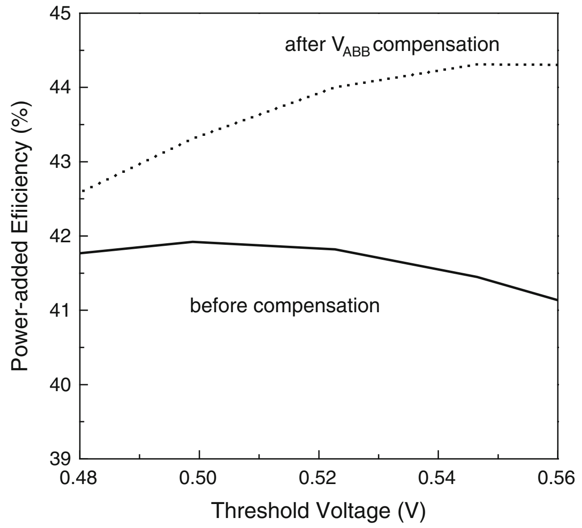


Fig. 8.15 Power-added efficiency as a function of threshold voltage (© Elsevier)

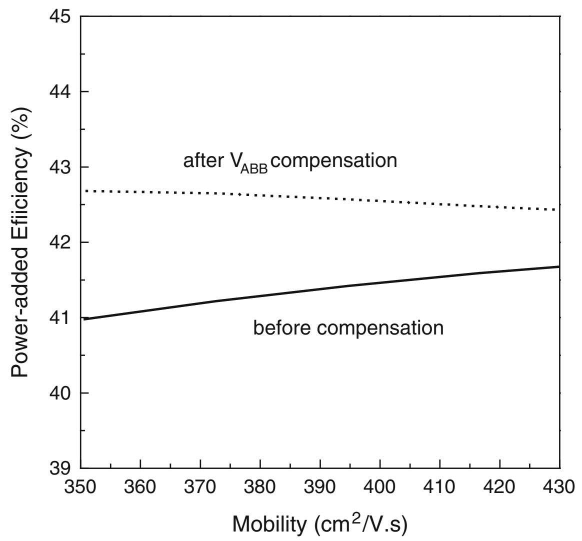


Fig. 8.16 Power-added efficiency as a function of mobility (© Elsevier)

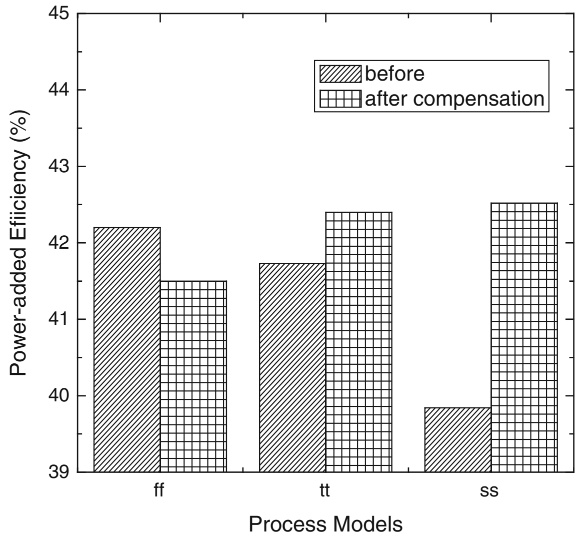


Fig. 8.17 Power-added efficiency versus process corner models (© Elsevier)

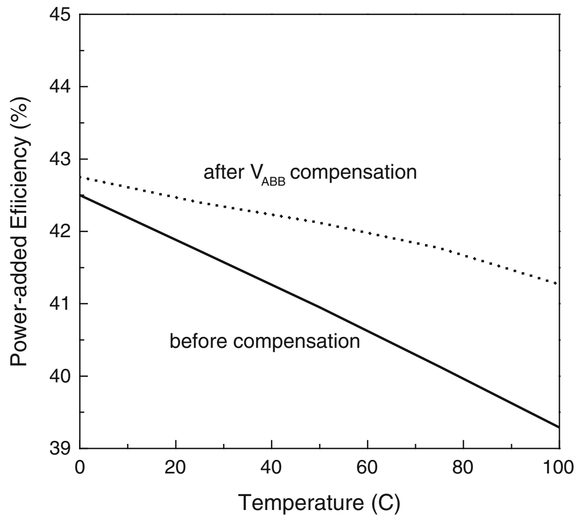


Fig. 8.18 Power-added efficiency versus temperature (© Elsevier)

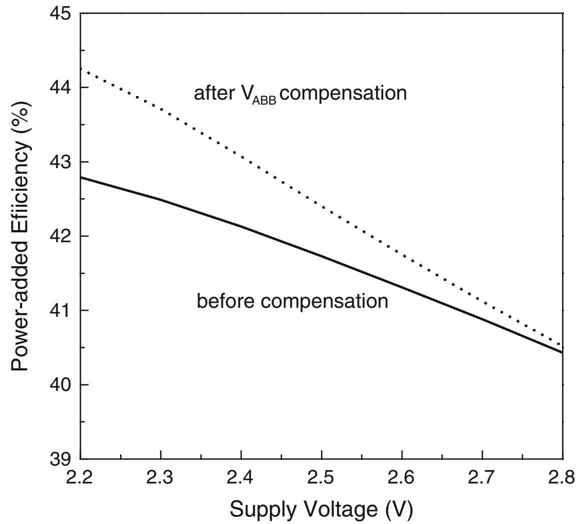


Fig. 8.19 Power-added efficiency versus supply voltage (© Elsevier)

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