Chapter 7
LNA Design for Variability

Nanoscale CMOS transistors are more susceptible to long-term electrical stress-induced reliability degradations. When those devices are used for radio frequency (RF) or microwave applications, a single transistor aging can lead to significant circuit performance degradation resulting from threshold voltage V_T shift and electron mobility μ_n drift. In addition, process variations in nanoscale transistors are another major concern in today's circuit design. Random dopant fluctuation, oxide thickness variation, and line edge roughness result in significant threshold voltage variation of CMOS transistors at sub-20 nm technology node and beyond [1].

The design for reliability (DFR) method intends to reduce the circuit over-design, while increasing its robustness against long-term aging. Here, the adaptive substrate (or body) bias scheme is described for the LNA design for process variability and circuit reliability [2]. Figure 7.1 shows a simple adaptive body bias scheme. The adaptive body bias technique dynamically adjusts the substrate bias of the input transistor $M1$ to reduce impact of process variations and device aging on circuit performance.

7.1 Analytical Model and Equations

As seen in Fig. 7.1, the right side of the circuit controls the substrate voltage of the main transistor. By designing similar drain-source voltage and gate-source voltage for $M1$ and $M2$, both the main transistor and bias transistor may subject to similar aging effect such as threshold voltage shift and electron mobility degradation.

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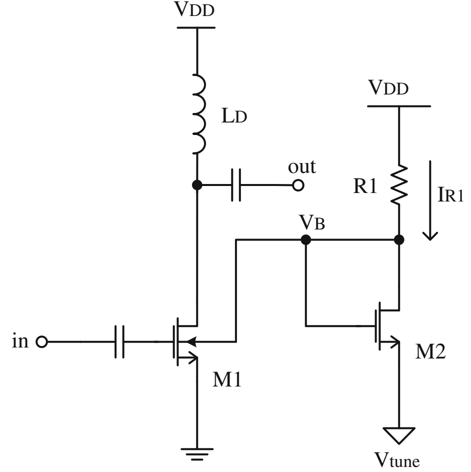

Fig. 7.1 Adaptive body bias design (© IEEE)

To account for possible different stress conditions between $M1$ and $M2$, mismatch between the main transistor aging and bias transistor aging is also considered. In Fig. 7.1, when the V_T of $M2$ increases, the current I_{R1} decreases. The reduced I_{R1} results in an increased body voltage V_B. The increase in V_B of $M1$ will decrease the threshold voltage of the input transistor due to source-body effect. Thus, this compensates the change of V_T from device aging. Similarly, the decrease in electron mobility, which decreases the drain current of the MOS transistor, will increase V_B of $M1$. The drain current of $M1$ is also compensated. Examining Fig. 7.1, the KCL equation to solve for V_B is given as

$$I_{\mathrm{R1}}R1 + V_B = V_{\mathrm{DD}} \tag{7.1}$$

$$I_{R1} \approx \frac{\beta'}{2}\left(V_B - V_{\mathrm{tune}} - V_T'\right)^2 \tag{7.2}$$

where V_{tune} is the tuning voltage, β' is the transistor parameter ($\beta' = \mu_n C_{\mathrm{ox}} W/L$) of $M2$, and V_T' is the threshold voltage of $M2$. Note that V_{tune} can be used to adjust the stress effect on $M2$ due to change of effective drain-source and gate-source voltages. Combining (7.1) and (7.2) and solving for V_B one obtains

$$V_B = V_{\mathrm{tune}} + V_T' + \frac{\sqrt{2\beta' R1(V_{\mathrm{DD}} - V_{\mathrm{tune}} - V_T') + 1} - 1}{\beta' R1}. \tag{7.3}$$

Using (7.3) the $\delta V_T'$ variation yields the body voltage fluctuation as follows:

$$\begin{aligned}\delta V_B &\approx \frac{\partial V_B}{\partial V_T'}\delta V_T' \\ &= (1+\frac{-2\beta' R1}{2\beta' R1\sqrt{2\beta' R1(V_{\mathrm{DD}}-V_{\mathrm{tune}}-V_T')+1}})\delta V_T' \\ &= \delta V_T' - \frac{\delta V_T'}{\sqrt{2\beta' R1(V_{\mathrm{DD}}-V_{\mathrm{tune}}-V_T')+1}}\end{aligned} \tag{7.4}$$

Due to the body effect, the V_T of $M1$ can be described by the following expression

$$V_T = V_{T0} + \gamma_b(\sqrt{2\phi_F - V_B} - \sqrt{2\phi_F}) \tag{7.5}$$

where γ_b is the body effect factor and ϕ_F represents the Fermi potential. The V_T shift of $M1$ due to degradation of $M1$ and $M2$ is thus modeled by the fluctuation of V_{T0} and V_B as

$$\delta V_T = \delta V_{T0} - \frac{\gamma_b \delta V_B}{2\sqrt{2\phi_{\mathrm{FP}} - V_B}}. \tag{7.6}$$

Combining (7.4) and (7.6) yields the V_T variation

$$\delta V_T = \delta V_{T0} - \frac{\gamma_b \delta V_T'}{2\sqrt{2\phi_{\mathrm{FP}} - V_B}}(1-\frac{1}{\sqrt{2\beta' R1(V_{\mathrm{DD}}-V_{\mathrm{tune}}-V_T')+1}}). \tag{7.7}$$

The first term in (7.7) represents the threshold voltage shift of $M1$, while the second term in (7.7) accomplishes the canceling effect resulting from the combination of threshold voltage shift of $M2$ and the body bias circuit of $M1$. Thus, the overall V_T shift of $M1$ due to process variation and reliability degradation is reduced. The level of reduction is related to $\delta V_T'$ of $M2$, body effect coefficient γ_b, $M2$ transistor β', and resistor $R1$. To achieve an optimal resilience to the variability and reliability, it is better to choose larger $R1$ and wider channel width of $M2$.

The noise factor is a measure of the degradation in signal-to-noise ratio that a system introduces. Equation (7.8) expresses the noise factor defined in the two-port network with noise sources and a noiseless circuit [3]. The noise figure is the noise factor expressed in decibels. The noise factor is written as

$$F = \frac{\overline{i_s^2} + \overline{|i_n + (Y_c + Y_s)e_n|^2}}{\overline{i_s^2}} = 1 + \frac{\overline{i_n^2} + |Y_c + Y_s|^2\overline{e_n^2}}{\overline{i_s^2}} \tag{7.8}$$

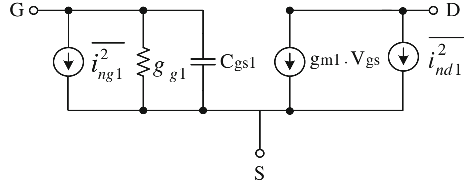

Fig. 7.2 nMOSFET noise model

where i_s is the noise current from the source, Y_s is the source admittance, i_n is the device noise current, e_n is the device noise voltage, and Y_c is the correlation admittance.

For n-channel MOS transistor $M1$ at high frequency, the small-signal equivalent circuit model with noise currents is displayed in Fig. 7.2. The $1/f$ flicker noise is ignored at high frequency. The nMOSFET consists of the drain current noise and gate noise. The drain current noise and gate noise in Fig. 2 can be written as [4, 5]

$$\overline{i_{\text{nd1}}^2} = 4kT\gamma_1 g_{d01}\Delta f \tag{7.9}$$

$$\overline{i_{\text{ng1}}^2} = 4kT\theta \frac{\omega^2 C_{\text{gs1}}^2}{5g_{d01}}\Delta f \tag{7.10}$$

where k is the Boltzmanns' constant, T is the absolute temperature, ω is the radian frequency, g_{d01} is the output conductance of $M1$, C_{gs1} is the gate-source capacitance of $M1$, γ_1 = 2/3 for long channel MOSFET and can be 2–3 times larger in short-channel devices, and θ is the gate noise coefficient.

For the DFR biasing circuit, the drain of nMOSFET M2 is shorted to its gate as seen in Fig. 7.3. Thus, the noise looking into the node B consists of the two noise sources $R1$ and $M2$ drain current noise. The resistor $R1$ thermal noise and $M2$ drain current noise are modeled as:

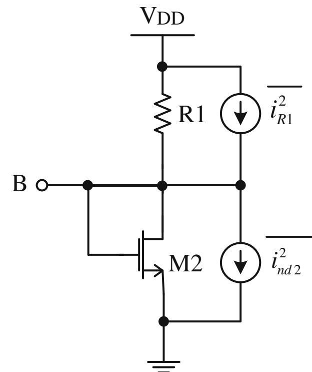

Fig. 7.3 DFR biasing circuit noise model (© IEEE)

$$\overline{i_{R1}^2} = 4kT\frac{1}{R1}\Delta f \tag{7.11}$$

$$\overline{i_{\mathrm{nd2}}^2} = 4kT\gamma_2 g_{d02}\Delta f \tag{7.12}$$

where g_{d02} is the output conductance of $M2$. Thus, the total mean squared noise voltage is

$$\overline{e_{B1}^2} = 4kT\frac{R1}{1+R1\gamma_2 g_{d02}}\Delta f. \tag{7.13}$$

The reflected drain current noise due to noise voltage in the body node is determined by a ratio of body transconductance g_{mb1}.

$$\overline{i_{nB1}^2} = 4kT\frac{R1}{1+R1\gamma_2 g_{d02}}g_{\mathrm{mb1}}^2\Delta f. \tag{7.14}$$

Due to the body effect of $M1$, the drain current noise is a combination of noise originated from the drain current and reflected from the body node B.

$$\overline{i_{n1}^2} = \overline{i_{\mathrm{nB1}}^2} + \overline{i_{\mathrm{nd1}}^2} = 4kT\left[\frac{R1}{1+R1\gamma_2 g_{d02}}g_{\mathrm{mb1}}^2 + \gamma_1 g_{d01}\right]\Delta f \tag{7.15}$$

The noise can be reflected back to the input gate of $M1$ by g_{m1}.

$$\overline{e_{n1}^2} = \frac{\overline{i_{n1}^2}}{g_{m1}^2} = 4kT\left[\frac{R1}{1+R1\gamma_2 g_{d02}}\frac{g_{\mathrm{mb1}}^2}{g_{m1}^2} + \frac{\gamma_1 g_{d01}}{g_{m1}^2}\right]\Delta f \tag{7.16}$$

The equivalent input noise voltage is completely correlated with the drain current noise. Thus, the noise resistance is

$$R_{n1} = \frac{\overline{e_{n1}^2}}{4kT\Delta f} = \frac{R1}{1+R1\gamma_2 g_{d02}}\frac{g_{\mathrm{mb1}}^2}{g_{m1}^2} + \frac{\gamma_1 g_{d01}}{g_{m1}^2} \tag{7.17}$$

The equivalent input noise voltage generator by itself does not fully account for the drain current noise. A noisy drain current also flows when the input is open circuited. Under this condition, the equivalent input voltage is obtained from dividing the drain current noise by the transconductance. When multiplying the input admittance, $\overline{e_{n1}^2}$ gives an equivalent input current noise as

$$\overline{i_{n1'}^2} = \overline{e_{n1}^2}(j\omega C_{\mathrm{gs1}})^2 \tag{7.18}$$

Here, it is assumed that the input admittance of $M1$ is purely capacitive, which is good approximation when the operating frequency is below the cutoff frequency.

The drain noise and gate noise of $M1$ are correlated with a correlation coefficient c_1 defined as

$$c_1 = \frac{\overline{i_{\mathrm{ng1}} \cdot i_{n1}^*}}{\sqrt{\overline{i_{\mathrm{ng1}}^2} \cdot \overline{i_{n1}^2}}} \tag{7.19}$$

The total equivalent input current noise consists of the reflected drain noise and the induced gate current noise. The induced gate noise current itself has two parts. One part, i_{ngc1}, is fully correlated with the drain current noise of $M1$, while the other, i_{ngu1}, is uncorrelated with the drain current noise. The correlation admittance is expressed as follows:

$$\begin{aligned} Y_c &= \frac{i_{n1'} + i_{\mathrm{ngc1}}}{e_{n1}} = j\omega C_{\mathrm{gs1}} + \frac{i_{\mathrm{ngc1}}}{e_{n1}} \\ &= j\omega C_{\mathrm{gs1}} + g_{m1}\frac{i_{\mathrm{ngc1}}}{i_{n1}} \end{aligned} \tag{7.20}$$

The last term must be manipulated in terms of cross-correlations by multiplying both numerator and denominator by the conjugate of the drain current noise:

$$g_{m1}\frac{i_{\mathrm{ngc1}}}{i_{n1}} = g_{m1}\frac{\overline{i_{\mathrm{ngc1}} \cdot i_{n1}^*}}{\overline{i_{n1} \cdot i_{n1}^*}} = g_{m1}\frac{\overline{i_{\mathrm{ng1}} \cdot i_{n1}^*}}{\overline{i_{n1}^2}} \tag{7.21}$$

Using the above equation, the correlation admittance can be rewritten as

$$\begin{aligned} Y_c &= j\omega C_{\mathrm{gs1}} + g_{m1}\frac{\overline{i_{\mathrm{ng1}} \cdot i_{n1}^*}}{\overline{i_{n1}^2}} \\ &= j\omega C_{\mathrm{gs1}} + g_{m1}\frac{\overline{i_{\mathrm{ng1}} \cdot i_{n1}^*}}{\sqrt{\overline{i_{\mathrm{ng1}}^2}}\sqrt{\overline{i_{n1}^2}}}\sqrt{\frac{\overline{i_{\mathrm{ng1}}^2}}{\overline{i_{n1}^2}}} = j\omega C_{\mathrm{gs1}} + g_{m1}c_1\sqrt{\frac{\overline{i_{\mathrm{ng1}}^2}}{\overline{i_{n1}^2}}} \end{aligned} \tag{7.22}$$

Inserting (7.10) and (7.15) into (7.22) yields the expression for Y_c. Note that the correlation coefficient c_1 is purely imaginary [3]. Thus, G_c (the real part of Y_c) equals zero. Using the definition of the correlation coefficient, the expression of the gate induced noise is written as

$$\overline{i_{\mathrm{ng1}}^2} = \overline{(i_{\mathrm{ngc1}} + i_{\mathrm{ngu1}})^2} = 4kT\Delta f\left(\frac{\theta\omega^2 C_{\mathrm{gs1}}^2 |c_1|^2}{5g_{d01}} + \frac{\theta\omega^2 C_{\mathrm{gs1}}^2 (1-|c_1|^2)}{5g_{d01}}\right). \tag{7.23}$$

Thus, the uncorrelated portion of the gate noise is

$$G_{u1} = \frac{\overline{i_{u1}^2}}{4kT\Delta f} = \frac{\theta\omega^2 C_{gs1}^2 (1 - |c_1|^2)}{5 g_{d01}}. \tag{7.24}$$

The minimum noise figure is given by

$$\begin{aligned} F_{\min} &= 1 + 2R_{n1}\left[G_{opt} + G_c\right] \approx 1 + 2R_{n1}\sqrt{\frac{G_{u1}}{R_{n1}}} \\ &= 1 + \frac{2}{\sqrt{5}}\frac{\omega C_{gs1}}{g_{m1}}\sqrt{\theta(1 - |c|^2)\left[\frac{R1 g_{mb1}^2}{(1 + R1\gamma_2 g_{d02}) g_{d01}} + \gamma_1\right]} \end{aligned} \tag{7.25}$$

Using (7.25) the minimum noise figure fluctuation is derived as

$$\begin{aligned} \Delta F_{\min} = &-\frac{2}{\sqrt{5}}\frac{\omega C_{gs1}}{g_{m1}^2}\sqrt{\theta(1 - |c|^2)\left[\frac{R1 g_{mb1}^2}{(1 + R1\gamma_2 g_{d02}) g_{d01}} + \gamma_1\right]}\Delta g_{m1} \\ &+ \frac{2}{\sqrt{5}}\frac{\omega C_{gs1}}{g_{m1}}\frac{\theta(1 - |c|^2) R1 g_{mb1}}{(1 + R1\gamma_2 g_{d02}) g_{d01}\sqrt{\theta(1 - |c|^2)\left[\frac{R1 g_{mb1}^2}{(1 + R1\gamma_2 g_{d02}) g_{d01}} + \gamma_1\right]}}\Delta g_{mb1} \\ &- \frac{1}{\sqrt{5}}\frac{\omega C_{gs1}}{g_{m1}}\frac{\theta(1 - |c|^2) R1 g_{mb1}^2}{(1 + R1\gamma_2 g_{d02}) g_{d01}^2\sqrt{\theta(1 - |c|^2)\left[\frac{R1 g_{mb1}^2}{(1 + R1\gamma_2 g_{d02}) g_{d01}} + \gamma_1\right]}}\Delta g_{d01} \\ &- \frac{1}{\sqrt{5}}\frac{\omega C_{gs1}}{g_{m1}}\frac{\theta(1 - |c|^2) R1^2 g_{mb1}^2 \gamma_2}{(1 + R1\gamma_2 g_{d02})^2 g_{d01}\sqrt{\theta(1 - |c|^2)\left[\frac{R1 g_{mb1}^2}{(1 + R1\gamma_2 g_{d02}) g_{d01}} + \gamma_1\right]}}\Delta g_{d02} \end{aligned} \tag{7.26}$$

In (7.26), the second term leads to the reduction of minimum noise figure sensitivity due to the body effect of MOSFET M1.

Small-signal gain S_{21} is related to the transconductance and gate-drain capacitance of $M1$. A detailed derivation of small-signal model is given in the following.

$$S_{21} = \frac{-2Y_{21}\sqrt{Z_{01}Z_{02}}}{\Delta_1} \tag{7.27}$$

$$\Delta_1 = (1 + Y_{11}Z_{01})(1 + Y_{22}Z_{02}) - Y_{21}Z_{01}Y_{12}Z_{02} \tag{7.28}$$

In the following discussion, one will see how Y_{21} fluctuates due to transconductance variation. Firstly, high frequency small-signal model for nMOSFET is shown in Fig. 7.4a. When the node D is tied to the ground terminal S, Fig. 7.4a reduces to Fig. 7.4b.

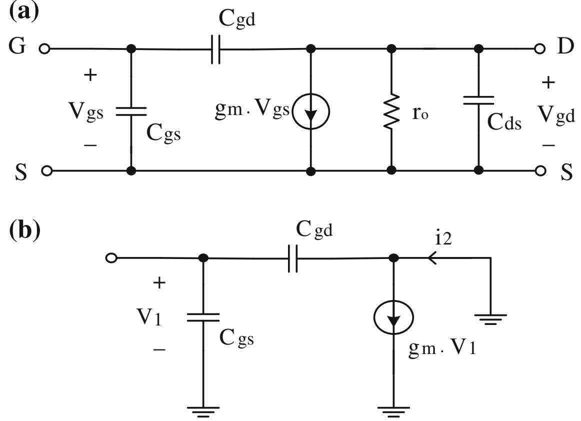

Fig. 7.4 **a** High frequency small-signal model of nMOSFET; **b** simplified equivalent circuit for Y_{21} derivation

Y_{21} for single nMOSFET without body effect is derived from Fig. 7.4b. In Fig. 7.4, V_1 refers to V_{gs} in terminal 1 (between G and S) and V_2 refers to V_{gd} in terminal 2 (between D and S). Using Fig. 7.4b Y_{21} without body biasing is given by

$$Y_{21}(f) = \frac{i_2(f)}{V_1(f)}|_{V_2=0} = -j\omega C_{gd} + g_m \tag{7.29}$$

Thus, the transconductance fluctuation results in Y_{21} variation:

$$\Delta Y_{21}(f) = \Delta g_m \tag{7.30}$$

Figure 7.5a shows small-signal model for nMOSFET with body bias terminal. When D of $M1$ is tied to ground with S of both $M1$ and $M2$ in the substrate biasing circuit in Fig. 7.1, a simplified equivalent circuit model is displayed in Fig. 7.5b. Using Fig. 7.5b, one can write the current i_2

$$i_2 = g_m V_1 + g_{mb1} V_2 - V_1 j\omega C_{gd1}. \tag{7.31}$$

At the node B in Fig. 7.5b, the KCL equation results in

$$V_2 j\omega(C_{sb1} + C_{db1}) + V_2 j\omega(C_{gs2} + C_{ds2}) + g_{m2} V_2 + \frac{V_2}{R1||r_{o2}} = (V_1 - V_2) j\omega C_{gb1} \tag{7.32}$$

Combining (7.31) and (7.32), Y_{21} is obtained:

$$Y_{21}(f) = \frac{i_2(f)}{V_1(f)}|_{V_2'=0} = -j\omega C_{gd1} + g_{m1} + \frac{j\omega C_{gb1} g_{mb1}}{j\omega C_{tot} + g_{m2} + \frac{1}{R1||r_{o2}}} \tag{7.33}$$

where $C_{tot} = C_{sb1} + C_{db1} + C_{gs2} + C_{ds2}$.

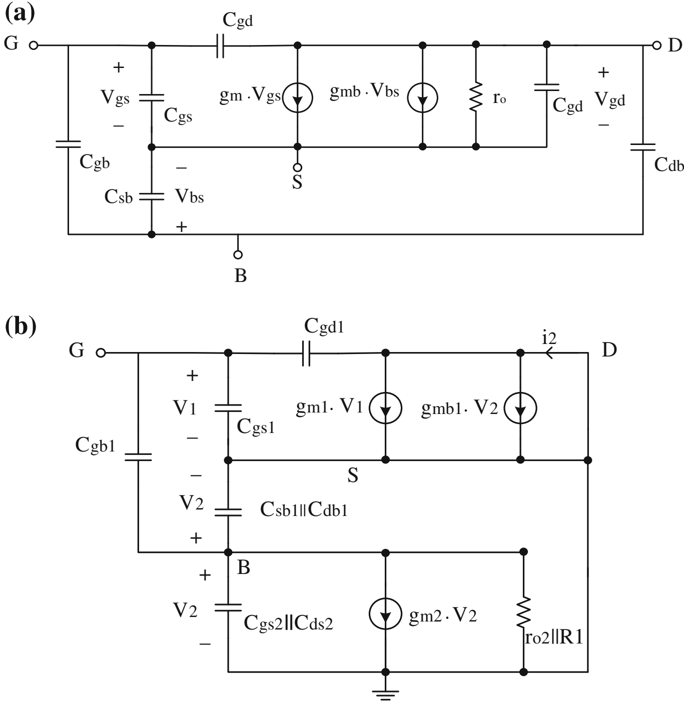

Fig. 7.5 a High frequency small-signal model of nMOSFET with body terminal and **b** small-signal model for Y_{21} derivation including substrate biasing circuit (© IEEE)

Note that V_2' in (7.33) represents what V_2 means in (7.29).

From (7.33) one can derive the fluctuation of Y_{21} as a function of g_{m1}, g_{mb1}, and g_{m2} as

$$\Delta Y_{21}(f) = \Delta g_{m1} - \frac{j\omega C_{\text{gb1}} g_{\text{mb1}}}{\left(j\omega C_{\text{tot}} + g_{m2} + \frac{1}{R1||r_{o2}}\right)^2} \Delta g_{m2} + \frac{j\omega C_{\text{gb1}}}{j\omega C_{\text{tot}} + g_{m2} + \frac{1}{R1||r_{o2}}} \Delta g_{\text{mb1}} \tag{7.34}$$

The second term in (7.34) will reduce Y_{21} sensitivity due to $M2$ in the DFR design. However, the third term in (7.34) due to the body effect of $M1$ will increase the fluctuation of Y_{21}. Thus, the transconductance of $M2$ helps reduce Y_{21} sensitivity, while the body transconductance of $M1$ may degrade Y_{21} sensitivity. Examining (7.26) and (7.34) together, the best sensitivity of noise figure and small-signal gain subject to body bias cannot be obtained simultaneously.

7.2 LNA Variability

A narrow-band cascode LNA designed at 24 GHz with adaptive body biasing is shown in Fig. 7.6. The main input transistor ($M1$) is connected with source degenerated inductor for better input matching and noise reduction. The cascode transistor ($M3$) provides the output to input isolation. All n-channel transistors are modeled using the PTM 65 nm technology [6]. The inductor values, MOS channel widths, and $R1$ are given in Fig. 7.6. V_{DD} = 1.0 V, V_{bias} = 0.7 V, and R_{bias} = 5 kΩ. The NF, NF_{min}, and S_{21} of the LNA without resilient biasing are 1.414, 1.226, and 12.124 dB at 24 GHz, while the corresponding values of the resilient design are 1.369, 1.327, and 11.531 dB, respectively.

Figures 7.7 and 7.8 show ADS Monte Carlo simulation [7] of the NF, NF_{min}, and S_{21} sensitivity subject to process variability. Monte Carlo simulation results demonstrate that a 10 % of V_T spread (STD/Mean) for the LNA without substrate biasing scheme yields 6.63 % NF spread and 5.58 % NF_{min} spread. A 10 % of V_T spread (STD/Mean) of the LNA with adaptive substrate biasing gives 3.85 % NF spread and 3.52 % NF_{min} spread. Comparing Figs. 7.7 and 7.8, it is apparent that the adaptive body biasing reduces the process variation effect significantly. It is also obtained that the ±0.2 V V_{tune} corresponds to the +5.41 to −4.16 % NF deviation and +5.20 to −3.92 % NF_{min} deviation. This spread fits into the compensation range for post-process V_{tune} calibration.

The reliability effect such as threshold voltage shift and mobility degradation on the LNA with or without adaptive substrate biasing is further evaluated. Figure 7.9 shows the normalized NF and NF_{min} to normalized threshold voltage shift for the

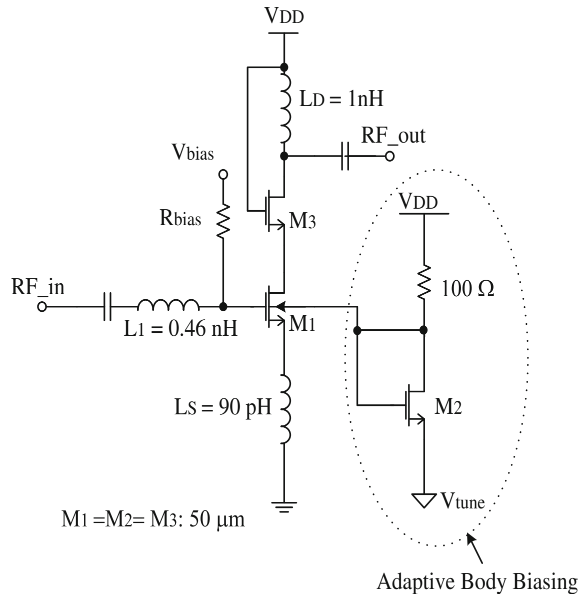

Fig. 7.6 A cascode low-noise amplifier with adaptive body bias (© IEEE)

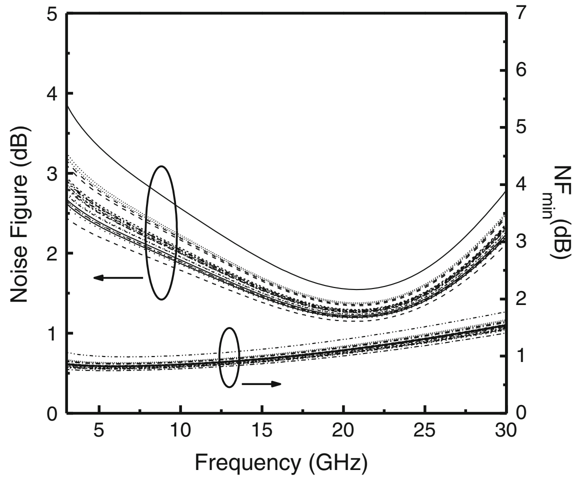

Fig. 7.7 Monte Carlo simulation of the LNA without substrate bias (© IEEE)

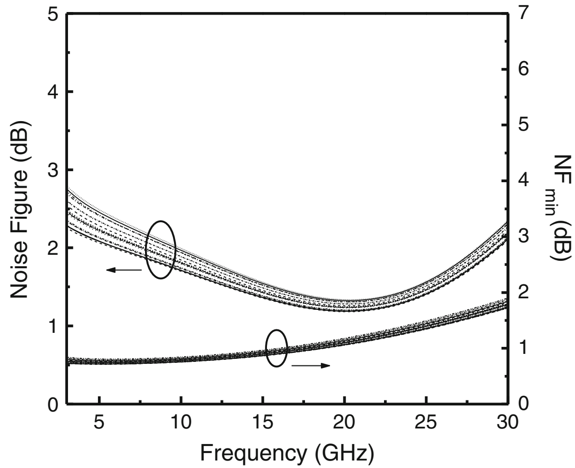

Fig. 7.8 Monte Carlo simulation of the LNA with the body bias technique (© IEEE)

original LNA compared to the LNA with adaptive bias design at different aging conditions. Since both drain-source voltage of main transistor *M*1 and substrate bias transistor *M*2 have the same designed drain-source voltage and similar gate-source voltage stress, *M*1 and *M*2 may have similar aging effect. However, different aging rates on *M*1 and *M*2 are also examined to account for a wide range of stress conditions. As seen in Fig. 7.9, the adaptive body biasing reduces the variation of normalized NF and NF_{min} significantly. In Fig. 7.9, the solid line represents the LNA without adaptive body bias and the solid lines with symbols represent the LNA with adaptive body bias, while the line with triangles corresponds to the *M*2 transistor's aging effect (threshold voltage shift or mobility degradation) is half of that of *M*1's, the line with empty circles is when both *M*1 and *M*2 have an identical

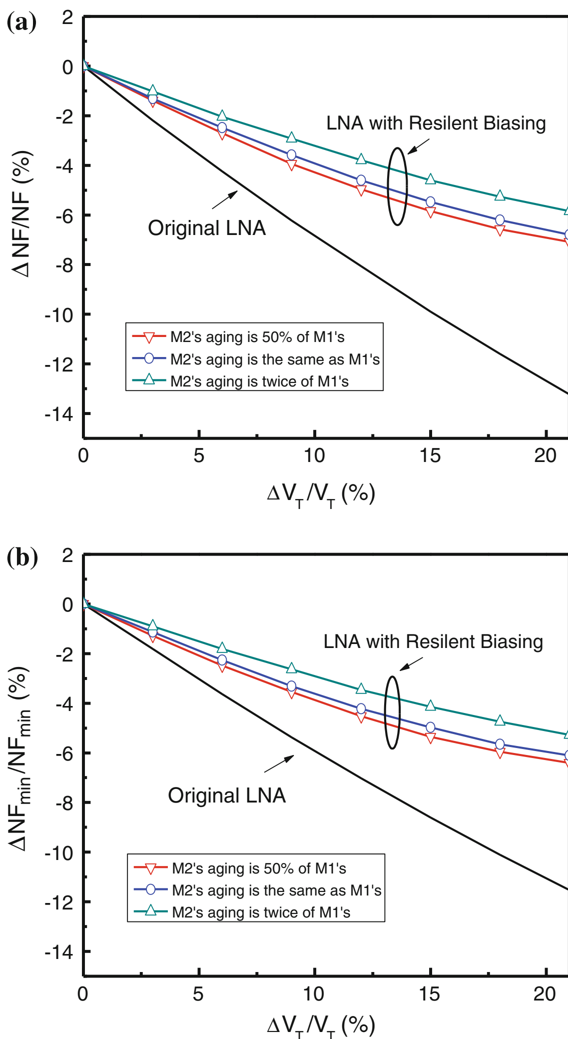

Fig. 7.9 Normalized **a** NF and **b** NF_{min} versus normalized V_T shift of the LNA without adaptive body bias compared to that with adaptive body bias (© IEEE)

aging degradation, and the line with inverse triangles represents that $M2$'s aging effect is twice of $M1$'s. It is seen from Fig. 7.9 that the LNA with resilient substrate bias scheme reduces the noise figure and minimum noise figure sensitivity significantly even when the $M2$'s aging is different from that of $M1$'s. It is interesting to point out that larger $M2$ aging in fact reduces the noise figure sensitivity even further. This is due to an additional $\delta V_T'$ in $M2$ to compensate the threshold voltage shift δV_{T0} in $M1$ as indicated in Eq. (7.7).

Figure 7.10 shows the normalized NF and NF_{min} variation versus normalized mobility degradation for the original LNA compared to the LNA with adaptive body bias at different mobility degradations. The line and symbol representations

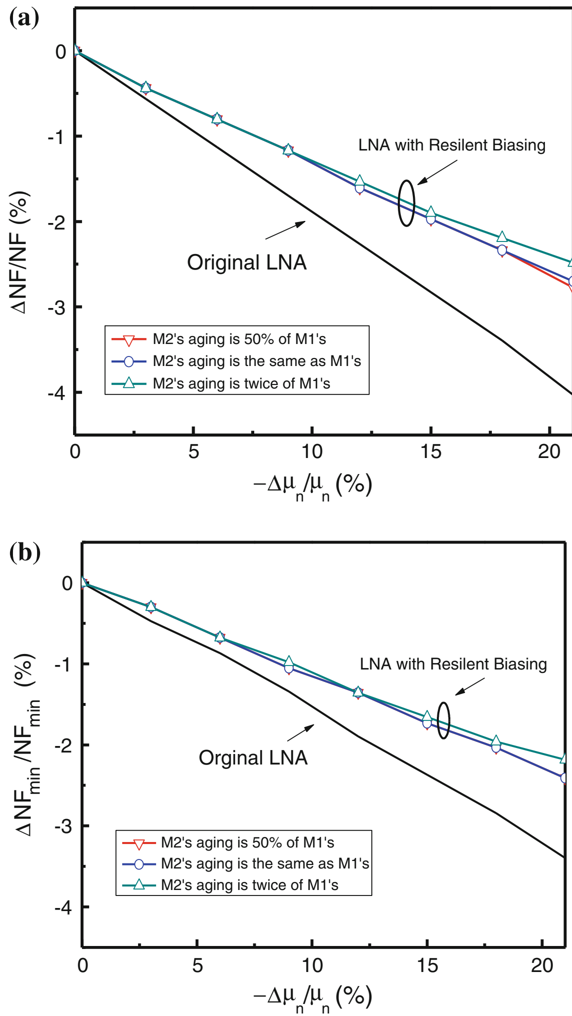

Fig. 7.10 Normalized **a** NF and **b** $\mathrm{NF_{min}}$ versus normalized μ_n degradation of the LNA without adaptive bias compared to the LNA with adaptive body bias (© IEEE)

are the same as those defined in Fig. 7.9. The adaptive body biasing reduces the sensitivity of normalized NF and $\mathrm{NF_{min}}$ against mobility degradation also, though its effect is not as large as that in threshold voltage shift. With larger aging degradation on $M2$, the resilient biasing effect is further improved slightly.

The small-signal gain sensitivity versus V_T shift considering different aging is displayed in Fig. 7.11. Again, in this figure the solid line represents the LNA without adaptive body bias and the solid lines with symbols represent the LNA with adaptive body bias, while the triangles correspond to the $M2$ transistor's aging effect is half of that of $M1$'s, the empty circles are when both $M1$ and $M2$ have the

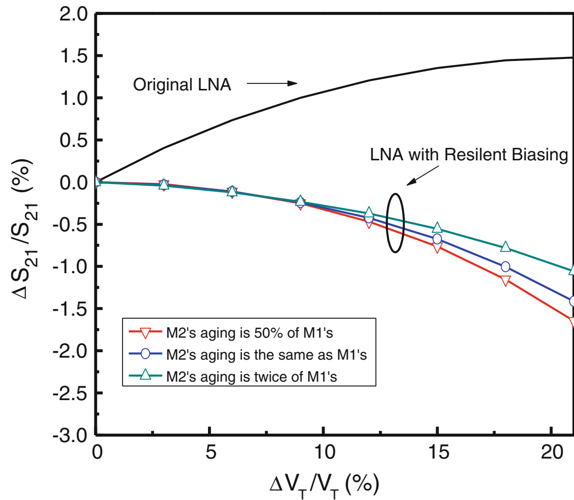

Fig. 7.11 Small-signal gain sensitivity versus threshold voltage shift (© IEEE)

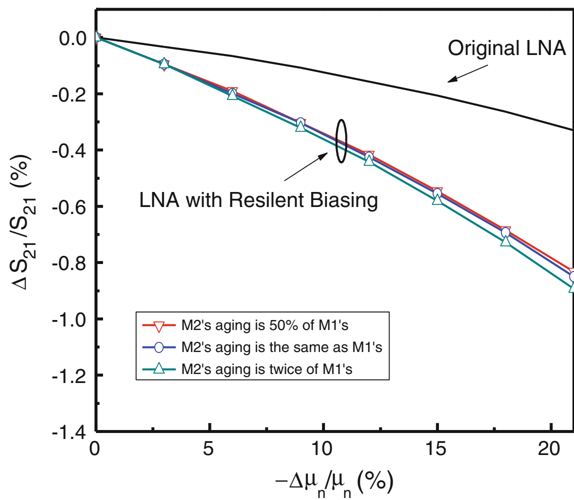

Fig. 7.12 Small-signal gain sensitivity versus electron mobility variation (© IEEE)

same aging degradation, and the inverse triangles represent $M2$'s aging effect twice of $M1$'s. In Fig. 7.11, the adaptive body biasing does not help reduce S_{21} sensitivity much as implied by Eq. (7.34). Figure 7.12 shows the normalized S_{21} sensitivity versus mobility degradation for the LNA with or without adaptive bias scheme. The adaptive body biasing increases the S_{21} sensitivity slightly subject to electron mobility degradation.

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