Chapter 4
FDTD Model for Crosstalk Analysis of Multiwall Carbon Nanotube (MWCNT) Interconnects

Abstract This chapter introduces an equivalent single conductor (ESC) model of MWCNT interconnects. Based on the ESC model, this chapter presents an accurate FDTD model of MWCNT while incorporating the quantum effects of nanowire and nonlinear effects of CMOS driver. To reduce the computational effort required for analyzing the CMOS driver, a simplified but accurate model is employed named as modified alpha-power law model.

Keywords Crosstalk · Equivalent *RLC* model · Kinetic inductance · Multiwall carbon nanotube (MWCNT) quantum resistance · Quantum capacitance

4.1 Introduction

The conventional interconnect copper material is unable to meet the requirements of future technology needs, since it suffers from low reliability with downscaling of interconnect dimensions. Moreover, the resistivity of copper increases, due to electron-surface scattering and grain boundary scattering with smaller dimensions. Therefore, researchers are forced to find an alternative material for global VLSI interconnects. Carbon nanotubes have been proposed to be one of the potential candidates for VLSI interconnects due to their unique physical properties, such as extraordinary mobility, large mean free path, and high current carrying capability [1, 2].

Carbon nanotubes can be classified into single-walled carbon nanotube (SWCNT) and multiwalled carbon nanotube (MWCNT) [3–6]. The promising interconnect solution for global interconnect lengths are MWCNTs due to their high current carrying capabilities than SWCNT bundles. Naeemi et al. observed that for longer interconnects, MWCNTs can have conductivities several times greater than SWCNT bundles [6]. Hence, many researchers consider the MWCNTs as a potential solution for global interconnect material. The experimental and theoretical investigations of MWCNTs as interconnect material have been presented in [7] and [8], respectively.

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The performance of an MWCNT interconnect line is generally evaluated by means of an equivalent transmission line model. Li et al. proposed a multiconductor transmission line (MTL) model to represent the MWCNT interconnect [9]. However, the analysis of MWCNT using the MTL model can be computationally expensive. For this reason, the equivalent single conductor (ESC) model was proposed in [8], using the assumption that voltage at an arbitrary cross section along MWCNT are the same, such that all nanotubes are connected in parallel at the both ends. The accuracy of the ESC model has been verified by several researchers [4, 8, 10]. They observed that the transient responses of ESC model and MTL model are in good agreement.

The FDTD technique has been used widely to analyze the transmission lines due to their better accuracy [11]. However, incorporation of different boundary conditions in the FDTD models is a challenging task. Previously, Paul [12, 13] incorporated the boundary conditions to analyze the transmission lines for resistive driver and resistive load boundaries. However, these studies were focused only on copper interconnects and hence, not suitable for next-generation graphene-based nanointerconnects. The quantum and contact resistances at the near-end and far-end terminals of a nanointerconnect line results in complex boundary conditions. For the first time, Liang et al. [14] proposed a crosstalk noise model for the analysis of MWCNT interconnects using FDTD technique. However, the authors represented the nonlinear CMOS driver by a resistive driver, thus limiting the accuracy of their model. Moreover, they did not validate their proposed model with respect to HSPICE. Therefore, a more accurate model is required that allows a better crosstalk-induced performance estimation of MWCNT interconnects.

The fabrication technique of MWCNT bundles was reported in [15], using thermal chemical vapor deposition technique. The authors have demonstrated the feasibility of growing perfectly aligned carbon nanotube bundles. Recently, Wang et al. [16] fabricated the MWCNTs arrays using microwave plasma chemical vapor deposition on Si substrate with interdigital electrodes. This method is able to control the thickness of MWCNT arrays based on the growth time. Although, the controlled growth of MWCNTs with high CNT density is realizable, the researchers are still facing some challenges in terms of large imperfect metal–nanotube contact resistance, poor control on number of shells, chirality and orientation, higher growth temperature during the fabrication process. However, efforts are underway to fabricate MWCNTs for interconnect applications.

This chapter presents an accurate numerical model for comprehensive crosstalk analysis of coupled MWCNT interconnects based on FDTD method. Using this method, the voltage and current can be accurately estimated at any particular point on the interconnect line. Since the proposed model requires less number of assumptions, the accuracy is very high. The nonlinear CMOS driver effects are incorporated using the modified alpha-power law model with suitable boundary conditions. Using the proposed FDTD method, the functional and dynamic crosstalk analysis is carried out. The results demonstrate that the proposed model has high accuracy that matches closely with the HSPICE results. In addition to this, the proposed model is highly time efficient than the HSPICE. Although, this chapter

demonstrates the crosstalk effects on two coupled interconnect lines, the model can be extended to N lines.

The rest of the chapter is organized as follows: Sect. 4.2 describes the ESC model of an MWCNT. In Sect. 4.3, the FDTD method is developed for coupled MWCNT interconnect lines. Section 4.4 is devoted to the validation of proposed model for coupled-two lines. In Sect. 4.5, the sensitivity analysis is performed to evaluate the validity of the assumptions associated with the proposed model. Finally, Sect. 4.6 concludes this chapter.

4.2 Equivalent Single Conductor Model of the MWCNT Interconnect

This section presents an equivalent *RLC* model of an MWCNT interconnect line. Consider a horizontal MWCNT bundle interconnect line positioned over a ground plane at a distance H and placed in a dielectric medium with dielectric constant ε. The geometry of an MWCNT interconnect is shown in Fig. 4.1. The coupling parasitics between the two MWCNT interconnects is shown in Fig. 4.2, where s is the spacing between the interconnect lines, and l_{12} and c_{12} represent the mutual inductance and coupling capacitance between the interconnect lines, respectively. The MWCNT interconnect consists of N number of tubes

$$N = 1 + \text{int}\left[\frac{(d_N - d_1)}{2\delta}\right] \tag{4.1}$$

where δ, d_1, and d_N represent intershell distance, innermost shell diameter, and outermost shell diameter, respectively.

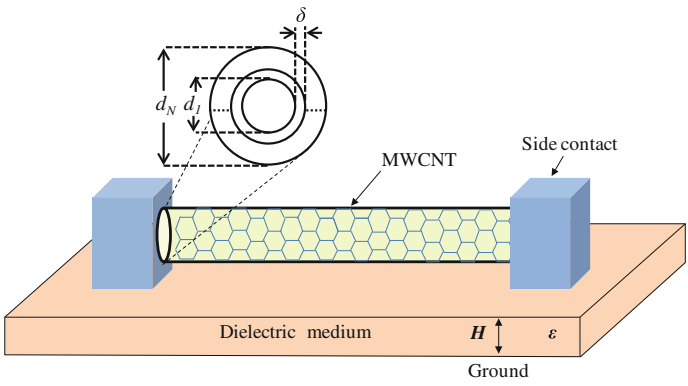

Fig. 4.1 Geometry of an MWCNT interconnect above the ground plane

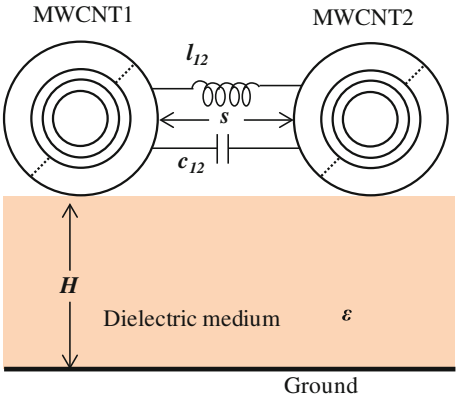

Fig. 4.2 Cross-sectional view and coupling parasitics between the MWCNT interconnects

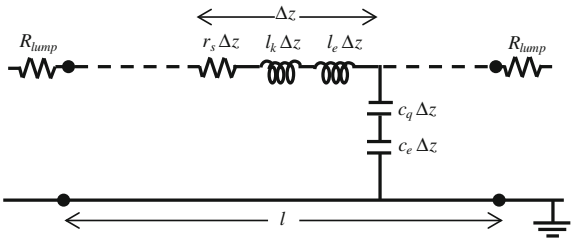

Fig. 4.3 Electrical equivalent model of an MWCNT interconnect

The MWCNT interconnect has been represented by an equivalent single conductor (ESC) model as shown in Fig. 4.3 [8]. The *RLC* parasitics of an MWCNT interconnect are primarily dependent on the number of conducting channels. The number of conducting channels in a CNT can be derived by adding all the subbands contributing to the current conduction. Using Fermi function, it can be expressed as

$$N_{\mathrm{ch},i} = \sum_{\text{subbands}} \frac{1}{\exp(|E_i - E_{\mathrm{F}}|/k_{\mathrm{B}}\,T) + 1} \tag{4.2a}$$

where T is the temperature, k_{B} is the Boltzmann constant, and E_i is the lowest (or highest) energy for the subbands above (or below) the Fermi level E_{F}.

A simplified form of expression (4.2a) is [6]:

$$\begin{aligned} N_{\mathrm{ch},i} &\approx k_1 T d_i + k_2 \qquad d_i > d_{\mathrm{T}}/T \\ &\approx 2/3 \qquad\quad d_i < d_{\mathrm{T}}/T \end{aligned} \tag{4.2b}$$

where d_i represents the diameter of CNT in an MWCNT, k_1 and k_2 are curve fitted constants. The value of d_{T} (=1300 nm K) is determined by the gap between the subbands and the thermal energy of electrons. The *RLC* parasitics can be extracted a follows:

4.2.1 Resistance

Each shell in the MWCNT primarily demonstrates three different types of resistances: (1) quantum resistance (R_Q) due to the finite conductance value of quantum wire if there is no scattering along the length; (2) imperfect metal–nanotube contact resistance (R_{MC}) that exhibits a value ranging from zero to few kilo-ohms depending on the fabrication process [17–19]; and (3) scattering resistance (r_s) due to acoustic phonon scattering and optical phonon scattering that occurs when the nanotube lengths exceed the mean free path of electrons. The scattering resistance appeared as per unit length distributed resistance along the line, whereas (1) and (2) are considered as lumped resistances placed at the contacts of near-end and far-end terminals. The overall effective lumped resistance at the near-end/far-end terminals of the MWCNT can be expressed as

$$R_{\text{lump,ESC}} = \frac{1}{2}\left[\sum_{i=1}^{N}\left(\frac{R_Q}{2N_{\text{ch},i}} + R_{\text{MC},i}\right)^{-1}\right]^{-1} \quad \text{where} \quad R_Q = \frac{h}{e^2} \approx 25.8\ \text{K}\Omega \tag{4.3a}$$

The p.u.l. scattering resistance of an MWCNT can be expressed as

$$r_{\text{s,ESC}} = \frac{h/e^2}{\sum_{i=1}^{N} 2N_{\text{ch},i}\,\lambda_{\text{mfp},i}} \quad \text{where} \quad \lambda_{\text{mfp},i} = \frac{10^3 d_i}{(T/T_0) - 2},\ T_0 = 100\,\text{K} \tag{4.3b}$$

where h and e represent the Planck's constant and the charge of an electron, respectively.

4.2.2 Inductance

The MWCNT demonstrates two different types of inductances:

(1) Magnetic inductance: The magnetic inductance (l_e) is due to the magnetic field generation around a current-carrying conductor. In the presence of ground plane, the p.u.l. magnetic inductance of a CNT shell shown in Fig. 4.4 is given by [20]

$$l_e = \frac{\mu}{2\pi}\cosh^{-1}\left(\frac{d+2H}{d}\right) \tag{4.4a}$$

where d and H represent the shell diameter and height from the ground plane, respectively. Additionally, the intershell mutual inductance (l_m) is mainly due to the magnetic field coupling between the adjacent shells in an MWCNT. The p.u.l. l_m can be expressed as [9]

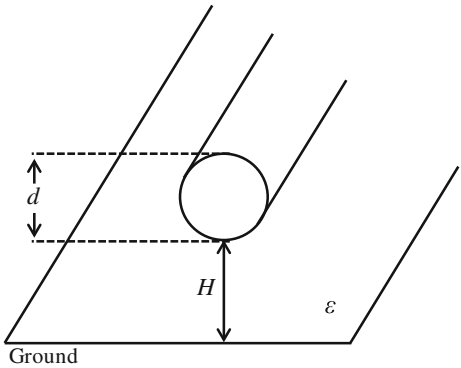

Fig. 4.4 A single CNT shell above a ground plane

$$l_m = \frac{\mu}{2\pi}\ln\left(\frac{d_i}{d_{i-1}}\right) \tag{4.4b}$$

(2) Kinetic inductance: The kinetic inductance (l_k) is mainly due to the kinetic energy of electrons. By equating kinetic energy stored in each conducting channel of a CNT shell to the effective inductance, the kinetic inductance of each conducting channel (l'_k) in a CNT can be expressed as [20]

$$l'_k = \frac{h}{2e^2 v_F} \tag{4.4c}$$

where v_F is the Fermi velocity $\approx 8 \times 10^5$ m/s [21].

By adopting a recursive approach proposed in [8], the equivalent inductance ($l_{k,ESC}$) of Fig. 4.3 can be expressed as

$$l_{equ,1} = l_{k,1} \tag{4.4d}$$

$$l_{equ,i} = \left(\frac{1}{l_{equ,\,i-1} + l_m^{i-1,i}} + \frac{1}{l_{k,\,i}}\right)^{-1}, \quad i = 2, 3, \ldots, N \tag{4.4e}$$

$$l_{k,ESC} = l_{equ,N} \tag{4.4f}$$

where

$$l_m^{i-1,i} = \frac{\mu}{2\pi}\ln(d_i/d_{i-1}), \quad i = 2, 3, \ldots, N \tag{4.4g}$$

$$l_{k,i} = \frac{1}{2N_{ch,i}}\frac{h}{2e^2 v_F} \quad 1 \le i \le N \tag{4.4h}$$

4.2.3 Capacitance

The MWCNT interconnect consists of two types of capacitances:

(1) Electrostatic capacitance: It represents the electrostatic field coupling between the CNT and the ground plane. The electrostatic capacitance (c_e) of MWCNT appears between the external shell and the ground plane, as external shell shields the internal ones. The p.u.l. c_e of a CNT shell shown in Fig. 4.4 can be expressed as [20]

$$c_e = \frac{2\pi\varepsilon}{\cosh^{-1}\left(\frac{d+2H}{d}\right)} \tag{4.5a}$$

Additionally, the intershell coupling capacitance (c_m) is mainly due to the potential difference between adjacent shells in MWCNT. The p.u.l. c_m can be expressed as [9]

$$c_m = \frac{2\pi\varepsilon}{\ln\left(\frac{d_i}{d_{i-1}}\right)} \tag{4.5b}$$

(2) Quantum capacitance: It originates from the quantum electrostatic energy stored in a CNT shell when it carries current. According to the Pauli exclusion principle, it is only possible to add extra electrons into the CNT shell at an available state above the Fermi level. By equating this energy to the effective capacitance energy, the quantum capacitance of each conducting channel (c'_q) in a CNT can be expressed as

$$c'_q = \frac{2e^2}{hv_F} \tag{4.5c}$$

The distributed line capacitance $c_{q,ESC}$ is expressed in terms of quantum capacitance (c_q) and coupling capacitance (c_m) between shells

$$c_{equ,1} = c_{q,1} \tag{4.5d}$$

$$c_{equ,i} = \left(\frac{1}{c_{equ,i-1}} + \frac{1}{c_m^{i-1,i}}\right)^{-1} + c_{q,i}, \quad i = 2, 3, \ldots, N \tag{4.5e}$$

$$c_{q,ESC} = c_{equ,N} \tag{4.5f}$$

where

$$c_m^{i-1,i} = \frac{2\pi\varepsilon}{\ln(d_i/d_{i-1})}, \quad i = 2, 3, \ldots, N \tag{4.5g}$$

$$c_{\mathrm{q},i} = 2N_{\mathrm{ch},i}\frac{2e^2}{hv_{\mathrm{F}}} \quad 1 \le i \le N \tag{4.5h}$$

4.3 FDTD Model of MWCNT Interconnect

The FDTD method is used to model the coupled MWCNT interconnect lines. The coupled-two interconnect lines are analyzed in this section; however, the model can be extended to coupled-N lines with a low computational cost.

4.3.1 The MWCNT Interconnect Line

The coupled-two MWCNT interconnect line structure is shown in Fig. 4.5, where $r_{\mathrm{s}1}$, $r_{\mathrm{s}2}$ are the scattering resistances; $l_{\mathrm{k}1}$, $l_{\mathrm{k}2}$ are the kinetic inductances; l_{e1}, l_{e2} are the magnetic inductances; $c_{\mathrm{q}1}$, $c_{\mathrm{q}2}$ are the quantum capacitances; $c_{\mathrm{e}1}$, $c_{\mathrm{e}2}$ are the electrostatic capacitances; and $C_{\mathrm{L}1}$, $C_{\mathrm{L}2}$ are the load capacitances of line 1 and line 2, respectively, where all these values are mentioned in p.u.l. The parameters c_{12} and l_{12} are the p.u.l. coupling capacitances and mutual inductances, respectively

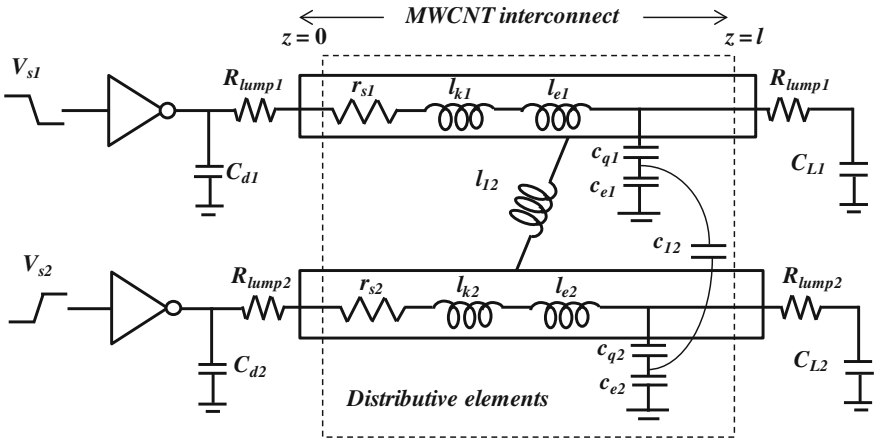

Fig. 4.5 Coupled MWCNT interconnect lines

[22–32]. The position along the interconnect line, and time are denoted as z and t, respectively.

For uniform coupled-two transmission lines the telegrapher's equations in the transverse electromagnetic (TEM) mode [11] are represented as

$$\frac{\mathrm{d}}{\mathrm{d}z}\boldsymbol{V}(z,t)+\boldsymbol{R}\boldsymbol{I}(z,t)+\boldsymbol{L}\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{I}(z,t)=0 \tag{4.6a}$$

$$\frac{\mathrm{d}}{\mathrm{d}z}\boldsymbol{I}(z,t)+\boldsymbol{C}\frac{\mathrm{d}}{\mathrm{d}t}\boldsymbol{V}(z,t)=0 \tag{4.6b}$$

where $\boldsymbol{V}$ and $\boldsymbol{I}$ are 2 × 1 column vectors of line voltages and currents, respectively. The line parasitic elements are obtained in 2 × 2 per unit length matrix form, i.e., $\boldsymbol{V}=\begin{bmatrix}V_1\\V_2\end{bmatrix}$, $\boldsymbol{I}=\begin{bmatrix}I_1\\I_2\end{bmatrix}$, $\boldsymbol{R}=\begin{bmatrix}r_{s1}&0\\0&r_{s2}\end{bmatrix}$, $\boldsymbol{L}=\begin{bmatrix}l_{k1}+l_{e1}&l_{12}\\l_{12}&l_{k2}+l_{e2}\end{bmatrix}$ and $\boldsymbol{C}=\begin{bmatrix}\left(1/c_{q1}+1/c_{e1}\right)^{-1}+c_{12}&-c_{12}\\-c_{12}&\left(1/c_{q2}+1/c_{e2}\right)^{-1}+c_{12}\end{bmatrix}$.

Central difference approximation is used to analyze the first-order differential Eqs. (4.6a) and (4.6b) by neglecting the higher order terms. This assumption results in a negligibly small loss of accuracy in the estimation of the transient response, since the value of time segment Δt is limited by CFL condition [33]. Using the FDTD method, the analysis of telegrapher's equations shows better accuracy, if the voltage and current points are chosen at the alternate space location and separated by one-half of the position discretization, i.e., $\Delta z/2$ [12]. In the same manner, the solution time for $\boldsymbol{V}$ and $\boldsymbol{I}$ should also be separated by $\Delta t/2$.

The interconnect line of length l is driven by a resistive driver at $z = 0$ and terminated by a capacitive load at $z = l$. The line is discretized into Nz uniform segments of length $\Delta z = l/Nz$. The voltage and current solution points are discretized along the line as shown in Fig. 4.6.

Applying finite difference approximations to (4.6a) results in

$$\frac{\boldsymbol{V}_{k+1}^{n+1}-\boldsymbol{V}_{k}^{n+1}}{\Delta z}+\boldsymbol{L}\frac{\boldsymbol{I}_{k}^{n+3/2}-\boldsymbol{I}_{k}^{n+1/2}}{\Delta t}+\boldsymbol{R}\frac{\boldsymbol{I}_{k}^{n+3/2}+\boldsymbol{I}_{k}^{n+1/2}}{2}=0 \tag{4.7a}$$

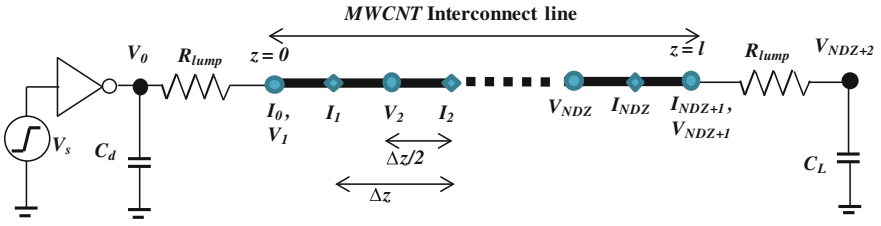

Fig. 4.6 Illustration of space discretization of line for FDTD implementation

$$\boldsymbol{I}_k^{n+3/2} = \boldsymbol{EF}\boldsymbol{I}_k^{n+1/2} + \boldsymbol{E}\left[\boldsymbol{V}_k^{n+1} - \boldsymbol{V}_{k+1}^{n+1}\right] \quad \text{for } k = 1, 2, \ldots, Nz \tag{4.7b}$$

where $\boldsymbol{E} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{L} + \frac{\Delta z}{2}\boldsymbol{R}\right]^{-1}$, $\boldsymbol{F} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{L} - \frac{\Delta z}{2}\boldsymbol{R}\right]$.

Applying finite difference approximations to (4.6b) results in

$$\frac{\boldsymbol{I}_k^{n+1/2} - \boldsymbol{I}_{k-1}^{n+1/2}}{\Delta z} + \boldsymbol{C}\frac{\boldsymbol{V}_k^{n+1} - \boldsymbol{V}_k^{n}}{\Delta t} = 0 \tag{4.8a}$$

$$\boldsymbol{V}_k^{n+1} = \boldsymbol{V}_k^{n} + \boldsymbol{D}\left[\boldsymbol{I}_{k-1}^{n+1/2} - \boldsymbol{I}_k^{n+1/2}\right] \quad \text{for } k = 2, 3, \ldots, Nz \tag{4.8b}$$

where $\boldsymbol{D} = \left[\frac{\Delta z}{\Delta t}\boldsymbol{C}\right]^{-1}$.

4.3.2 Boundary Condition at Near-End Terminal

The voltage and current points at the near-end terminal are represented by $\boldsymbol{V}_1$ and $\boldsymbol{I}_0$, respectively. As indicated in Fig. 4.6, it is observed that to apply the boundary conditions in (4.8b), Δz is replaced by $\Delta z/2$. Therefore, at $k = 1$ Eq. (4.8b) becomes

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{V}_1^{n} + 2\boldsymbol{D}\left[\boldsymbol{I}_0^{n+1/2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{4.9a}$$

The source current $\boldsymbol{I}_0$ at $(n + 1/2)$ time interval is obtained by averaging the source current at (n) and $(n + 1)$ time intervals. Then Eq. (4.9a) becomes

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{V}_1^{n} + 2\boldsymbol{D}\left[\frac{\boldsymbol{I}_0^{n+1} + \boldsymbol{I}_0^{n}}{2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{4.9b}$$

where $\boldsymbol{I}_0$ is the driver current. Applying Kirchhoff's current law (KCL) at near-end terminal, $\boldsymbol{I}_0$ can be written as

$$\boldsymbol{V}_0^{n+1} = \boldsymbol{V}_0^{n} + \boldsymbol{A}\left[\frac{\boldsymbol{C}_m}{\Delta t}\left(\boldsymbol{V}_s^{n+1} - \boldsymbol{V}_s^{n}\right) + \boldsymbol{I}_p^{n+1} - \boldsymbol{I}_n^{n+1} - \boldsymbol{I}_0^{n}\right] \tag{4.9c}$$

$$\boldsymbol{V}_1^{n+1} = \boldsymbol{B}\boldsymbol{V}_1^{n} + 2\boldsymbol{B}\boldsymbol{D}\left[\frac{\boldsymbol{V}_0^{n+1}}{2\boldsymbol{R}_{\text{lump}}} + \frac{\boldsymbol{I}_0^{n}}{2} - \boldsymbol{I}_1^{n+1/2}\right] \tag{4.9d}$$

$$\boldsymbol{I}_0^{n+1} = \frac{1}{\boldsymbol{R}_{\text{lump}}}\left[\boldsymbol{V}_0^{n+1} - \boldsymbol{V}_1^{n+1}\right] \tag{4.9e}$$

where $\boldsymbol{A} = \left[\frac{\boldsymbol{C}_m + \boldsymbol{C}_{\text{d}}}{\Delta t}\right]^{-1}$, $\boldsymbol{B} = \left[\boldsymbol{U} + \frac{\boldsymbol{D}}{\boldsymbol{R}_{\text{lump}}}\right]^{-1}$ $\boldsymbol{C}_m$ is the drain to gate coupling capacitance, $\boldsymbol{C}_{\text{d}}$ is the drain diffusion capacitance of CMOS inverter, $\boldsymbol{I}_p$ and $\boldsymbol{I}_n$ are the

PMOS and NMOS currents, respectively. The modified alpha-power law model that includes the drain conductance parameter is used to express the NMOS current as

$$\boldsymbol{I}_n = \begin{cases} 0 & \boldsymbol{V}_S \le V_{\text{tn}} \quad \text{(off)} \\ \boldsymbol{K}_{\text{ln}}(\boldsymbol{V}_s - \boldsymbol{V}_{\text{tn}})^{\alpha_n/2}\boldsymbol{V}_0 & \boldsymbol{V}_0 < \boldsymbol{V}_{\text{DSATn}} \quad \text{(lin)} \\ \boldsymbol{K}_{\text{sn}}(\boldsymbol{V}_s - \boldsymbol{V}_{\text{tn}})^{\alpha_n}(1+\sigma_n \boldsymbol{V}_0) & \boldsymbol{V}_0 \ge \boldsymbol{V}_{\text{DSATn}} \quad \text{(sat)} \end{cases} \tag{4.9f}$$

where K_{ln}, K_{sn}, V_{tn}, α_n, and σ_n are the linear region transconductance parameter, saturation region transconductance parameter, threshold voltage, velocity saturation index, and drain conductance parameter of NMOS, respectively. In a similar manner, the PMOS current can be expressed as

$$\boldsymbol{I}_p = \begin{cases} 0 & \boldsymbol{V}_S \ge \boldsymbol{V}_{\text{DD}} - \left|V_{\text{tp}}\right| \quad \text{(off)} \\ \boldsymbol{K}_{\text{lp}}\left(\boldsymbol{V}_{\text{DD}} - \boldsymbol{V}_s - \left|\boldsymbol{V}_{\text{tp}}\right|\right)^{\alpha_p/2}(\boldsymbol{V}_{\text{DD}} - \boldsymbol{V}_0) & \boldsymbol{V}_0 > \boldsymbol{V}_{\text{DD}} - \boldsymbol{V}_{\text{DSATp}} \quad \text{(lin)} \\ \boldsymbol{K}_{\text{sp}}\left(\boldsymbol{V}_{\text{DD}} - \boldsymbol{V}_s - \left|\boldsymbol{V}_{\text{tp}}\right|\right)^{\alpha_p}\left(1+\sigma_p(\boldsymbol{V}_{\text{DD}} - \boldsymbol{V}_0)\right) & \boldsymbol{V}_0 \le \boldsymbol{V}_{\text{DD}} - \boldsymbol{V}_{\text{DSATp}} \quad \text{(sat)} \end{cases} \tag{4.9g}$$

4.3.3 Boundary Condition at Far-End Terminal

Here the objective is to derive the voltage expression at $k = Nz + 1$ and $Nz + 2$.

At $k = Nz + 1$, Eq. (4.8b) becomes

$$\boldsymbol{V}_{Nz+1}^{n+1} = \boldsymbol{V}_{Nz+1}^{n} + 2\boldsymbol{D}\left(\boldsymbol{I}_{Nz}^{n+1/2} - \frac{\boldsymbol{I}_{Nz+1}^{n+1} + \boldsymbol{I}_{Nz+1}^{n}}{2}\right) \tag{4.10a}$$

Applying KCL at far-end terminal, the output current ($\boldsymbol{I}_{Nz+1}$) can be expressed as

$$\boldsymbol{V}_{Nz+1} - \boldsymbol{V}_{Nz+2} = \boldsymbol{R}_{\text{lump}}\boldsymbol{I}_{Nz+1} \tag{4.10b}$$

The discretized form of (4.10b) is

$$\boldsymbol{I}_{Nz+1}^{n+1} = \frac{1}{\boldsymbol{R}_{\text{lump}}}\left[\boldsymbol{V}_{Nz+1}^{n+1} - \boldsymbol{V}_{Nz+2}^{n+1}\right] \tag{4.10c}$$

Using (4.10a) and (4.10c) the far-end voltage $\boldsymbol{V}_{Nz+1}$ can be expressed as

$$\boldsymbol{V}_{Nz+1}^{n+1} = \boldsymbol{B}\boldsymbol{V}_{Nz+1}^{n} + 2\boldsymbol{B}\boldsymbol{D}\left[\frac{\boldsymbol{V}_{Nz+2}^{n+1}}{2\boldsymbol{R}_{\text{lump}}} + \boldsymbol{I}_{Nz}^{n+1/2} - \frac{\boldsymbol{I}_{Nz+1}^{n}}{2}\right] \tag{4.10d}$$

and the load voltage $\boldsymbol{V}_{Nz+2}$ is

$$\boldsymbol{V}_{Nz+2}^{n+1} = \boldsymbol{V}_{Nz+2}^{n} + \frac{\Delta t}{\boldsymbol{C}_L}\boldsymbol{I}_{Nz+1}^{n} \tag{4.10e}$$

These equations are evaluated in a bootstrapping fashion. Initially, the voltages along the line are evaluated for a specific time from Eqs. (4.9c), (4.9d), (4.8b), (4.10e), and (4.10d) in terms of the previous values of voltage and current. Thereafter, the currents are evaluated from (4.9e), (4.7b), and (4.10c) in terms of these voltages and previous current values.

4.4 Validation of the Model

The coupled MWCNT interconnects are analyzed using the actual CMOS driver. The proposed model is implemented with the MATLAB. The industry standard HSPICE simulations are used for the validation of the results. The HSPICE simulations are carried out using the subcircuit model with 50 distributed segments for interconnect and using BSIM4 technology model for MOSFET. A symmetric CMOS driver is used to drive the interconnect load. The equivalent resistance of the driver is evaluated by averaging the resistance value over an interval when the input is between V_{DD} and $V_{DD}/2$ [34]. The signal integrity analysis is carried out at the global interconnect length of 1 mm for 32 nm technology and 0.9 V of V_{DD}. The interconnect dimensions are based on the ITRS data [35]. The interconnect width and height from the ground plane are 48 and 110.4 nm, respectively. The spacing between the two interconnects is 48 nm. The relative permittivity of the inter layer dielectric medium is 2.25. The load capacitance and input transition time are 2 fF and 20 ps, respectively. The following *RLC* parasitics are used in the experiments [36–43]:

$$\boldsymbol{R} = \begin{bmatrix} 653.67 & 0 \\ 0 & 653.67 \end{bmatrix} \frac{\text{k}\Omega}{\text{m}}, \quad \boldsymbol{L} = \begin{bmatrix} 14.83 & 0.61 \\ 0.61 & 14.83 \end{bmatrix} \frac{\mu\text{H}}{\text{m}} \quad \text{and}$$

$$\boldsymbol{C} = \begin{bmatrix} 93.33 & -71.50 \\ -71.50 & 93.33 \end{bmatrix} \frac{\text{pF}}{\text{m}}$$

In the interconnect system, lines 1 and 2 are considered as aggressor and victim lines, respectively. For the above-mentioned setup, the transient response is analyzed at the far-end terminal of the victim line using the proposed model, resistive driver-based model [14], and HSPICE simulations using CMOS driver. From Fig. 4.7, it can be observed that the model presented in [14] is unable to capture the timing waveform accurately. However, the proposed model is able to successfully capture the HSPICE waveform characteristics.

The crosstalk-induced delay is analyzed under two different cases. First case considers out-phase delay where the input signals of aggressor and victim lines are

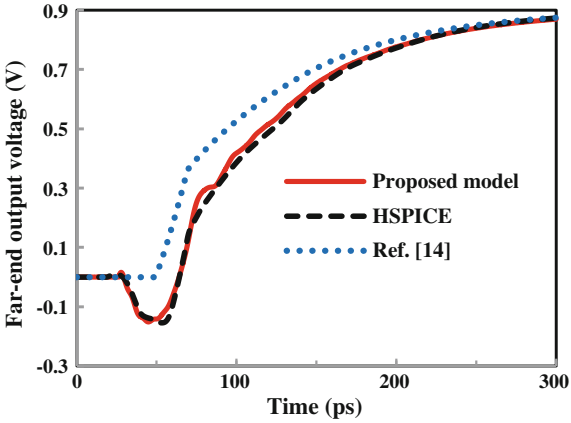

Fig. 4.7 Transient response at the far-end terminal of the victim line when the aggressor and victim lines are switched out-of-phase

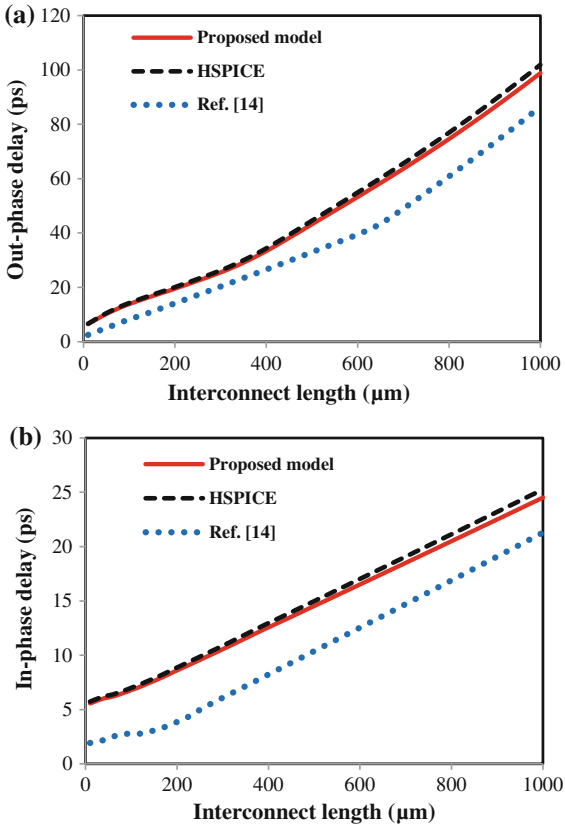

Fig. 4.8 Crosstalk-induced delay comparison **a** out-phase delay and **b** in-phase phase delay with the variation of interconnect length

switched out-of-phase. Second case considers in-phase delay where the input signals of aggressor and victim lines are switched in-phase. Figure 4.8a, b show out-phase and in-phase delay comparison, respectively, for different interconnect

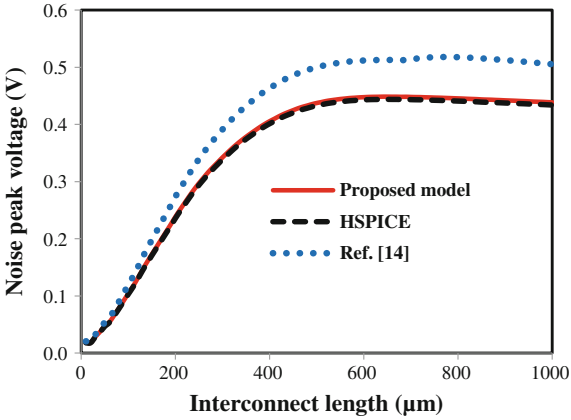

Fig. 4.9 Noise peak voltage comparison of victim line 2 with the variation of interconnect length

lengths. It can be clearly observed that the model proposed in [14], fails to estimate the crosstalk-induced delay for all interconnect lengths. The model proposed in [14] underestimates the delay for both out-phase and in-phase switching by average errors of 27.2 and 35.3 %, respectively.

The functional crosstalk noise is analyzed when the aggressor line is switched and the victim line is kept in quiescent mode. Figure 4.9 depicts the noise peak voltage comparison on the victim line. It can be observed that the resistive driver model [14] overestimates the noise peak voltage, wherein the average error is observed to be 15 %.

To test the robustness, the proposed model is examined at different input transition times. The interconnect length is considered as 500 μm. Figure 4.10 depicts the computational error involved in predicting the crosstalk-induced propagation delay. It can be observed that the proposed model accurately predicts the delay for both out-phase and in-phase transitions. The average error involved is only 1.4 and

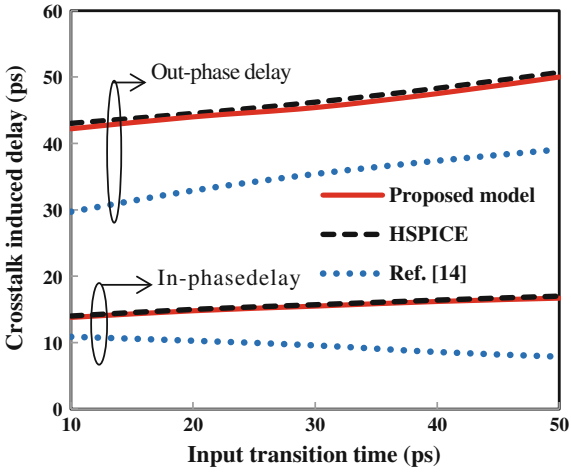

Fig. 4.10 Crosstalk-induced delay comparison on victim line 2 with the variation of input transition time

Table 4.1 CPU runtime comparison between proposed model and HSPICE with 1000 time segments

Number of space segments	HSPICE (s)	Proposed model (s)	% reduction in runtime
1	0.14	0.02	85.71
10	0.68	0.06	91.17
50	2.97	0.23	92.25
100	6.04	0.31	94.86

1.5 % during in-phase and out-phase switching, respectively. Contrastingly, with the resistive driver model [14], the average errors involved are 38.6 and 25.1 % for in-phase and out-phase switching, respectively.

Modified nodal analysis (MNA) is the core approach used in SPICE to formulate the system equations. Applying the Kirchhoff's current law and following the energy conversion principle, the MNA generates the set of matrix equations. The order of the matrix is determined by the number of nodes and unknown variables in the circuit. The unknown variables are solved after the inversion of the matrix and therefore require more computational time. However, the FDTD operator is matrix free and therefore fast and memory efficient as compared to HSPICE simulations.

The efficiency of the proposed model is examined under different test cases. The analysis is carried out by varying the space segment while keeping the time segment constant for coupled interconnects. Using a PC with Intel Dual Core CPU (2.33 GHz, 4 GB RAM), the comparison results are provided in Table 4.1. Using the proposed model, it is observed that the CPU runtime reduces by an average of 91 % in comparison to HSPICE simulations. Additionally, the proposed model is compared with the HSPICE simulations using the same modified alpha-power law model. It is observed that the average CPU runtime reduces by 88 % in comparison to HSPICE simulations.

4.5 Sensitivity Analysis

The primary assumptions made in the proposed work are for: (1) number of conducting channels and (2) contact resistance. This subsection presents the sensitivity analysis to evaluate the validity of these assumptions.

4.5.1 Sensitivity Analysis for Number of Conducting Channels

The number of conducting channels in a CNT can be obtained from expression (4.2b), which is an approximated form of (4.2a). Table 4.2 shows the variations in

Table 4.2 Variation between (4.2a) and (4.2b) on parasitics and crosstalk-induced performance parameters

Variation between (4.2a) and (4.2b)	Parasitic parameter				Performance parameter		
	Lumped resistance (Ω)	Scattering resistance (Ω)	C (fF)	L (pH)	Noise peak voltage (V)	In-phase delay (ps)	Out-phase delay (ps)
From Eq. (4.2a)	11.79	675.10	21.84	15.28	0.433	26.0	64.3
From Eq. (4.2b)	11.43	653.67	21.83	14.83	0.424	25.3	63.6
% change	3.05	3.17	0.04	2.94	2.1	2.6	1.1

parasitics and crosstalk-induced performance parameters using Eqs. (4.2a) and (4.2b). The average percentage change in parasitics and performance parameters are just 2.3 and 2 %, respectively. It can be inferred that the parasitics and crosstalk-induced performance parameters are almost insensitive to the usage of approximated expression for obtaining N_{ch} [44].

4.5.2 *Sensitivity Analysis for Contact Resistance*

The value of imperfect metal contact resistance can range from the best case value of zero to the worst case value of few kilo-ohms depending on the fabrication process. As reported earlier [9], the R_{MC} value is considered as 3.2 kΩ per shell. However, a sensitivity analysis on parasitic $R_{lump,ESC}$ and crosstalk-induced performance parameters for R_{MC} varying from 0 to 8 kΩ is carried out and the results are presented in Table 4.3. A maximum variation of 5 % in $R_{lump,ESC}$ and almost no change in the crosstalk performance are noticed with the change in R_{MC}. This is due to the fact that the crosstalk-induced performance parameters primarily depend on the scattering resistance and almost insensitive to the change in R_{MC}.

Table 4.3 Variation of performance parameters due to change in R_{MC}

Parasitic parameter		Performance parameter			
R_{MC} (per shell) (k Ω)	Lumped resistance ($R_{lump,ESC}$) (Ω)	Noise peak voltage (V)	Noise peak timing (ps)	In-phase delay (ps)	Out-phase delay (ps)
0	11.20	0.425	54.5	25.1	63.5
2	11.3	0.425	54.4	25.3	63.5
4	11.49	0.424	54.4	25.3	63.6
6	11.63	0.424	54.4	25.4	63.6
8	11.77	0.424	54.4	25.4	63.8

4.6 Summary

This chapter presented an accurate model to analyze the crosstalk effects in coupled MWCNT interconnect lines. The CMOS driver and the coupled MWCNT interconnect are modeled by modified alpha-power law model and FDTD method, respectively. It has been observed that the results of the proposed model exhibit a good agreement with HSPICE simulations. Over the random number of test cases, the average error in the propagation delay measurement is observed to be less than 2 %. Moreover, the sensitivity analysis is performed based on the assumptions used in the proposed model. It is observed that the percentage change in parasitic elements and performance parameters are almost negligible with respect to the assumptions associated with the model. This analysis suggests that with continuous advancements in FDTD technique the proposed model would play a significant role in performance analysis of MWCNT on-chip interconnects and would be potentially incorporated in TCAD simulators.

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