

A Novel Thermal Protection Circuit Based on Bandgap Voltage Reference

Wei Ding, Yong Xu, Rui Min, Zheng Sun and Yuan-Liang Wu

Abstract A novel thermal protection circuit based on a bandgap voltage reference is presented in this paper. Simulation was carried out using Cadence Spectre, based on a 0.25 μm CMOS (Complementary Metal-Oxide-Semiconductor Transistor) process, which indicated that the thermal protection temperature threshold is approximately 130 $^{\circ}\text{C}$. It was also found that the hysteresis is nearly 20 $^{\circ}\text{C}$ in all types of process corners, and the designed bandgap reference voltage is 1.205 V with a temperature coefficient of 12.84 ppm/ $^{\circ}\text{C}$.

Keywords Thermal protection · Hysteresis temperature · Bandgap voltage reference · CMOS

1 Introduction

With the development of high performance and high speed integrated circuits, the thermal problem in chips has attracted increasing attention [1]. The chip, particularly the power-integrated circuit with large consumption, can be permanently damaged when the internal temperature exceeds the permitted temperature [2, 3].

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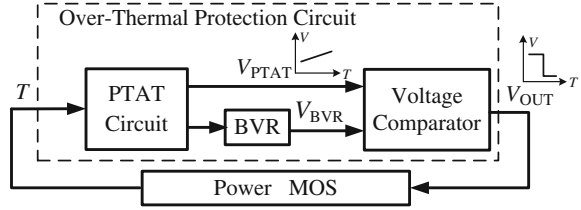
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Fig. 1 Block diagram of the thermal protection circuit



In order to ensure the reliability and lifetime of the circuit, a thermal protection circuit should be integrated into the chip [4, 5]. In this paper, a novel thermal circuit is proposed which consists primarily of PTAT (Proportional To Absolute Temperature) circuit, BVR (Bandgap Voltage Reference) and voltage comparator; the block diagram is shown within the dotted box in Fig. 1. The PTAT circuit beside the power MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) detects the internal temperature of the chip and transfers it to V_{PTAT} , which is proportional to the absolute temperature. When the temperature exceeds the acceptable temperature, the V_{OUT} would shut off the power MOS via the comparison of V_{PTAT} and V_{BVR} .

This work proposes a CMOS thermal protection circuit based on bandgap reference sources. The simulation results of the proposed circuit in a 0.25 μm CMOS process indicates that the circuit has the characteristics of simple structure, long-term stability, low power consumption and strong portability.

2 Circuit Design

The thermal protection circuit consists of four parts, including the PTAT & BVR circuit, temperature judgment circuit, bias circuit and startup circuit. The implemented structure is presented in Fig. 2.

2.1 PTAT & BVR Circuit

As the core of the circuit, the PTAT & BVR circuit consists of M_{11} – M_{17} , R_0 – R_4 , Q_1 – Q_2 , and op amp A_1 . In order to increase the stability of BVR, the circuit adopts a cascade current mirror [6]. Furthermore, the output of A_1 is set as the bias voltage of the cascode to introduce negative feedback while M_{11} and M_{12} have the same ratio of width and length, namely, $S_{11} = S_{12}$. Consequently, the current I_0 is given as [7]:

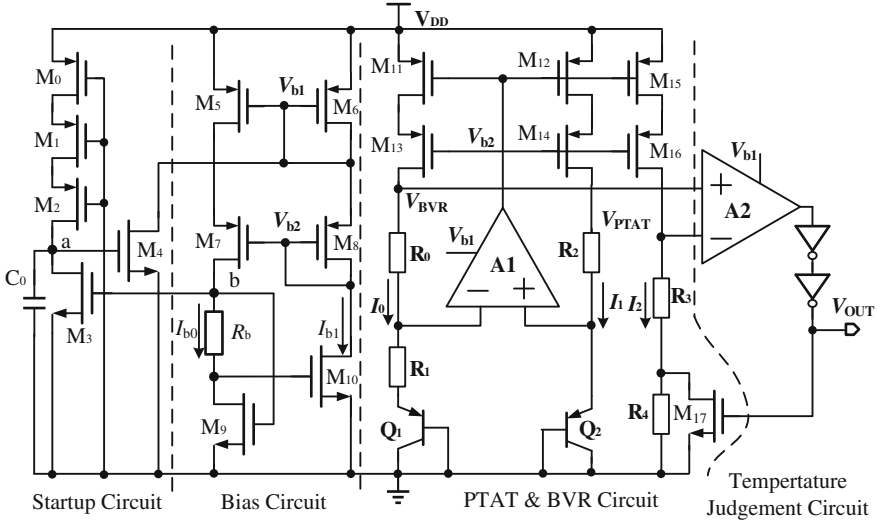


Fig. 2 Schematic of proposed thermal protection circuit

$$I_0 = I_1 = \frac{\ln n}{R_1} V_T \tag{1}$$

where V_T is the thermal voltage, n is the ratio between the emitter areas of the Q_2 and Q_1 bipolar transistors, $V_T = (k/q)T$, k is Boltzmann's constant, T is temperature and q is the conducted charge. V_T with the temperature coefficient $+0.085 \text{ mV}/^\circ\text{C}$ at room temperature is proportional to the absolute temperature T .

It is clear that I_0 is proportional to the temperature, so that I_0, I_1, I_2 are all positive temperature coefficients. The PTAT voltage is expressed as:

$$V_{PTAT} = \ln n \frac{S_{15} R_3}{S_{11} R_1} V_T \tag{2}$$

Equation (2) implies that V_{PTAT} is entirely independent of the power supply and process parameters. The ratio of resistances is not sensitive to temperature changes when using the same type of resistance. Therefore, V_{PTAT} has good linearity by ignoring the effects of resistance temperature characteristic.

V_{BVR} is the terminal voltage of R_0 , and can be expressed as:

$$V_{BVR} = \ln n \frac{R_0}{R_1} V_T + V_{EB2} \tag{3}$$

At room temperature, V_{EB2} has a negative temperature coefficient of approximately $-2.2 \text{ mV}/^\circ\text{C}$. Therefore, V_{BVR} has little dependence on the power supply and

process parameters by adjusting the ratio of resistor R_0 and R_1 . V_{BVR} realizes zero temperature coefficient, namely, the BVR [8].

2.2 Temperature Judgment Circuit

The temperature judgment circuit consists of a comparator A2 and two inverters. A2 adopts the classical two-stage CMOS op amp using M_{18} – M_{24} is shown in Fig. 3. The first stage consists of differential amplifier PMOS transistors; the second stage consists of a common-source MOSFET, and M_{18} , M_{23} provide bias currents.

The integrated op amp A1 has the same structure. A miller compensation is adopted by connecting capacitor C_1 between the outputs of two stages in order to achieve adequate phase margin ($>60^\circ$) to ensure A1 working steadily [9].

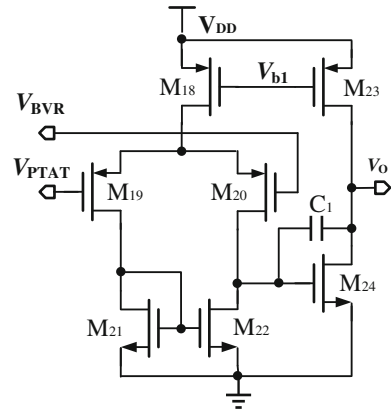
At room temperature, V_{PTAT} is less than V_{BVR} . While the temperature rises, V_{PTAT} increases linearly until $V_{PTAT} = V_{BVR}$. And the comparator flips at the temperature, namely thermal temperature protection T_+ [10]. From this relationship, T_+ can be expressed as:

$$T_+ = \frac{q V_{BVR} S_{11} R_1}{k \ln n S_{15} R_3} \quad (4)$$

It is shown that T_+ is determined by the ratio of R_1 and R_3 . Simultaneously, the temperature characteristic of V_{BVR} also determines the stability of T_+ .

V_{OUT} is the output of the comparator shaped by two-stage inverter. Once the temperature exceeds T_+ , V_{OUT} jumps to low level which can shut off the power MOS and M_{17} . Meanwhile, V_{PTAT} is increased by the voltage drop of R_4 . Once V_{PTAT} is equal to V_{BVR} , V_{OUT} turns to high level and opens power MOS and M_{17} at the threshold temperature named T_- . The hysteresis temperature ΔT can be solved as follows:

Fig. 3 Comparator circuit



$$\Delta T = T_+ - T_- = \frac{1}{R_3/R_4 + 1} T_+ \quad (5)$$

It is clear that ΔT is determined by R_4 at certain T_+ . The feedback circuit composed of M_{17} and R_4 introduces a hysteresis comparison that the risk of thermal oscillation phenomena can be avoided at the temperature T_+ [11].

2.3 Bias Circuit and Startup Circuit

As shown in Fig. 2, the bias circuit supplies bias current I_{b0} and the bias voltages V_{b1} and V_{b2} for op amp A1, A2, PTAT and BVR circuit.

Once the bias circuit is unable to provide necessary voltages and currents, the entire circuit will fail to work normally [12]. So the startup circuit which consists of M_0 – M_4 and C_0 is necessary. After power is on, C_0 will be charged until point a exceeds the threshold voltage of M_4 . After M_4 is on, V_{b1} decreases and point b increases. Then, M_3 is on, point a is much less than the threshold voltage of M_4 , and M_4 is reliably disconnected between the startup circuit and the bias circuit. Thus far, the entire startup process is complete and the bias circuit is in normal balance.

3 Simulation Results and Discussion

The proposed circuit is implemented in a CSMC 0.25 μm 2P5M process. As shown in Fig. 4, the layout covers an area of $0.27 \times 0.29 \text{ mm}^2$. V_{BVR} and V_{out} can be scanned in five parameters: tt, ss, ff, sf and fs corners from -40 to 150 $^\circ\text{C}$. The results of Cadence Spectre simulation is shown in Figs. 5 and 6.

Figure 5 shows that V_{BVR} is highly overlapping at all corners. This indicates that V_{BVR} is little influenced by the corners, in favor of the stability of the temperature of thermal protection. It is observed that the center value of V_{BVR} is 1.205 V with a temperature coefficient of 12.84 ppm/ $^\circ\text{C}$.

V_{OUT} is scanned in double direction in the range of -40 to 150 $^\circ\text{C}$, the simulation results in Fig. 6 indicate that the protection temperature is 130 $^\circ\text{C}$, hysteresis temperature is 20 $^\circ\text{C}$, and the proposed circuit exhibits good temperature sensitivity. The maximum temperature error is 1.4 $^\circ\text{C}$ in different process corners, and the hysteresis temperature approximation is 20 $^\circ\text{C}$ in the same corner. This validates the stability and reliability of the proposed circuit.

Furthermore, the same performance was recorded from other simulation results. Table 1 lists the performance comparison with other works. It is shown that the proposed circuit in this paper has several advantages, such as the largest temperature range and power supply range, smallest circuit area, and good temperature coefficient.

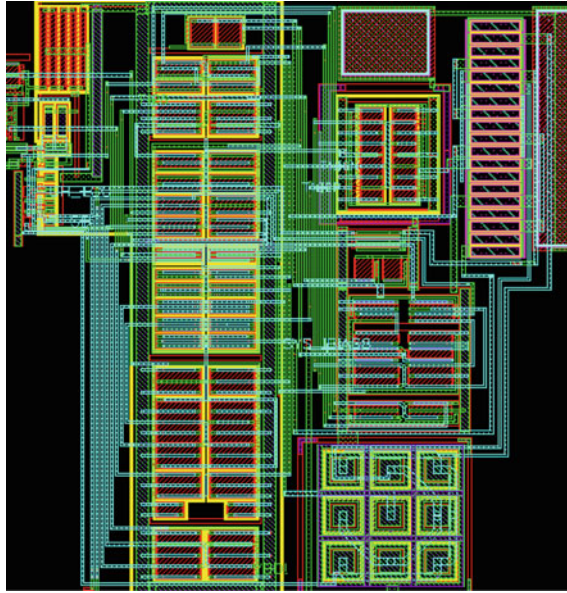


Fig. 4 Layout of the circuit

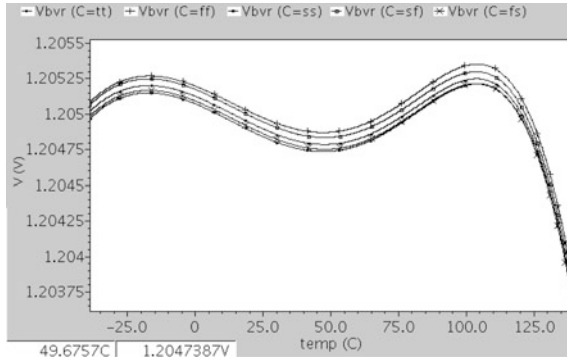


Fig. 5 Simulated temperature characteristic of V_{BVR}

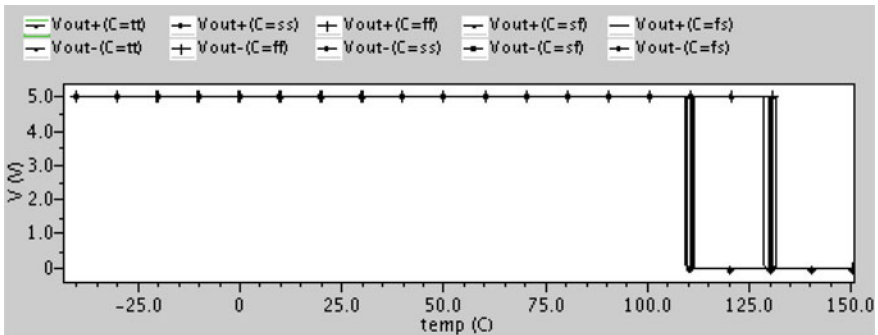


Fig. 6 Simulated temperature characteristic of the output

Table 1 Performance comparison with other works

	Current work	Dong et al. [13]	Wang et al. [14]
Process (μm)	0.25	0.6	0.18
Scale of temperature ($^{\circ}\text{C}$)	-40 to 150	30-130	0-120
Power supply (V)	1.6-10	4.5-5.5	0.7-3.6
V_{REF} (V)	1.205	2.75	0.4306
Temperature coefficient (ppm/ $^{\circ}\text{C}$)	12.84	86	2.97
Area (mm^2)	0.27×0.29	1.9695×1.9683 include pad	0.02

4 Conclusions

A novel thermal protection circuit based on CMOS BVR is proposed. Cadence Spectre simulation results show that the thermal protection temperature is approximately 130°C , the temperature error is less than 1.4°C , the hysteresis temperature is nearly 20°C , and the bandgap reference voltage is 1.205 V with a temperature coefficient $12.84\text{ ppm}/^{\circ}\text{C}$ from -40 to 150°C . Long-term stability, high sensitivity, small size, and high portability have been achieved by the proposed circuit which can be widely used in different application fields.

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