

Crosstalk Noise Voltage Analysis in Global Interconnects

Purushottam Kumawat and Gaurav Soni

Abstract The rapid growth of VLSI technology is generally due to the continuous reduction in the feature size of device. The work of an interconnect is to distribute the data signals and to make available power or ground to and among the different circuit functions on the chip. As the scaling of devices, the traditional transistor has thus far met the challenges like crosstalk, coupling, and noise margin. Due to this, scaling of interconnects has become one of the performance limiting factor for the new VLSI designs. As the advancements in process technology scaling are going on, the spacing between the adjacent interconnect wires keeps shrinking. This causes an increase in coupling capacitance between the interconnect wires. Hence, coupling noise became an important part which must be taken into account while performing timing verification for VLSI chips. The crosstalk generated due to switching of signals will induce noise onto nearby lines which can further deteriorate the signal integrity and reduce noise margins. These aspects of crosstalk make the system performance dependent on data patterns, switching rates, and line-to-line spacing.

Keywords Crosstalk · Parasitic capacitance · Signal integrity

1 Introduction

Interconnects are used to connect components on a VLSI chip, to connect chips on a multichip structure, and to connect multichip structures on a system board. As transistors become smaller in size, they dissipate lesser power, switch faster, and are cheaper to manufacture. Interconnects can be categorized as local, semi-global, and global. Local interconnects are the lowest level of interconnects. These are used in

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localized regions of a chip to provide electrical path between nearby nodes. They use the most bottom layers of metals. Semi-global interconnects are usually used to connect devices within a block. The coupling phenomenon occurs in digital as well as in analog blocks. However, digital blocks are more densely interconnected to each other and for this reason, coupling of capacitance tends to be more significant in this type of circuit. Crosstalk owing to capacitive coupling wires can result in functional failure of the circuit. It is a well-known fact that signal integrity (SI) is robustly affected by both the nonlinear behavior of CMOS drivers and the transmission line behavior of interconnect. Therefore, accurate estimation of time delay and crosstalk noise should be done. Crosstalk in one line to another will occur when the electromagnetic fields from different structures come interact. In multiconductor systems, excessive line-to-line coupling can create some pernicious effects. The crosstalk is also one of them that will affect the performance of interconnect by modifying the propagation velocity and effective characteristic impedance. This will adversely affect signal integrity and system level timings. The crosstalk will also induce noise into other nearby lines which can further degrade the signal integrity of the integrated circuit. This aspect of crosstalk makes the system performance densely dependent on switching rates, data patterns, and line-to-line spacing [1].

2 Signal Transmission in Interconnect

Any electronic system is composed of functional blocks interconnected with each other; that is, capable of transmitting signal from one part to another. This information is in the form of a voltage or a current value. Ideally, the transmission of the signal between two interconnected blocks must be without any distortion and instantaneous. However, this ideal picture cannot be achieved in practice. The reason behind is that physically there is always a propagation time for transmitting the information from one point to the other. If the signals varies very slowly compared to this propagation time, the transmission may be considered instantaneous and the ideal picture is right. Hence, signal delay must be taken into account when designing the system to ensure that all the blocks receive the information at the expected time. If, on the other hand, the signal varies hastily compared to the propagation time, several effects may be observed:

- Reflections coming from the end of the interconnection and it interfered with the signal sent.
- Interference between nearby interconnections (Crosstalk).

All these effects may influence the behavior of the system and they represent a limitation on performance. If they are not properly addressed at the design stage, they may be adequate to completely distort the transmitted signal and therefore cause a system malfunction [2].

3 Physical Factors Affecting Interconnect Design

The signal transmission will eventually depend on some physical factors of the interconnections that determine the respective values of R , L , and C . There are three physical components influencing electrical parameters:

- Material properties of the conductors forming interconnects and the dielectrics between them. This affects R and C respectively.
- The Dimensions of conductor and dielectric materials: width, length and thickness of conductors, pitch and dielectric thickness, which determines the distance between stacked interconnections. This influences R , L and C .
- Connection of the wires carrying reference voltages, generally known as power supply distribution. This Influence on L and C .

The first depends exclusively on technology, the second one depends on technological design and restrictions, and the third one depends mostly on design, but is also restricted by the type of technology used [3].

4 Modeling an Interconnect

4.1 Transmission Line Model

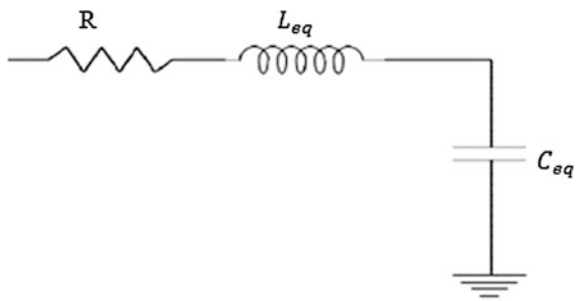
The RLC transmission line model is used to represent the wire as interconnects. The model was developed to calculate equivalent circuit parameters for a copper-based interconnect geometry (Fig. 1).

According to the model, the thickness of interconnect is t , the width of interconnect is w , and h is the height of interconnect above the ground. The mathematical formulae for these are [4]:

Resistance

$$R = \frac{\rho L}{A} = \frac{\rho L}{HW} \quad (1)$$

Fig. 1 Transmission line using RLC [4]



Capacitance

$$C_W = \varepsilon \left[1.15 \frac{w}{t} + 2.80 \left(\frac{h}{t} \right)^{0.222} + \left(0.66 \frac{w}{t} + 1.66 - 0.14 \left(\frac{h}{t} \right)^{0.222} \right) \cdot \left(\frac{t}{s} \right)^{1.34} \right] \quad (2)$$

$$C_c = \varepsilon \left[1.14 \frac{t}{s} \left(\frac{h}{h+2.06s} \right)^{0.09} + 0.74 \left(\frac{w}{w+1.59s} \right)^{1.14} + 1.16 \left(\frac{w}{w+1.87s} \right)^{0.16} \cdot \left(\frac{h}{h+0.98s} \right)^{1.18} \right] \quad (3)$$

where

s is the interwire spacing (assumed $s = w$), ε is the dielectric permittivity, and $C_c =$ Coupling Capacitance.

For global inductance, we include inductance whose formula is:

Inductance

$$L_W = 2 \times 10^{-7} l \left(\ln \frac{2l}{w+h} + 0.5 + \frac{w+h}{3l} \right) \quad (4)$$

4.2 Crosstalk

Crosstalk is defined as the energy proclaimed to a transmission line due to signals in nearby lines. The magnitude of the induced crosstalk noise is a function of net configuration, rise time, and signal line geometry. More aggressive technology scaling will cause an increment in the contribution of the coupling capacitances to the total interconnects capacitance.

4.3 Interconnect Modeling Fundamentals

Crosstalk is caused by energy coupling from one line to another line via:

1. Mutual capacitance, C_m (Fig. 2)
2. Mutual inductance, L_m (Fig. 3)

$$V_{\text{noise}} = L_m dI_{\text{driver}}/dt \quad (5)$$

$$I_{\text{noise}} = C_m dV_{\text{driver}}/dt \quad (6)$$

Fig. 2 Mutual capacitance (C_m) [5]

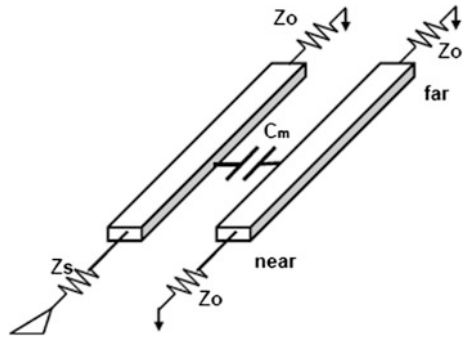
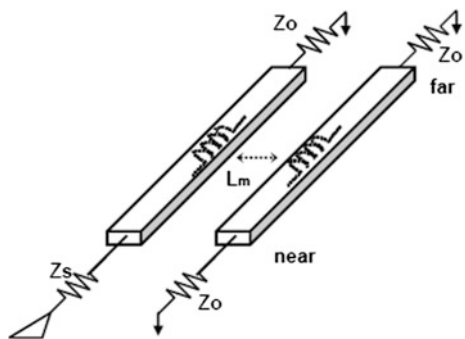


Fig. 3 Mutual inductance (L_m) [5]



Coupled currents on victim line is sum to produce near and far-end crosstalk noise which is given by

$$I_{\text{near}} = I_{C_m} + I_{L_m} \tag{7}$$

$$I_{\text{far}} = I_{C_m} - I_{L_m} \tag{8}$$

4.4 Odd Mode Propagation

When the two coupled interconnects are carrying the voltages of equal magnitude and phase difference of 180° with each other, then it is called odd mode propagation. The effective capacitance of interconnects will be augmented by twice the mutual capacitance and on the other side, the equivalent inductance will be decreased by the mutual inductance [1, 5].

4.5 Even Mode Propagation

When the coupled interconnects are carrying the voltages of same magnitude and in phase with each other, then this type of propagation is called even mode. In this mode, the effective capacitance of the line will be decreased by the mutual capacitance and on the other side, equivalent inductance will be increased by the mutual inductance. The current in this mode contains equal magnitude and flow in the same direction between the two coupled lines and interacts with each other. These interactions affect the delay and impedance of the transmission line [1, 5].

5 Circuit Models and Parameters Used

See Table 1.

6 Noise Analysis in Interconnect

Experimental set up as shown in Fig. 4 have been used for the crosstalk noise analysis. Two interconnects shown are coupled by a coupling capacitor (C_c). CMOS inverters have been used as driver and load. The input signal is transmitted through the first interconnect (known as aggressor interconnect) and the effect of switching is measured in the second interconnect (known as victim interconnect). When the signal goes from one state to another state in aggressor, a spike (crosstalk noise) is generated in the victim line which affects the information traveling through it. Input has been taken in the form of a pulse for transient analysis and the output waveforms are shown in Figs. 5 and 6. The experiment has been done for different lengths of interconnects, different power supply values, different frequencies of input signal, and also for different dielectric material. The RLC parameters calculated for different interconnect lengths is shown in Table 2.

Table 1 Hardware, software, and parameters used by various researchers

Circuit model used	Software used	Parameter	Results
Interconnect using RLCG	H-SPICE	$R = 8.829 \Omega$	The run time off is reduced to 0.01–0.003 [6]
		l (pH/ μm) = 1.538	
		c (fF/ μm) = 0.18 (parasitic parameter)	
Interconnect using RLCG	H-SPICE	$R_s = 100 \Omega$	The Time delay is reduced to 181.32–173.23 ps [7]
		$C_1 = 1.75$ pF	
RLC interconnect network	H-SPICE	line resistance varying from 0 to 90 Ω	% error in delay is reduced to 7.5–6.3 % [8]

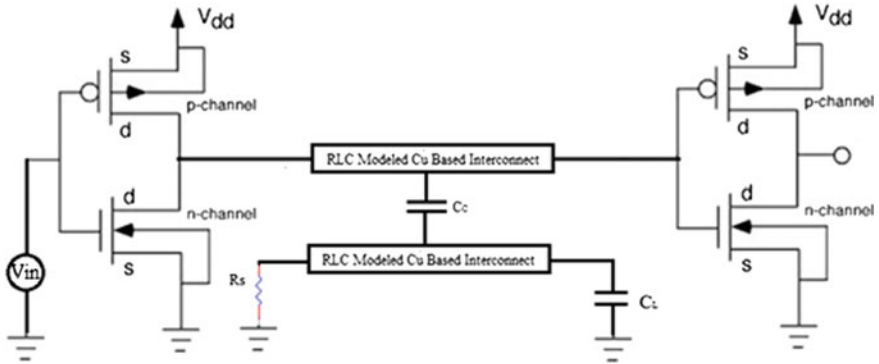


Fig. 4 Experimental set up

Fig. 5 Transient response of coupled interconnect at 200 μm length

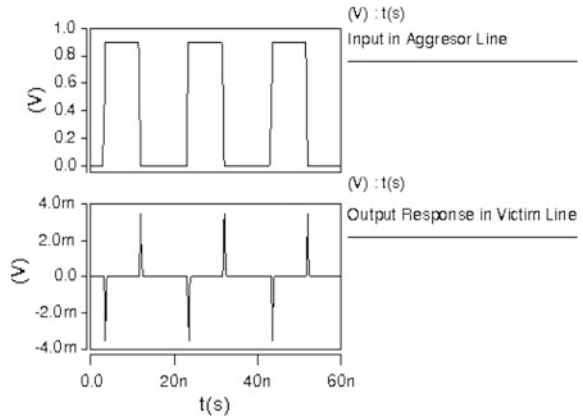


Fig. 6 Transient response of coupled interconnect at 300 μm length

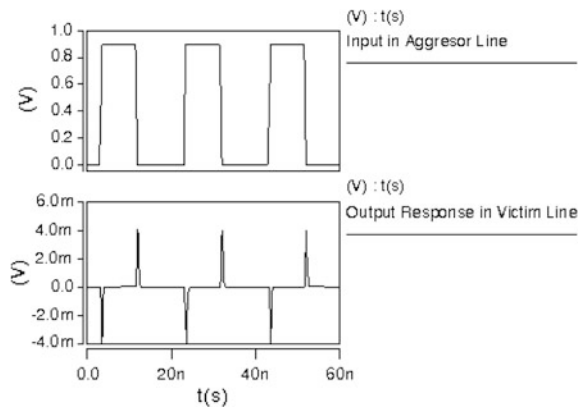


Table 2 RLC parameters for different lengths of transmission line

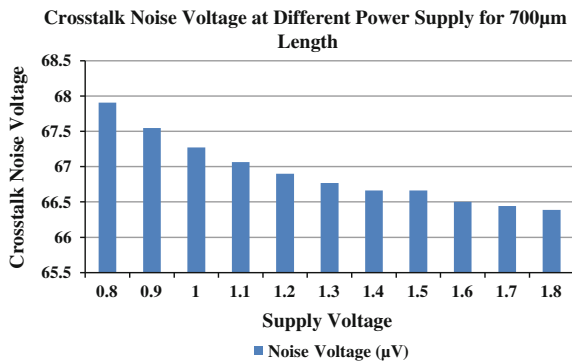
Length (μm)	R (Ω)	L (nH)	C_g (fF)
200	4.074	0.106	14.5418
300	8.148	0.239	29.0836
400	12.222	0.383	43.6254
500	16.296	0.534	58.1672
600	20.37	0.69	72.709
700	24.444	0.85	87.2508
800	28.518	1.014	101.7926
900	32.592	1.18	116.3344
1000	36.666	1.349	130.8762

Table 3 Crosstalk noise voltage at different lengths

Length of interconnect (μm)	Noise voltage (μV)
200	63.5230
300	64.4574
400	64.6542
500	64.9832
600	65.1891
700	65.5469
800	65.9544
900	66.7898
1000	66.9887

(for $V_{dd} = 0.9 \text{ V}$; input = 0.9 V)

Fig. 7 Noise at different power supply voltages (length = 700 μm)



It is to be noted here that parasitic inductances have not been considered for analysis of crosstalk noise.

The calculated output noise for different lengths of interconnects is listed in Table 3. The interconnect length has been varied from 200 to 1000 μm for crosstalk analysis.

Table 4 Crosstalk noise voltage of 700 μm interconnect length with different power supply voltages

V_{dd} (V)	Noise voltage (μV)
0.8	67.9102
0.9	67.5469
1.0	67.2750
1.1	67.0662
1.2	66.9023
1.3	66.7710
1.4	66.6642
1.5	66.6642
1.6	66.5034
1.7	66.4418
1.8	66.3877

(Input = 0.9 V)

Table 5 Crosstalk noise voltage at different interconnect lengths with different dielectric materials

Interconnect length (μm)	Dielectric material		
	SiO ₂ (μV)	Al (ceramic package) (μV)	HfO ₂
200	64.6542	63.9926	62.5667
300	64.523	64.4494	63.4727
400	64.4574	63.4295	63.2951
500	64.255	63.7595	62.7733
600	64.1891	62.8861	62.8031
700	67.5469	64.2344	62.0253
800	63.9832	63.5778	61.8396

(for $V_{\text{dd}} = 0.9$ V; input = 0.9 V)

Power supply voltage is varied for 700 μm interconnect length from 0.8 to 1.8 V. The effect of power supply variation is shown in Fig. 7 (Table 4).

The noise voltages at different frequencies are listed in Table 6 (Fig. 9).

7 Results

The two capacitively coupled interconnects with CMOS driver and load circuit were used for analyzing crosstalk noise voltage. The interconnect length was varied from 200 to 1000 μm . Table 3 shows that as the length is increased the noise voltage is also increased for capacitively coupled interconnect. However it increases if parasitic inductances are also considered for crosstalk noise analysis [2, 9]. The

Table 6 Crosstalk noise voltage for 700 μm interconnect length with different frequencies

Frequency	Noise voltage (μV)
200 MHz	12.8216
400 MHz	18.0933
600 MHz	22.0887
800 MHz	25.4019
1 GHz	28.2622
1.2 GHz	30.7866
1.4 GHz	33.0451
1.6 GHz	35.0837
1.8 GHz	36.9352
2 GHz	38.6246
10 GHz	59.3642
20 GHz	62.0447

(for $V_{dd} = 0.9 \text{ V}$; input = 0.9 V)

Fig. 8 Crosstalk noise voltage at different dielectric materials

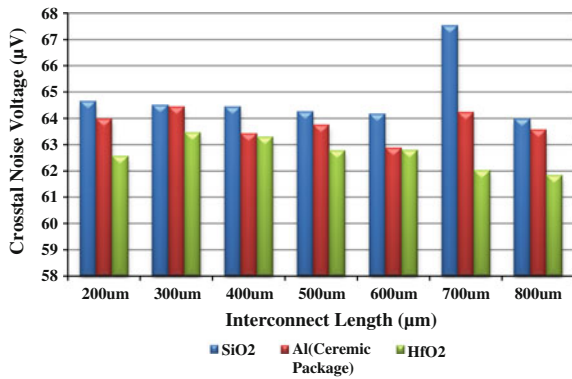
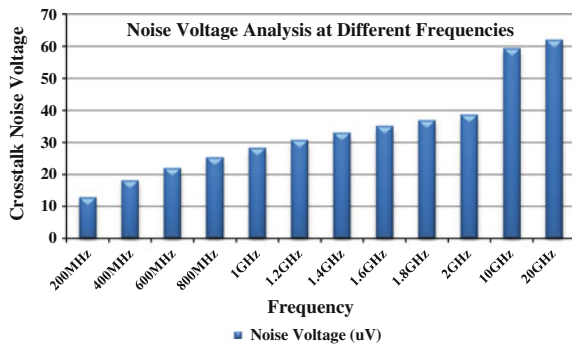


Fig. 9 Crosstalk noise voltage at different frequencies (length = 700 μm)



effect of power supply variation was also carried out in which supply voltage was varied from 0.8 volt to 1.8 volt. The result as shown in Fig. 7 indicates that as the power supply voltage is increased, the crosstalk noise voltage is decreased. At lower supply voltages, the noise voltage is high. Also, the crosstalk noise voltage was measured for different dielectric materials like SiO₂, Al (Ceramic Package), and HfO₂. Lower crosstalk noise voltage was observed with HfO₂ material as shown in Fig. 8. Figure 9 represents that as the frequency increases, the noise voltage also increases. At lower frequency, the noise is low but at higher frequencies it increases rapidly.

8 Conclusion

The experimental results show that copper is not a suitable material for interconnects in low power, high speed, and complex chips based on devices of nanometer regime. The ever-increasing density, performance, and reliability requirements of VLSI circuits create significant process integration challenges for the future interconnect systems. So facing to these issues, new materials such as CNT and optical interconnects can play a vital role in meeting the performance challenge.

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