General Principles of Spin Transistors and Spin Logic Devices

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Abstract

This chapter provides an overview of the field of spin-based devices, circuits, and architectures for digital information processing. Electron spin – as opposed to electron charge – is used as a classical degree of freedom to encode binary bits, and this approach improves the energy efficiency of information processing. However, there are also disadvantages associated with unreliability, difficulty of reading and writing information, and sometimes the need for cryogenic operation. These issues are discussed exhaustively, pointing the readers to niche applications where spin-based devices may offer some advantage. Both the basic and the applied aspects of spintronic information processing are discussed.

Introduction

The fundamental device at the heart of all digital computing hardware is the binary switch that has two well-separated stable states. They store and encode the binary bits 0 and 1. When the switch is implemented with metal-oxide-semiconductor field-effect transistors (MOSFET), the two states are the high-conductance ("on") and low-conductance ("off") states of the device. The MOSFET is turned on by moving charge into the "channel" and turned off by moving charge out. Switching is therefore associated with motion of charges.

In all charge-based switches, the switching action invariably requires charge motion. This is because charge is a *scalar* quantity. Therefore, the two states must be demarcated by a difference in the magnitudes of the charge in the device. Switching will require changing the magnitude by an amount ΔQ, in a time Δt,

leading to a current flow of magnitude $I = \Delta Q/\Delta t$. This current causes an unavoidable energy dissipation of $I^2R\Delta t = (\Delta Q)^2R/\Delta t$, where R is the resistance in the path of the current. One can reduce this dissipation by increasing Δt (switching slowly) or by decreasing ΔQ, but neither is desirable since the former makes the switch slow and error prone, while the latter reduces noise immunity since it decreases the logic-level separation by bringing the two states closer together.

The above shortcoming of charge-based devices has motivated the search for alternate state variables, such as electron spin, to encode binary bits. For example, a single electron's spin polarization in a magnetic field has two stable states that are parallel and antiparallel to the field since these are the allowed eigenstates. These two mutually antiparallel polarizations can encode the bits 0 and 1. Switching between them merely requires flipping the spin, without moving the electron in space and causing current flow. This eliminates the $I^2R\Delta t$ dissipation, but does not eliminate dissipation altogether since the two spin states are nondegenerate and separated in energy by the Zeeman splitting $g\mu_B B$ (g = Landé g-factor, μ_B = Bohr magneton, B = flux density of the magnetic field). Therefore, even if a single spin is used as a binary switch [1], the minimum energy dissipation would have been $g\mu_B B$ per bit flip event.

In fact, the minimum energy dissipation for any "single" entity (single spin, single charge, single "anything") will be always $k_BT\ \ln(1/p)$(k_B = Boltzmann constant, T = absolute temperature, and p = probability of random switching between the two bits at temperature T) as long as the switch is in thermodynamic equilibrium with its surrounding (and therefore characterized by a unique temperature T) [2, 3]. From that perspective, it should make no difference whether single charge or single spin is used as the vehicle to encode logic bits. However, what does make a difference is that no single entity is ever stable enough in a noisy environment to encode logic bits reliably. Therefore, an *ensemble* of entities (many spins, many single electron charges) is required to encode a logic bit in a robust fashion. In that case, *spin has a very important advantage over charge*.

The minimum energy dissipated to switch an ensemble of information carriers (spins, charges, etc.) is $Nk_BT\ \ln(1/p)$, where N is the number of degrees of freedom that the ensemble possesses. In the case of charges, $N = M$, where M is the number of charges in the ensemble. This happens because the different charges act independently. However, in the case of spin, $N \sim 1$, since exchange interaction between spins makes all of them act in unison. In fact, in a single-domain magnet, the entire ensemble behaves like one giant classical spin [4, 5], and all spins rotate together under an applied torque, so that effectively $N = 1$. Therefore, the minimum ratio of the dissipations incurred in switching a spin ensemble and a charge ensemble is

$$\frac{\text{Dissipation}|_{\text{spin ensemble}}}{\text{Dissipation}|_{\text{charge ensemble}}} = \frac{1}{M}$$

which gives spin a significant advantage over charge when $M > 1$.

Spin Field-Effect Transistors

The field of "spintronics," which deals with the science and technology of storing, processing, and communicating information (including digital information in the form of binary bits 0 and 1) via the spins of charge carriers, came into maturity with the early proposals for spin field-effect transistors (SPINFETs) [6]. In a SPINFET, the current flowing between two terminals (the "source" and the "drain") is modulated by applying an electrostatic potential to the third terminal (the "gate"), as in a MOSFET. The difference is that the gate potential does not modulate the charge, or number of charge carriers, in the channel, but instead modulates the spin polarization of the carriers. If the source and drain contacts are efficient spin filters, then modulation of the spin polarization can modulate the current flowing between the source and drain, thus realizing transistor action. The gate potential can therefore turn the transistor on or off, but without changing the amount of charge in the channel. In other words, $\Delta Q = 0$, which should make the energy dissipation $(\Delta Q)^2 R/\Delta t$ vanish. That it does, but there is additional energy cost associated with modulating spin polarization, and that cost may or may not exceed $(\Delta Q)^2 R/\Delta t$. If it does exceed, then the SPINFET is actually less energy efficient than the MOSFET. This issue will be visited later following the description of the earliest SPINFET due to Datta and Das [6], but it is curious that numerous papers on spintronics start out with the preamble "spin devices/transistors promise low dissipation and faster speed. . .." Unfortunately, there is almost never any substantiation of such claims in the same papers. The reality is that spin transistors are generally no more energy efficient than MOSFETs, and they are not faster either. In fact, they may have major shortcomings that make them less desirable than MOSFETs as binary switches. These issues are discussed later in this chapter.

Datta-Das Transistor

The spin field-effect transistor (SPINFET) concept was first proposed more than two decades ago by Datta and Das [6]. They examined a structure identical to that of a traditional depletion-mode MOSFET that is normally on, i.e., the transistor's conductance is high when the gate voltage is zero. Application of a gate voltage turns the transistor off by making the conductance go low. The only difference between the SPINFET's and the depletion-mode MOSFET's structure is that the source and drain contacts in the SPINFET are ferromagnetic and magnetized along the direction of current flow. Figure 1 shows this structure. Although the channel can be either one-, two-, or three-dimensional, the operation of the transistor will be explained by assuming it to be one-dimensional (a quantum wire), with only the lowest transverse subband occupied by carriers. Extension of the theory to polydimensional channels, or even the one-dimensional channel with multiple subbands occupied, is unfortunately not trivial and will be addressed later.

The two ferromagnetic contacts in the SPINFET are magnetized along the direction of current flow in the channel, and their magnetizations are mutually

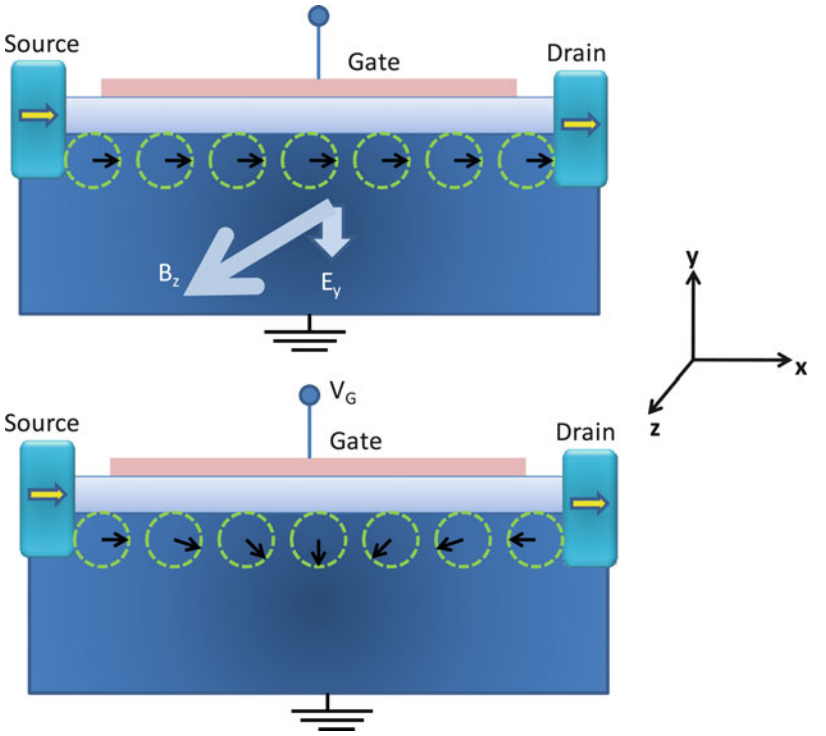

Fig. 1 Structure of the Datta-Das spin field-effect transistor with a one-dimensional channel. The spin orientations of electrons at different regions of the channel are shown within *broken circles* when the gate voltage $V_G = 0$ (*top panel*) and $V_G = V_{th}$ (*bottom panel*). The gate voltage causes an electric field E_y in the y-direction, while the source-to-drain current flows in the x-direction. The electric field induces Rashba spin-orbit interaction in the channel that causes an effective magnetic field in the z-direction whose magnitude depends on the electron's velocity in the x-direction. Precession of electron spin around this magnetic field gives rise to current modulation and transistor action

parallel. One of them (the "source" contact) injects electrons into the channel with spins aligned along the direction of the source's magnetization, which, in this case, is the $+x$-direction. The spin injection efficiency is assumed to be 100 %, so that every injected carrier has its spin aligned in the $+x$-direction. If there is no spin-orbit interaction in the channel and one can neglect the magnetic field caused by the magnetized contacts, then the electron spins do not precess as the electrons travel from the source to the drain under a source-to-drain bias V_{DS}. Now, if there is no spin relaxation in the channel due to magnetic impurities, spin flip events, hyperfine interaction with nuclear spins, etc., then the injected carriers arrive at the "drain" contact with their spins still aligned in the original ($+x$) direction. This is shown in the top panel of Fig. 1. The drain is a spin-selective transmitter since it is also ferromagnetic. Assume that it is a 100 % efficient spin filter which allows only carriers whose spins are aligned parallel to its magnetization (i.e., the $+x$-direction)

to go through and completely blocks carriers whose spins are antiparallel (i.e., pointing in the $-x$-direction). Since the arriving carriers have their spins aligned parallel to the drain's magnetization, the drain transmits all of them and the maximum possible current flows between the source and drain contacts.

When an electrostatic potential V_G is applied between the "gate" terminal and ground, it induces an electric field transverse to the channel (in the y-direction). This electric field induces Rashba spin-orbit interaction in the channel [7] which produces an effective magnetic field that is oriented in a direction mutually perpendicular to the direction of current flow and the gate-induced electric field. Since the channel is strictly one-dimensional, current flows only in the x-direction. Therefore, the effective magnetic field of flux density B_{Rashba} is directed along the z-direction. Because of the one-dimensionality of the channel, the axis of this magnetic field is *fixed* and always points along the z-axis.

The strength of this magnetic field depends on the carrier's velocity, although starting with the Ehrenfest theorem of quantum mechanics one can show that this field is actually proportional to the electron's wavevector instead of the velocity. But in that case, it will be *spin dependent* since an electron of a given energy will have two different wavevectors in the two spin-split bands. If one wishes to define a spin-independent field, it will be necessary to postulate that the field is proportional to the velocity of the electron since that quantity is the same in two spin-split bands for any given energy. One should note that in the presence of spin-orbit interaction, an electron's velocity is not proportional to the wavevector even if the band is parabolic. With this consideration, the field is given by

$$B_{\text{Rashba}}(v) = \frac{2m^* a_{46}}{g\mu_B \hbar} E_y v, \tag{1}$$

where v is the carrier velocity, E_y is the gate-induced electric field causing the Rashba interaction, m^* is the carrier effective mass, a_{46} is a material constant, and e is the electronic charge.

The spins of the injected carriers execute Larmor precession about $\vec{B}_{\text{Rashba}}(v)$ with a frequency Ω given by the Larmor relation:

$$\Omega(v) = \frac{g\mu_B B_{\text{Rashba}}(v)}{\hbar} = \frac{2m^*}{\hbar^2} a_{46} E_y v. \tag{2}$$

This precession takes place on the x-y plane since the axis of the magnetic field is along the z-direction.

At this point, it is necessary to assume that there is no "damping" in the system, meaning that there is no energy dissipation. In other words, inelastic processes are absent. If strong damping is present, then the electron spins must ultimately align along the magnetic field $\vec{B}_{\text{Rashba}}(v)$, so that all spins will be pointing in the z-direction. To prevent this from happening, all energy relaxation processes must be eliminated. That requires the channel length to be much shorter than the inelastic

mean free path of electrons, which may be a few tens of nanometers at best if the device is operated at room temperature. At low temperatures (~4.2 K), the inelastic mean free path can be a few tens of μm.

If no damping is present, then the electron spins will precess continuously about $\vec{B}_{\text{Rashba}}(v)$ since that field is in the z-direction, while the spins are polarized in the x-direction. Therefore, the *spatial* rate at which spin rotates when the electron travels through the SPINFET's channel can be obtained from the Larmor frequency as

$$\begin{aligned} \Omega(v) = \frac{d\phi}{dt} = \frac{d\phi}{dx}\frac{dx}{dt} = \frac{d\phi}{dx}v = \frac{2m^*}{\hbar^2}a_{46}E_y v \\ \Rightarrow \underbrace{\frac{d\phi}{dx}}_{\text{spatial rate}} = \frac{2m^*}{\hbar^2}a_{46}E_y, \end{aligned} \tag{3}$$

where ϕ is the angle through which spin rotates.

Note that the spatial rate $d\phi/dx$ is *independent* of the carrier velocity. Therefore, every electron, regardless of its injection velocity and regardless of any elastic momentum randomizing collision that it suffers in the channel, rotates by exactly the *same* angle as it traverses the distance between the source and drain. This angle is given by

$$\Phi_{\text{Rashba}} = \frac{2m^*}{\hbar^2}a_{46}E_y L, \tag{4}$$

where L is the source-to-drain separation (or the channel length). Thus, if every electron was injected by the source with the same spin polarization, every electron arrives at the drain with identical spin polarization. There is no randomization of spin polarization in the channel, no matter how much momentum randomizing elastic scattering there is, because the spin precession angle is a constant independent of carrier velocity. This is a remarkable result for the strictly one-dimensional SPINFET.

Now, if the electric field E_y is such that $\Phi_{\text{Rashba}} = (2n + 1)\pi$, where n is an integer, then the carriers arriving at the drain have had their spins rotated by an odd multiple of 180°, which means their spin polarization is antiparallel to the original polarization and the drain's magnetization. Therefore, these carriers are blocked by the drain from transmitting and ideally no current flows. On the other hand, if $\Phi_{\text{Rashba}} = 2n\pi$, then the arriving carriers have their spins aligned parallel to the drain's polarization and are fully transmitted. Thus, by changing E_y with a gate potential, one can change Φ_{Rashba} and modulate the source-to-drain current. *This realizes field-effect transistor action.*

Note that this one-dimensional transistor can operate at elevated temperatures, as long as the temperature is not so high as to make the channel length approach the inelastic mean free path. The only effect of higher temperature will be to induce a

thermal spread in the electron velocity and perhaps increase the rate of elastic collisions that change an electron's velocity randomly, but none of this matter. Since Φ_{Rashba} is independent of electron velocity, thermal averaging and increased momentum randomizing elastic collisions have no effect on Φ_{Rashba}. Therefore, raising the temperature does not degrade the performance of the one-dimensional SPINFET, as long as the temperature is not so high as to introduce inelastic collision processes.

Another Spin Field-Effect Transistor

In addition to the Rashba interaction, there can be other types of spin-orbit interaction in a semiconductor channel which can be modulated by an external gate potential. An example is the Dresselhaus spin-orbit interaction [8] which generally exists in any material that lacks crystallographic inversion symmetry. This interaction also results in an effective magnetic field in the channel, just like the Rashba interaction. Assume that the channel of the transistor is in the [9] crystallographic direction and that it is made of a non-zinc-blende semiconductor. It has been claimed that the Dresselhaus interaction vanishes in the [9] crystallographic direction in one-dimensional structures made of zinc-blende semiconductors [10], which is why a non-zinc-blende semiconductor is chosen. In the lowest order approximation, one can neglect weak Dresselhaus contributions. In that case, the effective magnetic field due to the Dresselhaus interaction in the channel of the one-dimensional transistor shown in Fig. 2 will be directed along the x-axis and its strength will be given by

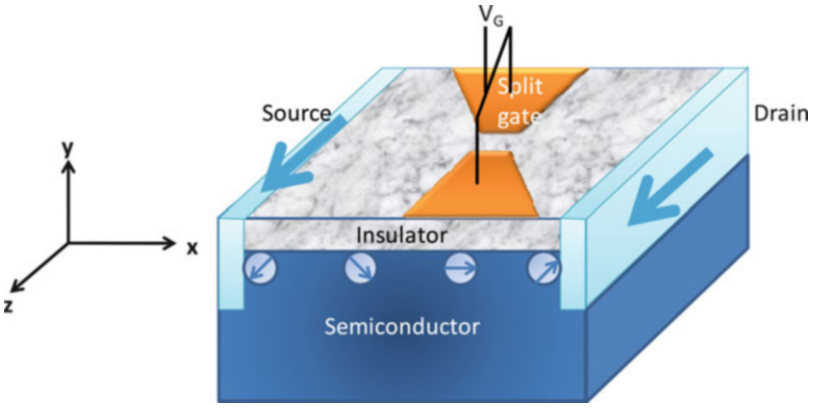

Fig. 2 Structure of the spin field-effect transistor based on the Dresselhaus interaction. The one-dimensional channel is realized with split gates, and its width can be varied with a split gate potential V_G that increasingly constricts the channel as the potential is made more negative. The contacts are magnetized in the +z-direction. The Dresselhaus spin-orbit interaction in the channel gives rise to an effective magnetic field in the x-direction whose magnitude depends on the electron's velocity in the x-direction

$$B_{\text{Dresselhaus}}(v) = \frac{2m^* a_{42}}{g\mu_B \hbar}\left[\left(\frac{\pi}{W_z}\right)^2 - \left(\frac{\pi}{W_y}\right)^2\right] v, \tag{5}$$

where W_z, W_y are the transverse dimensions of the quantum wire channel (assumed to be of rectangular cross section) and a_{42} is another material constant. Fortunately, this effective magnetic field is also proportional to the carrier velocity v.

It is easy to understand that if one injects spins from the source contact that are initially polarized along either the y- or z-axis (this will require magnetizing the source and drain contacts along the y- or z-axis), then these spins will precess about the x-directed effective magnetic field due to the Dresselhaus interaction. The precession takes place in the y-z plane. The angle by which the spin precesses in traveling between the source and drain will be given by (compare with Eq. 4)

$$\Phi_{\text{Dresselhaus}} = \frac{2m^* a_{42}}{\hbar^2}\left[\left(\frac{\pi}{W_z}\right)^2 - \left(\frac{\pi}{W_y}\right)^2\right] L. \tag{6}$$

This angle too is independent of the carrier velocity. One can change $\Phi_{\text{Dresselhaus}}$ by varying the width of the one-dimensional channel W_z with a split gate potential V_G. That will also realize transistor action since changing $\Phi_{\text{Dresselhaus}}$ will modulate the source-to-drain current [11]. This device has all the advantages of the original Datta-Das SPINFET, namely, that since $\Phi_{\text{Dresselhaus}}$ is independent of carrier velocity, thermal averaging and elastic momentum-relaxing scattering have no deleterious effect. Accordingly, this transistor is also able to operate at elevated temperatures, without any serious degradation in performance, as long as the temperature is not so high as to induce inelastic collisions in the channel.

Nonidealities

If both Rashba and Dresselhaus interactions are present in the channel of a Datta-Das SPINFET or the SPINFET based on the Dresselhaus interaction, then the total effective magnetic field experienced by an electron in the channel due to spin-orbit interaction is the vector sum of the individual fields:

$$\mathbf{B}_{SO} = B_{\text{Dresselhaus}}\hat{\mathbf{x}} + B_{\text{Rashba}}\hat{\mathbf{z}}, \tag{7}$$

where $\hat{\mathbf{x}}$ and $\hat{\mathbf{z}}$ are the unit vectors along the x- and z-axes. This resultant field lies in the x-z plane and subtends an angle θ with the x-axis (channel axis or direction of current flow in the channel) given by

$$\tan\theta = \frac{B_{\text{Rashba}}}{B_{\text{Dresselhaus}}} = \frac{a_{46}}{a_{42}} \frac{E_y}{\left[\left(\frac{\pi}{W_z}\right)^2 - \left(\frac{\pi}{W_y}\right)^2\right]}. \tag{8}$$

Note that this angle is also independent of carrier velocity. Hence the axis of the effective magnetic field $\mathbf{B}_{SO}$ is again the *same* for every electron, at any fixed values of E_y, W_z, and W_y. If one injects spins with polarization normal to this axis, they will all precess about this axis (on a plane normal to this axis) as they travel from the source to the drain. The precession angle will be given by (compare with Eqs. 4 and 6)

$$\Phi_{\text{total}} = \frac{2m^*L}{\hbar^2}\sqrt{\left(a_{46}E_y\right)^2 + a_{42}^2\left(\left[\frac{\pi}{W_z}\right]^2 - \left[\frac{\pi}{W_y}\right]^2\right)^2}. \tag{9}$$

One can change Φ_{total} by changing E_y with a gate potential, but doing that also changes the angle θ (see Eq. 8) and therefore the axis of the effective magnetic field will change. Thus, the precession plane will change if one changes the gate voltage, unlike in the previous two cases. This is a complicated effect. The reader will understand that if the source and drain contacts are magnetized in the same direction, which is *fixed*, then the current is never completely blocked at any gate voltage and a large leakage current will flow through the transistor during the off state. Therefore, the simultaneous presence of both Rashba and Dresselhaus interactions is not desirable.

There is an additional problem. The ferromagnetic contacts will induce a real magnetic field $\mathbf{B}_{\text{real}}$ in the channel, whether or not it is a fringing field or a direct field. This field is *not* proportional to the carrier velocity (it is a constant) and therefore the angle by which a spin precesses about it, as the carrier travels a fixed distance L from the source to the drain, will depend on the carrier velocity v. This angle will be $g\mu_B|\mathbf{B}|_{\text{real}}vL/\hbar$. In that case, different electrons with different velocities due to scattering and the finite spread in electron energy will precess by different angles in traversing the transistor's channel. Consequently, ensemble averaging over all the electrons will reduce the current modulation significantly. In other words, both the on-to-off-conductance ratio and the transconductance of the transistor will decrease. The magnetic field can also increase spin flip scattering rate in the presence of spin-orbit interaction, which is an additional problem since it randomizes spin polarization. All these damaging effects have been discussed in Ref. [12].

Other Types of SPINFET

A number of other SPINFETs, inspired by the Datta-Das construct, have been proposed over time. One of them – the so-called non-ballistic SPINFET – works on the following principle:

Consider a two-dimensional semiconductor channel in the x-z plane as in Fig. 1 or 2. The quantum mechanical Hamiltonian describing an electron in this system is

$$H = \frac{p_x^2 + p_y^2 + p_z^2}{2m^*} + V(y) - \frac{\eta}{\hbar}[p_x\sigma_z - p_z\sigma_x] - \frac{\nu}{\hbar}[p_x\sigma_x - p_z\sigma_z], \tag{10}$$

where η and ν are the strengths of the Rashba and Dresselhaus interactions, respectively. In terms of material constants, $\eta = a_{46}|\mathbf{E}|; \nu = -\frac{a_{42}}{\hbar^2}\left\langle p_y^2 \right\rangle = a_{42}\left\langle \frac{\partial^2}{\partial y^2} \right\rangle$, where $\mathbf{E}$ is the electric field inducing the Rashba interaction and $\langle p_y^2 \rangle / 2m^*$ is the expectation value of the kinetic energy associated with motion in the direction of confinement. This quantity will be different in different subbands and will depend on the shape of the confining potential (e.g., in a rectangular well with infinite barriers, $\langle p_y^2 \rangle = (n\pi\hbar/W)^2$ in the n-th subband where W is the width of the well and m^* is the electron's effective mass). The σ-s are the Pauli spin matrices and $V(y)$ is the confining potential in the y-direction.

Since the Hamiltonian is invariant in the coordinates x and y, the wavevectors k_x and k_y are good quantum numbers, and one can write the spatial (or orbital) part of the wavefunction as

$$\psi(x, y, z) = e^{ik_x x} e^{ik_z z} \lambda_n(y). \tag{11}$$

Using this wavefunction, the spatial average of the Hamiltonian is calculated as

$$\langle H \rangle = \varepsilon_n + \frac{\hbar^2}{2m^*}\left(k_x^2 + k_z^2\right) - \eta[k_x\sigma_z - k_z\sigma_x] - \nu[k_x\sigma_x - k_z\sigma_z], \tag{12}$$

where ε_n are the subband energy levels in the quasi two-dimensional electron gas formed in the x-z plane.

Writing this Hamiltonian explicitly by replacing the Pauli spin matrices, one gets

$$\begin{aligned} \langle H \rangle &= \varepsilon_n + \frac{\hbar^2}{2m^*}\left(k_x^2 + k_z^2\right) - \eta\begin{bmatrix} k_x & 0 \\ 0 & -k_x \end{bmatrix} + \eta\begin{bmatrix} 0 & k_z \\ k_z & 0 \end{bmatrix} - \nu\begin{bmatrix} 0 & k_x \\ k_x & 0 \end{bmatrix} + \nu\begin{bmatrix} k_z & 0 \\ 0 & -k_z \end{bmatrix} \\ &= \begin{bmatrix} E_n - \eta k_x + \nu k_z & \eta k_z - \nu k_x \\ \eta k_z - \nu k_x & E_n + \eta k_x - \nu k_z \end{bmatrix}, \end{aligned} \tag{13}$$

where $E_n = \varepsilon_n + \frac{\hbar^2}{2m^*}\left(k_x^2 + k_z^2\right)$.

Diagonalization of this Hamiltonian yields the dispersion relations of the two spin-split branches of any subband and the corresponding eigenspinors. The former are

$$E_{\pm}(n, k_x, k_y) = E_n \pm \sqrt{(\eta k_x - \nu k_z)^2 + (\nu k_x - \eta k_z)^2}, \tag{14}$$

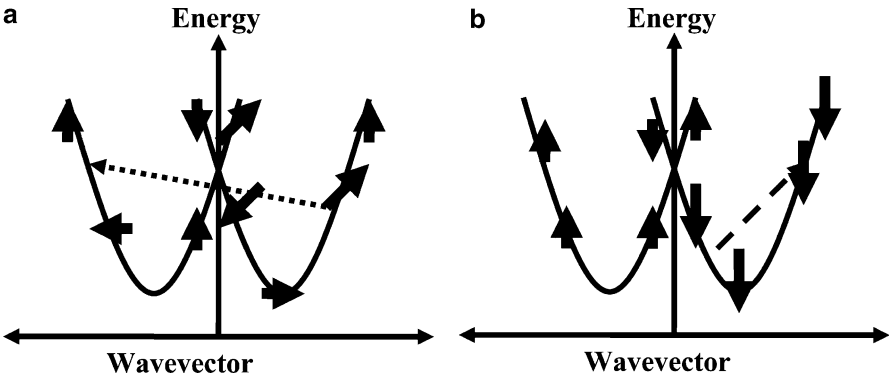

Fig. 3 Energy dispersion relations of any spin-split subband showing the spin orientations at various wavevector states: (**a**) when $\eta \neq \nu$ and (**b**) when $\eta = \nu$. The *broken arrows* show momentum-relaxing scattering events

while the latter are

$$\begin{aligned} \varphi_+(k_x, k_y) &= \begin{bmatrix} -\sin(\phi_k) \\ \cos(\phi_k) \end{bmatrix} \\ \varphi_-(k_x, k_y) &= \begin{bmatrix} \cos(\phi_k) \\ \sin(\phi_k) \end{bmatrix}, \end{aligned} \tag{15}$$

where

$$\phi_k = \frac{1}{2}\arctan\left[\frac{-\eta k_z + \nu k_x}{\eta k_x - \nu k_z}\right]. \tag{16}$$

Note that if $\eta \neq \nu$, then the angle ϕ_k is wavevector dependent which makes the eigenspinors in Eq. 15 wavevector or velocity dependent. Therefore, neither spin-split branch has a fixed spin quantization axis. The spin orientation of an electron in either branch depends on its wavevector or velocity. This situation is depicted in Fig. 3a. Note that since the electron's spin will orient in the direction of the effective magnetic field $\mathbf{B}_{SO}$ (for a positive g-factor), clearly the direction of $\mathbf{B}_{SO}$ is velocity or wavevector dependent in either branch.

But now consider the special case when $\eta = \nu$. In this case, $\phi_k = \pi/8$, so that the eigenspinors become wavevector independent. In that case, each branch has a fixed (wavevector independent) spin quantization axis. However, these axes will be mutually antiparallel in the two branches since the eigenspinors are orthogonal. This situation is shown in Fig. 3b. Once again, since the spins will have oriented along $\mathbf{B}_{SO}$, it can be concluded that the direction of $\mathbf{B}_{SO}$ is fixed in either branch, albeit mutually antiparallel in the two branches.

When $\eta \neq \nu$, and the eigenspinor in either spin-split branch changes with wavevector, it is always possible to find two states in the two branches at different

wavevectors whose eigenspinors are not orthogonal, meaning that the spin orientations in these two states are not exactly antiparallel. A nonmagnetic impurity or phonon can then induce a scattering between these two states because the matrix element for such scattering will be nonzero. However, such a scattering event will change the electron's spin polarization since the spin orientations of the initial and final states are. Therefore, any interbranch scattering caused by a nonmagnetic impurity or phonon will relax spin. In fact, even an intra-branch scattering event will relax spin since the spin orientation changes with wavevector within the same branch as well. Note that since the wavevector also changes in such scatterings, spin relaxation is accompanied by momentum relaxation and vice versa. This is essentially the Elliott-Yafet mechanism of spin relaxation [13, 14]. However, when $\eta = \nu$, the eigenspinors in the two branches are perfectly orthogonal *at every wavevector*. Consequently, it is impossible to have any interbranch scattering via phonons or nonmagnetic impurities since the matrix element for such a transition is exactly zero. It is of course possible to have intra-branch transition since the initial and final states have parallel spins (which makes the matrix element nonzero), but such a transition does not relax spin at all because the spin orientations of the initial and final state are parallel. Therefore, phonons and nonmagnetic impurities cannot relax spin in the special situation when $\eta = \nu$. In other words, the Elliott-Yafet mechanism becomes inoperative when $\eta = \nu$.

Next, recall that the effective magnetic field due to spin-orbit interaction $\mathbf{B}_{SO}$ has a constant direction, independent of wavevector or velocity, in either branch when $\eta = \nu$. Therefore, there can be no D'yakonov-Perel' relaxation in this case since the latter is caused by change in the direction of $\mathbf{B}_{SO}$ when an electron's velocity changes due to momentum-relaxing scattering [15, 16]. If the direction of $\mathbf{B}_{SO}$ is independent of velocity, then no amount of change in the velocity due to scattering will change the direction of $\mathbf{B}_{SO}$ and cause D'yakonov-Perel' spin relaxation. In the end, if $\eta = \nu$, then the two major spin-relaxation mechanisms in the channel of a SPINFET, namely, Elliott-Yafet and D'yakonov-Perel', are eliminated. The only remaining spin-relaxation mechanisms are those due to magnetic impurities, the Bir-Aronov-Pikus mechanism [17] and hyperfine interaction with nuclear spins. These mechanisms are usually very weak.

It is now possible to describe the operation of the "non-ballistic SPINFET," but before doing that, it should be pointed out that when $\eta = \nu$, the eigenspinors [from Eqs. 15 and 16] are

$$\varphi_+ = \begin{bmatrix} -\sin(\pi/8) \\ \cos(\pi/8) \end{bmatrix}$$

$$\varphi_- = \begin{bmatrix} \cos(\pi/8) \\ \sin(\pi/8) \end{bmatrix}.$$

Therefore, the components of an electron's spin along the x-, y-, and z-axis in either spin-split branch is given by

$$S_x = [\varphi_\pm][\sigma_x][\varphi_\pm] = \pm \sin(\pi/4) = \pm\frac{1}{\sqrt{2}}$$
$$S_y = [\varphi_\pm][\sigma_y][\varphi_\pm] = 0$$
$$S_z = [\varphi_\pm][\sigma_x][\varphi_\pm] = \pm \cos(\pi/4) = \pm\frac{1}{\sqrt{2}},$$

which means that when the electron is in an eigenstate, its spin polarization vector lies in the x-z plane and subtends an angle of 45° with the x- or z-axis.

The so-called non-ballistic SPINFET proposed by two groups independently [18, 19] works as follows. The device has exactly the same structure as the one in Fig. 1, except that the source and drain contacts are magnetized (parallel to each other) in the x-z plane in a direction that subtends an angle of 45° with the x- or z-axis. The gate voltage is tuned to make $\eta = \nu$ and the source injects spins into the channel in an eigenstate. The Dresselhaus interaction strength ν is independent of the gate voltage, but the Rashba interaction strength η depends on it since $\eta = a_{46}E_y$. Next, it is assumed that the spin injection efficiency is 100 %, so that *every* spin, without exception, is injected in the same eigenstate. The injected electrons do not relax spin via the Elliott-Yafet and D'yakonov-Perel' mechanisms as explained before and therefore arrive at the drain with their spins aligned along the drain's magnetization. These electrons are all transmitted by the drain and the current is a maximum. This is the "on" state of the transistor.

To turn the device off, the gate voltage is detuned to make $\eta \neq \nu$. Then, Elliott-Yafet and D'yakonov-Perel' mechanisms become operative and relax spin. As a result, many of the electrons reaching the drain will have their spins flipped. They will be blocked by the drain (assuming that the drain is a 100 % efficient spin filter) and the current will drop. This is interpreted as the "off" state.

A little bit of reflection will convince the reader that the maximum ratio of the on-to-off-conductance is only 2:1. That is because, when spins are flipped randomly in the channel, what can happen at best is that 50 % of the spins arriving at the drain will have their spins antiparallel to the drain's magnetization (blocked), while the remaining 50 % will have their spins parallel (transmitted). After all, the spin polarization of the current cannot be less than zero. Thus, the off-current is no less than 50 % of the on-current, so that the maximum conductance ratio is 2. An actual simulation carried out by Shafir et al. [20] found that the conductance ratio in realistic scenarios is not even 2:1, but only ~1.2:1. Transistors require a conductance modulation of about 10^5:1 for mainstream applications. Therefore, this "transistor" is not suitable for any such application.

One can obviously improve the conductance ratio by making a minor simple change to the design. Let us consider the situation when the magnetizations of the source and drain are *antiparallel*. One possible way to make them effectively antiparallel is to magnetize them in the same direction but ensure that the signs of spin polarizations of carriers at the Fermi energy are opposite in the two contacts. One can implement this by choosing two different materials such as iron and nickel for the two contacts [21]. In that case, when $\eta = \nu$, the drain blocks every electron and the current is ideally zero. When the gate voltage is changed to make $\eta \neq \nu$,

spins flip and the drain now transmits the flipped spins. Then, the transmitted current will be nonzero. With the antiparallel arrangement, the conductance ratio I_{on}/I_{off} is *ideally* infinite, which would have been excellent, but in reality it is far from that. The real ratio is quite small since it is impossible to inject or filter spins with 100 % efficiency. This is shown below.

If the source injects both majority spins and minority spins, then the former will be blocked by the drain when $\eta = \nu$ (if the drain is an ideal spin filter), but the latter will still transmit. Thus, the off-current will be *nonzero* due to the minority spins. Furthermore, if the drain is nonideal as well and transmits both its own majority and minority spins, then that too will make the off-current nonzero. If the spin injection efficiency at the source is ξ_S and the spin-filtering efficiency of the drain is ξ_D, then the ratio of on-current to off-current will be

$$\frac{I_{on}}{I_{off}} = \frac{1}{1 - \xi_S \xi_D}. \tag{17}$$

The spin injection efficiency is defined as $\xi_s = \frac{I_{maj} - I_{min}}{I_{maj} + I_{min}}$, where I_{maj} is the current due to majority spins in the injecting contact and I_{min} is the current due to minority spins in the injecting contact. Similarly, the spin detection efficiency is $\xi_D = \frac{i_{maj} - i_{min}}{i_{maj} + i_{min}}$ where i_{maj} is the current due to majority spins in the detecting contact and i_{min} is the current due to minority spins in the detecting contact.

In order to make this ratio 10^5, which is typical of modern transistors, the spin injection and filtering efficiencies have to be 99.9995 %!

It is unlikely that one can achieve spin injection efficiency this high at room temperature. Not only is this impossible in the near term, it may be *forever* impossible, since there are fundamental barriers to ~100 % spin injection efficiency, particularly at room temperature.

There are two known routes to achieving high spin injection efficiency: (1) using highly spin-polarized half metals as the ferromagnetic spin injector and detector and (2) using spin-selective barriers that inject and detect spins of a particular polarization only [22, 23]. Unfortunately, there can be *no* half metals with 100 % spin polarization at any temperature above absolute zero. Dowben and Skomski [24] has shown that all half metals lose their high degree of spin polarization at temperature $T > 0$ K because of magnons and phonons. Even at $T = 0$ K, there are no ideal half metals with 100 % spin polarization because of surfaces and inhomogeneities [24]. Therefore, half metals will not achieve ~100 % spin injection efficiency, even at 0 K, let alone room temperature. Consequently, half metals are not a viable route.

Spin-selective barriers can at best transmit one kind of spin at one specific injection energy. The best spin-selective barriers use resonant tunneling [22]. At 0 K, the transmission energy bandwidth can approach zero, so that nearly 100 % spin injection efficiency is possible in principle, but at any nonzero temperature, thermal broadening of the carrier energy will ensure that the spin injection efficiency is far less than 100 %. Therefore, this route will not work either at room temperature.

The highest spin injection efficiency for spin injection from a metallic ferromagnet into a semiconductor through a tunneling barrier, demonstrated at or near room temperature, is only about 70 % [25]. and at very low temperatures, a spin injection efficiency of ~90 % has been shown to be possible [26]. If these two values for ξ are used in Eq. 17, then the maximum on-to-off ratio of the conductance are only 2 and 5, which are still a far cry from the 10^5 required. Therefore, these spin transistors may be theoretical curiosities, but are not viable as "transistors."

The reader will understand that the same problem afflicts the device of Ref. [1]. In fact, this is a generic problem that afflicts *all* spin field-effect transistors that require spin injection and detection.

Neither Ref. [1] nor Refs. [18, 19] ever made the claim that their device is competitive with the silicon MOSFET which is the workhorse of electronics. The authors of Ref. [1], in particular, carefully avoided calling their device a "transistor." However, claims were made by a group [27] that their SPINFET will be superior to a MOSFET. This group has proposed a device whose structure is very similar (almost identical) to that of the device of Refs. [18, 19] with the sole difference being that the source and drain contacts are magnetized in the antiparallel configuration, rather than the parallel configuration. The way this device works is as follows. The source injects electrons with spins polarized parallel to the source's magnetization. When the gate voltage is zero, the spin-orbit interaction in the channel is small or nonexistent so that both Elliott-Yafet and D'yakonov-Perel' relaxations are suppressed and the injected spins do not flip much. The drain therefore blocks most or all injected electrons from transmitting and the current is zero or at least low. This is the "off" state. When the gate voltage is turned up, the spin-orbit interaction in the channel increases dramatically, and the spins flip much more frequently. When electrons with flipped spins arrive at the drain, they are transmitted and the current rises. This is the mode of switching the transistor from the "off" to the "on" state with the gate voltage.

It should be obvious to the reader that the maximum conductance ratio of this device is given by Eq. 17 since this device suffers from the same malady as all SPINFETs, namely, that spin injection and filtering efficiencies have to be very high for the device to work with adequate conductance on-off ratio. If one generously assumes a spin injection efficiency of even 90 % at room temperature, then the maximum conductance ratio of this device is only 5:1, which immediately makes it noncompetitive with the silicon MOSFET by a long shot because the latter has on/off ratios exceeding 10^6:1 [28, 29]. Additionally, it is not clear at all that a reasonable gate voltage can increase spin-orbit interaction in the channel by a lot, which is the basic operating principle of this device. Nitta et al. [30] studied the dependence of Rashba spin-orbit interaction on gate voltage in a transistor channel and found a weak dependence. Kwon et al. [31] experimentally measured the dependence of spin-relaxation length on gate voltage and found that an increase of gate voltage by 3 V decreases the spin-relaxation length by a mere 2.5 %. In view of that, the claim in Ref. [27] that only ~100 mV of gate voltage can turn the transistor fully on and provide a large on/off ratio of the conductance seems to be overly optimistic, if not far-fetched. It is believed that even if the spin injection and

spin detection efficiencies could miraculously reach 100 %, the on/off ratio will still be very small, possibly much less than 10:1, despite the claim in Ref. [27] that it will be ~10^5:1.

Two-Dimensional Datta-Das SPINFET

The analysis of the Datta-Das SPINFET that was presented in section titled Datta-Das Transistor assumed a one-dimensional channel. For such a device, the source-to-drain current at any given gate voltage V_G will be given by [32]

$$I_{SD}^{1-D} = \frac{I_0}{2}[1 + \xi_s \xi_D \cos \Phi_{\text{Rashba}}(V_G)], \tag{18}$$

where I_0 is the maximum current that flows through the transistor when it is on and $\Phi_{\text{Rashba}}(V_{GS})$ is the gate-voltage-dependent spin precession angle. Since the transistor is on when $\Phi_{\text{Rashba}}(V_{GS}) = 0$ and it is off when $\Phi_{\text{Rashba}}(V_{GS}) = \pi$, the maximum ratio of on- to off-current for the one-dimensional Datta-Das SPINFET is

$$\left.\frac{I_{\text{on}}}{I_{\text{off}}}\right|_{1-\text{D Datta}-\text{Das}} = \frac{1 + \xi_S \xi_D}{1 - \xi_S \xi_D}. \tag{19}$$

The source-to-drain current in a two-dimensional Datta-Das SPINFET however does not obey Eq. 18. The expression for a two-dimensional channel has been derived in a number of publications [33–35] and (for 100 % spin injection and detection efficiencies) is given by

$$\begin{aligned} I_{SD}^{2-D} &= \frac{e^2 W_z}{\pi h} \int_0^{k_F} dk_z \left[\cos^2\Theta(k_z, k_F, V_{GS}) + \frac{k_z^2}{k_F^2} \sin^2\Theta(k_z, k_F, V_{GS}) \right] V_{SD} \\ &= \frac{e^2 W_z}{\pi h} \int_0^{k_F} dk_z \left[\frac{k_z^2}{k_F^2} + \left(1 - \frac{k_z^2}{k_F^2}\right) \cos^2\Theta(k_z, k_F, V_{GS}) \right] V_{SD}, \end{aligned} \tag{20}$$

where k_z is the wavevector in the direction transverse to current flow in the two-dimensional channel, W_z is the width of the channel, k_F is the Fermi wavevector, and

$$\Theta(k_z, k_F, V_{GS}) = \frac{\left(2m^* E_y[V_{GS}]/\hbar^2\right) k_F - (m^*)^2 E_y^2[V_{GS}]/\hbar^4}{\sqrt{k_F^2 - k_z^2}} L. \tag{21}$$

Equation 20 is valid only at low temperatures and under small applied source-to-drain bias. Clearly in this case the ratio of on- to off-current is much less than infinity even if the spin injection and detection efficiencies at the source and drain contact were 100 %. This is because the minimum current or off-current is

$$I_{\text{off}}^{2-D} = \frac{e^2 W_z}{\pi h} \int_0^{k_F} dk_z \frac{k_z^2}{k_F^2} V_{SD} = \frac{e^2 W_z k_F}{3\pi h} V_{SD} \neq 0, \tag{22}$$

while the maximum current or on-current is

$$I_{\text{on}}^{2-D} = \frac{e^2 W_z}{\pi h} \int_0^{k_F} dk_z V_{SD} = \frac{e^2 W_z k_F}{\pi h} V_{SD}. \tag{23}$$

Therefore, the best possible conductance on-off ratio is 3:1. Scattering and other nonidealities will make it worse than 3:1. This is the reason why the Datta-Das SPINFET has been so elusive to experimentalists who typically employ two-dimensional structures.

Experimental Status

The ability to modulate Rashba spin-orbit interaction strength in the channel of an FET-like structure was demonstrated long ago [30], but an experimental demonstration of current modulation in a SPINFET due to gate-induced modulation of the spin-orbit interaction strength has remained elusive even two decades after the first proposal of the Datta-Das SPINFET. There has been a recent claim in the literature that a two-dimensional SPINFET structure has exhibited the conductance modulation expected from a Datta-Das SPINFET due to gate voltage change [36], but unfortunately the authors of this claim used the wrong one-dimensional formula (Eq. 18) to match their experimental data with theory, even though their device structure was two-dimensional. This makes their claim dubious, although it is possible that in the regime where this device operated, the actual difference between the predictions of the correct two-dimensional formula (Eq. 20) and the incorrect one-dimensional formula (Eq. 18) may not be perceptible [35]. Calculations have shown that the predictions of the correct two-dimensional formula disagree with the experimental data by about ~15 %, but more importantly the experimental data had only one and one-half periods of conductance modulation which is not enough to draw any definitive conclusion either way. In a two-dimensional channel, scattering plays a major role since it can randomize the spin precession angle $\Theta(k_z, k_F, V_{GS})$ [because the transverse wavevector k_z is randomized by momentum relaxation events]. This is a major difference between a one- and a two-dimensional channel. Therefore, inclusion of scattering can further complicate matters, and a claim has been made [37] that scattering can make the correct two-dimensional formula agree with the experimental data of Ref. [36]. This is however never a convincing argument since the details of scattering in a particular structure cannot be known with certainty.

The more important issue to understand is that the two-dimensional channel has inherently poor on/off ratio because of ensemble averaging over the transverse

wavevector represented by the integral over k_z in Eq. 20. Only one-dimensional SPINFETs are immune to the deleterious effect of ensemble averaging, but they are unfortunately unable to carry much current since the maximum conductance of a one-dimensional channel will be e^2/h. Thus, it is impossible to attain both high current levels (for large fan-out) and large on/off ratios with SPINFETs. This is a major shortcoming and seems to be insurmountable.

Obstacles to Experimental Demonstration

There are serious obstacles to demonstrating the Datta-Das SPINFET and its various clones, primary among which is the inability to inject and detect spins with high enough efficiencies at the source/channel and drain/channel interfaces. In Fig. 4, the on/off ratio of the current (or conductance) of the one-dimensional Datta-Das SPINFET is plotted as a function of the spin injection or detection efficiency [32].

Clearly, even when the spin injection and detection efficiency is as large as 90 %, the conductance on/off ratio is a mere 10:1. This makes the conductance modulation of the transistor very weak and probably undetectable in a noisy environment. The second obstacle to experimental realization is the weak spin-orbit interaction in the conduction band of semiconductors which makes it difficult to precess the spin

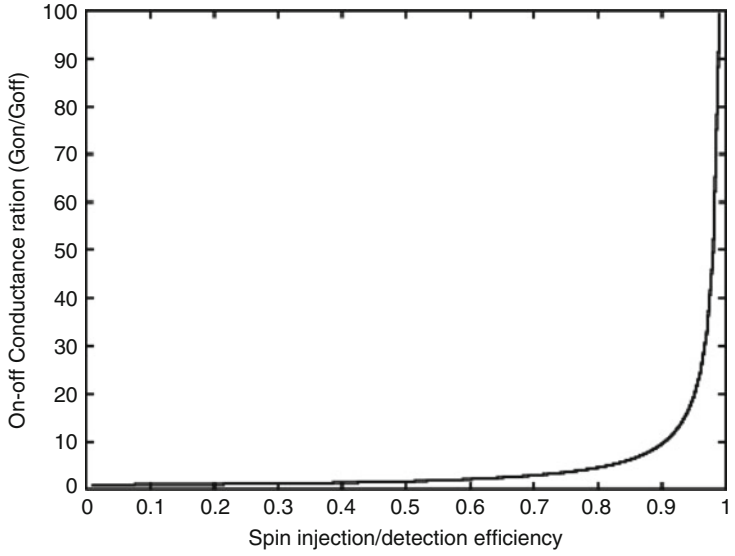

Fig. 4 The conductance on/off ratio of the one-dimensional Datta-Das SPINFET as a function of spin injection or detection efficiency (assuming the two are equal). Everything else is assumed to be ideal (Reproduced from [32] ("Switching voltage, dynamic power dissipation and on-to-off conductance ration of a spin field effect transistor") with permission from Institute of Engineering and Technology)

by 180° with a reasonable gate voltage. Spin-orbit interaction can be stronger in the valence band of some semiconductors [38, 39], but spin precession of holes is a more complicated business because of the presence of two different types of holes (heavy and light) and possible mixing between them. Therefore, it is not clear whether a p-channel SPINFET is any easier to demonstrate than an n-channel SPINFET. The third obstacle is the inevitable magnetic field in the channel caused by the ferromagnetic source and drain contacts. Since these are two ferromagnets facing each other, they will invariably generate a magnetic field in the channel. This field, like the Rashba field, also causes Larmor spin precession and the spatial rate of precession due to it is *not* velocity independent unlike that due to the Rashba field (see Eq. 3). As a result, electrons with different velocities in the channel undergo different additional spin precessions, and ensemble averaging over these electrons will dilute the conductance modulation. Finally, there is also the possibility of Ramsauer resonances occurring in the channel of the SPINFET which may cause current oscillation [11]. Under some circumstances, these oscillations may be mistaken for current modulation due to the Rashba effect [11] and therefore complicate matters. The channel magnetic field also causes a leakage current [37]. As a result, the experimental demonstration of the Datta-Das SPINFET (or any other related device) is very challenging and eluded the most committed efforts.

The other types of SPINFET that have been discussed are even harder to demonstrate. The device in Ref. [10] avoids a channel magnetic field, but employs the Dresselhaus interaction which is typically weaker than the Rashba interaction in technologically important semiconductors. It also requires a more complicated structure that is more vulnerable to fabrication defects. Therefore, it is harder to implement. The devices of Refs. [18, 19], on the other hand, require a very delicate balance between the Rashba and the Dresselhaus interactions, which is difficult to achieve given the numerous imperfections in fabrication. Therefore, these devices have remained theoretical curiosities and eluded experimental realization.

Are SPINFETs Energy Efficient?

Research in SPINFETs, or for that matter any nontraditional transistor, is motivated by a desire to overcome the fundamental speed and power limitations of MOSFETs. The MOSFET is switched from the "on" state to the "off" state (or vice versa) by moving charge carriers into and out of the channel with a gate voltage. This physical motion of charges causes excessive energy dissipation. There is no way to eliminate this dissipation, as was explained in the Introduction section. The high levels of dissipation have serious physical consequences. Currently, the amount of energy dissipated to switch an isolated nanoscale MOSFET is about 50,000 kT at room temperature and in a circuit, that dissipation goes up to roughly 10^6 kT because of additional capacitances and drive overheads. With current 22-nm node technology, the device density on a chip is approaching 10^{10} cm^{-2} and if the energy

dissipation per switching event remains the same, then at a clock rate of 2 GHz, the power dissipation per unit area will be 8.4 kW/cm^2 if roughly 10 % of the transistors are switching every clock cycle. This is just about enough to overwhelm current heat sinking technology. Further downscaling of transistors and increasing their density on a chip seems to be impossible in this scenario unless the energy dissipation per switching event can be reduced. Without that, Moore's law [41] that envisions doubling of the device density on a chip every 18 months is seriously threatened. A consensus seems to be emerging that charge-based devices are fundamentally energy inefficient and will not be able to extend Moore's law beyond the year 2020, which is why alternate state variables, such as electron spin, are being increasingly examined.

At first look, it appears that the SPINFET is a promising candidate since it is switched without changing the carrier concentration in the channel. Therefore, it might appear that no current needs to flow to switch the transistor, thus eliminating the $I^2R\Delta t$ loss. Unfortunately, this is *not* true since switching is still accomplished with a gate voltage and some current flow is needed to charge up the gate (a capacitor) to the required voltage. The energy dissipated to charge up the gate to a voltage V_G is still $(1/2)CV_G^2$ if the gate is charged abruptly or non-adiabatically (it can be shown that if the voltage V_G on the gate is turned on abruptly or non-adiabatically, then the energy dissipated $I^2R\Delta t$ is exactly equal to $(1/2)CV_G^2$ where C is the gate capacitance [37]). Thus, in terms of gate dissipation, the SPINFET is no different from the MOSFET where the gate dissipation is again the same $(1/2)CV_G^2$. It does not matter what the gate voltage does – whether it changes the carrier concentration or the spin polarization of the carriers. The energy dissipated to charge the gate non-adiabatically is always $(1/2)CV_G^2$ regardless of the role of the gate voltage. Therefore, the SPINFET provides no special advantage. If any advantage were to accrue, it would be solely due to the fact that the gate voltage required to switch a SPINFET is smaller than that required to switch a MOSFET.

Bandyopadhyay et al. [10] examined whether the gate voltage needed to switch a SPINFET is indeed less than that required to switch a MOSFET. For nanoscale transistors, the answer turned out to be *negative*. In fact, the SPINFET normally will require a much larger gate voltage than a comparable MOSFET and hence is *less* energy efficient, as long as the channel length is shorter than ~1 μm. The problem is that the gate voltage in a spin transistor changes the spin polarization of carriers by affecting *spin-orbit interaction* – be it the Rashba or the Dresselhaus spin-orbit interaction. The gate voltage dependence of spin-orbit interaction in the conduction band of most semiconductors is very weak, so that a very large gate voltage will be required to induce sufficient change in the spin polarization to turn a SPINFET from "on" to "off," or vice versa. The ratio of the gate voltages required to switch the SPINFET of Ref. [1] and to switch a comparable MOSFET was shown to be [10]

$$\frac{V_G^{\text{SPINFET}}}{V_G^{\text{MOSFET}}} \approx \frac{\hbar^2 \pi e}{2m^* \gamma E_F L}, \tag{24}$$

where E_F is the Fermi energy in the channel, m^* is the electron effective mass in the channel, L is the channel length and γ is the rate of change of spin-orbit interaction strength with gate voltage ($\gamma = \partial\eta/\partial V_G$, where V_G is the gate voltage).

For realistic values of E_F and γ, the above ratio was shown to be smaller than unity only if the channel length of the transistor is several micrometers long [10]. Thus, no sub-micron SPINFET, of the type in Ref. [1], has any advantage over a comparable MOSFET in terms of power dissipation or energy efficiency, since the power dissipated to turn the transistor on or off is proportional to the square of the gate voltage required to switch the transistor.

The same conclusion holds for the SPINFET of Ref. [27]. The gate voltage required to modulate the conductance of this structure between the maximum and minimum values is likely to exceed that of MOSFETs by a large margin since a large amount of voltage is required to change the spin-relaxation length in a channel. This will make such a transistor much less energy efficient than a MOSFET.

In the end, traditional SPINFETs do *not* produce any advantage over traditional MOSFETs in terms of energy efficiency, which begs the question why should there be so much interest in SPINFETs. Part of it is certainly due to the novelty of the concept and the allure of anything nontraditional. However SPINFETs may have some unique features that do set them apart and make them desirable for certain niche applications.

Unusual Features of SPINFETs

The transfer characteristic of a Datta-Das SPINFET is non-monotonic and *oscillatory* as shown in Fig. 5. Now, if the ac gate voltage happens to be a sinusoid with amplitude V_a and the period of the oscillation in the transfer characteristic is V_p, then for every period of the gate voltage swing, the source-to-drain current oscillates by V_a/V_p periods. Hence if the frequency of the sinusoidal gate voltage is f, then the frequency of the source-to-drain current will be $(V_a/V_p)f$. In other words,

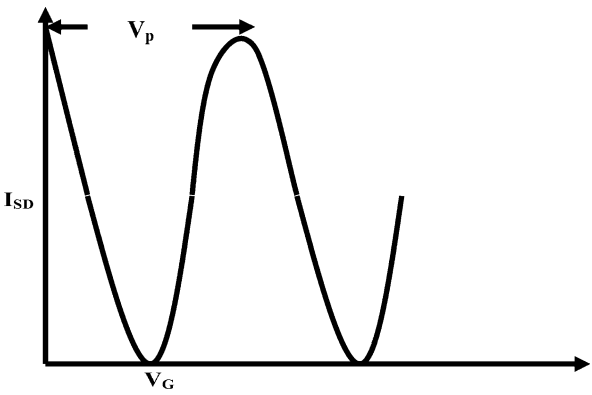

Fig. 5 The transfer characteristic (drain current vs. gate voltage) of an ideal Datta-Das SPINFET with a one-dimensional channel, no spin relaxation in the channel, no magnetic field in the channel, and 100 % spin injection/detection efficiencies

the device can act like a frequency multiplier with a multiplication ratio of V_a/V_p. This is made possible by the oscillatory nature of the transfer characteristic. Thus, one can implement a *single-transistor-frequency-multiplier* with a SPINFET, which is not possible with traditional MOSFETs. However, this is not unique to SPINFETS; any device whose transfer characteristic is oscillatory (quantum interference transistors of 1980s vintage is one such example [42]) can implement a single-transistor-frequency-multiplier.

Another interesting feature is that the transconductance of the transistor, which is the slope of the transfer characteristic in Fig. 5, can be either positive or negative depending on the value of V_G, or the gate bias. By connecting two SPINFETs in series – one with positive and the other with negative transconductance – one can realize a complementary device (analogous to CMOS), where the static energy dissipation is zero and current flows only during switching, resulting in dynamic dissipation only. This, of course, assumes that the off-current in a SPINFET is exactly zero, which can happen only in a true one-dimensional device where a single subband is occupied in the quantum wire channel, there is no spin relaxation in the channel, there is no extraneous magnetic field in the channel, and the spin injection/detection efficiencies of the ferromagnetic source and drain contacts are both exactly 100 %. All of these requirements – especially the last – are very difficult to fulfill. In general, the leakage current (current flowing in the off state) is quite high in a SPINFET, which makes the standby (static) energy dissipation substantial and possibly much more than that in a modern CMOS device.

Transit Time Spin Field-Effect Transistor (TTSFET)

A different of genre of transistors that exploit spin properties for operation was proposed by Appelbaum and Monsma, which they termed "transit time spin field-effect transistor" (TTSFET) [43]. This device employs silicon – the most technologically developed semiconductor – which unfortunately also has very weak spin-orbit interaction. Therefore, this device could not possibly have relied on gate controlled spin-orbit interaction to precess spins and modulate current as in the Datta-Das SPINFET. Instead it uses a fixed magnetic field in the channel (directed along the length of the channel) and a bias voltage to modulate the electron's velocity in the channel. The velocity modulation modulates spin precession. This, together with spin-selective injection and extraction of carriers in the channel, realizes transistor action very much like in the Datta-Das SPINFET.

The TTSFET is a four-terminal device and consists of six material layers with current flowing perpendicular to the heterointerfaces. The structure of this device is shown in Fig. 6.

The principle of operation of this transistor can be explained in five steps: First, a tunnel junction, composed of the first three layers on the left, injects unpolarized spins from a nonmagnetic metal emitter into the ferromagnetic base (Ferromagnet 1) under the emitter bias V_e applied between terminals 1 and 2. Second, the ferromagnetic base preferentially scatters the hot minority spins which then lose

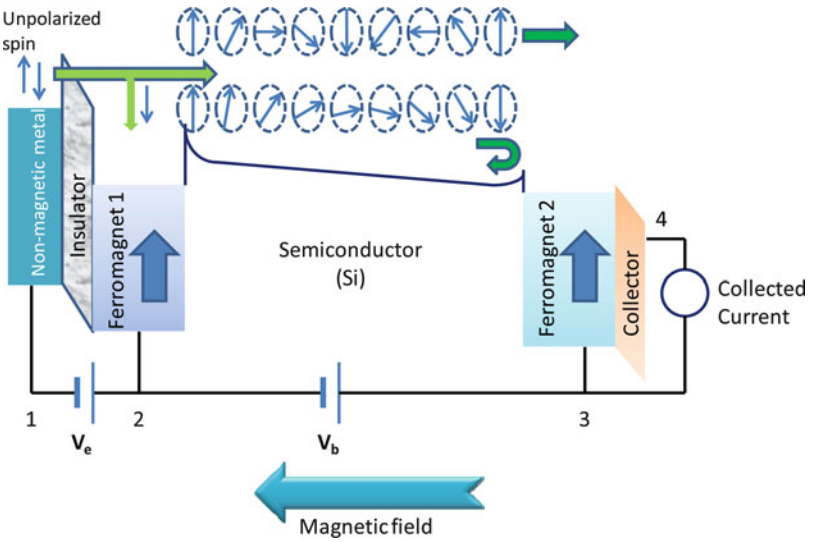

Fig. 6 Structure and operational principle of the TTSFET

energy and fall down into the base. The majority spins (i.e., spins whose polarizations are parallel to the magnetization of Ferromagnet 1) are much less scattered and hence do not lose much of their energy. As a result, they are able to emit over the Schottky barrier into the semiconductor (Si) [44, 45] – a phenomenon known as "hot-electron ballistic spin filtering." Third, the electrons that enter the semiconductor layer are at least partially spin polarized as a result of the filtering action. There is a static magnetic field in the semiconductor layer pointing in the direction of current flow. As the entering spins drift through this layer under the applied bias V_b applied between terminals 2 and 3, they precess about this magnetic field with an angular frequency given by the Larmor formula:

$$\Omega = \frac{d\phi}{dt} = \frac{g\mu_B B}{\hbar}. \tag{25}$$

The angle by which a given spin precesses in traveling from the ferromagnetic source to the ferromagnetic drain is

$$\Phi = \frac{g\mu_B B}{\hbar}\tau_t = \frac{g\mu_B B}{\hbar}\frac{L}{v}, \tag{26}$$

where τ_t is the transit time through the semiconductor layer, L is the width of the layer, and v is the electron's velocity in this layer.

Upon reaching the second ferromagnetic layer (Ferromagnet 2), spins which are parallel to this ferromagnet's magnetization are transmitted while the antiparallel spins are blocked. This step, namely, spin detection, is the fourth step in device

operation. In the final (fifth) step, the transmitted electrons are collected by the collecting layer which results in a current between terminals 3 and 4.

One can calculate the total transmission probability through the entire structure taking into account the imperfect spin-filtering action of Ferromagnet 1 and imperfect spin detection action of Ferromagnet 2.

Let the ferromagnets be magnetized in the +z-direction so that the spinors describing majority and minority spins in either ferromagnet are

$$\begin{aligned}[\Psi]_{\text{maj}} &= \begin{bmatrix} 1 \\ 0 \end{bmatrix} \\ [\Psi]_{\text{min}} &= \begin{bmatrix} 0 \\ 1 \end{bmatrix}. \end{aligned} \tag{27}$$

The spin-filtering action by Ferromagnet 1 will allow majority spins to enter the semiconductor layer with a probability of $(1 + \xi_1)/2$ and minority spins to enter with a probability of $(1 - \xi_1)/2$, where ξ is the spin-filtering efficiency for Ferromagnet 1. Using the Bloch sphere notation, the spinor describing the precessed majority spin at the interface with Ferromagnet 2 is

$$[\Upsilon]_{\text{maj}} = \begin{bmatrix} \cos\left(\dfrac{\Phi}{2}\right) \\ e^{i\nu} \sin\left(\dfrac{\Phi}{2}\right) \end{bmatrix} \tag{28}$$

while the spinor describing the precessed minority spin at the interface with Ferromagnet 2 is

$$[\Upsilon]_{\text{min}} = \begin{bmatrix} \sin\left(\dfrac{\Phi}{2}\right) \\ -e^{i\nu} \cos\left(\dfrac{\Phi}{2}\right) \end{bmatrix} \tag{29}$$

The overall probability of the precessed majority spin transmitting into the majority and minority spin bands of Ferromagnet 2 are respectively

$$\begin{aligned} \left|T_{\text{maj-maj}}\right| &= \frac{(1+\xi_1)(1+\xi_2)}{4} \left| \begin{bmatrix} \cos\left(\frac{\Phi}{2}\right) & e^{-i\nu} \sin\left(\dfrac{\Phi}{2}\right) \end{bmatrix} \begin{bmatrix} 1 \\ 0 \end{bmatrix} \right|^2 \\ &= \frac{(1+\xi_1)(1+\xi_2)}{4} \cos^2\left(\frac{\Phi}{2}\right) \\ \left|T_{\text{maj-min}}\right| &= \frac{(1+\xi_1)(1-\xi_2)}{4} \left| \begin{bmatrix} \cos\left(\frac{\Phi}{2}\right) & e^{-i\nu} \sin\left(\dfrac{\Phi}{2}\right) \end{bmatrix} \begin{bmatrix} 0 \\ 1 \end{bmatrix} \right|^2 \\ &= \frac{(1+\xi_1)(1-\xi_2)}{4} \sin^2\left(\frac{\Phi}{2}\right) \end{aligned} \tag{30}$$

where ξ_2 is the spin detection efficiency at Ferromagnet 2.

Similarly, the overall probability of the precessed minority spin transmitting into the majority and minority spin bands of Ferromagnet 2 are respectively

$$\begin{aligned} |T_{\text{min-maj}}| &= \frac{(1-\xi_1)(1+\xi_2)}{4}\left|\begin{bmatrix} \sin\left(\frac{\Phi}{2}\right) & -e^{-i\nu}\cos\left(\frac{\Phi}{2}\right)\end{bmatrix}\begin{bmatrix}1\\0\end{bmatrix}\right|^2 \\ &= \frac{(1-\xi_1)(1+\xi_2)}{4}\sin^2\left(\frac{\Phi}{2}\right) \\ |T_{\text{min-min}}| &= \frac{(1-\xi_1)(1-\xi_2)}{4}\left|\begin{bmatrix} \cos\left(\frac{\Phi}{2}\right) & -e^{-i\nu}\cos\left(\frac{\Phi}{2}\right)\end{bmatrix}\begin{bmatrix}0\\1\end{bmatrix}\right|^2 \\ &= \frac{(1-\xi_1)(1-\xi_2)}{4}\cos^2\left(\frac{\Phi}{2}\right). \end{aligned} \tag{31}$$

The total transmission probability is therefore

$$\begin{aligned} |T_{\text{total}}| &= |T_{\text{maj-maj}}| + |T_{\text{maj-min}}| + |T_{\text{min-maj}}| + |T_{\text{min-min}}| \\ &= \frac{1}{2}(1+\xi_1\xi_2\cos\Phi). \end{aligned} \tag{32}$$

Note that the total transmission probability is not the same for every electron since Φ depends on electron velocity v.

The angle Φ in Eq. 26 can be varied by varying the average electron velocity $\langle v\rangle = v_d$ by changing the bias voltage V_b across the semiconducting layer. Note that because of the Schottky barriers at the Ferromagnet 1/Semiconductor and Ferromagnet 2/Collector interfaces, the bias V_b, by itself, does not cause a current to flow. Instead, it modulates the current caused by V_e, i.e., the current flowing between terminals 3 and 4, by controlling the spin precession in the semiconducting layer by varying the drift velocity v_d. Since V_b controls the current flowing between terminals 3 and 4, transistor action has been realized.

This device shares one feature with the Datta-Das SPINFET and all its clones, namely, that current modulation is achieved via spin precession and not via charge modulation. In all other respects, it is very different from the Datta-Das SPINFET since it (1) does not rely on modulating spin-orbit interaction with a voltage (which is an advantage since it takes a lot of voltage to change spin-orbit interaction strength even slightly), and (2) it is a four-terminal device instead of a three-terminal device. The major disadvantage however is that the spin precession angle Φ is *not* velocity or energy independent, unlike in the case of the Datta-Das SPINFET. As a result, ensemble averaging over the electron energy (or velocity) will reduce the current modulation and adversely affect the transconductance of the transistor as well as causing some leakage current in the OFF state. The saving grace is that because of hot-electron transport across the semiconducting layer, the spread in the electron velocity is likely to be relatively small and hence the deleterious effect of ensemble averaging over the electron velocity may not be drastic.

One way to account for the deleterious effect of ensemble averaging phenomenologically is to replace Eq. 32 with the equation

$$|T_{\text{total}}| = \frac{1}{2}\left[1 + \xi_1\xi_2 v_0 \int_0^{\tau_t} \frac{1}{\sqrt{4\pi Dt}} \cos\left(\frac{g\mu_B B}{\hbar}t\right) e^{-t/\tau_s} e^{-(L-v_d t)^2/4Dt} dt\right]$$

where v_0 is a normalizing velocity, τ_t is the transit time, L is the separation between the two ferromagnetic contacts, τ_s is the spin-relaxation time, v_d is the drift velocity, and D is the diffusion coefficient of electrons. The integral in the above equation represents the effect of ensemble averaging. One would like to keep τ_t and L small in order to suppress the deleterious effect of ensemble averaging as much as possible, but then the spin may not be able to rotate by a sufficiently large angle between the two ferromagnetic contacts. Since the rotation rate is the Larmor precession rate that is fixed by the magnetic field, the angle of rotation increases with increasing transit time. One can try to increase the Larmor precession rate by increasing the magnetic field to compensate for a shorter transit time, but there is a limit on the magnetic field. If the magnetic field is too large, it will demagnetize the magnetic contacts and flip their magnetizations in the direction of the field. In other words, the magnetic field cannot exceed the coercive field of the contacts and hence cannot be increased indefinitely. The consequence of all this is that the effect of ensemble averaging remains a problem, unlike in the case of the Datta-Das transistor, and this limits the performance of the TTSFET.

Is the TTSFET an Energy-Efficient Device?

Since the TTSFET does not require charge modulation to achieve conductance modulation, and furthermore since the conductance modulation does not require modulating spin-orbit interaction which is weak in technologically important semiconductors, it may appear that the TTSFET will be more energy efficient than the Datta-Das SPINFET. However, this may not be true. It is a hot-electron device and therefore necessarily a high-power device. Hot-electron transport is needed for both the spin-filtering effect and to ensure that the energy spread in the transiting electrons is small so that energy averaging over the spin precession angle does not reduce the conductance modulation (on/off ratio) too much. The energy of the hot electrons that transit the device is dissipated in the collecting contact. Thus, it is not clear that the TTSFET is any more energy efficient than the Datta-Das SPINFET; in fact, it is likely to be less energy efficient since it takes a lot of energy to generate hot electrons.

In terms of conductance on/off ratio, that quantity is once again determined by the efficiencies of ballistic spin filtering and spin detection at ferromagnet/paramagnet interfaces. In fact, from Eq. 32, it can be predicted that the on-off ratio cannot exceed $(1 + \xi_1\xi_2)/(1 - \xi_1\xi_2)$ which makes it very similar to the Datta-Das SPINFET.

"Base Transport Factor" of the TTSFET

The expression for the transmission probability derived above did not account for the "base transport factor" α_T which is the fraction of the hot carriers injected into the semiconductor layer from the emitter that successfully makes it to the collector without being lost in the semiconductor layer (which is called "base") due to recombination with carriers of the opposite polarity or other effects. Since the carriers injected in the base of the TTSFET are hot carriers with high kinetic energy, they have a significant probability of being backscattered into the emitter and never reaching the collector. This will reduce α_T and hence $|T_{\text{total}}|$, which, in turn, reduces the on-current and the transconductance of the transistor. In order to retain a high enough α_T, it is imperative to keep the semiconductor layer width as small as possible in order to reduce the probability of backscattering. The problem with that approach is (see Eq. 26) if the layer width L is reduced, then the magnetic field strength B has to be increased in order to obtain the same degree of spin precession [same Φ] with all other variables being the same. This is not always desirable.

Experimental Status of the TTSFET

There has been significant progress towards the experimental demonstration of the TTSFET. Huang et al. and Appelbaum et al. have shown spin injection and detection in this transistor as well as transistor operation [46, 47]. In particular, Ref. [46] showed a 37 % spin injection efficiency and clear modulation of the transistor current by varying the bias voltage across the semiconductor layer which causes a variation in the spin precession angle Φ. The modulation however is small – the collector current changes by a factor of 7 or so, indicating that the conductance on/off ratio of this device is currently of the order of 7:1. This small ratio is most likely due to inefficient ballistic spin-filtering effect and spin detection, as well as perhaps some deleterious effect of ensemble averaging over electron velocity. Thus, it seems that all SPINFET type devices that require spin injection and detection at ferromagnet/paramagnet interfaces, including the TTSFET, suffer from the curse of having a very small conductance on/off ratio. The only solution to this problem is to enhance spin injection and detection efficiencies, but that seems to be a tall order.

Comparison Between the SPINFET, TTSFET, and MOSFET for Device Density, Speed, and Cost

The device density and cost for the SPINFET and the MOSFET are about the same since both are identical structures, except that the source and drain are

ferromagnetic for the SPINFET. The TTSFET will have a slightly lower device density and a slightly higher cost because it is a 4-terminal device as opposed to a 3-terminal device.

The speeds of these devices are determined by the transit time of carriers through the active region (channel in the cases of MOSFET and SPINFET, and the semiconducting layer in the case of the TTSFET). Since the thickness of the semiconducting layer in TTSFET is determined by film growth techniques while the channel lengths in SPINFET and MISFET are determined by lithography, and furthermore since the velocity of carriers in TTSFET is higher because they are hot carriers, the TTSFET is likely to have a slightly higher switching speed because carriers will travel through it faster.

Spin Bipolar Junction Transistors

Spin *bipolar* junction transistor (SBJT) proposals appeared in the literature soon after the SPINFET proposal by Datta and Das [48, 49] which were preceded by the proposal for a spin unipolar junction transistor (SUJT) [50] that was supposed to mimic a bipolar junction transistor.

These devices do require some kind charge modulation, and hence they are not any more energy efficient than traditional (charge-based) bipolar junction transistors. However, in the case of SBJT, there may be some additional *functionality* available because this device could, in principle, act as a four-terminal device that gives it more flexibility. This is discussed next.

The SBJT is identical to a traditional BJT except that the base of the transistor is ferromagnetic (e.g., GaMnAs) and therefore carriers residing in it are spin polarized. The conduction band profile of an SBJT, where the emitter is n^+-GaAs, the base is p^+ GaMnAs, and collector layer is n-GaAs, is shown in the left panel of Fig. 7, assuming that the transistor is n^+-p^+-n and is biased in the active region (emitter–base junction is forward biased, while base-collector junction is reverse

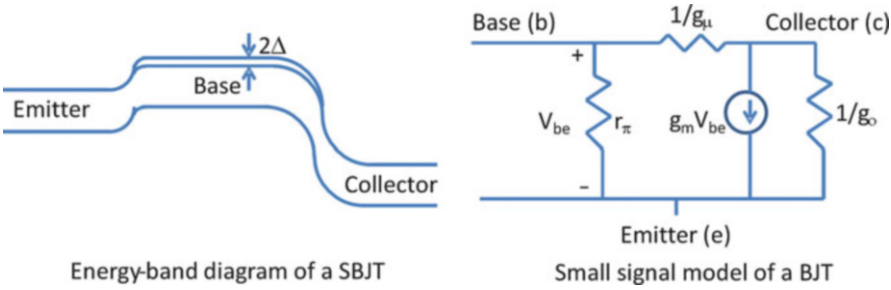

Fig. 7 Energy band diagram of an SBJT and the small signal model of any BJT. Any spin splitting in the valence band is ignored since it is not germane to the discussion

biased). The expressions for the emitter, base, and collector currents – I_E, I_B, and I_C – were derived in Ref. [39] and reproduced below.

$$\begin{aligned} I_C &= qA\frac{D_{nb}}{L_{nb}}\frac{1}{\sinh(W/L_{nb})}n_{be}\left[e^{V_{EB}/kT}-1\right]-qA\frac{D_{nb}}{L_{nb}}\coth(W/L_{nb})n_{bc}\left[e^{V_{CB}/kT}-1\right] \\ &\quad -qA\frac{D_{pc}}{L_{pc}}\coth\left(W_c/L_{pc}\right)p_{oc}\left[e^{V_{CB}/kT}-1\right] \\ I_E &= qA\frac{D_{nb}}{L_{nb}}\coth(W/L_{nb})n_{be}\left[e^{V_{EB}/kT}-1\right]-qA\frac{D_{nb}}{L_{nb}}\frac{1}{\sinh(W/L_{nb})}n_{bc}\left[e^{V_{CB}/kT}-1\right] \\ &\quad +qA\frac{D_{pe}}{L_{pe}}\coth\left(W_e/L_{pe}\right)p_{oe}\left[e^{V_{EB}/kT}-1\right] \\ I_B &= -I_E-I_C, \end{aligned} \tag{33}$$

where A is the cross-sectional area of the transistor, W_c is the collector width, W_e is the emitter width, D_{nb} (L_{nb}) is the minority carrier diffusion coefficient (length) of electrons in the base, D_{pc} (L_{pc}) is the minority carrier diffusion coefficient (length) of holes in the collector, D_{pe} (L_{pe}) is the minority carrier diffusion coefficient (length) of holes in the emitter, $n_{be}=\left(n_i^2/N_{AB}\right)(1+\alpha_e\alpha_{0b})/\sqrt{1-\alpha_{0b}^2}$, $n_{bc}=\left(n_i^2/N_{AB}\right)(1+\alpha_c\alpha_{0b})/\sqrt{1-\alpha_{0b}^2}$, $p_{oc}=(n_i^2/N_{DC})$, $p_{oe}=(n_i^2/N_{DE})$, N_{AB} is the acceptor concentration in the base, N_{DC} is the donor concentration in the collector, N_{DE} is the donor concentration in the emitter, α_e and α_c are the non-equilibrium spin polarizations in the emitter and collector, and $\alpha_{0b}=\tanh(\Delta/kT)$ is the equilibrium spin polarization in the base, while 2Δ is the spin-splitting energy of the conduction band in the base.

A routine small signal analysis carried out in Ref. [51] has shown that the SBJT has about the same voltage and current gains as a conventional (non-spin-based) BJT. The short-circuit current gain $\beta=\partial I_C/\partial I_B$ however is not constant and depends on the spin-splitting energy Δ in the base. This last quantity can be modulated with an external magnetic field, which can therefore act as a fourth terminal. Thus, this device will be suitable for a frequency mixer. If the base current is an ac sinusoid with an angular frequency ω_1 and the modulating magnetic field is another sinusoid with an angular frequency ω_2, then the collector current will contain frequency components $\omega_1 \pm \omega_2$. This nonlinear functionality makes the SBJT a more powerful device than a conventional BJT.

The SUJT of Ref. [50] unfortunately turns out to be a device which simply cannot work as a transistor. Transistors are benchmarked by two properties: the output conductance g_0 which determines the fan-out and the voltage gain given by $a_v=g_m/g_0$ (where g_m is the transconductance of the transistor) and the so-called feedback conductance g_μ which determines the isolation between the input and output terminals. Isolation is an extremely important property which ensures that the output signal of any device is controlled by the input signal, but not the other way around. The well-known small signal model of a bipolar junction transistor is

shown in the right panel of Fig. 6. Both g_0 and g_μ should be vanishingly small to yield a large voltage gain and good isolation between input and output terminals. Bandyopadhyay and Cahay [51] showed that both these quantities are actually extremely large in the SUJT; in fact, g_μ is 34 *orders of magnitude* larger in the SUJT than in a conventional BJT, meaning that the SUJT practically has no isolation, not to mention that it may not have any gain either because of the very large g_0. Such a "transistor" is obviously not suitable for signal processing of any kind.

There is a plethora of other spin-based transistors which have been proposed and some have been experimentally demonstrated. Not all of them can be discussed here, but there are two transistors that deserve special mention because of the significant experimental progress made in fabricating and demonstrating them. These two devices are the all-metal spin transistor proposed by Johnson [52, 53] and the spin-valve transistor demonstrated by a large number of researchers including Monsma et al. [44], Mizushima et al. [54], and LeMinh et al. [55]. Their performances are probably not superior to that of the SBJT, but they have attracted considerable attention from experimentalists. They are not discussed here, but instead the reader is referred to an excellent review of these transistors by Jansen et al. [56].

Single-Spin Logic

The idea of encoding logic bits 0 and 1 in *orthogonal* (mutually antiparallel) spin polarizations of a single electron is probably due to Feynman, although no definitive work exists in the literature that points to this. A single electron (or its spin) will obviously be the smallest vehicle for a logic bit since quarks are not stable. If indeed one could host logic bits in the spin polarization of a single electron, then one should be able to switch bits by simply flipping spins, without moving the electrons in space and causing current flow. This is potentially a very energy-efficient scheme.

The reason why it can work is that the spin of an electron, unlike its charge, is a pseudo-vector that has a fixed magnitude of $\hbar/2$ but a variable direction. If a lone electron is placed in a magnetic field, then the direction of the spin (or spin polarization) can point either parallel or antiparallel to the field. No other direction would be stable. This can be shown easily from the Pauli equation that governs the electron's spin property:

$$\left\{[H_0] - \frac{g}{2}\mu_B \vec{B}^B \bullet \left[\vec{\sigma}\right]\right\}[\psi] = E[\psi], \tag{34}$$

where $[H_0]$ is the spin-independent Hamiltonian, g is the Landé g-factor, $\vec{B}$ is the flux density of the magnetic field, $\left[\vec{\sigma}\right]$ is the Pauli spin matrix, and $[\psi]$ is the 2×1 component spinor describing the spin. Assume now that the magnetic field is in

the z-direction which makes $\vec{B} \bullet \left[\vec{\sigma}\right] = B_z\left[\vec{\sigma}_z\right]$. In that case, diagonalization of the total Hamiltonian in Eq. 17 immediately yields that the eigenspinors are

$$[\psi] = \begin{bmatrix} 1 \\ 0 \end{bmatrix} \text{ or } \begin{bmatrix} 0 \\ 1 \end{bmatrix}, \tag{35}$$

which are +z and −z polarized states, meaning that they are oriented parallel and antiparallel to the magnetic field. Therefore, the electron's spin can point only in *two* directions: either parallel to the field (labeled the "down" state, or $|\downarrow\rangle$) or antiparallel (labeled the "up" state, $|\uparrow\rangle$). These two "polarizations" could represent the binary bits 0 and 1. Switching between the two bits would simply require flipping the spin *without moving the electron in space and causing a current to flow*.

Flipping the spin, however, does dissipate some energy. The two spins polarizations do not have the same energy since the two eigenenergies of Eq. 34 are separated by an amount $g\mu_B|B|$ which is the Zeeman splitting energy [57]. At the very least, this amount of energy must be dissipated in flipping the bits from 0 to 1, or vice versa. But this energy can be made very small by using a weak magnetic field that has a small flux density B. It cannot be made arbitrarily small in the presence of noise, but ultimately what matters is whether this approach could be more energy efficient than the traditional charge-based transistor paradigm or the SPINFET/TTSFET paradigm. That will determine whether "single spintronics" – where bit information in encoded in single spins – has any potential in digital information processing.

It is intuitive to think that if one encodes binary information in antiparallel spin states in a magnetic field, one must ensure that $|g\mu_B B| >> kT$ where kT is the thermal energy, since the two spin levels might be broadened in energy by $\sim kT$ and therefore the above condition must be satisfied so that the two spin states are distinguishable at a temperature T. This is untrue. Spin-phonon coupling is very weak, much weaker than charge phonon coupling, so that spin levels are not broadened by $\sim kT$ at a temperature T unlike energy states coupled to the charge degree of freedom. As a result, $|g\mu_B B|$ can be much less than the thermal energy kT and yet the spin levels can remain distinguishable at the temperature T. A case in point is electron spin resonance (ESR) which involves transitions between two Zeeman split levels separated in energy by $|g\mu_B B|$ which is typically a few tens of μeV (microwave photon energy) in most solids. In spite of that, when ESR experiments are carried out at room temperature (when $kT >> |g\mu_B B|$), the signals remain well resolved, meaning that the spin-split levels remain distinguishable even when $|g\mu_B B| << kT$. This can happen only if the spin levels are not broadened by $\sim kT$. Therefore, in principle, the logic states will remain demarcated even if $|g\mu_B B| << kT$. However, that does not mean that one can work with $|g\mu_B B| << kT$. The reason one *cannot* has nothing to do with level distinction or level broadening, but has to do with the static error rate that can be tolerated.

If the spin system is in equilibrium with its surrounding, then the spin occupation probability will follow Fermi-Dirac distribution or at least Boltzmann distribution.

Therefore, the static error probability, which is the probability of the spin spontaneously transitioning between the two levels (and causing a static error), is $\exp[-|g\mu_B B|/kT]$. If one wants to keep this probability small, then one must ensure that $|g\mu_B B| >> kT$. For example, if one wants this probability to be as small as 10^{-15}, then $|g\mu_B B| = 34.5\ kT$. Since there are practical limits on how large the g-factor in any technologically important material can be and how strong a magnetic field can be generated on a chip, it is obvious that there are limits on how large $|g\mu_B B|$ can be. Indeed it is this limitation that makes room-temperature operation impossible and mandates working at liquid helium temperatures.

Note that spin has two other advantages over charge. First, because of weaker spin-phonon coupling, a spin system can be maintained in a nonequilibrium state longer and more easily than a charge system since it is the coupling to the thermal bath that enforces equilibrium. In a nonequilibrium system, the occupation probability of the two spin-split states encoding the binary bits 0 and 1 is *not* governed by Boltzmann statistics or Fermi-Dirac statistics, so that the relative occupation probability of the two states is *not* $\exp[-|g\mu_B B|/kT]$. Therefore, the bit error probability p associated with occupation of the wrong state is not $\exp[-|g\mu_B B|/kT]$, but could be considerably less. In that case, one might possibly work at higher temperatures if nonequilibrium spin systems are involved. Boolean logic operations in nonequilibrium systems have been discussed by Zhirnov et al. [58] and Cavin et al. [59]. Energy dissipation in some nonequilibrium systems has been discussed by Nikonov et al. [60]. However, these are not particularly attractive from the perspective of energy efficiency since maintaining a system out of equilibrium needs a continuous supply of energy and the additional energy cost may outweigh any energy saving accruing from nonequilibrium dynamics.

A second advantage of spin over charge is that the former does not couple easily to stray electric fields (except through spin-orbit interaction). Hence spin is more robust against electrical noise. These two features make "spin" superior to "charge." It is not an intrinsic advantage, but an extrinsic advantage.

The shortcomings of charge as a state variable to encode information were anticipated (although not expounded) in Refs. [58, 59] which advocated investigating alternate state variables, different from charge, to encode logic states (see also [61]). Later work [62, 63] that questioned this belief did not account for the extrinsic advantages of spin (weaker spin-phonon coupling, easier enforcement of nonequilibrium dynamics, stronger immunity against noise, etc.). Therefore, the pronouncement of Ref. [62, 63] that spin and charge are "equal" is not really correct; spin may not have an intrinsic advantage, but it does have an extrinsic advantage. In more realistic scenarios, when a *collection* of spin moments (namely, the magnetic moment of a single-domain nanomagnet) and a *collection* of electronic charges (namely, the channel charge in a MOSFET) are used to encode logic bits, spin turns out to have an *intrinsic* advantage as well. There is an internal interaction between spins that reduces the energy dissipation when a many-spin system (e.g., a single-domain nanomagnet) switches, compared to a many-charge system (e.g., a MOSFET). That interaction is the exchange interaction between spins which makes all the numerous spins in a single-domain magnet rotate in

unison during magnetization flip and act like a giant classical spin [4, 5]. There is no such interaction between charges that makes them act in concert. Thus N spins can have a single degree of freedom while N electronic charges have N degrees of freedom. This can reduce the energy dissipation in switching N spins by a factor of N compared to switching N charges.

Single-Spin Logic (SSL) Family

A well-known paradigm where bistable spin polarizations of an electron (placed in a magnetic field) are used to represent the binary bits 0 and 1 is *Single-Spin Logic* (SSL) [1, 64, 65] which is a single-spin-based approach to combinational and sequential logic.

In SSL, single electrons are confined in semiconductor quantum dots that are delineated on a wafer. The latter is placed in a dc magnetic field. This field may be generated by a permanent magnet or an electromagnet, with the former requiring no energy budget. The magnetic field defines the spin quantization axis and makes the spin polarization of every electron on the wafer bistable, i.e., only polarizations parallel and antiparallel to the global field are stable or metastable in each dot. These two polarizations represent the logic bits 1 and 0, respectively.

Each spin can interact only with its nearest neighbor via exchange. This is ensured by maintaining a small separation (~10 nm) between nearest neighbor dots so that the wavefunctions of their resident electrons overlap in space. Wavefunctions of electrons in second nearest neighbor dots do not overlap, and therefore there is no second nearest neighbor exchange interaction.

Input data are provided to the quantum dot array by aligning the spins in certain chosen dots (designated as input ports) in desired directions (parallel or antiparallel to the global magnetic field) using external agents, such as local magnetic fields (**writing**). These are generated with nanomachined spin-polarized scanning tunneling microscope tips that are hardwired and connected to the input dots with fine-line lithography. The arrival of the inputs takes the interacting array into a many-body excited state. The system is then allowed to relax to the thermodynamic ground state by coupling to the thermal bath. The coupling of a single isolated electron to the thermal bath is weak, but the collective coupling of many interacting electrons (a many-body system) to the thermal bath is much stronger. Hence the many-body system relaxes to ground state much faster than an isolated spin.

When the ground state is reached by emitting phonons, magnons, etc., the spin orientations in certain other chosen dots (designated as output ports) will represent the result of a specific computation in response to the input bits. The quantum dots are arranged in space in such a way that the nature of the nearest neighbor interactions guarantees this occurrence. The result of the computation (spin orientations in output ports) can be read using a variety of schemes, all of which have been experimentally demonstrated [66–68] (**reading**). Since this is an "all-hardware" computer with no involvement of any "software," it is extremely fast in producing the final result. The disadvantage however is that a particular computer

can do only one specific computation since the computer is entirely hard wired and is not easily reconfigured for a different task. This is an extreme example of application-specific integrated circuit (ASIC).

Note that unlike the SPINFET, which is a single device or switch, the SSL is a complete architecture that goes well beyond a single device or even a gate. A single switch can only switch on and off, while a single gate can carry out one specific Boolean operation and nothing else. Therefore, both are incapable of performing universal computation. In contrast, SSL is capable of universal computation since (as will be shown later) one can implement universal Boolean logic gates (the NAND gate) and connect them in any desired fashion using "spin wires" to realize arbitrary combinational or sequential circuits.

Note also that SSL is an equilibrium system where the spins are *not* maintained out of equilibrium. In fact, computation is performed by relaxation of excited spins to the ground state by coupling with the thermal bath (phonons). Therefore, this paradigm does not exploit any possible advantage of the nonequilibrium dynamics discussed in Refs. [58–60]. At the same time, no energy is expended to maintain the system out of equilibrium.

Equilibrium statistics mandates that the absolute minimum energy dissipated in a single irreversible logic operation should be the Landauer-Shannon limit *kTln2* [2]. However, reaching this limit requires complicated switching dynamics (e.g., time-modulated potentials) and extreme timing synchronization between various components of the switching cycle [2]. If that precision is unattainable, no time-modulated potential is available, and switching is carried out in a simple abrupt step, then the minimum energy dissipation will be

$$E_{diss}^{\min} = kT\ln(1/p), \tag{36}$$

where p is the static bit error probability (i.e., the probability that the bit flips spontaneously). It turns out that the energy dissipated in any irreversible logic operation in an SSL NAND gate is given by the above expression [65]. This is actually a remarkable result since it shows that no paradigm can better the SSL in dissipation for an irreversible logic operation carried out non-adiabatically without elaborate time-modulated potentials and ultra-precise timing mechanisms, since SSL operates at the thermodynamic limit.

SSL NAND Gate for Universal Boolean Logic

SSL is extremely efficient for application-specific integrated circuits (ASICs) which can be very fast. However, this is not necessarily very useful since ASICs can do only one type of computation and are not universal computing machines. For general purpose computing (GPC), or to build a universal computing machine, one must construct combinational and sequential Boolean logic circuits by employing universal logic gates (e.g., the NAND gate) realized with few interacting single spins. These must then be interconnected with "spin wires" that ferry spin signals between them

unidirectionally. The two ingredients – NAND gates and unidirectional spin wires – are all that are required to implement a universal computing machine.

A NAND gate is implemented with a linear array of three quantum dots each containing a single conduction band electron. Single electron occupancy in each dot is guaranteed by placing the Fermi level above the lowest spin-split subband level in the conduction band, but below the higher spin-split level. Fermi level placement is accomplished by proper choice of materials and doping. All three quantum dots are placed in a global static magnetic field which causes the spin splitting of every subband level.

The wavefunctions of the conduction band electrons are sufficiently delocalized in space that wavefunctions of nearest neighbor electrons overlap. As a result, there is nearest neighbor exchange interaction, but no second nearest neighbor interaction. The global magnetic field defines the spin quantization axis since the spin in any dot will be aligned either parallel or antiparallel to it. If a spin is parallel to the field, it encodes the binary bit 1, and if it is antiparallel, it encodes the binary bit 0. It is assumed that the dots are small enough and their capacitance is small enough that it is not energetically favorable for electrons to jump between dots. The temperature is also assumed to be low.

The two peripheral dots in the array are treated as input ports whose resident spins are aligned to conform to input bits – either 0 or 1 – with external agents that can generate local magnetic fields. The central dot is the output port and its resident spin's polarization encodes the output bit. This system is shown in Fig. 7.

It was rigorously shown in Ref. [65] that the ground state spin configuration in this system is *anti-ferromagnetic*, i.e., spins in nearest neighbor quantum dots will be mutually antiparallel as long as the exchange interaction strength between nearest neighbors is greater than one-half the Zeeman splitting energy in any dot due to the global magnetic field, and the local magnetic fields applied to the input dots are much stronger than the global magnetic field. In that case, whenever the two inputs are 1, the output must be 0 to preserve the anti-ferromagnetic ordering, and similarly whenever the two inputs are 0, the output must be 1. When one input is 1 and the other is 0, a tie seemingly occurs. This tie however is broken by the global magnetic field, which will generate a slight preference for the spin in the output dot to be aligned parallel to the field when the two inputs are dissimilar (assuming that the g-factor of the dot material is positive). Since spin orientation parallel to the global magnetic field encodes logic bit 1, the output will be 1. Thus, the input–output relation of this system obeys the truth table of the NAND gate shown in Fig. 8.

Theory of the SSL NAND Gate

To treat this 3-dot system using rigorous quantum mechanics and show that it indeed acts as described (i.e., performs the NAND logic operation), one must consider the Hamiltonian of the array. This can be described by a Hubbard Hamiltonian which will have 29 independent basis states. However, if *single* electron occupancy is assumed in each dot, then the Hubbard Hamiltonian can be reduced to a much

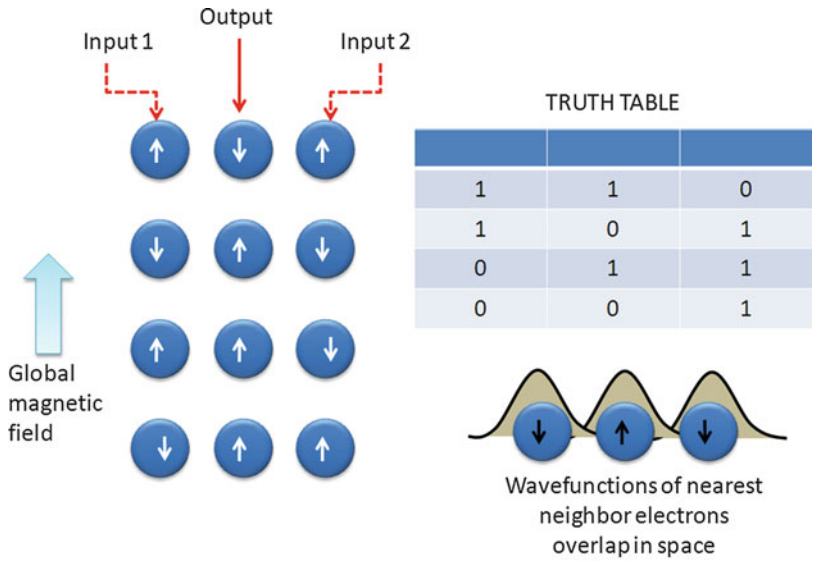

Fig. 8 A linear array of three quantum dots, with nearest neighbor exchange interaction, implements a NAND gate if the array is placed in a global magnetic field. Spin parallel to the field encodes bit 1 and spin antiparallel encodes bit 0. The following conditions must be satisfied: (i) the exchange interaction strength must exceed one-half of the Zeeman splitting caused by the global magnetic field, and (ii) the local magnetic field used to align input spins causes a Zeeman splitting that is far greater than the Zeeman splitting due to the global magnetic field

simpler Heisenberg Hamiltonian [64, 65] which has only eight independent (orthonormal) basis states. This requires that the dots are so small and have such small capacitance that the energy cost to add a second electron to any dot is prohibitive.

The Heisenberg Hamiltonian is given by

$$H_{\text{Heisenberg}} = \sum_{<ij>} J_{ij}^{\parallel} |\sigma_{zi}\sigma_{zj} + \sum_{<ij>} J_{ij}^{\perp} \left(\sigma_{xi}\sigma_{xj} + \sigma_{yi}\sigma_{yj}\right) - \sum_{\text{input dots}} \sigma_{zi} h_{zi}^{\text{inputs}} - \sum_{i} \sigma_{zi} h_{zi}^{\text{global}} \tag{37}$$

where the σ-s are Pauli spin matrices. The convention adopted is that the local magnetic field needed to align spins in input dots, and the global magnetic field, are always along the z-axis.

The last two terms in the Hamiltonian account for the Zeeman energies associated with these fields. The first two terms account for exchange interaction between nearest neighbors (the angular brackets denote summation over nearest neighbors). Finally, the isotropic case is considered when $J_{ij}^{\perp} = J_{ij}^{\parallel} = J$, where J is the exchange energy, which is nonzero if the wavefunctions in dots i and j overlap in space.

The spins in the quantum dots are polarized in either the +z- or −z-direction by the global magnetic field (conforming to bits 1 or 0), and the corresponding states

are designated as "upspin" (↑) and "downspin" (↓) states, respectively. Recall that the upspin state (aligned antiparallel to the global magnetic field) encodes bit 0 and the downspin state (parallel to the global field) encodes bit 1.

There are eight independent 3-spin basis states representing the spin configurations in the 3-dot array, which are $|\uparrow\uparrow\uparrow\rangle, |\uparrow\uparrow\downarrow\rangle, |\uparrow\downarrow\uparrow\rangle, |\uparrow\downarrow\downarrow\rangle, |\downarrow\uparrow\uparrow\rangle, |\downarrow\uparrow\downarrow\rangle, |\downarrow\downarrow\uparrow\rangle, |\downarrow\downarrow\downarrow\rangle$. In each state, the first entry is the spin polarization in the left dot, the second in the central dot, and the third in the right dot. These eight basis functions form a complete orthonormal set. The matrix elements $< \phi_m|H_{\text{Heisenberg}}|\phi_n >$ are given in the matrix below, where the ϕ-s are the 3-electron basis states enumerated above.

$$\begin{pmatrix}
2J-h_L-h_R-3Z & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\
0 & -h_L+h_R-Z & 2J & 0 & 0 & 0 & 0 & 0 \\
0 & 2J & -2J-h_L-h_R-Z & 0 & 2J & 0 & 0 & 0 \\
0 & 0 & 0 & -h_L+h_R+Z & 0 & 2J & 0 & 0 \\
0 & 0 & 2J & 0 & h_L-h_R-Z & 0 & 0 & 0 \\
0 & 0 & 0 & 2J & 0 & -2J+h_L+h_R+Z & 2J & 0 \\
0 & 0 & 0 & 0 & 0 & 2J & h_L-h_R+Z & 0 \\
0 & 0 & 0 & 0 & 0 & 0 & 0 & 2J+h_L+h_R+3Z
\end{pmatrix}$$

In the above matrix, Z is one-half of the Zeeman splitting energy associated with the global magnetic field (i.e., $2Z = g\mu_B B_{\text{global}}$), while $2h_L$ and $2h_R$ are Zeeman splitting energies in the left and right input dots caused by the local magnetic fields that write input data ($2h_L = g\mu_B B_{\text{local}}^{\text{left}}$; $2h_R = g\mu_B B_{\text{local}}^{\text{right}}$). If the local magnetic field is in the same direction as the global field and writes bit 1, then the corresponding h is positive; otherwise, it is negative. The quantity J is always positive.

Agarwal et al. [65] diagonalized the above Hamiltonian for the four possible inputs to the NAND gate corresponding to both inputs being logic 1 ($h_L = h_R = h$), left input logic 1 and right input logic 0 ($h_L = -h_R = h$), left input logic 0 and right input logic 1 ($h_L = -h_R = -h$), and both inputs being logic 0 ($h_L = h_R = -h$). It was found that the ground state wavefunctions in the four cases approach the states $|\uparrow\downarrow\uparrow\rangle$, $|\uparrow\uparrow\downarrow\rangle, |\downarrow\downarrow\uparrow\rangle, |\downarrow\uparrow\downarrow\rangle$, respectively, provided $h_L, h_R > J$ and $J > Z/2$. Thus, the ground state spin polarization in the output dot is always the NAND function of the spin polarizations in the input dots, provided the Zeeman splitting caused by the local magnetic fields that "write" input bits in the input dots is much larger than the strength of exchange coupling between nearest neighbors, and the latter, in turn, is larger than one-fourth of the Zeeman splitting caused by the global magnetic field. Therefore, the NAND gate is indeed realized by three spins with nearest neighbor exchange coupling if one can satisfy the conditions $h_L, h_R > J$ and $J > Z/2$. Since the NAND gate is universal, any arbitrary combinational or sequential circuit can be implemented by interconnecting NAND gates with a "spin wire" shown in Fig. 9.

Spin Wire: Unidirectional Information Transfer Along a Spin Wire

A spin wire is a linear array of quantum dots, each containing a single electron, with *tunable* nearest neighbor exchange interaction. Between each pair of neighbors, there is a metal gate that is electrically accessed. Delineating these gates is a

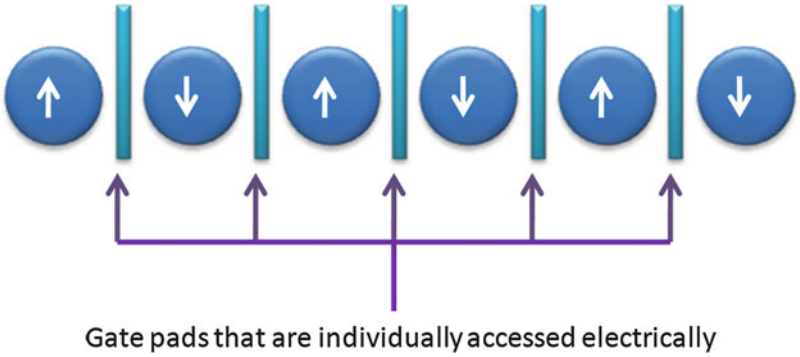

Fig. 9 A "spin wire" for transmitting binary bit information encoded in single electron spins unidirectionally. The spin state is replicated in every other dot. The gate pads are raised to high potential pairwise at a time with a 3-phase clock to make a logic bit propagate unidirectionally down the chain

lithographically challenging job since the spacing between dots will not exceed 10 nm for sufficient exchange-coupling strength. However, with CMOS approaching the 22 nm node technology where individual gates are contacted, lithography has now progressed to the point where this will soon be feasible, if it is not already feasible.

When a positive potential is applied to the gate, it lowers the potential barrier between the flanking dots and allows their resident electrons' wavefunctions to overlap in space. This turns on the exchange coupling between them only when the gate pad is activated. Without the positive gate potential, the barrier between dots is so high that exchange coupling is insignificant and the two dots are decoupled. Thus, one can turn the exchange interaction on or off with the gate pad potential.

The next subsection will describe how a spin polarization state can be *unidirectionally* propagated from left to right along the spin wire in Fig. 9 using a 3-phase clock. The clock signal is a sequence of positive voltage pulses that are applied to the gates interposed between each pair of dots. The arrival of a positive voltage pulse temporarily lowers the potential barrier between two adjacent quantum dots. By sequentially exchange coupling three adjacent dots at a time using a 3-phase clock, the spin state can be propagated *unidirectionally* from left to right in a bucket-brigade fashion [69]. In conventional circuits, the wires are bidirectional, but the logic devices (transistors) are unidirectional since they possess isolation between their input and output terminals. Here, the wires have to be unidirectional to implement logic circuits. Otherwise, back propagation of logic signals from one do to another will wreak havoc with logic operation.

A spin wire can obviously also perform the role of fan-out where a signal is split into multiple paths in order to drive multiple stages with the output of one stage.

Finally, one last requirement that wires must satisfy is the function of "cross-over" where two wires cross each other in space without interfering with one another. Combinational logic circuits (e.g., adders and subtractors) do not always

need crossover, but sequential circuits (e.g., flip-flops) will require feedback of an output state to an input state and therefore crossover. This is the most challenging requirement and normally will be implemented with multiple layers of dots where a dot in one layer is sufficiently distant from the nearest dot in the closest layer to avoid significant exchange coupling. As a result, combinational logic is always easier to implement in SSL than sequential logic.

Not only should a spin wire be able to ferry spin state from one dot to a remote dot, but it must do so *unidirectionally*, so that signal always flows from the input stage to the output stage and not the other way around. In conventional circuits, the wires are not unidirectional since the devices (transistors) themselves are inherently unidirectional. For example, in a field-effect transistor, the input signal (in the form of a voltage) is applied to the gate terminal which affects the current flowing through the channel and this current is the output signal. However, the channel current does not affect the gate voltage. Thus, a master–slave relationship exists between the input and output, where the former controls the latter, but the latter has no influence over the former. Device physicists and engineers call this property "isolation" between the input and output.

Unfortunately, there is no isolation between two quantum dots – one input and the other output – when they are coupled by exchange interaction. Exchange interaction is perfectly bidirectional. As a result, the input dot affects the output dot just as much as the output dot affects the output dot. Since the device is not unidirectional, one must make the wires unidirectional.

There is indeed no easy way to impose unidirectionality in *space*, but there is a way to impose it in *time* via sequential clocking [70]. This is actually a standard technique used to steer signal unidirectionally through devices that lack isolation between their input and output terminals. A well-known example of this is the charge-coupled-device shift register, frequently used in digital imagers, where a charge packet carrying bit information is steered unidirectionally through a linear array of charge-coupled devices (which are bidirectional themselves) using 3-phase clocks [71]. A similar scheme is adopted for SSL. By sequentially raising and lowering potential barriers between two pairs of dots at a time using a 3-phase clock, one can sequentially turn exchange interactions on and off between any two adjacent pairs and steer spin signal unidirectionally along a spin wire. This paradigm was explained in Ref. [69].

In order to carry out the sequential clocking, the potentials of two succeeding gate pads are raised simultaneously. Thus, three consecutive electrons are exchange coupled and the third electron begins to assume the polarization of the first as the array approaches the anti-ferromagnetic ground state. It is assumed that the many-body ground state is reached in a time shorter than the clock period, which is a reasonable assumption since a coupled spin system can relax to the ground state much faster than a single isolated spin. When the relaxation is complete, the spin state of the first electron has been replicated in the third and ultimately in every odd-numbered electron, thus transmitting signal unidirectionally.

Energy Dissipation in SSL

There are two sources of energy dissipation in SSL: internal dissipation in the gate while it carries out a logic operation (flipping of spins) and dissipation in the clock that steers bits unidirectionally. Both are examined below:

Gate Dissipation

Agarwal et al. [65] showed that the energy dissipated in a NAND gate operation is of the order of $g\mu_B|B_{\text{global}}|$ which also happens to be the energy difference between the two antiparallel spin states in any isolated dot. Furthermore, it was shown that if the coupled spin system is in thermal equilibrium and governed by Boltzmann statistics, then the energy $g\mu_B|B_{\text{global}}|$ is also equal to $kTln(1/p)$ where p is the probability of gate error caused by spins straying from the many-body ground state (which represents the correct gate result) into many-body excited states by absorbing phonons or magnons [65]. Remarkably, this energy – $kTln(1/p)$ – is the minimum energy that any irreversible gate must dissipate in a single logic operation as long as the gate is in thermodynamic equilibrium with the environment, and the switching is carried out abruptly without any time-modulated potential, by taking the system from one state to another.

The energy dissipated in a gate operation, as well as the strength of the global magnetic field, is therefore determined by how much gate error probability can be tolerated at a given temperature. If the error probability cannot exceed 10^{-15}, then the energy dissipated in a gate operation will be $kT\ \ln(10^{15}) = 34.5\ kT$ at any temperature. Since this energy is also equal to $g\mu_B|B_{\text{global}}|$, one must choose the global magnetic field strength such that $\left|B_{\text{global}}\right| = \frac{kT}{g\mu_B}\ln(1/p)$. With $p = 10^{-15}$, $\left|B_{\text{global}}\right| = \frac{34.5\,kT}{g\mu_B}$.

Clock

The clock in SSL causes additional dissipation. If one uses non-adiabatic clocking to maintain sufficient speed of operation and adequate noise margin, then the energy dissipated in the clock will be $\sim CV^2$ where C is the capacitance of the clock pad and V is the amplitude of the clock pulse. This energy should be considerably larger than kT to protect against thermal noise [72]. Let us assume that the clock amplitude V is 10 times larger than the thermal voltage fluctuation on the clock pad which is $\sqrt{kT/C}$, resulting in a signal-to-noise ratio of 20 dB. Therefore, the clock dissipation will be 100 kT per cycle.

It should be clear now that there are two dissipaters in an SSL circuit – the clock and the device. The former could dissipate about 100 kT per clock cycle and the latter dissipates $kTln(1/p)$ per bit flip, which will be 34.5 kT if one operates with a bit error probability of 10^{-15}. Therefore, the total dissipation per clock cycle per bit is potentially ~134.5 kT, which is considerably less than the ~50,000 kT that present CMOS transistors dissipate.

Speed of SSL

The speed of SSL (i.e., the maximum allowable clock frequency) is determined by four factors: (1) the speed with which an input bit can be written in an input port by the writing agent, (2) the speed with which an output bit can be read in an output port by the reader, (3) the gate switching speed, and (4) whether or not the architecture is pipelined. If the architecture is pipelined, then the clock speed is limited by the lowest of the other three speeds; otherwise, the clock speed will be much slower. In a non-pipelined architecture, the clock speed will be M times slower than in a fully pipelined architecture, where M is the number of bit flips required to execute the most complex calculation. Needless to say, the number M can be extremely large, which makes all non-pipelined architectures impractical.

Pipelining in SSL

Fortunately, SSL is a pipelined architecture. The clock in SSL not only propagates signals unidirectionally, but it is also responsible for making the architecture pipelined. To understand this concept, consider the spin wire in Fig. 9. The input bit is applied to the leftmost (first) dot by aligning its spin in the up direction. This is done during the first clock cycle. In the next cycle, the potentials in the first two gate pads are raised to cause nearest neighbor exchange coupling between the first three dots which then orders their spin in the anti-ferromagnetic configuration. In the third cycle, the potential in the first gate pad is lowered, while that in the second gate pad is held and that in the third gate pad is raised to cause nearest neighbor coupling between the second, third, and fourth dots. This ensures anti-ferromagnetic ordering within this latter trio which successfully orients the fourth dot's spin antiparallel to the input spin. In the fourth cycle, the potential at the second gate pad is lowered, that in the third gate pad is held high and that in the fourth gate pad is raised, which successfully transfers the input bit applied at the first dot to the fifth dot, thereby ensuring unidirectional signal propagation along the wire.

The point to note here is that as soon as the potential in the first gate pad is lowered in the third cycle, the first dot is decoupled from the chain and the input applied to this dot *can then be changed without affecting successful replication of the original input bit in the fifth dot as described above*. In other words, the input can be changed during the fourth cycle regardless of how long the chain is. During the fifth clock cycle, when the first and second gate pad's potentials are raised again to exchange couple the first three dots, the original input bit has already propagated down the chain (to the sixth dot) and is decoupled from the input side since the third gate potential has been lowered in the fifth cycle, which decouples the input side from the output side. Thus, the traveling bit will not be affected by the new input. In other words, a new input bit can be fed to the spin wire *before* the earlier input makes it to the very end of the wire. Therefore, the input bits can be *pipelined*. The reader should be able to determine that in this case, the input bit rate will be only one-third of the bit flip rate and not $1/M$ times the bit flip rate where M is the number of dots in the chain ($M \gg 3$).

The pipelining however comes with a cost since gate pads must now be inserted between *every* pair of dots in order to apply a local potential between any chosen pair to exchange couple them. This scheme of clocking is called "granular clocking" since every pair has its own clock pad. This increases the fabrication complexity and cost and limits the bit density on a chip. However, the alternate is a non-pipelined architecture which will be extremely slow and hence unacceptable. Later, when magnetic quantum cellular automata architecture is discussed, it will be shown that it is possible to apply a global clock to ensure unidirectional propagation of signal in SSL. This would have doubtlessly relieved much of the fabrication burden and increased the bit density, but it would have also made the architecture non-pipelined and extremely slow.

One intriguing possibility to retain pipelining without the need to address each gate pad individually is to launch a guided electromagnetic wave in a waveguide built underneath a spin wire. When the crest of the wave arrives at a set of dots, the corresponding gate pad voltages are raised. Since one needs to raise two gate voltages at a time, the wavelength of this wave should be roughly the distance spanned by four gate pads in order to isolate bits in the pipeline. This distance may be roughly 100 nm, requiring ultraviolet waves. This idea allows pipelining of data *without* requiring separate electrical connections to every gate pad and therefore appears to be very attractive. However, this is also fraught with some danger since the magnetic field in the electromagnetic wave may interfere with the spin states.

Another possibility is to launch a traveling magnetic field pulse in a waveguide buried underneath the spin wire. This field is *not* collinear with the global field. A quantum dot positioned at the crest of this pulse experiences a net magnetic field that is at an angle with the global field. The spin in this dot will align with the local field and hence will be slanted with respect to the global field. If the input bit propagates synchronously with this pulse, it can propagate unidirectionally in the wake of the pulse. This method too does not require individual connections to every quantum dot to implement a pipelined architecture.

The Clock Speed in SSL

Once it has been established that SSL is a pipelined architecture, the writing speed, the reading speed, and the gate switching speed have to be determined next in order to ascertain which is the slowest among them. The slowest speed will determine the maximum allowable clock speed.

Writing Speed

The speed with which an input bit can be written in an input port (by aligning the spin of the lone electron in a designated quantum dot using a local magnetic field) depends on the flux density of the local field B_{input}. The stronger this field, the faster is the writing speed. The energy in this field, however, need *not* be dissipated (the energy dissipated in switching an input bit is still $g\mu_B B$ where B is the flux density of the global magnetic field that has no relation with B_{input}). Agarwal et al. [65] showed that this field must be strong enough that the Zeeman splitting it causes is

at least 20 times larger than the exchange-coupling strength between dots. The latter can be about 1 meV in semiconductor dots [73]. Therefore, in InSb quantum dot systems,

$$\begin{aligned} g\mu_B B_{\text{input}} &\geq 20 \text{ meV}; \\ B_{\text{input}} &\geq 6.94 \text{ Tesla}, \end{aligned} \tag{38}$$

where the g-factor of bulk InSb has been assumed, which is −51. The g-factor in quantum dots can be less than in bulk, which will increase B_{input}. There are some materials like $InSb_{1-x}N_x$ which reportedly have a g-factor as large as 900 in the bulk [74]. Assuming that the same g-factor can be retained in quantum dots, the value of B_{input} needs to be only ~0.4 T, if one employs $InSb_{1-x}N_x$ quantum dots as hosts for the spins. Generating field strengths of this magnitude locally is still not easy.

The time required to complete the "writing" of input bits in isolated input dots is of the order of $\sim h/(2g\mu_B B_{\text{input}})$. Using the g-factors and associated local magnetic fields that have been discussed, the writing time is found to be ~0.1 ps, which is indeed *very fast*.

Reading

There are many strategies to ascertain the spin polarization of single electrons in quantum dots [66–68], among which the scheme of Ref. [68] is best suited to SSL. In Ref. [68], the reading time was of the order of a millisecond. This time is determined by the speed with which electrons can tunnel in and out of the dot and therefore one should be able to increase this speed dramatically with better engineered structures. There does not appear to be any fundamental barrier to reducing the reading time to about 1 ns.

Gate Switching Speed

The gate switching speed is determined by how long it takes for a gate to complete a logic operation. That, in turn, depends on how fast the coupled spin system can relax to the ground state when coupled with the external thermal bath. This time is much shorter than the spin-relaxation time of a single isolated spin for essentially the same reasons that the ensemble averaged spin dephasing time of many interacting spins is orders of magnitude shorter than the dephasing time of a single isolated spin [75]. The authors are not aware of any measurement of spin-relaxation times in *coupled* (as opposed to isolated) quantum dots. However, when the magnetization of a single-domain nanomagnet (which is a system of many interacting spins) is disturbed from the ground state, it relaxes to the ground state in ~1 ns. Absent any better estimate, it appears that the gate operation time may be on the order of 1 ns.

It is clear now that among all the three switching speeds, the gate switching speed and the reading speed are the slowest and therefore will determine the clock speed. Assuming reading times and gate switching times of ~1 ns, the maximum clock frequency will be

$$f_{\text{clock}}^{\max} \approx 1 \text{ GHz}. \tag{39}$$

Gate Error Probability in SSL

There are two types of gate error in SSL: (1) the intrinsic error caused by the coupled spin system in a gate occupying thermally excited states instead of the ground state with probability p and (2) extrinsic error is caused by a spin in a dot flipping spontaneously during a clock period (due to coupling with the environment) and its probability is given by (assuming a Markovian process)

$$p_{\text{extrinsic}} = 1 - e^{-\frac{T_c}{T_1}}, \tag{40}$$

where T_c is the clock period and T_1 is the spin flip time of an *isolated* spin. Spin flip times of an isolated spin as long as 1 s has been demonstrated in GaAs quantum dots at very low temperatures of 120 mK [76] and in organic nanostructures at much higher temperatures of 100 K [77]. Assuming $T_c = 1$ ns and $T_1 = 1$ s at the operating temperature, $p_{\text{extrinsic}} = 10^{-9}$, which is acceptable. Note that for a single isolated spin, $p = p_{\text{extrinsic}}$ (since straying into the excited state invariably involves a spontaneous spin flip), but for a multi-spin system, $p \neq p_{\text{extrinsic}}$.

Temperature of Operation of SSL

Agarwal et al. [65] showed that if one wants a fixed intrinsic error probability p, then the temperature of operation is determined by the condition

$$2J = g\mu_B \left|B_{\text{global}}\right| = kT \ln\left(\frac{1}{p}\right), \tag{41}$$

where J is the energy of exchange coupling between neighboring dots. Assuming $J = 1$ meV, which is achievable with today's quantum dot technology [73], the maximum operating temperature turns out to be

$$T_{\max} \approx 1 \text{ K}, \tag{42}$$

if one operates with an intrinsic error probability of 10^{-9}. This is very low temperature and requires He^3 cooling, which is a distinct inconvenience. Room-temperature operation with such low error probability would have required exchange-coupling strengths in excess of 300 meV, which is not presently achievable with semiconductor quantum dot technology.

Had one operated at room temperature with the presently achievable $J = 1$ meV, then the bit error probability would have been $p = e^{-\frac{2J}{kT}} = 92.6$ %, which is clearly unacceptable. At 4.2 K temperature (which requires He^4 cooling instead of the more elaborate He^3 cooling), the bit error probability would have been 4×10^{-3} which may be acceptable in some situations if significant error correction resources are available.

A recent development has raised some hopes regarding higher temperature operation. It has been shown that *graphene nanoflakes* can implement SSL type logic gates with much higher exchange interaction strength ($2J = 180$ meV) which allows room-temperature operation with a bit error probability $p = e^{-\frac{2J}{kT}} = 0.1$ % [78]. This is a very exciting and promising route for SSL.

Equation 41 also yields the value of the global dc magnetic field required for operating at 1 K with an error probability of 10^{-9}. In an InSb quantum dot with $g = -51$, $|B_{\text{global}}|$ will be 0.7 T, which is easily achieved. If the quantum dot material has a g-factor of 900 [74], then the required strength of $|B_{\text{global}}|$ is only 0.04 T. These field strengths can be easily achieved with permanent magnets.

Current Experimental Status of SSL

Like the SPINFET, SSL has also never been demonstrated, but the pathways to low-temperature demonstration are clear. This architecture requires the delineation of an array of quantum dots, each containing a single electron, in specific topological patterns on a wafer. Neighboring dots must be spaced within ~10 nm to allow significant exchange coupling between nearest neighbor spins, and gate pads must be inserted between every pair of dots to allow clocking. Such systems are typically fabricated with fine-line lithography. Self-assembly, which is usually preferable over lithography for delineating quantum dots with high density, is unfortunately not easily adaptable to SSL since self-assembly is not capable of generating arbitrary geometries.

Numerous groups have demonstrated arrays of quantum dots with single electron occupancy [79] and manipulation of single electron spins in isolated quantum dots has also been demonstrated by a number of groups recently [80–89]. These results inspire hope that SSL, which only requires single electron dots with nearest neighbor exchange coupling, is within the reach of current technology. The only major challenge is the alignment of gate pads between every pair of dots with a high degree of reliability. Recent demonstration of field-effect transistors with 6 nm gate length [90] shows that lithography is advancing to the level where such challenges can be met.

Nanomagnetic Logic

The major drawback with SSL is that a single spin is not robust and hence one needs cryogenic operation to retain adequate fault tolerance (or low bit error probability). A multi-spin system, such as a single-domain nanomagnet, is intrinsically much more robust and its magnetization is very stable at room temperature. For example, consider a single-domain nanomagnet shaped like an elliptical cylinder whose

major axis is 105 nm, minor axis is 95 nm, and thickness is 6 nm. These dimensions guarantee that the magnet has but a single domain [5]. This magnet is shown in Fig. 10.

Because of the anisotropic shape, the magnetization vector of this magnet has two (mutually antiparallel) stable orientations along the easy axis, which is the major axis of the ellipse. The minimum energy barrier separating these stable states is related to the degree of shape anisotropy and is given by

$$E_b = \frac{\mu_0}{2} M_s^2 \left(N_{d-yy} - N_{d-zz}\right)\Omega, \tag{43}$$

where μ_0 is the permeability of free space, M_s is the saturation magnetization of the magnet ($\sim 5 \times 10^5$ A/m for common materials like nickel and cobalt), Ω is the nanomagnet's volume, and N_{d-yy}, N_{d-zz} are the demagnetization factors along the y- and z-axes, respectively. The demagnetization factors are given by [91]

$$\begin{aligned} N_{d-zz} &= \frac{\pi}{4}\frac{l}{a}\left[1 - \frac{1}{4}\left(1 - \frac{b}{a}\right) - \frac{3}{16}\left(1 - \frac{b}{a}\right)^2\right] \\ N_{d-yy} &= \frac{\pi}{4}\frac{l}{a}\left[1 + \frac{5}{4}\left(1 - \frac{b}{a}\right) + \frac{21}{16}\left(1 - \frac{b}{a}\right)^2\right] \\ N_{d-xx} &+ N_{d-yy} + N_{d-zz} = 1, \end{aligned} \tag{44}$$

where a is the major axis, b is the minor axis, and l is the thickness of the magnet. Note that $\Omega = (\pi/4)abl$. For the dimensions chosen, the minimum energy barrier in a nickel or cobalt nanomagnet is ~34 kT at room temperature. The probability that the magnetization will spontaneously flip in a period of time τ is $p_{\text{extrinsic}}^{\text{magnet}} = 1 - \exp[-\tau/\tau_r]$, where τ_r is the "magnetic retention time" given by $\tau_r = \tau_0 \exp[E_b/kT]$, with

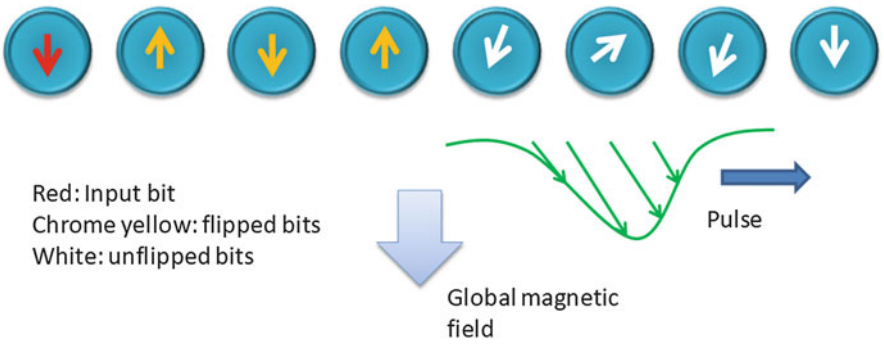

Fig. 10 A method of pipelining without requiring individual connections to each dot. A traveling magnetic pulse turns the spins of magnets within its zone of influence sideways, thereby breaking the inversion symmetry in the array and allowing bits following in its wake to travel unidirectionally

τ_0 being the "attempt frequency," which is between 1 ps and 1 ns [82]. Therefore, at room temperature ($kT = 26$ meV), τ_r is between 588 and 588,000 s since $E_b = 34\,kT$. If the clock frequency is 1 GHz or $\tau = 1$ ns, then $\tau << \tau_r$. That makes $p_{\text{extrinsic}}^{\text{magnet}} \approx \frac{\tau}{\tau_r} = \frac{\tau}{\tau_0} e^{\frac{-E_b}{kT}} \sim e^{\frac{-E_b}{kT}}$ which is $e^{-34} = 1.7 \times 10^{-15}$ at room temperature. Thus, clearly, room-temperature operation is possible with very high error resilience.

At this point, one might think that replacing a single spin with a single-domain magnet will come at the price of much higher energy dissipation. A single domain may contain ~10^4 spins, so that energy dissipated in a bit flip (in this case magnetization flip) will be 10^4 times higher than in SSL for the same error probability, i.e., the minimum dissipation will be $NkTln(1/p)$ where N (~10^4) is the number of spins in the magnet and p is the probability of flipping a single spin ($p = p_{\text{extrinsic}}^{\text{single - spin}} \approx p_{\text{extrinsic}}^{\text{magnet}}$).

In a seminal work, the authors of Ref. [4] pointed out that this line of thinking is wrong. In a single-domain magnet, all the N spins collectively behave as one giant single spin [5] and rotate together in *unison* because of the strong exchange interaction among them that keeps them mutually parallel at all times. As long as the exchange interaction strength is much larger than kT, this will happen at any temperature T. Thus, there is a single degree of freedom and *not* N independent degrees of freedom. As a result, the minimum energy dissipated to switch a single spin and a single magnet consisting of many spins is the same! This crucial realization makes the idea of replacing a single spin with a single magnet worth pursuing.

Magnet-based switches are potentially very energy efficient. In a nanotransistor, where there are N charges (information carriers) in the channel, the minimum energy dissipation will indeed be $NkTln(1/p)$, but in a single-domain nanomagnet, it can be $kTln(1/p)$. Thus, the magnet has an intrinsic advantage over the transistor, particularly when $N >> 1$.

A nanomagnet version of SSL appeared in the literature under the name "magnetic quantum cellular automata" [93]. Each nanomagnet has two stable magnetization orientations along the easy axis. If the line joining the centers of two adjacent magnets is parallel to their common easy axis, then dipole interaction between them enforces ferromagnetic ordering whereby the magnetizations of the two magnets become parallel. If that line is perpendicular to the easy axis of both magnets, then the ordering is anti-ferromagnetic, whereby the two orientations become mutually antiparallel. This is shown in Fig. 11.

Magnetic Quantum Cellular Automata

Magnetic quantum cellular automaton is a logic scheme inspired by SLL and is implemented with shape-anisotropic nanomagnets that act as logic switches. The two stable orientations of the nanomagnet's magnetization along the easy axis encode the logic bits 0 and 1. Nearest neighbor magnets are coupled by dipole interaction which enforces the ordering shown in Fig. 11. A NAND gate is realized

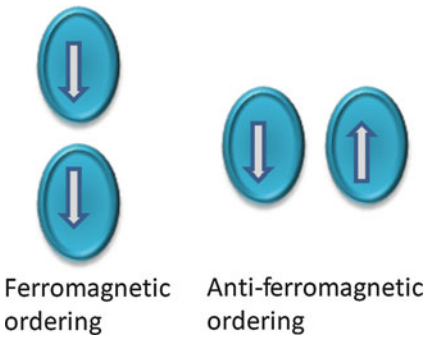

Fig. 11 A shape-anisotropic nanomagnet has two stable magnetization directions along the major axis (easy axis) which can encode logic bits 0 and 1. When the line joining the centers of two magnets is parallel to the easy axis, the ordering is ferromagnetic, but if that line is perpendicular to the easy axis, then the ordering in anti-ferromagnetic

in exactly the same way as shown in Fig. 8, with dipole interaction playing the role of exchange interaction. This system can work at room temperature with an extrinsic error probability nearly zero for a clock period of 1 ns.

There are two sources of energy dissipation in the nanomagnets: (1) the internal energy dissipated when the magnet switches magnetization (its minimum value is $kTln(1/p)$) and (2) the energy dissipation in the switching circuitry, which depends on the method of switching.

One method of switching the nanomagnets is by generating a local magnetic field in the vicinity of a magnet with a current [94]. The current flows in a loop circling the magnet. The magnetic field $\vec{H}$ generated by this current is given by Ampere's law:

$$I = \int \vec{H} \bullet d\ \vec{l}\ , \tag{45}$$

where the line integral is taken around the loop in which the current I flows.

The last equation relates the minimum current $I_{\min}$ needed to flip the magnetization to the minimum magnetic field $\vec{H}_{\min}$ that can overcome the energy barrier E_b in Eq. 43 and make the magnetization switch from one stable state to the other. One can estimate $\vec{H}_{\min}$ by equating the magnetic energy of this field to the energy barrier:

$$\mu_0 M_s |H_{\min}| \Omega = E_b \tag{46}$$

where Ω is the nanomagnet's volume. It is reasonable to assume that $E_b = 30\ kT$ at room temperature since this makes the static error probability $e^{-30} = 10^{-13}$ at room temperature, and $M_s = 10^5$ A/m (typical for cobalt or nickel). If the nanomagnet is shaped like an elliptical cylinder, the dimensions that yield this value of E_b

(see Eqs. 43 and 44) are as follows: $a = 105$ nm, $b = 95$ nm, and $l = 6$ nm. Hence, $\Omega = \frac{\pi}{4}abl = 47,000\,\text{nm}$. Equation 46 then yields the value of $|H_{\min}|$ as 21,262 A/m = 267 Oe. From Eq. 45, one gets $I_{\min} = 13$ mA, assuming the loop radius to be 100 nm. Therefore, the energy dissipated to flip a bit per clock cycle (assuming a switching time Δt of 1 ns) is $I_{\min}^2 R\Delta t = 1.7$ picoJoules $= 4 \times 10^8\ kT$ at room temperature, assuming the resistance of the loop to be 10 Ω. This is two orders of magnitude *larger* than the energy dissipated to switch a transistor in 1 ns in a circuit. Therefore, this method of switching nanomagnets is clearly energy inefficient.

A second method of switching nanomagnets is by passing a spin-polarized current through it. This either delivers a spin transfer torque [95–99] or induces domain wall motion [100], resulting in magnetization flip. The energy dissipated in this method is also of the order of $10^8\ kT$ [101] although there is a report of switching a nanomagnet with domain wall motion in ~2 ns while dissipating about $10^4\ kT$ of energy [102].

Hybrid Spintronics and Straintronics

Multiferroics are unusual magnets. A 2-phase multiferroic may consist of a single-domain magnetostrictive (magnet) layer overlying a piezoelectric layer. A tiny voltage of ~10 mV applied across the piezoelectric layer generates strain in it, which is transferred elastically to the magnetostrictive layer and rotates its magnetization by large angles. If the strain is withdrawn at the right juncture, rotation by ~180° is possible with > 99.99 % probability even in the presence of thermal noise at room temperature. The switching takes less than 1 ns, making this strategy one of the most energy-efficient switching methodology extant. Because spins are rotated with electrically generated strain, this approach was termed *hybrid spintronics and straintronics*. It is discussed next.

Consider a magnet shaped like an elliptical cylinder whose cross section is in the y-z plane. The z-axis is along the major axis of the ellipse and is the easy axis of magnetization. The stable magnetization orientations are along the $\pm z$-axis. There are two hard axes: the y-axis is the in-plane hard axis and the x-axis is the out-of-plane hard axis. Because the thickness of the magnet is much smaller than the lateral dimensions, the x-axis is "harder" than the y-axis.

The magnet is assumed to contain a *single* domain whose magnetization has a fixed magnitude at a given temperature. In the spherical coordinate system, the magnetization is directed in the radial direction. Hence, the magnetization orientation is specified by the coordinates (r, θ, ϕ), where r is fixed. The polar angle θ is the angle subtended by the magnetization vector with the $+z$-axis, and the azimuthal angle ϕ is the angle subtended by the projection of the vector on the x-y plane with the $+x$-axis. Thus, $\theta = 0°, 180°$ corresponds to the stable orientations along the easy axis, while $\phi = 90°, 270°$ corresponds to the plane of the magnet. The coordinate system is shown in Fig. 12.

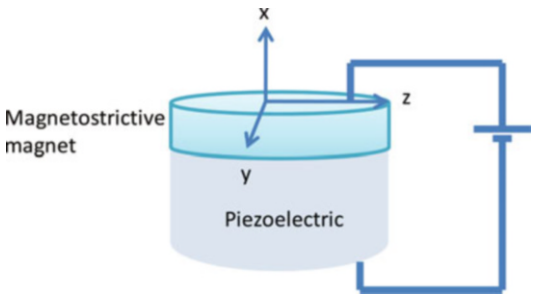

Fig. 12 A 2-phase multiferroic nanomagnet shaped like an elliptical cylinder. It consists of a magnetostrictive layer elastically coupled to a piezoelectric layer. An electrostatic potential applied across the piezoelectric generates a strain in that layer, which is transferred almost entirely to the magnetostrictive layer if the latter layer is much thinner than the former. This generates stress in the magnetostrictive layer and will rotate the magnetization away from the stable z-axis if the product of the stress and the magnetostrictive coefficient is negative. Provided the voltage is shut off as soon as the magnetization vector's projection on the y-z plane aligns along the y-axis, the magnetization vector will continue to rotate and ultimately assume an orientation antiparallel to the initial orientation, resulting in the magnetization flipping

The total potential energy of the shape-anisotropic magnetostrictive nanomagnet is the sum of shape- and stress-anisotropy energy:

$$\begin{aligned} E(t) &= E(\theta(t), \phi(t)) \\ &= \underbrace{\frac{\mu_0}{2} M_s^2 \Omega \left[N_{d-xx} \cos^2\phi(t) + N_{d-yy} \sin^2\phi(t) \right] \sin^2\theta(t) + N_{d-zz} \cos^2\theta(t)}_{\text{shape anisotropy energy}} \\ &\quad \underbrace{-\frac{3}{2} \lambda_s \sigma(t) \Omega \cos^2\theta(t)}_{\text{stress anisotropy energy}}, \end{aligned} \tag{47}$$

where λ_s is the magnetostrictive coefficient and $\sigma(t)$ is the time-dependent stress. The magnet is assumed to be polycrystalline so that magnetocrystalline-anisotropy energy can be ignored.

Because of the inequality $N_{d-xx} >> N_{d-yy} > N_{d-zz}$, it is clear that in the absence of stress, the minimum energy configurations are $\theta = 0°, 180°$ and $\phi = 90°, 270°$. Therefore, the stable orientations of the unstressed shape-anisotropic nanomagnet's magnetization are along the $\pm z$-axis. However, in the presence of stress, the minimum energy orientation will shift to $\theta = 90°$ and $\phi = 90°, 270°$ if the product $\lambda_s \sigma(t)$ is negative and the stress is sufficiently high to make

$$|3\lambda_s \sigma| > \mu_0 M_s^2 \left[N_{d-yy} - N_{d-zz} \right]. \tag{48}$$

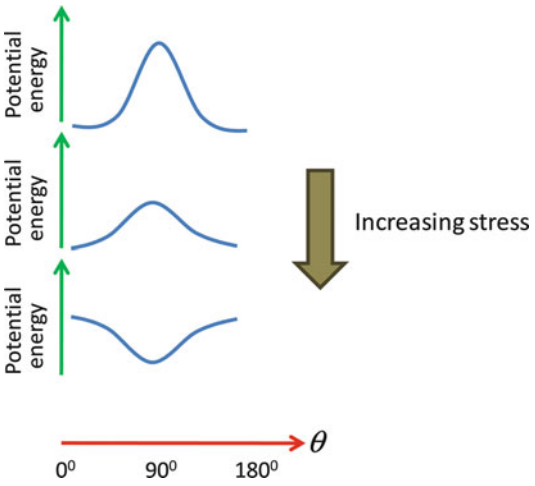

Fig. 13 Potential energy profile in the plane of the magnet ($\phi = 90°$) as a function of the polar angle θ of the magnetization vector

The potential energy profile as a function of the polar angle is shown in Fig. 13.

Thus, by applying stress, one can rotate the magnetization vector away from the stable orientation along the $\pm z$-axis.

One way to apply stress is to employ a 2-phase "multiferroic" nanomagnet consisting of a magnetostrictive layer elastically coupled to an underlying piezoelectric layer. The latter layer could be lead zirconate titanate (PZT). Application of a voltage across the PZT layer, as shown in Fig. 12, generates a strain in that layer via the d_{31} coupling. This strain is mostly transferred to the magnetostrictive layer if that layer is much thinner than the PZT layer. That strain generates a stress depending on the Young's modulus of the magnet. If the $\lambda_s \sigma$ product is negative (as per the convention used here, a tensile stress is positive and a compressive stress is negative), then the magnetization vector will rotate to $\theta = 90°$ if Eq. 48 is satisfied. This is the basis of magnetization rotation.

Logic

A logic system consists of two essential ingredients: (1) a universal logic gate such as NAND or NOR and (2) a unidirectional "wire" for communicating logic bits from one stage to the next. These two components are both necessary and sufficient to implement any combinational or sequential logic circuit.

Universal gate: An implementation of a nanomagnetic NAND gate is shown in Fig. 14. The array is placed in a global magnetic field B such that the magnetostatic energy due to this field $M_s B$ (where M_s is the saturation magnetization of the magnet) is smaller than either the shape-anisotropy energy or the dipole interaction energy. When laid out in the fashion shown in Fig. 14, dipole interaction between the magnets ensures that the output bit is always the NAND function of the two input bits for any of the four input combinations (0, 0), (0, 1), (1, 0), and (1, 1) [103].

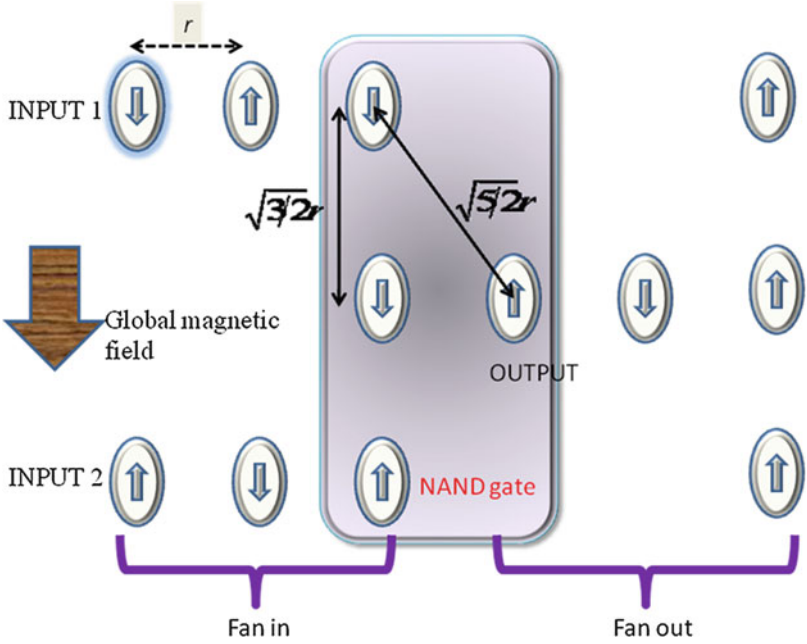

Fig. 14 A NAND gate with fan-in and fan-out. The four magnets in the shaded region implement the basic gate. Note that specific distances must be maintained between magnets to implement the gate successfully. The layout is different from the SSL NAND gate

Bits will propagate unidirectionally through this gate if the four groups of magnets (classified into groups I, II, III, and IV) are clocked sequentially with a sinusoidal 4-phase clock that are phase shifted from each other by 90° [103]. The entire gate (including fan-in and fan-out) dissipates only about 5 aJ of energy per logic operation [103].

Logic wire: A logic wire is implemented with a linear array of nanomagnets where the line joining the centers of adjacent magnets is parallel to the in-plane hard axis of the magnets (Fig. 15). Bits are propagated *unidirectionally* through the wire (or chain) by stressing the magnets sequentially pairwise using a 3-phase clock. The stress rotates the magnetization of any magnet by ~90°, aligning it temporarily along the in-plane hard axis just as shown in Fig. 15. When stress is withdrawn from the first stressed magnet, it flips up or down in response to the state of its nearest left neighbor and propagates a logic bit once cell to the right. This is termed "Bennett clocking" [104]. By repeating this sequence, a logic bit can be propagated unidirectionally through the entire chain [105].

The notable feature of this method of Bennett clocking is the ultralow energy consumed in the process. Atulasimha and Bandyopadhyay [105] showed that the voltage required to stress the magnets sufficiently for Bennett clocking is 200 mV if the magnet material is nickel. If the magnet material is Terfenol-D, which has a much larger magnetostrictive coefficient than nickel, then the voltage required

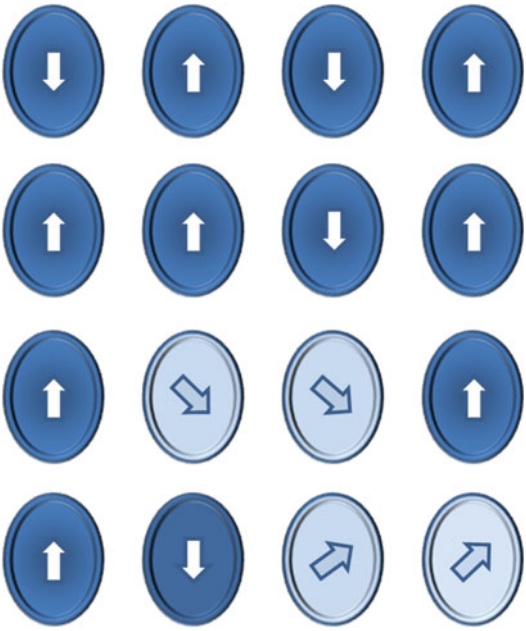

Fig. 15 Bennett clocking scheme for propagating a binary logic bit unidirectionally along a chain of nanomagnets or logic wire. (*First row*): A chain of magnets in the ground state. Dipole interaction ensures the anti-ferromagnetic ordering. (*Second row*): Magnetization of the first magnet is flipped with an external agent, but the second magnet does not necessarily respond since the dipole interactions from its left and right neighbors are equal and opposite, resulting in no net dipole interaction. (*Third row*): The second and third magnets are stressed to rotate the magnetization. The second magnet is freed from stress and it flips since the dipole interaction from its left neighbor is now stronger than that from its right neighbor. At the same time, the fourth magnet is stressed. At the end of this cycle, the input bit has propagated through the first magnet on the right. By repeating this cycle, the bit can be progressively propagated to the right unidirectionally

reduces to ~10 mV. This low voltage results in very low energy dissipation in switching.

In order to calculate the energy dissipation as a function of switching speed, one needs to solve the Landau-Lifshitz-Gilbert (LLG) [9] equation that describes the magnetization dynamics. This equation governs the magnetization rotation under the torque generated by shape and stress anisotropy. This torque is given by

$$\vec{T}_E(t) = \hat{e}_r \times \vec{h}_{eff}(t) = -\hat{e}_r \times \vec{\nabla} E(\theta(t), \phi(t)), \tag{49}$$

where $\hat{e}_r$ is the unit vector along the radial direction (direction of magnetization), $\vec{h}_{\text{eff}}(t)$ is an effective magnetic field due to shape and stress anisotropy, and the gradient is taken in $\theta -$ and $\phi -$ space.

At room temperature, thermal noise generates an additional torque given by [106]

$$\vec{T}_{th} = M_v \hat{e}_r \times \vec{h}_{th}(t), \tag{50}$$

where

$$\begin{aligned} \vec{h}_{\text{eff}}(t) &= h_x(t)\hat{x} + h_y(t)\hat{y} + h_z(t)\hat{z} \\ h_i(t) &= \sqrt{\frac{2\alpha kT}{|\gamma|(1+\alpha^2)M_v \Delta t}} G_{0,1}(t), \end{aligned} \tag{51}$$

where α is a phenomenological constant known as the Gilbert damping constant [9], kT is the thermal energy at temperature T, γ is the gyromagnetic ratio equal to $g\mu_B\mu_0/\hbar$ (g = Lande g-factor of the magnet, μ_B is the Bohr magneton), $M_v = \mu_0 M_s \Omega$, Δt is proportional to the inverse of the attempt frequency for thermal noise to disrupt magnetization, and $G_{0,1}(t)$ is a Gaussian distribution with zero mean and unit standard deviation.

From Eqs. 47 and 49, one gets

$$\begin{aligned} \vec{T}_E(t) = &-\left\{\frac{\mu_0}{2} M_s^2 \Omega \left[N_{d-xx}\cos^2\phi(t) + N_{d-yy}\sin^2\phi(t) - N_{d-zz}\right] + \frac{3}{2}\lambda_s \sigma(t)\Omega\right\} \sin(2\theta(t))\hat{e}_\phi \\ &-\frac{\mu_0}{2} M_s^2 \Omega \left(N_{d-xx} - N_{d-yy}\right) \sin(2\phi(t)) \sin\theta(t)\hat{e}_\theta \end{aligned} \tag{52}$$

where $\hat{e}_\phi$ and $\hat{e}_\theta$ are the unit vectors in the ϕ- and θ-direction, respectively.

Similarly, one can write

$$\begin{aligned} \vec{T}_{th}(t) &= P_\theta(t)\hat{e}_\phi - P_\phi(t)\hat{e}_\theta \\ P_\theta(t) &= M_v\left[h_x(t)\cos\theta(t)\cos\phi(t) + h_y(t)\cos\theta(t)\sin\phi(t) - h_z(t)\sin\theta(t)\right] \\ P_\phi(t) &= M_v\left[h_y(t)\cos\phi(t) - h_x(t)\sin\phi(t)\right]. \end{aligned} \tag{53}$$

The so-called stochastic LLG equation [107] describes the temporal evolution of the magnetization vector according to

$$\frac{d\vec{n}_m(t)}{dt} - \alpha\left(\frac{\vec{n}_m(t) \times d\vec{n}_m(t)}{dt}\right) = -\frac{|\gamma|}{M_v}\left[\vec{T}_E(t) + \vec{T}_{th}(t)\right], \tag{54}$$

where $\vec{n}_m(t)$ is the unit vector along the magnetization direction. This equation yields the following coupled equations for the time evolution of $\theta(t)$ and $\phi(t)$:

$$(1+\alpha^2)\frac{d\theta(t)}{dt}=\frac{|\gamma|M_s\Omega}{2}\begin{bmatrix}\alpha\left(N_{d-xx}-N_{d-yy}\right)\sin\left(2\phi(t)\right)\\+\left\{N_{d-xx}\cos^2\phi(t)+N_{d-yy}\sin^2\phi(t)-N_{d-zz}+\frac{3\lambda_s\sigma(t)}{\mu_0M_s^2\Omega}\right\}\cos\left(\theta(t)\right)\\-\frac{2}{\mu_0M_s^2\Omega^2\sin\theta(t)}\left(P_\theta(t)-\alpha P_\phi(t)\right)\end{bmatrix}$$

$$(1+\alpha^2)\frac{d\phi(t)}{dt}=\frac{|\gamma|M_s\Omega}{2}\begin{bmatrix}\left(N_{d-xx}-N_{d-yy}\right)\sin\left(2\phi(t)\right)\sin\theta(t)\\-\alpha\left\{N_{d-xx}\cos^2\phi(t)+N_{d-yy}\sin^2\phi(t)-N_{d-zz}+\frac{3\lambda_s\sigma(t)}{\mu_0M_s^2\Omega}\right\}\sin\left(2\theta(t)\right)\\+\frac{2}{\mu_0M_s^2\Omega^2}\left(\alpha P_\theta(t)+P_\phi(t)\right)\end{bmatrix} \tag{55}$$

Error Rates in Magnetic Quantum Cellular Automata

The major drawback of architectures like magnetic quantum cellular automata that rely on dipole coupling between neighboring magnets for information transmission is the high error rate associated with switching. When the magnetization vector of a nanomagnet switches from one orientation (logic 0) to the other (logic 1), it invariably lifts out of the plane of the magnet before it settles down to the desired orientation in the plane. The out-of-plane excursion can be erratic and error prone in the presence of thermal noise. Error occurs when the magnetization vector fails to flip and returns to the original orientation. Stronger dipole coupling between neighbors should reduce this error by increasingly preferring anti-ferromagnetic ordering between neighbors, but regrettably dipole coupling can never be strong enough to ensure this for reasonable parameters (magnet volume, inter-magnet spacing, etc.).

This problem has been studied by a number of authors [107–111], who have all concluded that the error rate is unacceptably high for Boolean logic. Boolean logic typically would require the error probability in a switching event to remain below $\sim 10^{-15}$, while most simulations predict the switching error probability at room temperature in a nanomagnet dipole coupled to its neighbor to be as high as 0.1 % for slow switching (~10 ns). Faster switching increases the error probability and makes it approach 100 % for very high speeds.

It is quite possible that because of the impractical error probabilities, magnetic quantum cellular type of architectures may be doomed as far as Boolean logic is concerned. However, there are other non-Boolean architectures for computing that may benefit immensely from dipole-coupled magnets that act as binary switches and process information in the manner of neuromorphic systems or Bayesian networks. After all, magnets have one unbeatable advantage: very low energy dissipation during switching.

Memory

A memory element implemented with a multiferroic nanomagnet is shown in Fig. 16. The bit information is stored in the magnetization orientation of the soft

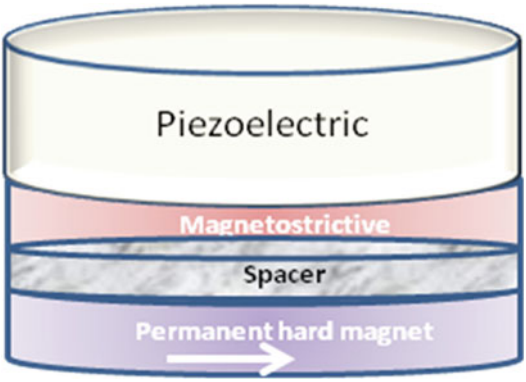

Fig. 16 A multiferroic memory element. The bit is stored in the magnetization orientation of the soft magnetostrictive layer. The spin-valve structure comprising the bottom three layers are used to "read" the stored bit. Writing of bits in the magnetostrictive layer is accomplished by applying a potential between the top and bottom of the structure to flip the magnetization of the soft layer, if necessary

magnetostrictive magnet shaped like an ellipsoidal cylinder. The two (mutually antiparallel) orientations along the major axis of this magnet are the stable states and encode bits 0 and 1.

In order to **read** a stored bit (or the magnetization orientation of the soft magnetostrictive layer), a "spin valve" is used. This structure consists of the soft magnetostrictive layer separated from a permanently magnetized hard magnet by a thin spacer layer. Let us say that the magnetization orientation of the hard permanent magnet represents bit 1. If the soft layer stores bit 1, its magnetization will parallel to that of the hard layer and the vertical resistance of the spin-valve structure will be small. If the soft layer stores bit 0, its magnetization will be antiparallel to that of the hard layer and the spin-valve's resistance will be larger. Thus, by measuring the spin-valve's ac resistance with a small signal, one can read the stored bit.

For **writing**, the stored bit is first read. If it is the desired bit, no action is taken. Otherwise, the bit is flipped by applying a potential between the top piezoelectric layer and the permanent hard magnet. This potential is dropped mostly across the piezoelectric since the magnets are metallic and the spacer layer is ultrathin.

One important issue is that dipole interaction between the soft layer and hard layer will be very strong in this configuration since they are separated by an ultrathin layer of spacer material. This will make it very difficult to write bit 1 in memory since one will have to overcome the dipole interaction energy plus the shape-anisotropy energy with stress, and the former will be very strong. In order to mitigate this problem, one typically uses a synthetic antiferromagnet (SAF) as the hard magnet. It consists of two anti-ferromagnetically coupled layers (the top layer is the hard magnet) separated by a thin Ru layer.

In order to write bits in memory, stress generated by the applied voltage should be able to not only rotate the magnetization of the soft magnetostrictive layer, but

rotate it by 180°, resulting in a bit flip. Solution of Eq. 55 shows that this is indeed possible if the stress is withdrawn as soon as the angle θ reaches 90°. This was shown rigorously in Ref. [108].

The power dissipated internally in the magnet during a bit flip (while writing a bit) is given by

$$P_d(t) = \frac{\alpha|\gamma|}{(1+\alpha^2)M_v}\left|\vec{T}_E(t)\right|^2. \tag{56}$$

The thermal torque does not dissipate any power since its time average is zero. The energy dissipated internally during the switching is

$$E_d = \int_0^\tau P_d(t)dt, \tag{57}$$

where τ is the time is takes to flip the magnetization.

The total energy dissipated during switching has two components: (1) the internal energy E_d and (2) the external energy $(1/2)CV^2$ dissipated in the switching circuit that applies the voltage to generate the stress. The external energy can be reduced further by switching slowly or adiabatically, but at the expense of decreased switching speed.

Energy Dissipation in Straintronics

Roy et al. [112] and later work by Salehi-Fashami et al. have shown that the total energy dissipated per bit flip is about 400 kT at room temperature if the magnet is switched in ~1 ns. Thus, in a chip with 10^8 logic switches per square centimeter, the power dissipated is 17 mW/cm^2 at a clock rate of 1 GHz, if 10 % of the devices switch at any given time (10 % activity level). This opens up unprecedented applications. Chips with such low power requirements can run by scavenging energy from the environment without requiring a battery. There are numerous energy harvesting schemes that can harvest this level of energy from energy radiated by cable TV and 3G networks [113, 114]. Furthermore, devices of this type are ideally suited for medically implanted devices, such as processors implanted in an epileptic patient's brain that monitor brain signals and warn of an impending seizure. These processors can run by harvesting energy from the patient's head movements or from electromagnetic radiation in the environment, without every requiring a battery. Another possible application of such processors is in distributed sensor networks for structural health monitoring that can run off the power harvested from mechanical vibrations in the structure (buildings, bridges) induced by wind or passing traffic.

All-Electrical Spintronics

All-Electrical Spintronics Using Quantum Point Contacts (QPCs)

One of the most important challenges facing spintronics is the creation, manipulation, and detection of spin-polarized currents by *purely electrical* means. Since spin-orbit coupling (SOC) couples electron orbital motion to its spin, there is an ongoing effort to harness SOC as a possible tool for all-electrical spin control and generation of spin-polarized current without ferromagnetic contacts and applied magnetic fields. The Rashba spin-orbit coupling phenomenon [7, 115] (RSOC) has been the focus of intense research in recent years [116, 117], but despite all that effort, there has been no successful demonstration of unambiguous spin injection or control by RSOC.

Over the last few years, several groups have investigated the effects of SOC induced by the transverse in-plane electric field due to the gradients of the lateral confining potential of a quantum wire [118]. This mechanism is referred to as *lateral spin-orbit coupling* (LSOC). It is distinctly different from RSOC, which arises from an electric field due to the asymmetry in the confining potential of a quantum well (QW) structure. Several recent theoretical reports have shown that LSOC can induce accumulation of opposite spin species on opposite edges of a quantum wire when a current flows through it [119–121]. None of these theoretical efforts, however, predicts a *net* spin polarization that can generate a spin-polarized current.

Spin Polarization Using Quantum Point Contacts (QPCs)

There is now mounting evidence that a net spin polarization could be achieved by electrical means through the use of QPCs. For more than a decade, there have been experimental reports of anomalies in the quantized conductance of QPCs. These anomalies appear at non-integer multiples of the conductance quantum $G_0 = (2e^2/h)$. Examples of them include the observation of anomalous conductance plateaus around 0.5 and $0.7G_0$. (For a review, see [122–126]). There is a growing consensus that these conductance anomalies are indirect evidence for the onset of spontaneous spin polarization in the narrow portion of the QPC [127–134]. There is also mounting evidence that the number and location of the conductance anomalies can be further tuned by deliberately introducing a broken symmetry in the electrostatic confinement in the narrow portion of the QPC [135, 136]. More recently, the change in the impurity potential in a GaAs QPC, with an asymmetric lateral confinement due to an offset bias between two split gates, has been shown to affect the location of the conductance anomalies strongly [137].

0.5 Conductance Plateau in QPCs with Lateral Spin-Orbit Coupling (LSOC)

Recently, Debray et al. [138] showed that the lateral spin-orbit coupling (LSOC), resulting from the lateral in-plane electric field of the confining potential of an in-plane side-gated QPC, can be used to create a strongly spin-polarized current by purely electrical means *in the absence of any applied magnetic field*. The semiconductor structures used in their work were *symmetric* InGaAs/InAs QW structures with a two-dimensional electron gas (2DEG) in the InAs quantum well. The low band-gap semiconductor InAs has a large intrinsic SOC, more than an order of magnitude larger than that in GaAs. Hall measurements at 4.2 K gave a 2DEG mobility of 10^5 cm^2/Vs and a sheet electron density of 1.2×10^{12} cm^{-2}. The electron mean free path of the 2DEG was about 2 μm at 4.2 K. The spin coherence length was a few μm at this temperature. Side-gated single and dual QPC devices were made using state-of-the-art nanofabrication techniques on length scales smaller than both the electron mean free path and the spin coherence length to ensure ballistic, spin-coherent transport. A side gate is just a piece of the 2DEG isolated from the conduction channel by deep trenches cut by wet etching. Figure 17 shows the scanning electron micrograph (SEM) image of a QPC. The effective channel width of a QPC is controlled by appropriately voltage-biasing the side gates.

Figure 18a shows representative plots of measured conductance at 4.2 K of QPC devices as a function of sweeping voltage V_G, applied simultaneously to all the gates. A negative voltage was applied to reduce the channel width and ultimately pinch the device off. A short plateau at conductance G $\cong 0.5(2e^2/h)$ was observed *in the absence of any applied magnetic field* when the lateral confining potential of the QPC was made significantly *asymmetric* by applying appropriate bias voltages to the side gates. The asymmetry is arbitrarily referred to as "forward" when the lower side gate is at a potential higher than the upper side gate and "reverse" when it is the

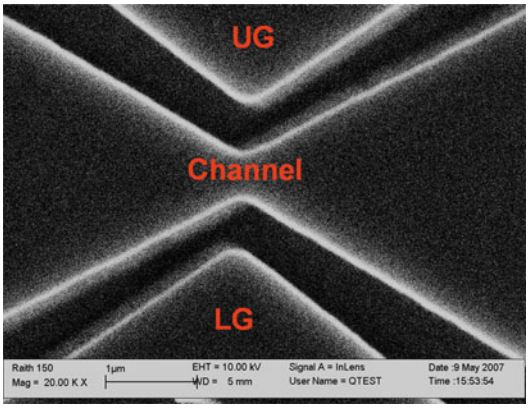

Fig. 17 SEM image of a QPC device, created by the side gates UG and LG. *Dark areas* are isolation trenches cut by wet etching

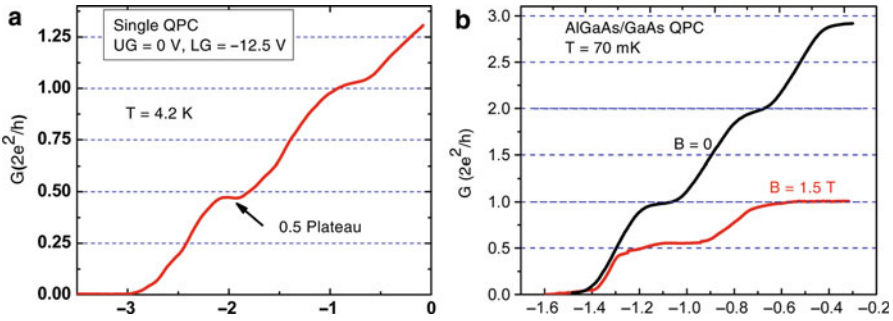

Fig. 18 (**a**) Representative plot of conductance G of InAs QPC devices measured at a reverse asymmetry of 12.5 V, showing the 0.5 plateau. (**b**) Conductance G of a GaAs QPC, showing the Zeeman spin splitting of the first quantized conductance plateau in an external magnetic field (B). V_G is the sweeping voltage applied simultaneously to all gates

opposite. The 0.5 plateau was also observed when the asymmetry of the confining potential was reversed by reversing the gate bias voltages. The plateau survives up to about 13 K. *The 0.5 feature was absent when the confining potential was made symmetric*.

The quantization of the conductance results in a conductance staircase as the Fermi level is made to sweep across the 1D subband bottoms either by changing the electron density or by changing the width of the wire by applied gate bias voltages. When the spin degeneracy is removed, e.g., by a strong external magnetic field B, the conductance is quantized at integral values of $0.5G_0$. The spin splitting of the first quantized plateau observed in a GaAs QPC in applied magnetic field is shown in Fig. 18b. The occurrence of a plateau at $G = 0.5G_0$ in the conductance is a signature of complete spin polarization [128]. Wan et al. used a nonequilibrium Green's function (NEGF) to analyze the experimental data of Debray et al. while modeling a small QPC [139, 140] and showed that three ingredients were essential in generating a strong spin polarization: (1) an asymmetric lateral confinement, (2) a LSOC induced by the lateral confining potential of the QPC, and (3) a strong electron–electron (e-e) interaction. Actually, extensive NEGF simulations carried out for a wide range of QPC dimensions and biasing parameters reveal the appearance of many conductance anomalies at non-integer values of $G_0 = 2e^2/h$, besides the 0.5 plateau. The number of coexisting conductance anomalies increases with the aspect ratio of the QPC. These anomalies are related to a plethora of spin textures in the narrowest part of the QPC which show either a Spin Hall regime or the presence of a leaky single qubit state, developing first into a leaky singlet state and then into a leaky spin-density wave in the channel as the QPC aspect ratio increases [140]. Analysis suggests that the conductance anomalies reported by many experimental groups using different QPC designs and biasing conditions are most likely fingerprints of complex spin textures that result from a combination of large device aspect ratio, spatial asymmetry in the QPC confining potential, and the presence of strong e-e interaction [122–136].

Outlook

The study of the electrical control of the conductance of single QPCs, with the use of asymmetrically biased split gates or side gates, is of practical importance since this would provide the means to create a perfect spin polarizer and analyzer. This is of practical importance since the spin polarization of two QPCs in series could be tuned for either spin up or spin down injection, opening the path for the realization of an all-electric spin valve. The resulting on-/off-conductance ratio of that spin valve could be further controlled by the addition of side gates acting on the channel between the two QPCs. As has been repeatedly shown in this chapter, the tallest roadblock in the path of spintronics is the poor spin injection/detection efficiencies that bedevil almost every spintronic device starting from the SPINFET and even spin-based magnetic field sensors [141–143]. Even nanomagnetic logic and memory schemes suffer from this malady since reading of nanomagnetic logic bits (or stored memory bits) requires spin valves with high on/off ratios that can come about only from high spin injection and detection efficiencies. Thus, the ability to inject and detect spin with high efficiency is of paramount importance.

Conclusion

In this chapter, a family of spintronic devices and architectures has been discussed, concluding with the prognosis for all-electrical spintronics. Much progress has been made and much remains to be made, but the vast resources that have been invested in spin-based electronics have already begun to bear some fruit. The allure of spintronics will always remain in view of the extreme energy efficiency that spin-based logic schemes promise, and it remains to be seen how much of that promise can be realized in the short term.

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