Chapter 8
Conclusions and Future Work

The final goal of this thesis was the fabrication of a CMOS-integrated piezoresistive pressure sensor. SiGe MEMS was selected as the technology platform in which to reach this goal. This dissertation provides all the steps for the successful design and fabrication of MEMS pressure sensors directly on top of their readout circuitry, allowing for smaller chips. The monolithic integration of MEMS on top of CMOS is also expected to improve the signal/noise ratio as compared to the traditional hybrid approaches: by processing the pressure signal in close proximity to the transducer, the parasitics introduced by the IC-MEMS interconnects and the effect of external noise can be greatly reduced. In this chapter an overview of the key aspects and contributions of this dissertation is presented, together with a list of recommendations to further improve the technology and the performance of the fabricated devices.

8.1 Conclusions and Contribution of the Dissertation

The primary contribution of this work is the realization of an integrated poly-SiGe-based piezoresistive pressure sensor directly fabricated above 0.13 μm Cu-backend CMOS technology. This represents not only the first integrated poly-SiGe pressure sensor directly fabricated above its readout circuit, but also the first time that a poly-SiGe MEMS device is processed on top of Cu-backend CMOS.

As explained in Chap. 1, polycrystalline SiGe has emerged as a promising MEMS structural material since it provides the desired mechanical properties at lower temperatures compared to poly-Si, allowing the post-processing of MEMS on top of CMOS. Of the different existing approaches for CMOS-MEMS monolithic integration, the MEMS-last approach is the most interesting one as it leads to smaller die areas and enables integrating the MEMS without introducing any changes in standard foundry CMOS processes. Compared to alternative technologies, for example using the CMOS top interconnect layers to fabricate the MEMS device, poly-SiGe offers a more generic and flexible technology for above CMOS integration, thanks

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to the fact that the MEMS fabrication can be completely decoupled from the CMOS fabrication.

In the past, imec already proved the potential of poly-SiGe for MEMS-above-CMOS integration by presenting, for example, an integrated poly-SiGe micromirror array and an integrated gyroscope, both of them fabricated on top of Al-based CMOS (from an external foundry). However, the aggressive interconnect scaling, essential to the continuation of Moore's law, has led to the replacement of the traditional aluminum metallization by copper metallization, due to its lower resistivity and improved reliability. The results obtained in this work demonstrate that the poly-SiGe MEMS process flows are also compatible with post-processing above Cu-based CMOS, broadening the applications of poly-SiGe to the integration of MEMS with the advanced CMOS technology nodes.

The described integrated sensor (fully fabricated in imec) includes a surface-micromachined piezoresistive pressure sensor, with a poly-SiGe membrane and four poly-SiGe piezoresistors, and an instrumentation amplifier fabricated using imec's 0.13 μm CMOS technology, with Cu-interconnects (two metal layers) and Si-oxide dielectric. Several steps were completed to realize the integrated pressure sensor. These steps comprised: development of a poly-SiGe piezoresistive layer to be used as sensing element in the pressure sensor, modeling and design of the sensors using FEM (Finite Element Methods), process development, fabrication and testing of the designed MEMS sensors, design of a readout circuit for the sensors and finally, proving the CMOS compatibility of the developed MEMS technology by fabricating the MEMS sensors directly on top of the CMOS readout circuit.

Other contributions of this work include the study, for the first time, of the piezoresistive properties of poly-SiGe. Also, never befefore was poly-SiGe used both as structural and sensing layer for MEMS pressure sensor applications. Moreover, together with the piezoresistive pressure sensors, also functional capacitive pressure sensors were succesfully fabricated on the same wafer, proving the versatility of poly-SiGe for MEMS sensor applications.

All of these key developments were addressed in detail in the different chapters of this thesis.

1. *Study of the electrical and piezoresistive properties of poly-SiGe*. Chapter 2 presents a detailed investigation on the influence of deposition conditions, germanium content and doping concentration on the electrical and piezoresistive properties of boron-doped poly-SiGe. The studied electrical properties include resistivity and temperature coefficient of resistance. Four different poly-SiGe layers were characterized. First, a heavily doped CVD poly-$Si_{24}Ge_{76}$, deposited at 450 °C was considered. This layer is used as the standard electrode layer in the SiGe-MEMS platform in imec. The layer exibitted a resistivity lower than 1 mΩ cm, a TCR of only 2.7×10^{-4} °C^{-1} and a gauge factor of 2.8. This gauge factor, although comparable to the gauge factor found for a similarly doped poly-Si layer (G = 4.2), is low for typical piezoresistive applications. Next, the piezoresistive and electrical properties of poly-$Si_{51}Ge_{49}$ and poly-$Si_{36}Ge_{64}$ for different doping concentrations (from 5×10^{17} to 1×10^{20} cm^{-3}) were evaluated.

Similar as for poly-Si, the gauge factor of poly-SiGe is found to tail off for low and high boron concentrations, reaching a maximum for a boron concentration around $1 \times 10^{19} \text{cm}^{-3}$. This optimum boron concentration also corresponds to a very low TCR, which is ideal for piezoresistive sensors applications. However, the processing temperatures used during the deposition and annealing of these layers were too high (above 500 °C) to allow for the monolithic integration of MEMS above CMOS. For this reason, a new poly-SiGe layer (Ge∼77 %), deposited at 450 °C and annealed at 455 °C was developed to be used as sensing layer in the pressure sensors. A maximum gauge factor of ∼15 was obtained, which is somewhat smaller than reported maximum values for poly-Si. However, the possibility to post-process on top of CMOS still makes poly-SiGe a very interesting material for MEMS piezoresistive sensors as monolithic integration leads to a higher signal/noise ratio which might offset the slightly smaller gauge factor.

2. *Design of poly-SiGe based piezoresistive pressure sensors* (Chap. 3). Finite element simulations are used together with the experimentally obtained piezoresistive coefficients for poly-SiGe (Chap. 2) to predict the impact of the design parameters on sensor sensitivity and linearity. The design parameters include membrane area and shape and piezoresistors location, shape and dimensions. Finally, two membrane shapes (square and rectangular), four membrane areas (200×200, 250×250, 300×300 and $350 \times 175\,\mu\text{m}^2$) and six different piezoresistor designs were included in the layout (Appendix A).
3. *The pressure sensor fabrication process*. The considered pressure sensors consist in a deformable poly-SiGe membrane, supported by a 25 µm-wide anchor ring, and four poly-SiGe piezoresistors placed on top following a Wheatstone bridge configuration. To enable above-CMOS integration the maximum processing temperature of the complete sensor, including the poly-SiGe piezoresistors, is kept ≤ 455 °C. A thin SiC isolation layer is included between the SiGe membrane and the SiGe piezoresistors. Also, to protect the electronic circuit from the aggressive etch and deposition steps which are needed to fabricate the MEMS devices, a SiC passivation layer was included. SACVD Si-oxide was used to seal the released (in vHF) membranes. The whole process sequence requires nine lithographic masks and more than 100 operations. The maximum process temperature was 455 °C, and corresponds to the SiGe depositions and the different annealing steps (for example after piezoresistor implantation for dopant activation) included during the flow. In total, during the processing of the MEMS pressure sensors on top of the read-out circuit, the CMOS will withstand a maximum temperature of approximately 455 °C for ∼8.5 h.
4. *Sealing process development*. The sealing process is one of the most important steps in the fabrication of a pressure sensor. For this reason a whole chapter of this thesis (Chap. 5) is dedicated to it. The most important requirements a sealing layer must fulfil are: provide a hermetic sealing of the cavity with a stable, preferably low, sealed-in pressure. Two different sealing techniques involving thin-film deposition are investigated: direct sealing and sealing using an intermediate porous layer. The sealing materials studied include Si-oxide and

sputter-deposited AlCu. To verify the sealing process, optical measurements of membrane deflection were carried out both in air and in vacuum. Analytical modelling and Finite Element Methods (FEM) were used to study the load-deflection behaviour of the (poly-SiGe/sealing layer) composite membranes and derive the overall stress and the pressure inside the cavities. The experimental results prove that both Si-oxide and AlCu can provide short- and long-term air-tight sealing. The use of a porous cover, although preventing the deposition of sealing material inside the cavity, resulted, for the cavities studied in this work, in a higher sealed-in pressure. Although direct sealing with AlCu provides a near-vacuum sealed cavity, its use for piezoresistive pressure sensors is not immediate as an extra isolation layer and/or extra processing steps might need to be introduced to avoid a short-circuit between piezoresistors. Finally, SACVD Si-oxide was the selected sealing layer for the pressure sensors since it represents a simple technique for the direct sealing of the sensors, with a resulting cavity pressure below 10 kPa and a marginally tensile stress in the sealed membrane.

5. *Experimental characterization of the fabricated MEMS pressure sensors*. In Chap. 6, the realized stand-alone poly-SiGe pressure sensors (both piezoresistive and capacitive) were evaluated in the pressure range from 0 to 1 bar. Sensitivities between 1.5 and 5.5 mV/V/bar have been obtained for the piezoresistive sensors, with nonlinearity errors below 4 %. In general, good qualitative agreement with the simulations in Chap. 3 is observed. The temperature dependence of the sensors was also characterized in the temperature range of 25 to 125 °C, leading to a temperature coefficient of sensitivity (TCS) in the range of −1000 to −2000 ppm/°C. The fabricated sensors exhibited very high voltage offsets with a large spread: values between −182 and 105 mV (for an input voltage of 3.3 V) were measured.
   For the capacitive pressure sensors, the impact of sensor membrane area, bottom electrode area and electrode/membrane gap on the sensor sensitivity was characterized. The highest measured sensitivity in this work is 73±3 fF/bar, and corresponds to a $200 \times 200\,\mu m^2$ sensor with a gap of 1 μm and an electrode of $150 \times 150\,\mu m^2$. If higher sensitivities are required, an array of such sensors could be used. Thanks to the low processing temperature of the described sensor, relative large arrays can be integrated with the readout electronics without extra die consumption. Moreover, this type of sensors is expected to benefit more from the parasitic reduction thanks to the above-CMOS integration than the piezoresisitve counterparts.
6. *Fabrication and evaluation of CMOS-integrated pressure sensors*. An instrumentation amplifier was designed to be used as the readout circuit for the piezoresistive pressure sensors. Two versions of the amplifier were implemented: with fixed and variable gain. The circuit was fabricated using a modified version of imec's 0.13 μm technology, with thicker gate oxide to allow for higher operating voltages (3.3 V instead of 1.2 V). The CMOS included two copper-based interconnect layers, with Si-oxide dielectric and Cu-filled metal-to-metal vias. To connect the top Cu-based CMOS metal layer and the bottom Al-based MEMS electrode, tungsten-filled vias were employed. The CMOS circuit showed no

significant deterioration after the MEMS processing, although an increase of $\sim$22 % in the CMOS-MEMS via resistance was observed. Only one integrated sensor could be properly evaluated. The poly-SiGe piezoresistive sensor alone ($250 \times 250\ \mu m^2$ membrane) showed a sensitivity of around 2.5 mV/V/bar. The integrated sensor (same sensor + Cu-based CMOS amplifier underneath) showed a sensitivity $\sim$159.5 $\pm$ 1 mV/V/bar, $\sim$64 times higher than the stand-alone sensor.

8.2 Future Research Directions and Recommendations

Although the developed poly-SiGe technology was successfully used to fabricate stand-alone MEMS pressure sensors, and the compatibility of the presented MEMS fabrication flow with CMOS was demonstrated through a functional integrated piezoresistive pressure sensor directly fabricated on top of its readout circuit, there is still room for improvement.

A better understanding of the poly-SiGe piezoresistors is needed. Characteristics such as noise and temperature coefficient of the gauge factor were not studied in this work. These material characteristics are important for the performance of piezoresistive pressure sensors as they contribute to define the minimum detectable pressure and resolution of the sensor, and the temperature coefficient of sensitivity. Also the nonlinearity of the piezoresistive response should be evaluated. In addition, it could be useful to develop an analytical model for the poly-SiGe piezoresistivity, similar to the model developed for poly-Si. Further improvement of the layer gauge factor by tuning the deposition and/or annealing conditions might also still be possible.

Despite not being designed for any specific application, the performance of the fabricated pressure sensors is comparable to commercially available devices. Only the offset voltage and the nonlinearity (NL) seem to be out of range. The reason for the high offset voltages is not yet fully understood. One possible reason could be the bad aluminum filling of the piezoresistor contacts. A bad filling of the contacts can translate into high contact resistance, and also lead to a large spread in the contact resistance values which might explain the high offset voltages. Test structures to better characterize the piezoresistor contact resistance should be designed, and different materials and/or deposition conditions could be studied to improve the contact filling. Also the uniformity of the poly-SiGe piezoresistive layer should be improved to reduce the offset voltage. In this sense, work at imec is ongoing to transfer the CVD part of the SiGe deposition process from the current PECVD tool to a CVD tool; an improvement in the uniformity of the SiGe layers is expected as a result. Finally, different sensor designs, based on a local stiffening of the membrane while the resistors are kept in a local stress concentration area, could be implemented to improve the linearity while minimizing the sensitivity loss.

On the other hand, by substituting the SACVD oxide by a sealing layer with a coefficient of thermal expansion (CTE) closer to the CTE of the poly-SiGe structural layer (for example using SiGe also as sealing layer), the temperature coefficient of sensitivity of the sensors could also be reduced. It would also be beneficial to

have vacuum-sealed cavities, as this will eliminate the trapped gas effects. Finally, a barrier coating (for example SiC or SiN) should be deposited on top of the metal interconnects to avoid corrosion.

Moreover, reliability tests of the fabricated pressure sensors should be performed. Important parameters, such as maximum allowed pressure or the operating temperature range were not determined. Also the repeatability of the sensor performance was not evaluated. The environment the piezoresistive sensors may be exposed to, depending on the application, may include cyclic or steady-state temperature, static or dynamic pressure, harsh media, vibration, and/or electric fields. To be assured that the sensor can sustain the environment, reliability testing should include media compatibility (i.e. exposure to fuel, water or strong acids), pulsed pressure with a cyclic temperature and bias, high and low temperature storage, high humidity exposure, and temperature cycling.

On the other hand, due to the limited time, the performance of the integrated sensors was evaluated only in terms of pressure response. A complete evaluation should include other important performance parameters like temperature drift and signal-to-noise ratio (SNR). Especially the SNR could be an important indicator to evaluate if the parasitic reduction thanks to the CMOS-monolithic integration really results in the promised improved performance with respect to the traditional hybrid integration.

A detailed study of the advantages offered by the above-CMOS integration is also missing in this work. From the fabricated devices, only the area reduction advantage can be appreciated. The supposed parasitic reduction and improved signal-to-noise ratio should be proven. For that purpose, specific structures were included in the layout to compare the hybrid versus monolithic integration approach; however, due to time limitations, this study could not be realized. The focus of this study was piezoresistive pressure sensors, and therefore little attention was paid to capacitive sensors. However, the benefits of above-CMOS monolithic integration, like for example the parasitic reduction, could be more obviously tested with an integrated capacitive sensor. Therefore, for a future work focusing on the advantages of monolithic over hybrid integration, capacitive pressure sensors, or also an RF MEMS device, would be a more suitable demonstrator.

Finally, a more complete readout circuit for the sensors is necessary. The simple readout circuit proposed in this work (just an amplifier) might be enough for a first demonstrator, but for real commercial applications, the circuit should include temperature compensation, offset calibration, etc. Also, the CMOS used in this work employs Si-oxide as dielectric layer. In standard copper-based advanced CMOS technologies, the low-permittivity dielectrics utilized in the metallization stack are less tolerant of post-deposition annealing, which might further restrict the thermal budget for the MEMS processing ($\sim$400 °C or even lower). In this case, the deposition temperature of the poly-SiGe structural layer and the processing temperature of the piezoresistors (455 °C in this work) have to be lowered. New techniques, like for example laser annealing, might need to be developed to avoid degradation of the poly-SiGe piezoresistivity.