Chapter 7
CMOS Integrated Poly-SiGe Piezoresistive Pressure Sensor

This chapter describes the fabrication and testing of an integrated poly-SiGe-based piezoresistive pressure sensor directly fabricated above 0.13 μm Cu-backend CMOS technology. This represents not only the first integrated poly-SiGe pressure sensor directly fabricated above its readout circuit, but also the first time that a poly-SiGe MEMS device is processed on top of Cu-backend CMOS. In the past, imec already proved the potential of poly-SiGe for MEMS-above-CMOS integration by presenting, for example, an integrated poly-SiGe micromirror array and an integrated gyroscope , both of them fabricated on top of Al-based CMOS. However, the aggressive interconnect scaling, essential to the continuation of Moore's law, has led to the replacement of the traditional aluminum metallization by copper metallization, due to its lower resistivity and improved reliability.

The described integrated sensor includes a surface-micromachined poly-SiGe based piezoresistive pressure sensor (fabricated following the process flow described in Chap. 4) and an instrumentation amplifier that acts as the sensor readout circuit. The amplifier has been fabricated using imec's 0.13 μm CMOS technology, with Cu- interconnects (two metal layers), oxide dielectric and Cu-filled metal-to-metal vias. The chapter begins with a description of the design, fabrication and testing of the instrumentation amplifier used as the sensor readout circuit. The processing of the integrated sensor is explained next, with special attention to the development of the CMOS (Cu) to MEMS (Al) interface. The effect of the MEMS processing on the underlying CMOS performance is also characterized. Finally, the performance of the fabricated integrate sensor is evaluated.

7.1 The Sensor Readout Circuit: An Instrumentation Amplifier

A typical signal conditioning circuit for a piezoresistive pressure sensor comprises the following blocks (Fig. 7.1) [1]: a biasing circuit, an amplifier, a temperature compensation stage, an offset compensation stage and, in case digital output is required,

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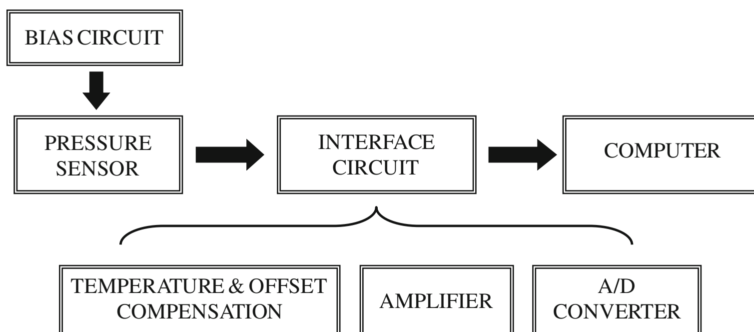

Fig. 7.1 Basic block diagram of a typical signal conditioning circuit for piezoresistive pressure sensors

an analog-to-digital converter. The biasing circuit provides the electrical excitation to the sensor bridge. An amplifier is needed due to the typically weak electrical output signal of piezoresistive sensors. Since the bridge output is not only sensitive to pressure but also to temperature, compensation for the temperature drift is important, especially for high accuracy applications. Some read out circuits may also include a linearization stage to compensate for the nonlinearity in the sensor output.

The zero pressure offset and, in general, the errors caused by processing variations can effectively be handled by the double-bridge compensation technique [2]. It makes use of two piezoresistive Wheatstone bridges: one fabricated on top of the movable sensor membrane while an identical compensation bridge is located on a rigid, non-release part of the sensor chip. The output of the first bridge is, therefore, a function of pressure, temperature and process variations, whereas the compensation bridge response is dependent on temperature and process variations only. The difference of the two bridge outputs removes the voltage offset and any other effect of process variations. Another possibility for compensation of zero-pressure voltage offset and TCO is to connect, in parallel with each of the four bridge piezoresistors, an electrically adjustable resistor with independent adjustment of its total resistance and TCR [3]. By trimming one or more of these adjustable resistors, the offset and TCO can be compensated. Yet another option to cancel the offset could be to power each of the two arms of the sensor Wheatstone bridge by an independent current source; by adjusting the value of the input currents, a zero offset can be achieved.

One of the main reasons for the sensor sensitivity to temperature is the variation of the piezoresistive effect with temperature. A simple way of compensating the TCS is to power the sensor with current instead of voltage. In this way, the TCS will be a function of both the temperature coefficient of piezoresistivity and the TCR of the bridge resistors, which are opposite in sign (depending on the doping concentration). A better compensation, proposed in [4], is to power the sensor with a voltage controlled current source with a pre-defined thermal coefficient, which should have an absolute value close in magnitude but opposite in sign to the sensor TCS. Another scheme for temperature drift cancellation, proposed in [5], is to divide

the sensor Wheatstone bridge in two half bridges with a common reference arm. The output voltages of each half-bridge are amplified separately by a differential amplifier. The gains of the amplifiers are adjusted so that the temperature sensitivities of the half-bridge output voltages cancel each other.

Even though, as can be concluded from the results reported in Chap. 6, the fabricated poly-SiGe pressure sensors in this work exhibited large offsets and a pronounced temperature drift, due to time and resources limitations, the designed sensor readout includes only an amplification circuitry, with no temperature compensation. In any case, as the objective of this work is not to provide a complete integrated sensor suitable for commercial applications but just a demonstrator of the above-CMOS integration capabilities of poly-SiGe, a simple amplifier can be considered enough for this purpose.

The main requirements for an amplifier to be used at the output of a resistive bridge sensor are [6]: relatively high gain, high common mode rejection ratio (CMRR) and high input impedance, to avoid loading the resistive bridge, altering its functioning. One amplifier circuitry fulfilling these requirements, widely used in piezoresistive pressure sensors applications, is the instrumentation amplifier. An instrumentation amplifier (in-amp) [7, 8] is a differential operational amplifier (op-amp) circuit with two high impedance input terminals, which provides effective rejection of the dc common-mode voltage appearing at the two bridge outputs, while amplifying the weak bridge signal voltage. An in-amp employs an internal feedback resistor network that is isolated from its signal input terminals. The gain of the instrumentation amplifier is controlled by the values of these resistors and can be easily adjusted.

7.1.1 Design

The designed amplifier is a classic three-op-amp instrumentation amplifier as shown in Fig. 7.2. The amplifier was designed using a modified version of the imec 0.13 μm technology, with thicker oxide to allow for a higher bias voltage (3.3 V instead of 1.2 V). A higher bias voltage was preferred as the sensor output is directly proportional to the input voltage (as was already seen in Chap. 3). The minimum allowed gate length is 0.35 μm. Spectre, from the Cadence Virtuoso platform [9], was used for the circuit simulations.

The three op-amps is the most straight forward implementation of an instrumentation amplifier. It consists of two non-inverting input buffer amplifiers, followed by a difference amplifier. The two amplifiers on the left, connected in a buffer configuration, provide the high input impedance to the amplifier, necessary to avoid loading the sensor. The third amplifier is used to subtract the two gained input signals, providing a single ended output. The gain of this circuit is determined by the internal feedback resistor network according to expression (7.1):

$$V_{out} = \left(V^{+} - V^{-}\right) \times \left(1 + \frac{2R_1}{R_{gain}}\right) \cdot \frac{R_3}{R_2} \tag{7.1}$$

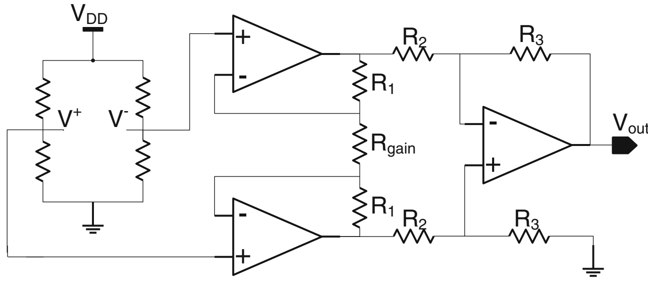

Fig. 7.2 Schematic of the integrated sensor designed in this work: on the *left*, the resistive Wheatstone bridge representing the pressure sensor, and on the *right*, the instrumentation amplifier that acts as the sensor readout circuit

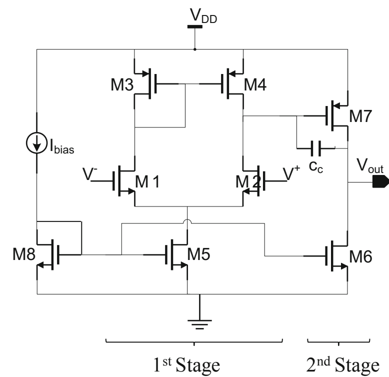

Fig. 7.3 Schematic of a classic two-stage Miller compensated op-amp with an n-channel input differential pair and a p-channel common-source amplifier at the output

where $V^+ - V^-$ represents the differential output of the sensor bridge. Ideally, the common-mode gain of an instrumentation amplifier should be zero. However, mismatches in the values of the equally-numbered resistors and in common mode gains of the two input op-amps result in a non-zero common-mode gain.

All the three op-amps in the instrumentation amplifier are classic two-stage Miller differential-input, single-output op-amps [10, 11] as depicted in Fig. 7.3. This simple op-amp provides good CMRR, output swing and voltage gain. The first stage consists of an n-channel differential pair $M_1 - M_2$ with a p-channel current mirror load $M_3 - M_4$ and an n-channel tail current source M_5. The second stage consists of a p-channel common-source amplifier M_7 with an n-channel current-source load M_6. For biasing purposes, a single input current source is needed; transistor M_8 provides the mirror current for both M_5 and M_6. A compensation capacitor connects the output of the second stage back to the output of the first stage. This capacitor adds stability through the so-called pole splitting Miller compensation [11–13].

The main design specifications considered in this work for the op-amps were high gain and good phase margin ($\geq 60°$). The phase margin (PM in Fig. 7.4) is a measure of stability in a feedback system; it represents the difference between the phase (in degrees) of the amplifier output signal and $-180°$, measured at the unity-gain

Table 7.1 Final transistor dimensions (W/L), compensation capacitor (C_c) and bias current (I_{bias}) for the two types of op-amps designed. The transistors gate width (W) and length (L) are expressed in µm

Device	Input OP-AMPS		Output OP-AMP	
	W	L	W	L
$M_{1,2}$	2	8	2	8
$M_{3,4}$	2	8	2	8
M_5	2	4	2	4
M_6	20	4	40	4
M_7	10	1	5	1
M_8	2	4	2	4
C_c	2 pF		2 pF	
I_{bias}	10 µA		2 µA	

frequency. In most of the cases, 60° phase margin is considered an optimum one. A 60° phase margin will also allow for the fastest settling time when attempting following a voltage step input. For the two input op-amps (Fig. 7.2), apart from high gain and safe phase margin, also high output current is required in order to be able to drive the resistor network in the instrumentation amplifier.

The design parameters include transistor dimensions (W/L), bias current (I_{bias}) and compensation capacitor. The design of the op-amps was performed following the steps described in [11]. For the compensation capacitor, an increment in value improves the phase margin, but also an increase in die area consumed. Finally a value of 2 pF was chosen. The final transistor dimensions (Table 7.1) were obtained after several simulation iterations, until the desired requirements were met. Figure 7.4 shows the frequency response of one of the two op-amps that act as input buffer in the instrumentation amplifier. The designed operational amplifiers exhibit >70 dB of open-loop gain and ~60° of phase margin (PM). The output current for each one of the two input op-amps is ~80µA, whereas for the output op-amp is ~10µA. Even though the minimum allowed gate length in the used technology was 0.35 µm, long gate lengths ($L > 1$ µm) were chosen for the design as transistors with longer gates are more robust against process variations.

Two types of instrumentation amplifiers were designed: with fixed and with variable gain. Both types are based on the schematic shown in Fig. 7.2, with the same three op-amps. The only difference is the design of the resistor network. According to expression (7.1), the gain of the instrumentation amplifier is determined by the value of the resistors. In order to obtain an amplifier with variable gain, it is necessary to replace the resistors in Fig. 7.2 by resistors whose value can be externally adjusted. In this work, these "variable resistors" were designed as depicted in Fig. 7.5: a group of resistor/switch pairs connected in parallel. Every switch is built-up by a combination of a CMOS inverter and a transmission gate. Every switch has an independent input signal to turn it off/on. In this way the gain of the amplifier can be tuned by activating the switch corresponding to the required resistance value. For example, by activating

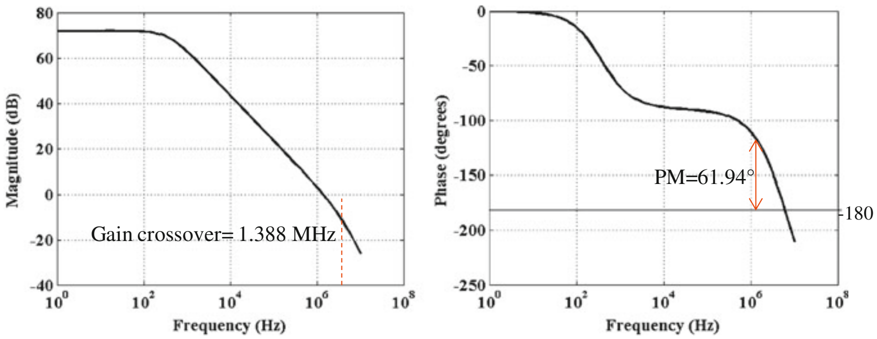

Fig. 7.4 Magnitude and phase plot (from simulations) of the input op-amp of the instrumentation amplifier

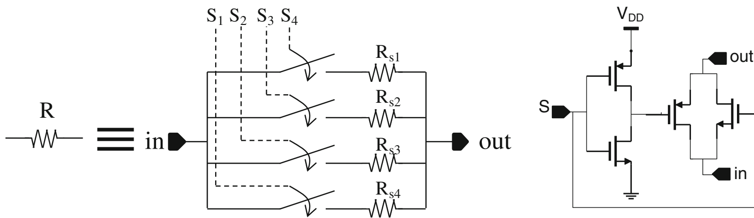

Fig. 7.5 Schematic of the designed variable resistor. By activating the corresponding switch signal ($S_1 \ldots S_4$), the desired resistance is selected. On the right, schematic of one of the CMOS switches

Table 7.2 Value of resistors (in kΩ) for the two types of instrumentation amplifiers designed: with fixed and with variable gain. The expected gain (obtained from simulations) in each case is also included

	Fixed gain	Variable gain
R_1	1	1
R_2	2	3, 5, 7, 10
R_3	100	50, 100, 150, 200
R_{gain}	5	5
Gain	65.2	3.3 194.4

S_1 (S_1='1') while keeping the other signals off ($S_{2...4}$='0'), the value of R will be equal to R_{S1}. Note that it is also possible to activate several switch signals at the same time. In that case, the value of R will be equal to the parallel of the selected resistors.

Only two resistors (R_2 and R_3 in Fig. 7.2) were designed as variable resistors, while resistors R_1 and R_{gain} exhibit fixed values. For the instrumentation amplifier with fixed gain, on the other hand, only standard resistors with fixed value were used. Table 7.2 lists the values of the different components of the resistor network for the two types of amplifiers. The expected gains, obtained in each case from the slope of

the corresponding simulated output voltage versus input voltage, are also listed. A gain of 65.2 is obtained for the instrumentation amplifier with fixed resistors. For the variable gain amplifiers, on the other hand, the gain can vary from 3 up to almost 200 depending on the selected resistor values. There is a slight mismatch between the amplifier gain obtained from simulations and the gain calculated using expression (7.1). From example, by substituting in expression (7.1) the resistor values listed in column 1 in Table 7.2, a gain of 70 is calculated for the amplifier with fixed gain, $\sim$7.4% higher than the gain obtained from simulations. This mismatch is mainly due to the fact that expression (7.1) is obtained by analyzing the circuit in Fig. 7.2 considering the op-amps as ideal: infinite gain, infinite input-impedance, zero input-current and zero output impedance. However, in the simulations, real models of the transistors that build up the op-amps are used, and therefore "non-idealities" such as finite gain or finite input impedance are included.

7.1.2 Layout

The layout was performed using Layout XL from the Cadence Virtuoso platform [9]. The following techniques were used to verify layout: DRC (Design Rule Check) and LVS (Layout vs. Schematic). The designs were made for the HAWK maskset (2009), which includes both CMOS and MEMS masks for integrated fabrication. In this section, only specific details of the amplifiers layout are included. A more general description of the HAWK maskset, including also the MEMS part, can be found in appendix A.

Figure 7.6 shows the layout of an instrumentation amplifier with fixed gain. The compensation capacitors (three in total, one per op-amp) occupy most of the die area. The capacitors are realized using the poly and metal 1 layers as the bottom and top plates, respectively, assuming a nominal capacitance of $150 \cdot 10^{-6}$ pF/μm^2(total area needed for a 2 pF capacitor is $\sim 116 \times 116\ \mu$m^2). The resistors are implemented as non-silicided (using an extra layer to block silicidation) polysilicon resistors on n-well, with a nominal sheet resistance of 230 $\Omega/\square$. Two types of resistor layouts are implemented (Fig. 7.7). For better matching, an interdigitized structure is used for a pair of resistors that need to be equal (like R_1, R_2 or R_3). For R_{gain}, a "serpentine" structure is used.

Figure 7.8 shows a close-up view of the layout of one of the two input op-amps of the instrumentation amplifier. The eight transistors (5 NMOS and 3 PMOS) are visible, together with part of the poly-metal compensation capacitor. The following layout techniques were used for better performance [11, 14–17]:

- Guard ring around PMOS transistors M_3, M_4 and M_7 to reduce substrate coupling noise.
- "Common-centroid" configuration in differential pair (M_1 and M_2) to cancel first-order gradient: each of the two transistors is decomposed in two halves that are placed opposite of each other and connected in parallel.

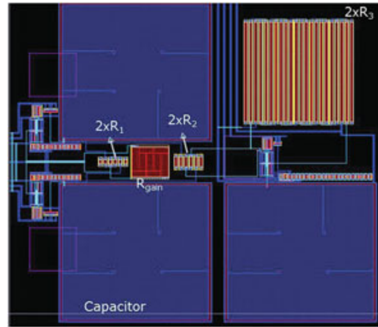

Fig. 7.6 Layout of a 3 op-amps instrumentation amplifier with fixed gain. The three compensation poly-metal capacitors are visible, together with the poly resistors (of fixed value). Resistors pairs (R_1, R_2 or R_3 in Fig. 7.2) are interdigitated for better matching. For R_{gain}, a simple serpentine structure is used

- The source diffusion and the drain diffusion are filled with the maximum number of contacts to reduce the metal/diffusion contact resistance.
- To avoid circuit failure due to bad-processed vias or contacts, at least double contacts or double vias are used whenever possible.
- The gate oxide underneath the poly is incredibly thin. If the charge accumulated on the poly is sufficiently large, the accumulated charge can threaten to overstress and irreparably damage the thin gate oxides of the transistor, causing unreliable operation. This is known as process antenna effect. To protect the transistors gate, no contacts or vias are placed over the poly gate, and no routing is done over the gates.
- Fingering of wide transistors. The fingering technique allows reducing the drain and source area, reducing in turn the parasitic capacitance which results in an increased transistor speed. Folded transistors also have smaller gate resistance, and can therefore turn off and on faster. This fingering technique is only applied

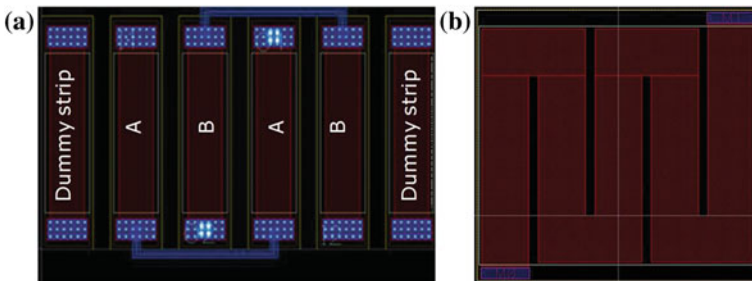

Fig. 7.7 **a** Interdigitated structure of two resistors of 2 kΩ (A-A and B-B), corresponding to R_2 in the amplifier schematic (Fig. 7.2). Each poly line is 1 kΩ. Two "*dummy poly lines*" are included on the sides for better matching: to make sure the ending elements have the same boundary conditions than the inner elements. **b** Resistor of 5 kΩ (corresponding to R_{gain}) with "serpentine" structure

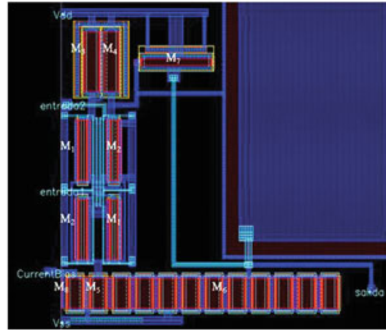

Fig. 7.8 Layout of a two-stage Miller op-amp, corresponding to one of the two input op-amps of the instrumentation amplifier. Only part of the compensation capacitor is visible. Transistors are named according to Fig. 7.3

to transistor M_6, which forms a current mirror with transistor M_8 (W/L = 2/4). To improve matching, transistor M_6(W/L = 20/4 or 40/4 for input and output op-amp, respectively) is divided into 10 (or 20) transistors of 2/4 connected in parallel. Metal, instead of poly, was used to interconnect the gates, as poly exhibits a higher resistivity and a larger parasitic capacitance poly-substrate.

It is important to note that the amplifier layout was not optimized in terms of die area consumption. The layout of the fixed gain instrumentation amplifier (shown in Fig. 7.6) occupies a total area of $290 \times 280\ \mu m^2$. Robustness was the main layout design concern, and not area consumption. For example, very large transistors were used as they are more robust against process variations. From the interconnections point of view, wide lines (width at least double of the minimum allowed by technology) were used with enough spacing from one another (to avoid unwanted shorts during fabrication). A considerable amount of the circuit area is devoted to the poly resistors; especially large is resistor R_3 (100 kΩ). To save area, a (properly biased) transistor could have been used instead, as a transistor can provide a large resistance with significantly smaller area. However, the resulting resistor would be non-linear. For this reason, non-silicided polyresistors, although more area consuming, were used.

Figure 7.9 shows the layout of the two types of variable gain amplifiers designed. In the first amplifier (Fig. 7.9a) the resistors are designed as simple "serpentine" structures; the resistance values in each "resistive block" are: $R_2 = 3/5/7/10$ kΩ and $R_3 = 50/100/150/200$ kΩ. In the second amplifier (Fig. 7.9b) "interdigitated" resistors (see Fig. 7.7) are used for better matching; R_2 contains four resistors with values 2, 5, 7 and 10 kΩ while R_3 contains only two resistors with values 100 and 200 kΩ. The total circuit areas are $\sim 540 \times 270$ and $\sim 525 \times 285\ \mu m^2$, respectively. In both cases the op-amp layouts are exactly the same as for the fixed-gain amplifier (Fig. 7.8).

Figure 7.10 shows the final layout. Eight blocks can be identified, containing three fixed-gain amplifier and five variable gain amplifiers: two with "interdigitated" variable resistors (Fig. 7.9b) and three with "serpentine" resistors (Fig. 7.9a). In some cases, certain building blocks of the instrumentation amplifiers (like the op-amps or the variable resistors) are wired out independently for testing purposes. Each module

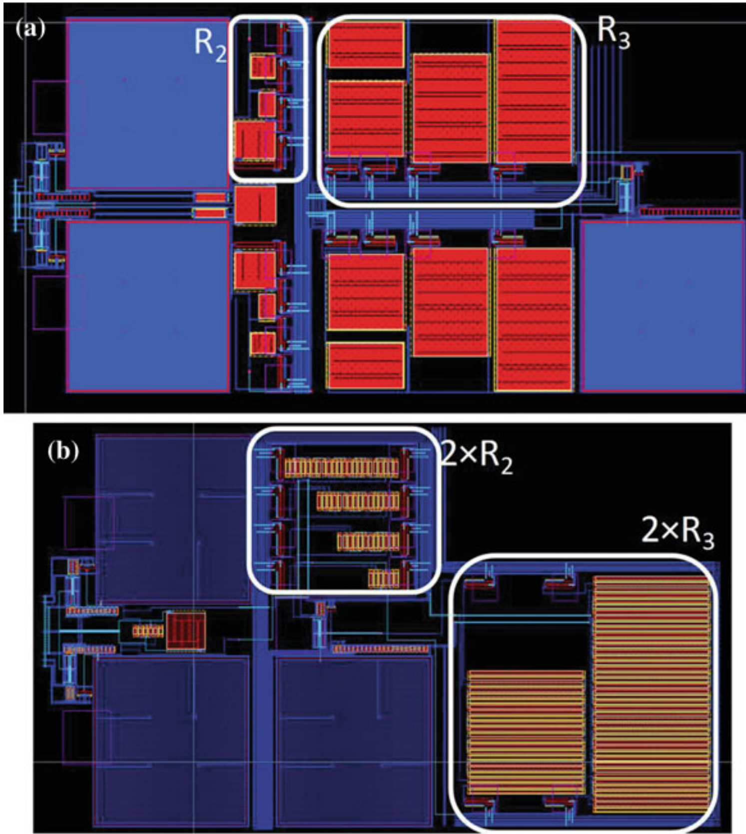

Fig. 7.9 Layout of the two instrumentation amplifiers with variable gain designed in this work. In **a** "serpentine" resistors are used while in **b** interdigitated resistors for better matching are employed

contains a standard imec 24 pins probecard pad structure. It contains 24 bondpads of $80 \times 60\ \mu m^2$ with a vertical (horizontal) pitch of 40 μm (30 μm). This is not the optimum bondpads distribution from area consumption point of view; a smarter design could use bondpads placed surrounding the circuit. However, the use of a non-standard probecard layout is also more time consuming: not only the specific layout has to be designed, but the appropiate probecard for the electrical measurements must also be fabricated. Four of the modules include ESD protection [18, 19]. It consists of two wide parallel lines (metal 1 for GROUND and metal 2 for VDD) interconnected by one diode (in reverse) and 6 diodes (alternating). Each bondpad is connected by diodes to VDD (reversed) and GROUND.

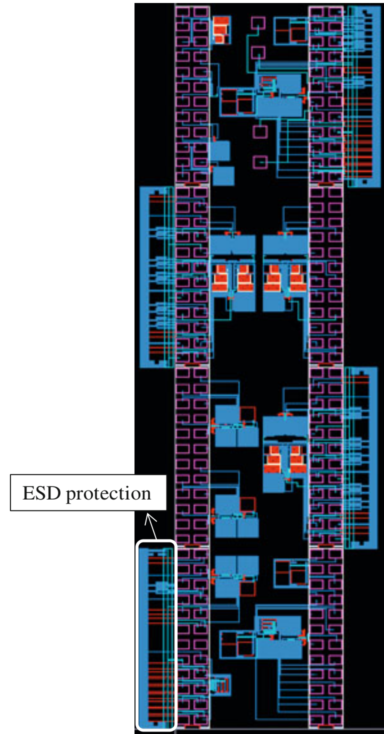

Fig. 7.10 General overview of the complete CMOS layout designed for the HAWK maskset. It includes eight modules, each of them containing the layout for imec's 24 pins standard probecard. The use of the standard probecard will facilitate the electrical measurements later on. The top-right module contains four extra bondpads to study the "hybrid" integration (wirebonding) with the MEMS pressure sensor (see appendix A)

7.1.3 Fabrication

The designed amplifiers were fabricated using a modified version of imec's 0.13 μm CMOS technology, with a thicker gate oxide (∼7 nm instead of ∼2 nm) to allow for higher voltages (3.3 V instead of 1.2 V). The polysilicon gate is 150 nm thick. The front end of line process includes shallow trench isolation, N-well and P-well implants, NMOS and PMOS source and drain formation (including pocket implants to reduce short channel effects) and nickel salicidation. The back end of line process includes two copper (Cu) interconnect layers with thicknesses of 360 nm (for Metal 1) and 600 nm (for Metal 2) with $0.2 \times 0.2\ \mu m^2$ Cu-filled vias connecting the two layers. Before each (Cu) metal layer deposition, a thin Ta (adhesion)/TaN (barrier) layer is deposited. The intermetal dielectric is formed by 50 nm SiC (Cu diffusion barrier layer and etch stop) and 600 nm PECVD (Plasma-enhanced Chemical Vapor Deposition) Si-oxide. The pre-metal dielectric (between poly and metal 1) is formed by 50 nm of Si-nitride, 500 nm of PSG (phophosilicate glass) and 10 nm PECVD SiO_2. Tungsten (W) filled $0.15 \times 0.15\ \mu m^2$ vias with Ti/TiN diffusion barrier are used to connect the poly and metal 1 layers. Figure 7.11 shows the schematic cross-section.

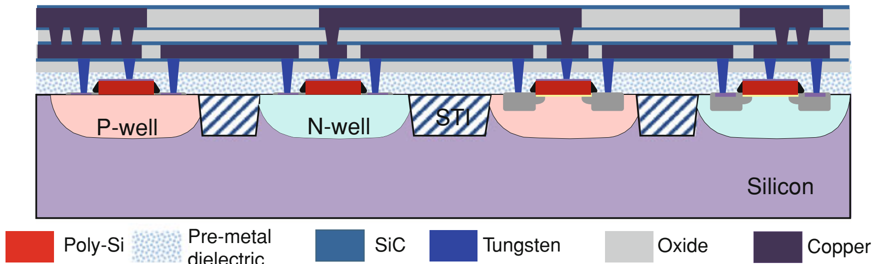

Fig. 7.11 Schematic cross-section of the described 0.13 μm CMOS technology. Dimensions not to scale.

7.1.4 Measurements

The fabricated circuit has been tested on a Suss PA300 probe station with measurement equipment from National Instruments and Keithley. Labview software was used to control the measurement setup. Figure 7.12 plots the output voltage vs. input differential voltage for an instrumentation amplifier with fixed gain. A very high yield (above 88 %) for this kind of amplifiers was obtained. Figure 7.12 also includes an histogram representing the distribution of the measured amplifier gain (obtained from the output voltage slope). The gain, with a mean value of 68.3, exhibits a great uniformity across the wafer (with a variation within 0.8 %). The measured gain is also very close to the gain predicted by simulations (65.2, see Table 7.2). As can be observed in Fig. 7.12, the output voltage of the amplifier for zero input voltage is different from zero. This output voltage for zero input is known as offset, and it is generally undesired. Most of the measured amplifier exhibited an offset of ∼43 mV, although some devices had offsets up to 300 mV. This offset might be explained considering imbalance of resistors values or mismatches between transistors. Finally, the amplifier output saturates at a voltage of ∼3.15 V, slightly lower than the power supply voltage (3.3 V).

Figure 7.13 shows the response of an instrumentation amplifier with variable gain for different combinations of the switch activation signals of the programmable resistors. Table 7.3 lists the corresponding resistance values for each switch combination, together with the measured and simulated gain. As can be observed, the gain of the amplifier can be varied according to the input switch combination. When integrated with a pressure sensor, this kind of amplifiers can be very useful as the gain can be tuned according to specifications or the sensitivity or offset of the sensor. For example, if the final sensitivity of the sensor is lower than expected, a higher gain can be selected. On the other hand, if the offset is too high, a lower gain can be chosen in order to avoid early saturation.

The results shown above correspond to a variable gain amplifier with “interdigitated” resistors (Fig. 7.9b). For the secon d type of variable gain amplifiers, with “serpentine” resistors (Fig. 7.9a), a similar behaviour is observed: the gain can be

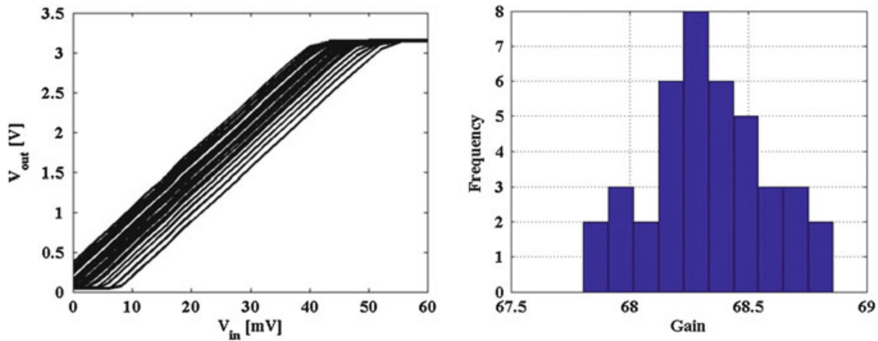

Fig. 7.12 Measured output voltage versus input differential voltage for a fixed gain amplifier across full wafer. On the right, histogram representing the gain distribution across the wafer. A great uniformity in the measurements is observed

tuned according to the chosen switch signals, and the measured gains matched very closely those predicted by simulations.

7.2 Fabrication of a CMOS Integrated Pressure Sensor

After the fabrication of the CMOS readout circuit is completed, the processing of the poly-SiGe pressure sensor takes place. Two main measures were taken during the MEMS fabrication in order to avoid introducing any degradation in the underlying CMOS circuitry. First, the maximum processing temperature of the complete sensor, including the poly-SiGe piezoresistors, is kept $\leq$455 °C. And second, to protect the

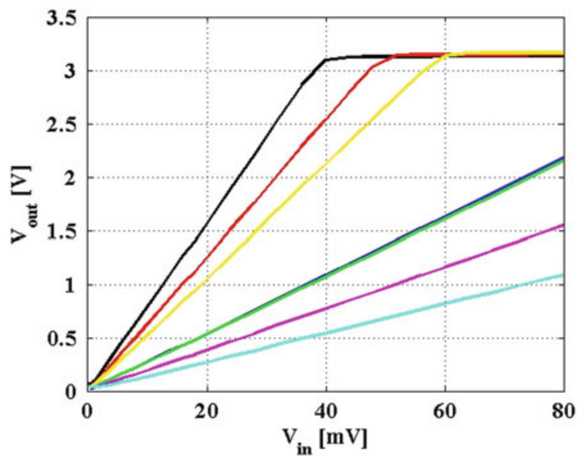

Fig. 7.13 Measured output voltage of a variable gain amplifier with “interdigitated” resistors for different switch signals. A different response is obtained for each switch combination

Table 7.3 Corresponding resistance values (R_3 and R_2) for each switch combination. A comparison between the measured and simulated gains is also included. In general, a good matching between the simulated and the measured gains is observed

R_3		R_2				R_3 (kΩ)	R_2 (kΩ)	Gain measured	Gain simulations
S_1	S_2	S_4	S_3	S_2	S_1				
1	1	1	1	1	1	67	1	78.7	82.7
1	0	0	0	0	1	200	10	27.3	27.3
0	1	1	0	0	0	100	2	63.8	65.2
0	1	0	1	0	0	100	5	27	26.98
1	0	0	0	1	0	200	7	53.5	38.7
0	1	0	0	1	0	100	7	19.4	19.4
0	1	0	0	0	1	100	10	13.7	13.65

electronic circuit from the aggressive etch and deposition steps (specially the release process in vHF) which are needed to fabricate the MEMS devices, a SiC protection layer was used.

Figure 7.14 shows the layout and a top view microscope picture of two integrated sensors. The two shown sensors have an "n-shape" piezoresistor design (see Chaps. 3

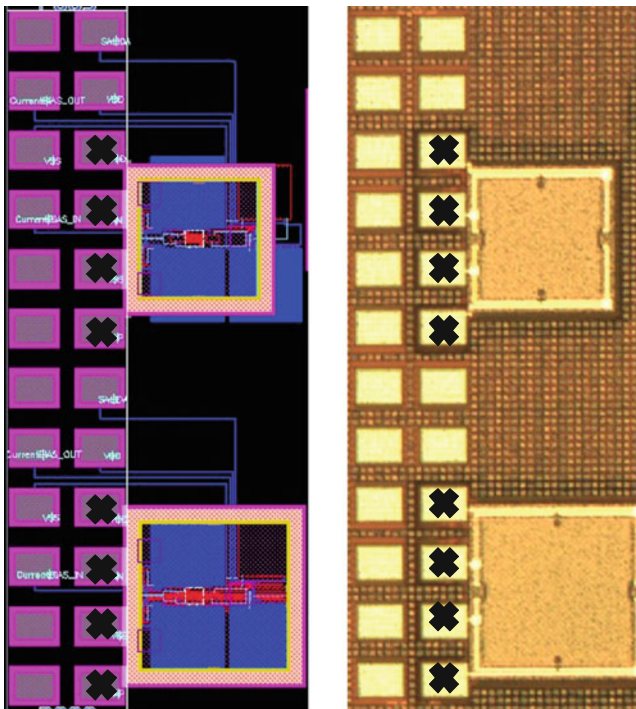

Fig. 7.14 Layout and microscope picture of two integrated pressure sensors. The sensor bondpads appear marked with a cross

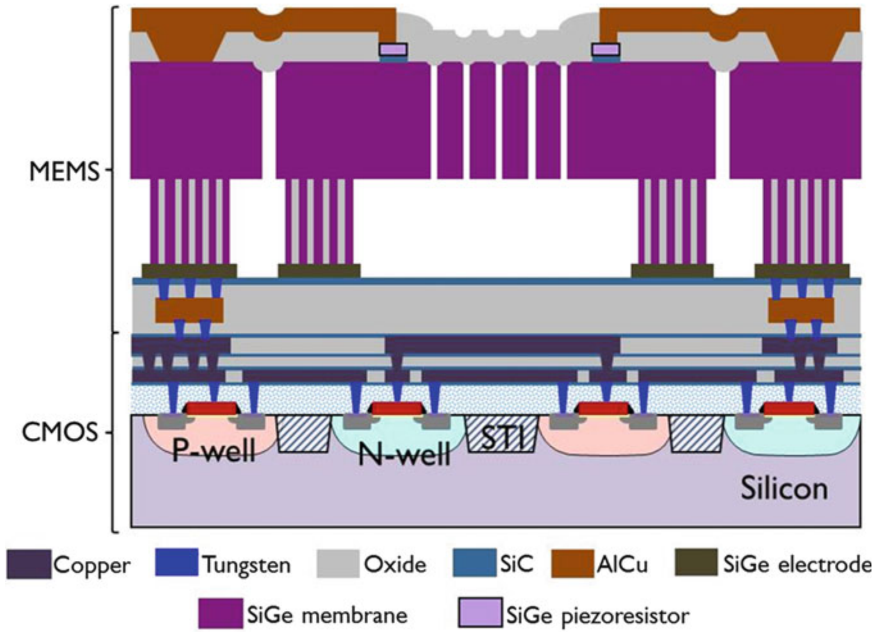

Fig. 7.15 Cross-section of the integrated pressure sensor, with the most relevant layers highlighted

and 6) with the transverse piezoresistors placed at the membrane edge. Both of them are integrated with a fixed gain amplifier. In the layout snapshot, the CMOS circuit just below the pressure sensor is clearly visible. In the microscope picture only the sensors can be appreciated, as the CMOS is completely covered by MEMS layers (the SiC protection layer and the sacrificial oxide, among others). For the bottom integrated sensor ($250 \times 250\,\mu m^2$), the circuit (without including the bondpads) occupies approximately the same area as the poly-SiGe piezoresistive sensor. In this case, by fabricating the MEMS directly on top of the CMOS (only possible thanks to the use of poly-SiGe), the total die area occupied by the complete integrated sensor has been reduced by a factor of $\sim$2, as compared to the traditional integration methods (see Chap. 1). This is a clear example of one of the main advantages of using poly-SiGe as MEMS structural material: the reduction in area consumption.

Figure 7.15 shows a cross-section of the fabricated integrated sensor. The MEMS process starts with the formation of $0.5 \times 0.5\,\mu m^2$ tungsten-filled vias that provide electrical connection between the pressure sensor and the CMOS circuit. These vias connect the CMOS top-metal layer (Cu) and the MEMS metal layer (AlCu). They are located exclusively on the bondpads; in the rest of the die area, the MEMS are completely isolated from the CMOS. All the 24 bondpads (and not only the 8 corresponding to the sensor) shown in Fig. 7.14 include these vias, to be able to provide the necessary inputs to the circuit after the MEMS processing. The vias are

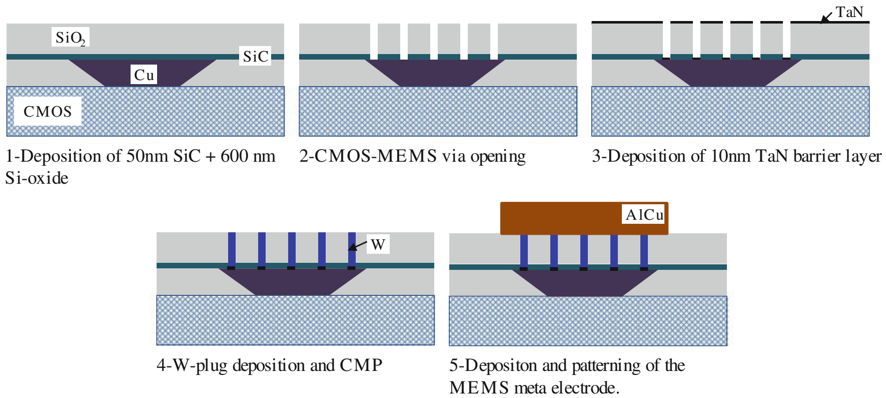

Fig. 7.16 Schematic process flow for the fabrication of the W-filled CMOS-MEMS vias. Note that scales are distorted

distributed forming a perfect μm^2 square grid with a pitch of 4.5 µm. In total there are 165 CMOS-MEMS vias in each bondpad.

The fabrication of these CMOS-MEMS vias is schematically illustrated in Fig. 7.16. The isolation between the CMOS top-metal layer (Cu) and the MEMS metal layer (AlCu) is provided by a thin SiC layer (50 nm), which acts as a Cu diffusion barrier, and 600 nm of PECVD Si-oxide. A dry etch process is used to etch both the SiC and the Si-oxide to open the CMOS-MEMS vias. These $0.5 \times 0.5\ \mu m^2$ vias are filled by a stack of 10nm TaN (Cu diffusion barrier), Ti/TiN (15/10 nm) liner/barrier layer and 350 nm of tungsten (W). After via filling, a CMP step is performed to remove the W everywhere except in the vias. This CMP also removes the TaN layer everywhere except inside the CMOS-MEMS vias. The 880 nm-thick AlCu MEMS bottom electrode is then deposited and patterned, following the process described in Chap. 4. Figure 7.17 shows a cross-section SEM picture of a W via connecting the Cu top metal layer and the Al MEMS bottom electrode. The measured contact resistance of one of these CMOS-MEMS vias is 0.8 Ω with a ±6 % maximum variation across the wafer.

After the formation of these CMOS-MEMS vias, the rest of the MEMS pressure sensor fabrication proceeds as explained in Chap. 4. The main steps in the pressure sensor fabrication process are (a more detailed description can be found in Chap. 4):

1. Deposition and patterning of a metal stack composed of 5 nm of Ti, 880 nm of AlCu (0.5 wt%) and 60 nm of TiN.
2. Deposition of the 400 nm-thick SiC CMOS protection layer. This passivation layer protects the electronic circuit from the aggressive etch and deposition steps which are needed to fabricate the MEMS devices.
3. Formation of 400 nm-thick boron doped ($B \sim 1 \times 10^{21}\ cm^{-3}$) SiGe electrodes. The SiGe electrodes and MEMS metal layer are separated by the SiC protection layer plus 600 nm of oxide, and connected through $0.5 \times 0.5\ \mu m^2$ W-filled vias.

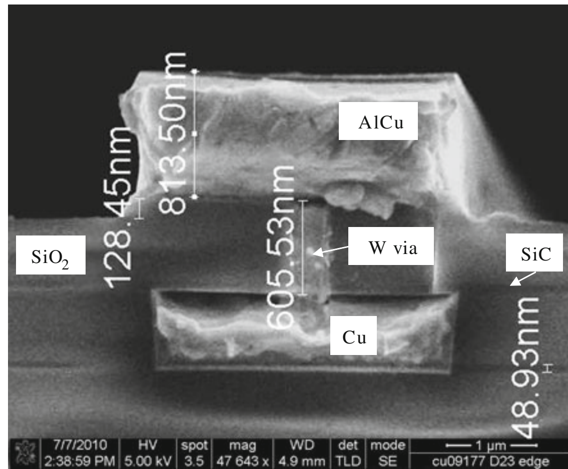

Fig. 7.17 Cross-section of a W-filled CMOS-MEMS via. The bottom Cu and top Al layers, together with the SiC+SiO_2 dielectric, are visible

4. Deposition of 3 µm of sacrificial oxide, followed by the patterning of the membrane anchors.
5. Deposition of the poly-SiGe membrane and filling of the anchors by a combination of CVD and PECVD processes.
6. To define the piezoresistors, a 200 nm-thick poly-SiGe layer (∼77 % Ge) is deposited, boron doped through implantation ($B \sim 1 \times 10^{19}\,\mathrm{cm}^{-3}$), and annealed at 455 °C for 30 min. The longitudinal and transverse gauge factors for such a poly-SiGe layer are, approximately, 12.9 and 5.2, respectively (see Chap. 2). A thin SiC layer (∼ 60 nm) is used as isolation layer between the SiGe membrane and the SiGe piezoresistors.
7. Opening of $1 \times 1\,\mu\mathrm{m}^2$ etching channels in the membrane and removal of the sacrificial oxide by a combination of anhydrous vapor HF (AVHF) and ethanol vapor.
8. Sealing of the membrane with ∼1.2 µm of SACVD (Sub-atmospheric CVD) Si-oxide. The cavity pressure after sealing, determined from load-deflection measurements, is ∼7 kPa (Chap. 5).
9. Opening of contacts, followed by the deposition and patterning of 500 nm AlCu to connect the piezoresistors.
10. A final lithographic step, followed by the etching of the sealing and SiGe membrane layer, to separate the bondpads and cavities from one another.

Figure 7.18 shows a SEM picture of an integrated sensor with “n-shape” piezoresistors. At the bottom, the two Cu metal layers of the CMOS circuitry are visible. The poly-SiGe piezoresistive pressure sensor, fabricated directly on top of the CMOS, can also be observed. Figure 7.19 shows a closer view to the bottom layers: the two Cu metal lines, the AlCu MEMS bottom electrode, the SiC CMOS protection layer and the MEMS SiGe electrode are clearly visible. Even the CMOS transistors can be appreciated.

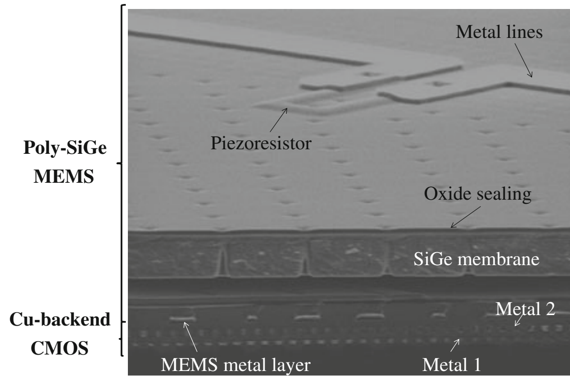

Fig. 7.18 Cross-section SEM picture of the integrated sensor. At the bottom, the two Cu metal lines of the CMOS circuit can be observed. Above, the MEMS layers (the poly-SiGe membrane and piezoresistors, the oxide sealing layer and the metal interconnects) are visible

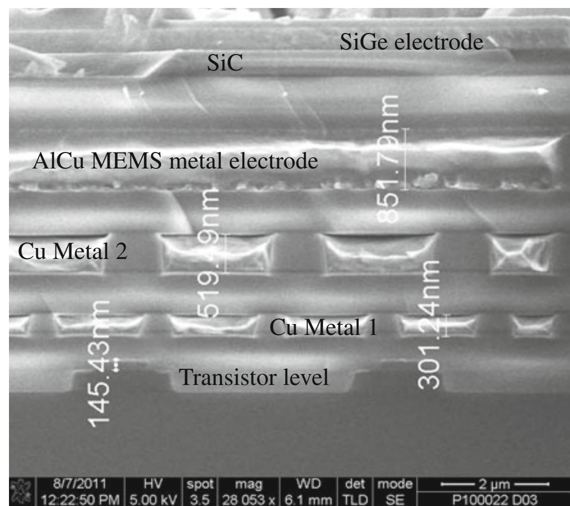

Fig. 7.19 XSEM picture offering a closer view to the metal bottom layers (the two CMOS Cu lines and the AlCu MEMS electrode). Above, the SiC protection layer and the SiGe electrode can be appreciated. At the bottom, the CMOS transistor level is visible

The two biggest issues faced during the MEMS fabrication above Cu-based CMOS were:

1. Delamination. Although already observed during the stand-alone pressure sensors fabrication, delamination issues were worse during the integrated sensor fabrication. This might be due to the extra stress coming from the CMOS layers.
2. Contamination. Cu is considered level 3 in imec's cleanroom facility, while most of the MEMS processing tools are level 2. In order to ensure no copper contamination of the level 2 tools, Total reflection X-ray fluorescence (TXRF) analysis [20] had to be performed after each critical processing step (all the wet and dry etch/strip operations). However, no Cu was ever found after the processing of the integrated wafers, which indicate that both TaN and SiC are good Cu barrier layers.

Table 7.4 Effect of MEMS post-processing on relevant CMOS parameters

	Before MEMS	After MEMS[a]
Threshold voltage linear	0.495 V ± 26 mV	0.527 V ± 85mV
Threshold voltage saturation	0.538 V ± 9.7mV	0.56 V ± 11 mV
Leakage current	12.8 ± 7.4 pA	13.1 ± 7 pA
Drive current	351 ± 5.45 μA	343 ± 5.33 μA
R_{sheet} Metal 2 (mΩ/sq)	43.02 ± 1.33	41.79 ± 1.23
M1/M2 contact	3.12 ± 0.5 Ω	7.93 ± 4.36 Ω

[a] The measurements before and after MEMS were performed on different wafers (although with the same CMOS processing), so the observed variations may also be partially due to wafer to wafer variations

7.3 Effect of the MEMS Processing on CMOS

This section evaluates the impact of the MEMS post-processing on the underlying CMOS. During the MEMS pressure sensor fabrication, the CMOS wafers withstand a maximum process temperature of 455 °C (corresponding to the SiGe depositions and several annealing steps) for ∼ 8.5 h (see Chap. 4 for more details). Table 7.4 shows the effect of the MEMS processing on relevant transistor parameters, CMOS backend and overall amplifier gain. The measurements before and after MEMS correspond to different wafers (although with the same processing), so the observed variations may also be partially due to wafer to wafer variations.

The threshold voltage, in the linear and saturation region, has been measured at a drain to source voltage of 0.1 and 3.3 V, respectively. After the MEMS processing, a slight increase in both the linear and the saturation threshold voltage is observed. The change for the linear threshold voltage was 32 mV (∼ 6.4 %), while for the saturation threshold voltage the increase was around 22 mV (∼ 4.1 %). Also for positive channel MOS (PMOS) transistors an increase in threshold voltage was observed. Similar results were obtained in [21], where electron trapping during the annealing step was proposed as explanation. The transistor leakage current seems to increase after the MEMS processing, although the measured variation (0.3 pA) is well within the error margin and can be considered negligible. On the other hand, the transistor drive current is found to decrease (∼ 2.3 %) due to the MEMS processing, which is in agreement with the observed increase in threshold voltage.

For the CMOS backend, a decrease of ∼ 3.2 % in the sheet resistance of the Cu metal 2 line was observed, which might be attributed to a possible grain growth due to the thermal budget of the MEMS processing [22], although the change is too small to draw any conclusion. The metal-to-metal Cu-filled vias resulted to be the most temperature sensitive structure in the CMOS, with a pronounce increase in via resistance. One possible explanation for this increase in via resistance could be the formation of voids to relax the mechanical stress induced by the mismatch between the thermal expansion coefficient of copper and the surrounding oxide [23]. In [24], voids in Cu-filled Through Silicon Vias (TSV) were observed after Cu electroplating, and void-growth was observed at the void location after annealing. The authors

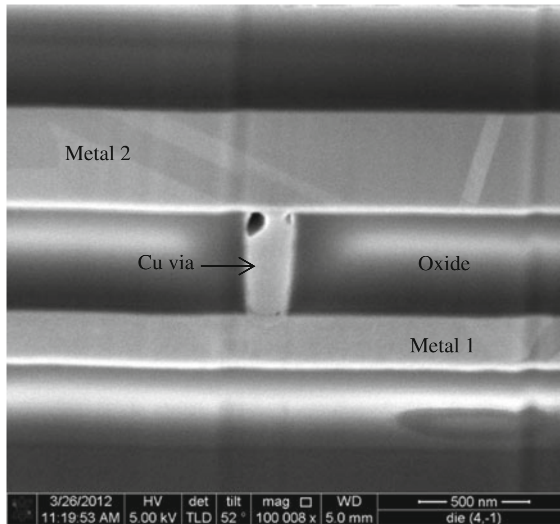

Fig. 7.20 Cross-section picture of a $0.2 \times 0.2 \mu m^2$ CMOS Cu-filled via after MEMS processing. Voids in the via are clearly visible

suggested hydrostatic stress-assisted void growth as the responsible mechanism. Figure 7.20 shows a cross-section picture (obtained in a FIB-SEM system) of one of these $0.2 \times 0.2\,\mu m^2$ CMOS Cu-filled vias. A void is clearly visible at the via/metal 2 interface. There seem to be also small voids at the barrier sidewalls and bottom.

The found increase in via resistance is much more pronounced than predicted by previous annealing tests (see appendix D) on similar CMOS wafers ($< 10\,\%$ for 6 h annealing at 455 °C). One explanation for this could be the longer time that the wafers must withstand at high temperature (455 °C) during MEMS processing as compared to the times considered in the annealing tests. Moreover, all of the SiGe depositions and annealing steps during the MEMS flow are performed in a hydrogen-rich atmosphere. In [25], a much higher density of voids in samples annealed in atmosphere containing hydrogen was observed, as compared to samples annealed in an Ar atmosphere. A possible reaction of oxygen impurities contained in the Cu films to form water vapor when annealed at high temperatures in an hydrogen atmosphere was proposed as explanation. To prevent this Cu via degradation, work at imec is ongoing to further reduce the MEMS processing time (e.g by reducing the number and length of the annealing steps) and temperature (e.g. below 400 °C) and/or to reduce the amount of hydrogen used in the process flow. In any case, no significant impact on the amplifier gain was observed, although after the MEMS processing the values exhibited a larger spread (Fig. 7.21).

Regarding the CMOS-MEMS interface, the resistance of the tungsten-filled vias increased from $\sim$0.82 Ω to $\sim$1 Ω. The MEMS processing also resulted in an increase in the sheet resistance of the Al MEMS bottom electrode from 340 m/sq to 396 m/sq, which can be explained by Ti/Al reactions [26].

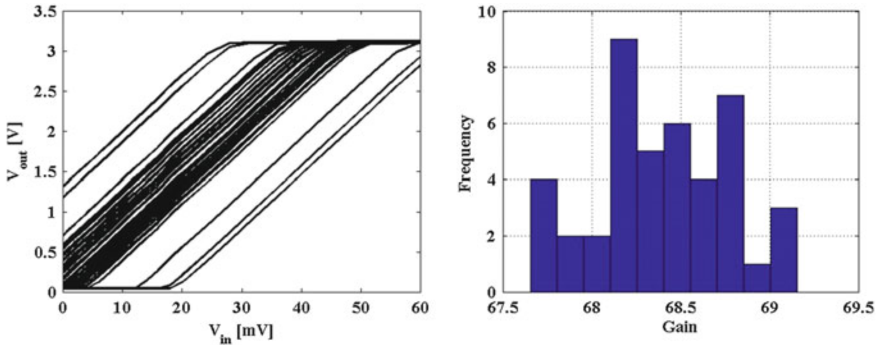

Fig. 7.21 Output voltage for a fixed gain instrumentation amplifier measured after MEMS post-processing. On the *right*, histogram representing the gain distribution across the wafer

These resistance changes are however not detrimental to the overall performance of the CMOS circuit, as demonstrated by the functional integrated pressure sensor (see next section). A more complete study of the thermal budget limits for imec standard 0.13 μm CMOS technology is presented in appendix D.

7.4 Evaluation of the CMOS-Integrated Pressure Sensor

Similar as the stand alone pressure sensors (Chap. 6), the integrated sensors have been tested in the pressure range from 0 to 1 bar using an environmental chamber in combination with a HP4156A precision parameter analyzer. For these experiments the used environmental chamber was a Suss Microtech PAV-150 instead of the PMV-150 chamber used in the evaluation of the stand alone sensors. The difference between these two chambers is that the PAV is a semiautomatic vacuum prober while the PMV is a manual prober. The PAV was preferred for the measurements of the integrated sensors since up to eight probes can be added to the chamber, while in the PMV the maximum number of probes is only six. For the measurement of the integrated sensor, the minimum number of probes needed is seven (corresponding to a sensor integrated with a fixed gain amplifier).

It is important to note that, due to time limitations, only the pressure response of the integrated sensors could be characterized. A complete evaluation should include other important performance parameters, like temperature drift and signal-to-noise ratio (SNR). The SNR could be an important indicator to evaluate if the parasitic reduction thanks to the CMOS-monolithic integration really results in the promised improved performance with respect to the traditional hybrid integration.

Figure 7.22 shows a microscope picture of a 250 × 250 μm^2 poly-SiGe piezoresistive sensor integrated with a fixed gain amplifier. The necessary electrical stimuli are indicated on top of the corresponding bondpads. All the electrical signals

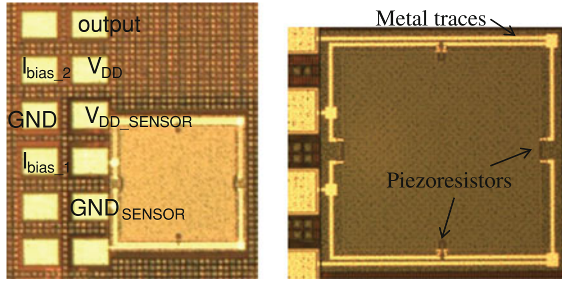

Fig. 7.22 Microscope picture of a fabricated integrated sensor (with fixed gain amplifier). The necessary electrical stimuli for measurements are indicated. For the CMOS, two input currents ($I_{bias}_1 = 10\,\mu A$ and $I_{bias}_2 = 2\,\mu A$), one ground and one power supply are needed. For the sensor, only two electrical signals (ground and V_{DD}) are needed. The output of the integrated sensor (CMOS+MEMS) can be read through the bondpad mark as "output". On the right, close-up view of the sensor, with the piezoresistors and metal interconnects clearly visible, can be observed

are provided by the HP4156A parameter analyzer and its four input/output ports. Two ports are used to provide the two current bias necessary for the CMOS circuit ($I_{bias}_1 = 10\,\mu A$ and $I_{bias}_2 = 2\,\mu A$). One port is used to provide the bias voltage ($V_{DD} = 3.3$ V) both to the circuit and the sensor. And finally, one port is used to measure the output of the integrated sensor (CMOS+MEMS). Note that the input differential voltage for the amplifier comes directly from the differential output of the sensor. The ground connection of the parameter analyzer provides the ground for the circuit and the sensor.

Figure 7.23 plots the pressure response of a $250 \times 250\ \mu m^2$ pressure sensor with "n-shape" longitudinal piezoresistors and transverse piezoresistors placed at the edge of the membrane (design D2 according to Fig. 6.3). The left graph plots the voltage output versus pressure for the sensor alone, while the right graph plots the output of the integrated sensor (CMOS+MEMS). The sensitivity of the poly-SiGe piezoresistive sensor alone was around 2.48 mV/V/bar (similar to the stand-alone sensors with the same design, see Chap. 6). The integrated sensor (same sensor + Cu-based CMOS amplifier underneath) showed a sensitivity of $\sim 159.5 \pm 1$ mV/V/bar, $\sim$64 times higher than the stand-alone sensor. This gain is very close to the gain exhibitted by the CMOS amplifier alone ($\sim$68), which corroborates the conclusion from the previous section: the MEMS processing does not have a significant effect on the CMOS circuit.

One of the main problems exhibited by the stand alone pressure sensors in Chap. 6 was a very high offset. Since the amplifier does not include offset compensation, the offset of the pressure sensor is also amplified by a factor of $\sim$64. For the sensor described in Fig. 7.23, a zero-pressure output of $\sim$43 mV is obtained, which translates into an initial voltage output of $\sim$2.78 V for the integrated sensor. On the other hand, the maximum voltage at the output of the amplifier is $\sim$3.15. This means that, for the sensor above, the maximum output swing is $\sim$370 mV, which corresponds to the pressure range 0–0.7 bar. For higher pressures, the output saturates.

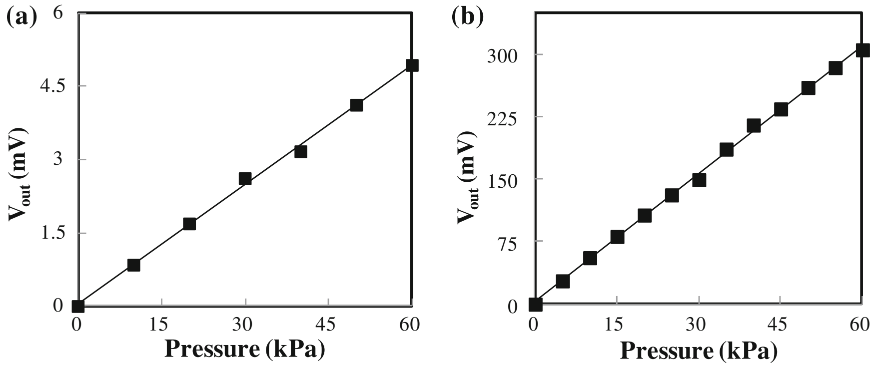

Fig. 7.23 Measured output voltage versus applied pressure for (**a**) a stand-alone pressure sensor and (**b**) the same sensor + an instrumentation amplifier with fixed gain. The pressure sensor is 250 × 250 μm^2 with design D2 (see Fig. 6.3). The data point at vacuum is taken as reference for the data, to eliminate the offset. The data points are fitted to a linear function. In (**b**) the last three points had to be obtained by data extrapolation due to saturation of the output voltage

Table 7.5 Measured output voltage for different switches configuration for a sensor integrated with a variable gain amplifier. The output of the sensor alone, together with the measured and calculated gains (from (7.1)) are also listed. The measurements were performed under 1 bar external pressure

R_3				R_2				R_3	R_3	V_{out}	V_{out}	Gain[a]	Gain
S_4	S_3	S_2	S_1	S_4	S_3	S_2	S_1	(KΩ)	(KΩ)	(S+A) (V)	(Sensor) (mV)		calculated
0	0	0	1	1	0	0	0	50	3	1	48.4	20.8	22.2
0	0	1	0	1	0	0	0	100	3	1.75	48.4	36.4	44.3
0	0	0	1	0	1	0	0	50	5	0.63	48.4	13	13.5
0	0	0	1	0	0	1	0	50	7	0.44	48.4	9.1	9.7
0	0	0	1	0	0	0	1	50	10	0.34	48.4	7.1	6.8

[a] Calculated as the ratio of the sensor output voltage measured before and after amplification

Another problem occurs for pressure sensors with negative offset, since the amplifier was designed to work only for positive inputs. Combining the condition of positive offset with the saturation problem, we can conclude that only sensors with an offset between 0 and 50 mV can, at least partially, be tested. Moreover, a problem with the ESD protection (Fig. 7.10) after the MEMS post-processing was observed: the diodes start conducting at voltages below 3.3 V, clipping the voltage and causing a short between the signal and power lines and the malfunctioning of the circuit. Due to this, modules with ESD protection, i.e. three modules out of seven per die, will not work .The stringent offset condition combined with the ESD problem, plus other MEMS processing issues (like broken membranes due to delamination), caused that only one integrated sensor with fixed-gain amplifier (in a whole wafer) could be properly tested.

Regarding the integrated sensors with variable gain amplifiers, the offset limitation is more flexible since the gain can be increased or decreased as needed. However,

as these type of sensors require nine or eleven probes to be tested, depending on the type of resistors used (“interdigitated” or “serpentine”), and the maximum number of probes in the PAV is eight, their pressure response could not be tested. A possible solution to this problem would be to add an “arm” with a 24-pin standard probecard to the pressure chamber. Due to time limitations, this option could not be further explored. For this reason, this type of integrated sensor could only be tested at 1 bar (atmospheric pressure) using the measurement setup employed to characterize the CMOS circuit, and described in Sects. 7.1–7.4. Table 7.5 lists the measurement results of one sensor integrated with “variable-gain” amplifier. As can be observed, the device worked as expected: different output voltages depending on the selected resistance values, and a measured gain (obtained dividing the output voltage of the sensor + amplifier by the output voltage of the sensor alone) close to the gain exhibited by the amplifier before the MEMS processing.

7.5 Conclusions

A prototype integrated poly-SiGe-based piezoresistive pressure sensor directly fabricated above its readout circuit has been presented. A classic three op-amp instrumentation amplifier acted as the readout circuit of the pressure sensor. The surface-micromachined piezoresistive pressure sensor consisted in a poly-SiGe membrane with four poly-SiGe piezoresistors placed on top in a Wheatstone bridge configuration, as described in previous chapters. Tungsten-filled vias were used to connect the CMOS Cu top metal layer and the Al MEMS bottom electrode.

In this chapter, the CMOS readout circuit design, layout generation, fabrication and electrical evaluation have been described in detail. A modified version of imec 0.13 μm Cu-backend CMOS technology, with thicker oxide (∼7 nm instead of ∼2 nm) in order to allow for a higher bias voltage, has been used. Two Cu metal layers were provided for interconnections, with Cu-filled metal-to-metal vias and oxide intermetal dielectric. Two types of instrumentation amplifiers have been considered: with fixed gain and with variable gain. In the variable-gain amplifiers, the standard resistors have been replaced by “resistive blocks”, which include several resistors connected in parallel through switches. By activating the corresponding switch, the desired resistance value is selected. The fabricated circuits exhibited a behavior very close to that predicted by simulations.

The impact of the MEMS processing on the CMOS circuit and the CMOS-MEMS interface has also been studied. The CMOS circuit showed no significant deterioration after the MEMS processing, although a resistance increase for the Cu-filled metal-to-metal and the tungsten-filled CMOS-MEMS vias was observed.

Measurements of an integrated sensor with a $250 \times 250\ \mu m^2$ membrane and fixed gain amplifier showed a sensitivity of ∼159.5 mV/V/bar, about 64 times higher than the stand-alone pressure sensor (∼2.5 mV/V/bar). For pressure sensors integrated with a variable gain amplifier, different sensitivities were obtained depending on the switch selection.

The devices presented in this chapter represent the first integrated poly-SiGe pressure sensors directly fabricated above their readout circuit. It is also the first time that a poly-SiGe MEMS device is processed on top of Cu-backend CMOS. The results obtained in this work demonstrate that the poly-SiGe MEMS process flows can potentially be compatible with post-processing above Cu-based CMOS, broadening the applications of poly-SiGe to the integration of MEMS with the advanced CMOS technology nodes. However, to ensure the complete CMOS-compatibility of the presented poly-SiGe flow, extra work is needed to better understand, and prevent, the observed deterioration of the Cu-filled CMOS vias after MEMS post-processing.

The presented integrated sensor is not in any way complete: the readout circuit includes only the amplifier stage, ignoring some of the fundamental parts of any piezoresistive sensor interface circuitry: temperature and offset compensation. Moreover, from the MEMS side, the poly-SiGe piezoresistive pressure sensor was not designed to fulfill typical performance requirements (in terms of temperature dependence, offset, linearity, etc). For these reasons, the integrated pressure sensor fabricated in this work may not have an immediate commercial application. However, as a demonstrator, it has a high significance.

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