Chapter 4
The Pressure Sensor Fabrication Process

This chapter describes in detail the pressure sensor fabrication process. the maximum processing temperature of the complete sensor, including the poly-SiGe piezoresistors, is kept below 460 °C to enable above-CMOS integration. The developed process allows for the simultaneous fabrication of both piezoresistive and capacitive pressure sensors. It can also be used to fabricate sensors of different size and with different requirements (i.e, sensitivity, nonlinearity, sealed-in pressure, etc). Many of the process steps used in the fabrication of the pressure sensor are borrowed from the thin-film packaging flow, part of the SiGe-MEMS platform in imec.

Section 4.1 presents a generic cross-section of a combined piezoresistive/capacitive pressure sensor. Section 4.2 describes the different steps of the developed process flow for the fabrication of the pressure sensor. In Sect. 4.3 a more detailed description of the different process developments performed at imec specifically for the pressure sensor is given. The chapter ends with a summary of the developed fabrication process.

4.1 The Pressure Sensor Fabrication Process: A Generic Technology

One of the main challenges during the development of the pressure sensor fabrication process was to build-up a process flow compatible with post-processing on top of CMOS, to allow for the monolithic integration of MEMS-above-CMOS. In order to avoid introducing any degradation in the underlying CMOS circuitry, some care has to be taken during the fabrication of the MEMS pressure sensor: firstly, the electronic circuit needs a good passivation, so that it is well protected from the aggressive etch and deposition steps which are needed to fabricate the MEMS devices; and secondly the processing temperature for each step in the MEMS process flow needs to be low enough so that the performance of the underlying CMOS circuit is not deteriorated. The thermal budget limits for standard 0.35 and 0.25 μm CMOS wafers

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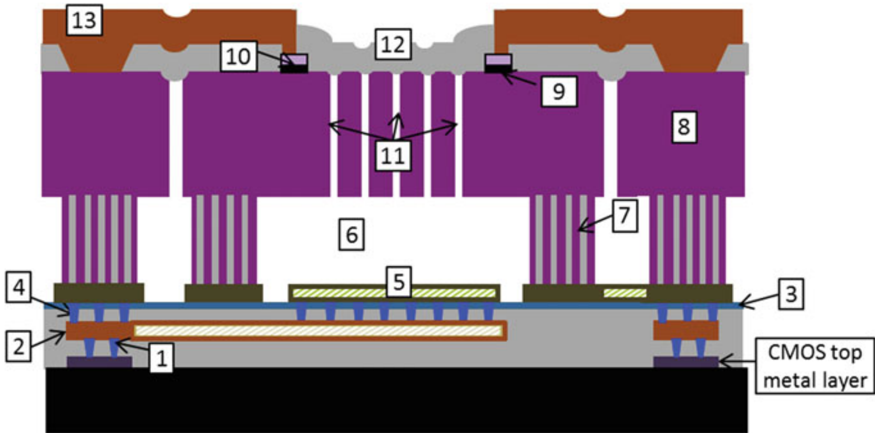

Fig. 4.1 Cross-section of a generic capacitive/pressure sensor. *Dashed parts* are only present if capacitive sensing is also required; for piezoresistive-only sensors they are unnecessary

with aluminum based interconnects have already been experimentally investigated in [1] and [2], respectively. In both cases it was found that the degradation of the metal interconnects, rather than the transistor performance, is the limiting factor. In [1] a degradation of the interconnect resistance at temperatures above 450 °C was reported. In [2] an increase of more than 10 % in via resistance was found after only 2 h annealing at 450 °C. In this work the maximum processing temperature of the complete sensor, including the poly-SiGe piezoresistors, is kept below 460 °C to enable above-CMOS integration.

The developed fabrication process can be used to fabricate a capacitive, piezoresistive or a combined capacitive/piezoresistive pressure sensor. Figure 4.1 shows a cross-section of a pressure sensor that can be simultaneously used as capacitive and piezoresistive sensor. In appendix A, a layout of such a sensor is presented.

The different layers and structural components that form the pressure sensor are numbered in the figure and listed below.

1. **CMOS-MEMS via.** This via connects the top CMOS metal layer (Cu) to the bottom metal electrode of the MEMS (Al). As this work represents the first attempt in IMEC to build a poly-SiGe MEMS device on top of Cu CMOS, this module was specifically developed within this thesis. More details on the processing and electrical characterization of this copper to aluminum via will be given in Chap. 7.
2. **MEMS metal electrode.** This Ti/AlCu(0.5 %)/TiN metal electrode is the first MEMS device layer in the process flow. It functions as intermediate metal layer between the top CMOS metal layer and the MEMS SiGe electrode. It can also be used as a connection between the bondpad and the bottom electrode in capacitive pressure sensors, as depicted in Fig. 4.1. In thin-film packaging applications this

metal electrode provides an electrical feed through connection to the packaged device.

3. **CMOS passivation layer.** The purpose of this layer is to protect the metal electrodes and the underlying dielectric layers and CMOS circuit during the MEMS processing. Especially aggressive is the etching of the sacrificial oxide to release the sensor membrane, performed in vapor hydrogen-fluoride (vHF). A 400 nm-thick silicon carbide (SiC) is used as passivation layer. SiC was the selected material as it is resilient to the MEMS release process and it has good electrical isolation. SiC is also thermally stable, which assures that its microstructure does not change during the high temperature deposition steps and it is a very dense/hard material, so that the chemicals cannot diffuse through it [3–5] and attack the CMOS circuit.
4. **MEMS via.** These Tungsten-filled vias provide an electrical connection between the MEMS metal electrode and the MEMS SiGe electrode, through the SiC passivation layer.
5. **SiGe MEMS electrode.** These electrodes can be used to form the electrical interconnect between the different MEMS structures. For example, in a capacitive pressure sensor, the electrode layer provides an electrical path to connect the sensor membrane to the corresponding biasing bondpad. Also in the capacitive pressure sensor this electrode is the bottom plate of the capacitor. A 400 nm-thick CVD-deposited poly-SiGe layer is used as MEMS electrode.
6. **Gap.** The gap is the separation between the SiGe membrane and the SiGe bottom electrode. For capacitive pressure sensors, a smaller gap is preferred as it translates into a bigger (and therefore easier to measure) initial capacitance; it also results in improved sensitivity. For piezoresistive pressure sensors, the depth of the gap does not have an influence in sensor sensitivity. In general, the depth of the gap limits the maximum deflection of the membrane, and together with the maximum tensile strength of the membrane, limits the maximum pressure that the sensor can withstand, determining thus the working range of the device. This is not necessarily true for capacitive pressure sensors as they can also work in "touch" mode [6]. The gap depth is defined by the thickness of the deposited sacrificial oxide. Therefore, it is scalable: it can be easily made larger or smaller depending on the specifications of the required application. In this thesis, a nominal gap of 3 μm was used. For 1 wafer a gap of 1 μm was used to improve the performance of the capacitive sensors, as will be seen in Chap. 6.
7. **Anchor.** Trenches are etched in the sacrificial oxide, stopping in the underlying MEMS electrodes, and filled with SiGe (during the structural layer deposition) to define the anchors. These SiGe anchors fulfill two purposes. First they provide support to the MEMS structural layer. In this thesis, a 25 μm-wide ring of anchors surrounds each sensor, holding the membrane. And second, they offer an electrical connection to the SiGe electrode underneath. To ensure a nice SiGe filling and a planarized membrane layer after deposition, a fixed trench width of 0.8 μm was used in this work. The chosen anchor design (Fig. 4.2) consists of crossing vertical and horizontal anchor lanes with a spacing of 2.2 μm. This anchor design was

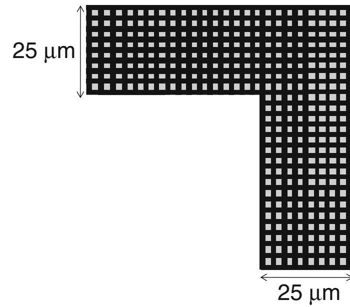

Fig. 4.2 Anchor design. The poly-SiGe anchors (in *black*) have a width of 0.8 μm and are separated by 2.2 μm-wide oxide (in *light grey*) trenches

already used by Claes in [7] and proved to be robust enough for thin film packaging applications, as it meets the MIL-standard requirements for shear strength.

8. **SiGe structural layer.** This layer constitutes the sensor membrane. As already shown in Chap. 3, a thinner membrane results in a larger deflection for a certain applied pressure, therefore increasing the sensitivity of the pressure sensor. In practice, the membrane thickness will be defined according to requirements such as maximum working pressure, sensitivity or linearity. In this work, a fixed SiGe structural thickness of 4 μm was used, although other thicknesses, ranging from 1 to 10 μm, are supported in imec SiGe MEMS platform.
9. **Isolation layer.** This layer provides isolation between the SiGe membrane and the SiGe piezoresistors. A thin (100 nm) SiC layer is used as isolation layer. SiC is the selected material as it offers good electrical isolation and it is resilient to vHF, therefore preventing the SiGe piezoresistors to be etched off during the release process. This SiC isolation layer is later patterned: it only remains below the piezoresistors, being etched away everywhere else. In this way its impact in the overall sensor performance is minimized.
10. **Piezoresistors.** A thin undoped SiGe layer is deposited on top of the SiC isolation layer. After deposition this layer is boron implanted and annealed to create the poly-SiGe piezoresistive layer. The implantation and annealing conditions affect the piezoresistive and electrical properties of the layer, as was already explained in Chap. 2, and can be adapted according to the required specifications. It is important to note that steps 9 and 10 are specific for piezoresistive pressure sensors, and do not need to be implemented if only capacitive sensors are sought.
11. **Release holes.** Access holes are opened on the SiGe structural layer to provide a path for the vHF to etch away the sacrificial oxide beneath the membranes. In order to reduce the time required to etch away the sacrificial layer, and also preventing in this way attacking the anchor region, etch ports are opened in the membranes on top instead of using lateral etch paths. A symmetrical pattern of square release holes of $1 \times 1\,\mu m^2$ was used (Fig. 4.3). The size of the release holes was selected to be large enough to enable efficient sacrificial etching but, at the same time, small enough to limit both the required thickness of the sealing layer and the quantity of sealing material deposited on the interior surfaces of the cavity. The deposited sealing material will increase the membrane thickness.

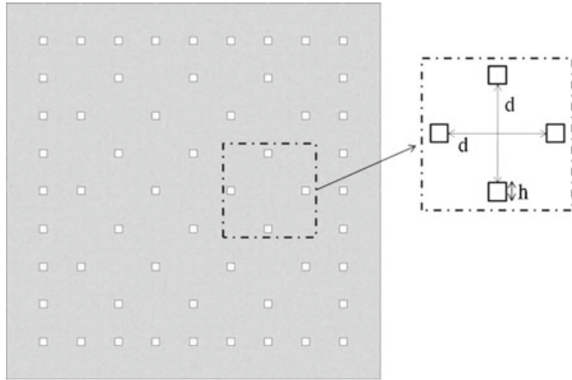

Fig. 4.3 Top view of a perforated square membrane with square vertical release *holes*. On the *right*, a close view of the designed pattern of release *holes*, where h is 1 μm and d is 9.5 μm

For pressure sensor applications, a thin sealing layer is preferred to avoid degradation of the sensor sensitivity. A thin sealing layer also leads to less bi-material effects and ensures that the average membrane properties are close to those of the preferred SiGe material.

12. **Sealing layer.** The release holes are sealed by thin-film deposition. This layer must provide a hermetic sealing of the released cavity. Different sealing layers were considered in this thesis, as will be explained in detail in Chap. 5.
13. **Metal interconnect.** This metal layer provides electrical connection among the piezoresistors (in a Wheatstone bridge configuration) and between the piezoresistors and the bondpads. An AlCu (0.5 wt.%)-based stack is used for this purpose in this work. As modules 9 and 10, this metal interconnect is only necessary for piezoresistive pressure sensor.

These are the most important layers and modules that constitute the pressure sensor fabricated in this thesis. Most of these modules are part of the standard imec SiGe MEMS platform. With the exception of modules 9, 10 and 13, the pressure sensor fabrication process is similar to the imec thin-film packaging process flow [8]. Modules 9, 10 and 13 are particular for piezoresistive pressure sensors and were specifically developed in the frame of this thesis. Also module 1 was developed as part of this thesis, although it can be used for the integration of any MEMS with Cu-based interconnects CMOS circuit. Although module 12 is also part of the thin-film packaging flow, the sealing layer specifications for pressure sensor applications are not necessarily the same as for thin-film packaging. For this reason, an important part of this thesis was dedicated to the study and evaluation of different sealing layers (Chap. 5).

Finally, it is important to note that the developed pressure sensor processing was conceived as a generic technology. Many of the above mentioned modules can be tuned according to the specifications of the considered application. For example, the gap depth and the SiGe structural layer thickness can be easily scalable. Also the properties of the poly-SiGe sensing layer (for piezoresistive sensors) can be controlled by the implantation and annealing conditions. Moreover, this technology allows for both piezoresistive and capacitive pressure sensors to be fabricated simultaneously.

4.2 Pressure Sensor Schematic Process Flow

Poly-SiGe pressure sensors of different areas (200 × 200, 250 × 250, 300 × 300 and 350 × 175 μm^2) were fabricated using surface micromachining. Figures 4.4 and 4.6 give an overview of the pressure sensor schematic process flow. For simplicity only the parts that are relevant for the piezoresistive pressure sensor are drawn. This chapter deals exclusively with the processing of the stand-alone pressure sensors, starting at the metal electrode. The fabrication of a CMOS-integrated pressure sensor, including the CMOS-MEMS via module, will be explained in Chap. 7.

Figure 4.4 shows the first part of the pressure sensor fabrication process. This part includes the metal and SiGe electrodes deposition and patterning, the MEMS via formation and the deposition and patterning of the sacrificial oxide to define the anchors. All these modules are part of the standard SiGe MEMS platform, and were already reported in [8] and [9] for the fabrication of SiGe thin-film packages and SiGe resonators, respectively.

A standard 8-in-diameter Si (100) wafer is used as starting substrate. We first deposit 1 μm of High Density Plasma (HDP) Si-oxide to electrically isolate the

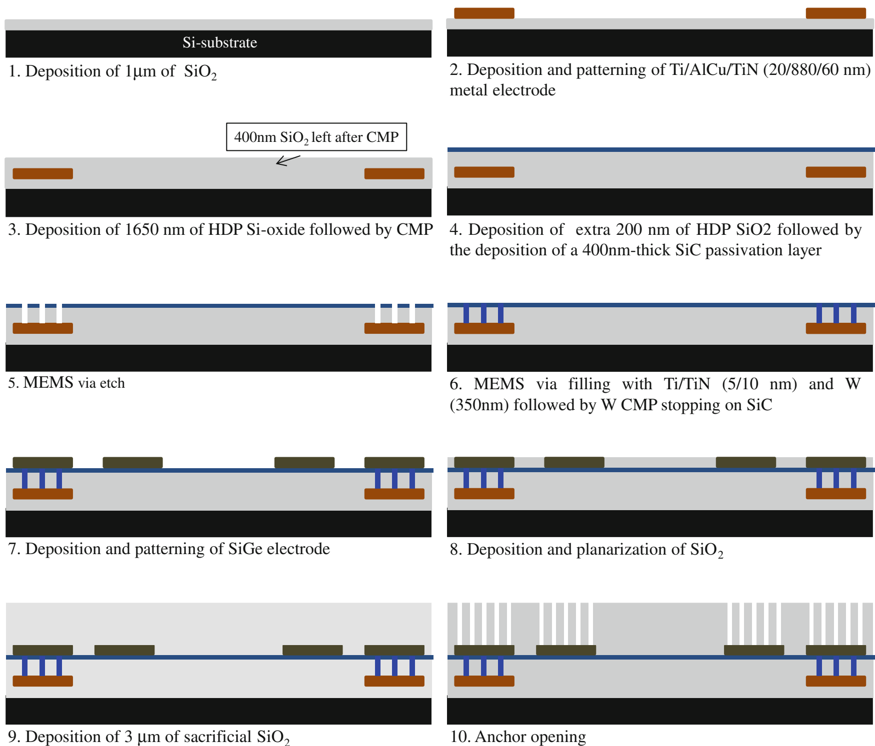

Fig. 4.4 Part I of the process flow of the fabricated pressure sensor. Note that scales are distorted

metal electrodes from the conductive Si-substrate. A metal stack composed by 5 nm of Ti, 880 nm of AlCu (0.5 wt %) and 60 nm of TiN is deposited and patterned next to define the metal electrodes. In the pressure sensor design, the metal electrodes only appear in the bondpad regions and below the membranes of those sensors designed to be used both as piezoresistive and capacitive pressure sensors. After the metal electrode patterning, a 1,650 nm-thick HDP Si-oxide layer is deposited, followed by the backside deposition of a 200 nm-thick Si-nitride layer for stress compensation. A chemical mechanical polishing (CMP) step is then performed to obtain a planarized surface. This CMP operation is time-controlled, with weight measurements performed right before and after to target for a thickness of $\sim$400 nm of remaining oxide layer on top of the metal electrodes. 200 nm extra HDP Si-oxide is then deposited, followed by the deposition of the 400 nm-thick SiC passivation layer. The purpose of this SiC layer, as explained above, is to protect the metal electrodes during the aggressive vHF MEMS release process. Two annealing steps of 30 min at a temperature of 455 °C are performed right before and after the SiC deposition. The purpose of the pre-deposition annealing step before the SiC protection layer deposition is to ensure a proper outgassing of the underlying layers. As the SiC is very hermetic, if the underlying layers still outgas after SiC deposition, bubbles below the SiC could be formed. The post-deposition annealing step is to promote densification of the SiC passivation layer, eliminating possible defect paths in the SiC that could allow infiltration of vHF during the release process.

The MEMS vias are then opened to provide electrical connection, through the SiC and Si-oxide layers, to the underlying metal electrodes (Fig. 4.5a). These MEMS vias are square in shape with a fixed dimension of $0.5 \times 0.5\ \mu m^2$ and a maximum spacing of 10 μm. A thin Ti/TiN (15/10 nm) layer followed by 350 nm of tungsten (W) is then deposited to fill the vias. An 18 nm Argon (Ar) pre-sputtering is performed before the Ti/TiN filling to remove any possible native oxide that could degrade, or even kill, the future electrical connection. To avoid blistering of the W, an anneal step (30 min at 455 °C) is done in between the Ti/TiN and the W depositions. After via filling, a CMP step is performed to remove the W everywhere except in the vias.

A 400 nm-thick highly boron doped ($B{\sim}1 \times 10^{21} cm^{-3}$) SiGe layer is deposited and patterned next to define the SiGe bottom electrodes. In the pressure sensor design these SiGe electrodes are defined in the bondpad regions, below the membrane anchors and, in the case of capacitive sensors, below the membrane itself (bottom electrode). This electrode is later embedded in an 800 nm-thick layer of sacrificial oxide followed by CMP with stop on the SiGe electrode to realize a flat topography (Fig. 4.5b). This CMP step to planarize the SiO_2 layer is necessary due to the topography created by the SiGe electrodes when SiO_2 is grown over them. This topography can limit the resolution of the following litho steps and makes subsequent deposition/etch steps more challenging. During the pressure sensor fabrication process several CMP steps are included to ensure a planarized surface, avoiding unwanted topography.

The bulk of the sacrificial oxide layer is deposited next, on top of the planarized SiGe electrode. The thickness of this sacrificial layer will determine the gap between the free standing membrane and the bottom electrode, as depicted in Fig. 4.1. In this

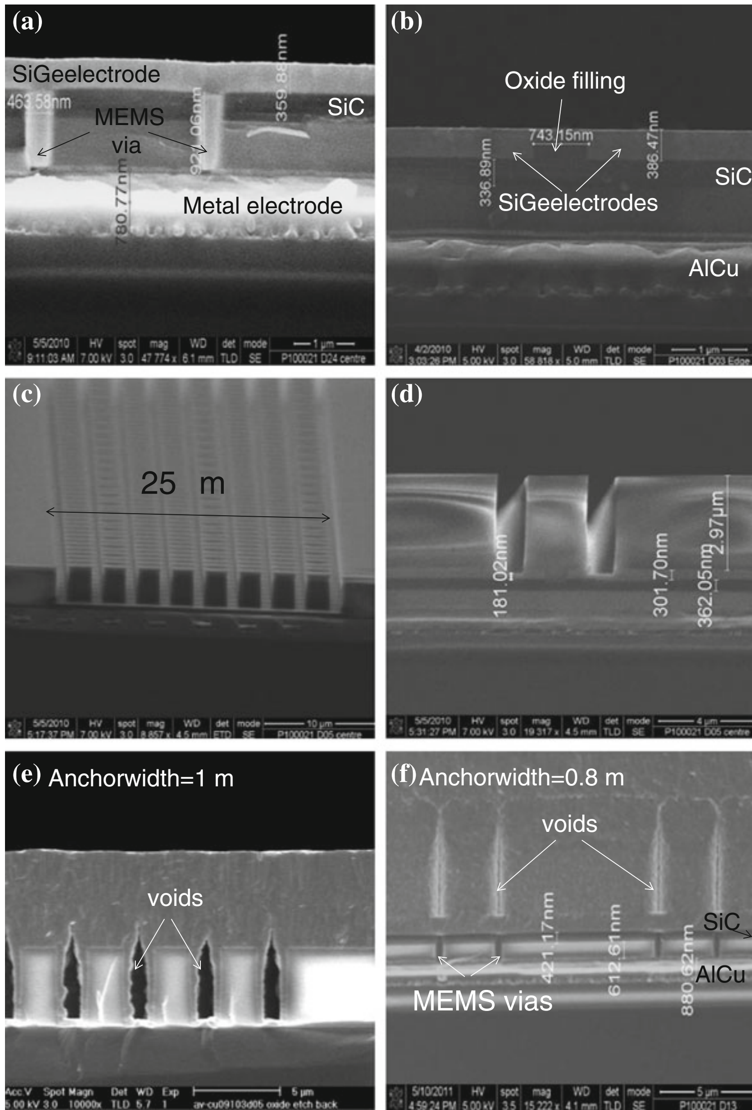

Fig. 4.5 Cross-section pictures illustrating different steps in the pressure sensor process flow. **a** SiGe and metal electrodes with SiC passivation layer in between. The MEMS via connections are also visible. **b** SiGe electrodes embedded in sacrificial oxide after CMP. **c** and **d** show the anchor trenches etched in the sacrificial oxide. During the oxide etch the SiGe electrode layer underneath is attacked. Anchor filling by SiGe for a width of **e** 1 μm and **f** 0.8 μm

work, the nominal thickness of the HDP Si-oxide layer used as sacrificial material is 3 μm, although for one wafer a 1 μm-thick HDP Si-oxide layer was used instead to improve the performance of the capacitive sensors (see Chap. 6).

To define the anchor region, trenches are opened in the sacrificial Si-oxide by physical plasma etch using Ar as etch gas (Fig. 4.5c and d). As explained in Sect. 4.1, these anchors serve two purposes: they form the electrical contact to the lower electrodes and they anchor the structural layer to the bulk of the wafer. In the pressure sensor design, the total anchor region surrounding each membrane is 25 µm. Anchor trenches are also etched in the bondpad regions. Initially, an anchor width of 1 µm was used. However, the SiGe filling of these trenches during the structural layer deposition was not perfect, leaving voids as can be seen in Fig. 4.5e. For this reason the anchor width was reduced to 0.8 µm, resulting in a nicer SiGe filling (Fig. 4.5f).

All the processing steps explained up till now are part of the standard imec SiGe MEMS platform. Figure 4.6 shows the second part of the pressure sensor process flow, which includes pressure sensor specific modules like piezoresistors and metal interconnects.

The SiGe structural layer is now deposited. An annealing step of 30 min at 455 °C is performed before the SiGe deposition to ensure a proper outgassing of the underlying layers, avoiding the formation of bubbles later on. A thin Ti/TiN (5/10 nm) is deposited first to improve adhesion and avoid delamination; it also lowers the contact resistance between the SiGe electrodes and the SiGe structural layer [10]. The B-doped poly-SiGe structural layer is then deposited at 460 °C chuck temperature (450 °C wafer temperature) by a combination of CVD and PECVD (Plasma Enhanced CVD). The CVD and PECVD depositions are both performed in an Applied Materials PECVD Centura CxZ chamber. The silicon gas source is pure silane, whereas 10 % germane in hydrogen has been used as the germanium gas source. The boron gas source is 1 % diborane in hydrogen. Table 4.1 lists the deposition conditions. During the two PECVD depositions, an extra H_2 flow is included since hydrogen is shown to be beneficial for the crystallinity and uniformity of the deposited layer [11].

The PECVD SiGe layer is deposited on top of a polycrystalline CVD SiGe seed layer (∼400 nm-thick); the CVD layer forms a crystalline seed for the PECVD SiGe growth [12] and it also refills the anchor trenches, thanks to the good step coverage of the CVD process. The maximum thickness of PECVD SiGe that can be deposited before a chamber clean is required is ∼2 µm. If a thicker layer is needed, PECVD layers can be stacked until the final thickness is reached. In this case, a 30 s CF_4 clean is performed before each extra PECVD deposition to remove any unwanted oxide at the PECVD/PECVD interfaces [13]. The stack to achieve the 4 µm thick structural layer used in this work is composed by a 400 nm-CVD seed layer +1.6 µm PECVD +2 µm PECVD SiGe layer. The total deposition time for the SiGe structural layer is ∼40 min. The Ge concentration, as determined by Rutherford Backscattering , is ∼75 % for the CVD layer [14]. The obtained poly-SiGe layer exhibited mechanical and electrical properties suitable for MEMS applications [8]: a tensile residual stress around 70 MPa, a stress gradient below $10^{-5}/\mu m$ and an electrical resistivity below 4 mΩ· cm. The Young's modulus, obtained by nanoindentation, is 147 GPa.

After the SiGe structural layer deposition, a CMP (Chemical Mechanical Polishing) process is applied to planarize and smooth the poly-SiGe membrane surface. A flat smooth top surface is important to facilitate the adhesion of the future

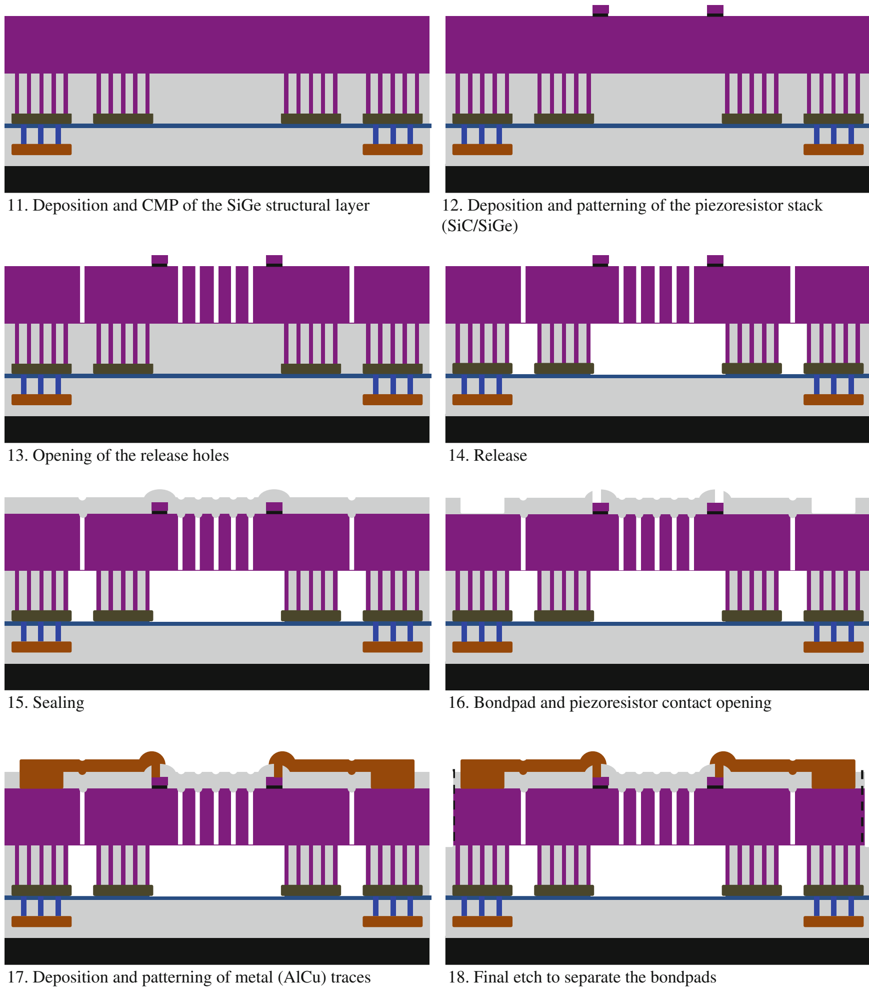

Fig. 4.6 Part II of the pressure sensor process flow. Note that scales are distorted

piezoresistive layers; moreover unwanted topography or roughness can limit the resolution of the following litho steps and makes subsequent deposition/etch steps more challenging. This CMP is also partially responsible for the fact that the final poly-SiGe thickness (~3.5 μm) is slightly lower than the targeted 4 μm.

The piezoresistor stack is deposited next. First a thin (100 nm) SiC layer is used as isolation layer between the SiGe membrane and the SiGe piezoresistors. Then a 200 nm-thick CVD undoped poly-SiGe layer with a Ge content of 77 % (determined by RBS) is deposited as piezoresistive layer. This poly-SiGe piezoresistive layer is deposited at 460 °C chuck temperature (450 °C wafer temperature) in the same tool used for the poly-SiGe structural layer. The deposition time is ~12 min.

Table 4.1 Deposition conditions for the 4 µm-thick (CVD + PECVD + PECVD) poly-SiGe structural layer used in this work. The conditions for the CF4 clean performed before the second PECVD deposition are also listed

	Base layer		**CF_4-interclean**	**2nd PECVD layer**
	CVD	**PECVD**		
Thickness	400 nm	1.6 µm	–	2 µm
Time (sec)	810	610	30	780
Pressure (Torr)	4.3	5.4	1	5.4
H_2 (sccm)	0	450	0	450
CF_4 (sccm)	0	0	560	0
SiH_4 / GeH_4	0.9	0.4545	0	0.4545
B_2H_6 (sccm)	10	50	0	50

The electrical and piezoresistive properties of this layer for different doping concentrations and annealing conditions were already reported in Chap. 2 (layer 4 in Table 2.1).

After deposition, the poly-SiGe film was doped through ion implantation of boron at 35 keV with a dosage of 2×10^{14} cm^{-2} (concentration 1×10^{19} cm^{-3}). This boron concentration resulted in the highest gauge factor (Chap. 2) and was therefore the one selected for the piezoresistive layer in the pressure sensor. After implantation, the films are annealed in a conventional furnace at 455 °C. The selected annealing time was 30 min, although the optimum annealing time for maximum gauge factor is 1 h (see Chap. 2). Delamination of the piezoresistor layers and the SiGe structural layer was observed after sinter for 1h (Fig. 4.7a). This delamination might be due to the stresses generated in the layers due to the thermal budget; also outgassing of the underlying layers was proposed as explanation. To limit this delamination issue in this work, it was decided to limit the annealing time to 30 min; also, the annealing step was moved after piezoresistor patterning. In this way delamination of the piezoresistor layers is avoided, although bubbles in the SiGe structural layer (especially in the unpatterned region at the edge of the wafers) are still observed (Fig. 4.7b). In the future, extra annealing steps could be included before and after the 100 nm-thick SiC isolation layer to improve adhesion of the piezoresistors and allow a longer doping activation anneal.

After litho, the piezoresistor stack is patterned in two consecutive dry etch operations; first, the SiGe piezoresistive layer is etched, and then the SiC isolation layer is also etched away, remaining only below the piezoresistors. In this way the effect of this SiC isolation layer in the sensor membrane response is minimized. During this SiC etch, there is an overetch (~100 nm) of the underlying SiGe structural layer (Fig. 4.8). The poly-SiGe structural layer is then patterned and plasma-etched in order to open the release holes. A symmetrical pattern of square release holes of nominally $1 \times 1 \mu m^2$ with a maximum spacing of 9.5 µm was used (Fig. 4.3). The final size of the release holes after etch is $\sim 1.2 \times 1.2 \mu m^2$ (Fig. 4.9).

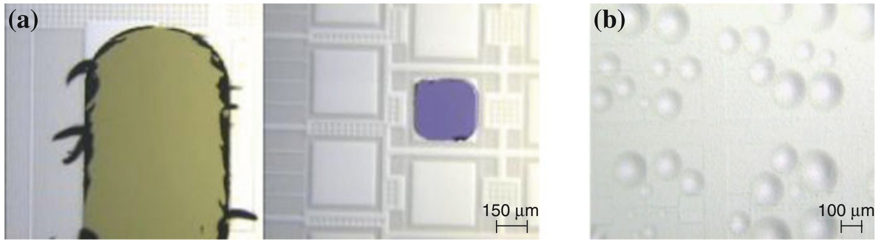

Fig. 4.7 Microscope pictures after piezoresistor annealing. In **a** the annealing step is performed before piezoresistor patterning while in **b**, it is performed afterwards. In **a** delamination of the piezoresistor layers and structural layer is observed. On the *right picture* a pressure sensor membrane is gone. In **b** *small bubbles* in the structural layer, especially at the edge of the wafers, can be observed

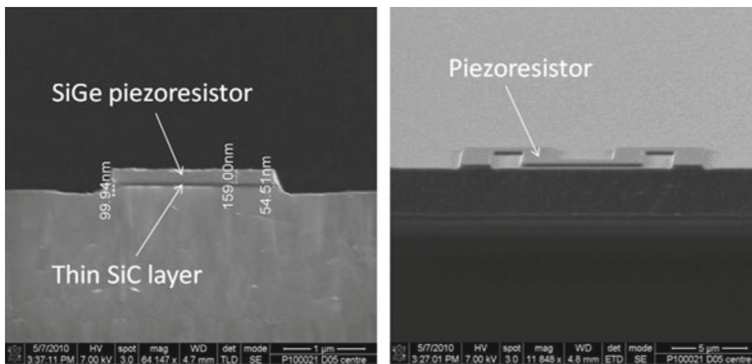

Fig. 4.8 Piezoresistor stack (SiC + SiGe) patterning. Around 100 nm of SiGe membrane is consumed during piezoresistor etch

All sacrificial oxide inside the cavities is removed by vHF on a Primaxx Clean Etch Technology (CET) tool. To avoid stiction during the release, AvHF (Anhydrous Vapor HF) together with ethanol vapor [15] is used to etch the sacrifical oxide. After release, the membranes are sealed with Si-oxide (Fig. 4.10b). The sealing oxide is then opened using a dry etch process to create contact vias on top of the piezoresistors and bondpads (Fig. 4.10c). In the sensor layout two masks were included for this via etch: one mask to pattern the contacts on top of the piezoresistors (CWPIEZO) and a second mask to open the bondpads (MEMPASS). If only stand-alone pressure sensors are desired, only the contacts above the piezoresistors need to be opened. For CMOS-integrated and/or capacitive pressure sensors the opening of the bondpads is also necessary. In this case both exposures (CWPIEZO + MEMPASS) can be performed together in the same litho operation.

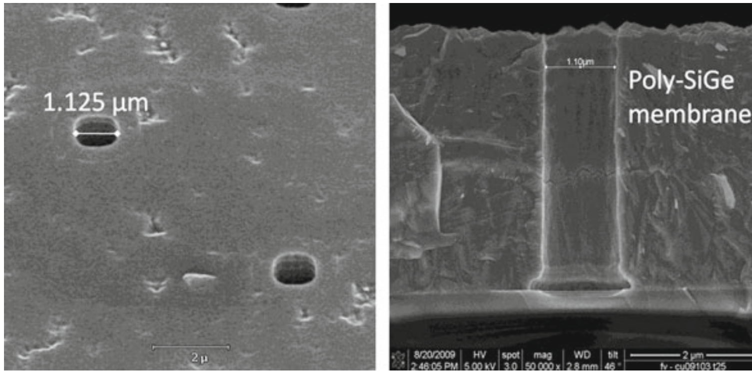

Fig. 4.9 Top and cross-section SEM pictures of a perforated membrane before release. The *holes* size after etch is slightly bigger than the printed dimension ($1 \times 1\,\mu m^2$). In the picture on the right the interface between the two PECVD SiGe layers is visible. Also an overetch "pocket" at the oxide interface can be observed

A Ti/AlCu (0.5 wt%)/TiN metal stack was then deposited and patterned to contact the piezoresistors. Note that this is the same metal stack used to define the metal electrodes at the beginning of the flow. The inital Ti layer helps to fill the contacts thanks to its great conformality. The final TiN layer is included to facilitate lithography. From Fig. 4.10d we can see that the metal stack does not fill the piezoresistor contacts nicely. This problem will be analyzed in detail in Sect. 4.3.5.

After patterning the metal interconnects, a final lithography step operation, followed by the etching of the sealing Si-oxide and the SiGe membrane, is performed to pattern the sensors, separating the cavities from one another and isolating the bondpads. Figure 4.10e shows a sensor membrane and two bondpads after this final etch. The AlCu metal traces connecting the bondpads with the piezoresistors remain "hanging" over the trench separating membrane and bondpad. It is important to mention that these 1.5 µm-wide isolation trenches are etched at the same time as the release holes and they remain protected by resist during this final etch. Therefore these trenches remain filled with sealing oxide, which acts as a support for the metal traces, preventing them from breaking. Note that, as the vHF during the release step only etched the sacrificial SiO_2 below the membranes and below the small, a ring of sacrificial SiO_2 remains surrounding each sensor, increasing the robustness of the membranes (Fig. 4.10f). Note also that, if only stand-alone piezoresistive sensors are sought, this final litho/etch operation is unnecessary since the bondpads are not opened and therefore they are not electrically connected.

4.3 Process Developments and Challenges

During the fabrication of the pressure sensor a number of challenges were faced, like the bad piezoresistor contact discussed before. Moreover some processing steps, that are specific for a piezoresistive pressure sensor and therefore not part of imec's SiGe

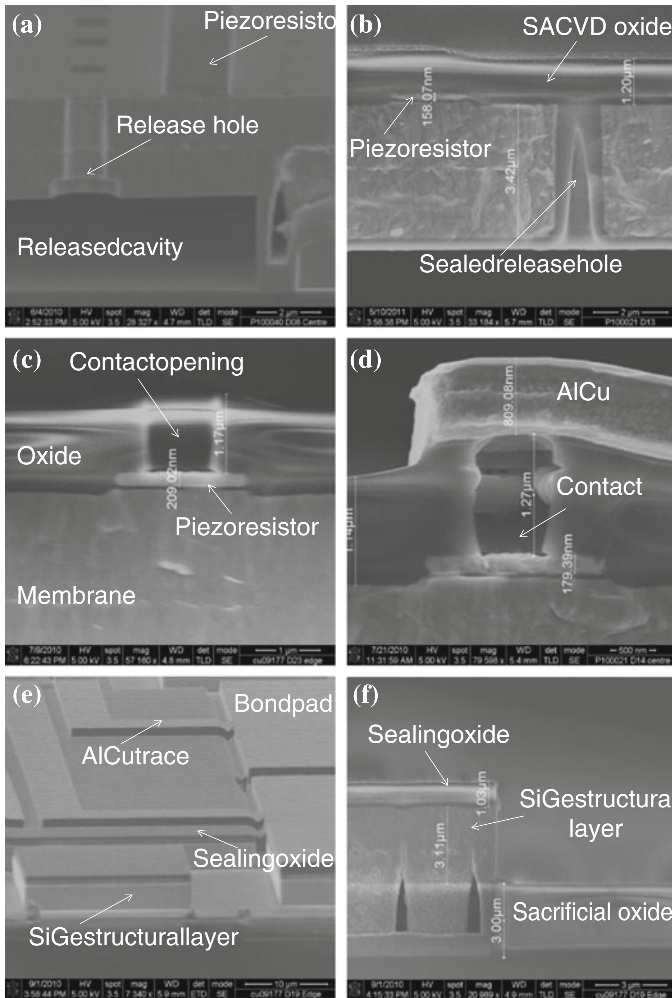

Fig. 4.10 Cross-section pictures illustrating different process steps in the second part of the pressure sensor fabrication flow. **a** Membrane release. Note that the piezoresistors, exposed during the release in vHF, remain unattacked. **b** Sealing of the released membranes with oxide. A piezoresistor embedded in sealing oxide is visible. **c** Etching of the sealing oxide to contact the piezoresistors. **d** Contact filling by the metal stack deposited to connect the piezoresistors. **e** and **f** Patterning of the sealing oxide and SiGe membrane to isolate bondpads and seaparate sensors from one another. Note that a ring of sacrificial oxide remains surrounding the structures

MEMS platform, needed to be developed in the frame of this work. These challenges and process developments are summarized in this section.

4.3.1 Piezoresistive Layer

A key part of this thesis was the development of a SiGe layer deposited at temperatures below 460 °C with good piezoresistive properties to be used as sensing layer in the pressure sensor. The existing SiGe layers in imec's MEMS platform, used for example as electrodes or structural layers, are deposited *in situ* doped with a high concentration of boron ($> 1 \times 10^{20} cm^{-3}$). At such high dopings, semiconductors exhibit metallic behavior with limited piezoresistive effect [16]. The solution was to develop a recipe to deposit SiGe undoped while keeping the low deposition temperature of the standard SiGe layers. The developed recipe deposits a SiGe layer with a thickness of around 220 nm composed by 20 nm of undoped PECVD SiGe plus 200 nm of undoped CVD SiGe.

The layer exhibits a high compressive stress (~ -150 MPa) after deposition, but becomes tensile after annealing. The layer can be then boron doped through implantation with the appropriate dose depending on the required electrical properties. The mechanical and electrical properties of this layer (layer 4 in Table 2.1) were already reported in Chap. 2.

4.3.2 Piezoresistor Patterning

The piezoresistors used in the fabricated pressure sensor are composed by two layers. The first layer is a 100 nm-thick SiC used as isolation between the SiGe piezoresistors and the SiGe membrane. The real thickness of this layer after deposition is slightly smaller, in the range of 60–70 nm. The second layer is the poly-SiGe sensing layer described above. To pattern the piezoresistors, these two layers need to be etched sequentially. A new etching recipe was developed specifically for this purpose. In the developed recipe, the patterning of the piezoresistors is done sequentially using two dry etching processes in two different tools: first the etch of the SiGe in a LAM Domino 2,300 system, followed by the etch of the SiC isolation layer in a LAM Alliance (A6) 9400 PTX Poly/Nitride Etch System.

Initially, an existing recipe for the dry etch of 200 nm of SiGe, using a hydrogen bromide (HBr) gas-based chemistry, was tried to etch the SiGe piezoresistive layer. After inspection it was found that the SiGe was not completely etched in the open areas (Fig. 4.11a). The recipe was then modified to target 50 % SiGe overetch. Figure 4.11b shows the results: the piezoresistor is perfectly defined, with vertical walls, while the SiGe is completely gone everywhere else. The initial recipe also included an *in situ* dry strip that was removed in the modified recipe since the strip has to be done after the second etch (SiC) is done. Moreover, this in situ strip proved to be not very efficient in removing the resist and the polymers formed during etch (Fig. 4.11a).

After the patterning of the SiGe piezoresistive layer is done, the SiC etch takes place. The SiC is patterned using a CHF_3/CF_4 plasma. Figure 4.12 shows

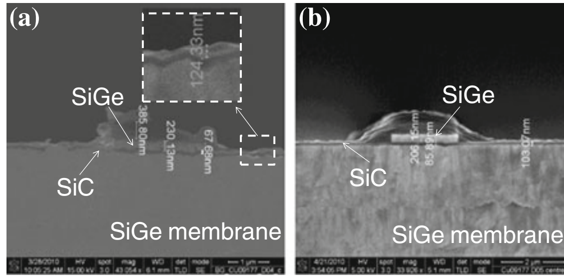

Fig. 4.11 Cross-section pictures illustrating the patterning of the SiGe piezoresistive layer. **a** SiGe etch using initial recipe (with an *in situ* strip included). A zoom in showing remaining SiGe in open areas is included. **b** Result after modified recipe targeting 50 % SiGe overetch and without *in situ* strip

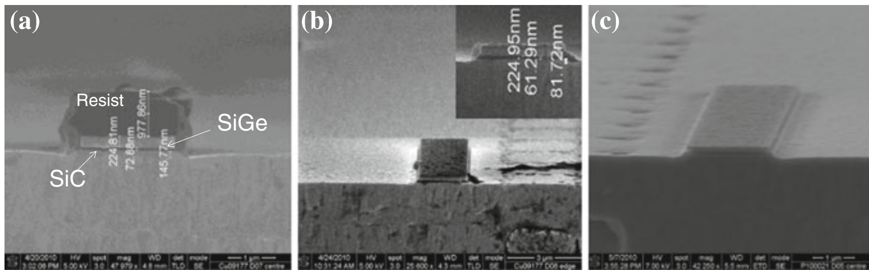

Fig. 4.12 Cross-section pictures after **a** 120" SiC etch (without strip), **b** 75" SiC etch (plus strip) and **c** 50" SiC etch (also plus strip). In **c** a side attack in the SiC/SiGe (piezoresistor) interface can be observed

cross-section pictures after SiC etch for 120”, 75” and 50”. In all cases the SiC is completely etched everywhere except below the SiGe piezoresistors. With the initial etch time of 150”, around 150 nm of the SiGe membrane is consumed (Fig. 4.12a). To limit this overetch, the etch time was reduced to 75”. In this way the thickness of the consumed SiGe is reduced below 100 nm, while still successfully etching the SiC isolation layer (Fig. 4.12b). However, the top surface of the SiGe piezoresistors gives an impression of being “burnt” (probably due to the excessive formation of polymers during the etch process). In an attempt to avoid this issue, the SiC etch time was further reduced to 50”, which resulted in an efficient and “clean” etch of the SiC layer with limited SiGe membrane consumption (Figs. 4.12c and 4.10). This is finally the etch time used in the pressure sensor flow for the patterning of the SiC isolation. The strip is performed in two consecutive steps: first a dry strip using an oxygen plasma and second a wet strip based on diluted buffer HF (DBHF).

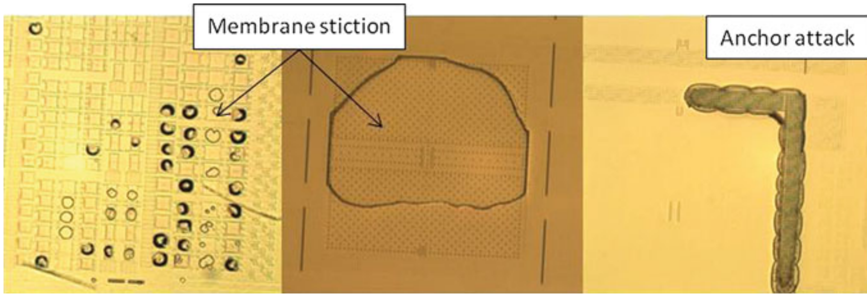

Fig. 4.13 Microscope pictures of membranes released in one step of 80 min. Issues with membrane stiction and anchor attack are observed on the wafer

4.3.3 Release

During the release process all the sacrificial oxide inside the cavities is removed. Vapor HF (vHF) is the chosen etchant, since it is very selective to SiGe and has a high etch rate for SiO_2. As already mentioned in Sect. 4.2, to avoid stiction during the release, AvHF (Anhydrous Vapor HF) together with ethanol vapor [15] is used to etch the sacrifical oxide. The release process is carried out on a Primaxx Clean Etch Technology (CET) tool. In a first attempt, the membranes were released in one step of 80 min. However, as can be seen in Fig. 4.13, this release recipe resulted in membrane stiction (probably due to excess of water, a byproduct of the etch process) and anchor attack.

To avoid these issues it was decided to divide the release process in eight steps instead of using only one step, as before. Breaking down the release time in steps has several advantages, the most important being:

- Reduction of the etch rate, making the recipe less aggressive and therefore limiting possible attacks of the anchor region, layer interfaces and the SiC CMOS protection layer.
- Reduced chance for stiction as water, which is a byproduct of the etching process, can be removed easily when the release time is broken in steps.

Two different recipes were investigated: 8 steps of 6 min and 8 steps of 8 min. To evaluate the release process, microscope inspection together with the so-called "tape test" was used. In this test, a standard adhesive tape is applied to an area of the wafer containing the released membranes. If the membranes are successfully released they will be pulled off by the tape when this one is removed. Figure 4.14 shows the results. From Fig. 4.14a we can conclude that 6 min per step is not enough to completely etch all the sacrificial oxide below the membrane. After the membranes are pulled off during the tape test, some oxide traces, in the form of columns, remain on the bottom of the cavities. By increasing the etch time to 8 min per step (Fig. 4.14b) all

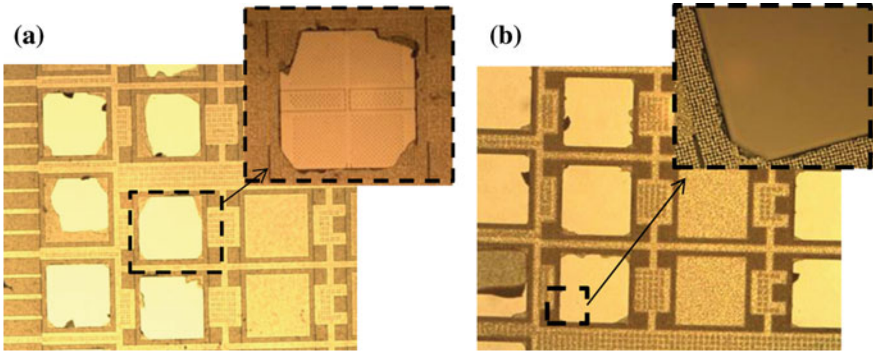

Fig. 4.14 Microscope pictures after tape test for membranes released in 8 steps of 6 min (**a**) and 8 steps of 8 min (**b**). Oxide traces below the pulled off membranes are visible in (**a**), while in (**b**) the cavity *bottom* appears clean.

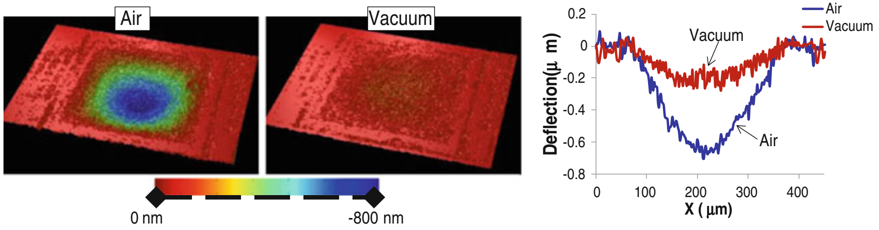

Fig. 4.15 Optical measurements of the deflection of a 300 x 300 μm^2 membrane sealed with oxide. Deflection is measured in air (1 bar) and vacuum (0.25 bar). The difference in deflection indicates that the membrane is sealed

the oxide is completely removed, without observing issues with membrane stiction or anchor attack anywhere on the wafer. In the pressure sensor fabrication process, the membranes are released in 8 steps of 8 min.

4.3.4 Sealing

The sealing process is one of the most important steps in the fabrication of a pressure sensor. For this reason a whole chapter of this thesis is dedicated to it. One of the most important requirements a sealing layer must fulfill is to provide a hermetic sealing of the cavity with a stable, preferably low, sealed-in pressure. In this work, several sealing layers were investigated (see Chap. 5). Finally SACVD (Sub-Atmospheric CVD) Si-oxide was the chosen sealing material.

It was found that 900 nm of SACVD Si-oxide was already sufficient to seal the membranes. However, for safety reasons, considering that some oxide could be consumed in following etching steps, a thickness of 1.2 µm was finally selected.

Figure 4.10b already showed a cross-section picture of a membrane sealed with a 1.2 μm-thick SACVD Si-oxide layer. This oxide sealing layer is deposited in two steps of 600 + 600 nm. To check if the membranes are successfully sealed, the membrane deflection under two different external pressures (air and vacuum) was optically measured (Fig. 4.15). The difference in deflection indicated that the membranes are sealed. The reasons behind the selection of SACVD oxide as sealing material, together with extra information about measurement set up, hermeticity tests and sealed-in pressure, can be found in Chap. 5.

4.3.5 Piezoresistor Contact

In the developed fabrication sequence, the sealing process takes place after the poly-SiGe piezoresistors have been deposited and patterned. This means that, once the 1.2 μm-thick SACVD Si-oxide sealing layer is deposited, the poly-SiGe piezoresistors are totally embedded in oxide (Fig. 4.16a). In order to provide electrical contact to the piezoresistors, $1 \times 1\,\mu m^2$ vias were etched in the sealing oxide on top of the piezoresistors. An oxide dry etch process stopping using in SiGe was used for this purpose. The oxide dry etch process used is based on a plasma of reactive gases such as Helium (He), Argon (Ar), Oxygen (O_2) and Octafluorocyclobutane (C_4F_8). After etch, these contacts are filled with a Ti (20 nm)/AlCu (880 nm)/TiN (60 nm) metal stack deposited at 350 °C. This is the same metal stack used to define the metal electrodes at the beginning of the flow (Fig. 4.4). Before the metal deposition, a 20 nm Ar pre-sputtering is performed to remove any unwanted oxide on the SiGe piezoresistor surface. However, as illustrated in Fig. 4.16b, the AlCu filling of the vias is not good, resulting in a poor electrical contact. This bad AlCu filling is mainly due to two factors: the straight vertical side walls, a consequence of the dry etch process used, and the relatively high aspect ratio of the contact holes (they are 1.2 μm high and only 1 μm wide).

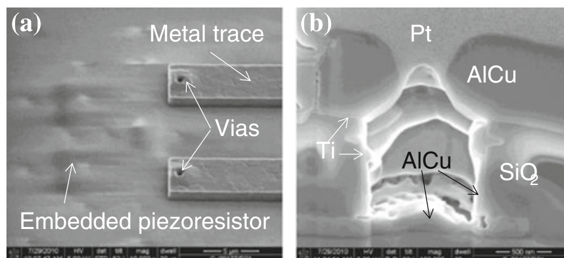

Fig. 4.16 **a** *Top* SEM picture of a piezoresistor embedded in sealing oxide. The metal traces and contact vias are also visible. **b** FIB picture of the bad AlCu via filling. It is thanks to the thin (20 nm) Ti layer, which deposits conformally, that there is electrical connection at all. Pt is deposited during the FIB process to increase the contrast and get a sharper picture

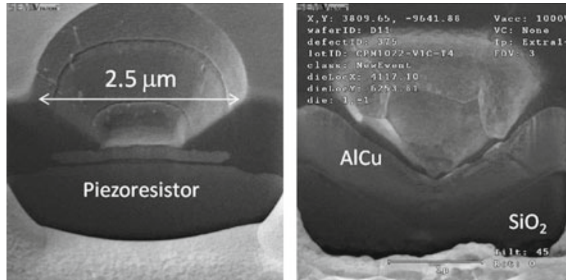

Fig. 4.17 Results of the HDP deposition experiments: FIB pictures of a contact via before (*left*) and after (*right*) the metal deposition. The standard Ti/AlCu/TiN (20/880/60 nm) metal stack, deposited at 350 °C is used to fill the vias. After the HDP deposition plus HF wet etch, the contact walls were nicely inclined. In this condition, the AlCu can easily flow in, completely filling the contact

In order to improve the metal filling of the contacts, an experiment to try to increase the angle of the contact sidewalls was carried out: AlCu is expected to deposit better on inclined walls as compared to 90° vertical walls. In order to achieve inclined sidewalls, 50 nm of HDP Si-oxide was deposited on top of the opened vias. For the HDP Si-oxide deposition, a process with more sputtering than deposition was used. The sputtering performed during this deposition serves to clip the corners of the contact holes. After the HDP deposition, an extra sputtering of 80 s is performed. To remove the HDP oxide deposited on the SiGe inside the contacts, an oxide wet etch with HF for 5 min was performed. As can be seen from Fig. 4.17, this experiment resulted in nicely filled contacts with ∼135° inclined walls. However, a microscope inspection revealed that all the membranes were either broken or completely gone after the HDP deposition (Fig. 4.18). One possible explanation for this could be the difference in stress of the layers. HDP Si-oxide typically exhibits high compressive stress (∼−200 MPa), in contrast with the marginally tensile stress expected from the SACVD Si-oxide sealed poly-SiGe membranes (see Table 5.3). Moreover, the HDP deposition occurs at a high temperature (400 °C), which can result in high induced

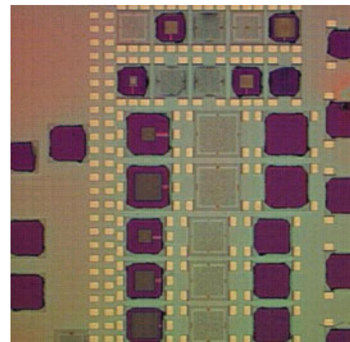

Fig. 4.18 Delamination after HDP deposition. All the pressure sensor membranes are gone or broken. The only remaining membranes visible on the picture are those of the "dummy" (non-released) sensors

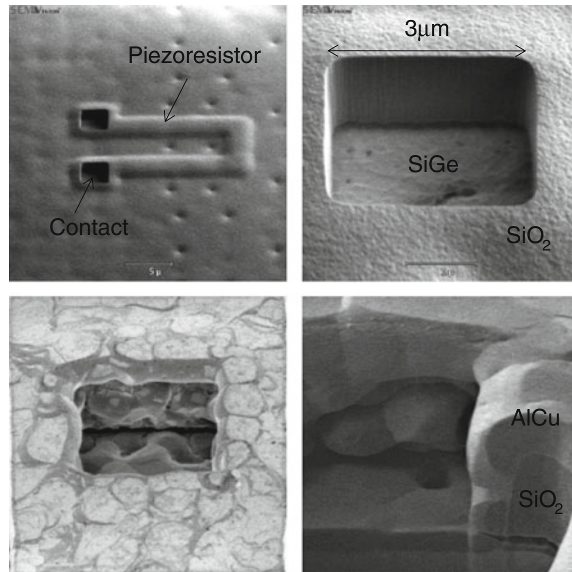

Fig. 4.19 Top: pictures of the new $3\times3\,\mu m^2$ contacts after oxide etch. *Bottom*: *Top* (*left*) and Cross-section (*right*) pictures of a $3\times3\,\mu m^2$ contact via filled with 500 nm AlCu. Although not yet perfect, the filling, and thus the electrical contact, is much better than with the original $1\times1\,\mu m^2$ vias

stresses due to the different thermal expansion coefficients of the layers that form the membranes.

After the failure of the above described experiment, it was decided to redesign two masks of the pressure sensor layout (specifically the mask to pattern the piezoresistors and the mask to open the vias in the oxide) in order to have larger contacts. The new contacts are $3\times3\,\mu m^2$, resulting in an improved AlCu filling. Figure 4.19 shows top and cross-section pictures of the new contacts, before and after AlCu filling. To avoid stress-related delamination issues, and since the filling was already good enough, a thinner AlCu (500 nm instead of 880 nm) was used to contact the piezoresistors. The final metal stack is thus 20 nm Ti / 500 nm AlCu, with no TiN. The only purpose of this top TiN layer is to facilitate lithography, but here dimensions are large enough such that lithography is not an issue.

4.4 Discussion on the Poly-SiGe Pressure Sensor Process

In this chapter, a process flow suitable for the fabrication of surface micromachined poly-SiGe piezoresistive and/or capacitive pressure sensors has been presented. Throughout the fabrication flow, the processing temperature is always kept below 460 °C to allow for post-processing on top of CMOS. Figure 4.20 shows top microscope pictures of two of the fabricated devices: a piezoresistive-only and a combined (piezoresistive and capacitive) pressure sensors. The bondpads, the four piezoresistors (as the sealing oxide is transparent) and the metal interconnects can all

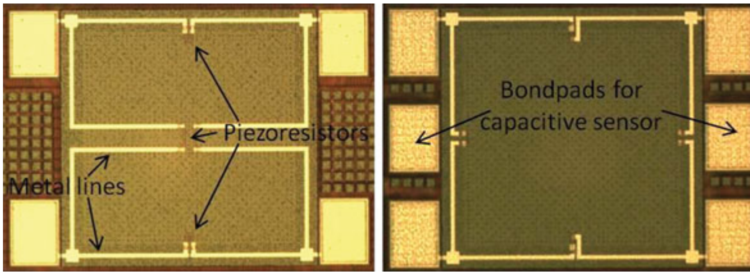

Fig. 4.20 *Top* microscope pictures of a piezoresistive-only (*left*) and a combined piezoresistive-capacitive (*right*) pressure sensor. The bondpads, piezoresistors and metal lines are visible. For the combined pressure sensor six bondpads are needed: four (in the corners) for piezoresistive measurements, and two (in the centre) for capacitive measurements

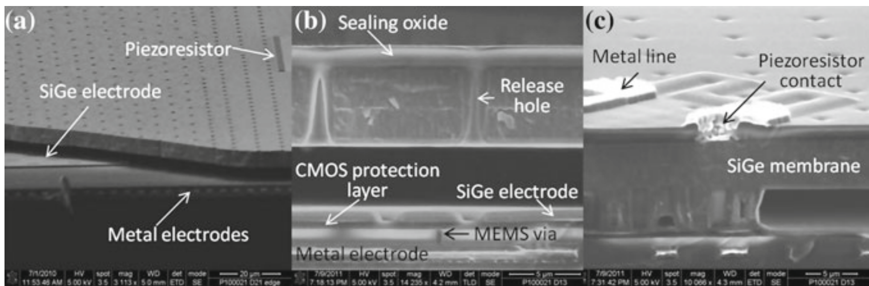

Fig. 4.21 SEM pictures of some of the fabricated devices. **a** An unsealed combined (piezoresistive and capacitive) pressure sensor. The SiGe electrode below the membrane can be observed. **b** Cross-section picture of a finished device. The bottom components (metal and SiGe electrodes, the SiC CMOS protection layer and a MEMS via) can be observed. Two sealed release holes are also visible. In **c**, a piezoresistor covered in sealing oxide is shown, together with the two piezoresistor contacts and the AlCu interconnects

be observed. Three SEM pictures of fabricated devices are depicted in Fig. 4.21. The main components of the developed process flow are visible in these pictures; first, the bottom metal electrode (embedded in oxide), the SiC protection layer (to protect the metal electrode during the aggressive vHF MEMS release), the SiGe electrode and the tungsten-filled MEMS vias, connecting both (metal and SiGe) electrodes. Also, the poly-SiGe membrane, release holes and piezoresistorsv are clearly visible. And finally, the SACVD sealing oxide, the piezoresistor contacts and the AlCu interconnects can be seen. In Fig. 4.21b and c, the deposition of sealing oxide inside the cavity (SACVD oxide deposits conformally) can also be appreciated.

The whole process sequence requires ten lithographic masks and more than 100 operations (including depositions, litho exposures, etching and strips, annealing steps, etc). As mentioned above, in order to make the process flow CMOS-compatible, the maximum temperature allowed in these operations was 460 °C. Table 4.2 lists the operations that required the highest ($\geq$ 400 °C) temperatures.

Table 4.2 List of the operations in the pressure sensor process flow performed at temperatures ≥ 400 °C. The total time per operation is also included. For operations that happen more than once in the flow, the total time is the sum of the times for each single operation

Operation	Where in the process flow?	Temperature (°C)	Total time (min)
HDP Si-oxide deposition	Sacrificial oxide, electrode embedding,...	400	∼15
SACVD Si-oxide deposition	Sealing	420	7.3
SiGe deposition	Electrode, structural layer, piezoresistors	450	∼60
Annealing	After piezoresistor implantation, before SiGe structural layer deposition, ...	455	450[a]

[a] For a total of 5 annealing steps in the flow, each with a duration of 1.5 h (the required 30' + 1 h for warm-up and cool-down periods). A 30 min annealing step (+ 1 h for warm-up and cool-down periods) after piezoresistor implantation is considered

The processing time for these operations can also be found in this table. As reported in [1, 2], not only the temperature but also the time that the wafers must endure that high temperature play an important role in the degradation of the CMOS performance.

As can be seen from Table 4.2, the operations requiring the highest temperatures are the annealing steps and the poly-SiGe depositions. The annealing steps account for most of the highest temperature processing time. All the annealing steps in the flow are performed in a hydrogen-rich atmosphere at a temperature of 455 °C with a typical duration of 30 min. However, each annealing step is preceded by a warm-up and stabilization period (of ∼30 min), and followed by a 30 min cool-down period. Therefore, for each annealing step of 30 min, the total time the wafer is kept at 455 °C is approximately 1.5 h. These annealing steps fulfill different purposes in the process flow. For example, there is an annealing step after piezoresistor implantation to activate the boron atoms (as seen in Chap. 2, the length of this annealing step will affect the piezoresistor performance). Two annealing steps are performed right before and after the SiC protection layer deposition to promote densification. Another annealing step is also added right before the SiGe structural layer, to outgass the underlying layers, avoiding later delamination issues. In total, during the processing of the MEMS pressure sensors on top of the read-out circuit, the CMOS will withstand a maximum temperature of approximately 455 °C for ∼8.5 h. The resulting degradation in the CMOS performance is evaluated in Chap. 7.

In this chapter, also the most important process developments required for the fabrication of the pressure sensors in this work are explained. These include: the development of a poly-SiGe piezoresistive layer processed at CMOS-compatible temperatures (see Chap. 2 for more information), the piezoresistor patterning, the sealing process (with more information in Chap. 5) and the improvement of the AlCu filling of the piezoresistor contacts. Although not specifically mentioned, one

of the main issues encountered during the fabrication process was delamination. This is thought to be due to the internal stresses of the layers; moreover, the difference in thermal expansion coefficients might also lead to high temperature-induced stresses. In some cases, these stresses resulted in broken membranes, mostly the biggest ones (300×300 and $250\times250\,\mu m^2$). In general, all operations performed after the membranes are sealed are more sensitive to result in broken membranes.

In the frame of this work, piezoresistive pressure sensors using a slightly different, and shorter (using only five lithopgraphic masks), process flow were also fabricated. These pressure sensors were fabricated starting at anchor level, and therefore do not include any of the bottom layers, such as metal and SiGe electrodes, SiC protection layer or MEMS vias. The piezoresistor annealing time was 2 h, instead of the 30' annealing used in the process described in this chapter. More information about the fabrication and performance of these sensors can be found in appendix B.

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