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Pilar González Ruiz
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Ann Witvrouw

# Poly-SiGe for MEMS-above-CMOS Sensors

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# Poly-SiGe for MEMS-above-CMOS Sensors

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Leuven, September 2012 Pilar González Ruiz

# Contents

**1 Introduction** . . . . . 1
1.1 Motivation and Goal of This Work . . . . . 1
1.2 MEMS: Definition, Technologies and Applications . . . . . 2
1.3 CMOS-MEMS Integration: Why, How and What? . . . . . 5
1.4 Polycrystalline SiGe for MEMS-above-CMOS Applications . . . . 8
1.4.1 SiGe MEMS Demonstrators . . . . . 8
1.4.2 Poly-SiGe Deposition Technology. . . . . 10
1.4.3 Selected Poly-SiGe Structural Layer . . . . . 11
1.5 A Poly-SiGe Based MEMS Pressure Sensor . . . . . 13
1.5.1 Applications of MEMS Pressure Sensors . . . . . 13
1.5.2 Technologies for MEMS Pressure Sensors . . . . . 14
1.5.3 Why a Poly-SiGe Based MEMS Pressure Sensor? . . . . . 15
1.6 Outline of the Book. . . . . 17
References . . . . . 19

**2 Poly-SiGe as Piezoresistive Material** . . . . . 25
2.1 Introduction to Piezoresistivity . . . . . 25
2.1.1 Single Crystalline Materials . . . . . 26
2.1.2 Polycrystalline Materials . . . . . 29
2.1.3 Definition of the Gauge Factor . . . . . 30
2.2 Sample Preparation . . . . . 30
2.2.1 Layout and Fabrication Process . . . . . 30
2.2.2 Poly-SiGe Layers Studied . . . . . 32
2.3 Measurement Setup . . . . . 34
2.3.1 The Four Point Bending Method. . . . . 36
2.3.2 Calculation of the Piezoresistive Coefficients . . . . . 37
2.4 Results and Discussion. . . . . 38
2.4.1 Standard Poly-SiGe Layer and Comparison to Poly-Si. . . 38
2.4.2 Optimization of Boron Doped Poly-SiGe Layers for Piezoresistive Sensing Applications . . . . . 41
2.4.3 Piezoresistivity and Electrical Properties of Poly-SiGe Deposited at CMOS-Compatible Temperatures . . . . . 45

2.5 Summary and Conclusions . . . . . 46
References . . . . . 47

**3 Design of a Poly-SiGe Piezoresistive Pressure Sensor** . . . . . 51
3.1 A Piezoresistive Pressure Sensor: Definition and Important Performance Parameters . . . . . 51
3.1.1 Definition. . . . . 51
3.1.2 Important Parameters. . . . . 53
3.2 Design . . . . . 57
3.2.1 Membrane Area and Thickness. . . . . 59
3.2.2 Piezoresistor Placement . . . . . 62
3.2.3 Piezoresistor Dimensions . . . . . 65
3.2.4 Piezoresistor Shape . . . . . 67
3.2.5 Membrane Shape . . . . . 69
3.2.6 Effect of Supports. . . . . 71
3.3 Summary and Conclusions of the Sensor Design. . . . . 71
References . . . . . 73

**4 The Pressure Sensor Fabrication Process** . . . . . 75
4.1 The Pressure Sensor Fabrication Process: A Generic Technology . . . . . 75
4.2 Pressure Sensor Schematic Process Flow . . . . . 80
4.3 Process Developments and Challenges . . . . . 87
4.3.1 Piezoresistive Layer . . . . . 89
4.3.2 Piezoresistor Patterning . . . . . 89
4.3.3 Release . . . . . 91
4.3.4 Sealing . . . . . 92
4.3.5 Piezoresistor Contact. . . . . 93
4.4 Discussion on the Poly-SiGe Pressure Sensor Process . . . . . 95
References . . . . . 98

**5 Sealing of Surface Micromachined Poly-SiGe Cavities**. . . . . 101
5.1 Introduction . . . . . 101
5.2 Fabrication Process . . . . . 103
5.3 Direct Sealing. . . . . 106
5.3.1 Sealing with Si-Oxide . . . . . 106
5.3.2 Sealing with AlCu. . . . . 109
5.4 Intermediate Porous Cover . . . . . 109
5.5 Measurement Setup . . . . . 113
5.6 Analytical Model. . . . . 114

5.7 Results and Discussion . . . . . 116
5.7.1 Membrane Behavior Under 0-Pressure Difference . . . . . 119
5.7.2 Cavity Pressure . . . . . 121
5.7.3 Long-Term Hermeticity . . . . . 123
5.8 Summary and Conclusion . . . . . 124
References . . . . . 125

**6 Characterization of Poly-SiGe Pressure Sensors** . . . . . 127
6.1 Measurement Setup . . . . . 127
6.2 Measurement Results: Pressure Response . . . . . 129
6.2.1 Sensitivity . . . . . 131
6.2.2 Comparison to Simulations . . . . . 134
6.2.3 Offset . . . . . 138
6.2.4 Nonlinearity . . . . . 139
6.2.5 Thermal Behaviour . . . . . 140
6.3 Summary and Conclusions . . . . . 141
6.4 Capacitive Pressure Sensors . . . . . 144
References . . . . . 147

**7 CMOS Integrated Poly-SiGe Piezoresistive Pressure Sensor** . . . . . 149
7.1 The Sensor Readout Circuit: An Instrumentation Amplifier . . . . 149
7.1.1 Design . . . . . 151
7.1.2 Layout . . . . . 155
7.1.3 Fabrication . . . . . 159
7.1.4 Measurements . . . . . 160
7.2 Fabrication of a CMOS Integrated Pressure Sensor . . . . . 161
7.3 Effect of the MEMS Processing on CMOS . . . . . 167
7.4 Evaluation of the CMOS-Integrated Pressure Sensor . . . . . 169
7.5 Conclusions . . . . . 172
References . . . . . 173

**8 Conclusions and Future Work** . . . . . 175
8.1 Conclusions and Contribution of the Dissertation . . . . . 175
8.2 Future Research Directions and Recommendations . . . . . 179

**Appendix A** . . . . . 181

**Appendix B** . . . . . 189

**Appendix C** . . . . . 193

**Appendix D** . . . . . 197

# Symbols and Abbreviations

## Symbols

$A$ — Cross-sectional area ($m^2$)
$C_c$ — Compensation capacitor (pF)
E — Electric Field Vector (V)
$E$ — Young’s modulus (GPa)
$\varepsilon$ — Strain
F — Force (N)
G — Gauge factor ($\Delta R/R \cdot 1/\varepsilon$)
$\delta$ — Grain boundary thickness (nm)
$i$ — Current vector (A)
$L$ — Resistor or membrane length (mm or μm)
$\mu$ — Mobility ($cm^2/Vs$)
$m_{1\parallel}$ — Longitudinal effective mass of heavy holes (kg)
$m_1\perp$ — Transversal effective mass of heavy holes (kg)
$m_{2\parallel}$ — Longitudinal effective mass of light holes (kg)
$m_2\perp$ — Transversal effective mass of light holes (kg)
$v$ — Poisson’s ratio
$\pi_1$ — Longitudinal piezoresistive coefficient ($Pa^{-1}$)
$\pi_t$ — Transverse piezoresistive coefficient ($Pa^{-1}$)
$\pi_{1t}$ — Shear piezoresistive coefficient ($Pa^{-1}$)
P — Pressure (Pa)
$p_{act}$ — Active carrier concentration ($cm^{-3}$)
$p_{che}$ — Chemical carrier concentration ($cm^{-3}$)
$S_x$ — Activation signal for switch x (V)
T — Temperature (°C)
$t_x$ — Thickness of layer x (m)
$\rho$ — Electrical resistivity (mΩ cm)
$\Delta\rho$ — Electrical resistivity change (mΩ cm)
$\rho_g$ — Electrical resistivity of the grain (mΩ cm)
$\rho_b$ — Electrical resistivity of the grain boundary (mΩ cm)
R — Electrical resistance (Ω)

| | |
|---|---|
| $\sigma$ | Stress (MPa) |
| $\sigma_{xx}$ | Normal stress (MPa) |
| $\sigma_{cr1}$ | Critical stress (MPa) |
| $\sigma_1$ | Longitudinal stress (MPa) |
| $\sigma_t$ | Transverse stress (MPa) |
| $\sigma_b$ | Bending stress (MPa) |
| $\sigma_c$ | In-plane stress (MPa) |
| $\sigma_0$ | Residual stress (MPa) |
| $\tau$ | Shear stress (MPa) |
| $V_{DD}$ | IC power supply (V) |
| $w_0$ | Centre deflection (μm) |
| w | Sample width (mm) |
| W | Membrane width (μm) |
| W/L | Transistor gate width/gate length |

## Abbreviations

| | |
|---|---|
| 3D | Three-dimensional |
| Al | Aluminum |
| AlCu | Aluminum copper |
| AMAT | Applied materials |
| AvHF | Anhydrous vapor HF |
| Ar | Argon |
| B | Boron |
| $B_2H_6$ | Di-borane |
| $BF_2$ | Boron difluoride |
| BiCMOS | Bipolar CMOS |
| CET | Clean etch technology |
| $CF_4$ | Tetrafluoromethane or carbon tetrafluoride |
| $C_4F_8$ | Octafluorocyclobutane |
| $CHF_3$ | Trifluoromethane |
| CMOS | Complementary metal-oxide semiconductor |
| CMRR | Common mode rejection ratio |
| CSM | Continuous stiffness measurement |
| CTE | Coefficient of thermal expansion ($\mu m(m°C)^{-1}$) |
| Cu | Copper |
| CVD | Chemical vapor deposition |
| CMP | Chemical mechanical polishing |
| DBHF | Diluted buffer HF |
| DRIE | Deep reactive ion etching |
| ESD | Electro static discharge |
| FEM | Finite element method |
| FEA | Finite element analysis |
| FIB | Focus ion beam |

| | |
|---|---|
| FS | Full-scale |
| FSS | Full-scale span (mV) |
| Ge | Germanium |
| $GeH_4$ | Germane |
| $H_2$ | Hydrogen |
| $H_3PO_4$ | Phosphoric acid |
| HBr | Hydrogen bromide |
| He | Helium |
| HDD | High dose implantations |
| HF | Hydrogen fluoride |
| $HNO_3$ | Nitric acid |
| HP | Hewlett Packard |
| HVAC | Heating, ventilation, and air-conditioning |
| IC | Integrated circuits |
| In-amp | Instrumentation amplifier |
| LCR | Inductance, capacitance and resistance |
| LPCVD | Low pressure chemical vapor deposition |
| μc-SiGe | Microcrystalline silicon germanium |
| MEM | Micro electro mechanical |
| MEMS | Micro electro mechanical systems |
| MOS | Metal-oxide semiconductor |
| $N_2$ | Nitrogen |
| $N_2O$ | Nitrous oxide |
| $NH_3$ | Ammonia |
| Ni | Nickel |
| NiSi | Nickel silicide |
| NL | Nonlinearity (%FSS) |
| NMOS | Negative channel MOS |
| $O_2$ | Oxygen |
| $O_3$ | Ozone |
| Op-amp | Operational amplifier |
| P | Phosphorus |
| PECVD | Plasma-enhanced chemical vapor deposition |
| PM | Phase margin |
| PMOS | Positive channel MOS |
| Poly-Si | Polycrystalline silicon |
| Poly-SiGe | Polycrystalline silicon germanium |
| PSG | Phosphosilicate glass |
| RBS | Rutherford backscattering |
| RF | Radio frequency |
| S | Pressure sensitivity (mV/V/bar) |
| SACVD | Sub-atmospheric chemical vapor deposition |
| SEM | Scanning electron microscopy |
| Si | Silicon |
| SiC | Silicon carbide |

| | |
|---|---|
| SiGe | Silicon germanium |
| $SiH_4$ | Silane |
| SIMS | Secondary ion mass spectrometry |
| SNR | Signal to noise ratio |
| $SiO_2$ | Silicon dioxide |
| Ta | Tantalum |
| TaN | Tantalum nitride |
| TCR | Temperature coefficient of resistance ($°C^{-1}$) |
| TCS | Temperature coefficient of sensitivity (ppm/°C) |
| TCO | Temperature coefficient of offset voltage (mV/°C) |
| TEM | Transmission electron microscopy |
| TEOS | Tetraethyl orthosilicate ($Si(OC_2H_5)_4$) |
| Ti | Titanium |
| TiN | Titanium nitride |
| TNO | Temperature nonlinearity of offset voltage |
| TNS | Temperature nonlinearity of sensitivity (ppm/°C) |
| TPMS | Tire pressure monitoring system |
| TTM | Through transmissive media |
| UTS | Ultimate tensile strength (GPa) |
| vHF | Vapor-HF |
| VM | Von Mises stress (MPa) |
| Voff | Offset voltage (mV) |
| WLI | White light interferometry |
| W | Tungsten |
| XRD | X-ray diffraction |

# Abstract

Microelectromechanical systems (MEMS) were first introduced in the 1960s in the form of pressure sensors. The technology quickly evolved from innovative concepts to practical demonstrations and early products. Nowadays MEMS have become commonplace products. The next natural step in the micro-technology evolution is the integration of MEMS and the controlling and readout electronics on the same substrate. This CMOS-MEMS monolithic integration can lead to more compact MEMS with improved performance. The post-processing route (fabricating MEMS directly on top of CMOS) is the most promising approach for CMOS-MEMS monolithic integration as it leads to smaller die areas and enables integrating the MEMS without introducing any changes in standard foundry CMOS processes.

Polycrystalline silicon germanium (poly-SiGe) has emerged as a promising MEMS structural material since it provides the desired mechanical properties at lower temperatures compared to poly-Si, allowing post-processing on top of CMOS. In the past, imec already proved the potential of poly-SiGe for MEMS above-aluminum-backend CMOS integration by presenting, for example, an integrated poly-SiGe micromirror array and an integrated gyroscope. However, aggressive interconnect scaling has led to the replacement of the traditional aluminum metallization by copper (Cu) metallization, due to its lower resistivity and improved reliability.

In this dissertation, an integrated poly-SiGe-based piezoresistive pressure sensor, which is directly fabricated above 0.13 μm Cu-backend CMOS technology, is presented. This represents not only the first integrated poly-SiGe pressure sensor directly fabricated above its readout circuit, but also the first time that a poly-SiGe MEMS device is processed on top of Cu-backend CMOS. The described integrated sensor (fully fabricated in imec) includes a surface-micromachined piezoresistive pressure sensor, with a poly-SiGe membrane and four poly-SiGe piezoresistors, and an instrumentation amplifier fabricated using imec's 0.13 μm CMOS technology, with two Cu metal layers and Si-oxide dielectric layers.

All the steps that were completed in order to realize the integrated pressure sensor are described in detailed in this thesis. First, a detailed investigation on the influence of deposition conditions, germanium content, and doping concentration on the electrical and piezoresistive properties of boron-doped poly-SiGe was

conducted. Once the sensing layer was developed, finite element simulations were used to design the pressure sensors. A CMOS-compatible process flow was then developed, with special attention to the sealing method, and piezoresistive pressure sensors with different areas and piezoresistor designs were successfully fabricated. Despite the low processing temperature (≤455 °C), the sensors featured good performance in terms of sensitivity and temperature drift. Finally, the readout circuit for the sensors was designed and the CMOS compatibility of the developed MEMS technology was demonstrated by fabricating the pressure sensors directly on top of the CMOS readout circuit. The CMOS circuit showed no significant deterioration after the MEMS processing, although a resistance increase for the Cu-filled metal-to-metal and the tungsten-filled CMOS-MEMS vias was observed.

The results obtained in this work show the compatibility of poly-SiGe with post-processing above Cu-based CMOS, broadening the applications of poly-SiGe to the integration of MEMS with the advanced CMOS technology nodes.

# Chapter 1
# Introduction

In this introductory chapter, the motivation and main topic of this work are introduced. After a general introduction to microelectromechanical systems (MEMS), the different existing approaches for the integration of the MEMS with the driving and controlling electronics are presented. The benefits of using silicon germanium (SiGe) as MEMS structural material are introduced next, together with an overview of the SiGe deposition technology and existing SiGe MEMS demonstrators. The last part of the chapter deals with MEMS pressure sensors, their applications and fabrication technologies. A poly-SiGe based MEMS pressure sensor is then presented as the chosen demonstrator in this work, together with the selected poly-SiGe structural layer. The chapter concludes with a description of the outline of this book.

## 1.1 Motivation and Goal of This Work

While microelectromechanical systems have matured significantly over the last decade to become commonplace products, there is an emerging interest for a fully CMOS compatible generic technology that would allow the MEMS to be fabricated on the same CMOS substrate as the controlling and readout electronics. This CMOS-MEMS monolithic integration can improve performance as well as reduce assembly and packaging cost [1]. The post-processing route (fabricating MEMS directly on top of CMOS) is the most promising approach for CMOS-MEMS monolithic integration as it leads to smaller die areas and enables integrating the MEMS without introducing any changes in standard foundry CMOS processes. Polycrystalline silicon germanium (poly-SiGe) has emerged as a promising MEMS structural material since it provides the desired mechanical properties at lower temperatures compared to poly-Si, allowing post-processing on top of CMOS.

In the past, imec already proved the potential of poly-SiGe for MEMS-above-CMOS integration by presenting, for example, an integrated poly-SiGe micromirror array [2] and an integrated gyroscope [3], both of them fabricated on top of

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aluminum-based CMOS (from an external foundry). However, the aggressive interconnect scaling, essential to the continuation of Moore's law, has led to the replacement of the traditional aluminum metallization by copper metallization, due to its lower resistivity and improved reliability [4]. The scope of this work is to study if the poly-SiGe based MEMS technology is also compatible with post-processing above Cu-based CMOS, broadening in this way the applications of poly-SiGe to the integration of MEMS with the advanced CMOS technology nodes.

This work aims at developing a CMOS-compatible process flow for the fabrication of piezoresistive pressure sensors. This represents not only the first time that poly-SiGe is used both as structural layer and sensing layer for MEMS pressure sensor applications, but also the first time that the piezoresistivity of poly-SiGe is studied in detail. During the proposed fabrication process, the maximum temperature is kept below 460° C to allow for the integration of the pressure sensors on top of their readout circuitry, allowing for smaller and cheaper systems with improved performance. The final goal is the realization of an integrated poly-SiGe-based piezoresistive pressure sensor directly fabricated above 0.13 μm Cu-backend CMOS technology. This would represent not only the first integrated poly-SiGe pressure sensor directly fabricated above its readout circuit, but also the first time that a poly-SiGe MEMS device is processed on top of Cu-backend CMOS.

## 1.2 MEMS: Definition, Technologies and Applications

MEMS stands for Micro Electro-Mechanical Systems and refers to micrometer-scale devices composed by micromechanical parts (sensors and/or actuators) interfacing electrical ones, where sensing and actuation functions interact with the surrounding environment [5]. MEMS can include two or more of the following subsystems: sensors, actuators, a power supply, and a driving, controlling and signal processing circuitry (see Fig. 1.1). The microelectronic integrated circuits can be thought of as the "brains" of the microsystem, and the mechanical components (sensors and actuators) can be seen as the "eyes" and "arms", allowing the microsystem to sense and control the environment. Sensors gather information from the environment through measuring mechanical, thermal, biological, chemical, optical, and magnetic phenomena. The electronics then process the information derived from the sensors and through some decision making capability direct the actuators to respond by moving, positioning, regulating, pumping, and filtering, thereby controlling the environment for some desired outcome or purpose [6]. The vast majority of today's MEMS products are better described as sub-systems, as they include only one type of functional element (sensor or actuator).

MEMS range in size from the sub-micrometer level to the millimetre level and are manufactured via "micromachining" processes. Micromachining extends the fabrication techniques developed for the integrated circuit (IC) industry to add mechanical elements such as beams, gears, diaphragms, and springs to devices [7]. Although many micromachining processing steps are derived from basic IC manufacturing,

MEMS fabrication is still different from IC fabrication in some aspects, like, for example, a larger feature size, the lack of standard processes or the use of unconventional materials [8]. Besides the conventional materials used in IC fabrication, MEMS fabrication processes also use other materials (quartz, ceramics, polymide, etc). Also, contrary to standard IC, MEMS include movable structures. For this reason, some specific problems, like stiction, must be considered. The mechanical properties of the layers (i.e. Young's modulus, poisson's ratio, residual stress, etc) are more important in MEMS than in IC fabrication since they determine the behaviour of the devices. Certain aspects of the fabrication process (like deposition temperatures or annealing processes) could greatly affect these properties. For all of these reasons, some IC-processes had to be adapted to be applied in MEMS fabrication and new processes, like Deep Reactive Ion Etching (DRIE) [9], appeared.

All of the micromachining processes can be divided into two broad classes: bulk micromachining and surface micromachining [7, 9]. The oldest succesfully commercial micromachining technology is bulk micromachining [7], which involves the selective removal of the substrate material in order to realize miniaturized mechanical components. In surface micromachining, the MEMS are defined by deposition/etching sequences from multilayer stacked and patterned thin films. Commonly, the structural or device layer is deposited on top of some temporary or sacrificial thin-film material; the structural layer is then patterned and the temporary layer is etched away to release the mechanical structure, thereby allowing the structural layer to move. Surface micromachining offers better dimensional control, larger variety of structure, sacrificial and etchant combinations and is more IC-compatible. It can also have some drawbacks, like possible stiction problems during the release process or reproducibility issues of the thin-films mechanical properties.

MEMS technology was first introduced in the late 60s in the form of pressure sensors. The technology quickly evolved from innovative concepts on to practical demonstrations on to early products. Nowadays, MEMS is replacing most of the

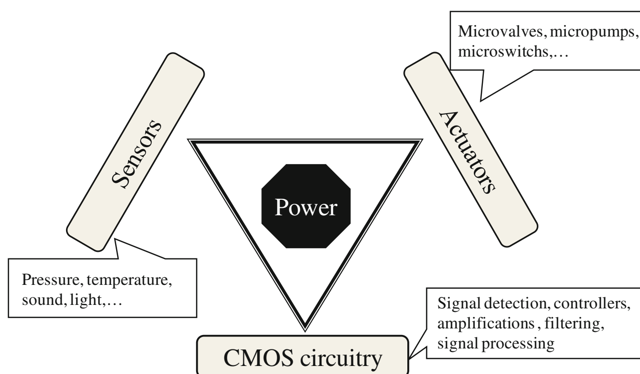


**Fig. 1.1** Components of a micro-electro-mechanical system

conventional systems in a wide variety of everyday applications thanks to its many benefits [9, 11]:

- Smaller dimensions. Micromechanical devices and systems are inherently smaller, lighter and faster than their macroscopic counterparts, and often also more precise. The reduction of the physical dimensions also translates into a significant reduction in fabrication cost and power consumption. As an example to clarify this point, if we consider a conventional mechanical gyroscope, its power consumption is, on the average, 35 W, and it weighs 1.5 kg [12]. Miniaturizing this device, using MEMS technology, reduces the mass down to 10 g and power consumption to a few mW.
- Batch fabrication. Because MEMS devices are manufactured using batch fabrication techniques similar to those used for ICs, unprecedented levels of functionality, reliability and sophistication can be placed on a small silicon (Si) chip. Moreover, the possibility of batch fabrication further reduces the manufacturing cost and time and enables mass-volume production.
- Integration with IC. Since the mechanical components are fabricated with IC-compatible microfabrication techniques, they can be integrated with the electronics creating complete smart systems on a single chip.

The versatility of the MEMS devices that have been developed so far is large and many of those developments found already successful commercial application in various fields like the automotive industry, for biomedical and military applications, for process control in industry, consumer electronics and communications. The automotive industry uses a wide range of MEMS devices like pressure sensors, accelerometers and gyroscopes for the active safety of car passengers [13, 14], active suspension systems and navigation [15]. Similar devices are now used in the multimedia market with applications in, for example, the WII remote gaming control and in smartphones [16]. RF MEMS have come to the market more recently than other types of MEMS, but the RF MEMS market is now growing with devices such as switches, micro-filters, resonators or varactors, find application in microwave systems, antennas and wireless communication [17, 18]. Other MEMS devices include microphones for cell phones or noise cancelation in modern cars, and acoustical wave filters that facilitate wireless internet access, among others.

All of these MEMS devices need an integrated circuit employed for actuator driving and sensor signal conditioning and processing. The decision to integrate CMOS and MEMS devices is mainly driven by performance, yield, reliability and cost. There are different ways to combine the MEMS devices and the CMOS electronics. The following sections give an overview of the existing techniques for CMOS-MEMS integration and present poly-SiGe as, in our view, the best candidate for MEMS-above-CMOS integration, the integration approach adopted in this work.

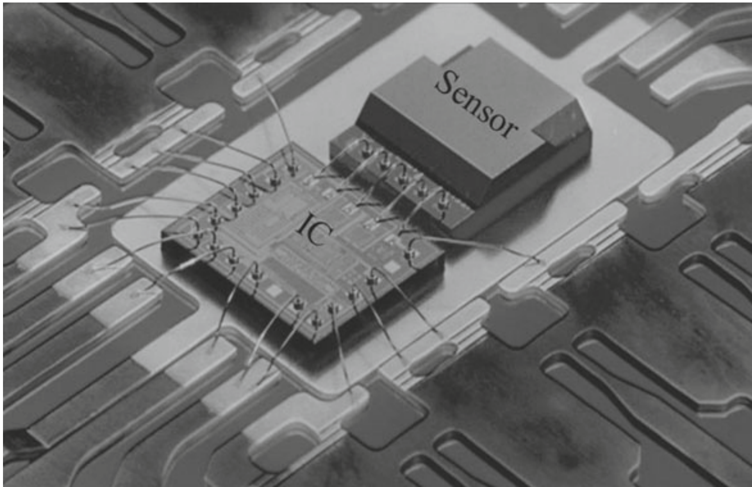


**Fig. 1.2** Freescale 2-axis MEMS accelerometer to ASIC module assembly [21]

## 1.3 CMOS-MEMS Integration: Why, How and What?

Nowadays the integration of MEMS with the CMOS readout electronic circuit is generally achieved by the so-called hybrid integration [19]. In this approach the MEMS and the CMOS chips are processed separately and interconnected by means of wirebonds. Figure 1.2 shows a hybrid solution from Freescale, the 2-axis accelerometer MMA62xxQ [20]. The MEMS chip on the right is connected to the IC on the left using tiny wires and both are mounted in a metal frame before encapsulation in the same package. Such an approach is modular and has a much shorter development time as compared to the monolithic approach discussed next. It also allows for the independent optimization of the IC and MEMS processes (for example choice of processing temperatures or materials). However, compactness and reliability suffers from the additional elements and the packaging becomes slightly more complicated as compared to the monolithic integrated case. Moreover, the tiny wires used for connecting the sensing element with the electronics introduce extra parasitics that may attenuate the signal and introduce additional noise.

A more compact integration approach is the monolithic integration, where the silicon chip carries both the electronics and the MEMS [1]. Having the MEMS devices and electronics circuits on the same die results in higher compactness and lower packaging cost and can improve the reliability by minimizing the number of off-chip electrical connections [22]. The elimination of the connecting wirebonds also results in a reduction of parasitics, which may translate into a noise reduction and, in general, in an improved system performance. There are three different ways

of adding the transducer specific process steps and modules to a CMOS process [23]: pre-CMOS micromachining, intra-CMOS or interleaved processing and post-CMOS processing.

In pre-CMOS processing, the MEMS part is completely fabricated before the CMOS. As an advantage, high MEMS deposition temperatures are allowed. However, the MEMS structures need to be protected from the subsequent CMOS processing steps. The technique is further complicated by the fact that MEMS devices may introduce topography in the wafer, thus affecting the resolution of the CMOS steps. In conclusion, the pre-CMOS processing approach introduces lots of changes into a standard CMOS process flow and hence, the integration becomes very expensive.

In the intra-CMOS or interleaved fabrication, the MEMS and the CMOS are processed in parallel, for example by making the MEMS structures below the CMOS interconnect metal lines. As an example, Infineon Technologies fabricated an intra-CMOS capacitive pressure sensor from a 0.8 μm BiCMOS process by using the CMOS poly-Si gate layer as the MEMS structural layer [24]. The capacitor is formed by a fixed electrode in the substrate generated by implantation and a movable membrane (top electrode) of polycrystalline silicon. With this technique it is possible to correctly anneal polysilicon at high temperatures to get the proper stress profile in the polysilicon structure. However, it does not offer flexibility to the MEMS designer in the choice of dimensions and materials. Interleaving the processes also leads to processing compromises that limit the microsystem performance [22]. Moreover, this fabrication module introduces certain modifications to the standard CMOS fabrication flow and makes it necessary to do both the CMOS fabrication and the MEMS micromachining at the same foundry.

A better integration approach, in our opinion, is the post-CMOS fabrication, where the MEMS are processed after the CMOS has been made. This can be done either by adding layers on top of the completed CMOS wafers or by modifying certain CMOS layers (after the CMOS processing) to define the microstructures. Some of the advantages of the post-CMOS integration are:

- It enables integrating the MEMS without introducing any changes in the standard CMOS fabrication processes.
- Both the MEMS and the CMOS can be fabricated in separate foundries.
- The MEMS can be placed on top of the CMOS, reducing the total area consumption of the complete system.

In [25], a post-CMOS technique for the realization of RF-MEMS parallel-plate tunable capacitors directly from a 0.35 μm standard CMOS wafer was presented. The top Al metal interconnect layer (Metal 4) was used as a mask, the metal layers 3 and 1 constituted the top and bottom capacitor plates, respectively, and Metal 2 was used as sacrificial layer. This type of post-CMOS integration technique, using the CMOS interconnect metal layers to define the MEMS, is time and cost efficient since less process steps (practically no material deposition) are required. However, as a drawback, this technique does not offer flexibility in the design. The thickness of the metal layers, used as MEMS structural layers, will be fixed by the CMOS

foundry. Moreover, the use of metals as structural layers might not be ideal for certain applications, like pressure sensors, as metals often suffer from creep [26]. This technique is also not suitable for certain MEMS, as for example piezoresistive pressure sensors, due to the low piezoresistive sensitivity typically exhibited by metals.

The second post-CMOS integration route consists in defining the MEMS by depositing sacrificial and structural layers on top of the completed CMOS wafer. This technique results in a modular approach where the MEMS fabrication is completely decoupled from the CMOS fabrication, allowing for independent optimization and more flexibility in the design. In addition, a new generation of circuitry can easily replace the older one without affecting the MEMS on top of it. For these reasons this technique is considered as the most promising approach for the CMOS-MEMS integration and is therefore the approach adopted in this work.

There is a key condition that must be fulfilled for a successful MEMS-above-CMOS integration: the CMOS post-processing thermal budget must be respected. This condition poses a limit in the maximum temperature that can be used during the MEMS process flow in order not to introduce any damage or degradation in the underlying CMOS circuit. The allowed thermal budget for the MEMS fabrication depends on the CMOS technology considered. For example, the thermal budget limits for 0.35 μm standard CMOS wafers with aluminum based interconnects were experimentally investigated in [27] through annealing tests. It was concluded that the increase in the sheet resistance of the Al interconnects (probably caused by the reaction of Al with Ti forming $TiAl_3$), rather than transistor performance, was the limiting factor. A similar study reported in [28], showed that, for 0.25 μm standard CMOS wafers with again aluminum based interconnects, the thermal budget is mostly limited by an increase in the tungsten-filled intermetal vias. With a failure criterion of 10 % increase, the authors concluded that the maximum allowed post-processing thermal budget is 2 h at 450° C or 30 min at 475° C. For more advanced CMOS technologies, where copper based interconnects and low-permittivity dielectrics are employed as insulating intermetallic layers, the thermal constraints may be even more severe [1].

Due to these thermal budget limitations for post-processing on top of CMOS, high-quality poly-Si, the most commonly used material for surface micromachined MEMS, cannot be used as structural layer since very high temperature (higher than 800° C) [29, 30] are required for dopant activation and for achieving the desired mechanical properties (such as low tensile stress). Materials that can be processed at CMOS-compatible temperatures include metals and amorphous silicon. However, even though the use of these materials as MEMS structural materials has been demonstrated [31–36], they are not ideal candidates due to the performance and reliability problems they might cause. For example, certain metals, like Al, exhibit a tendency to creep, which might result in reliability problems and degraded performance in devices such as pressure sensors or RF switches [37]. Amorphous semiconductors, on the other hand, have large low frequency (1/f) noise, large resistances and often high compressive stress that dramatically limit the performance of MEMS. Neither

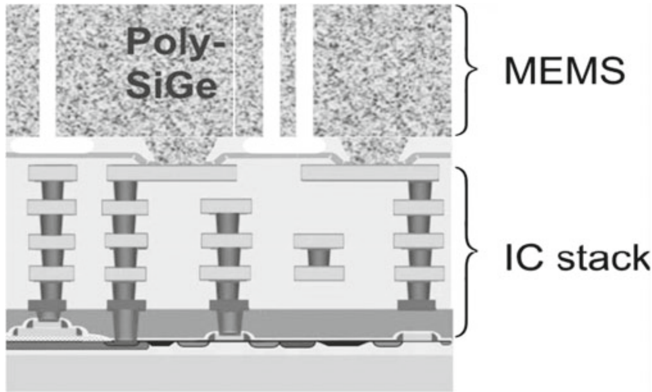


**Fig. 1.3** Conceptual sketch of monolithic integration of poly-SiGe with the conditioning CMOS circuitry

metals nor amorphous silicon are suitable candidates for piezoresistive sensor applications, as their piezoresistive effect is substantially lower than for crystalline or polycrystalline silicon [37, 38].

## 1.4 Polycrystalline SiGe for MEMS-above-CMOS Applications

Polycrystalline silicon germanium (poly-SiGe) has emerged as an attractive MEMS structural material for above-CMOS applications (Fig. 1.3) since it provides the desired mechanical properties (i.e high tensile strength, a low tensile residual stress, and a low stress gradient over the layer thickness) at lower temperatures in comparison to poly-Si [39]. Depending on the germanium concentration and the deposition temperature, the transition temperature from amorphous to crystalline can be reduced to 450° C [40], or even lower, as compared to the 580° C or more necessary for low-pressure chemical vapor deposition (LPCVD) poly Si [41]. At these lower deposition temperatures low resistivity values can still be achieved [42]. In comparision with poly-Si, the melting point of SiGe is lower, but still high enough (well above 900° C) to ensure reliable MEMS devices. Also the elastic constant is highly suitable for MEMS applications (around 140 GPa [43], depending on the Ge content). In addition, poly-SiGe holds a high tensile strength (around 1.6 GPa [44]).

### *1.4.1 SiGe MEMS Demonstrators*

The first poly-SiGe MEMS device fabricated at imec was an infrared bolometer [45]. Since then, several poly-SiGe MEMS devices have been presented. For example, in [46, 47] a poly-SiGe based cantilever structure for probe storage device was

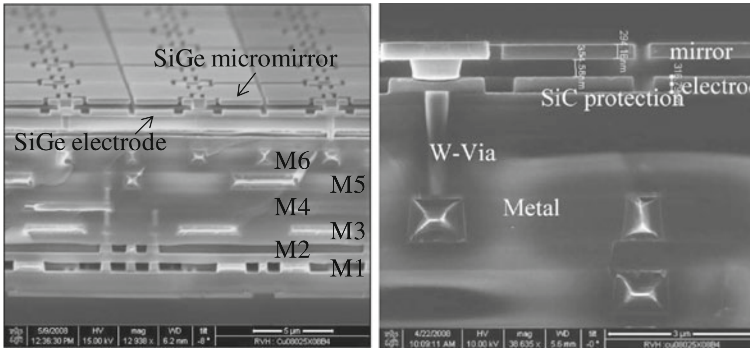


**Fig. 1.4** Cross-Section pictures of poly-SiGe micromirrors deposited on *top* of 0.18 CMOS wafers with 6 Al metal levels [2]. In the *right* picture a W-filled via connecting the Al *top* CMOS layer and the *bottom* SiGe MEMS electrode can be appreciated

reported. In [48, 49] a poly-SiGe resonator, which could also be used as optical (heat) sensors, was presented. Recently, thin film packaging has been added into imec's poly-SiGe MEMS-last technology [50, 51]. Outside of imec, also the University of California Berkley has worked on the development of SiGe structural layers for MEMS-above-CMOS applications, presenting micromachined poly-SiGe structures such as resonators [52] or a low frequency lateral comb drive [53].

Moreover, the suitability of poly-SiGe for the fabrication of MEMS devices on top of standard CMOS wafers with aluminum-based metallic interconnects has also been demonstrated. The first CMOS-integrated poly-SiGe device was a resonator presented by UC Berkley in [22]. In [3], imec presented CMOS-integrated gyroscopes processed on top of 0.35 μm CMOS wafers with five levels of aluminum metal interconnects. In [2], CMOS-integrated $10\,\text{cm}^2$ 11-megapixel SiGe-based micromirror arrays were presented. The micromirror arrays were fabricated on top of planarized 0.18 μm CMOS wafers with six aluminum-based metal levels (see Fig. 1.4). A 300 nm-thick microcrystalline SiGe layer [54] was used as MEMS structural layer. CVD poly-SiGe electrodes were used for micromirror actuation, with tungsten-filled vias providing connection to the underlying CMOS circuit. Each $8 \times 8$ μm pixel can be individually addressed by an analog voltage to enable accurate tilt angle modulation. The obtained pixel density was almost double compared to the state-of-the art. The SiGe micromirrors showed no creep and met a $10^{12}$ cycles mechanical lifetime.

All the above described integrated SiGe-based MEMS devices were fabricated on top of CMOS wafers with aluminum-based metallization. However, the aggressive interconnect scaling, essential to the continuation of Moore's law, has led to the replacement of the traditional aluminum metallization by copper metallization, due to its lower resistivity and improved reliability [4]. In this work, for the first time, the compatibility of poly-SiGe for post-processing on top of copper back-end CMOS is studied. Moreover, a new demonstrator will be added to the list of successful SiGe-based micromechanical devices: a pressure sensor.

### 1.4.2 Poly-SiGe Deposition Technology

In general, silicon germanium (SiGe) thin films can be deposited by Chemical Vapor Deposition (CVD). Silane ($SiH_4$) is typically used as silicon gas source, whereas germane ($GeH_4$) is used as the germanium source and diborane in hydrogen ($B_2H_6$) can be used for "*in situ*" doping. The deposition rate, crystallinity and the germanium content depend mainly on the deposition temperature, gas type, partial pressure and flow rate. In this regard, decreasing the deposition temperature generally results in a decrease in the deposition rate [55]. For the same gas source and deposition temperature, by increasing the Ge content, the growth rate is noticeably increased [29, 55]. An increase in Ge content also enhances crystallization [39]. In general, for a given deposition temperature, it is recommended to keep the Ge content to the minimum value that results in polycrystalline film, as a high Ge content could affect the device reliability due to the fact that Ge is more attacked by humidity in comparison to silicon. Another drawback for using a high Ge content is that, for the same deposition temperature, surface roughness is increased [56], which is not desired in applications such as optical MEMS [57], where a smooth surface is essential.

On the other hand, for the same deposition temperature, both the germanium content and the growth rate decrease by reducing the deposition pressure [58]. The decreasing germanium content can be explained by the fact that reducing the pressure enhances desorption of absorbed hydrogen from the deposition surface. Consequently there are more free sites for decomposition and adsorption of silicon atoms. Also reducing the deposition pressure decreases the time in which the gas precursors are inside the deposition chamber, hence decreasing the growth rate. Also, in [29], it was found that for the same silane and germane flow rates, decreasing the deposition pressure resulted in a slight decrease in the variation of grain size with thickness.

For films deposited at low temperature, *in situ* boron doping enhances films crystallinity and reduces the strain gradient. A detailed overview of the effect of different process parameters on the stress and strain gradient was made by Low et al in [59–61]. Also, increasing the diborane flow enhances the growth rate [62] as the boron atoms act as adsorption sites for both silicon and germanium atoms [63].

In conclusion, to enhance the deposition rate and crystallinity at relatively low temperatures ($\sim$400° C), when using low pressure CVD (LPCVD), it is better to use an "*in situ*" doping with a high boron concentration and increasing the germanium content to $\sim$70 % [39]. However, although CVD techniques result in good quality layers, the obtained deposition rates, even with a high boron and Ge content, are too low (4–20 nm/min). A low deposition rate translates into longer processing times, which, apart from being not cost efficient, increases the risk of CMOS back-end degradations in MEMS-above-CMOS applications [27, 28]. One possibility to increase the deposition rate is to use Plasma Enhanced CVD (PECVD) techniques. For the same deposition temperature and germanium content, a significant increase in growth rate can be achieved by employing PECVD [64]. For example, a PECVD SiGe deposited at 400° C has almost the same deposition rate as Low Pressure CVD

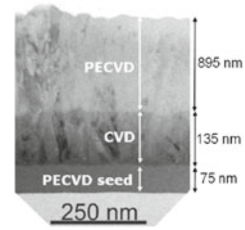


**Fig. 1.5** Transmission electron microscopy (TEM) image of the PECVD-CVD-PECVD poly-SiGe base layer [67]

(LPCVD) SiGe deposited at 600° C. However, at low temperatures, PECVD SiGe films are amorphous.

A combination of the two aforementioned deposition techniques (CVD and PECVD) is a good compromise: a thin CVD-deposited poly-SiGe layer acts as a crystalline seed layer, promoting crystallinity, and a thicker, PECVD layer can be grown on top having columnar-shaped grains. Optionally, a thin PECVD layer is also used below the CVD layer to promote nucleation and initialize growth of the CVD SiGe layer on top of Si-oxide (typical sacrificial layer used in surface micromachined MEMS devices). The layer build-up can be seen in Fig. 1.5. This multilayer (PECVD/CVD/PECVD) process was first reported in [65]. With this technique, high-quality films can be obtained at low temperature (450 ° C) with very high deposition rates (100 nm/min). This technique can be exploited to obtain 1 μm-thick layers. If thicker films are needed, such 1 μm layers can be stacked on top of one another till the desired film thickness is reached [66, 67]. This stacking lowers the overall strain gradient of the SiGe film.

The only drawback of the above presented 1 μm-thick base layer stacking technique is the long deposition time that is needed due to the slow CVD deposition process. For example, for a 4 μm thick stacked layer the deposition time is around 4920 s [67]. Also, a chamber clean is required after each deposition of the 1 μm-thick base layer to avoid particle formation. The poly-SiGe structural layer used in this work is based on a modified version of this stacking technique.

### *1.4.3 Selected Poly-SiGe Structural Layer*

In order to reduce the deposition time, the number of (slow growing) CVD layers in the stack was reduced and the thickness of the base layer was increased to ∼2 μm. Moreover, the initial thin PECVD seed layer was removed from the stacking in order to improve the anchor filling during the pressure sensor fabrication process (see Chap. 4), and lower the contact resistance between the SiGe anchors and the electrodes. This improvement in anchor filling is due to the fact that the CVD poly-SiGe deposition process, unlike the PECVD process, is very conformal. If the PECVD seed layer is omitted, typically an incubation periodis observed, during which a nucleation layer is formed on top of the underlying oxide surface [68]. Once the

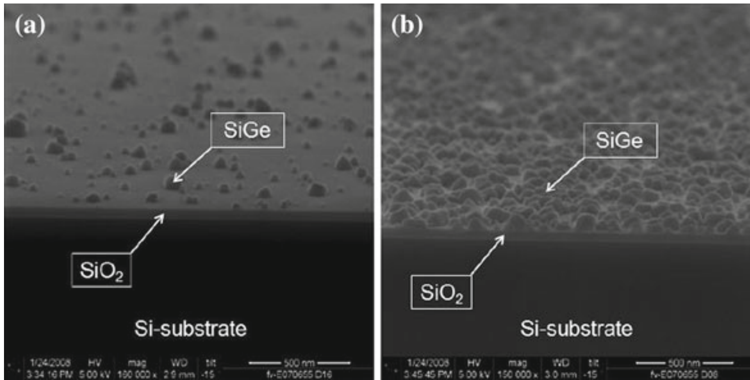


**Fig. 1.6** SEM pictures at different stages of the incubation period showing the gradual formantion of the CVD SiGe nucleation layer on oxide: **a** after 6 s, **b** after 150 s [68]

nucleation period is finished, the CVD SiGe can start to grow. Figure 1.6 shows the gradual formation of the SiGe nucleation layer on top of oxide. First, SiGe "islands" are formed. Once the substrate is completely covered by these "islands", growing in the vertical direction begins. The CVD layer incubation time, resistivity and residual stress can be tuned with the diborane flow [67].

The newly developed base layer is composed of a 400 nm-thick CVD SiGe layer and a 1.6 μm-thick PECVD SiGe layer. The PECVD SiGe layer is deposited on top of the polycrystalline CVD SiGe seed layer to induce crystallization in the PECVD layer [65]. To avoid particle defect generation, the maximum PECVD SiGe thickness that can be deposited before an in-situ chamber clean is required is ∼2 μm. If thicker layers are required, the deposition has to be performed sequentially: PECVD SiGe layers can be stacked on top of each other until the needed thickness is reached. After each PECVD deposition the wafer is removed from the chamber while this one is being cleaned. It has been shown that a Si-germanium oxide layer forms on the surface of the SiGe layer during the chamber clean, creating an interface between each PECVD SiGe deposition. A 30 seconds $CF_4$ clean is performed before each extra PECVD deposition to remove this unwanted oxide at the PECVD/PECVD interfaces [69].

In this work, the selected poly-SiGe structural layer has a thickness of 4 μm. The final nominal SiGe stack build-up is a 400 nm-thick CVD layer+ a 1.6 μm-thick PECVD SiGe + a 2 μm-thick PECVD SiGe. More details about the deposition conditions of this poly-SiGe layer can be found in Chap. 4. The total deposition time is ∼2230 seconds, less than half the time needed to deposit a 4 μm thick layer using the previous multilayer technique with 1 μm thick base layers. The reduction in deposition time is due to the increase in the thickness of the base layer (this action reduces the total number of chamber cleans needed, and thus, the total processing

time), and the reduction of time-consuming CVD depositions (only one is used in the new deposition technique, while the previous technique required four CVD deposition for the same total layer thickness).

## 1.5 A Poly-SiGe Based MEMS Pressure Sensor

MEMS pressure microsensors typically have a flexible diaphragm that deforms in the presence of a pressure difference. The deformation is converted to an electrical signal appearing at the sensor output. There are many well-established transduction principles for MEMS pressure sensors, such as piezoresistive, capacitive, piezoelectric or optical transduction [70]. Most of the commercially available pressure sensors use either the piezoresistive or the capacitive detection principle. In piezoresistive pressure sensors, several piezoresistors, typically arranged in a Wheatstone bridge configuration, are placed in the membrane. The membrane deflection, due to a pressure difference, translates into a change in resistance, which results in a variation of the bridge output voltage. In capacitive pressure sensors, the membrane acts as a movable electrode, while either the substrate or another layer deposited below the membrane acts as a fixed bottom electrode. The membrane deflection is thus detected by a change in the capacitance between the two electrodes.

### *1.5.1 Applications of MEMS Pressure Sensors*

Micromachined pressure sensors are one of the first developed MEMS devices that have been successfully commercialized [71]. They are used for a wide-range of applications in various fields like the automotive industry, for biomedical and military applications, for process control and consumer electronics. Due to their relatively low prices and expanding use in a host of automotive, medical and industrial applications, pressure sensors will become the leading MEMS device by 2014, according to IHS iSuppli [72]. By 2014, the revenue for MEMS pressure sensors will amount to $1.85 billion.

The automotive sector remains in 2011 the biggest area for MEMS pressure sensors, claiming 72 % share in revenue, followed by medical electronics at 11 % and the industrial segment at 10 %. The remaining 6 % of the market is split between consumer electronics on the one hand, and military-aerospace on the other [72]. Examples of succesful commercial applications include tire [73] and blood pressure sensors [74]. In the consumer sector, Freescale has recently presented a MEMS pressure sensor to be used as altimeter for indoor navigation in mobile applications [75]. Table 1.1 list some examples of present and future MEMS pressure sensors commercial applications in different industries.

Automotive design engineers typically use pressure sensors in four application areas: engine optimization, emission control, safety enhancement and comfort [76]. For safety enhancement, for example, pressure sensors monitor tire pressure and warn

the driver when a dangerous loss of pressure is detected. In EU, starting 2012, all new models of passenger cars must be equipped with a TPMS (Tire Pressure Monitoring System). Similar rule was already approved in US in 2007. Another important application in safety enhancement is brake fluid pressure monitoring. Pressure sensors can also be used for seat occupancy detection. As drivers and passengers increasingly vary in size and shape, pressure sensors are used to make driving more comfortable by controlling inflatable air bladders in dynamic seats for better lumbar support.

The largest market for MEMS pressure sensors in the medical sector is the disposable sensor used to monitor blood pressure [76]. Within the industrial sector [76], big segments for MEMS pressure sensors include the heating, ventilation and air conditioning (HVAC) sector, level measurements, and various industrial process and control applications. Aircrafts, for instance, use the sensors to monitor engines, flaps and other functions, in addition to precision altitude air pressure measurement. Military applications include tire-pressure monitoring in tanks. MEMS pressure sensors have also been tested in the booster rocket of the ejection seat used in the F-14 fighter [77].

MEMS pressure sensors to date have not been used as much in the consumer electronics and mobile space [72]. Among their diverse applications, however, are weather stations, sport watches, bike computers, diving equipment and pedometers, along with white goods, such as water-level sensors employed for energy-efficient washing machines. For the mobile segment, high-end smartphones in the future could include pressure sensors to act as an altimeter for location-based services indoors.

### *1.5.2 Technologies for MEMS Pressure Sensors*

For years single-crystal silicon (Si) has been the dominant material in MEMS pressure sensor applications thanks to its excellent mechanical and electrical properties [78]. Silicon pressure sensors are traditionally fabricated by bulk micromachining, in which the diaphragm is formed by a back-side silicon etching process. The sealed

**Table 1.1** Examples of present and future MEMS pressure sensors applications in different industries

| Industry | Applications |
|---|---|
| Automotive | Tire pressure monitoring, control of hydrocarbon emissions, brake fluid monitoring, engine control, seat comfort, etc |
| Medical | Blood pressure monitoring, respiratory monitoring, measurement of intrauterine pressure during birth, inhalers, etc |
| Industrial-militar | Process control, altitude measurements, tire-pressure monitoring in tanks, booster of ejection seats, etc |
| Consumer | Altimeters, weather stations, water-level sensors for energy-efficient washing-machines, etc |

cavity is then obtained by wafer bonding: a cap wafer (silicon, glass or ceramic) is bonded on the MEMS wafer, creating a hermetically sealed cavity. Wafer bonding includes [79] direct bonding (anodic and fusion bonding) and bonding using intermediate layers (metals or insulators). These wafer bonding techniques, even though well established and commercialized, are costly because they require a second substrate, careful alignment of the two parts, double the thickness of the chip and need additional die for the sealing frame. Moreover the high temperatures, high voltages and/or high pressures involved may affect the sensor membrane properties and therefore its performance.

In recent years surface micromachined pressure sensors based on poly-Si have appeared as candidates to replace the traditional bulk-micromachined silicon pressure sensors. Surface micromachining offers a series of advantages over bulk micromachining devices: more devices per unit area, better control of the membrane thickness, easier integration with electronics and the elimination of the need for the high temperatures, pressures or voltages usually employed in wafer bonding. In surface micromachining the membrane layer, usually poly-Si, is deposited on top of a sacrificial material (typically oxide), deposited or grown on the Si substrate. Access holes or channels are provided in the membrane to remove the sacrificial material and create a cavity underneath. After release, the access holes are sealed by a reactive gas sealing process (at temperatures above 900° C) [80], or by thin film deposition.

Apart from crystalline silicon and poly-Si, other materials used in the fabrication of MEMS pressure sensors include SiC and diverse metals. SiC material is attractive for high temperature applications because of its mechanical robustness, chemical inertness, and electrical stability at elevated temperatures and is expected to perform reliably well above 500° C [81]. Existing high-temperature pressure sensors are implemented using SiC-based piezoresistive devices and have demonstrated sensing capabilities up to 600° C [82–84]. Also SiC based capacitive pressure sensors capable of working at temperatures up to 600° C have been presented [85]. Metals exhibit a piezoresistive sensitivity several orders of magnitude lower than semiconductors [37]. For this reason, the use of metals in piezoresistive pressure sensors is very limited. On the other hand, several metal-based MEMS capacitive pressure sensors have been proposed [32, 86–88].

### *1.5.3 Why a Poly-SiGe Based MEMS Pressure Sensor?*

The advantages of the monolithic integration of the MEMS devices with the driving, controlling and signal processing electronics on the same CMOS substrate were already highlighted in Sect. 1.3. Similar benefits can be expected for monolithically integrated MEMS pressure sensors. The post-processing route (fabricating MEMS directly on top of CMOS) is the most promising approach for CMOS-MEMS monolithic integration as it leads to smaller die areas and enables integrating the MEMS without introducing any changes in standard foundry CMOS processes. Processing the micromechanical pressure sensors on top of the CMOS circuitry will lead to

smaller die areas, reduced packaging complexity and improved performance thanks to the reduction of interconnection parasitics. However, as previously explained, for above-CMOS integration, the MEMS fabrication thermal process budget must be carefully designed in order to avoid introducing any damage or degradation in the performance of the underlying electronics [27, 28]. Until now, the maximum post processing temperature on CMOS wafers with Al interconnects is generally considered to be $\sim$450° C [22, 27, 28].

Of the possible structural materials for MEMS pressure sensor applications listed above, high quality poly-Si, the most commonly used material for surface micromachined MEMS pressure sensors, and SiC are no suitable candidates for above-CMOS integration since they require high processing temperatures [29, 30, 89–91]. With bulk micromachining of crystalline silicon it is not possible to process the MEMS on top of the CMOS. It however still offers the possibility of monolithic integration by, for example, use a back-side wet etch process to create a free standing membrane after the CMOS processing is completed. A wafer-bonding technique can then be used to form a cavity. This technique requires less process steps and offers the possibility of using crystalline silicon, with a large piezoresistive effect, as sensing element. However, it presents also many limitations [23]. The CMOS process may have to be slightly modified to improve the doping profile for piezoresistors. A special mechanical wafer holder is used to protect the front of the wafer (which contains the CMOS circuit) during the back-side etch. The wafers must be manually placed in the mechanical holder, which is a slow production process. Finally, many layers cover the membrane, which may deteriorate sensor sensitivity and temperature dependence.

One possibility to have above-CMOS integration is to use metals as structural layer, either by deposition on top of completed CMOS wafers or by using the top CMOS metal interconnect layers to fabricate the MEMS device [86–88]. However, the use of metals as structural layers might not be ideal for pressure sensors, as metals often suffer from creep [26]. Metals are also not suitable for piezoresistive pressure sensors. Using the top CMOS metal layers, although cost efficient, does not offer flexibility in the design. The thickness of the metal layers, used as MEMS structural layers, will be fixed by the CMOS foundry.

Poly-SiGe, on the other hand, offers a generic and flexible technology for above CMOS integration. Since the MEMS fabrication can be completely decoupled from the CMOS fabrication, the designer is no longer limited by the CMOS foundry, and the MEMS dimensions can be optimized based on the application requirements. Moreover, recent experiments demonstrated the piezoresistive properties of microcrystalline-SiGe [92], broadening the possible applications of this material to the MEMS piezoresistive sensor market. With poly-SiGe it is also possible to monolithically integrate multiple sensors with the electronics, enabling sensors measuring motion along different axes to be precisely aligned, to have greater accuracy and to be less susceptible to external disturbance. If we take as an example a tire pressure monitoring system (TPMS), which is one of the most rapidly growing applications for MEMS pressure sensors, it normally includes a temperature sensor, a pressure sensor and an accelerometer (to power on the system when motion is detected). With

poly-SiGe, all of these MEMS sensors could be monolithically integrated together with the electronics, reducing the total system area and cost.

In this work, for the first time, both capacitive and piezoresistive poly-SiGe-based pressure sensors are fabricated and tested. As mentioned above, capacitive and piezoresistive sensing are the most used transduction principles in MEMS pressure sensor applications. The reasons to prefer a piezoresistive sensor include excellent linearity and simple conditioning circuits. However the dependence of the piezoresistive coefficients with temperature [93, 94] poses a serious limitation. The principal advantages of capacitive sensors over piezoresistive pressure sensors are increased pressure sensitivity and decreased temperature sensitivity [70, 95]. The pressure response of capacitive sensors exhibit, however, a larger nonlinearity. Some tire pressure sensor providers (like Motorola and Freescale Semiconductor) prefer capacitive sensors because they consume less power [73]. Other companies, like EnTire Solutions and SensoNor, find piezoresistive sensors more linear than capacitive sensors and a bit more accurate over wide pressure and temperature ranges [73]. They also point out that, while a piezo-resistive sensor may draw more power than a capacitive one, the sensor still accounts for a small percentage of the overall power consumed in the system.

The process flow developed in the frame of this work allows for both piezoresistive and capacitive sensors to be fabricated simultaneously. The maximum processing temperature of the complete sensor, including the poly-SiGe piezoresistors, is kept below 460° C to enable above-CMOS integration. The possibility of above-CMOS integration is particularly interesting for capacitive pressure sensors. For applications that require higher sensitivity, an array of such sensors can be used. Thanks to the possibility of post-processing on top of standard CMOS, relative large arrays of these capacitive sensors can be integrated with the readout circuitry without increasing the die area. Also the elimination of off-chip connections is crucial for the performance of capacitive pressure sensors, since the excessive signal loss from parasitic capacitance has long been an important concern which hindered the development of miniaturized capacitive sensors [87]. For piezoresistive pressure sensors the reduction of die area, although important, may not be as noticeable as for capacitive sensors. However, the reduction of parasitics may lead to better SNR, very important for high precision applications such as altimeters for mobile devices.

## 1.6 Outline of the Book

This book is divided into eight chapters. Chapter 1 introduces the concept of microelectromechanical systems, with their benefits and applications, and reports on the different approaches that exist for the CMOS-MEMS monolithic integration. Polycrystalline silicon-germanium is presented as a promising flexible and generic technology for the fabrication of the MEMS directly on top of their readout circuitry. The concept of ‘building’ a poly-SiGe MEMS structural layer is discussed and the deposition conditions for the poly-SiGe structual layer used in this work are listed.

Finally, the motivation for improved MEMS pressure sensors using imec's poly-SiGe technology is explained.

Chapter 2 focuses on the electrical and piezoresistive properties of polycrystalline silicon-germanium for different boron concentrations, germanium contents and deposition conditions. A new poly-SiGe film deposited at CMOS-compatible temperatures is developed and optimized for piezoresistive sensors applications.

Chapter 3 deals with the design of the piezoresistive pressure sensors. An overview of the most important parameters to evaluate the performance of a pressure sensor is presented. Finite-element simulations, together with the piezoresistive coefficients experimentally obtained in Chap. 2, are used to predict the performance of a possible poly-SiGe based piezoresistive pressure sensor. The considered design parameters include: regarding the sensor membrane, area, thickness and shape, and with respect to the poly-SiGe piezoresistors, dimensions, shape and placement. The design is optimized mainly in terms of pressure sensitivity and nonlinearity.

The developed process flow for the fabrication of poly-SiGe based surface micromachined pressure sensors is introduced in Chap. 4. The presented fabrication process allows for the simultaneous fabrication of both piezoresistive and capacitive pressure sensors. To enable above-CMOS integration the maximum processing temperature of the complete sensor, including the poly-SiGe piezoresistors, is kept below 460° C. Also, to protect the electronic circuit from the aggressive etch and deposition steps which are needed to fabricate the MEMS devices, an appropriate SiC passivation layer is included. A detailed description of the main process developments performed for the successful fabrication of the pressure sensors is also given.

The sealing of the reference cavity is one of the most important steps in the fabrication of a pressure sensor. Chapter 5 describes the sealing of polycrystalline SiGe (poly-SiGe) surface micromachined cavities for above-CMOS pressure sensor applications. Two different sealing techniques involving thin-film deposition are investigated: direct sealing and sealing using an intermediate porous layer. The sealing materials studied include Si-oxide, aluminum and SiGe. Both $\mu$c-SiGe and SiC are evaluated as porous layer. The sealed cavities are characterized considering many different aspects such as the inside-cavity sealing layer deposition, the cavity pressure, the membrane stress and the short and long term hermeticity. Analytical modelling and Finite Element Methods (FEM) were used to study the load-deflection behaviour of the (poly-SiGe/sealing layer) composite membranes and derive not only the pressure inside the cavities, but also the overall stress of the sealed membranes. The analytical model was modified to account for the effect of the release holes on the membrane stiffness.

In Chap. 6, the realized stand-alone poly-SiGe pressure sensors (both piezoresistive and capacitive) are tested and evaluated. The piezoresistive pressure sensors are evaluated mainly in terms of pressure sensitivity, although other aspects, such as temperature coefficient of sensitivity, offset voltage and non-linearity are also considered. The obtained measurement results are compared to the values predicted by simulations (Chap. 3); to explain the mismatch between the measured and the simulated sensitivity, further simulations, including the effect of the SiC isolation

layer and the oxide sealing layer, are performed. On the other hand, for the capacitive pressure sensors only the sensitivity is evaluated.

Chapter 7 describes the fabrication and testing of an integrated poly-SiGe-based piezoresistive pressure sensor directly fabricated above 0.13 μm Cu-backend CMOS technology. An instrumentation amplifier, with two Cu metal layers and oxide intermetal dielectric, has been designed and fabricated to act as the sensor readout circuit. The processing of the integrated sensor is explained in detail, with special attention to the development of the CMOS (Cu) to MEMS (Al) interface. The effect of the MEMS processing on the underlying CMOS performance is also characterized. Finally, the performance of the fabricated integrate sensor is evaluated.

Chapter 8 presents the conclusions of this work and recommendations for further studies.

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# Chapter 2
# Poly-SiGe as Piezoresistive Material

For years monocrystalline silicon has been the dominant material for the fabrication of piezoresistive MEMS sensors thanks to its high gauge factor and excellent mechanical properties. Despite its lower gauge factor, polycrystalline silicon (poly-Si) offers several advantages over monocrystalline silicon for sensor applications. In poly-Si piezoresistive pressure sensors, the piezoresistors can be laid out on an insulation layer grown on top of the membrane and are defined by deposition and etch, and not by implantation like in silicon sensors. This avoids time- and temperature-dependant p-n junctions and can be used at operating temperatures up to 200 °C. However, neither silicon nor poly-Si allows monolithic integration of MEMS directly on top of the CMOS. Polycrystalline silicon-germanium (poly-SiGe) is a very promising material for processing MEMS on top of CMOS thanks to its lower deposition temperature as compared to poly-Si. The monolithic integration of the MEMS on top of the electronics can potentially lead to smaller systems, improved performance and reduce packaging and instrumentation costs.

This chapter presents a detailed investigation on the influence of deposition conditions, germanium content and doping concentration on the electrical and piezoresistive properties of poly-SiGe. The studied electrical properties include resistivity and temperature coefficient of resistance (TCR). The experimental evaluation of the piezoresistive coefficients of poly-SiGe is especially important for the design of a poly-SiGe based piezoresistive pressure sensor, as they will influence the sensitivity of the sensor.

## 2.1 Introduction to Piezoresistivity

First discovered by Lord Kelvin in 1856, the piezoresistive effect describes the changing electrical resistance of a material due to an applied mechanical stress. Piezoresistivity is extensively used as sensing principle in many mechanical sensors [1]. In the MEMS field, piezoresistivity is used in a wide variety of sensing applications

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including, among others, accelerometers [2, 3], gyroscopes [2, 4], resonators [5, 6] and pressure sensors [7, 8], to which this book is devoted.

The relative resistance change ΔR/R in electrical resistance, due to strain (or stress) of a resistor with resistivity $\rho$, length $l$ and cross-sectional area $A$ is given by (2.1):

$$R = \rho \cdot \frac{l}{A} \rightarrow \frac{\Delta R}{R} = \frac{\Delta \rho}{\rho} + \frac{\Delta l}{l} - \frac{\Delta A}{A} \tag{2.1}$$

The change in resistance due to applied stress is a function of geometry and resistivity changes. On one hand, the length and cross section will change when the resistor is strained. For example, when a resistor is stretched under longitudinal stress, its length will increase whereas the cross-sectional area will reduce due to the Poisson effect, resulting in a resistance increase. This geometry deformation mechanism is the main responsible for the resistance change with strain in metal resistors. On the other hand, in semiconductors, also the resistivity changes significantly with strain. The magnitude of resistance change due to this last mechanism is typically much greater than what is achievable from the first one.

### *2.1.1 Single Crystalline Materials*

#### 2.1.1.1 Physical Nature

The piezoresistive effect of single crystalline semiconductors like silicon and germanium was observed by Charles S. Smith in 1954 for the first time [9]. The piezoresistive phenomenon in semiconductors arises from the influence of mechanical stress on the energy band structure, thereby varying the carrier effective mass, the mobility and the conductivity. The piezoresistivity in bulk n-type material has been well explained in terms of the many-valley model [10]: the resistance changes with stress due to a shift of the three different conducting valley pairs, which causes a redistribution of the carriers between valleys with different mobilities. In p-type material the phenomena is somewhat more complex, and both a transfer of carriers and a change in effective mass needs to be considered. The physical origin of p-type silicon piezoresistivity can be explained by studying the stress-effect on the valence-band structure. Figure 2.1 shows a simplified sketch of the valence-band structure of silicon, which comprises two sub-bands, heavy- and light-hole bands, degenerated at $k = 0$, and a split-off band 40 meV below these bands at zero stress [11, 12]. The application of uniaxial stresses will lift the degeneracy and alter the valence band structure, causing the sub-bands to be shifted relative to each other. As a result, the effective masses of the heavy and light holes will change and holes will repopulate between the heavy- and light-hole bands.

Under uniaxial tensile stress, the heavy-hole sub-band moves up and the light-hole sub-band moves down with a band splitting ΔE (Fig. 2.1b). Since holes tend to fill lower energy levels, this shift causes a hole transfer from the light-hole band to the

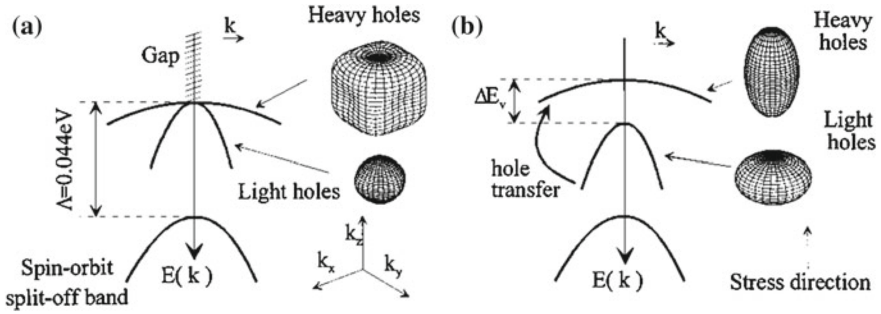


**Fig. 2.1** Simplified sketch of p-type silicon valence-band and energy surfaces in k space, for both heavy- and light-hole bands. **a** Unstressed case. The energy surfaces are warped due to the degeneracy. **b** Under uniaxial tensile stress. The energy surfaces are elongated and oblate ellipsoids, both having axial symmetry along the stress direction. *Reprinted with permission from* [11]. *Copyright (1998) American Physical Society*

heavy-hole band, resulting in more carriers with low mobility and less carriers with high mobility. Since the conductivity is proportional to the mobility, the resistance increases with the tensile stress. On the other hand, in case of a uniaxial compressive stress, the light-hole band rises above the heavy-hole band; the resulting hole repopulation from the heavy- to light-hole band translates into a decrease in the resistance. In Fig. 2.1, next to the E-K diagram, the energy surfaces of the heavy- and light-hole bands are also shown. As can be seen, the shapes of these constant energy surfaces are also altered under applied stress, causing a change in the effective masses of the heavy and light holes.

#### 2.1.1.2 Mathematical Description

Following Ohm's law, for a three-dimensional anisotropic crystal (like silicon or germanium), the electric field vector (E) is related to the current vector ($i$) by a $3 \times 3$ resistivity tensor. For silicon the resistivity tensor is symmetrical, reducing the number of independent coefficients to six [1, 13, 14]:

$$\begin{pmatrix} E_x \\ E_y \\ E_z \end{pmatrix} = \begin{bmatrix} \rho_1 & \rho_6 & \rho_5 \\ \rho_6 & \rho_2 & \rho_4 \\ \rho_5 & \rho_4 & \rho_3 \end{bmatrix} \cdot \begin{pmatrix} i_x \\ i_y \\ i_z \end{pmatrix} \tag{2.2}$$

If the cartesian axes are aligned with the <100> axes of the crystal, the $\rho_1$, $\rho_2$ and $\rho_3$ define the dependence of the electric field along one of the <100> crystal axes on the current in the same direction; $\rho_4$, $\rho_5$ and $\rho_6$ are cross-resistivities, relating the electric field along one axis to the current in the perpendicular direction. For an isotropic conductor, like for example unstressed silicon, $\rho_1 = \rho_2 = \rho_3 = \rho$ and

$\rho_4 = \rho_5 = \rho_6 = 0$. As seen before, when mechanical stresses are applied, the bulk resistivity will change as follows:

$$\begin{pmatrix} \rho_1 \\ \rho_2 \\ \rho_3 \\ \rho_4 \\ \rho_5 \\ \rho_6 \end{pmatrix} = \begin{bmatrix} \rho \\ \rho \\ \rho \\ 0 \\ 0 \\ 0 \end{bmatrix} + \begin{pmatrix} \Delta\rho_1 \\ \Delta\rho_2 \\ \Delta\rho_3 \\ \Delta\rho_4 \\ \Delta\rho_5 \\ \Delta\rho_6 \end{pmatrix} \tag{2.3}$$

The stress situation of the material can also be decomposed into six components: three normal stresses ($\sigma_{xx}$, $\sigma_{yy}$ and $\sigma_{zz}$) and three shear stresses ($\tau_{xy}$, $\tau_{yz}$ and $\tau_{zx}$). The change in resistivity and the applied stress are related through a matrix of 36 piezoresistive coefficients, $\pi_{ij}$, expressed in $Pa^{-1}$. Due to symmetry, for a cubic crystal like silicon or germanium, the 36 coefficients are reduced to three linearly-independent piezoresistive coefficients, $\pi_{11}$, $\pi_{12}$ and $\pi_{44}$, and the matrix takes the following form [1, 13]:

$$\frac{1}{\rho} \cdot \begin{pmatrix} \Delta\rho_1 \\ \Delta\rho_2 \\ \Delta\rho_3 \\ \Delta\rho_4 \\ \Delta\rho_5 \\ \Delta\rho_6 \end{pmatrix} = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \cdot \begin{pmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \tau_{xy} \\ \tau_{yz} \\ \tau_{zx} \end{pmatrix} \tag{2.4}$$

Neglecting the geometrical changes in (2.1), the relative resistance change in a semiconductor can be considered to arise exclusively from the shift in resistivity ($\Delta R/R = \Delta\rho/\rho$). In the most common situations for piezoresistive sensor devices, there is a contribution to resistance change from stresses that are longitudinal ($\sigma_l$) and transverse ($\sigma_l$) with respect to the current flow. The relationship between resistance change and applied stress can then be described by only two piezoresistive coefficients according to:

$$\frac{\Delta R}{R} = \pi_l \sigma_l + \pi_t \sigma_t \tag{2.5}$$

where $\pi_l$ and $\pi_t$ are the longitudinal and transverse piezoresistive coefficients. The above expression is independent from the crystal orientation. Both $\pi_l$ and $\pi_t$ are a linear combination of $\pi_{11}$, $\pi_{12}$ and $\pi_{44}$; the expressions, for various directions in cubic crystal, can be found in [13].

In general, $\pi_l$ in p-type silicon is found to be positive while $\pi_t$ has a negative sign. According to [11], the longitudinal piezoresistive properties of p-type silicon are mainly explained by the hole transfer from the light- to the heavy- hole band, leading to an increase in resistivity due to the average effective mass growth (since $m_{1||} > m_{2||}$, where $m_{1||}$ and $m_{2||}$ represent the longitudinal effective masses for the heavy and light holes, respectively). In the transverse case, although the hole transfer

tends to induce an increase of resistivity (similar as for the longitudinal case), the negative sign for $\pi_t$ is explained by the mass change effect. The transverse effective masses for the heavy ($m_1\perp$) and light ($m_2\perp$) holes are strongly stress dependent, with $m_1\perp$ decreasing sharply with tensile stress, while $m_2\perp$ increases. Therefore, in the transverse case, the hole transfer translates into a decrease in resistivity as $m_1\perp < m_2\perp$.

### 2.1.2 Polycrystalline Materials

A polycrystalline material is composed of small crystallites or "grains" separated from one another by grain boundary regions. The grain boundaries contain a large number of defects and dangling bonds which act as trapping states and/or segregation sites [15]. The electrical behaviour of the grain boundaries can be modelled by a potential barrier, which limits the carrier transport. This potential barrier is due to trapping of free carriers by grain boundaries [16], which creates a space-charge region inside the grain.

For polycrystalline semiconductor material, the resistivity of the film can be described by contributions from both the grain and grain boundary and is given by [17]:

$$\rho = \frac{L - (2W + \delta)}{L} \cdot \rho_g + \frac{(2W + \delta)}{L} \cdot \rho_b \tag{2.6}$$

where $\rho$, $\rho_g$ and $\rho_b$ are the resistivities of the film, grain and grain boundary, respectively, and $\delta$ is the grain boundary thickness. $L$ and $W$ are the lengths of the grain and depletion region, respectively.

Under mechanical stress, the overall relative resistivity change ($\Delta\rho / \rho$) will be a combination of the fractional changes in the grain and grain boundary resistivities, $\Delta\rho_g / \rho_g$ and $\Delta\rho_b / \rho_b$, respectively. In polysilicon, the grains can be considered as small single crystals with the same lattice and same energy band structure as single crystal silicon. Therefore, in a first approximation, the stress effect on $\rho_g$ can be considered to be the same as for the silicon resistivity [11]. The potential barrier piezoresistivity can be studied starting from the grain boundary resistivity expression. In general, $\rho_b$ is calculated taking into account thermionic emission and tunneling effect through the potential barrier [17]. The physical explanation for the grain boundary piezoresistivity also involves heavy-hole and light-hole valence bands [11]. A theoretical model for piezoresistance in polysilicon was developed by French and Evans, and can be found in [17].

In general, the piezoresistive effect of the grain boundary is much lower than in the grain crystal. Moreover, due to the random orientations of the grains and considering that the piezoresistivity of silicon is anisotropic, it is necessary to average the grain region piezoresistivity in order to take into account all possible orientations of the grains [11]. These two considerations help explain the lower piezoresistive effect in polysilicon as compared to single crystal silicon.

### *2.1.3 Definition of the Gauge Factor*

A quantity often used to characterize the piezoresistive properties of a material is the so-called gauge factor (G). The gauge factor is defined as the ratio of the relative resistance change to the mechanical strain ε (with ε = dl/l, where l is the original length):

$$G = \frac{\Delta R}{\varepsilon R} \tag{2.7}$$

For an isotropic, homogeneus material, stress is related to strain by Hooke's Law [18], $\varepsilon = \sigma / E$, where $E$ is the Young's modulus. The gauge factor for most metals is about 2 [19], attributable to their geometric changes when subjected to mechanical stress. For p-type single crystal silicon gauge factors in the range 100–175 have been reported [9, 20]. N-type silicon, on the other hand, has a negative gauge factor down to −140. The value of the gauge factor in silicon decreases with increasing temperature and doping concentrations [1, 21]. The gauge factor of polycrystalline silicon is also not constant but is influenced by the doping concentration, type of dopant, grain size and temperature of the substrate. In [17] a maximum gauge factor of 43 was found for a boron doped ($B \sim 1 \times 10^{19}\,cm^{-3}$) poly-Si layer. In [22] and [23] gauge factors from 15 to 30 and from 2 up to 20, respectively, were experimentally obtained for poly-Si layers with different boron concentrations.

## 2.2 Sample Preparation

### *2.2.1 Layout and Fabrication Process*

Figure 2.2 shows the layout of several of the designed samples for the characterization of the electrical and piezoresistive properties of poly-SiGe. The maskset comprises two masks: one for the metal interconnects and bondpads (in light grey) and one mask for the poly-SiGe resistors (in black). Figure 2.2a shows the layout of four differently orientated ($\varphi = 0°, 60°, 90°$ and $150°$) resistors used in piezoresistive measurements. All four resistors have the same dimensions, L = 2.95 mm and W = 50 μm in Fig. 2.3. To measure the resistivity and TCR of the poly-SiGe layers, resistors with different lengths (from 0.5 to 18 mm) and widths (from 25 to 100 μm) are used (Fig. 2.2b, c).

To fabricate the samples, silicon wafers (100) covered with 500 nm-thick Si-oxide were used as starting substrates. The poly-SiGe layers, with thicknesses between 200 and 400 nm (see Table 2.1), are then deposited on top of the Si-oxide using chemical vapor deposition (CVD). The poly-SiGe layers were patterned using a dry etch process for ∼35 s in a Surface Technology Systems (STS) Advanced Silicon Etch (ASE) inductively coupled plasma DRIE tool [24]. Each resistor is contacted by 1 μm-thick sputter-deposited aluminum copper (AlCu 0.1 %) traces to four

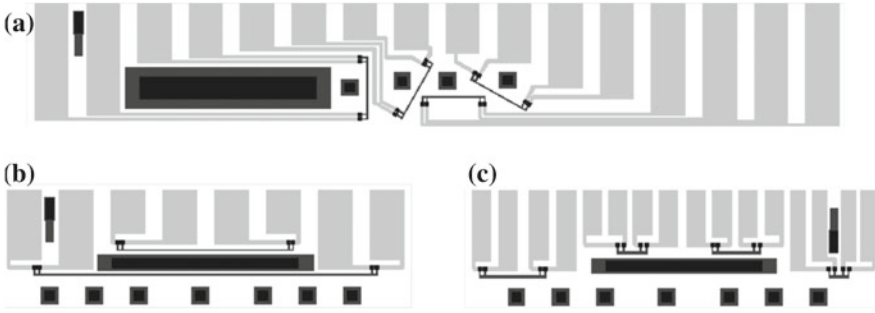


**Fig. 2.2** Layout of poly-SiGe resistors connected by aluminum pads. **a** Four differently orientated resistors to measure the piezoresistive coefficients following (2.5). **b** Two resistors with different lengths (9 and 18 mm) and width = 100 µm that can be used to measure piezoresistivity, resistance and/or TCR. **c** Resistors with four different lengths, 3, 2, 1 and 0.5 mm, and the same width (150 µm) to measure resistance and/or TCR

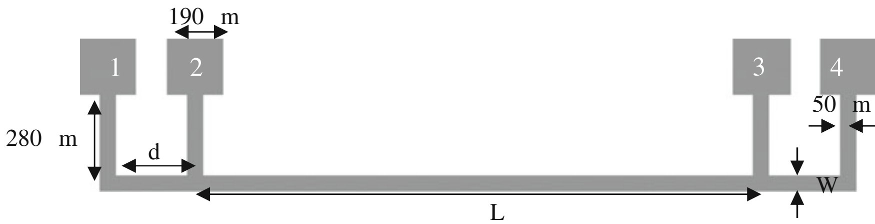


**Fig. 2.3** Schematic representation of the designed resistors. Resistors with different lengths (from 0.5 to 18 mm) and widths (25, 50, 100 and 150 µm) were designed. Each resistor is connected by four pads in order to perform four point measurements. By this method, a current is applied to the resistor through contacts 1 and 4 while the voltage drop is measured between contacts 2 and 3. Distance d between contacts 1–2 and 3–4 is 150 or 200 µm, depending on the resistor

**Table 2.1** Relevant processing conditions and material properties for the different poly-SiGe layers considered

| Layer | Deposition temperature (°C) | Ge content[a] (%) | Boron concentration ($cm^{-3}$) | Annealing temperature (°C) | Thickness (nm) | Young's modulus[e] (GPa) |
|---|---|---|---|---|---|---|
| 1 | 460 | 76 | $3.6 \times 10^{21}$ [b] | – | 361±11[c] | – |
| 2 | 500 | 64 | $5\times10^{17}$–$1\times10^{20}$ | 570 | 386±16[d] | 108.2±1.97 |
| 3 | 540 | 49 | | 620 | 354±10[d] | 107.2±1.06 |
| 4 | 460 | 77 | $5\times10^{18}$–$5\times10^{19}$ | 455 | ~200 | 103.8±2.69 |

[a] Determined by Rutherford Back Scattering (RBS)
[b] Determined by Secondary Ion Mass Spectrometry (SIMS)
[c] Determined using a Dektak profiler
[d] Estimated from cross-section pictures
[e] Obtained by nanoindentation

bonding pads in order to measure the resistance by the four-point probe method (see Fig. 2.3), eliminating any spurious contribution of contacts and metal traces. The AlCu metal traces were etched in a wet solution containing acetic acid, $H_3PO_4$ and $HNO_3$. Figure 2.4 shows microscope pictures of typical samples used for piezoresistive measurements.

### 2.2.2 *Poly-SiGe Layers Studied*

In this work, poly-SiGe layers with different germanium content and doping concentration were characterized. The impact of varying the processing conditions on the electrical and piezoresistive properties of the layers was also characterized. These processing conditions include deposition temperature, annealing temperature and time and deposition tool. Table 2.1 lists all the poly-SiGe layers studied with their relevant process parameters. Of the four different poly-SiGe layers considered, only layer 4 was developed specifically for this work. Layers 1–3 correspond to existing recipes in imec's deposition tools, and for this reason they were characterized first. Layer 1 was deposited *in-situ* doped while the other three layers were deposited undoped and then doped through ion implantation of boron. This last doping procedure allows for a more controlled and varied range of boron concentrations. Only p-doped layers with boron will be considered in this work, since boron has lower activation energy as compared to phosphorus (traditional n-type dopant in piezoresistive materials), which is important considering the thermal restrictions for above-CMOS integration.

The first layer studied is a heavily B-doped poly-SiGe layer used as the standard electrode layer in the SiGe-MEMS platform in imec (see Chap. 4). This *in situ* doped CVD poly-SiGe layer is deposited at 460 °C chuck temperature (450 °C wafer temperature) and 4.3 Torr in an Applied Materials (AMAT) PECVD CxZ chamber, mounted on an Applied Materials Centura Giga-Fill SACVD platform. The silicon gas source

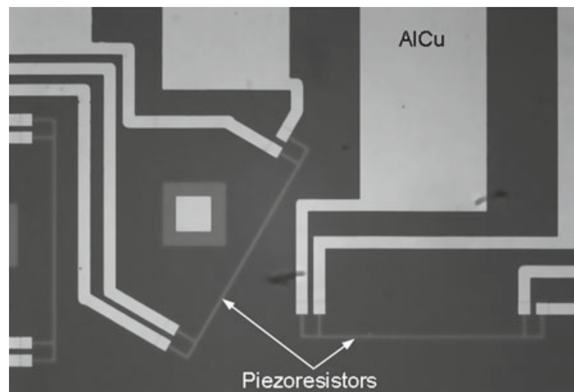


**Fig. 2.4** Microscope picture of 3 differently orientated poly-SiGe resistors in a typical sample used for piezoresistive measurements

is pure silane, whereas 10 % germane in hydrogen acts as the germanium gas source. 1 % diborane in hydrogen is used as the boron gas source. The silane/germane flow ratio equals 0.9 and the diborane flow is 40 sccm. For films deposited at such low temperature, *in situ* boron doping enhances the films crystallinity and reduces the strain gradient, as already mentioned in chapter 1. Rutherford Back Scattering (RBS) and Secondary Ion Mass Spectrometry (SIMS) analyses were used to determine the germanium and boron concentrations [25]. The values measured on similar samples are $3.6 \times 10^{21}$ at/cm$^{-3}$ for boron concentration and 76 % for Ge content.

The next two layers studied were CVD-deposited at 540 and 500 °C chuck temperature (∼500 and 460 °C wafer temperature), respectively, and 275 Torr in an Applied Materials (AMAT) Centura platform. A pure Si seedlayer was used for both films. 1 % germane in hydrogen has been used as the germanium gas source. The germane flow rate has been fixed to 975 sccm for all depositions, while the flow rate of the silicon gas source (pure silane) has been adjusted to yield a germanium concentration of 49 and 64 %, respectively, as determined by Rutherford Back Scattering (RBS). The films were doped through ion implantation of boron at 65 keV with dosages between $2 \times 10^{13}$ to $4 \times 10^{15}$ cm$^{-2}$. After implantation, the films were annealed for 30 min at 570 °C (for 64 % Ge) and 620 °C (for 49 % Ge) in a 10 % $H_2/N_2$ gas atmosphere. The boron concentrations were determined by SIMS (Fig. 2.5). Figure 2.6 shows Transmission Electron Microscopy (TEM) pictures of layer 3 (poly-$Si_{51}Ge_{49}$). V-shaped grains through the layer can be observed, with smaller isotropic grains at the oxide interface. Layer 2 (poly-$Si_{36}Ge_{64}$) exhibited a similar grain morphology.

The last of the considered layers is a CVD poly-SiGe layer with ∼77 % Ge deposited at a chuck (wafer) temperature of 460 (450 °C) in an Applied Materials (AMAT) PECVD CxZ chamber, mounted on an Applied Materials Centura Giga-Fill SACVD platform. At such low temperature, the incubation time needed to deposit an undoped (i.e, without in situ B-doping) CVD SiGe layer can be very high. For this reason, a 20 nm-thick PECVD SiGe seed layer is used. This PECVD layer is deposited at 5.4 Torr using silane (15 sccm) and 10 % germane in hydrogen (330 sccm)

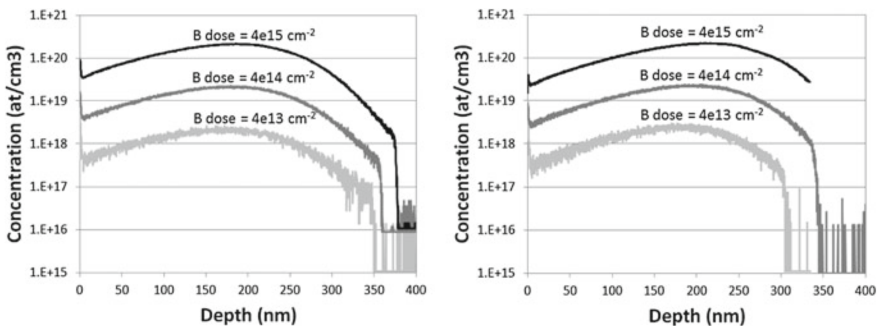


**Fig. 2.5** SIMS results for Poly-Si36Ge64 (*left*) and Poly-Si51Ge49 (*right*) layers with three different doping doses: $4 \times 10^{13}$, $4 \times 10^{14}$ and $4 \times 10^{15}$ cm$^{-2}$

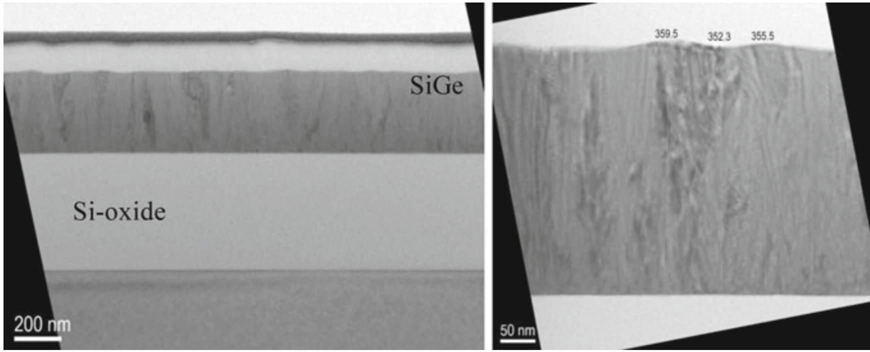


**Fig. 2.6** TEM pictures depicting the grain morphology of Poly-Si51Ge49 (layer 3 in Table 2.1). Columnar grains through the layer can be observed, with smaller grains at the *bottom* (interface with oxide)

as gas precursors. The 200 nm-thick CVD SiGe layer is then deposited on top at 4.3 Torr with a silane and germanium flows of 15 and 166 sccm, respectively. Both the PECVD and the CVD layers are deposited undoped. After deposition the films were boron implanted at 35 keV with dosages between $1 \times 10^{14}$ and $1 \times 10^{15}\,\text{cm}^{-2}$ and annealed at 455 °C. Three different annealing times were considered: 30 min, 1 and 2 h.

All the mentioned annealing steps were performed in a 10 % $H_2/N_2$ gas atmosphere. The annealing times mentioned above only account for the time the wafers are subjected to the corresponding temperature in the mentioned hydrogen-rich atmosphere. However, each annealing step is preceded by a warm-up and stabilization period of ∼30 min, and followed by a 30 min cool-down period, both of them in a $N_2$ atmosphere. Therefore, for each of the annealing operations mentioned in this chapter, and in general throughout this book, the wafers are kept at the target temperature for approximately 1h longer than the specified annealing time.

## 2.3 Measurement Setup

The samples used in the piezoresistive measurements are $80 \times 8\,\text{mm}^2$, with the differently orientated resistors placed in the centre region (Figs. 2.2 and 2.4). Such samples, whose length is much higher than their width, can be stressed in pure bending [26] in order to create a constant and uniform stress in the piezoresistors. The measurement setup used to evaluate the piezoresistive properties of the different poly-SiGe layers considered is illustrated in Fig. 2.7.

The samples are stressed in a tool called “Delaminator”, a four point bending fixture, which creates a pure bending condition. While bending the samples, the electrical resistance of the poly-SiGe piezoresistors is measured by a HP4156 pre-

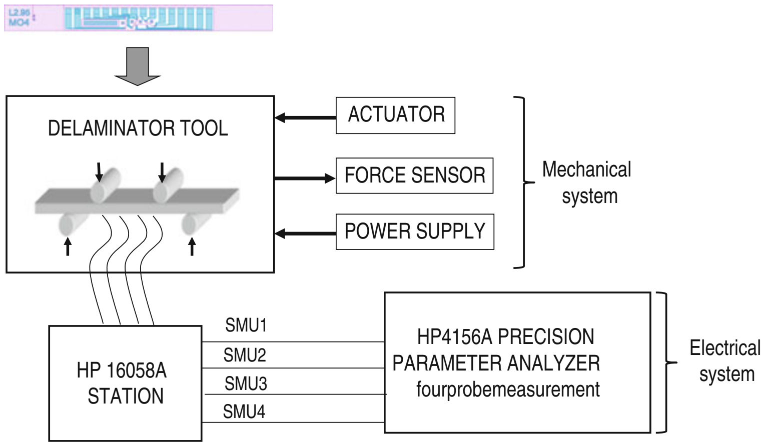


**Fig. 2.7** Schematic representation of the setup used for the piezoresistive measurements. While the sample is bended by the fours blades of the Delaminator tool, the electrical resistance is measured by the parameter analyzer. The SM1-4 are coaxial cables connecting the parameter analyzer and the sample wires through the HP 16058 A

cision parameter analyzer. Wires are bonded to the four pads of each piezoresistors, providing an electrical path to the resistor being measured. These wires are connected to the parameter analyzer through an HP 16058A station. The parameter analyzer provides a current sweep and at the same time measures the voltage drop across the resistors, according to the four probe method (Fig. 2.3). By measuring this voltage drop for different bending force values, the relative resistance change as a function of applied stress can be obtained.

In Fig. 2.8 pictures of a sample being stressed in the "Delaminator" can be observed. The sample is placed between the two arms of the tool, one is movable

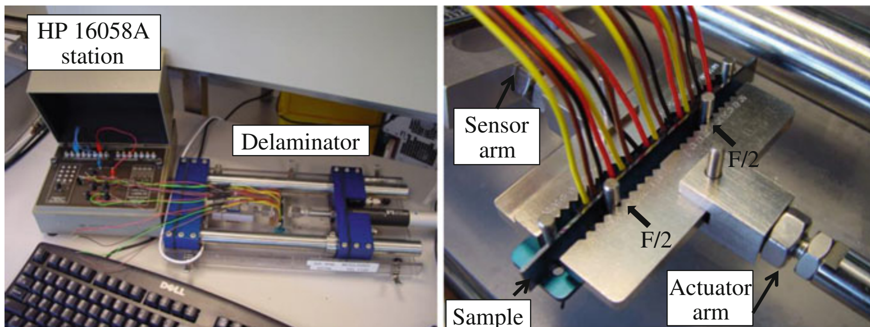


**Fig. 2.8** **a** Global view of the delaminator tool. The HP 16058A station acts as an "adapter" between the resistor wires and the four coaxial cables connecting the parameter analyzer. **b** Close-up of a sample stressed by the delaminator arms

while the other one is fixed. The moving part is connected to an actuator, and by controlling its displacement a bending force is applied to the sample. The fixed arm is connected to a sensor that measures the force exerted upon the sample. In order to emulate a four point bending fixture (Fig. 2.9), four blades are placed along the sample, two between the sample and the "actuator" arm and the other two on the "sensor" side. These four blades transform the exerted force in a uniform and unidirectional stress on top of the region in between the inner blades, where the piezoresistors are placed.

### 2.3.1 The Four Point Bending Method

As explained above, in this work the piezoresistivity of the poly-SiGe films is estimated by measuring the resistance variation ($\Delta R/R$) under a uniform and uniaxial stress provided by a four point bending fixture. Four point bending is often used in material analysis and has also been used for piezoresistive measurements [27]. The four point bending method is illustrated in Fig. 2.9, which depicts a rectangular sample of width $w$ and thickness $t$ being stressed by four blades. The two outer blades are fixed while the two inner blades exert a force F upon the sample. This applied force results in a uniform and unidirectional stress in the surface of the sample, between the two inner blades, given by [27]:

$$\sigma = \frac{3 \cdot F \cdot d}{w \cdot t^2} \tag{2.8}$$

where F is the applied force, d is the distance between inner and outer blades and $w$ and $t$ are sample width and thickness, respectively.

The samples used in this work are a composite of three layers (silicon, Si-oxide and SiGe) are shown in Fig. 2.10. Expression (2.8) describes the stress induced on the silicon surface ($y = t_1/2$ in Fig. 2.10), but what will be the stress on the poly-SiGe top layer? Based on Timoshenko's theory, a constant bending moment will stretch the composite beam, generating a stress along the x-axis in the ith layer ($\sigma_{xi}$) given by [26]:

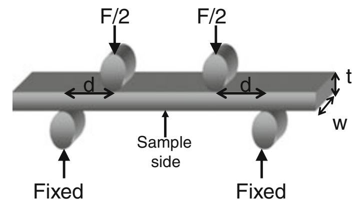


**Fig. 2.9** Sketch of a four point bending fixture. In the surface of the *rectangular* sample in the region between the two *upper* blades, the stress is constant and uniaxial

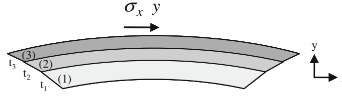


**Fig. 2.10** Composite three-layer beam under pure bending. Layers (1), (2) and (3) are Si, Si-oxide and SiGe, respectively. ti represents the thickness of the i-layer. The origin of the y-axis corresponds to the centre of the Si layer

$$\sigma_{xi} = \frac{ME_i}{\sum_{j=1}^{3} E_j I_j} \cdot y \tag{2.9}$$

where $M$ is the bending moment and $E_i$ and $I_i$ are the Young's modulus and the moment of inertia of the i-layer, respectively. In the samples fabricated in this work, $t_1 = 725\,\mu m$ (Si substrate), $t_2 = 500\,nm$ (S-oxide isolation layer) and $t_3 \leq 400\,nm$ (SiGe layer). Therefore we can consider $t_{2,3} << t_1$ and $I_{2,3} << I_1$. The stress σ on the SiGe layer surface ($y \approx t_1/2$) can thus be expressed by the formula [6]:

$$\sigma_{x3} \cong \frac{M}{I_1} \cdot \frac{E_3}{E_1} \left(\frac{t_1}{2}\right) = \frac{E_3}{E_1} \cdot \sigma_{x1}\big|_{y=\frac{t_1}{2}} \tag{2.10}$$

Finally, by substituting (2.8) in (2.10), the stress induced in the poly-SiGe piezoresistors when bending the samples in the four point bending fixture ("Delaminator" tool) is given by:

$$\sigma \cong \frac{E_3}{E_1} \cdot \frac{3 \cdot F \cdot d}{w \cdot t^2} \tag{2.11}$$

## *2.3.2 Calculation of the Piezoresistive Coefficients*

According to [28], the relative resistance variation of a polycrystalline piezoresistor subjected to uniform and unidirectional stress $\sigma$ and orientated at an angle $\varphi$ with respect to the stress direction is given by:

$$\frac{\Delta R}{R} = \sigma (\pi_l \cos^2 \varphi + \pi_t \sin^2 \varphi - \pi_{lt} \cos \varphi \sin \varphi) \tag{2.12}$$

where $R$ and $\Delta R$ are the zero-stress resistance and the resistance variation due to $\sigma$, respectively.

The piezoresistive coefficients of poly-SiGe can thus be determined from the measured relative resistance variation by applying equation (2.12). In this work we are mainly interested in the longitudinal ($\pi_l$) and transverse ($\pi_t$) piezoresistive coefficients. For this reason, in most cases only the horizontal ($\varphi = 0°$) and vertical ($\varphi = 90°$) resistors (see Figs. 2.2 and 2.4) are measured. The longitudinal piezore-

sistive coefficient can be obtained from the measured relative resistance variation of a horizontal resistor under a uniaxial stress σ parallel to the current flow:

$$\pi_l = \frac{1}{\sigma} \cdot \frac{\Delta R}{R}\bigg|_{\varphi=0} \tag{2.13}$$

In the same way the transverse piezoresistive coefficient can be calculated from the relative resistance variation of a vertical resistor subjected to the same uniaxial stress σ, which in this case is perpendicular to the current flow:

$$\pi_t = \frac{1}{\sigma} \cdot \frac{\Delta R}{R}\bigg|_{\varphi=90^\circ} \tag{2.14}$$

Both (2.13) and (2.14) can be derived from (2.11) by substituting $\varphi = 0^\circ$ and $\varphi = 90^\circ$, respectively. The value of the stress $\sigma$ induced in the piezoresistors when bending the samples in the four point bending fixture is given by (2.11). Finite element simulations (using COMSOL3.3 [29]) were performed to validate the theoretical stress (Fig. 2.11). A good agreement (within 4 %) between the simulated and the calculated stress values was obtained. For example, assuming a Young's modulus = 140 GPa for poly-SiGe [30], the simulated valued of stress in the poly-SiGe resistor corresponding to a bending force of 1 N is 8.62 MPa. The equivalent calculated value from (2.11) is 8.3 MPa.

## 2.4 Results and Discussion

### *2.4.1 Standard Poly-SiGe Layer and Comparison to Poly-Si*

This section reports on the electrical and piezoresistive properties of the CVD-deposited heavily-doped poy-SiGe used in imec's SiGe MEMS platform as the standard electrode layer (layer 1 in Table 2.1). This layer is deposited at a wafer

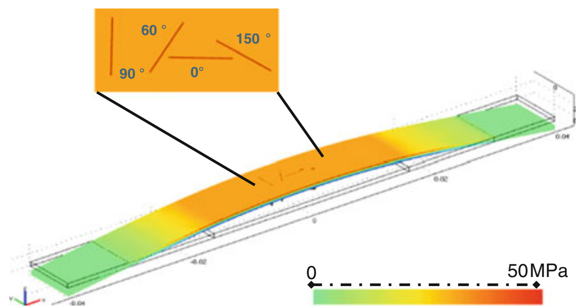


**Fig. 2.11** Stress simulation in COMSOL: global view of the deformed sample for an applied force F = 6 N. The thicknesses of the Si substrate, Si-oxide and poly-SiGe layers are 725 μm, 500 and 400 nm, respectively

temperature of 450 °C, a temperature compatible with MEMS integration on top of CMOS. To allow for a direct comparison between the electrical properties of poly-SiGe and poly-Si, *in situ* boron doped poly-Si layers were also deposited by low pressure CVD at 550 °C and 300 mTorr (in a vertical furnace, batchtool) with an estimated chemical doping concentration of $1 \times 10^{21}\,\text{cm}^{-3}$. The poly-Si layers, which had a thickness (determined using a Dektak profiler) of 378 ± 25 nm, were patterned following the same two-mask process used for the poly SiGe layers.

#### 2.4.1.1 Electrical Properties

The resistivity is measured in the temperature range of −10 to 200 °C by performing four point resistance measurements of resistors of different dimensions. The measured resistivities for poly-SiGe and poly-Si are plotted as a function of temperature in Fig. 2.12. As can be seen from this figure, the resistivity is more or less a linear function of temperature in the temperature interval −10 to 200 °C. Based on this observation, the TCR can be defined in the following way [31]:

$$TCR = \frac{\rho_2 - \rho_1}{\rho_1 \cdot (T_2 - T_1)} \tag{2.15}$$

where $\rho_2$ and $\rho_1$ represent the resistivity at temperature $T_2$ and $T_1$, respectively. Equation (2.15) was used to calculate the TCR for all samples, with $T_1 = -10\,°C$ and $T_2 = 200\,°C$. The obtained results for resistivity and TCR of poly-SiGe and poly-Si (Table 2.2) are compatible with previously reported data for heavily doped films [31–34]. The poly SiGe film showed very good electrical properties with a resistivity of only 0.86 mΩ·cm and a low TCR of 270 ppm/°C. The resistivity of poly-SiGe was lower than that of poly-Si (2.6 mΩ·cm), what was predictable as,

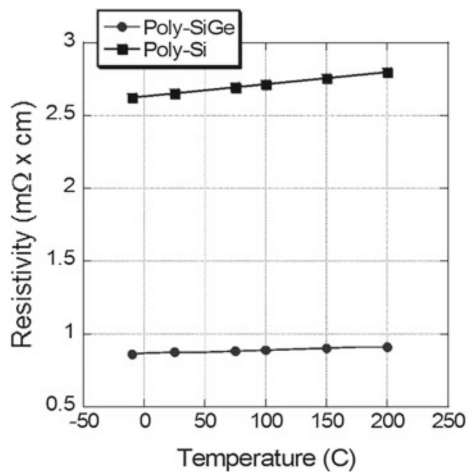


**Fig. 2.12** Resistivity as a function of temperature for poly Si24Ge76 and poly Si

**Table 2.2** Measured electrical properties of poly SiGe and poly Si

| | Poly-$Si_{24}$ $Ge_{76}$ | Poly-Si |
|---|---|---|
| Resistivity (mΩ·cm) | 0.86 (±4 %) | 2.6 (±8 %) |
| TCR (°$C^{-1}$) | $2.7\times10^{-4}$ (±4 %) | $3\times10^{-4}$ (±3 %) |

according to [32], in boron doped films the resistance decreases with increased Ge content due to both an increased effective carrier concentration and a higher Hall mobility. As expected for heavily-doped polycrystalline films, the resistivity of both poly-SiGe and poly-Si increases with temperature leading to a positive TCR. This is because, as stated in [34], at high doping levels the barrier height is small and the effect of grain boundaries on electrical conduction is negligible compared to the resistivity of the grains. Within the grains, the current transport is by carrier drift and the resistivity of the grain region behaves essentially like that of the single crystal material [7]. Therefore, as the mobility decreases with temperature (due to the thermal vibrations of the atoms), the resistivity of the grain region increases with temperature, translating into a positive TCR. We can observe that poly-SiGe (Table 2.2) exhibits a lower TCR than poly-Si [31, 34] at similar doping levels; this property can be very useful for the design of some devices as for example pressure sensors with piezoresistive sensing elements.

#### 2.4.1.2 Piezoresistivity

The relative resistance variation of several poly-SiGe and poly-Si resistors with different orientations ($\varphi = 0$, 60, 90 and 150 degrees) has been measured at room temperature by the four point bending method described in Sect. 2.3. The force applied in the "Delaminator" tool to bend the samples was varied from 0 to 6 N. In Fig. 2.13 the measured relative resistance variation ($\Delta R/R$) versus applied stress is plotted. The stress induced in the resistors due to the force applied in the "Delaminator" was determined by finite element simulations using an assumed Young's modulus $E = 140$ GPa [30] and $E = 163$ GPa for poly-SiGe and poly-Si, respectively [35].

By substituting the measured relative resistance variation and the simulated value of the stress in (2.12), the piezoresistive coefficients can be found. Results show $\pi_l = 2 \times 10^{-11}$, $\pi_t = -0.7 \times 10^{-11}$ and $\pi_{lt} = 0.8 \times 10^{-11}$ [$Pa^{-1}$] for poly SiGe and $\pi_l = 2.6 \times 10^{-11}$, $\pi_t = -1.11 \times 10^{-11}$ and $\pi_{lt} = -0.7 \times 10^{-11}$ [$Pa^{-1}$] for poly Si. The maximum variation in the piezoresistive coefficients from sample to sample is ±20 % (8 samples measured) in the case of poly-SiGe and ±13.3 % for poly-Si (7 samples measured). These results translate into a longitudinal gauge factor of 2.8 (4.2) for poly SiGe (poly Si). The low gauge factors found both for poly-SiGe and poly-Si are not surprising taking into account the high doping concentrations of the studied films. At such high doping levels, the semiconductors are said to be degenerated and start to act like metals, with the consequent limited piezoresistive effect. The degradation in gauge factor with increasing doping concentration both for poly-Si and c-Si is well known [1, 17, 21].

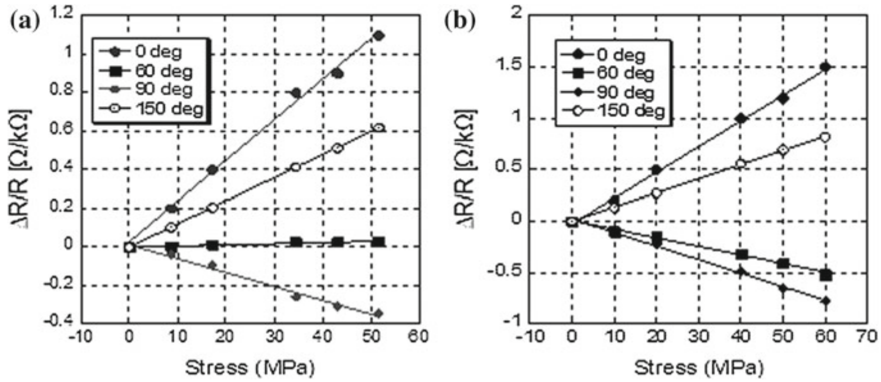


**Fig. 2.13** Relative resistance variation vs. applied stress for (**a**) poly-SiGe and (**b**) poly-Si resistors with 4 different orientations (in degrees)

## *2.4.2 Optimization of Boron Doped Poly-SiGe Layers for Piezoresistive Sensing Applications*

The gauge factor found in the previous section for the standard imec's poly-SiGe electrode layer is too low for this layer to be used as sensing layer in piezoresistive sensor applications. An optimization of the piezoresistive properties of poly-SiGe is therefore needed. Assuming that the piezoresistivity of poly-SiGe will exhibit similar modulation with doping concentration as that of poly-Si, we can expect to improve the gauge factor by decreasing the doping concentration. This section reports the electrical and piezoresistive properties of boron-implanted poly-SiGe layers with a B-dose varying from $2 \times 10^{13}$ to $4 \times 10^{15}\,\mathrm{cm}^{-2}$. Two different germanium contents (Ge $=$ 64 and 49 %) are considered. The processing conditions of these two layers (layers 2 and 3 in Table 2.1) were already described in Sect. 2.2.2.

### 2.4.2.1 Electrical Properties

The resistivity has been measured on blanket wafers using a four-point probe on 49 different locations on the wafer. From Fig. 2.14 we can observe that the resistivity of poly-SiGe reduces with increasing boron concentration and Ge content. In boron doped poly-SiGe films, the decreased resistance with increasing Ge fraction is due both to the increased effective carrier concentration and the higher mobility [32, 36].

To study the temperature coefficient of resistance (TCR) of the layers, four point resistance measurements of patterned structures with different lengths (from 0.5 to 3 mm) and widths (from 25 to 150 μm) have been performed in the temperature range of 25–150 °C. The relative resistance change with temperature for both poly-$Si_{36}Ge_{64}$ and poly-$Si_{51}Ge_{49}$ is shown in Fig. 2.15 with the doping concentration as the varying parameter. The resistivity of a polycrystalline material is determined by the

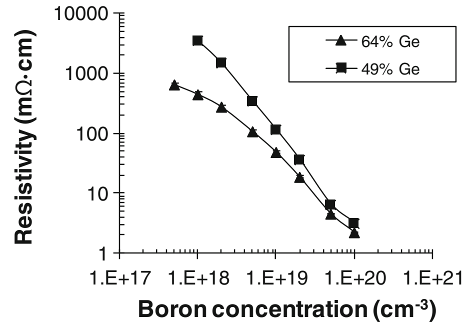


**Fig. 2.14** Dependence of the resistivity on doping dose for poly-Si36Ge64 and poly-Si51Ge49

resistance within the grains and the "barrier" resistivity across the grain boundaries, which is controlled by a thermionic emission process [37]. At low and moderate doping levels the effect of the grain boundaries is dominant, leading to a non-linear (as expected from the thermionic emission model) and negative TCR: at higher temperatures more carriers can overcome the boundary barriers and the grain boundary resistance decreases with temperature rise. At higher doping levels the barrier height is small and the effect of the grain boundaries is negligible compared to the resistivity of the grains. Within the grains the current transport is by carrier drift, resulting in a positive TCR [7]: as the mobility decreases with temperature (thermal scattering), the resistivity of the grain region increases.

In Fig. 2.16 we observe that the temperature dependence of poly-SiGe increases with decreasing doping concentration, being practically constant for doping levels above $2 \times 10^{15}\,\mathrm{cm}^{-2}$. The TCR is found to vary from strongly negative values for low doping to slightly positive values for high doping, with a cross-over point with TCR$\sim$0 for doping doses around $1 \times 10^{15}\,\mathrm{cm}^{-2}$. In conclusion, similar as for

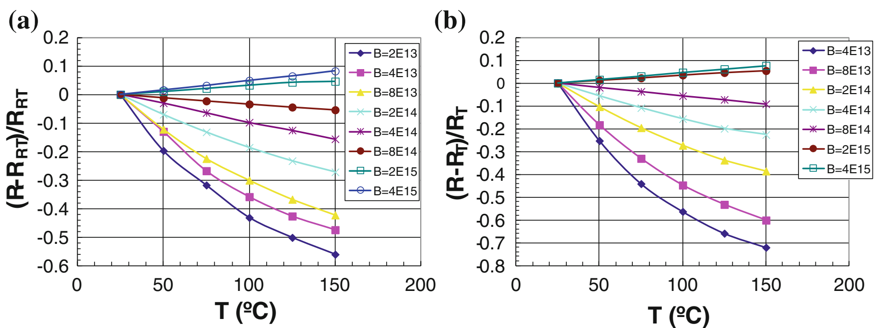


**Fig. 2.15** Dependence of resistivity on temperature for $(4 \times 10^{1}3)$ poly-Si36Ge64 and $(4 \times 10^{1}3)$ poly-Si51Ge49 for different boron doses. RT represents the resistance at room temperature

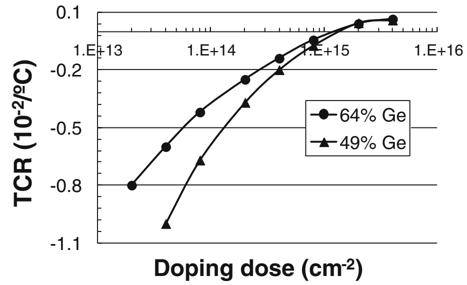


**Fig. 2.16** Dependence of TCR (calculated from the slope at room temperature) on doping dose for poly-Si36Ge64 and poly-Si51Ge49

poly-Si [7, 8, 17, 38], the TCR of poly-SiGe modulates with doping concentration, making it possible to obtain a positive, negative or even zero TCR depending on the specifications of the considered application.

#### 2.4.2.2 Piezoresistivity

The samples were stressed in the four point bending fixture, and the relative resistance variation (ΔR/R) of horizontal ($\varphi = 0°$) and vertical ($\varphi = 90°$) resistors were measured by means of the parameter analyzer, as explained in Sect. 2.3. By substituting in expressions (2.13) and (2.14) the measured ΔR/R and the simulated value of stress σ, the longitudinal and transverse piezoresistive coefficients were calculated. The Young's modulus (obtained by nanoindentation) used in the stress simulations are 108.2 GPa for poly-$Si_{36}Ge_{64}$ and 107.2 GPa for poly-$Si_{51}Ge_{49}$ (see Table 2.1). The obtained coefficients for the different layers are listed in Table 2.3. Figure 2.17 plots the obtained longitudinal and transverse gauge factors as a function of the doping dose. The longitudinal gauge factor of poly-SiGe exhibits a similar behavior as that of poly-Si [17], tailing off for high and low doping levels and reaching a maximum for a doping dose of around $4 \times 10^{14}$ cm$^{-2}$ ($2 \times 10^{14}$ cm$^{-2}$) for the 64 % Ge (49 % Ge) layer. The modulation of the longitudinal gauge factor with doping concentration can be explained as follows. At low doping levels, the piezoresistivity of the grain boundaries, which is lower than the grain piezoresistivity, is dominant. As the doping concentration increases, the effect of grain piezoresistivity gains ground, and the overall piezoresistivity increases. At very high doping concentrations the layers start exhibiting metallic behavior, with the consequent decrease in gauge factor [1].

It is also interesting to point out the sign change in the transverse piezoresistive coefficients of both layers. In [11] the sign change in the transverse gauge factor of p-type polysilicon was explained as follows. As already discussed in Sect. 2.1.1.2, the positive sign for the longitudinal gauge factor arises from the hole transfer from the light- to the heavy-hole band. The negative sign for the transverse gauge factor, on the other hand, is due to the mass change effect. Following [39], the mass change effect mainly concerns carriers that have weak energy. According to this, for low doping concentration, as the potential barrier is high and only carriers that

**Table 2.3** Obtained longitudinal ($\pi_1$) and transverse ($\pi_t$) piezoresistive coefficients (in $Pa^{-1}$)

| B ($cm^{-2}$) | Poly-$Si_{51}Ge_{49}$ | | PolySi$_{36}$Ge$_{64}$ | |
|---|---|---|---|---|
| | $\pi_1(10^{-11})$ | $\pi_t(10^{-11})$ | $\pi_1(10^{-11})$ | $\pi_t(10^{-11})$ |
| $4 \times 10^{13}$ | 13.7 | 6.28 | 11.96 | 0.95 |
| $2 \times 10^{14}$ | 17.4 | 2.7 | 16.85 | 2.04 |
| $4 \times 10^{14}$ | 12.7 | 1 | 18.6 | 1.28 |
| $8 \times 10^{14}$ | 7.85 | 0.43 | 11.7 | −0.58 |
| $4 \times 10^{15}$ | 5.42 | −0.43 | 5.43 | −0.68 |

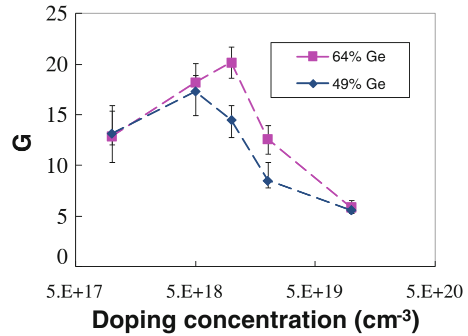


**Fig. 2.17** Longitudinal Gauge factor as a function of doping concentration

have enough energy to overcome the high potential barrier take place in electrical conduction, the mass change phenomena does not play a role. Therefore, for low doping concentration, the transverse piezoresistivity can be interpreted only in terms of hole transfer, similar as the longitudinal case. This explains the positive sign of the transverse gauge factor for low doping concentrations. When the doping concentration increases, the potential barrier height decreases and more carriers take part in the electrical conduction, notably those having weak energy. Therefore the mass change effect gains importance and $\pi_t$ becomes negative, as in silicon (see Sect. 2.1.1.2).

Poly-$Si_{36}Ge_{64}$ showed slightly better piezoresistive properties than poly-$Si_{51}Ge_{49}$, although at high doping levels the piezoresistivity of poly-SiGe seems to be practically independent on Ge content. The higher gauge factor for the films with 64 % Ge might be explained by the different grain size. As stated in [40] the average grain size is larger in films with higher Ge content and according to [17, 41], the gauge factor of a polycrystalline material is expected to increase with grain size. The average grain size of both poly-$Si_{36}Ge_{64}$ and poly-$Si_{51}Ge_{49}$ layers was estimated from X-ray diffraction (XRD) profile analysis, by measuring the half bandwidth of the XRD peak [42]. The obtained average grain size for a poly-$Si_{36}Ge_{64}$layer with a boron concentration of $\sim 1 \times 10^{19}$ $cm^{-3}$ was 50.2 nm. A similarly doped poly-$Si_{51}Ge_{49}$layer exhibited an average grain size of 39.5 nm, approximately 21 % smaller than for the poly-$Si_{36}Ge_{64}$ layer.

### 2.4.3 Piezoresistivity and Electrical Properties of Poly-SiGe Deposited at CMOS-Compatible Temperatures

Although the results obtained in the previous section were very promising, the processing temperatures used during the deposition and annealing of the studied layers were too high (above 500 °C) to allow for the monolithic integration of MEMS above CMOS. In this section, a new CVD poly-SiGe (Ge∼77 %) layer deposited at CMOS-compatible temperatures (i.e. 450 °C) is characterized (layer 4 in Table 2.1). The 200 nm-thick poly-SiGe layers are deposited undoped and are then boron-implanted with a B-concentration varying from $5 \times 10^{18}$ to $5 \times 10^{19}$ cm$^{-3}$. After implantation the layers were annealed at 455 °C.

#### 2.4.3.1 Electrical Properties

The resistivity has been measured on blanket wafers with different boron concentrations and annealed at 455 °C for 1 h using a four-point probe on 49 different locations on the wafer. To study the temperature coefficient of resistance (TCR) of the layers, four point resistance measurements have been performed in the temperature range of 25–150 °C. From Fig. 2.18 we observe that both the resistivity and the temperature coefficient of resistance (TCR) of this new layer show similar behavior as those of our previous poly-SiGe layers (Sect. 2.4.2).

#### 2.4.3.2 Piezoresistivity

The piezoresistivity is estimated from the resistance variation when stressing the films in the four point bending fixture, as described in previous Sections. For this experiment, only layers doped with B∼$1 \times 10^{19}$ cm$^{-3}$ were measured, since this doping concentration resulted in the highest gauge factor in our previous poly-$Si_{36}Ge_{64}$ layer (see Fig. 2.17). In order to study the effect of annealing time on the piezoresistors, three different annealing times were considered: 30 min, 1 and 2 h. From Fig. 2.19 we can see that the optimum annealing time for a maximum gauge factor is 1 h.

For an annealing time of 30 min the measured gauge factor is ∼13, 40 % lower than the gauge factor found in the previous section for the poly-$Si_{36}Ge_{64}$ layer with the same boron concentration and annealing time. One possible explanation for this degradation in piezoresistivity might be the expected smaller grain size due to the lower deposition and annealing temperatures of the poly-SiGe piezoresistive layer used here. This layer was deposited (and annealed) at a temperature 50 °C (120 °C) lower than the poly-$Si_{36}Ge_{64}$ film described in the previous section. Based on X-ray diffraction (XRD) profile analysis, the grain size for this new poly-SiGe layer processed at CMOS-compatible temperatures is ∼22 % smaller than the grain size

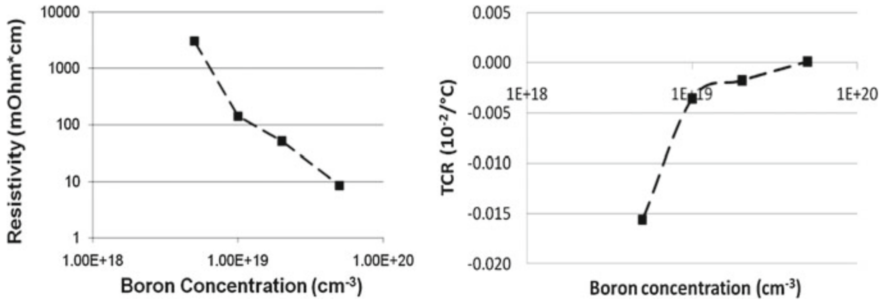


**Fig. 2.18** Dependence of resistivity (*left*) and TCR (*right*) on doping concentration. The TCR has been calculated from the slope at room temperature

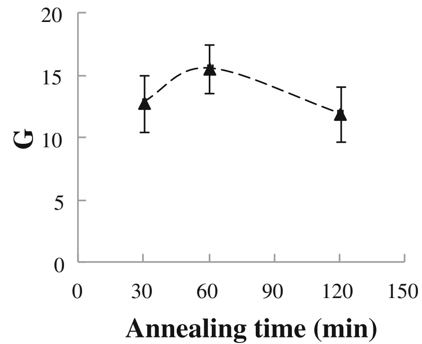


**Fig. 2.19** Effect of annealing time (for an annealing temperature of 455 °C) in the longitudinal gauge factor of CVD poly-Si23Ge77 layers deposited at 460 °C. The number of samples measured are 5, 2 and 3, respectively

found for the poly-$Si_{36}Ge_{64}$film (Sect. 2.4.2). As stated above, the gauge factor of a polycrystalline material is expected to increase with grain size [17, 41].

## 2.5 Summary and Conclusions

In this chapter, several poly-SiGe layers, with different processing conditions, Ge content and boron concentration, have been characterized as piezoresistive materials. The properties studied include piezoresistivity, resistivity, and temperature coefficient of resistance (TCR). The TCR of the layers was evaluated by measuring the films resistivity at different temperatures. The piezoresistivity is estimated by measuring the resistance variation when a uniform and uniaxial stress provided by a four point bending fixture is applied to the films.

In total four different layers were considered. First, a heavily doped CVD poly-$Si_{24}Ge_{76}$, deposited at 460 °C (compatible with above-CMOS integration) was characterized. The layer proved to have very good electrical properties, with a resistivity lower than 1 mΩ·cm and a TCR of only $2.7 \times 10^{-4}\,°C^{-1}$. However, the gauge factor

(G = 2.8), although comparable to the gauge factor found for a similarly highly doped poly-Si layer (G = 4.2), is low for typical piezoresistive applications.

In an attempt to optimize the piezoresistive properties of poly-SiGe, two layers with different Ge contents (64 and 49 %, respectively) were studied next. The layers were boron-implanted with concentrations between $5 \times 10^{17}$ and $1 \times 10^{20}\,\mathrm{cm}^{-3}$. Similar as for poly-Si, the gauge factor of poly-SiGe is found to tail off for high and low doping levels, reaching a maximum at $B{\sim}1\times10^{19}\,\mathrm{cm}^{-3}$. The 64 % Ge layer exhibited a higher gauge factor than the 49 % Ge layers, which might be explained by the different grain size. The maximum measured gauge factor was ∼20, corresponding to a poly-$Si_{36}Ge_{64}$ layer with $B{\sim}1\times10^{19}\,\mathrm{cm}^{-3}$. This gauge factor is in the range of reported maximum values for poly-Si [17, 22, 23]. Results also show that with proper tuning of the boron concentration, a TCR around 0, which is ideal for piezoresistive sensor applications, is achievable.

Despite the promising results obtained for this poly-$Si_{36}Ge_{64}$ film, the processing temperatures used during the deposition and annealing of this layer were too high (above 500 °C) to allow for the monolithic integration of MEMS above CMOS. For this reason, a new CVD poly-SiGe layer (Ge∼77 %), deposited and annealed at temperatures $\leq$ 460 °C, was developed and characterized. This new layer exhibited a maximum gauge factor of ∼15, corresponding to a $B{\sim}1\times10^{19}\,\mathrm{cm}^{-3}$ and an annealing time of 1 h. The lower piezoresistive sensitivity of this layer as compared to the two previous ones might be explained by the smaller grain size due to the lower deposition and annealing temperatures.

The results obtained in this work prove the potential of using poly-SiGe as a sensing layer for piezoresistive sensors. Despite the somewhat lower piezoresistive sensitivity as compared to poly-Si, we believe that the possibility to post-process on top of CMOS still makes poly-SiGe a very interesting material for MEMS piezoresistive sensors as monolithic integration leads to a higher signal/noise ratio which might offset the slightly smaller gauge factor.

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# Chapter 3
# Design of a Poly-SiGe Piezoresistive Pressure Sensor

In this chapter, an extensive analysis, based on FE (Finite Element) simulations, on the structural design and optimisation of poly-SiGe based piezoresistive pressure sensors is presented. The considered pressure sensors consist of a deformable poly-SiGe membrane, fully clamped at its edges, and four poly-SiGe piezoresistors placed on top following a Wheatstone bridge configuration. Finite element simulations are used together with the experimentally obtained piezoresistive coefficients for poly-SiGe (Chap. 2) to optimize the sensor design parameters for enhanced sensitivity and linearity. The design parameters include the membrane area and shape and the location, shape and dimensions of the piezoresistors. The chapter begins by introducing the working principle of piezoresistive pressure sensors and their governing equations. The most important performance parameters for such sensors are also listed. The impact of the aforementioned design parameters on sensor performance is then evaluated, paying special attention to sensor sensitivity and linearity. Finally, two membrane shapes (square and rectangular), four membrane areas ($200 \times 200$, $250 \times 250$, $300 \times 300$ and $350 \times 175\ \mu m^2$) and six different piezoresistor designs are included in the layout (see Appendix A).

## 3.1 A Piezoresistive Pressure Sensor: Definition and Important Performance Parameters

### *3.1.1 Definition*

The piezoresistive pressure sensor proposed in this work consists of a thin poly-SiGe membrane with four poly-SiGe piezoresistors placed on top, following a Wheatstone bridge configuration [1] (see Fig. 3.1). A basic Wheatstone bridge consists of four resistors connected in a loop. An input voltage ($V_{bias}$) is applied across two junctions that are separated by two resistors. The voltage drop across the other two junctions forms the output. One or more resistors in the loop may be sensing resistors, while the

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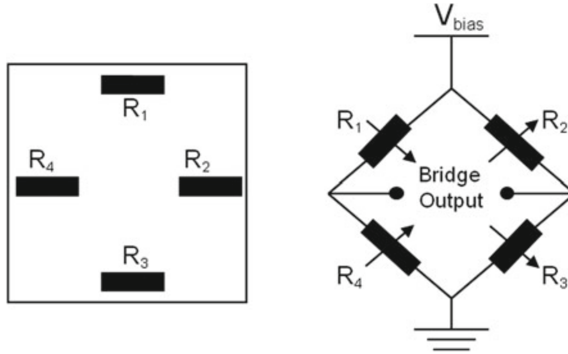


**Fig. 3.1** Four piezoresistors on a square membrane and Wheatstone bridge configuration of the four piezoresistors

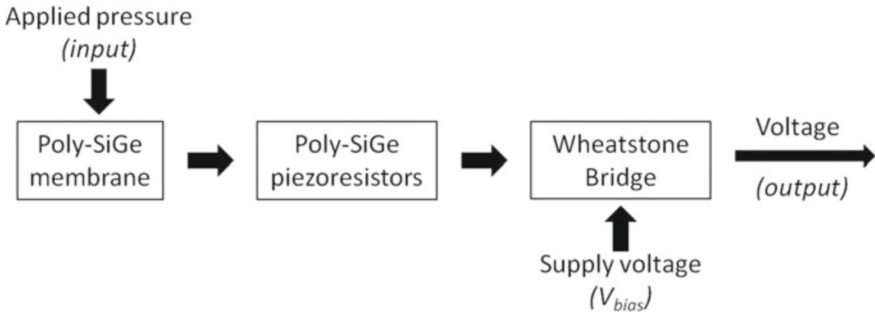


**Fig. 3.2** Working principle of the piezoresistive pressure sensor considered in this work

other resistors can be made insensitive to strains by being located in regions where the mechanical strain is zero, such as on rigid substrates. In this work, the four resistors in the Wheatstone bridge are sensing resistors, placed on the deformable diaphragm. The working principle of a piezoresistive pressure sensor is schematically illustrated in the block diagram in Fig. 3.2.

If we assume that the four piezoresistors in the Wheatstone bridge are ideally balanced ($R_3/R_4 = R_2/R_1$), then the bridge output voltage is zero when no pressure is applied on the membrane. When a pressure is applied, the membrane of the sensor will deform and induce bending stresses in the piezoresistors, which will translate into a variation in the resistance due to the piezoresistive effect. There is a contribution to the resistance change from stresses that are longitudinal ($\sigma_l$) and transverse ($\sigma_t$) with respect to the current flow. The piezoresistive coefficients relate the fractional change in resistance of the piezoresistors to the applied stress, according to the formula [2, 3]:

$$\frac{\Delta R}{R} = \pi_l \cdot \sigma_l + \pi_t \cdot \sigma_t \tag{3.1}$$

where $\pi_l$ and $\pi_t$ are the longitudinal and transverse piezoresistive coefficients and $\sigma_l$ and $\sigma_t$ represent the longitudinal and transverse stress components, respectively. As the membrane deflects, the piezoresistors are subjected to both longitudinal and transverse strains at the same time, though one of them will play a clearly dominating role. In Fig. 3.1 we can identify two longitudinal piezoresistors ($R_1$ and $R_3$) and two transverse piezoresistors ($R_2$ and $R_4$). For the longitudinal piezoresistors, the dominant stress component is parallel to the current flow; for the transverse piezoresistors, on the other hand, the main stress component is perpendicular to the current flow. It was shown in Chap. 2 that the transverse and longitudinal piezoresistive coefficients of poly-SiGe are different to each other in magnitude (and even opposite in sign, depending on the doping concentration). Due to the two different piezoresistive coefficients, together with the two different orientations of the piezoresistors, the resistance variation of the longitudinal resistors will be different from that of the transverse resistors when the sensor membrane is subjected to pressure. This unbalance created in the Wheatstone bridge will result in an electrical output $V_0$ given by (for $\Delta R << R$) [1, 4]:

$$\frac{V_0}{V_{\text{bias}}} \approx \frac{r}{(1+r)^2} \cdot \left( \frac{\Delta R_1}{R_1} - \frac{\Delta R_2}{R_2} + \frac{\Delta R_3}{R_3} - \frac{\Delta R_4}{R_4} \right) \tag{3.2}$$

where $r = R_1/R_2 = R_3/R_4$. It is easy to note that expression (3.2) has a maximum for $r = 1$. For this reason, in the pressure sensors considered in this work, the four piezoresistors are designed to have the same zero-stress resistance value ($R_1 = R_2 = R_3 = R_4 = R$). Also, due to symmetry, the resistance variation of the two longitudinal piezoresistors will be equal in magnitude to each other ($\Delta R_1 = \Delta R_3 = \Delta R_l$), the same as for the two transverse piezoresistors ($\Delta R_2 = \Delta R_4 = \Delta R_t$). Expression (3.2) might be rewritten as:

$$\frac{V_0}{V_{\text{bias}}} \approx \frac{1}{2} \cdot \left( \frac{\Delta R_l}{R} - \frac{\Delta R_t}{R} \right) \tag{3.3}$$

### *3.1.2 Important Parameters*

The most important parameters to evaluate the performance of a pressure sensor are the following:

- *Sensitivity*. The pressure sensitivity (S) is defined as the relative change of output voltage ($\Delta V_{out}/V_{\text{bias}}$) per unit of applied pressure ($\Delta P$) [5].

$$S = \frac{\Delta V_{out}}{V_{\text{bias}}} \cdot \frac{1}{\Delta P} \tag{3.4}$$

  where $V_{\text{bias}}$ is the bridge-input voltage. In this work the sensitivity is expressed in mV/V/Bar. From expression (3.2) we can observe that the output voltage, and

therefore the pressure sensor sensitivity, depends on the relative resistance variation of the four piezoresistors. According to expression (3.1), the relative resistance variation will depend on the gauge factor of the poly-SiGe piezoresistors and on the induced stress by the bending of the sensor membrane. Thus, to increase the sensitivity of the sensor, one option is to improve the gauge factor of the poly-SiGe piezoresistors (by optimizing the boron concentration, germanium content or annealing temperature and time, as seen in Chap. 2). Another possibility would be to increase the induced bending stresses, for example by reducing the membrane thickness and/or increasing the membrane area. As it will be seen later in this chapter, also the membrane shape and the piezoresistors shape and placement can affect the sensor sensitivity.

- *Offset voltage* ($V_{off}$). The output voltage of the pressure sensor measured at room temperature with full bias voltage and without any pressure being applied is called the offset voltage. Ideally, the offset voltage should be zero. There are mainly three factors causing a $V_{off} \neq 0$. The first one is the residual stress on the sensor membrane and the piezoresistors. The second one is, for non vacuum-sealed sensors, the residual pressure inside the cavity. And the third one, which is the main reason, is the mismatch, due to process variations, in the resistance values of the four piezoresistors. This variability in the four resistors leads to an unbalanced Wheatstone bridge, causing the sensor output to be different from zero even when no pressure is applied.
- *Full-scale span (FSS)*. FSS is the difference between the output voltage measured with maximum input stimulus ($P_{max}$) and the lowest input stimulus ($P_{min}$) (see Fig. 3.3). The difference between the maximum and minimum readable pressure ($P_{max} - P_{min}$) is known as Full Scale (FS).
In commercial applications, $P_{max}$ is typically defined as the maximum peak pressure level that can be applied while keeping an optimum sensor response, for example in terms of linearity. In this work, however, $P_{max}$ will be defined as the maximum pressure that the sensor membrane can withstand without breaking (due to the fracture strength of the membrane material) or collapsing to the bottom (due to the limited gap below the membrane). On the other hand, the minimum detectable pressure ($P_{min}$) is determined by the noise of the sensor [6]. However, in this work, since the noise of the poly-SiGe piezoresistors is unknown, $P_{min}$ in this chapter is considered to be 0 and, therefore, the output voltage at a pressure equal to $P_{min}$ is the offset voltage. With this, the FSS can be mathematically expressed as:

$$FSS = V_0\left(P_{max}\right) - V_{off} \tag{3.5}$$

- *Nonlinearity*. The nonlinearity (NL) of a transducer can be defined as the maximum deviation of the calibration curve (output vs. input) from specified best fit straight line [5, 7]. Referring to the real output voltage ($V_0$) versus applied pressure (P), and the idealized linear response (shown in Fig. 3.3), the nonlinearity $NL_i$ of a piezoresistive pressure sensor at a specific pressure $P_i$ is defined as:

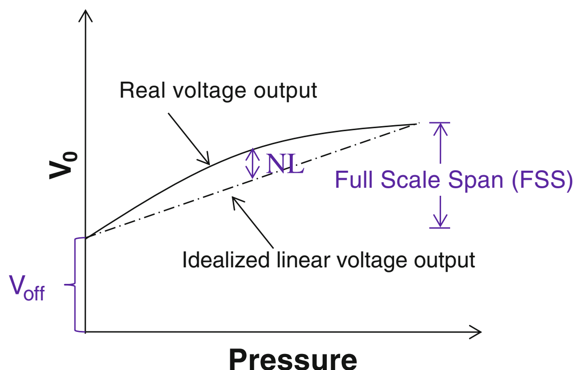


**Fig. 3.3** Output voltage ($V_0$) versus pressure, and the corresponding end-point straight line. Some of the most important parameters to evaluate a pressure sensor performance are included in the figure

$$NL_i = \frac{V_0'(P_i) - \frac{P_i}{P_{max}} V_0'(P_{max})}{V_0'(P_{max})} \times 100\% \tag{3.6}$$

where $V_0'(P_i) = V_0(P_i) - V_{off}$ and $V_0'(P_{max}) = V_0(P_{max}) - V_{off}$ are the output voltages (corrected with respect to offset voltage) at a pressure $P_i$ and $P_{max}$, respectively. The nonlinearity of the pressure sensor is the maximum value of NL. In expression (3.5) and Fig. 3.3, the idealized linear response is defined as the "end-point straight line". It is also possible to define the sensor nonlinearity with respect to a "best-fit straight line", obtained, for example, by the least squares method. Some manufacturers prefer the "best-fit" method as it gives better-looking data (lower nonlinearity). In this work, however, the end-point straight line will be used as it is the most straightforward, convenient and widely used method.

The nonlinearity of a full Wheatstone bridge operated with constant voltage supply has three main sources:

– *Structural nonlinearity*. the nonlinear dependence of the bending stresses with the applied pressure. According to the small deflections theory, the deflection of a clamped diaphragm is linear with pressure. However, if the membrane deflection is not small compared to its thickness (for deflections bigger than ~20 % of the membrane thickness), the neutral plane of the diaphragm will stretch like a balloon [5, 8]. Due to this balloon effect, the diaphragm is subjected to an in-plane stress component in addition to the stress caused by the bending of the diaphragm, and its load-deflection behavior will no longer be linear but it will include a third-order term [9, 10].
– *Piezoresistive nonlinearity*. For high values of mechanical stresses, the relation between stress and resistivity change is no longer linear, but instead second-order and third-order effects have to be taken into account [11–13]. However, a detailed study of the poly-SiGe piezoresistive nonlinearity was not performed; for this reasons this source of nonlinearity was not considered during the design of the sensors.

– *Bridge nonlinearity*. Another source of nonlinearity with Wheatstone bridges is the intrinsic nonlinearity of the equations [1, 14]. The above linear equation (3.2) is an approximation only valid if used close to the balanced bridge conditions ($R_3/R_4 = R_2/R_1$) or for small (infinitesimal) resistance changes (condition $\Delta R << R$ valid). Unbalance between the sensitivities of the different resistances which constitute the bridge will also contribute to this nonlinearity [8].

In the following discussion, only the structural nonlinearity will be considered. This is expected to be the largest source of nonlinearity, especially for very sensitive piezoresistive pressure sensors. Sensitivity can be increased using a greater $a/h$ ratio (where $a$ is the length of the membrane while $h$ represents its thickness). However, by increasing the $a/h$ ratio, the nonlinearity error will also increase, and at a much faster rate [7]. There is therefore a tradeoff between sensitivity and linearity. Several structures, based on a local stiffening of the membrane have been reported in order to improve the linearity minimizing the sensitivity loss [7]. However, for simplicity, only flat membranes are considered in this work.

- *Temperature coefficient of sensitivity (TCS)*. It measures the relative change in sensor sensitivity as the temperature is varied from the reference working temperature to any other temperature in the specified working range. It is usually expressed in (ppm/°C). It can be calculated using the expression [15]:

$$TCS = \frac{S(T) - S(T_0)}{S(T_o)} \cdot \frac{1}{\Delta T} \tag{3.7}$$

where $T$ is the final temperature, $T_0$ is the reference temperature and $\Delta T$ represents the difference between $T$ and $T_0$. In this work, room temperature is considered as reference temperature. There are two main sources for the variation of sensitivity with temperature:

– The variation of the piezoresistive coefficients with temperature [16, 17]. The sensitivity of a piezoresistive pressure sensor depends on the resistance variation of the piezoresistors with stress, which, in turn, depends on the piezoresistive coefficients (see expressions (3.1, 3.2 and 3.3)). The piezoresistive coefficients $\pi_l$ and $\pi_t$ are a function of temperature. In general, the piezoresistive coefficients decrease with temperature. For poly-Si, the temperature coefficient of piezoresistivity (TC$\pi$) is $\sim -0.1$ % [16]. For poly-SiGe, TC$\pi$ is unknown.
– The thermally-induced stresses due to the different coefficients of thermal expansion (CTE) of the materials that form the sensor. During the fabrication of a piezoresistive pressure sensor, different materials might be used for the sensor membrane, piezoresistors, sealing layer, etc. The CTE mismatch will induce residual stresses in the piezoresistors, and also in the membrane, that will affect the load-deflection response of the last one (as it will be seen in Chap. 5).

- *Temperature coefficient of voltage offset (TCO)*. Similar as the sensitivity, the offset voltage of the sensor will also change with temperature. One of the reasons for

this is again the variation of the stresses induced by the CTE mismatch of the different materials. Moreover, we must remember that the resistance values of the piezoresistors will also change with temperature. A mismatch between the TCR of the piezoresistors will also contribute to the TCO. Another reason is the variation of the cavity pressure with temperature due to the expansion of the gasses trapped inside the sensor cavity. For this reason it is in general preferred to have a vacuum-sealed cavity as this will minimize the trapped gas effects. The TCO is also expressed in ppm/°C.

The most important parameters to evaluate a piezoresistive pressure sensor performance are defined in the above list. Other important parameters, like Signal to Noise ratio (SNR), temperature nonlinearity of sensitivity (TNS) and temperature nonlinearity of offset voltage (TNO), will not be considered in this work. During the design phase of the piezoresistive pressure sensor, described in this chapter, only the sensitivity and nonlinearity will be considered. However, during the experimental evaluation of the fabricated devices (Chap. 6), all the parameters described above will be measured.

## 3.2 Design

The sensor design has been done based primarily on optimized sensitivity. The sensitivity of the different designs can be calculated from the piezoresistive coefficients for poly-SiGe measured in Chap. 2 by applying expression (3.3). However, in order to do so, the applied stress has to be calculated. The stress induced in the piezoresistors due to the deflection of the membrane under pressure can be predicted using FEM. FEM is a numeric procedure for the approximation solution of partial differential equations within boundary conditions. In this work, COMSOL Multiphysics [18] is used as finite element analysis and solver software package to simulate the mechanical behaviour of the sensor membrane.

Figure 3.4 shows a sketch (both top and cross-section views) of the piezoresistive pressure sensor considered in this work. The pressure sensor consists in a deformable membrane with four piezoresistors placed on top, following a Wheatstone bridge configuration. The membrane is fixed by a support ring to the substrate. In this figure, the different design parameters considered in this study are also illustrated. Regarding the sensor membrane, the main design parameters are the area and thickness. Most of the sensors simulated in this chapter will have a square membrane; however, in Sect. 3.2.2, the effect of using a rectangular membrane instead will be studied. From the piezoresistors point of view, the main design parameters include length, width, shape and location (represented as edge-offset, distance to the membrane edge).

Figure 3.5a shows the 3D FEA model of a square piezoresistive pressure sensor used in the simulations. To simplify the sensors model and reduce the computational time, the simulations are performed considering a simplified model of the sensors, including only the membrane and the piezoresistors. Therefore, important features

that will be present in the real sensors, like the release holes, sealing layer or isolation layer between the SiGe piezoresistors and the SiGe membrane, are not included in the FEA model. The effect of these extra layers on the final sensor performance will be evaluated in Chap. 6. Moreover, the membranes are modelled as perfectly clamped at all edges; in reality, however, the membranes will be supported by a ring of anchors that might bend as the membrane deflects. In order to characterize the error introduced by considering non-movable walls, in Sect. 3.2.1 the effect of support width (Fig. 3.4) on the membrane deflection, stress and sensor sensitivity will be illustrated. Figure 3.5b shows the mesh for the piezoresistive sensor model depicted in Fig. 3.5a. During mesh generation, special care has to be taken when selecting the element size; too fine a mesh will cause unnecessary computational overheads when running the model, whereas too coarse a mesh will produce intolerable approximation errors. In order to limit the computational time while keeping a reasonable accuracy in the solutions, a finer mesh was chosen for the piezoresistors and the membrane area surrounding the piezoresistors, while a coarser mesh was defined for the rest of the model.

The following material properties are used in the simulations: a Young's modulus of 147 GPa (108 GPa) for the membrane (piezoresistors) and a Poisson's ratio of 0.23, both for the membrane and the piezoresistors. The values for the Young's modulus were obtained by nanoindentation (see Chaps. 2 and 5). No initial residual stress, in the membrane or piezoresistors, was considered. As for the boundary conditions, the four edges of the membrane were fixed, while a uniform and perpendicular pressure load was applied on the top surface. The effect of the geometric nonlinearity, due to large deformations, was included in the simulations. From these simulations, results such as membrane deflection or the stress induced in the piezoresistors can be obtained.

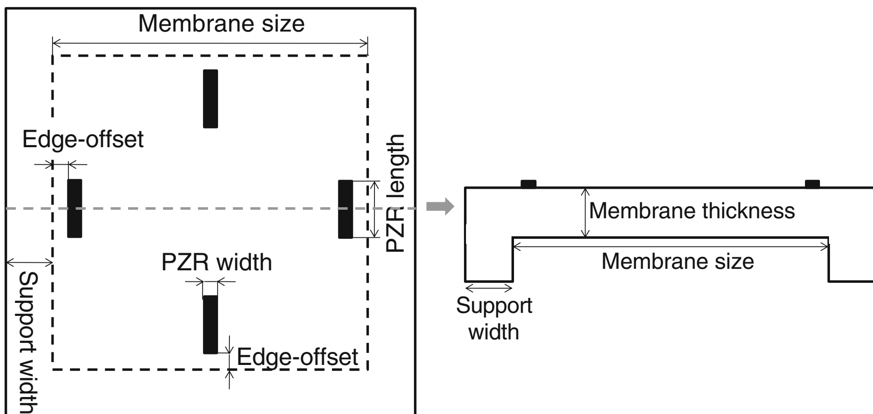


**Fig. 3.4** Top view and cross-section sketch of a typical pressure sensor with four sensing piezoresistors. The main design parameters are also illustrated. These design parameters include membrane dimensions and piezoresistors length, width, shape and location (represented by 'Edge-offset'). The width of the support ring surrounding the membrane is also a design parameter

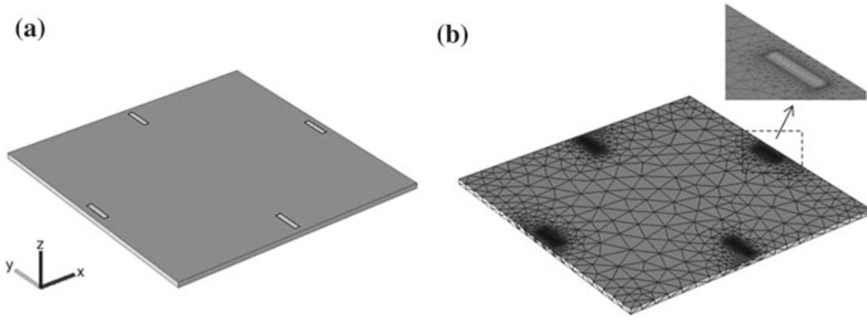


**Fig. 3.5** **a** COMSOL model of a square membrane with four piezoresistors placed on top. **b** Meshed view of the sensor model; mesh is denser in and around the object of interest (i.e, the piezoresistors)

In the following sections, the effect of the design parameters, illustrated in Fig. 3.4, on the sensor performance is studied. The relative resistance variation of the piezoresistors is calculated by substituting in (3.1) $\sigma_l$ and $\sigma_t$ by the simulated values of induced stresses, and $\sigma_l$ and $\sigma_t$ by the longitudinal and transverse piezoresistive coefficients experimentally obtained in Chap. 2. The output voltage of the sensor is then obtained from (3.3). The sensor performance for the different designs will be evaluated mainly on terms of sensitivity and nonlinearity.

The values for $\pi_l$ and $\pi_t$ used throughout this chapter correspond to a poly-$Si_{36}Ge_{64}$ layer deposited at 500 °C and annealed at 570 °C (layer 2 in Table 2.1) with an optimum doping concentration of $1 \times 10^{19}$ cm$^{-3}$($\pi_l = 18.7 \times 10^{-11}$ Pa$^{-1}$ and $\pi_t = 1.28 \times 10^{-11}$ Pa$^{-1}$). As already discussed in Chap. 2, this poly-SiGe layer, despite its attractive piezoresistive properties, is processed at a too high temperature ($\geq$ 500 °C) and it is therefore not compatible with post-processing above CMOS. In this work, the sensing layer used during the fabrications of the CMOS-compatible pressure sensors (Chaps. 4, 6 and 7) is a layer deposited and annealed at temperatures $\leq$ 460 °C (layer 4 in Table 2.1). However, the piezoresistive coefficients of this CMOS-compatible layer were not yet known at the time of the sensor design described in this chapter. For this reason, the $\pi_l$ and $\pi_t$ values of the poly-$Si_{36}Ge_{64}$ layer were used instead.

### *3.2.1 Membrane Area and Thickness*

The membrane dimensions are the design parameters with the highest impact on the sensitivity of the piezoresistive sensors. Figure 3.6 plots the simulated values of sensitivity (for a piezoresistive sensor similar to the one depicted in Fig. 3.5a) as a function of membrane thickness for sensors with different areas (from 200 × 200 to 500 × 500 μm$^2$). As can be expected, the sensitivity is higher for sensors with thinner membranes. In this work the membrane thickness was fixed to 4 μm, the standard

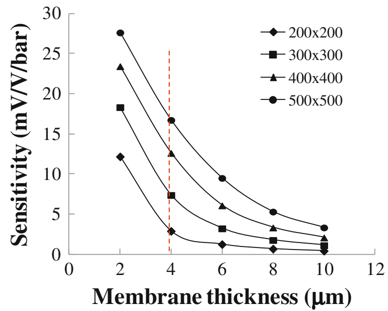


**Fig. 3.6** Sensor sensitivity as a function of membrane thickness for different membrane areas (in μm$^2$). In all cases the piezoresistors, located at a distance of 1 μm from the membrane edge, are 10 μm long and 2 μm wide

thickness of the structural layer in imec's poly-SiGe MEMS technology. For a fixed membrane thickness, the sensitivity increases with membrane area.

Figure 3.7a plots the sensor output voltage (considering a bias voltage of 1 V) versus applied pressure for sensors with different membrane areas but with a fixed membrane thickness of 4 μm. Smaller sensors exhibit very linear response while a clear deviation from the ideal linear response can be observed for a 500 × 500 μm$^2$ sensor. In general, larger membranes result in higher output signal, but they are also prone to large deflections and nonlinear effects. Figure 3.7b plots the calculated nonlinearity (using the "end-point line" method, as seen in Fig. 3.3) as a function of membrane length for a maximum applied pressure of 1 bar. We can conclude that for a fixed membrane thickness, the nonlinearity increases with membrane area at a much faster rate than the sensitivity, so a high sensitivity may involve a non-tolerable linearity error. In practice, during the design of a piezoresistive pressure sensor, if a maximum allowed nonlinearity error is specified, it is better to choose the membrane area to meet this specification (or at least as close as possible), since

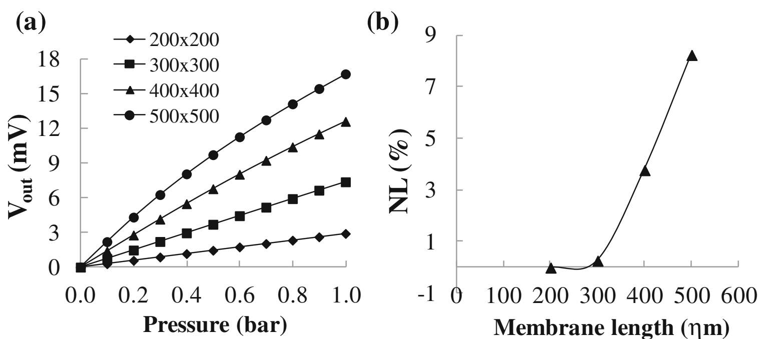


**Fig. 3.7** Simulated sensor output voltage for a $V_{bias}$ = 1V (**a**) and nonlinearity (**b**) for 4 μm-thick square sensors of different areas (in μm$^2$). As before, the piezoresistors are located at the edges of the membrane, with dimensions 10 μm long and 2 μm wide. Nonlinearity increases with membrane area, from 0.007 % for a membrane of 200 × 200 μm$^2$, to more than 8 % for a membrane of 500 × 500 μm$^2$

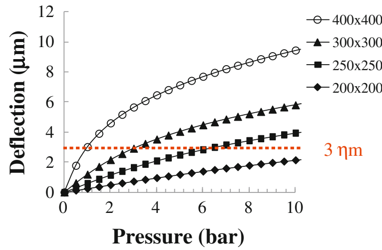


**Fig. 3.8** Maximum deflection (obtained by finite element simulations) in the centre of 4 μm-thick poly-SiGe membrane with different areas (in μm$^2$). The effect of the geometric nonlinearity is clearly visible in the load-deflection response of the bigger membranes. The maximum allowed deflection (defined by the cavity height below the membrane) is also indicated

the subsequent reduction in output signal can be easily taken care of in the readout circuit (for example, by including an amplifier).

In this work, the nonlinearity is not a primary design requirement. A high sensitivity is preferred. The maximum possible membrane area for a fixed thickness of 4 μm is limited by the allowed maximum deflection of the membrane into the sensor cavity and the excess stress. For proper pressure measurement, the deflection of the membrane at maximum pressure can never be larger than the cavity height. In this work, the cavitiy height is fixed to 3 μm, as will be seen in Chap. 4. On the other hand, to avoid failure of the device, the maximum stress on the membrane can never be greater than the fracture strength of poly-SiGe (∼1.6 GPa [19]). According to the maximum normal stress criterion, often used to predict the failure of brittle materials, failure occurs when the maximum (normal) principal stress reaches either the uniaxial tension strength or the uniaxial compression strength. For safety, we will limit the maximum allowed stress in the membrane to half of the fracture strength of poly-SiGe (∼800 MPa).

Figures 3.8 and 3.9 show the simulated maximum deflection (at the centre of the membrane) and the maximum induced stress, respectively, for 4 μm-thick membranes with different areas. As can be expected, larger membranes deflect more. The

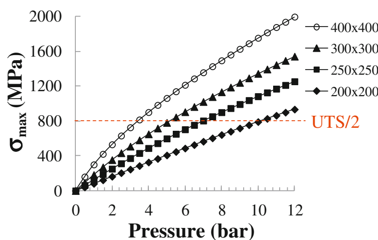


**Fig. 3.9** Maximum tensile stress (on top of the membrane, at the centre of the membrane edge) for 4 μm-thick poly-SiGe membrane with different areas (in μm$^2$). The maximum allowed stress (∼ half of the fracture strength of poly-SiGe) is also indicated

**Table 3.1** Simulated performance parameters for sensors with different membrane areas

| Membrane area ($\mu m^2$) | 200 × 200 | 250 × 250 | 300 × 300 |
|---|---|---|---|
| Working pressure range (bar) | 0–10 | 0–6 | 0–3 |
| Sensitivity (mV/V/bar) | 2.9 | 4.6 | 6.8 |
| NL (%FSS) | 1.76 | 3.5 | 3.61 |

Both the sensitivity and nonlinearity are calculated with respect to the full working pressure range. Nonlinearity is calculated using the end-point line method

effect of the geometric nonlinearity is clearly visible in the load-deflection response of 300 × 300 and 400 × 400 $\mu m^2$ membranes, while for a 200 × 200 $\mu m^2$ membrane a very linear response is obtained. In both graphs a red line indicates the design limitations: the maximum permitted deflection is 3 μm (gap depth) and the maximum allowable stress is 800 MPa (∼50 % of the fracture strength of poly-SiGe). From these graphs we can see that, in our case, the membrane deflection is the main limiting parameter. Only for the smallest considered membranes the stress is a concern. For a membrane of 200 × 200 $\mu m^2$ the maximum working pressure ($P_{max}$) will be ∼10 bar (limited by the maximum stress criterion). For the larger membranes, the pressure range is limited by the maximum deflection; for 300 × 300 $\mu m^2$ and 400 × 400 $\mu m^2$ membranes, $P_{max}$ is ∼3 and ∼1 bar, respectively. In general, for a fixed membrane area, these graphs help defining the working pressure range of the device. The opposite is also possible: determining the maximum possible membrane area for a given working pressure range. For example, if we need the poly-SiGe pressure sensor to work in the pressure range 0–10 bar, these two figures tell us that we need to use a membrane smaller than 200 × 200 $\mu m^2$. If the working pressure range is only from 0 to 1 bar, any of the three proposed membrane areas could be used, and the decision should be taken based on sensitivity or nonlinearity requirements.

Finally, in this work, square poly-SiGe pressure sensors with three different membrane areas were designed: 200 × 200, 250 × 250 and 300 × 300 $\mu m^2$. The expected sensitivities, nonlinearity and working pressure range are summarized in Table 3.1. The values correspond to sensors with the specified area and with four poly-SiGe piezoresistors arranged as in the model in Fig. 3.5. It was decided to limit the membrane area to a maximum of 300 × 300 $\mu m^2$, since the larger the membrane, the more prone to fracture/failure during the fabrication process they are, as will be seen in Chap. 4.

### *3.2.2 Piezoresistor Placement*

Figure 3.10 shows the stress distribution at the top of the membrane on a 250 × 250 $\mu m^2$ and 4 μm-thick poly-SiGe membrane when subjected to an external pressure of 5 bar. From this figure we can observe that the stress concentration is high at the centre and the areas near the middle edge of the membrane. Also, the stress

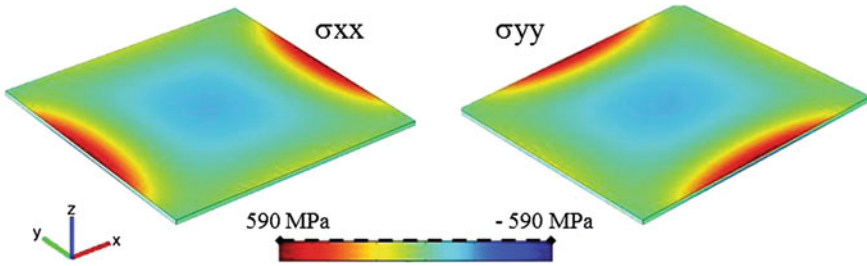


**Fig. 3.10** Simulated normal stress distribution for a 4 μm-thick and 250 × 250 μm$^2$ poly-SiGe membrane subjected to an external pressure of 5 bar

is tensile (positive) at the edge of the membrane and compressive (negative) in the centre. These observations are also valid for membranes with a different area and/or thickness.

In the previous simulations, the piezoresistors were always placed at the edge of the membrane, where the stress is positive. However, this might not be the optimal piezoresistor placement. From Chap. 2 we know that the longitudinal piezoresistive coefficient ($\pi_l$) of boron-implanted poly-SiGe is much larger than the transverse piezoresistive coefficient ($\pi_t$). Therefore, when poly-SiGe piezoresistors are used, they should be arranged in such a way that they should experience maximum longitudinal stress in order to achieve better sensitivity. Moreover, from expression (3.3) it can be seen that, to increase the sensor output voltage, the relative resistance variation for the transverse piezoresistors ($\Delta R/R_t$) should be negative (assuming a positive $\Delta R/R_l$). Based on these two considerations ($\pi_t$ of poly-SiGe a lot smaller than $\pi_l$, and the preferred negative $\Delta R/R_t$ ) we can conclude that by placing the transverse piezoresistors in the centre of the membrane, where a higher and negative longitudinal stress is found, the sensitivity can be improved as compared to the traditional piezoresistor placement (at the edge).

Figures 3.11 and 3.12 illustrate the effect of piezoresistor placement on the sensitivity of a $250 \times 250\ \mu m^2$ sensor. Figure 3.11 plots the sensor sensitivity as a function of the edge-offset (distance to the edge) of the transverse piezoresistor, while the longitudinal piezoresistor remains at the edge of the membrane. This graph confirms the previous reasoning: by placing the transverse piezoresistor in the centre of the membrane the sensitivity can be improved by a factor of about 2. A certain saturation is observed: once the transverse piezoresistors enter the area of negative stress, no significant further improvement of sensitivity is obtained. For example, the increase in sensitivity by placing the piezoresistors at a distance of 5 μm from the centre as compared to 25 μm is of only ∼2 %. This is due to the relatively flat profile of the stress around the centre of the membrane (Fig. 3.13).

Figure 3.12 plots the opposite situation: the longitudinal piezoresistor is the one which moves, while the transverse piezoresistor is fixed at the edge of the membrane. No improvement in sensitivity is observed: by placing the longitudinal piezoresistors closer to the centre while the transverse piezoresistors are placed at the edge, the

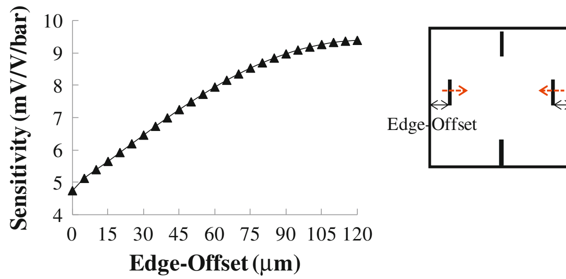


**Fig. 3.11** Sensor sensitivity (for a 250 × 250 $\mu m^2$ membrane) as a function of the transverse piezoresistor position. Edge-offset represents the distance to the edge: at the edge of the membrane is 0, while at the centre is 125 μm. The longitudinal piezoresistor is always located at a distance of 1 μm from the edge

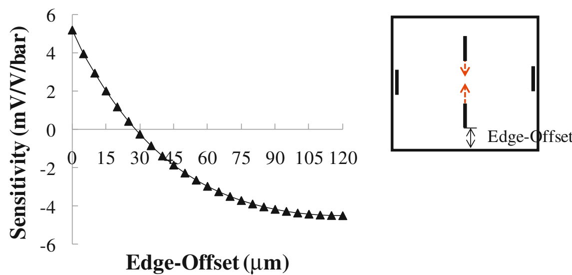


**Fig. 3.12** Simulated sensitivity as a funtion of the distance from the membrane edge of the longitudinal piezoresistor. The membrane is 250 × 250 $\mu m^2$ and the transverse piezoresistor is placed at a distance of 1 μm from the membrane edge

sensor sensitivity remains practically the same in magnitude but with opposite sign. It is important to note that if both the transverse and longitudinal piezoresistors are placed in the centre of the membrane, the sensitivity will be deteriorated as both relative resistance variations will have the same sign and similar magnitude (see expression (3.3)).

Finally, for each of the chosen membrane areas (see section above), two different sensor designs were considered: one design with the transverse piezoresistors placed at the edge, and one where they are placed in the centre (distance of 5 μm from the centre). However, by placing the transverse piezoresistors in the centre, not only the sensitivity is increased, but also the NL (for definition, see Sect. 3.1.2). For example, for a 250 × 250 $\mu m^2$ membrane with transverse piezoresistors placed at the edge the NL is ∼2.6 %, while if the piezoresistors are placed in the centre of the membrane the NL is ∼5.9 %. As explained in Sect. 3.1.2, the structural or geometric nonlinearity arises from the nonlinear relationship between the stress and the applied pressure when the deflection of the membrane is not small compared to its thickness (large deformation theory). In that case, the central plane of the diaphragm stretches like a balloon, causing the membrane to be subjected to an in-plane stress component

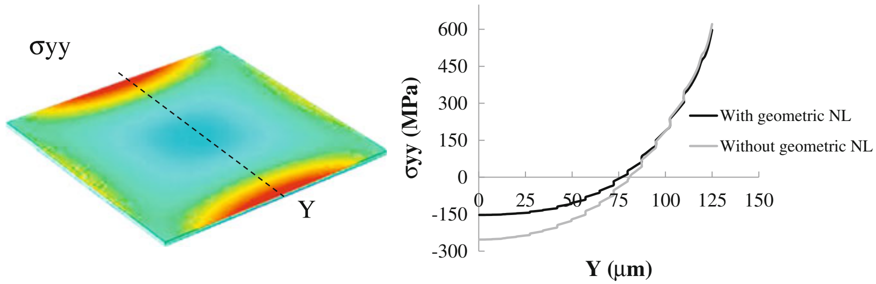


**Fig. 3.13** Simulated stress along the Y direction (for X = 0) versus position (Y = 0 represents the membrane centre while Y = 125 μm corresponds to the edge) for an applied pressure of 5 bar. In *red* the simulated curve including the geometric nonlinearity, and in *blue*, the idea curve (without nonlinearity). Both curves are very close at the membrane edge but differ considerably at the centre

($\sigma_c$) in addition to the stress caused by the bending of the membrane ($\sigma_b$). The bending stress ($\sigma_b$) gets reduced in magnitude as the stretch of the diaphragm takes part of the pressure load and this result in the nonlinearity. $\sigma_c$ is always positive whereas the polarity of $\sigma_b$ can be positive or negative depending on the location in the membrane (as was already seen in Fig. 3.10). Therefore, at the edge of the diaphragm, both stresses are positive and add up, and the total stress tends to be closer to the linear theory (small deflection theory). On the other hand, in the centre of the membrane $\sigma_b$ is negative while $\sigma_c$ is positive, and the total stress deviates more from the linear theory. This effect is illustrated in Fig. 3.13, in which the stress along the Y direction (across the centre of the membrane, with X = 0) is plotted versus position for an applied pressure of 5 bar; one curve represents the obtained stress when the geometric nonlinearity is included in the simulations, while the other curve corresponds to the linear case, without including geometric nonlinearity. It can be clearly seen how the stress in the centre (Y = 0) deviates more from the linear response, while in comparison the nonlinear effect at the edge is almost negligible. Therefore, piezoresistors placed in the centre of the membrane will exhibit a more nonlinear behaviour (Fig. 3.14).

### *3.2.3 Piezoresistor Dimensions*

In this section, the effect of the piezoresistors length and width on their stress resistance variation behaviour is studied. For optimum sensor sensitivity it is important to select the piezoresistor dimensions that result in the largest resistance variation with stress. As already seen in Sect. 3.1, a maximum in the sensor output voltage (expression (3.2)) occurs when r = 1. Considering this, together with a desirable zero-offset, we can conclude that for optimized sensitivity the resistance value of the four piezoresistors should be equal to each other. This means that, assuming that all

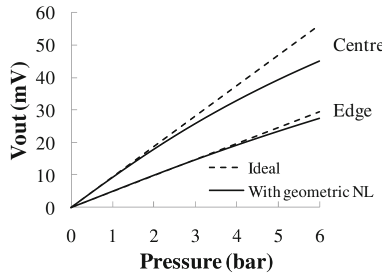


**Fig. 3.14** Deviation from the ideal output voltage (for $V_{bias} = 1$ V) vs. pressure response due to geometric nonlinearity for a sensor with the transverse piezoresistors placed in the centre or at the edge of the membrane. In both cases the longitudinal piezoresistor ($10 \times 2 \times 0.2\,\mu$m) is placed at the edge

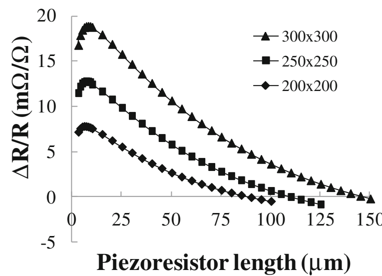


**Fig. 3.15** Relative resistance variation for the longitdinal piezoresistor as a function of the piezoresistor length for different membrane areas (in $\mu m^2$). The membrane thickness is always 4 $\mu$m, and the edge-offset is 1$\mu$m. The applied pressure is 1 bar

piezoresistors will (ideally) exhibit the same resistivity, they should all have the same dimensions. For this reason, only the dimensions of the longitudinal piezoresistors will be optimized here. The selected dimensions will be also applied to the transverse piezoresistors.

Figure 3.15 shows the simulated relative resistance variation of the longitudinal piezoresistors with respect to the resistor length for three different membrane areas. Similar graphs were reported in [19, 20] for polysilicon resistors. The thickness of the membrane is 4 $\mu$m and the width and thickness of the piezoresistors are 2 $\mu$m and 200 nm, respectively. The edge-offset is, for all cases, 1 $\mu$m. Pressure = 1 bar. Independently of the membrane area, once a certain length is reached, the relative resistance variation decreases drastically with increasing resistor length. This can be explained considering that the maximum tensile stress is concentrated in a small region around the centre edge of the membrane (Fig. 3.10). Outside of this stress-concentration area, while approaching the membrane centre, the stress drops rapidly, becoming eventually negative. Thus, if the resistors are too long, part of them will be subjected to little or even compressive stress, making the total average stress in the piezoresistor smaller. For the three membrane areas considered, an optimum resistor

length, resulting in a maximum in the resistance variation, is found. This optimum length decreases slightly with membrane area: for a $300 \times 300\,\mu m^2$ membrane the optimum length is $\sim$8 μm, while for a $200 \times 200\,\mu m^2$ is $\sim$6 μm. For simplicity, in the final pressure sensor design, a fixed piezoresistor length of 10 μm is used for all the membrane areas. The degradation in resistance variation for not using the exact optimum length is negligible (<3.5 % in the worst case, for a membrane of $200 \times 200\,\mu m^2$).

So far a fixed resistor width of 2 μm has been used in the simulations. In order to check if there is also an optimum width, the resistance change for a 10 μm long resistor was evaluated for different widths (from 1 to 10 μm). As shown in Fig. 3.16, for all three membrane areas considered, the effect of resistor width on the resistance variation with stress is negligible. Only a slight decrease ($\sim$1 %) as the resistor width approaches 10 μm is observed. In the final design, a fixed resistor width of 2 μm is used.

### 3.2.4 Piezoresistor Shape

After optimizing the piezoresistors location and dimensions in terms of sensor sensitivity, the last design parameter related to the piezoresistors considered in this work is the shape of the longitudinal piezoresistors. Only line-shape transverse piezoresistors are considered in this work. Figure 3.17 shows the three different longitudinal piezoresistor shapes considered. The first one is the usual piezoresistor line-shape. The second one depicts an "n-shape" piezoresistor while the last one consists in an "m-shape" piezoresistor. Similar piezoresistor designs were already used in [20, 21], where metal pads were used to connect the different parts of the resistors. In this work, to facilitate fabrication, the whole piezoresistor is made of poly-SiGe. For the last two piezoresistor designs, electrical simulations were performed in COMSOL to calculate the exact total resistance value. From this simulated value, the length that an equivalent line-shape resistor should have to match the resistance value of the

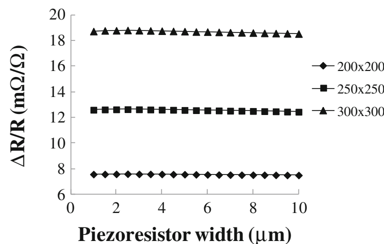


**Fig. 3.16** Relative resistance variation as a function of piezoresistor width for the longitudinal piezoresistors. The piezoresistors are located on 4 μm-thick membranes with different areas (in $\mu m^2$). The edge-offset is 1 μm for all cases

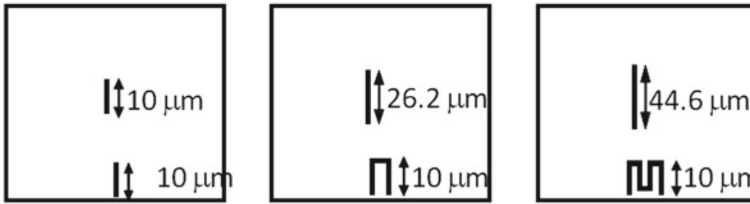


**Fig. 3.17** Different longitudinal piezoresistor designs considered. To ensure all 4 resistors have the same value, finite element simulations of the total longitudinal piezoresistor resistance were performed. From this simulated resistance value, the equivalent length for the transverse piezoresistor was calculated. The piezoresistor width is always 2 μm

"n-shape" or "m-hape" resistor is obtained. This calculated length is then applied to the transverse piezoresistors in order to ensure zero-offset and maximum output voltage.

In order to estimate the sensor output for the different designs, the stress distribution in the resistors must be simulated. Figure 3.18 shows the simulated stress distribution for the three different resistor patterns when the piezoresistors are located on top of a $300 \times 300\,\mu\text{m}^2$ and 4 μm thick membrane subjected to 1 bar pressure load. It can be observed that the stress distribution in the piezoresistors is not uniform. The average longitudinal (transverse) stress in the piezoresistors is obtained in the same way as in all simulations described in this work, by integrating the simulated $\sigma_{yy}$ ($\sigma_{xx}$) in the whole piezoresistor volume. It is important to note that both the "n-shape" resistor and the resistor with "m-shape" are considered as one single volume.

Figure 3.19 plots the calculated sensor output (assuming a 1V bridge bias) for a $300 \times 300\,\mu\text{m}^2$ and 4 μm thick membrane with the three considered longitudinal piezoresistor designs (Fig. 3.18). In all cases the transverse piezoresistors are placed

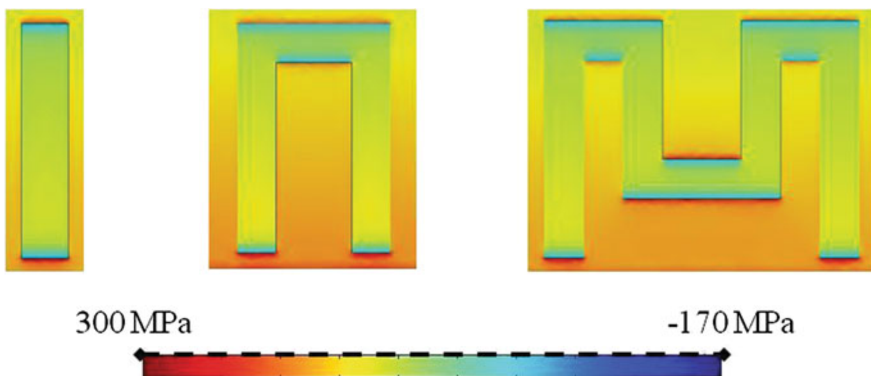


**Fig. 3.18** Simulated stress distribution in the longitudinal piezoresistor for the three considered designs. In all cases the piezoresistors are located on top of a 4 μm-thick and $300 \times 300\,\mu\text{m}^2$ poly-SiGe membrane subjected to 1 bar external pressure. The edge-offset is 1 μm

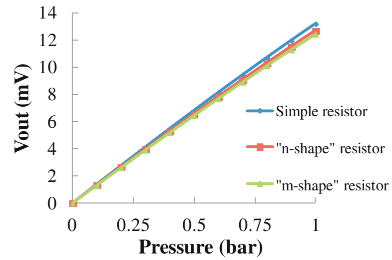


**Fig. 3.19** Simulated sensor output voltage as a function of applied pressure for the three different longitudinal piezoresistor designs considered

at a distance of 5 μm from the membrane centre, as depicted in Fig. 3.17. Similar as in [22], no influence of the resistor shape on the sensor sensitivity is observed. This is due to the fact that the average stress over the total volume of the piezoresistors is practically the same for the three designs. Actually, a slight decrease in sensor output voltage with an increasing number of "turns" of the piezoresistors is observed in Fig. 3.19. This can be explained considering that "n-shape" resistors or "m-shape" resistors incorporate a larger portion subjected to less stress (see Fig. 3.18), slightly decreasing the average stress. On the other hand, no difference in the sensor nonlinearity for the three piezoresistors considered was observed.

### *3.2.5 Membrane Shape*

The last design parameter studied in this work is the membrane shape. So far, only square-shape membranes were considered. In this section, the effect of using a rectangular membrane on the sensor sensitivity will be evaluated. Figure 3.20 shows the finite element simulations of the longitudinal stress (along the Y direction) in a rectangular sensor subjected to an outside pressure of 1 bar with central placement of piezoresistors.

The piezoresistors located at the edges of the membrane undergo maximum longitudinal tensile stress and those located at the centre of the membrane experience

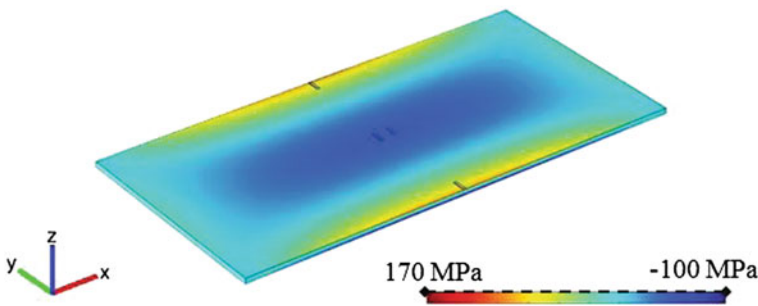


**Fig. 3.20** Simulated longitudinal stress ($\sigma yy$) for a 4 μm-thick rectangular sensor subjected to 1 bar external pressure

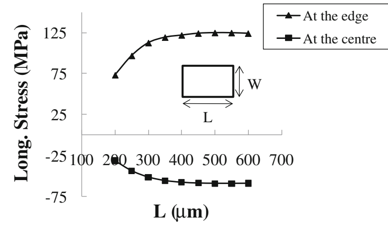


**Fig. 3.21** Maximum longitudinal stress (along Y direction for X = 0) for a 4 µm-thick rectangular membrane, as a function of its length for fixed width (W = 200 µm). Pressure = 1 bar

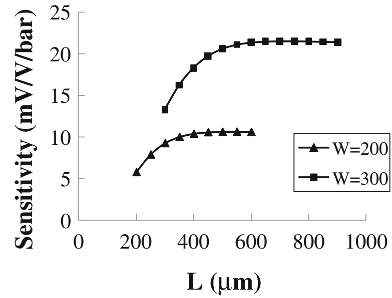


**Fig. 3.22** Simulated sensitivity (in the 0 to 1 bar pressure range) for a 4 µm-thick rectangular membrane with the piezoresistor pattern depicted in Fig. 3.20, as a function of membrane length with fixed width (in µm)

longitudinal compressive stress. The results of our simulations (Fig. 3.21) show that the magnitudes of these longitudinal stresses at the edge and at the centre increase and reach a maximum value when the membrane is rectangular with a length L to width W ratio equal to or larger than two. This maximum in the longitudinal stress for L/W = 2 translates into a maximum in the sensor sensitivity (Fig. 3.22). Similar results are found for poly-Si pressure sensors [5].

Table 3.2 offers a comparison between the performance of two pressure sensors: one sensor has a square-shaped membrane while the the other sensor is rectangular. Both of them with the same piezoresistor pattern/placement: line-shape resistors with the transverse piezoresistors placed in the centre (as in Fig. 3.20). For the same pressure range (0–1 bar), the rectangular sensor offers a 36 % higher sensitivity while exhibiting the same maximum deflection and nonlinearity. Finally we can conclude that, similar as for poly-Si [5], for poly-SiGe-based piezoresistive pressure sensors rectangular-shaped membranes offer better performance than equivalent square-shaped membranes, with an optimum length/width ratio equal to 2.

**Table 3.2** Comparison between the simulated values for deflection, sensitivity and nonlinearity for a square sensor of 200 × 200 µm$^2$ and a rectangular sensor of 350 × 175 µm$^2$

| Membrane area | 200 × 200 µm$^2$ | 350 × 175 µm$^2$ |
|---|---|---|
| Max. deflection (µm) | 0.24 | 0.28 |
| Sensitivity (mV/V/bar) | 5.74 | 7.83 |
| NL (%) | 0.1 | 0.114 |

In both cases the membrane thickness is 4 µm and the transverse piezoresistors are placed in the centre of the membrane. Values corresponding to a pressure range 0–1 bar

**Table 3.3** Comparison between the maximum deflection and stress for a $250 \times 250\,\mu m^2$ membrane modelled as perfectly clamped, or with 25 μm-wide supports

| Load (bar) | Fully clamped | | | With supports | | |
|---|---|---|---|---|---|---|
| | Deflection ($\mu$m) | $\sigma_{max}$ edge (MPa) | $\sigma_{max}$ centre (MPa) | Deflection ($\mu$m) | $\sigma_{max}$ edge (MPa) | $\sigma_{max}$ centre (MPa) |
| 1 | −0.59 | 117.6 | −47.39 | −0.6303 | 108.5 | −49.5 |
| 6 | −2.835 | 659 | −163.8 | −3.0242 | 602.5 | −169 |

### *3.2.6 Effect of Supports*

In all the described simulations the membranes are modeled as perfectly clamped in all four edges. In reality, however, this is not true. The membranes will be supported by a ring of poly-SiGe anchors that can bend as the membrane deforms, which may result in larger deflections and in a reduction of the stress. As will be seen in Chap. 4, the total anchor region surrounding each membrane is 25 μm for all the sensors. In order to estimate the error induced in the previous simulations by the assumption of rigid supports, finite element simulations of the deflection and maximum stress for a $250 \times 250\,\mu m^2$ membrane under two different loads were performed. Table 3.3 offers a comparison between the results obtained with the membrane modeled as fully clamped (left hand side), and with the membrane supported by a 25 μm-wide and 7 μm tall (considering a 3 μm cavity height) poly-SiGe wall. For the supported membranes, the stress caused by the external pressure bends the membrane walls inwards, resulting in an amplified displacement at the centre of the membrane, and in a minor tensile stress at the membrane edges. The compressive stress at the membrane centre, on the other hand, increases slightly. In any case, the error committed by considering the membranes as fully clamped is almost negligible. For a $250 \times 250\,\mu m^2$ membrane subjected to 6 bar pressure (maximum working pressure, see Sect. 6.2), the movable walls translate into an increase in deflection of less than 7 %, and a decrease in maximum tensile stress at the membrane edge of only ∼8.5 %. This decrease in tensile stress results in a reduction in sensitivity (in the 0–6 bar pressure range) of around 7 %, if the transverse piezoresistors are placed at the membrane edge, and about 5.2 % if they are placed in the centre of the membrane.

## 3.3 Summary and Conclusions of the Sensor Design

In this chapter, finite element simulations together with the experimentally obtained piezoresistive coefficients (Chap. 2) were used to evaluate the impact of several design parameters on the sensitivity and nonlinearity of a poly-SiGe-based piezoresistive pressure sensor. The considered design parameters include: the sensor membrane area

and shape, and the dimensions, shape and placement of the poly-SiGe piezoresistors. From the obtained results we can conclude:

- Larger membranes translate into higher sensitivities but also increased nonlinearity.
- Placing the transverses piezoresistors in the centre of the membrane instead of on the edge, as usual, increases the sensor sensitivity by a factor of ~2. This is due to the fact that the transverse piezoresistive coefficient for poly-SiGe is much smaller than the longitudinal one.
- Poly-SiGe sensors with a rectangular membrane offer an improved performance in terms of sensitivity and nonlinearity as compared to square-shaped sensors. The optimal membrane length to width ratio is about 2. This conclusion applies only if the transverse piezoresistors are placed in the centre of the membrane.
- For the considered membrane areas ($200 \times 200$, $250 \times 250$ and $300 \times 300\,\mu m^2$), the optimal length for the longitudinal piezoresistors is around 10 μm. On the other hand, the effect of piezoresistor width on the relative resistance variation is negligible.
- Three different shapes of the longitudinal piezoresistors were considered ("line-shape", "n-shape" and "m-shape" resistors); in all cases the expected sensor sensitivity was the same.

In order to corroborate the mentioned results and observations, three different membrane areas ($200 \times 200$, $250 \times 250$ and $300 \times 300\,\mu m^2$) with six different designs per area were included in the final layout (Fig. 3.23). The six different designs include three different longitudinal piezoresistor shape and two placements for the transverse piezoresistors: at the membrane edge and at a distance of 5 μm from the centre. The membrane areas were selected based on the maximum allowed deflection (fixed by the cavity height, 3 μm) and the fracture strength of poly-SiGe (~1.6 GPa).

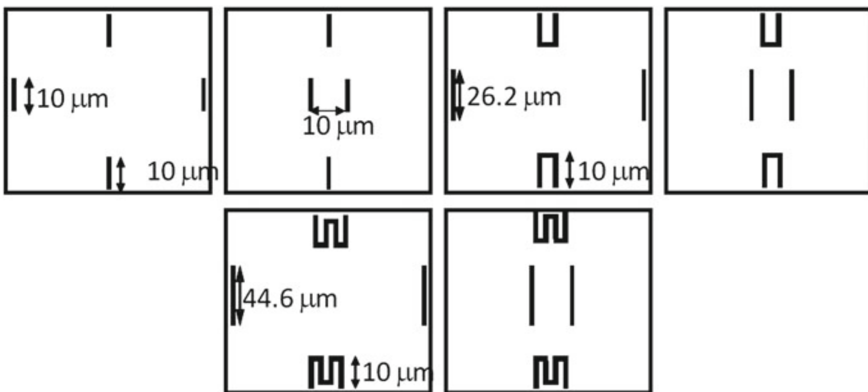


**Fig. 3.23** Six different piezoresistive sensor designs considered

For each of the three considered areas, the working pressure range is different. Also a rectangular membrane with dimensions $350 \times 175\ \mu m^2$ was included in the design. The final layout can be found in Appendix A.

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# Chapter 4
# The Pressure Sensor Fabrication Process

This chapter describes in detail the pressure sensor fabrication process. the maximum processing temperature of the complete sensor, including the poly-SiGe piezoresistors, is kept below 460 °C to enable above-CMOS integration. The developed process allows for the simultaneous fabrication of both piezoresistive and capacitive pressure sensors. It can also be used to fabricate sensors of different size and with different requirements (i.e, sensitivity, nonlinearity, sealed-in pressure, etc). Many of the process steps used in the fabrication of the pressure sensor are borrowed from the thin-film packaging flow, part of the SiGe-MEMS platform in imec.

Section 4.1 presents a generic cross-section of a combined piezoresistive/capacitive pressure sensor. Section 4.2 describes the different steps of the developed process flow for the fabrication of the pressure sensor. In Sect. 4.3 a more detailed description of the different process developments performed at imec specifically for the pressure sensor is given. The chapter ends with a summary of the developed fabrication process.

## 4.1 The Pressure Sensor Fabrication Process: A Generic Technology

One of the main challenges during the development of the pressure sensor fabrication process was to build-up a process flow compatible with post-processing on top of CMOS, to allow for the monolithic integration of MEMS-above-CMOS. In order to avoid introducing any degradation in the underlying CMOS circuitry, some care has to be taken during the fabrication of the MEMS pressure sensor: firstly, the electronic circuit needs a good passivation, so that it is well protected from the aggressive etch and deposition steps which are needed to fabricate the MEMS devices; and secondly the processing temperature for each step in the MEMS process flow needs to be low enough so that the performance of the underlying CMOS circuit is not deteriorated. The thermal budget limits for standard 0.35 and 0.25 μm CMOS wafers

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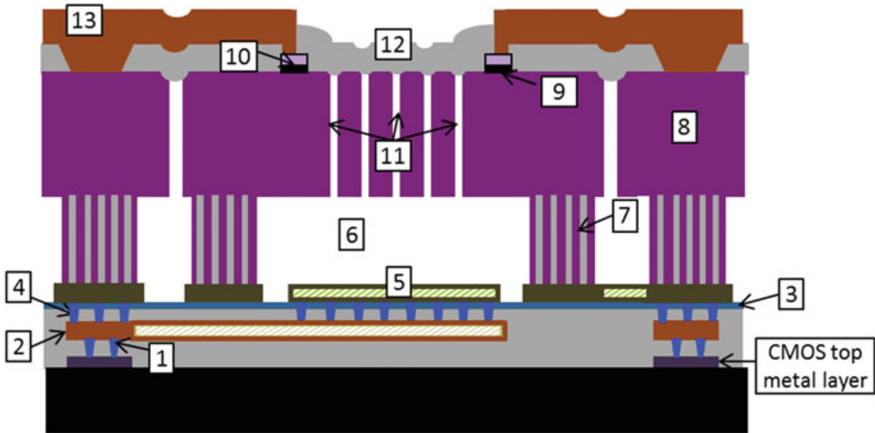


**Fig. 4.1** Cross-section of a generic capacitive/pressure sensor. *Dashed parts* are only present if capacitive sensing is also required; for piezoresistive-only sensors they are unnecessary

with aluminum based interconnects have already been experimentally investigated in [1] and [2], respectively. In both cases it was found that the degradation of the metal interconnects, rather than the transistor performance, is the limiting factor. In [1] a degradation of the interconnect resistance at temperatures above 450 °C was reported. In [2] an increase of more than 10 % in via resistance was found after only 2 h annealing at 450 °C. In this work the maximum processing temperature of the complete sensor, including the poly-SiGe piezoresistors, is kept below 460 °C to enable above-CMOS integration.

The developed fabrication process can be used to fabricate a capacitive, piezoresistive or a combined capacitive/piezoresistive pressure sensor. Figure 4.1 shows a cross-section of a pressure sensor that can be simultaneously used as capacitive and piezoresistive sensor. In appendix A, a layout of such a sensor is presented.

The different layers and structural components that form the pressure sensor are numbered in the figure and listed below.

1. **CMOS-MEMS via.** This via connects the top CMOS metal layer (Cu) to the bottom metal electrode of the MEMS (Al). As this work represents the first attempt in IMEC to build a poly-SiGe MEMS device on top of Cu CMOS, this module was specifically developed within this thesis. More details on the processing and electrical characterization of this copper to aluminum via will be given in Chap. 7.
2. **MEMS metal electrode.** This Ti/AlCu(0.5 %)/TiN metal electrode is the first MEMS device layer in the process flow. It functions as intermediate metal layer between the top CMOS metal layer and the MEMS SiGe electrode. It can also be used as a connection between the bondpad and the bottom electrode in capacitive pressure sensors, as depicted in Fig. 4.1. In thin-film packaging applications this

metal electrode provides an electrical feed through connection to the packaged device.

3. **CMOS passivation layer.** The purpose of this layer is to protect the metal electrodes and the underlying dielectric layers and CMOS circuit during the MEMS processing. Especially aggressive is the etching of the sacrificial oxide to release the sensor membrane, performed in vapor hydrogen-fluoride (vHF). A 400 nm-thick silicon carbide (SiC) is used as passivation layer. SiC was the selected material as it is resilient to the MEMS release process and it has good electrical isolation. SiC is also thermally stable, which assures that its microstructure does not change during the high temperature deposition steps and it is a very dense/hard material, so that the chemicals cannot diffuse through it [3–5] and attack the CMOS circuit.
4. **MEMS via.** These Tungsten-filled vias provide an electrical connection between the MEMS metal electrode and the MEMS SiGe electrode, through the SiC passivation layer.
5. **SiGe MEMS electrode.** These electrodes can be used to form the electrical interconnect between the different MEMS structures. For example, in a capacitive pressure sensor, the electrode layer provides an electrical path to connect the sensor membrane to the corresponding biasing bondpad. Also in the capacitive pressure sensor this electrode is the bottom plate of the capacitor. A 400 nm-thick CVD-deposited poly-SiGe layer is used as MEMS electrode.
6. **Gap.** The gap is the separation between the SiGe membrane and the SiGe bottom electrode. For capacitive pressure sensors, a smaller gap is preferred as it translates into a bigger (and therefore easier to measure) initial capacitance; it also results in improved sensitivity. For piezoresistive pressure sensors, the depth of the gap does not have an influence in sensor sensitivity. In general, the depth of the gap limits the maximum deflection of the membrane, and together with the maximum tensile strength of the membrane, limits the maximum pressure that the sensor can withstand, determining thus the working range of the device. This is not necessarily true for capacitive pressure sensors as they can also work in "touch" mode [6]. The gap depth is defined by the thickness of the deposited sacrificial oxide. Therefore, it is scalable: it can be easily made larger or smaller depending on the specifications of the required application. In this thesis, a nominal gap of 3 µm was used. For 1 wafer a gap of 1 µm was used to improve the performance of the capacitive sensors, as will be seen in Chap. 6.
7. **Anchor.** Trenches are etched in the sacrificial oxide, stopping in the underlying MEMS electrodes, and filled with SiGe (during the structural layer deposition) to define the anchors. These SiGe anchors fulfill two purposes. First they provide support to the MEMS structural layer. In this thesis, a 25 µm-wide ring of anchors surrounds each sensor, holding the membrane. And second, they offer an electrical connection to the SiGe electrode underneath. To ensure a nice SiGe filling and a planarized membrane layer after deposition, a fixed trench width of 0.8 µm was used in this work. The chosen anchor design (Fig. 4.2) consists of crossing vertical and horizontal anchor lanes with a spacing of 2.2 µm. This anchor design was

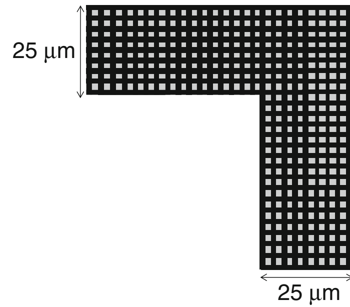


**Fig. 4.2** Anchor design. The poly-SiGe anchors (in *black*) have a width of 0.8 μm and are separated by 2.2 μm-wide oxide (in *light grey*) trenches

already used by Claes in [7] and proved to be robust enough for thin film packaging applications, as it meets the MIL-standard requirements for shear strength.

8. **SiGe structural layer.** This layer constitutes the sensor membrane. As already shown in Chap. 3, a thinner membrane results in a larger deflection for a certain applied pressure, therefore increasing the sensitivity of the pressure sensor. In practice, the membrane thickness will be defined according to requirements such as maximum working pressure, sensitivity or linearity. In this work, a fixed SiGe structural thickness of 4 μm was used, although other thicknesses, ranging from 1 to 10 μm, are supported in imec SiGe MEMS platform.
9. **Isolation layer.** This layer provides isolation between the SiGe membrane and the SiGe piezoresistors. A thin (100 nm) SiC layer is used as isolation layer. SiC is the selected material as it offers good electrical isolation and it is resilient to vHF, therefore preventing the SiGe piezoresistors to be etched off during the release process. This SiC isolation layer is later patterned: it only remains below the piezoresistors, being etched away everywhere else. In this way its impact in the overall sensor performance is minimized.
10. **Piezoresistors.** A thin undoped SiGe layer is deposited on top of the SiC isolation layer. After deposition this layer is boron implanted and annealed to create the poly-SiGe piezoresistive layer. The implantation and annealing conditions affect the piezoresistive and electrical properties of the layer, as was already explained in Chap. 2, and can be adapted according to the required specifications. It is important to note that steps 9 and 10 are specific for piezoresistive pressure sensors, and do not need to be implemented if only capacitive sensors are sought.
11. **Release holes.** Access holes are opened on the SiGe structural layer to provide a path for the vHF to etch away the sacrificial oxide beneath the membranes. In order to reduce the time required to etch away the sacrificial layer, and also preventing in this way attacking the anchor region, etch ports are opened in the membranes on top instead of using lateral etch paths. A symmetrical pattern of square release holes of $1 \times 1\,\mu m^2$ was used (Fig. 4.3). The size of the release holes was selected to be large enough to enable efficient sacrificial etching but, at the same time, small enough to limit both the required thickness of the sealing layer and the quantity of sealing material deposited on the interior surfaces of the cavity. The deposited sealing material will increase the membrane thickness.

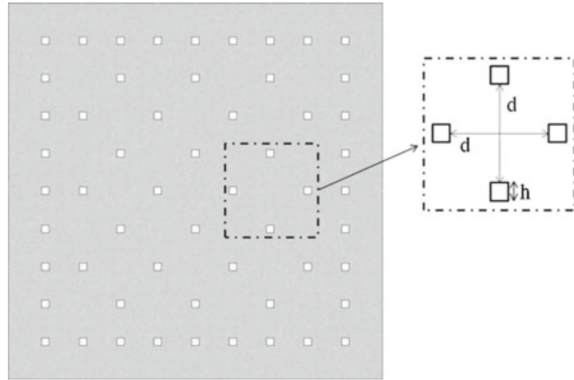


**Fig. 4.3** Top view of a perforated square membrane with square vertical release *holes*. On the *right*, a close view of the designed pattern of release *holes*, where h is 1 μm and d is 9.5 μm

For pressure sensor applications, a thin sealing layer is preferred to avoid degradation of the sensor sensitivity. A thin sealing layer also leads to less bi-material effects and ensures that the average membrane properties are close to those of the preferred SiGe material.

12. **Sealing layer.** The release holes are sealed by thin-film deposition. This layer must provide a hermetic sealing of the released cavity. Different sealing layers were considered in this thesis, as will be explained in detail in Chap. 5.
13. **Metal interconnect.** This metal layer provides electrical connection among the piezoresistors (in a Wheatstone bridge configuration) and between the piezoresistors and the bondpads. An AlCu (0.5 wt.%)-based stack is used for this purpose in this work. As modules 9 and 10, this metal interconnect is only necessary for piezoresistive pressure sensor.

These are the most important layers and modules that constitute the pressure sensor fabricated in this thesis. Most of these modules are part of the standard imec SiGe MEMS platform. With the exception of modules 9, 10 and 13, the pressure sensor fabrication process is similar to the imec thin-film packaging process flow [8]. Modules 9, 10 and 13 are particular for piezoresistive pressure sensors and were specifically developed in the frame of this thesis. Also module 1 was developed as part of this thesis, although it can be used for the integration of any MEMS with Cu-based interconnects CMOS circuit. Although module 12 is also part of the thin-film packaging flow, the sealing layer specifications for pressure sensor applications are not necessarily the same as for thin-film packaging. For this reason, an important part of this thesis was dedicated to the study and evaluation of different sealing layers (Chap. 5).

Finally, it is important to note that the developed pressure sensor processing was conceived as a generic technology. Many of the above mentioned modules can be tuned according to the specifications of the considered application. For example, the gap depth and the SiGe structural layer thickness can be easily scalable. Also the properties of the poly-SiGe sensing layer (for piezoresistive sensors) can be controlled by the implantation and annealing conditions. Moreover, this technology allows for both piezoresistive and capacitive pressure sensors to be fabricated simultaneously.

## 4.2 Pressure Sensor Schematic Process Flow

Poly-SiGe pressure sensors of different areas ($200 \times 200$, $250 \times 250$, $300 \times 300$ and $350 \times 175\,\mu m^2$) were fabricated using surface micromachining. Figures 4.4 and 4.6 give an overview of the pressure sensor schematic process flow. For simplicity only the parts that are relevant for the piezoresistive pressure sensor are drawn. This chapter deals exclusively with the processing of the stand-alone pressure sensors, starting at the metal electrode. The fabrication of a CMOS-integrated pressure sensor, including the CMOS-MEMS via module, will be explained in Chap. 7.

Figure 4.4 shows the first part of the pressure sensor fabrication process. This part includes the metal and SiGe electrodes deposition and patterning, the MEMS via formation and the deposition and patterning of the sacrificial oxide to define the anchors. All these modules are part of the standard SiGe MEMS platform, and were already reported in [8] and [9] for the fabrication of SiGe thin-film packages and SiGe resonators, respectively.

A standard 8-in-diameter Si (100) wafer is used as starting substrate. We first deposit $1\,\mu m$ of High Density Plasma (HDP) Si-oxide to electrically isolate the

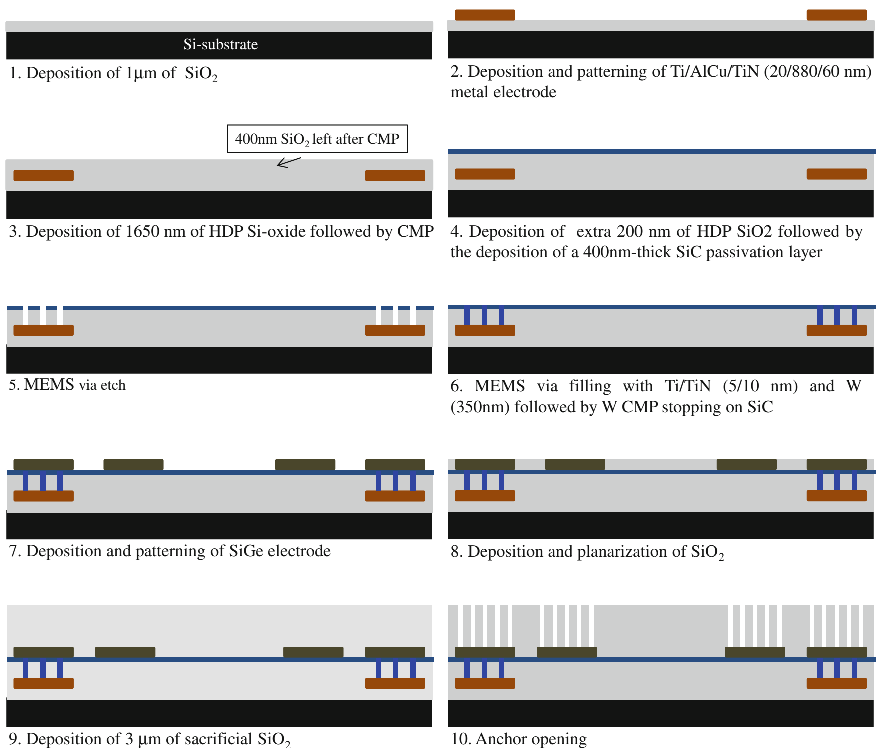


**Fig. 4.4** Part I of the process flow of the fabricated pressure sensor. Note that scales are distorted

metal electrodes from the conductive Si-substrate. A metal stack composed by 5 nm of Ti, 880 nm of AlCu (0.5 wt %) and 60 nm of TiN is deposited and patterned next to define the metal electrodes. In the pressure sensor design, the metal electrodes only appear in the bondpad regions and below the membranes of those sensors designed to be used both as piezoresistive and capacitive pressure sensors. After the metal electrode patterning, a 1,650 nm-thick HDP Si-oxide layer is deposited, followed by the backside deposition of a 200 nm-thick Si-nitride layer for stress compensation. A chemical mechanical polishing (CMP) step is then performed to obtain a planarized surface. This CMP operation is time-controlled, with weight measurements performed right before and after to target for a thickness of ~400 nm of remaining oxide layer on top of the metal electrodes. 200 nm extra HDP Si-oxide is then deposited, followed by the deposition of the 400 nm-thick SiC passivation layer. The purpose of this SiC layer, as explained above, is to protect the metal electrodes during the aggressive vHF MEMS release process. Two annealing steps of 30 min at a temperature of 455 °C are performed right before and after the SiC deposition. The purpose of the pre-deposition annealing step before the SiC protection layer deposition is to ensure a proper outgassing of the underlying layers. As the SiC is very hermetic, if the underlying layers still outgas after SiC deposition, bubbles below the SiC could be formed. The post-deposition annealing step is to promote densification of the SiC passivation layer, eliminating possible defect paths in the SiC that could allow infiltration of vHF during the release process.

The MEMS vias are then opened to provide electrical connection, through the SiC and Si-oxide layers, to the underlying metal electrodes (Fig. 4.5a). These MEMS vias are square in shape with a fixed dimension of $0.5 \times 0.5\ \mu m^2$ and a maximum spacing of 10 μm. A thin Ti/TiN (15/10 nm) layer followed by 350 nm of tungsten (W) is then deposited to fill the vias. An 18 nm Argon (Ar) pre-sputtering is performed before the Ti/TiN filling to remove any possible native oxide that could degrade, or even kill, the future electrical connection. To avoid blistering of the W, an anneal step (30 min at 455 °C) is done in between the Ti/TiN and the W depositions. After via filling, a CMP step is performed to remove the W everywhere except in the vias.

A 400 nm-thick highly boron doped ($B \sim 1 \times 10^{21} cm^{-3}$) SiGe layer is deposited and patterned next to define the SiGe bottom electrodes. In the pressure sensor design these SiGe electrodes are defined in the bondpad regions, below the membrane anchors and, in the case of capacitive sensors, below the membrane itself (bottom electrode). This electrode is later embedded in an 800 nm-thick layer of sacrificial oxide followed by CMP with stop on the SiGe electrode to realize a flat topography (Fig. 4.5b). This CMP step to planarize the $SiO_2$ layer is necessary due to the topography created by the SiGe electrodes when $SiO_2$ is grown over them. This topography can limit the resolution of the following litho steps and makes subsequent deposition/etch steps more challenging. During the pressure sensor fabrication process several CMP steps are included to ensure a planarized surface, avoiding unwanted topography.

The bulk of the sacrificial oxide layer is deposited next, on top of the planarized SiGe electrode. The thickness of this sacrificial layer will determine the gap between the free standing membrane and the bottom electrode, as depicted in Fig. 4.1. In this

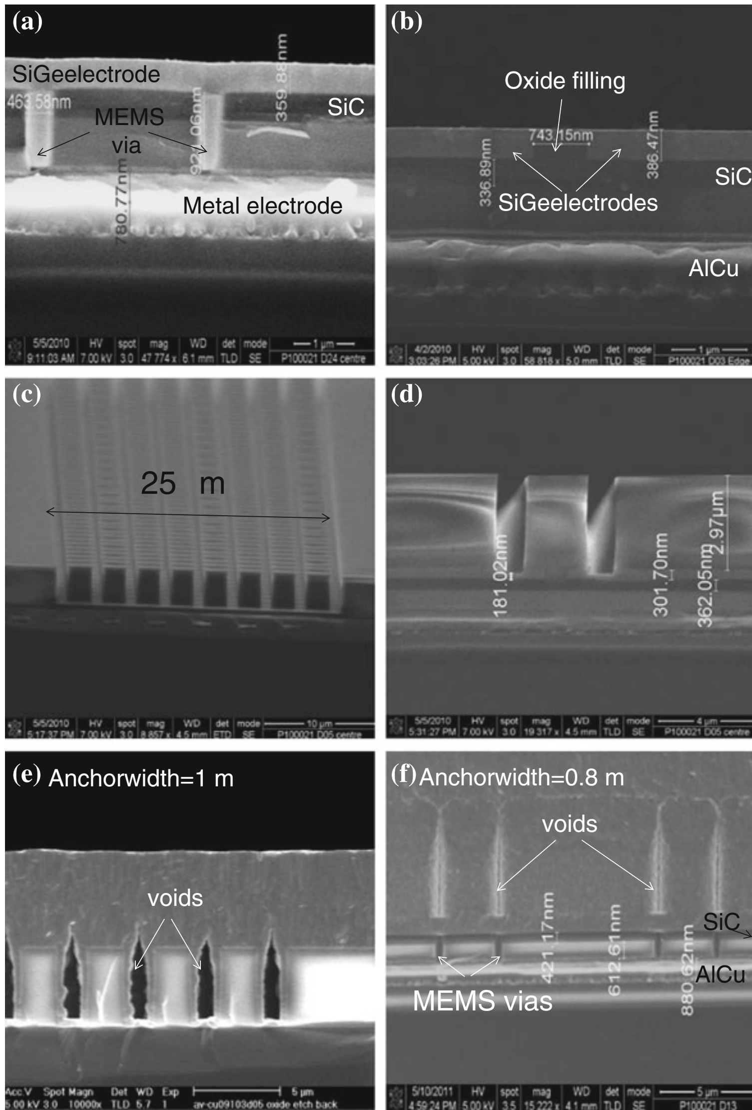


**Fig. 4.5** Cross-section pictures illustrating different steps in the pressure sensor process flow. **a** SiGe and metal electrodes with SiC passivation layer in between. The MEMS via connections are also visible. **b** SiGe electrodes embedded in sacrificial oxide after CMP. **c** and **d** show the anchor trenches etched in the sacrificial oxide. During the oxide etch the SiGe electrode layer underneath is attacked. Anchor filling by SiGe for a width of **e** 1 µm and **f** 0.8 µm

work, the nominal thickness of the HDP Si-oxide layer used as sacrificial material is 3 µm, although for one wafer a 1 µm-thick HDP Si-oxide layer was used instead to improve the performance of the capacitive sensors (see Chap. 6).

To define the anchor region, trenches are opened in the sacrificial Si-oxide by physical plasma etch using Ar as etch gas (Fig. 4.5c and d). As explained in Sect. 4.1, these anchors serve two purposes: they form the electrical contact to the lower electrodes and they anchor the structural layer to the bulk of the wafer. In the pressure sensor design, the total anchor region surrounding each membrane is 25 μm. Anchor trenches are also etched in the bondpad regions. Initially, an anchor width of 1 μm was used. However, the SiGe filling of these trenches during the structural layer deposition was not perfect, leaving voids as can be seen in Fig. 4.5e. For this reason the anchor width was reduced to 0.8 μm, resulting in a nicer SiGe filling (Fig. 4.5f).

All the processing steps explained up till now are part of the standard imec SiGe MEMS platform. Figure 4.6 shows the second part of the pressure sensor process flow, which includes pressure sensor specific modules like piezoresistors and metal interconnects.

The SiGe structural layer is now deposited. An annealing step of 30 min at 455 °C is performed before the SiGe deposition to ensure a proper outgassing of the underlying layers, avoiding the formation of bubbles later on. A thin Ti/TiN (5/10 nm) is deposited first to improve adhesion and avoid delamination; it also lowers the contact resistance between the SiGe electrodes and the SiGe structural layer [10]. The B-doped poly-SiGe structural layer is then deposited at 460 °C chuck temperature (450 °C wafer temperature) by a combination of CVD and PECVD (Plasma Enhanced CVD). The CVD and PECVD depositions are both performed in an Applied Materials PECVD Centura CxZ chamber. The silicon gas source is pure silane, whereas 10 % germane in hydrogen has been used as the germanium gas source. The boron gas source is 1 % diborane in hydrogen. Table 4.1 lists the deposition conditions. During the two PECVD depositions, an extra $H_2$ flow is included since hydrogen is shown to be beneficial for the crystallinity and uniformity of the deposited layer [11].

The PECVD SiGe layer is deposited on top of a polycrystalline CVD SiGe seed layer (∼400 nm-thick); the CVD layer forms a crystalline seed for the PECVD SiGe growth [12] and it also refills the anchor trenches, thanks to the good step coverage of the CVD process. The maximum thickness of PECVD SiGe that can be deposited before a chamber clean is required is ∼2 μm. If a thicker layer is needed, PECVD layers can be stacked until the final thickness is reached. In this case, a 30 s $CF_4$ clean is performed before each extra PECVD deposition to remove any unwanted oxide at the PECVD/PECVD interfaces [13]. The stack to achieve the 4 μm thick structural layer used in this work is composed by a 400 nm-CVD seed layer +1.6 μm PECVD +2 μm PECVD SiGe layer. The total deposition time for the SiGe structural layer is ∼40 min. The Ge concentration, as determined by Rutherford Backscattering , is ∼75 % for the CVD layer [14]. The obtained poly-SiGe layer exhibited mechanical and electrical properties suitable for MEMS applications [8]: a tensile residual stress around 70 MPa, a stress gradient below $10^{-5}/\mu m$ and an electrical resistivity below 4 mΩ· cm. The Young's modulus, obtained by nanoindentation, is 147 GPa.

After the SiGe structural layer deposition, a CMP (Chemical Mechanical Polishing) process is applied to planarize and smooth the poly-SiGe membrane surface. A flat smooth top surface is important to facilitate the adhesion of the future

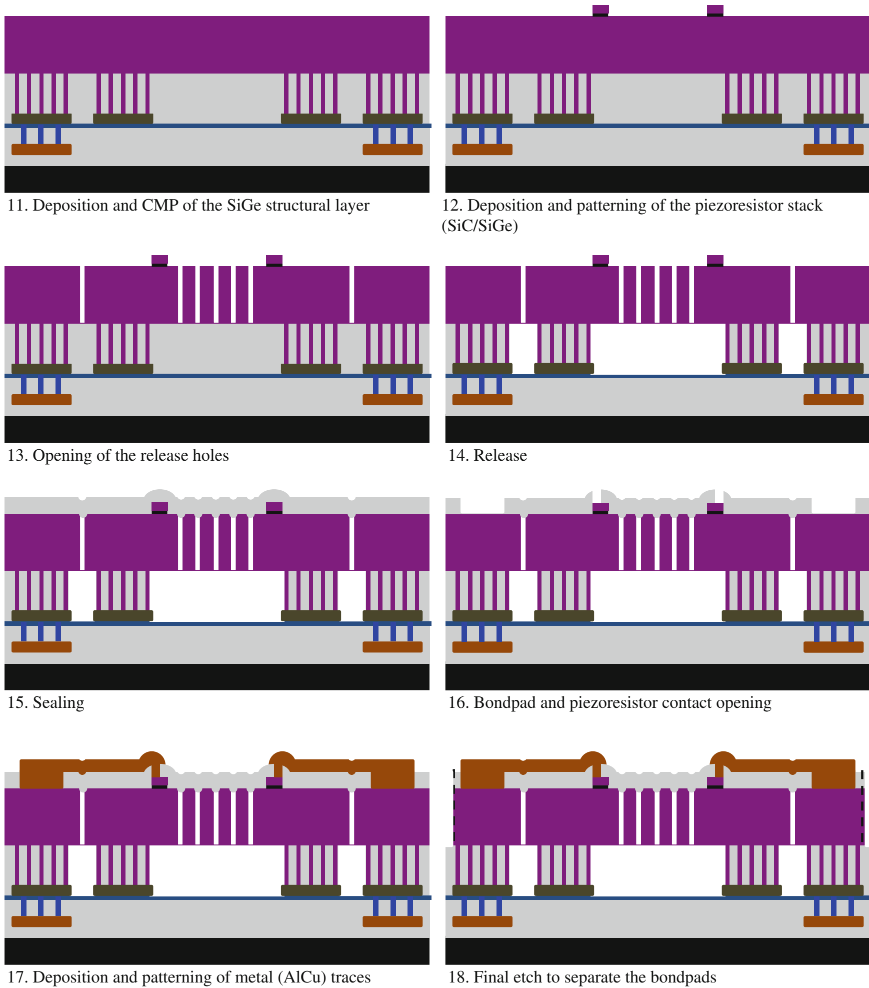


**Fig. 4.6** Part II of the pressure sensor process flow. Note that scales are distorted

piezoresistive layers; moreover unwanted topography or roughness can limit the resolution of the following litho steps and makes subsequent deposition/etch steps more challenging. This CMP is also partially responsible for the fact that the final poly-SiGe thickness (∼3.5 μm) is slightly lower than the targeted 4 μm.

The piezoresistor stack is deposited next. First a thin (100 nm) SiC layer is used as isolation layer between the SiGe membrane and the SiGe piezoresistors. Then a 200 nm-thick CVD undoped poly-SiGe layer with a Ge content of 77 % (determined by RBS) is deposited as piezoresistive layer. This poly-SiGe piezoresistive layer is deposited at 460 °C chuck temperature (450 °C wafer temperature) in the same tool used for the poly-SiGe structural layer. The deposition time is ∼12 min.

**Table 4.1** Deposition conditions for the 4 μm-thick (CVD + PECVD + PECVD) poly-SiGe structural layer used in this work. The conditions for the CF4 clean performed before the second PECVD deposition are also listed

| | **Base layer** | | **$CF_4$-interclean** | **$2^{nd}$ PECVD layer** |
|---|---|---|---|---|
| | **CVD** | **PECVD** | | |
| Thickness | 400 nm | 1.6 μm | – | 2 μm |
| Time (sec) | 810 | 610 | 30 | 780 |
| Pressure (Torr) | 4.3 | 5.4 | 1 | 5.4 |
| $H_2$ (sccm) | 0 | 450 | 0 | 450 |
| $CF_4$ (sccm) | 0 | 0 | 560 | 0 |
| $SiH_4$ / $GeH_4$ | 0.9 | 0.4545 | 0 | 0.4545 |
| $B_2H_6$ (sccm) | 10 | 50 | 0 | 50 |

The electrical and piezoresistive properties of this layer for different doping concentrations and annealing conditions were already reported in Chap. 2 (layer 4 in Table 2.1).

After deposition, the poly-SiGe film was doped through ion implantation of boron at 35 keV with a dosage of $2 \times 10^{14}$ cm$^{-2}$ (concentration $1 \times 10^{19}$ cm$^{-3}$). This boron concentration resulted in the highest gauge factor (Chap. 2) and was therefore the one selected for the piezoresistive layer in the pressure sensor. After implantation, the films are annealed in a conventional furnace at 455 °C. The selected annealing time was 30 min, although the optimum annealing time for maximum gauge factor is 1 h (see Chap. 2). Delamination of the piezoresistor layers and the SiGe structural layer was observed after sinter for 1h (Fig. 4.7a). This delamination might be due to the stresses generated in the layers due to the thermal budget; also outgassing of the underlying layers was proposed as explanation. To limit this delamination issue in this work, it was decided to limit the annealing time to 30 min; also, the annealing step was moved after piezoresistor patterning. In this way delamination of the piezoresistor layers is avoided, although bubbles in the SiGe structural layer (especially in the unpatterned region at the edge of the wafers) are still observed (Fig. 4.7b). In the future, extra annealing steps could be included before and after the 100 nm-thick SiC isolation layer to improve adhesion of the piezoresistors and allow a longer doping activation anneal.

After litho, the piezoresistor stack is patterned in two consecutive dry etch operations; first, the SiGe piezoresistive layer is etched, and then the SiC isolation layer is also etched away, remaining only below the piezoresistors. In this way the effect of this SiC isolation layer in the sensor membrane response is minimized. During this SiC etch, there is an overetch (∼100 nm) of the underlying SiGe structural layer (Fig. 4.8). The poly-SiGe structural layer is then patterned and plasma-etched in order to open the release holes. A symmetrical pattern of square release holes of nominally $1 \times 1 \mu m^2$ with a maximum spacing of 9.5 μm was used (Fig. 4.3). The final size of the release holes after etch is $\sim 1.2 \times 1.2 \mu m^2$ (Fig. 4.9).

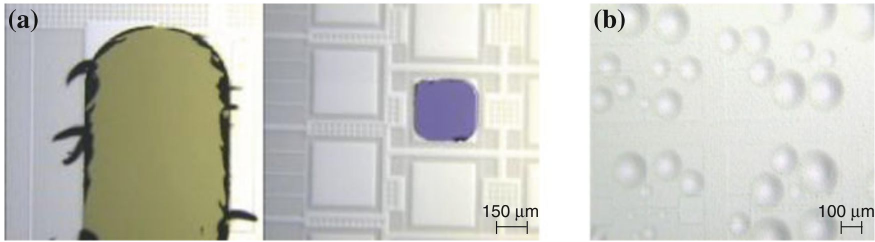


**Fig. 4.7** Microscope pictures after piezoresistor annealing. In **a** the annealing step is performed before piezoresistor patterning while in **b**, it is performed afterwards. In **a** delamination of the piezoresistor layers and structural layer is observed. On the *right picture* a pressure sensor membrane is gone. In **b** *small bubbles* in the structural layer, especially at the edge of the wafers, can be observed

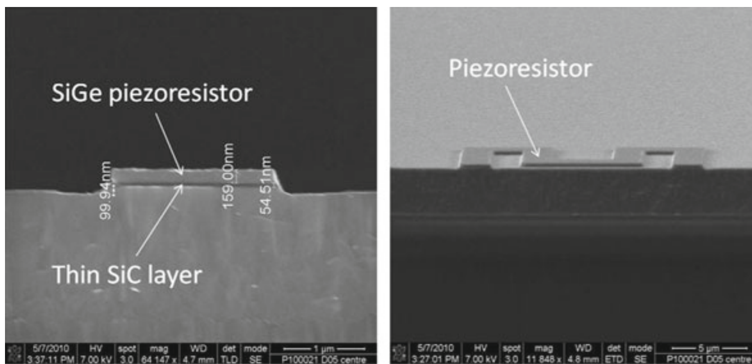


**Fig. 4.8** Piezoresistor stack (SiC + SiGe) patterning. Around 100 nm of SiGe membrane is consumed during piezoresistor etch

All sacrificial oxide inside the cavities is removed by vHF on a Primaxx Clean Etch Technology (CET) tool. To avoid stiction during the release, AvHF (Anhydrous Vapor HF) together with ethanol vapor [15] is used to etch the sacrifical oxide. After release, the membranes are sealed with Si-oxide (Fig. 4.10b). The sealing oxide is then opened using a dry etch process to create contact vias on top of the piezoresistors and bondpads (Fig. 4.10c). In the sensor layout two masks were included for this via etch: one mask to pattern the contacts on top of the piezoresistors (CWPIEZO) and a second mask to open the bondpads (MEMPASS). If only stand-alone pressure sensors are desired, only the contacts above the piezoresistors need to be opened. For CMOS-integrated and/or capacitive pressure sensors the opening of the bondpads is also necessary. In this case both exposures (CWPIEZO + MEMPASS) can be performed together in the same litho operation.

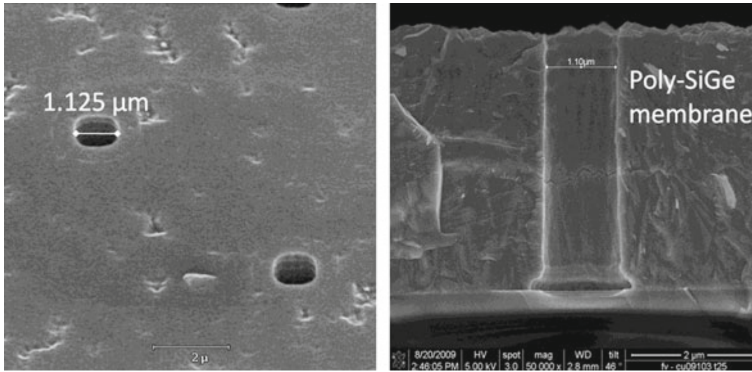


**Fig. 4.9** Top and cross-section SEM pictures of a perforated membrane before release. The *holes* size after etch is slightly bigger than the printed dimension ($1 \times 1\,\mu m^2$). In the picture on the right the interface between the two PECVD SiGe layers is visible. Also an overetch "pocket" at the oxide interface can be observed

A Ti/AlCu (0.5 wt%)/TiN metal stack was then deposited and patterned to contact the piezoresistors. Note that this is the same metal stack used to define the metal electrodes at the beginning of the flow. The inital Ti layer helps to fill the contacts thanks to its great conformality. The final TiN layer is included to facilitate lithography. From Fig. 4.10d we can see that the metal stack does not fill the piezoresistor contacts nicely. This problem will be analyzed in detail in Sect. 4.3.5.

After patterning the metal interconnects, a final lithography step operation, followed by the etching of the sealing Si-oxide and the SiGe membrane, is performed to pattern the sensors, separating the cavities from one another and isolating the bondpads. Figure 4.10e shows a sensor membrane and two bondpads after this final etch. The AlCu metal traces connecting the bondpads with the piezoresistors remain "hanging" over the trench separating membrane and bondpad. It is important to mention that these 1.5 µm-wide isolation trenches are etched at the same time as the release holes and they remain protected by resist during this final etch. Therefore these trenches remain filled with sealing oxide, which acts as a support for the metal traces, preventing them from breaking. Note that, as the vHF during the release step only etched the sacrificial $SiO_2$ below the membranes and below the small, a ring of sacrificial $SiO_2$ remains surrounding each sensor, increasing the robustness of the membranes (Fig. 4.10f). Note also that, if only stand-alone piezoresistive sensors are sought, this final litho/etch operation is unnecessary since the bondpads are not opened and therefore they are not electrically connected.

## 4.3 Process Developments and Challenges

During the fabrication of the pressure sensor a number of challenges were faced, like the bad piezoresistor contact discussed before. Moreover some processing steps, that are specific for a piezoresistive pressure sensor and therefore not part of imec's SiGe

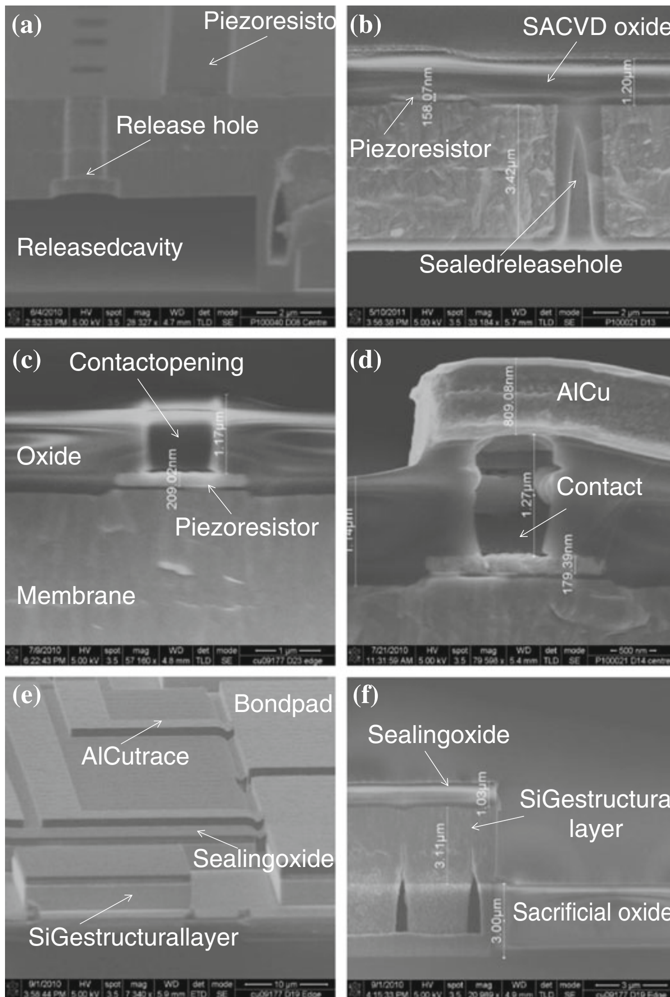


**Fig. 4.10** Cross-section pictures illustrating different process steps in the second part of the pressure sensor fabrication flow. **a** Membrane release. Note that the piezoresistors, exposed during the release in vHF, remain unattacked. **b** Sealing of the released membranes with oxide. A piezoresistor embedded in sealing oxide is visible. **c** Etching of the sealing oxide to contact the piezoresistors. **d** Contact filling by the metal stack deposited to connect the piezoresistors. **e** and **f** Patterning of the sealing oxide and SiGe membrane to isolate bondpads and seaparate sensors from one another. Note that a ring of sacrificial oxide remains surrounding the structures

MEMS platform, needed to be developed in the frame of this work. These challenges and process developments are summarized in this section.

### 4.3.1 Piezoresistive Layer

A key part of this thesis was the development of a SiGe layer deposited at temperatures below 460 °C with good piezoresistive properties to be used as sensing layer in the pressure sensor. The existing SiGe layers in imec's MEMS platform, used for example as electrodes or structural layers, are deposited *in situ* doped with a high concentration of boron ($> 1 \times 10^{20} cm^{-3}$). At such high dopings, semiconductors exhibit metallic behavior with limited piezoresistive effect [16]. The solution was to develop a recipe to deposit SiGe undoped while keeping the low deposition temperature of the standard SiGe layers. The developed recipe deposits a SiGe layer with a thickness of around 220 nm composed by 20 nm of undoped PECVD SiGe plus 200 nm of undoped CVD SiGe.

The layer exhibits a high compressive stress ($\sim -150$ MPa) after deposition, but becomes tensile after annealing. The layer can be then boron doped through implantation with the appropriate dose depending on the required electrical properties. The mechanical and electrical properties of this layer (layer 4 in Table 2.1) were already reported in Chap. 2.

### 4.3.2 Piezoresistor Patterning

The piezoresistors used in the fabricated pressure sensor are composed by two layers. The first layer is a 100 nm-thick SiC used as isolation between the SiGe piezoresistors and the SiGe membrane. The real thickness of this layer after deposition is slightly smaller, in the range of 60–70 nm. The second layer is the poly-SiGe sensing layer described above. To pattern the piezoresistors, these two layers need to be etched sequentially. A new etching recipe was developed specifically for this purpose. In the developed recipe, the patterning of the piezoresistors is done sequentially using two dry etching processes in two different tools: first the etch of the SiGe in a LAM Domino 2,300 system, followed by the etch of the SiC isolation layer in a LAM Alliance (A6) 9400 PTX Poly/Nitride Etch System.

Initially, an existing recipe for the dry etch of 200 nm of SiGe, using a hydrogen bromide (HBr) gas-based chemistry, was tried to etch the SiGe piezoresistive layer. After inspection it was found that the SiGe was not completely etched in the open areas (Fig. 4.11a). The recipe was then modified to target 50 % SiGe overetch. Figure 4.11b shows the results: the piezoresistor is perfectly defined, with vertical walls, while the SiGe is completely gone everywhere else. The initial recipe also included an *in situ* dry strip that was removed in the modified recipe since the strip has to be done after the second etch (SiC) is done. Moreover, this in situ strip proved to be not very efficient in removing the resist and the polymers formed during etch (Fig. 4.11a).

After the patterning of the SiGe piezoresistive layer is done, the SiC etch takes place. The SiC is patterned using a $CHF_3/CF_4$ plasma. Figure 4.12 shows

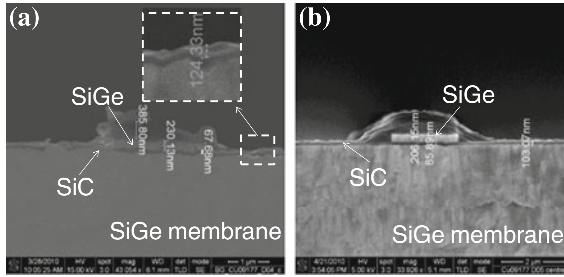


**Fig. 4.11** Cross-section pictures illustrating the patterning of the SiGe piezoresistive layer. **a** SiGe etch using initial recipe (with an *in situ* strip included). A zoom in showing remaining SiGe in open areas is included. **b** Result after modified recipe targeting 50 % SiGe overetch and without *in situ* strip

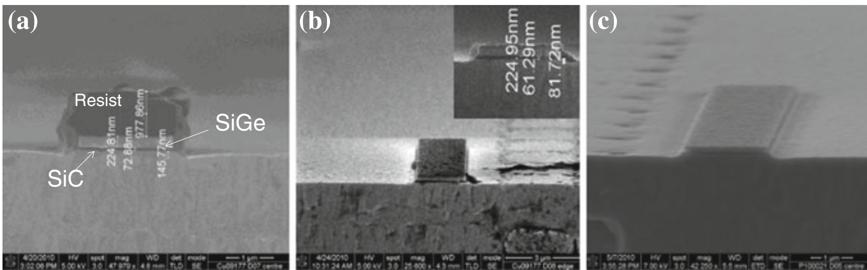


**Fig. 4.12** Cross-section pictures after **a** 120" SiC etch (without strip), **b** 75" SiC etch (plus strip) and **c** 50" SiC etch (also plus strip). In **c** a side attack in the SiC/SiGe (piezoresistor) interface can be observed

cross-section pictures after SiC etch for 120", 75" and 50". In all cases the SiC is completely etched everywhere except below the SiGe piezoresistors. With the initial etch time of 150", around 150 nm of the SiGe membrane is consumed (Fig. 4.12a). To limit this overetch, the etch time was reduced to 75". In this way the thickness of the consumed SiGe is reduced below 100 nm, while still successfully etching the SiC isolation layer (Fig. 4.12b). However, the top surface of the SiGe piezoresistors gives an impression of being "burnt" (probably due to the excessive formation of polymers during the etch process). In an attempt to avoid this issue, the SiC etch time was further reduced to 50", which resulted in an efficient and "clean" etch of the SiC layer with limited SiGe membrane consumption (Figs. 4.12c and 4.10). This is finally the etch time used in the pressure sensor flow for the patterning of the SiC isolation. The strip is performed in two consecutive steps: first a dry strip using an oxygen plasma and second a wet strip based on diluted buffer HF (DBHF).

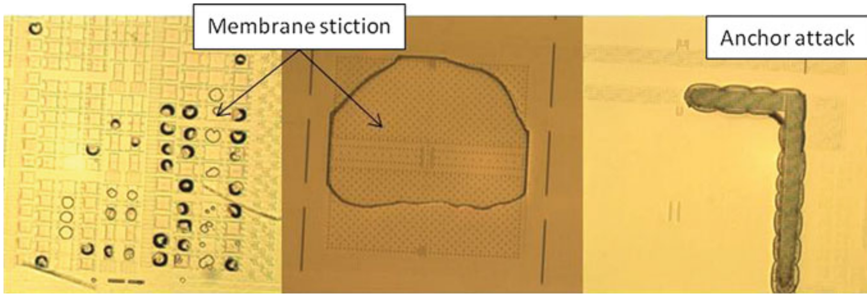


**Fig. 4.13** Microscope pictures of membranes released in one step of 80 min. Issues with membrane stiction and anchor attack are observed on the wafer

### *4.3.3 Release*

During the release process all the sacrificial oxide inside the cavities is removed. Vapor HF (vHF) is the chosen etchant, since it is very selective to SiGe and has a high etch rate for $SiO_2$. As already mentioned in Sect. 4.2, to avoid stiction during the release, AvHF (Anhydrous Vapor HF) together with ethanol vapor [15] is used to etch the sacrifical oxide. The release process is carried out on a Primaxx Clean Etch Technology (CET) tool. In a first attempt, the membranes were released in one step of 80 min. However, as can be seen in Fig. 4.13, this release recipe resulted in membrane stiction (probably due to excess of water, a byproduct of the etch process) and anchor attack.

To avoid these issues it was decided to divide the release process in eight steps instead of using only one step, as before. Breaking down the release time in steps has several advantages, the most important being:

- Reduction of the etch rate, making the recipe less aggressive and therefore limiting possible attacks of the anchor region, layer interfaces and the SiC CMOS protection layer.
- Reduced chance for stiction as water, which is a byproduct of the etching process, can be removed easily when the release time is broken in steps.

Two different recipes were investigated: 8 steps of 6 min and 8 steps of 8 min. To evaluate the release process, microscope inspection together with the so-called "tape test" was used. In this test, a standard adhesive tape is applied to an area of the wafer containing the released membranes. If the membranes are successfully released they will be pulled off by the tape when this one is removed. Figure 4.14 shows the results. From Fig. 4.14a we can conclude that 6 min per step is not enough to completely etch all the sacrificial oxide below the membrane. After the membranes are pulled off during the tape test, some oxide traces, in the form of columns, remain on the bottom of the cavities. By increasing the etch time to 8 min per step (Fig. 4.14b) all

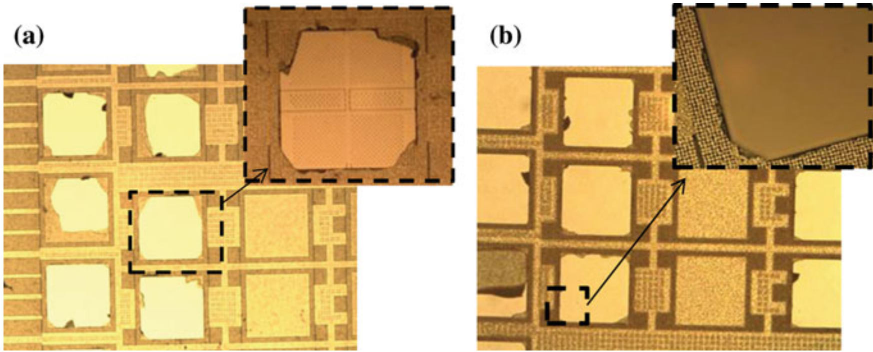


**Fig. 4.14** Microscope pictures after tape test for membranes released in 8 steps of 6 min (**a**) and 8 steps of 8 min (**b**). Oxide traces below the pulled off membranes are visible in (**a**), while in (**b**) the cavity *bottom* appears clean.

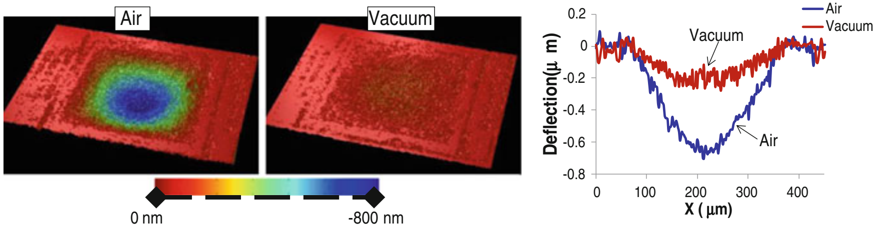


**Fig. 4.15** Optical measurements of the deflection of a 300 x 300 $\mu m^2$ membrane sealed with oxide. Deflection is measured in air (1 bar) and vacuum (0.25 bar). The difference in deflection indicates that the membrane is sealed

the oxide is completely removed, without observing issues with membrane stiction or anchor attack anywhere on the wafer. In the pressure sensor fabrication process, the membranes are released in 8 steps of 8 min.

### *4.3.4 Sealing*

The sealing process is one of the most important steps in the fabrication of a pressure sensor. For this reason a whole chapter of this thesis is dedicated to it. One of the most important requirements a sealing layer must fulfill is to provide a hermetic sealing of the cavity with a stable, preferably low, sealed-in pressure. In this work, several sealing layers were investigated (see Chap. 5). Finally SACVD (Sub-Atmospheric CVD) Si-oxide was the chosen sealing material.

It was found that 900 nm of SACVD Si-oxide was already sufficient to seal the membranes. However, for safety reasons, considering that some oxide could be consumed in following etching steps, a thickness of 1.2 μm was finally selected.

Figure 4.10b already showed a cross-section picture of a membrane sealed with a 1.2 μm-thick SACVD Si-oxide layer. This oxide sealing layer is deposited in two steps of 600 + 600 nm. To check if the membranes are successfully sealed, the membrane deflection under two different external pressures (air and vacuum) was optically measured (Fig. 4.15). The difference in deflection indicated that the membranes are sealed. The reasons behind the selection of SACVD oxide as sealing material, together with extra information about measurement set up, hermeticity tests and sealed-in pressure, can be found in Chap. 5.

### 4.3.5 *Piezoresistor Contact*

In the developed fabrication sequence, the sealing process takes place after the poly-SiGe piezoresistors have been deposited and patterned. This means that, once the 1.2 μm-thick SACVD Si-oxide sealing layer is deposited, the poly-SiGe piezoresistors are totally embedded in oxide (Fig. 4.16a). In order to provide electrical contact to the piezoresistors, $1 \times 1\,\mu m^2$ vias were etched in the sealing oxide on top of the piezoresistors. An oxide dry etch process stopping using in SiGe was used for this purpose. The oxide dry etch process used is based on a plasma of reactive gases such as Helium (He), Argon (Ar), Oxygen ($O_2$) and Octafluorocyclobutane ($C_4F_8$). After etch, these contacts are filled with a Ti (20 nm)/AlCu (880 nm)/TiN (60 nm) metal stack deposited at 350 °C. This is the same metal stack used to define the metal electrodes at the beginning of the flow (Fig. 4.4). Before the metal deposition, a 20 nm Ar pre-sputtering is performed to remove any unwanted oxide on the SiGe piezoresistor surface. However, as illustrated in Fig. 4.16b, the AlCu filling of the vias is not good, resulting in a poor electrical contact. This bad AlCu filling is mainly due to two factors: the straight vertical side walls, a consequence of the dry etch process used, and the relatively high aspect ratio of the contact holes (they are 1.2 μm high and only 1 μm wide).

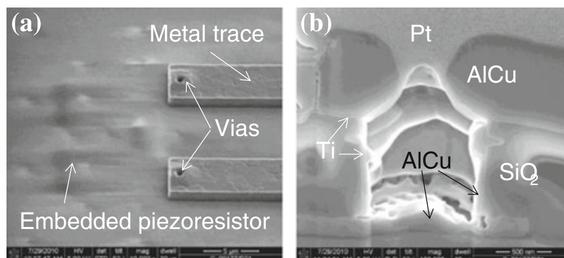


**Fig. 4.16** **a** *Top* SEM picture of a piezoresistor embedded in sealing oxide. The metal traces and contact vias are also visible. **b** FIB picture of the bad AlCu via filling. It is thanks to the thin (20 nm) Ti layer, which deposits conformally, that there is electrical connection at all. Pt is deposited during the FIB process to increase the contrast and get a sharper picture

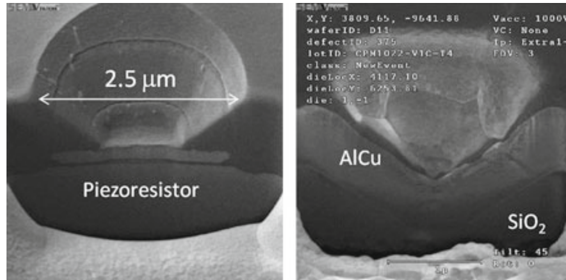


**Fig. 4.17** Results of the HDP deposition experiments: FIB pictures of a contact via before (*left*) and after (*right*) the metal deposition. The standard Ti/AlCu/TiN (20/880/60 nm) metal stack, deposited at 350 °C is used to fill the vias. After the HDP deposition plus HF wet etch, the contact walls were nicely inclined. In this condition, the AlCu can easily flow in, completely filling the contact

In order to improve the metal filling of the contacts, an experiment to try to increase the angle of the contact sidewalls was carried out: AlCu is expected to deposit better on inclined walls as compared to 90° vertical walls. In order to achieve inclined sidewalls, 50 nm of HDP Si-oxide was deposited on top of the opened vias. For the HDP Si-oxide deposition, a process with more sputtering than deposition was used. The sputtering performed during this deposition serves to clip the corners of the contact holes. After the HDP deposition, an extra sputtering of 80 s is performed. To remove the HDP oxide deposited on the SiGe inside the contacts, an oxide wet etch with HF for 5 min was performed. As can be seen from Fig. 4.17, this experiment resulted in nicely filled contacts with ∼135° inclined walls. However, a microscope inspection revealed that all the membranes were either broken or completely gone after the HDP deposition (Fig. 4.18). One possible explanation for this could be the difference in stress of the layers. HDP Si-oxide typically exhibits high compressive stress (∼−200 MPa), in contrast with the marginally tensile stress expected from the SACVD Si-oxide sealed poly-SiGe membranes (see Table 5.3). Moreover, the HDP deposition occurs at a high temperature (400 °C), which can result in high induced

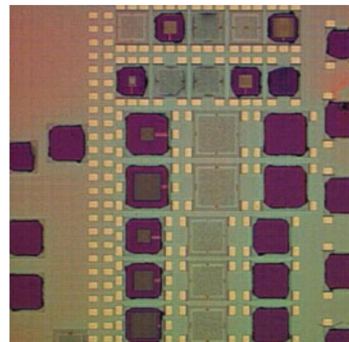

**Fig. 4.18** Delamination after HDP deposition. All the pressure sensor membranes are gone or broken. The only remaining membranes visible on the picture are those of the "dummy" (non-released) sensors

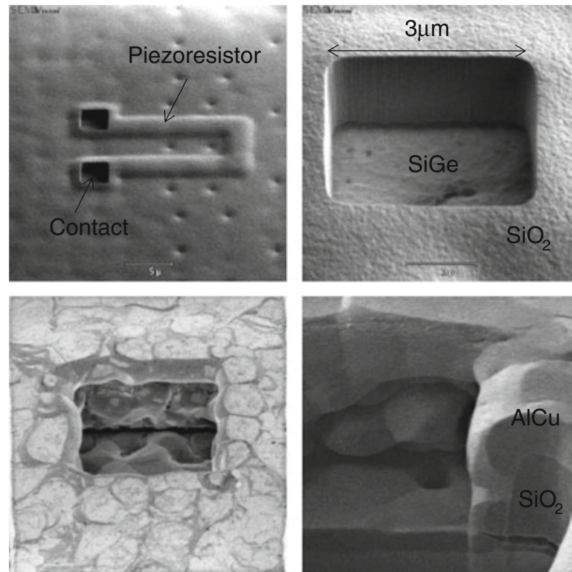


**Fig. 4.19** Top: pictures of the new $3\times3\,\mu m^2$ contacts after oxide etch. *Bottom*: *Top* (*left*) and Cross-section (*right*) pictures of a $3\times3\,\mu m^2$ contact via filled with 500 nm AlCu. Although not yet perfect, the filling, and thus the electrical contact, is much better than with the original $1\times1\,\mu m^2$ vias

stresses due to the different thermal expansion coefficients of the layers that form the membranes.

After the failure of the above described experiment, it was decided to redesign two masks of the pressure sensor layout (specifically the mask to pattern the piezoresistors and the mask to open the vias in the oxide) in order to have larger contacts. The new contacts are $3\times3\,\mu m^2$, resulting in an improved AlCu filling. Figure 4.19 shows top and cross-section pictures of the new contacts, before and after AlCu filling. To avoid stress-related delamination issues, and since the filling was already good enough, a thinner AlCu (500 nm instead of 880 nm) was used to contact the piezoresistors. The final metal stack is thus 20 nm Ti / 500 nm AlCu, with no TiN. The only purpose of this top TiN layer is to facilitate lithography, but here dimensions are large enough such that lithography is not an issue.

## 4.4 Discussion on the Poly-SiGe Pressure Sensor Process

In this chapter, a process flow suitable for the fabrication of surface micromachined poly-SiGe piezoresistive and/or capacitive pressure sensors has been presented. Throughout the fabrication flow, the processing temperature is always kept below 460 °C to allow for post-processing on top of CMOS. Figure 4.20 shows top microscope pictures of two of the fabricated devices: a piezoresistive-only and a combined (piezoresistive and capacitive) pressure sensors. The bondpads, the four piezoresistors (as the sealing oxide is transparent) and the metal interconnects can all

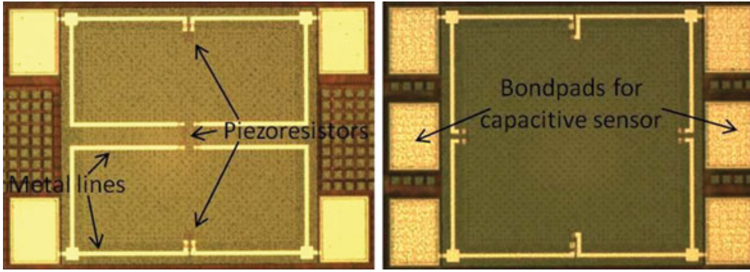


**Fig. 4.20** *Top* microscope pictures of a piezoresistive-only (*left*) and a combined piezoresistive-capactive (*right*) pressure sensor. The bondpads, piezoresistors and metal lines are visible. For the combined pressure sensor six bondpads are needed: four (in the corners) for piezoresistive measurements, and two (in the centre) for capacitive measurements

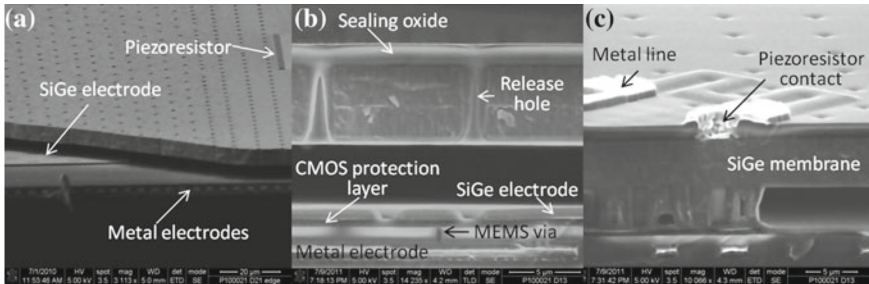


**Fig. 4.21** SEM pictures of some of the fabricated devices. **a** An unsealed combined (piezoresistive and capacitive) pressure sensor. The SiGe electrode below the membrane can be observed. **b** Cross-section picture of a finished device. The bottom components (metal and SiGe electrodes, the SiC CMOS protection layer and a MEMS via) can be observed. Two sealed release holes are also visible. In **c**, a piezoresistor covered in sealing oxide is shown, together with the two piezoresistor contacts and the AlCu interconnects

be observed. Three SEM pictures of fabricated devices are depicted in Fig. 4.21. The main components of the developed process flow are visible in these pictures; first, the bottom metal electrode (embedded in oxide), the SiC protection layer (to protect the metal electrode during the aggressive vHF MEMS release), the SiGe electrode and the tungsten-filled MEMS vias, connecting both (metal and SiGe) electrodes. Also, the poly-SiGe membrane, release holes and piezoresistorsv are clearly visible. And finally, the SACVD sealing oxide, the piezoresistor contacts and the AlCu interconnects can be seen. In Fig. 4.21b and c, the deposition of sealing oxide inside the cavity (SACVD oxide deposits conformally) can also be appreciated.

The whole process sequence requires ten lithographic masks and more than 100 operations (including depositions, litho exposures, etching and strips, annealing steps, etc). As mentioned above, in order to make the process flow CMOS-compatible, the maximum temperature allowed in these operations was 460 °C. Table 4.2 lists the operations that required the highest ($\geq$ 400 °C) temperatures.

**Table 4.2** List of the operations in the pressure sensor process flow performed at temperatures ≥ 400 °C. The total time per operation is also included. For operations that happen more than once in the flow, the total time is the sum of the times for each single operation

| Operation | Where in the process flow? | Temperature (°C) | Total time (min) |
|---|---|---|---|
| HDP Si-oxide deposition | Sacrificial oxide, electrode embedding,... | 400 | ∼15 |
| SACVD Si-oxide deposition | Sealing | 420 | 7.3 |
| SiGe deposition | Electrode, structural layer, piezoresistors | 450 | ∼60 |
| Annealing | After piezoresistor implantation, before SiGe structural layer deposition, ... | 455 | 450[a] |

[a] For a total of 5 annealing steps in the flow, each with a duration of 1.5 h (the required 30' + 1 h for warm-up and cool-down periods). A 30 min annealing step (+ 1 h for warm-up and cool-down periods) after piezoresistor implantation is considered

The processing time for these operations can also be found in this table. As reported in [1, 2], not only the temperature but also the time that the wafers must endure that high temperature play an important role in the degradation of the CMOS performance.

As can be seen from Table 4.2, the operations requiring the highest temperatures are the annealing steps and the poly-SiGe depositions. The annealing steps account for most of the highest temperature processing time. All the annealing steps in the flow are performed in a hydrogen-rich atmosphere at a temperature of 455 °C with a typical duration of 30 min. However, each annealing step is preceded by a warm-up and stabilization period (of ∼30 min), and followed by a 30 min cool-down period. Therefore, for each annealing step of 30 min, the total time the wafer is kept at 455 °C is approximately 1.5 h. These annealing steps fulfill different purposes in the process flow. For example, there is an annealing step after piezoresistor implantation to activate the boron atoms (as seen in Chap. 2, the length of this annealing step will affect the piezoresistor performance). Two annealing steps are performed right before and after the SiC protection layer deposition to promote densification. Another annealing step is also added right before the SiGe structural layer, to outgass the underlying layers, avoiding later delamination issues. In total, during the processing of the MEMS pressure sensors on top of the read-out circuit, the CMOS will withstand a maximum temperature of approximately 455 °C for ∼8.5 h. The resulting degradation in the CMOS performance is evaluated in Chap. 7.

In this chapter, also the most important process developments required for the fabrication of the pressure sensors in this work are explained. These include: the development of a poly-SiGe piezoresistive layer processed at CMOS-compatible temperatures (see Chap. 2 for more information), the piezoresistor patterning, the sealing process (with more information in Chap. 5) and the improvement of the AlCu filling of the piezoresistor contacts. Although not specifically mentioned, one

of the main issues encountered during the fabrication process was delamination. This is thought to be due to the internal stresses of the layers; moreover, the difference in thermal expansion coefficients might also lead to high temperature-induced stresses. In some cases, these stresses resulted in broken membranes, mostly the biggest ones ($300\times300$ and $250\times250\,\mu m^2$). In general, all operations performed after the membranes are sealed are more sensitive to result in broken membranes.

In the frame of this work, piezoresistive pressure sensors using a slightly different, and shorter (using only five lithopgraphic masks), process flow were also fabricated. These pressure sensors were fabricated starting at anchor level, and therefore do not include any of the bottom layers, such as metal and SiGe electrodes, SiC protection layer or MEMS vias. The piezoresistor annealing time was 2 h, instead of the 30' annealing used in the process described in this chapter. More information about the fabrication and performance of these sensors can be found in appendix B.

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# Chapter 5
# Sealing of Surface Micromachined Poly-SiGe Cavities

This chapter describes the sealing of polycrystalline SiGe (poly-SiGe) surface micromachined cavities for above-CMOS pressure sensor applications. Two different sealing techniques involving thin-film deposition are investigated: direct sealing and sealing by using an intermediate porous layer. The sealing materials studied include Si-oxide and aluminum. Both $\mu$c-SiGe and SiC are evaluated as porous layer. The maximum processing temperature is kept below 460 °C to allow for the post-processing on top of standard CMOS. Section 5.1 gives a short overview about the most common sealing methods for pressure sensors and lists the main requirements the sealing layer needs to fulfill. Section 5.2 explains the fabrication process of the test structures. The measurement set up used to characterize the deflection of the sealed membranes deflection under different applied loads is introduced in Sect. 5.3. In Sect. 5.4 the theoretical analysis of the load-deflection behavior of square membranes is introduced, and with the help of finite element simulations a model adapted to our test structures is developed. Section 5.5 gives the results of the short- and long-term hermeticity tests performed on the sealed membranes. This section also describes the use of micro-venting holes drilled using Focus Ion Beam (FIB) in some of the sealed membranes to study the behavior of the diaphragms under 0-pressure-difference. This chapter ends with a conclusion (Sect. 5.6) listing the main aspects of the different sealing techniques studied and the reasons behind the selection of SACVD (Sub-Atmospheric Chemical Vapor Deposition) oxide as sealing layer for our pressure sensor.

## 5.1 Introduction

Sealed cavities are crucial components in many micromachined applications, such as for packaging MEM components or for producing pressure sensors. For pressure sensors the sealed cavity supplies a reference for pressure measurements. In general there are two techniques for microcavity sealing: wafer bonding (used, for example,

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in silicon pressure sensors) and thin-film deposition (typically employed in surface micromachined pressure sensors).

In wafer bonding, a cap wafer (silicon, glass or ceramic) is bonded to the MEMS wafer by using either direct bonding or by bonding with an intermediate layer, creating a hermetically sealed cavity [1]. Wafer bonding techniques, even though well established and commercialized, are costly because they require a second substrate, careful alignment of the two parts, double the thickness of the chip and need a large area for the sealing frame. Moreover the high temperatures, high voltages and/or high pressures involved may affect the performance of the encapsulated device or the properties of the sensor membrane and therefore its performance.

In the second sealing technique the membrane layer is deposited on top of a sacrificial material. Access holes or channels are provided in the membrane to remove the sacrificial material and to create a cavity underneath. For release, horizontal (placed on the cavity sides) or vertical (on the membrane) access channels can be used. After release, the access holes are typically sealed by thin film deposition. Compared with wafer bonding, sealing by the deposition of a thin-film has several advantages:

1. It eliminates the need for aligning two wafers and the challenges of bonding on processed (i.e. not smooth) surfaces.
2. It reduces the topography and reduces the width of the required sealing ring, allowing for smaller devices.
3. It eliminates the need for high temperatures, pressures or voltages usually employed in wafer bonding.

Sealing of microcavities by thin-film deposition was first demonstrated by Guckel in [2], using LPCVD (Low Pressure CVD) polysilicon deposition to seal a poly-Si cavity. Since then great efforts have been made on sealing of surface micromachined cavities by CVD deposition of thin films. Besides poly-Si also LPCVD Si-nitride was used to successfully seal surface micromachined cavities [3, 4]. These CVD materials however require high deposition temperatures, typically above 700 °C, and are therefore not suitable for post processing of the MEMS above the CMOS circuitry. Different alternatives with lower process temperatures have been proposed in the last years. Liu [5] studied the use of LPCVD phosphosilicate glass (PSG) at 450 °C and PECVD (Plasma Enhanced CVD) Si-nitride at 300 °C for the sealing of poly-Si microcavities with lateral release holes. These low temperature sealing materials were however found to be inefficient since relatively thick layers were required to successfully seal the cavities. Alternatively, Al evaporation has been used to vacuum seal poly-Si cavities [6]. Recently sputter-deposited AlCu in combination with a μc-SiGe porous cover on top of the release holes was used to hermetically seal poly-SiGe cavities for thin-film packaging applications [7]. A modified version of this sealing process has been used to hermetically encapsulate SOI resonators[8].

The main requirements for pressure sensor sealing by thin film deposition can be enumerated as follows:

1. A low minimum required thickness of the sealing layer. Sealing occurs when the deposited thickness of sealing material reaches a threshold. In pressure sensor devices the sealing layer becomes an integral part of the cavity diaphragm, contributing to its overall thickness. A small threshold thickness is therefore desirable to avoid degradation of the sensor sensitivity. A thin sealing layer also leads to less bi-material effects and ensures that the average membrane properties are close to those of the preferred structural material (in our case, SiGe).
2. A low sealed-in pressure. The expansion of the gasses trapped inside the cavity with increasing temperature will degrade the temperature dependence of the pressure sensors performance. Therefore it is, in general, preferred to have a vacuum-sealed cavity for pressure sensor applications as this will minimize the trapped gas effects.
3. A low (residual) tensile stress. The residual stress of the sealing layer will contribute to the overall stress of the diaphragm, altering the sensor membrane response. In general, the higher the tensile stress in the diaphragm, the lower the membrane deflection for a certain pressure difference. A diaphragm with compressive stress will, on the other hand, deflect more, but it has the potential for buckling. A zero or marginally tensile residual stress will minimize the effect of the sealing layer.
4. The coefficient of thermal expansion (CTE) of the sealing layer should close to that of the sensor membrane since thermal shock or thermal cycling may cause membrane cracking and delamination if the materials are not matched.

For the fabrication of the pressure sensor two different approaches for the sealing of poly-SiGe cavities by thin film deposition were investigated. The first approach consists simply in direct sealing of the released cavities by deposition of different kinds of CVD (Chemical Vapor Deposition) Si-oxide or AlCu. In the second approach the sacrificial oxide release is done through an intermediate porous cover. This porous cover has two main functions: it prevents deposition of sealing material inside the cavity and it reduces the required thickness of the sealing layer. Two different materials were investigated as porous cover: SiC and μc-SiGe [9]. The use of Si-oxide, AlCu (and SiGe in the literature) for the sealing of cavities released through a porous cover was studied. The next section describes in detail the fabrication process of the sealed test structures.

## 5.2 Fabrication Process

The test structures consist of free-standing poly-SiGe membranes covering 3 μm-deep cavities. Poly-SiGe membranes with different areas (200×200, 250×250, 300×300 and 500×500 $\mu m^2$) and thicknesses (from 2 up to 8.5 μm) were fabricated. The general fabrication process for the test structures with a 3.5 μm thick membrane and sealed without intermediate porous layer is schematically illustrated in Fig. 5.1. The fabrication process for the test structures released and sealed using

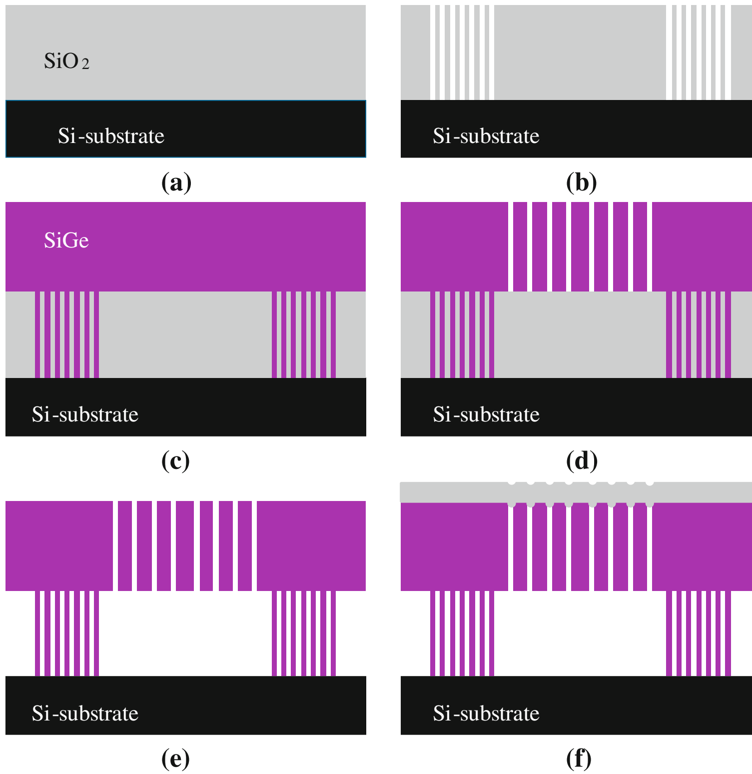


**Fig. 5.1** Schematic process flow. **a** Deposition of sacrificial oxide on a Si-wafer. **b** Patterning of the oxide to define the anchors. **c** Deposition of poly-SiGe structural layer. **d** Opening of the release holes in the membrane. **e** Etching of the sacrificial oxide by vHF. **f** Sealing

an intermediate porous cover is slightly more complex and will be explained in the corresponding subsection. Test structures with a membrane thickness different from 3.5 μm do not have anchors (see also further).

A standard 8-in-diameter Si (100) wafer is used as starting substrate. We first deposit a 3 μm-thick HDP oxide layer to be used as sacrificial material. To define the anchor region trenches were etched in the sacrificial oxide, stopping in the underlying Si substrate, and filled with poly-SiGe. The chosen anchor design consists of crossing vertical and horizontal anchor lanes, as depicted in Fig. 5.2. The total anchor region surrounding each membrane is 25 μm for all the test structures. However only the 3.5 μm-thick membranes had patterned anchors. For the rest of membranes the SiGe structural layer is deposited over unpatterned oxide (see Table 5.1).

The poly-SiGe structural layer was then deposited at 460°C chuck temperature (450 °C wafer temperature) in an Applied Materials (AMAT) PECVD CxZ chamber, mounted on an AMAT Centura Giga-Fill SACVD platform. All the layers, except for the thinner membranes, were deposited by a combination of CVD and PECVD

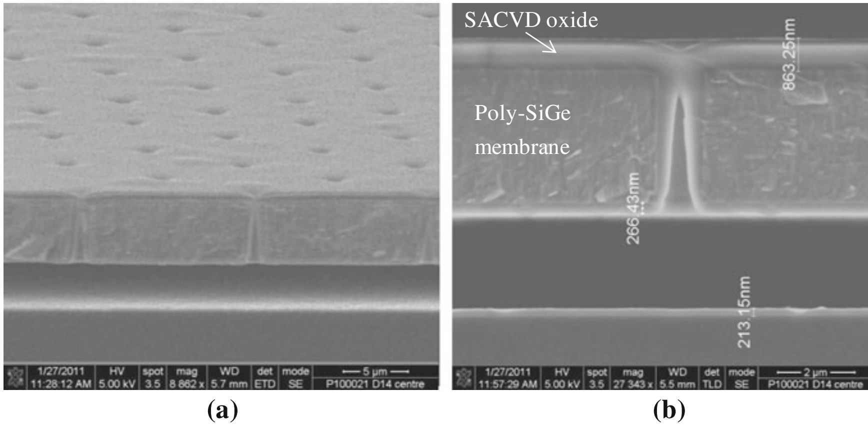


**Fig. 5.2** **a** *Top* and **b** Cross-section SEM picture of a poly-SiGe membrane sealed with SACVD. During sealing with 900nm SACVD Si-oxide, ~270 nm of oxide is deposited on the inner side of the membrane while ~220 nm of oxide is deposited at the *bottom* of the cavity

**Table 5.1** Process parameters for the different sealing methods considered

| Sealing technique | Sealing material | SiGe membrane thickness (μm) | Temp. (°C) | Pressure (kPa) | Anchor |
|---|---|---|---|---|---|
| Direct sealing | SACVD Si-oxide | 3.5 | 420 | 60 | Yes |
| | HDP Si-oxide | 3.5 | ~400 | NA | Yes |
| | PECVD Si-oxide | 3.5 | 400 | 0.35 | Yes |
| | AlCu | 8.5 | 350 | 0.001 | No |
| Porous layer | HDP Si-oxide | 3.5 | 400 | NA | Yes |
| | AlCu | 2 | 350 | 0.001 | No |

The SiGe membrane thickness for the corresponding test structure employed is also indicated

B-doped SiGe depositions with 30 seconds $CF_4$ clean at the PECVD/PECVD interfaces [10], similar as the poly-SiGe structural layer in the pressure sensor fabrication process (Chap. 4). The silicon gas source is pure silane, whereas 10% germane in hydrogen has been used as the germanium gas source. Three different poly-SiGe thicknesses are considered in this study. After deposition, a CMP (Chemical Mechanical Polishing) process is applied to planarize and smooth the poly-SiGe membrane surface. This CMP step was not included during the processing of the 2 μm-thick membranes. The final poly-SiGe stack build-up and thickness (estimated from cross-section pictures) is:

- For a 2 μm thick-membrane: a 2 μm thick PECVD SiGe layer without preceding crystalline CVD seed layer.
- For a 3.5 μm thick-membrane: a stack of a thin (~400nm) CVD SiGe seed layer and 2 PECVD SiGe layers.
- For a 8.5 μm thick-membrane: a stack of a thin CVD SiGe seed layer and 5 PECVD SiGe layers.

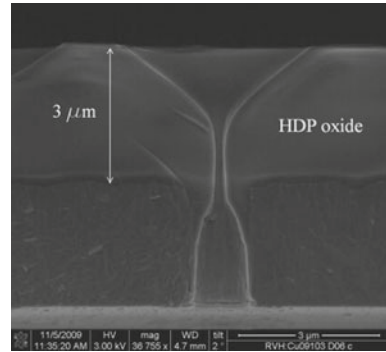


**Fig. 5.3** Sealing of a release hole with HDP oxide. A thickness of 3 μm is not enough to completely close the hole.

It is important to clarify that not all the test structures here described were fabricated specifically for the development of the pressure sensor process flow. The test structures with 2 μm thick or 8.5μm thick membranes were intended for the development of the packaging flow (work described in [11]). Hence the different membrane thicknesses and deposition processes.

After deposition, the poly-SiGe structural layer was patterned and plasma-etched to open the release holes. A symmetrical pattern of square release holes of $1 \times 1$ μm$^2$ with a maximum spacing of 9.5 μm was used (see Fig. 5.3). The final size of the release holes after etch is $\sim 1.2 \times 1.2$ μm$^2$. All sacrificial oxide inside the cavities is removed by a combination of anhydrous vapor HF (AVHF) and ethanol vapor on a Primaxx CET tool. More information about the release process can be found in Chap. 4. After release the membranes are sealed. Table 5.1 contains the main process parameters for the different sealing materials considered.

## 5.3 Direct Sealing

### *5.3.1 Sealing with Si-Oxide*

Si-oxide is an interesting sealing material for piezoresistive pressure sensor applications as it can be used simultanously as an isolation layer between membrane and piezoresistors. One drawback, however, is that oxide has a typical CTE ten times smaller than that of the poly-SiGe membrane (0.5 ppm/°C versus the 5 ppm/°C for the SiGe). This CTE mismatch may give rise to severe thermal stresses during the manufacturing of the pressure sensor and will compromise the temperature stability of the sensor.

Three different kinds of CVD (Chemical Vapor Deposition) oxide were considered as sealing layer: SACVD (Sub-Atmospheric CVD) Si-oxide, HDP (High Density Plasma) Si-oxide and PECVD (Plasma-Enhanced CVD) Si-oxide. In a CVD chamber conformal deposition occurs: the material is deposited on the top and bottom surfaces

of the diaphragm, the substrate and on the sidewalls of the release holes. Sealing occurs when the oxide deposited on opposite walls of the release holes meet in the center once a threshold thickness is reached [5].

- *Sealing with SACVD oxide:* The first sealing material studied is SACVD Si-oxide deposited by a reaction between TEOS ($Si(OC_2H_5)_4$ or Tetraethyl Orthosilicate) and ozone ($O_3$). During the reaction byproducts such as water vapour and ethylene are formed. A 900 nm-thick SACVD oxide layer was deposited at 420 °C and a pressure of 60 kPa on top of the released poly-SiGe membranes. From Fig. 5.2 we can see that the $1.2 \times 1.2\ \mu m^2$ release holes could be successfully sealed with a 900 nm-thick SACVD oxide. The top surface of the sealed membrane (Fig. 5.2b) is very smooth which is important to avoid adhesion and lithography problems during further processing. However, during the sealing process around 400 nm of oxide was deposited inside the cavity For thin film packaging, the deposition of sealing material inside the cavities is a concern since it will deposit on the surfaces of the packaged device, altering the device characteristics. This is not an issue for piezoresistive pressure sensors. On the other hand, for pressure sensors the thickness of the deposited material inside the cavity will reduce the cavity depth and might therefore reduce the full working pressure range of the devices.
- *Sealing with HDP oxide:* The second oxide sealing method considered employs HDP Si-oxide deposited by CVD based on a reaction between silane ($SiH_4$) and oxygen. The deposition temperature is not monitored, but it is expected to be around 400 °C. The process pressure is also not controlled as the throttle valve is fully opened during the chemical reaction. However, it is expected to be lower than the 60 kPa pressure used for the SACVD oxide deposition. Because of the non-conformal plasma-based process, very thick layers are required in order to seal release holes of $1.2 \times 1.2\ \mu m^2$ directly with HDP oxide (Fig. 5.3). This can be a benefit for thin film packaging applications as it results in more robust membranes, but it is not ideal for pressure sensors applications since a thicker membrane results in a lower sensitivity. For this reason the use of HDP Si-oxide for the direct sealing of the poly-SiGe pressure sensors was discarded.
- *Sealing with PECVD oxide:* The third oxide considered as sealing material is PECVD Si-oxide deposited by a reaction between silane and nitrous oxide ($N_2O$). Ammonia ($NH_3$) is a byproduct. The deposition of PECVD oxide is carried out at a low pressure (only 350 Pa), making it an interesting material for near-vacuum sealing of surface micromachined cavities for pressure sensors or thin-film packaging sealing. Figure 5.4 shows a cross-section picture of a 3.5 μm-thick poly-SiGe released membrane sealed with 3 μm of PECVD oxide. From this Figure it seems that to succesfully seal the $1.2 \times 1.2\ \mu m^2$ release holes around 2 μm of PECVD oxide could already have been enough. Similar as HDP oxide, PECVD oxide is also a non-conformal plasma-based process. Because of this the required thickness to seal the membranes is larger than in the case of SACVD Si-oxide. On the other hand, the quantity of material deposited inside the cavity is drastically reduced compared to SACVD sealing.

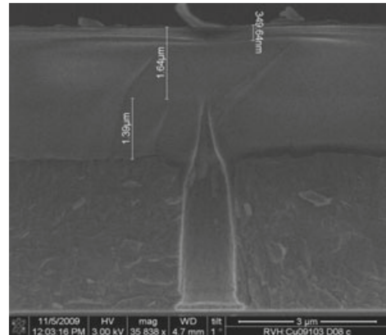


**Fig. 5.4** Sealing of a release hole with 3µm thick PECVD oxide. From this picture it seems that the minimum required thickness to seal the release holes is 1.5 µm < ts < 3 µm.

From these results we can conclude that the most efficient CVD Si-oxide layer for direct sealing of the poly-SiGe cavities is SACVD Si-oxide, followed by PECVD Si-oxide. HDP Si-oxide resulted to be the most inefficient for direct sealing as a very thick layer (thicker than 3 µm) is necessary to succesfully seal the release holes. Only SACVD Si-oxide will be further evaluated as sealing layer.

For pressure sensor applications, not only a low minimum required thickness is important, but also the residual stress of the sealing layer needs to be considered. The stress of the SACVD Si-oxide layer was determined from the measured wafer curvature after film deposition by applying Stoney's equation [12]. A 300 nm-thick SACVD oxide layer deposited on blanket Si wafers was used for the measurements. The stress was measured as deposited, three days, and a week after the deposition (Fig. 5.5). The initial stress of the as deposited film was 335 MPa (tensile) but it decreases over time, probably due to absorption of moisture from the air [13]. According to [13], the residual stress of a SACVD Si-oxide film will also change after annealing steps and can be tuned to a value from tensile to compressive depending on annealing temperature and ambient gas.

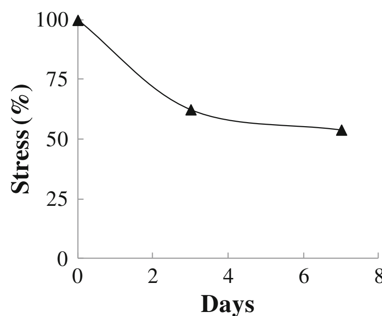


**Fig. 5.5** Stability over time of the residual stress of a SACVD layer deposited on a blanket wafer. After one day the stress of the film dropped to 62.5 % of the initial as-deposited value, although the decrease in the following days was not so steep. After 7 days the stress was ∼50 % of the initial value

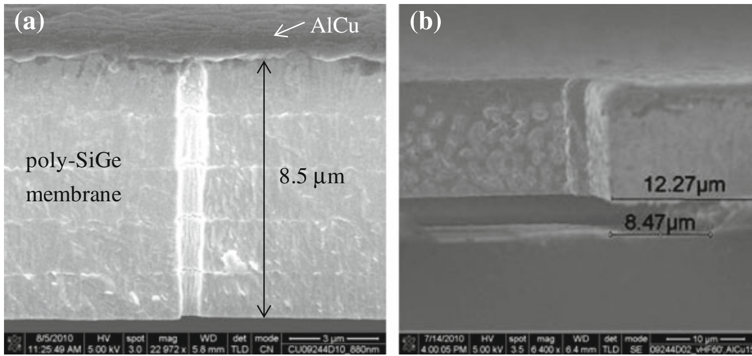


**Fig. 5.6** **a** Direct sealing of a 8.5 μm-thick poly-SiGe membrane with 1.5 μm of AlCu. The interface between the five PECVD SiGe layers is visible. **b** Strong reaction between the SiGe and AlCu is visible

### *5.3.2 Sealing with AlCu*

AlCu is a potential candidate for vacuum sealing of surface micromachined cavities due to its low deposition pressure (1 Pa). In this work the use of sputter-deposited AlCu (0.5 wt%) for the direct sealing of poly-SiGe microcavities is investigated. To limit the required AlCu thickness for direct sealing, the size of the printed release holes was reduced to $0.8 \times 0.8\ \mu m^2$ (final size after etch is $\sim 0.95 \times 0.95\ \mu m^2$). Figure 5.6a shows a cross-section picture of a 8.5 μm thick poly-SiGe membrane sealed with a 1.5 μm thick AlCu layer. The stress of the AlCu layer, as determined from wafer bow [12], is ∼100MPa tensile. Similar as the SACVD oxide, this stress can also relax with time [14]. From Fig. 5.6b it seems there is a strong reaction between the SiGe and the AlCu (there is no barrier layer), which may alter the properties and thus also the stress of the sealed membrane.

## 5.4 Intermediate Porous Cover

In this section the use of a porous cover on top of the release holes to prevent sealing material deposition inside the cavity and reduce the minimum required thickness of the sealing layer is discussed. In order to limit the effect of this (locally) porous layer on the thermal behaviour of the sealed membrane, it is preferred to use a layer with a thermal expansion coefficient (CTE) close to that of the poly-SiGe membrane. Since this porous cover could eventually be used as isolation between the poly-SiGe piezoresistors and the poly-SiGe membrane in the pressure sensor process flow, it must be a non-conductive layer. Two materials to be used as porous cover were considered: PECVD SiC and undoped PECVD microcrystalline (μc) SiGe. The process steps to create this porous cover are illustrated in Fig. 5.7. Similar

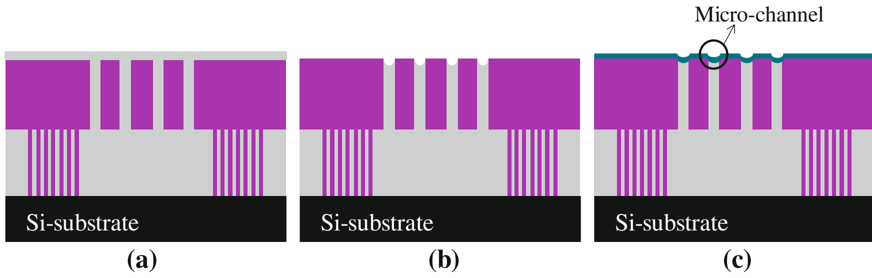


**Fig. 5.7** **a** Oxide filling of the release holes, **b** oxide dry recess and **c** porous cover deposition. Micro-channels, with a dimension significantly smaller than 100 nm, are formed above the release holes during the non-conformal deposition of the porous cover

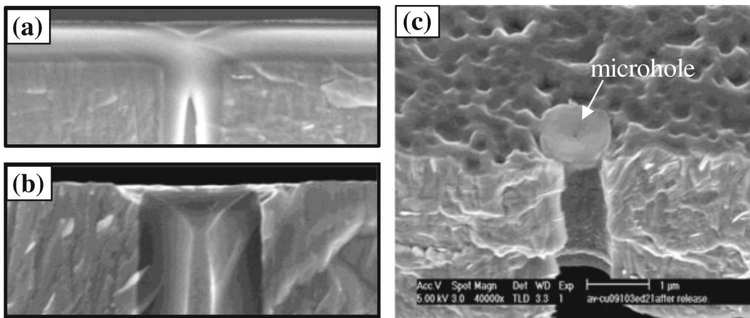


**Fig. 5.8** Cross-section SEM pictures of **a** oxide filling and **b** planarized surface after oxide etch back. **c** *Top* SEM picture of a microhole in the porous cover on top of a release hole

processing to form a porous cover on the membrane was already demonstrated in [7, 11]. Up to the opening of the release holes in the poly-SiGe membrane the fabrication flow of these tests structures is equivalent to the one showed in Fig. 5.1. After filling of the release holes with oxide, a dry etch is performed stopping on the SiGe membrane. This etch process creates a small recess in the filling oxide. A thin porous cover, with microchannels above the release holes (Fig. 5.8), is then deposited. All sacrificial oxide inside the cavity is etched by vHF (using the same recipe as for the direct sealed membranes) through the local microchannels in the porous cover. The presence of the porous cover does not affect the vHF Si-oxide etch rate [7]. After release the membranes can be sealed by thin film deposition.

The work on the PECVD SiC porous cover is described in Appendix C. As this material needed a thin Ti adhesion layer, it was ultimately not used for creating sealed cavities as this Ti layer could short-circuit the cavity membrane and the bondpads. The rest of this paragraph therefore deals with the work on μc-SiGe porous covers.

As mentioned before, the porous layer can eventually be used as isolation layer between the poly-SiGe piezoresistors and the poly-SiGe membrane. For this reason, a recipe to deposit a 200 nm-thick undoped μc-SiGe layer using a PECVD process

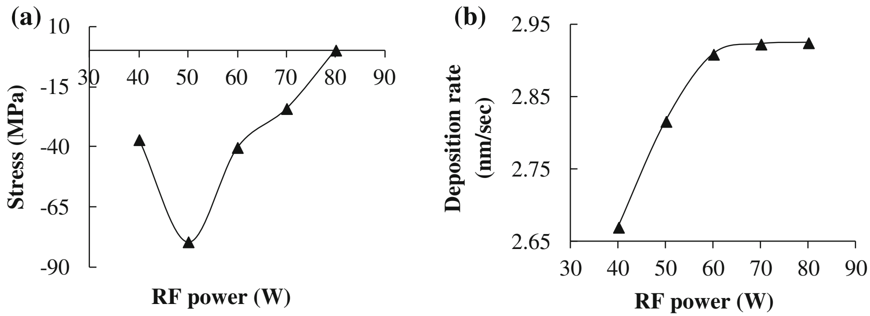


**Fig. 5.9** Effect of RF power on residual stress **a** and deposition rate **b** for a 200 nm-thick PECVD μc-SiGe layer. The μc-SiGe layer is deposited on oxide covered Si wafers

was developed specifically for this application. In order to limit the impact of this porous layer on the overall stress of the sealed membrane, a marginally tensile stress was targeted. By increasing the RF power from 40 to 80 W the residual stress in the layer (Fig. 5.9a) could be tuned from compressive to marginally tensile (∼0.3 MPa). The stress was calculated from the wafer curvature after deposition of the SiGe film on blanket Si wafers covered with oxide. An increase in RF power also translated into an increase in the deposition rate (Fig. 5.9b).

One advantage of using μc-SiGe as porous layer instead of SiC is that it eliminates the need of a "glue" layer (such as the conductive Ti layer in the case of a porous SiC cover, described in Appendix C) to improve adhesion to the SiGe membrane. Moreover, the use of a single μc-SiGe porous cover instead of the stack Ti/SiC will minimize the negative effects of thermally induced stresses due to CTE mismatch. Also, the marginally tensile stress of the optimized recipe makes μc-SiGe a much more attractive candidate than the Ti/SiC composite layer. For all these reasons μc-SiGe is the selected porous cover.

Two different layers to seal the poly-SiGe cavities released through a porous μc-SiGe were studied:

- 1 μm-thick HDP oxide layer (Fig. 5.10a)
- 690 nm-thick AlCu layer (Fig. 5.10b).

In the case of the HDP oxide, a 3.5 μm-thick sige membrane was used while to investigate AlCu as sealing layer, a 2 μm-thick membrane without patterned anchors was used. A colleague in imec studied the use of PECVD SiGe as sealing material for poly-SiGe cavities used in MEMS packaging [11]. In his work, 2 μm-thick poly-SiGe membranes released through a porous μc-SiGe cover and without patterned anchors were used. The porous μc-SiGe used as cover was a conductive layer, different from the μc-SiGe porous cover used in this work. Figure 5.10c shows SEM pictures of such membranes sealed with PECVD SiGe. We will further analyze the results obtained in [11] for the PECVD SiGe sealed-membranes and compare the results

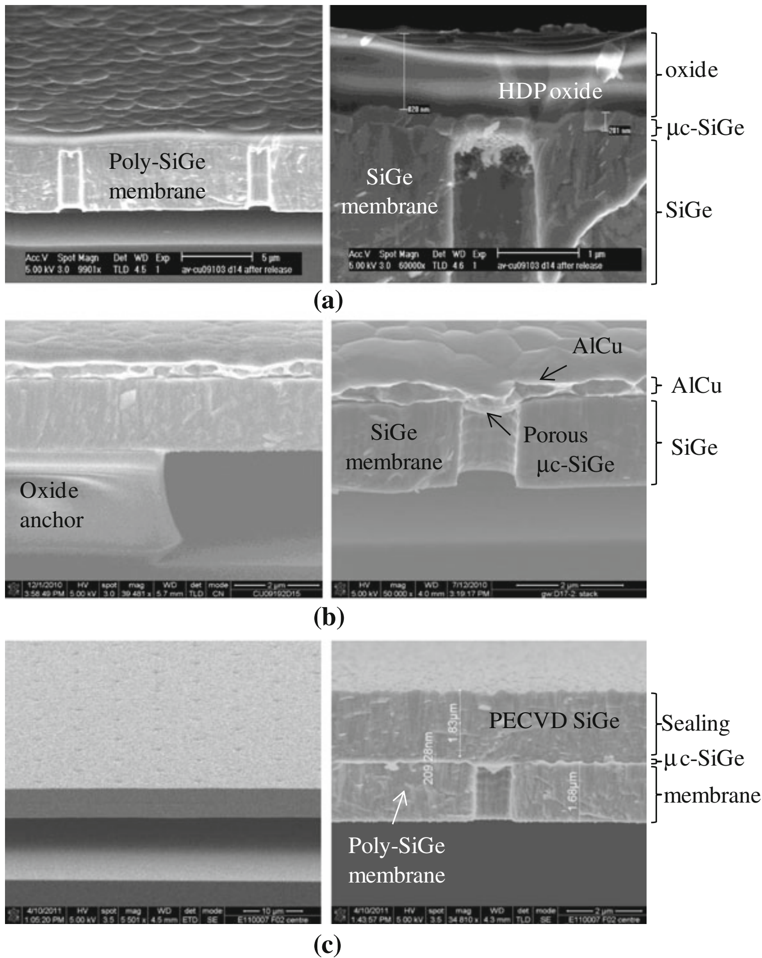


**Fig. 5.10** Poly-SiGe membranes released through a µc-SiGe porous cover and sealed with: **a** HDP oxide, **b** AlCu and **c** PECVD SiGe [11]. In **b**, the porous mc-SiGe cover is difficult to appreciate

to those obtained in this work for the HDP Si-oxide and the AlCu sealed poly-SiGe membranes.

In the case of the HDP Si-oxide sealed membranes, a final lithography step operation, followed by the etching of the HDP Si-oxide and the µc-SiGe cover (Fig. 5.11) was performed after sealing. The purpose of this patterning of the sealing layer was to check the effect of an exposed membrane/sealing layer interface on hermeticity. This final processing step was not performed for cavities sealed by any of the other sealing methods considered in this work.

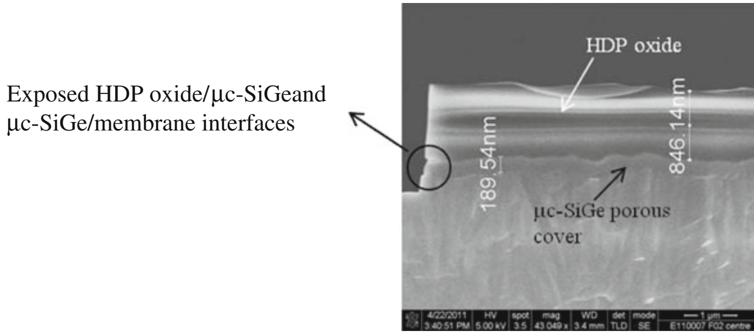


**Fig. 5.11** Close view of the exposed interfaces (HDP Si-oxide/μc-SiGe and μc-SiGe/membrane) after the final lithography step for a membrane sealed with HDP oxide and released through a porous μc-SiGe cover

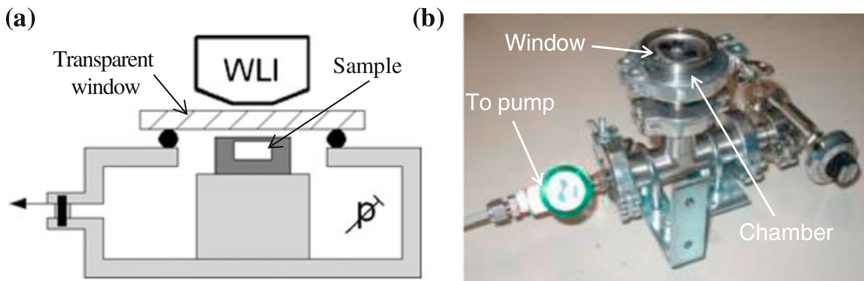


**Fig. 5.12** Deflection measurement setup. **a** Schematic—the chamber pressure can be switched between atmosphere (Air) and ∼25 kPa (Vacuum). A glass window is mounted on *top* of the chamber to facilitate the WLI inspection. **b** Photo of chamber—It can be connected to the clean room vacuum system which has a normal pressure of ∼25 kPa

## 5.5 Measurement Setup

To evaluate the different sealing technologies, the pressure-deflection response of sealed membranes of different dimensions was measured by WLI (White Light Interferometry) using an optical profilometer system (Wyko NT3300) [15, 16] combined with a Through Transmissive Media (TTM) module [17]. The samples were placed into a small dedicated vacuum chamber with a glass window, which is transparent for the light of the interferometer (Fig. 5.12). The membrane deflection is first measured at atmospheric pressure (101 kPa). Then the pressure inside the chamber is pumped down to ∼25 kPa, and the deflection profile is measured again. A difference in membrane deflection under the two pressures considered would indicate that the membranes are sealed. All measurements were done at room temperature.

From the measured membrane deflection under a known pressure together with the predicted deflection by analytical models and FEM (see also next section), the pressure inside the cavity can be estimated. To do so, it is necessary to measure the

membrane deflection accurately. This poses a problem for the oxide-sealed cavities since Si-oxide is transparent to light. To overcome this limitation, a thin (25 nm) Ti layer was deposited on top of the Si-oxide sealing layer. Due to the small thickness of the added Ti layer compared to the total diaphragm thickness (poly-SiGe membrane plus sealing layer), the effect of this Ti layer on the diaphragm response was considered negligible and not taken into account in the calculations and simulations described in the following sections.

## 5.6 Analytical Model

Both the overall stress and the cavity pressure of our sealed membranes can be determined using the membrane deflection method [18, 19]. In this technique the deflection of the membrane is measured as a function of applied pressure. By fitting the measurement data to an appropriate equation describing the load-deflection response of the membrane, parameters such as internal stress, Young's modulus and sealed-in pressure can be obtained. Different analytical solutions have been proposed to derive the maximum deflection in the centre of a uniformly loaded clamped membrane. In general the mechanical response of a membrane subjected to an external load is governed by its geometry (thickness, size and shape) and material properties (mainly residual stress, Young's modulus and Poisson's ratio).

Following the variational method, the load-deflection model of a clamped square membrane due to a differential pressure ΔP across the membrane is expressed as [20]:

$$\Delta P = \left[ C_r \frac{\sigma_0 t}{L^2} + C_b \frac{E_t^3}{\left(1 - v^2\right) L^4} \right] w_0 + \left[ C_s f_s(v) \frac{E_t}{L^4} \right] w_0^3 \tag{5.1}$$

where $\Delta P = P\text{-}P_{in}$ is the difference between the applied external pressure (P) and the cavity pressure ($P_{in}$),$w_0$ is the centre deflection, $L$ is the membrane side length, $t$ the membrane thickness, $\sigma_0$is the residual stress in the membrane, $E$ the Young's modulus and $v$ is the Poisson ratio. The Poisson ratio dependent function $f_s(v)$is given by [21]:

$$f_s\left(v\right) = \frac{1 - 0.271v}{1 - v} \tag{5.2}$$

In (5.1), the first term within the square bracket represents the stiffness of the membrane due to the residual stress while the second term is the stiffness due to bending. The last term represents the stiffness due to nonlinear spring hardening. This model has already been succesfully applied to extract mechanical properties of poly-Si and Si-nitride films [18, 22]. In these references, however, the assumption of $w_o >> $t (which is not true in our case) was applied and the term describing the stiffness due to bending (second term in first parenthesis) was neglected.

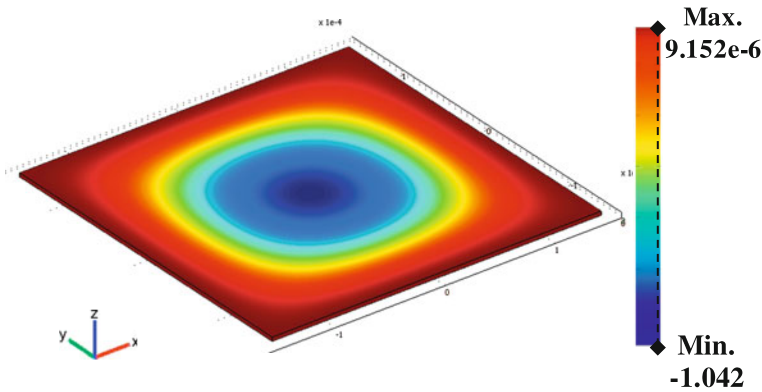


**Fig. 5.13** Simulated deflection (in μm) of a poly-SiGe membrane of length L = 300 μm and thickness 3.5 μm subjected to a total differential pressure of 1 bar

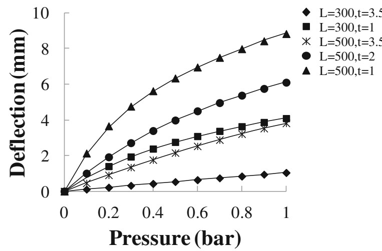


**Fig. 5.14** Simulated deflection together with fitting curves from Eq. (5.1) for square poly-SiGe membranes of length (L) and thickness (t) in μm. The markers are FEA simulated values. The *solid lines* represent the fitting curves. The pressure in the x-axis represents the differential pressure across the membrane

The value of the dimensionless constants $C_r$, $C_b$ and $C_s$ can be obtained by simulating the deflection of square membranes for a sequence of applied loads and fitting the results to Eq. (5.1). To do so, finite element simulations of square suspended membranes of different areas and thicknesses were carried out using the program COMSOL [23] (Fig. 5.13). Clamped edges were implemented as boundary conditions. A Young's modulus $E = 140$ GPa, a Poisson's ratio $\upsilon = 0.23$ and a residual stress $\sigma = 70$ MPa for poly-SiGe are used both in the simulations and calculations. Figure 5.14 plots the simulated deflection vs. pressure together with the fitting curves for square poly-SiGe membranes of different dimensions. The modeled values (with accuracy within 3 %) for $C_r$, $C_b$ and $C_s$ are 15.4, 65.6 and 31.7, respectively. These values are similar to the ones reported in [21] for square membranes with a possion's ratio $\upsilon = 0.25$.

In Eq. (5.1) the effect of the release holes is not included. A factor λ describing the decreased stiffness of the membrane due to the openings was empirically formulated in [24] as:

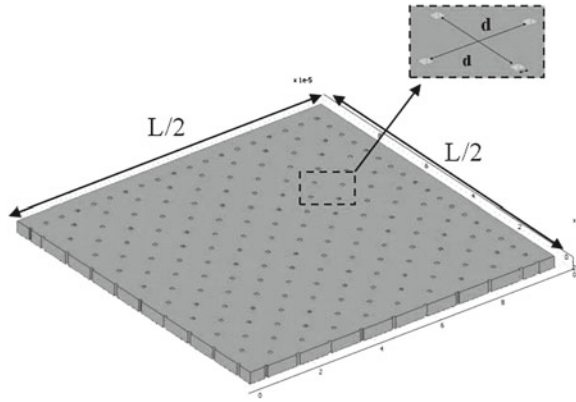


**Fig. 5.15** FEA model of a quarter of a membrane of length L. Zoom in the pattern of release holes (d = 9.5 μm)

$$\lambda = 1 - \frac{Area_{openings}}{Area_{total}} \tag{5.3}$$

which yields a value of ~0.975 for all the structures considered in this work. In order to account for the effect of release holes the Young's modulus $E$ in equation (5.1) can be replaced by $E_h = \lambda E$.

For a more accurate estimation of the value of parameter λ, finite element simulations of the load-deflection response of perforated membranes were performed. Square membranes with different lengths (from 50 to 500 μm) and thicknesses (from 0.1 to 3.5 μm) but with the same pattern of release holes (Fig. 5.3) were considered in the simulations. Since the designed structures posses' 4-fold symmetry only a quarter of the model is used in the simulations to reduce computational time (Fig. 5.15). Substituting the simulated deflection at a certain pressure in (5.1) (with $E$ replaced by $E_h$) and solving the equation in λ, a value of 0.967±0.006 was obtained. This value is very close to the one predicted by (5.3).

## 5.7 Results and Discussion

As mentioned before, the deflection of the sealed membranes is measured using an optical interference profilometry system under two different applied pressures. Figure 5.16 shows a 3D representation of the optically measured deflection in air (1 bar) of membranes sealed with μc-SiGe porous layer and HDP Si-oxide. Figure 5.17 plots the obtained deflection profiles along the centre of membranes (cut along X in Fig. 5.16) of 500 × 500 μm$^2$ sealed with AlCu (both as direct sealing and in combination with a porous cover) and SiGe, measured in air (1 bar) and vacuum (0.25 bar). Particularly interesting to note is the deflection profile in air for the membranes sealed with SiGe; such a profile is characteristic of postbuckled membranes under differential pressure [25]. The maximum deflection for membranes of different areas

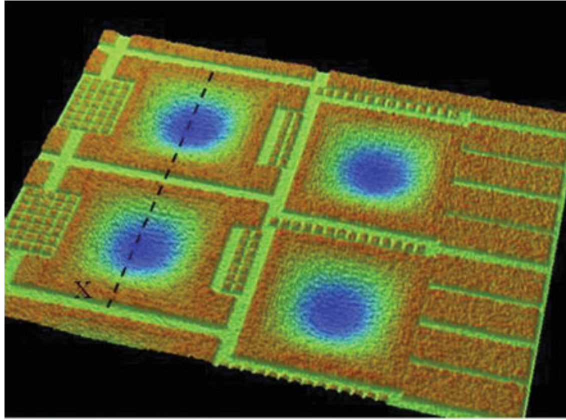


**Fig. 5.16** Optical picture of the deflection in air of $300 \times 300\,\mu m^2$ membranes sealed with HDP Si-oxide

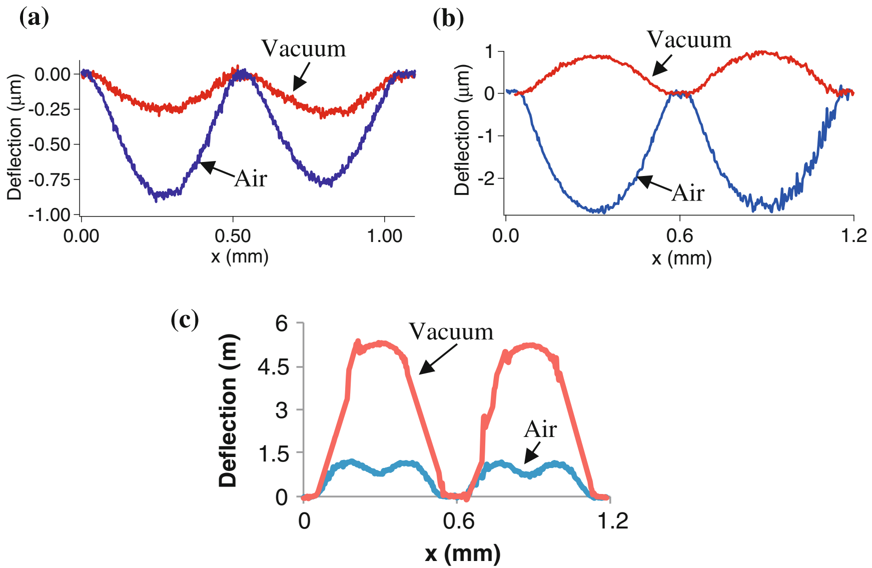


**Fig. 5.17** Measured membrane deflection for membranes sealed with **a** AlCu only, **b** µc-SiGe+AlCu and **c** µc-SiGe+SiGe (from [1]). The difference in *deflection* indicates that the membranes are sealed. Each graphs plots the deflection of two identical membranes

($200 \times 200$, $250 \times 250$ and $300 \times 300\,\mu m^2$) sealed with (a) SACVD Si-oxide and (b) HDP Si-oxide is shown in Fig. 5.18. From the obtained results we can conclude that all the sealing techniques and materials considered provide short-term hermetic sealing.

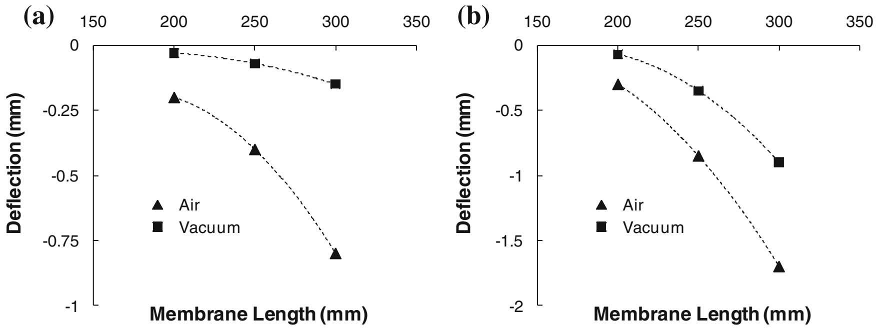


**Fig. 5.18** Measured deflections for membranes of different areas: 200 × 200, 250 × 250 and 300 × 300 μm². **a** Membranes sealed with SACVD oxide and **b** μc-SiGe/HDP oxide-sealed membranes

The resulting cavity pressure ($P_{in}$) and the residual stress ($\sigma_0$) of the composite membranes can be determined by fitting the measured load-deflection data to Eq. (5.1). For this method to be applicable, it is necessary to foresee a gap large enough to accommodate the maximum expected deflection of the membrane. An insufficient gap depth would translate into an erroneous measurement of the membrane deflection, therefore leading to a wrong estimation of the residual stress or cavity pressure. From Figs. 5.17 and 5.18 we can see that, in this work, the maximum measured deflection is, in all cases, less than the gap depth (3 μm).

The Young's modulus of the sealed membranes can be calculated by Eq. (5.4) [18], assuming the same value for Poisson's ratio for all layers:

$$E_c = \frac{\lambda \cdot E_{SiGe} \cdot t_{SiGe} + E_s \cdot t_s}{t_c} \tag{5.4}$$

where t is the thickness and the subscripts c and s represent the compound membrane and the sealing layer, respectively. The parameter λ (Sect. 5.6) is included to account for the reduction of the poly-SiGe membrane stiffness due to the release holes.

The Young's modulus of the poly-SiGe membrane and the different sealing materials was obtained from nanoindentation by using a continuous stiffness measurement (CSM) technique [26]. This technique consists of applying a small harmonic, high frequency amplitude force during indentation loading, and measuring the contact stiffness of the sample from the displacement response at the excitation frequency. The Young's modulus of the material is then derived from the contact stiffness. The Young's modulus of the compound membrane ($E_c$) is obtained from the measured values (Table 5.2) by applying Eq. (5.4). For the PECVD SiGe-sealed membranes, since no measurements were available, a Young's modulus $E = 140$ GPA was assumed [11]. For the porous μc-SiGe cover, a $E = 100$ GPa was considered.

**Table 5.2** Measured young's modulus by nanoindentation

| | SiGe (3.5μm) | SACVD oxide (0.9 μm) | HDP oxide (1 μm) | AlCu (1.5 μm) |
|---|---|---|---|---|
| E (GPa) | 147±6 | 60±4 | 73±9 | 67±5 |

In parenthesis the thickness of the layer used in the measurements

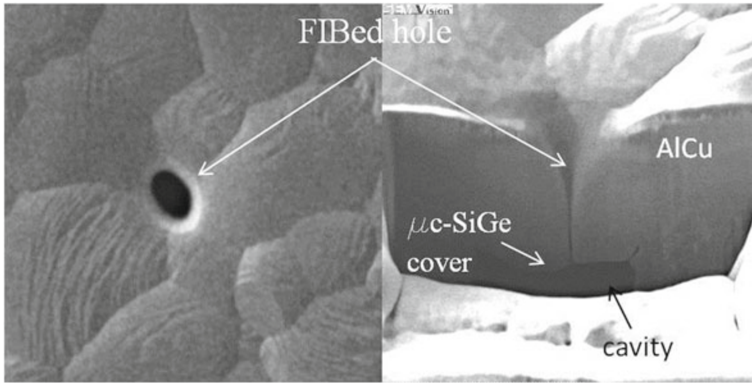


**Fig. 5.19** *Top* view and cross-section pictures of a micro hole drilled in a μc-SiGe +AlCu sealed membrane

## 5.7.1 Membrane Behavior Under 0-Pressure Difference

The load-deflection technique can only be applied to membranes that remain flat without load. If the residual stress is compressive and large enough the membrane may buckle, leading to erroneous estimation of the cavity pressure [19, 27]. To verify if the membrane layers buckled or not, micro-venting holes of 1×1 μm$^2$ were drilled using a Focus Ion Beam (FIB) in some of the sealed membranes (Fig. 5.19). In this way a 0-pressure-difference reference is available. This hole made by FIB is so small that the effect on the global stress in the membrane can be neglected. Under a 0-pressure difference, thin film membranes show the following behavior: with tensile residual stress ($\sigma_0 > 0$) or weakly compressive stress ($\sigma_{crl} < \sigma_0 < 0$), the membrane is stable in the flat position. For a compressive stress greater than a critical stress $\sigma_{crl}$(given by (5.5) [28]) the membrane will buckle transversally without any external load

$$\sigma_{crl} = -4.363 \cdot \frac{E \cdot h^2}{(1 - v^2) \cdot L^2} \tag{5.5}$$

where $E$ and $v$ are the Young's modulus and Poisson's ratio, respectively, $h$ is the membrane thickness and $L$ is the membrane length.

Figure 5.20 shows the measured deflection of two membranes (one of them with a micro venting hole opened by FIB) sealed by a combination of μc-SiGe porous

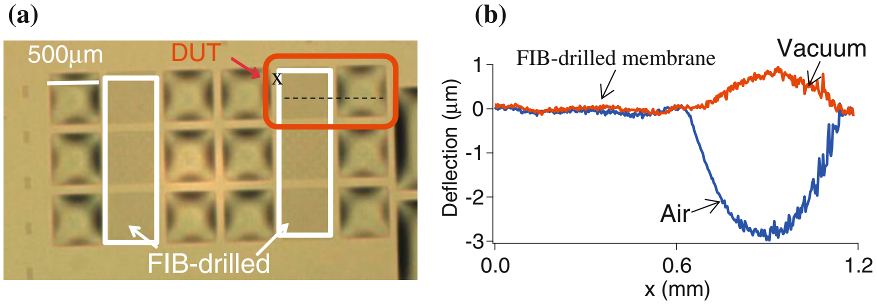


**Fig. 5.20** *Top*-view picture of the membrane deflection for 18 cavities sealed with μc-SiGe porous layer and AlCu, in 6 of them (inside *white square*) **a** hole was drilled by FIB, **b** Membrane deflection measured by WLI on two membranes with and without the micro venting hole

layer and AlCu. All the FIB-drilled membranes studied in this work, except those sealed with HDP Si-oxide or SiGe, remain flat, which indicates an overall stress in the diaphragm either tensile or less compressive than the minimum critical stress ($\sigma_{ctl}$ of the biggest membrane).

For HDP Si-oxide sealed membranes buckling was observed, which is not surprising considering the high compressive residual stress typically exhibited by HDP Si-oxide layers. However, only the larger membranes ($L = 300\,\mu\text{m}$) (Fig. 5.21a) buckled while the smaller membranes remain flat. This result indicates that the stress in the HDP-sealed membranes is compressive in the range ($\sigma_{ctl}(L = 300\,\mu\text{m})$, $\sigma_{ctl}(250\,\mu\text{m})$). From (5.5), the critical stress for $300\times300\ \mu\text{m}^2$ ($250\times250\ \mu\text{m}^2$) membranes sealed by HDP Si-oxide is $-137.34$ MPa ($-197.76$ MPa). On the other hand, the fact that the membranes of $500\times500\ \mu\text{m}^2$ sealed with SiGe exhibitted buckling indicates that the stress is more compressive than the critical stress of $-43.51$ MPa.

The exact value of the compressive residual stress in the buckled membranes can be extracted from the measured centre deflection of the FIB-drilled membranes by applying the expression given in [23]. The measured centre deflection is ∼760 nm in the case of the FIBed $300\times300\ \mu\text{m}^2$ HDP Si-oxide sealed membrane and ∼5 μm for the SiGe-sealed $500\times500\ \mu\text{m}^2$ FIBed membrane. The obtained value for the residual stress is $-139.2$ MPa for the HDP Si-oxide sealed membrane, which falls into the predicted range. For the SiGe sealed membrane the residual stress is calculated to be $-74.15$ MPa.

To corroborate these results, nonlinear finite-element simulations of the buckling of a $300\times300\mu\text{m}^2$ membrane sealed with HDP were performed using COMSOL (Fig. 5.21). The total membrane thickness, Poisson's ratio and Young's modulus (from Eq. (5.4)) were set to 4.6 μm, 0.23 and 126.8 GPa respectively. The compressive residual stress was simulated thermally, following a similar approach as in [28]. In order to obtain a simulated deflection equal to the measured one (760 nm) a compressive stress $\sigma = -136.9$ MPa was found, close to the value predicted analytically.

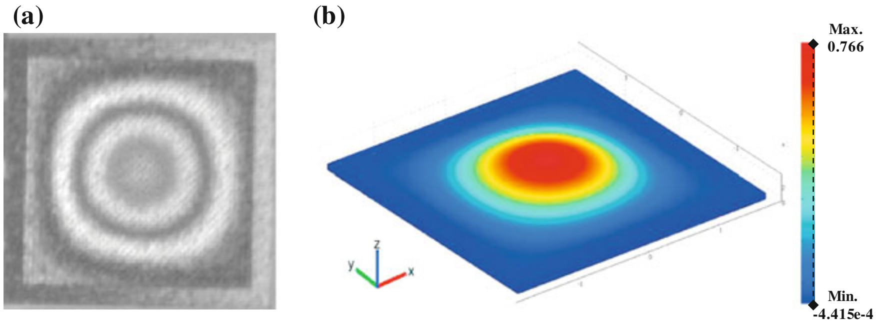


**Fig. 5.21** Buckling of a $300 \times 300\,\mu m^2$ membrane sealed with HDP oxide under a 0-pressure difference. **a** Interferometric contour image and **b** simulation of the deflection under a thermally induced stress $\sigma = -136.9\,\text{MPa}$

### *5.7.2 Cavity Pressure*

It is important to determine the residual pressure inside the sealed cavity in order to predict the device performance. In thin-film packaging, the cavity pressure will affect the packaged device performance. For absolute pressure sensors, the pressure inside the sealed cavities supplies a reference for pressure measurements. Moreover, as mentioned in Sect. 5.1, the expansion of the gasses trapped inside the cavity will degrade the temperature dependence of the pressure sensors performance. Therefore it is, in general, preferred to have a vacuum-sealed cavity for pressure sensor applications as this will minimize the trapped gas effects. From the measurements discussed above, we can derive both the sealed-in pressure and the membrane stress for the different sealing approaches studied.

Since all the sealed membranes in this study (except for the $300 \times 300\,\mu m^2$ membranes sealed with HDP Si-oxide and the $500 \times 500\,\mu m^2$ membranes sealed with SiGe) remain flat under 0-differential pressure, the value of the sealed-in pressure ($P_{in}$) and residual stress of the compound membranes ($\sigma_o$) can be easily calculated from the load-deflection measurements by substituting in (5.1) $E$ by $E_c$ as calculated from (5.4), $t$ by the total thickness of the composite membrane $t_c$ and $w_0$ by the measured deflection. A constant value of Poisson's ratio $\nu_{SiGe} = 0.23$ is assumed for all compound membranes. Table 5.3 contains the obtained values. In the case of SiGe sealing, since no flat membranes are available, the cavity pressure was estimated from finite-element simulations (COMSOL). A negative value for $\sigma_0$ indicates a compressive stress. The relatively big uncertainty on the calculated values is mainly due to the limited accuracy in the optical measurements ($\pm 0.05\,\mu m$) and the control of the "vacuum" pressure ($25 \pm 5$ kPa).

The values obtained for the overall stress in the sealed diaphragms ($\sigma_o$) are in good agreement with the observations made in Sect. 5.7.1 from the FIBed membranes. The compressive stress in the membrane with AlCu direct sealing is, as expected from the flat membranes after FIB hole drilling, below the critical pressure for buckling (Eq. (5.5)). The fact that the membranes sealed with AlCu only exhibitted compresive

**Table 5.3** Overall stress and cavity pressure obtained from the load-deflection data for the different sealing techniques.

| Sealing technique | Sealing layer | $t_c$ (μm) | $E_c$ (GPa) | $\sigma_0$ (MPa) | Pin (kPa) |
|---|---|---|---|---|---|
| Direct sealing | SACVD Si-oxide | 4.6[a] | 122.5 | 11±3 | 7±2 |
| | AlCu | 10 | 130.86 | −50±10 | <1 |
| μc-SiGe porous layer | HDP Si-oxide[c] | 4.6[b] | 126.8 | −130±10 | 20±5 |
| | AlCu | 2.89 | 121.3 | 90±5 | 40±2 |
| | PECVD SiGe [1] | 4 | 140 | −75 | 60 |

[a] $t_c$= 3.5 μm membrane + 0.2 μm bottom SACVD + 0.9 μm top SACVD (Fig. 5.2a).
[b] $t_c$= 3.5 μm membrane + 0.2 μm porous layer + 0.9 μm HDP oxide (Fig. 5.10a).
[c] Sealing layer/membrane interface exposed

stress is a bit surprising considering that both SiGe and AlCu normally exhibit tensile stress. One possible explanation could be the strong reaction observed between SiGe and AlCu (see Fig. 5.6b), which might lead to volume changes and the creation of compressive stress. In the case of membranes sealed with a combination of porous layer and AlCu this reaction is not observed as the porous layer probably easily oxidizes and then acts as a barrier, preventing any reaction. The overall stress is tensile in that case as expected from the measured flat membranes under 0-differential pressure (see Fig. 5.20).

As it can be expected from the low deposition pressure, direct AlCu sealing results in (near) vacuum-sealed cavities. In Fig. 5.17 we can observe that the AlCu-only sealed membranes have a less negative deflection in air than the μc-SiGe+AlCu membranes. This may seem surprising since the found inside cavity pressure is much lower for the AlCu-only sealed membranes. But it can be easily explained considering that the total membrane thickness of the AlCu-only sealed membranes (11.5 μm) is around four times greater than the total thickness of the membranes sealed with μc-SiGe+AlCu (2.89 μm).

For SACVD oxide sealing a cavity pressure of around 7 kPa was found, considerably smaller than the value expected from the processing pressure, temperature and overall chemical reaction [29], when using the ideal gas law [30]. A possible explanation for this low sealed-in pressure could be the continued reaction of the trapped gases after sealing, which reduces the amount of gaseous products and reactants, and the absorption of the residual water vapor generated during the chemical reaction by the oxide layer inside the cavity [31].

For the cavities sealed using a porous μc-SiGe cover in combination with Si-oxide, AlCu or SiGe a quite high residual pressure was found. Of particular significance is the case of the cavities sealed with porous μc-SiGe and AlCu, for which a much higher sealed-in pressure (∼40 kPa) than for equivalent cavities sealed with only AlCu was found. One possible cause for this could be outgassing from the porous μc-SiGe cover. Indeed, recent experiments proved that as-deposited SiGe can outgas large quantities of hydrogen, water vapour and, in some cases, $CO_2$ [32]. The μc-SiGe cover, due to its porous texture, is expected to outgas even more. Moreover, during the sealing layer deposition, the porous cover will trap most of the outgassing from the SiGe cavity walls while during direct sealing the gasses can diffuse more

freely out of the cavity. Another explanation, proposed in [7], is the existence of a temporary leak path in the exposed interface between the porous μc-SiGe cover and the SiGe membrane. However this explanation would only be valid for the porous layer + HDP sealed cavities, since in the AlCu and SiGe cavities this interface is not exposed.

These results make it clear that, in case a low sealed-in pressure is desired, it is very important to ensure that the layers inside the cavity are properly outgassed before the cavity is sealed. This can be achieved, for example, by introducing an annealing step just before the deposition of the sealing material [32].

### 5.7.3 Long-Term Hermeticity

Long-term hermeticity tests were performed for the cavities with the lowest residual pressure (SACVD Si-oxide and AlCu sealed cavities). The hermeticity was investigated by measuring the membrane deflection at regular intervals of time. A difference in deflection after a certain period of time under the same pressure loading would indicate the presence of a leak path. Long-term deflection monitoring for 300×300 $\mu m^2$ SACVD sealed cavities and 500×500 $\mu m^2$ AlCu sealed cavities (Fig. 5.22) shows that there is no detectable change in cavity pressure over time.

A leak can be characterized by a standard leak rate $r$ [33], defined as the quantity of dry air at 25 °C flowing through a leak or multiple leak paths per second when the high-pressure side is air at atmospheric pressure (101 kPa):

$$r = \frac{\Delta P \cdot V}{t} \tag{5.6}$$

where $r$ is the standard leak rate in air, $\Delta P$ is the variation in sealed-in pressure, $t$ is the time for the pressure change in seconds and $V$ is the internal volume of the cavity. Assuming a 0.05 μm resolution in the WLI measurement, which corresponds to a change in cavity pressure of ∼5.5 kPa for 300×300 $\mu m^2$ cavities (∼5.7 kPa for

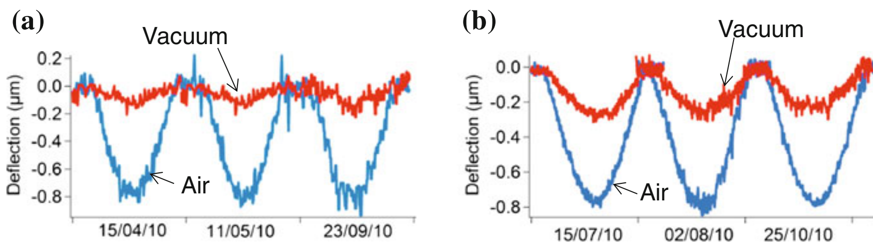


**Fig. 5.22** Deflection measurement (1 membrane is shown) indicating long term hermeticity. In **a** the cavity is 300×300 $\mu m^2$ and the sealing layer is 900 nm SACVD oxide. In **b** the cavity is 500×500 $\mu m^2$ and sealing layer is 1.5 μm AlCu

$500 \times 500\ \mu m^2$ cavities), and applying Eq. (5.6), the obtained long-term hermeticity results point out a maximum possible leak rate (deflection resolution/monitoring time) of $\sim 1 \times 10^{-16}$ Pa·m$^3$/s ($\sim 5.5 \times 10^{-16}$ Pa·m$^3$/s) for SACVD Si-oxide (AlCu) sealing.

## 5.8 Summary and Conclusion

Two different techniques for the sealing of poly-SiGe microcavities by thin-film deposition have been presented: direct sealing and the use of an intermediate porous cover. Two different sealing materials were considered: Si-oxide and AlCu. The results were compared with SiGe sealing experiments from literature [11].

The experimental results prove that both Si-oxide and AlCu can provide short- and long-term air-tight sealing. SACVD Si-oxide offers an attractive and simple technique for the direct sealing of surface micromachined cavities, with a resulting cavity pressure below 10 kPa. Direct sealing with AlCu provides a near-vacuum sealed cavity and can be a promising technique for applications such as thin-film packaging or capacitive pressure sensors. For piezoresistive pressure sensors the use of AlCu as sealing layer is however not practical; extra isolation layer and/or extra processing steps might need to be introduced to avoid a short-circuit between different piezoresistors.

For applications where the deposition of sealing material inside the cavity is undesirable, the use of a porous μc-SiGe cover in combination with Si-oxide or AlCu has been proposed. This porous cover, although preventing the deposition of sealing material inside the cavity, resulted, for the cavities studied in this work, in a higher sealed-in pressure. In order to use this porous cover it is important to ensure proper outgassing of the materials used inside the cavity and to avoid an exposed SiGe membrane/ μc-SiGe interface.

After all these experiments SACVD Si-oxide was the selected sealing material for the development of the pressure sensor. Sealing with SACVD Si-oxide is simple and efficient, since relatively thin layers are enough to seal the cavities. It also results in a smooth sealed surface that will facilitate further processing (like, for example, the deposition/patterning of the metal lines connecting the piezoresistors). Moreover the Si-oxide sealing layer can be used as isolation between the membrane, the different piezoresistors and the metal interconnects. The poly-SiGe cavities sealed with SACVD Si-oxide also exhibited marginally tensile stress, very attractive for pressure sensor applications. On the other hand, SACVD Si-oxide presents two important drawbacks. The first inconvenience is the relatively high sealed-in pressure that can pose a problem in low-pressure applications. For our test devices this is however not a big issue. A second important drawback of SACVD Si-oxide as sealing layer is the big CTE mismatch with the poly-SiGe membrane that will compromise the temperature stability of the pressure sensor performance. From CTE point of view the most interesting sealing material considered would be SiGe. In this way an all-SiGe (membrane, piezoresistors and sealing layers) pressure sensor can be obtained.

However, if SiGe is to be used as sealing material, further developments are needed to tune the stress to obtain an overall marginally tensile stress and avoid buckling. Also, a new recipe to have an undoped SiGe sealing layer would be required to avoid an unwanted electrical connection between the interconnects, the membrane and the piezoresistors.

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# Chapter 6
# Characterization of Poly-SiGe Pressure Sensors

In this chapter, the realized stand-alone poly-SiGe pressure sensors (both piezoresistive and capacitive) are tested and evaluated. The tested pressure sensors were fabricated following the process flow described in Chap. 4. The chapter begins with a description of the employed measurement setup. In this work, the fabricated sensors are tested in the pressure range from 0 to 1 bar using a Suss Microtec PMV-150 environmental chamber. The piezoresistive pressure sensors are evaluated mainly in terms of pressure sensitivity, although other aspects, such as temperature coefficient of sensitivity, offset voltage and non-linearity are also considered. The obtained measurement results are compared to the values predicted by simulations (Chap. 3); to explain the mismatch between the measured and the simulated sensitivity, further simulations, including the effect of the SiC isolation layer and the oxide sealing layer, are performed. On the other hand, for the capacitive pressure sensors only the sensitivity is evaluated. The chapter ends with a summary of the obtained results, including some observations about the performance of the fabricated sensors.

## 6.1 Measurement Setup

To experimentally characterize the pressure response of the fabricated sensors, the measurement setup illustrated in Fig. 6.1 was used. The used measurement setup consists of the following instruments:

- Suss Microtec PMV-150 environmental chamber [1, 2].
- HP4156 precision parameter analyzer [3].

The Suss Microtec PMV-150 is a manual vacuum prober suitable for the testing of MEMS at wafer-level in the pressure range from high vacuum (up to $10^{-7}$ mbar) to atmospheric pressure ($\sim$1 bar). It is equipped with a chuck stage, with movement in the X–Y ($150 \times 150$ mm) and Z direction, and six probe manipulators. Both the probing system and the chuck position are operated manually. The chamber is completed with a microscope connected to a PC screen, for the visualization

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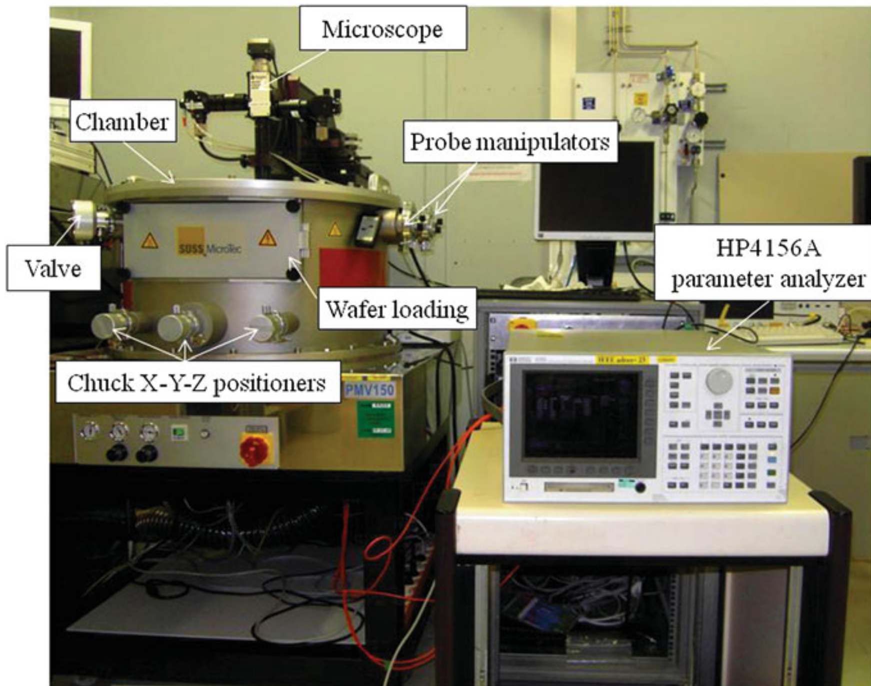



**Fig. 6.1** Picture of the measurement setup used to characterize the fabricated pressure sensors. Both the PMV-150 pressure chamber (with the different components highlighted) and the HP4156 parameter analyzer are visible. The cables (*orange*) providing electrical connection between the parameter analyzer and the probes inside the pressure chamber can also be observed

of the devices. Four cables connect the probes inside the environmental chamber to the electrical part of the measurement setup, formed by a HP4156A precision parameter analyzer which provides a bias voltage to the sensor and measures the output differential voltage.

All measurements described in Sect. 6.2 were performed at room temperature. After placing the wafer to be tested inside the PMV-150 chamber, the pressure inside the chamber is pumped down to $\sim$0 bar (the "vacuum" pressure used in these experiments is $\sim$5 mbar); the chamber pressure is then sequentially increased (by opening/closing the chamber valve) up to 1 bar (atmospheric pressure) in steps of 0.25 bar. For each pressure, a bias or input voltage is applied to the sensor and the corresponding output is measured and recorded (Fig. 6.2). Typically a bias voltage of 3.3 V is used as this is the bias voltage required by the CMOS technology used to fabricate the sensor readout circuit (see Chap. 7). Figure 6.2 shows a microscope picture of one of the fabricated devices, with the necessary electrical stimuli for measurements indicated on top of the corresponding bondpad.

To finish it is important to note that the PMV-150 includes a thermal controller that allows varying the chuck temperature from $-60$ to 200 °C. In this way, by applying

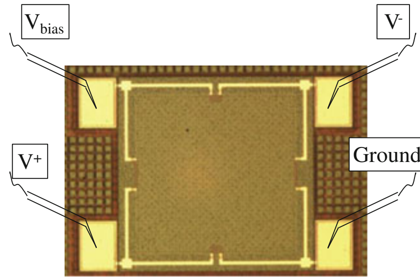



**Fig. 6.2** Top view microscope picture of one of the fabricated devices, including a drawing of the two probes used for electrical stimuli (bias voltage and ground) plus the two probes used for electrical detection ($V^+$ and $V^-$). The electrical stimuli and detection are all provided by the parameter analyzer. The output voltage of the sensor is obtained from $V_{out} = V^+ - V^-$

a measurement procedure similar to the one described above, the thermal behaviour of the fabricated sensors can also be characterized, as will be seen in Sect. 6.3.

## 6.2 Measurement Results: Pressure Response

This section reports the measured pressure response at room temperature of the fabricated poly-SiGe pressure sensors. The studied performance parameters include pressure sensitivity, voltage offset and nonlinearity (see Chap. 3 for a definition of these parameters). Figure 6.3 shows microscope pictures of the six different types of piezoresistive sensors characterized in this chapter. As explained in Chap. 3, the six sensor designs considered include three different shapes of the longitudinal piezoresistor and two different placements of the transverse piezoresistors (membrane centre and edge). To facilitate the description of the obtained results, each sensor design has an identifier (also included in Fig. 6.3). This identifier includes a number, 1, 2 or 3, corresponding to the longitudinal piezoresistor shape ("single-line", "n-shape" or "m-shape" respectively); for the sensors with the transverse piezoresistors placed in the centre, the identifier also includes the suffix "−T".

Moreover, two different types of sensors (square-shaped and rectangular) were characterized. For the square-shaped sensors, three different membrane areas ($200 \times 200$, $250 \times 250$ and $300 \times 300\ \mu m^2$) were considered. However, due to delamination problems during fabrication, not all the designed sensors could be measured. These delamination problems, caused mainly by the difference in stress of the different layers that form the sensors (see Chap. 4 ), affect primarily the bigger sensors ($300 \times 300\ \mu m^2$). For this reason, only one type of $300 \times 300\ \mu m^2$ sensor could be characterized (D3). For the smaller areas, all six designs could be measured.

All the details about the fabrication process of the characterized poly-SiGe pressure sensors can be found in Chap. 4. The fabricated pressure sensors consist in a poly-SiGe membrane with the poly-SiGe piezoresistors placed on top, with a thin

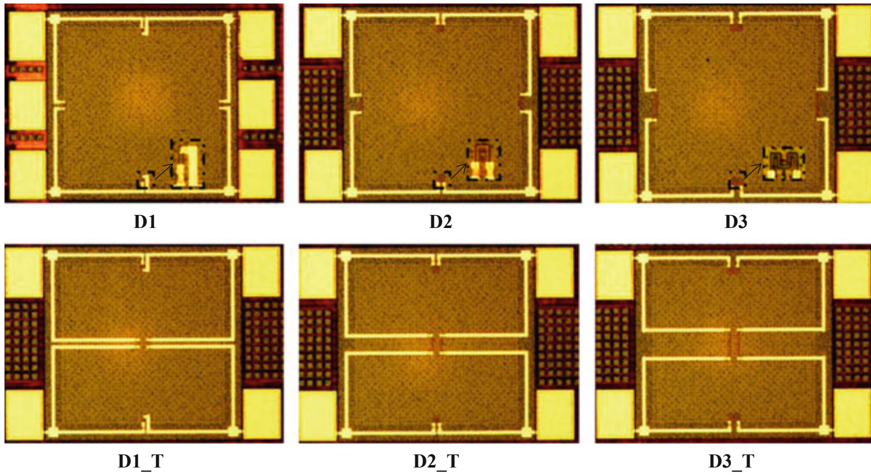



**Fig. 6.3** Microscope pictures of the different sensor designs fabricated: three different longitudinal piezoresistor shape (linear, n-shape and "three-turns") and two different locations for the transverse piezoresistors: at the membrane centre or at the edge. Below each picture, the corresponding sensor identifier is included. Sensor D1 (top left) has six bondpads because it is both capacitive and piezoresistive (see Chap. 4 for more information)

SiC isolation layer in between. The piezoresistors are connected through AlCu metal lines. The $\sim 1 \times 1\ \mu m^2$ release holes, located on top of the membrane, are sealed with a SACVD Si-oxide layer $\sim 1.2\ \mu m$ thick. The cavity pressure after sealing, determined from load-deflection measurements, is $\sim 7$ kPa (see Chap. 5). More information about the final thicknesses of these layers can be found in Sect. 6.2.2.

Finally it is worth highlighting that the used measurement setup only allows testing the sensors in the pressure range 0–1 bar. From Chap. 3 we know that the corresponding working pressure range is different for sensors with different membrane areas (up to 10 bar for $200 \times 200\ \mu m^2$ sensors but only from 0 to 3 bar for $300 \times 300\ \mu m^2$ sensors). However, due to the limitations in the measurement setup, the sensors could not be tested in their whole working range but only under pressures up to 1 bar.

**Table 6.1** Measured and simulated sensitivities for sensors with different membrane areas but the same piezoresistor arrangement (D3)

| Membrane area ($\mu m^2$) | Measured sensitivity (mV/V/bar) | Simulated sensitivity (mV/V/bar) |
|---|---|---|
| $200 \times 200$ | $1.58 \pm 0.1$ | 2.9 |
| $250 \times 250$ | $2.45 \pm 0.15$ | 4.6 |
| $300 \times 300$ | $3.45 \pm 0.06$ | 6.8 |

The number of sensors measured are 10, 7 and 1 for the $200 \times 200$, $250 \times 250$ and $300 \times 300\mu m^2$ areas, respectively.The error bars correspond to the standard deviation of the measured sensitivities data set

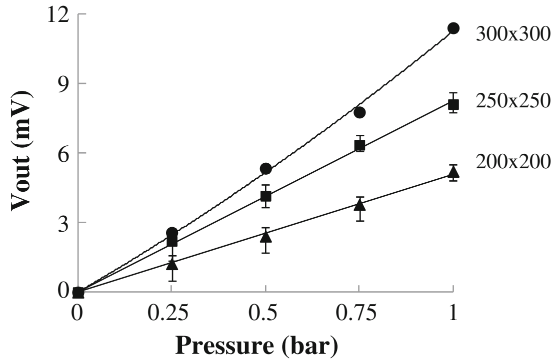



**Fig. 6.4** Measured output voltage (for $V_{bias} = 3.3$ V) as a function of the applied pressure for D3 sensors with different areas (in μm$^2$). The data point at vacuum is taken as reference for the data, to eliminate the bridge offset. The data points are fitted to a linear (for 200 × 200 and 250 × 250 μm$^2$ sensors) or quadratic (for 300 × 300 μm$^2$sensors) functions

### *6.2.1 Sensitivity*

The first design parameters considered in Chap. 3 were the membrane dimensions; since the membrane thickness was fixed by the technology (to 4 μm), only the membrane area could be varied. Figure 6.4 plots the measured output voltage as a function of applied pressure for square-shaped sensors with three different membrane areas: 200 × 200, 250 × 250 and 300 × 300 μm$^2$. All sensors have the piezoresistor arrangement corresponding to D3 (in Fig. 6.3): "m-shape" longitudinal piezoresistors with the transverse piezoresistors placed at the edge (at a distance of 1 μm from the membrane edge). Table 6.1 lists the corresponding sensor sensitivities together with the values predicted by simulations (Chap. 3) for comparison. The sensor sensitivity is calculated as the slope of an "end-point straight line" divided by the bias voltage ($V_{bias}$):

$$S = \frac{V_{out}\left(P_{max}\right) - V_{out}(P_{min})}{V_{\text{bias}}} \times \frac{1}{(P_{max} - P_{min})} \tag{6.1}$$

where $P_{max}$ and $P_{min}$ are 1 bar and 0 bar, respectively. As can be expected, and as was also predicted by simulations (Chap. 3, Sect. 3.1.1), for the same piezoresistor design and membrane thickness, larger sensors exhibit higher sensitivity. Keeping the same piezoresistor design and membrane thickness, by increasing the membrane area from 200 × 200 to 250 × 250 or 300 × 300 μm$^2$, the sensor sensitivity can be improved by a factor of ∼55 % or ∼118 %. This relative increase in sensitivity with sensor area is in good agreement with the results predicted by simulations. However the measured sensitivities are about 80 % lower than the simulated sensitivities; the reason for this mismatch will be analyzed in Sect. 6.2.2.

Apart from the membrane area, also the piezoresistor placement was considered as a design parameter. Figure 6.5 compares the output voltage as a function of applied pressure for 200 × 200 μm$^2$ pressure sensors with piezoresistor designs D1 and D1_T, respectively. The corresponding sensor sensitivities are 1.78 ± 0.07 mV/V/bar and 4.23 ± 0.3 mV/V/bar for D1 and D1_T, respectively. On the other hand, Fig. 6.6 plots the pressure response of 250 × 250 μm$^2$ sensors with designs D2 and D2_T. The

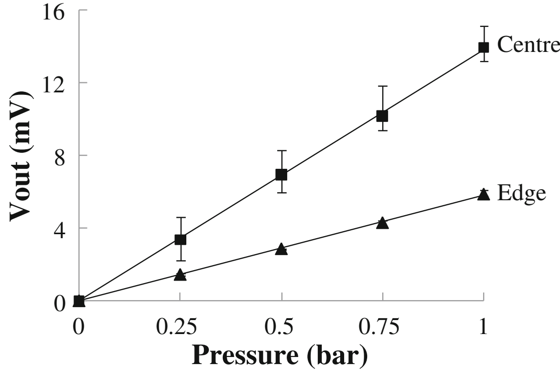



**Fig. 6.5** Measured output voltage (for $V_{bias} = 3.3\,V$) versus external pressure for $200 \times 200\,\mu m^2$ sensors with "single-line" longitudinal piezoresistors and two different placement of the transverse piezoresistors: at the membrane edge or at the centre. The corresponding sensitivities are 1.78 and 4.23 mV/V/bar, respectively. The data point at vacuum is taken as reference for the data, to eliminate the bridge offset

measured sensitivity for D2 is $2.58 \pm 0.2$ mV/V/bar, while D2_T exhibited a sensitivity of $5.91 \pm 0.5$ mV/V/bar. From these results we can conclude that, independently from sensor design and membrane area, by placing the transverse piezoresistors in the centre of the membrane, the sensitivity can be improved by a factor of about 2. This result is in good agreement with the conclusion drawn from the simulations in Chap. 3. As already discussed in Chap. 3, the negative longitudinal stress found in the centre of the membrane, in combination with the small transverse piezoresistive

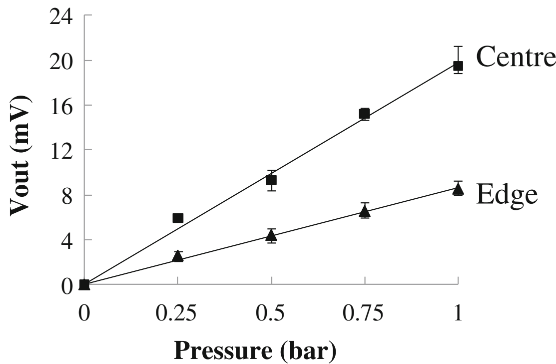



**Fig. 6.6** Measured output voltage (for an input voltage of 3.3 V) versus external pressure for $250 \times 250\mu m^2$ sensors with "n-shape" longitudinal piezoresistors and two different placement of the transverse piezoresistors: at the membrane edge or at the centre. The corresponding sensitivities are 2.58 and 5.91 mV/V/bar, respectively. The data point at vacuum is taken as reference for the data, to eliminate the bridge offset

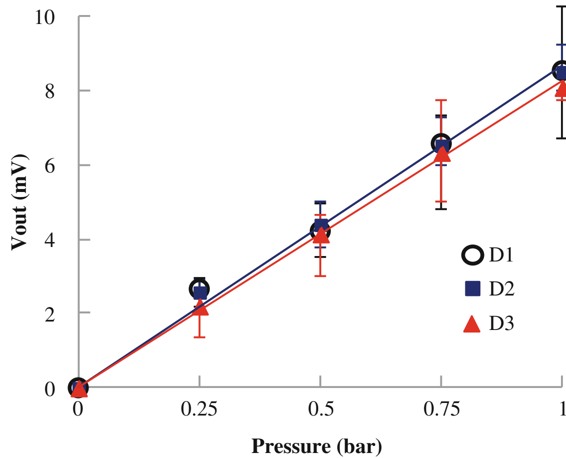



**Fig. 6.7** Measured output voltage (for $V_{bias} = 3.3$ V) versus external pressure for $250 \times 250\ \mu m^2$ sensors with piezoresistor design D1, D2 and D3, respectively. The data point at vacuum is taken as reference for the data, to eliminate the bridge offset

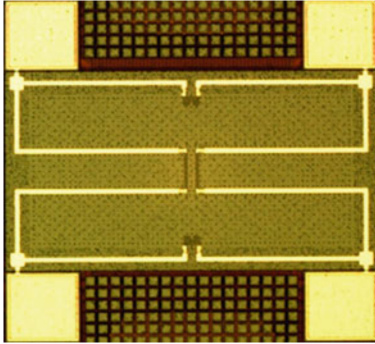
coefficient for poly-SiGe compared to the longitudinal one, explain the improvement in sensitivity by placing the transverse piezoresistors in the centre.

The last design parameter, with regard to the piezoresistors, considered in Chap. 3 was the shape of the longitudinal piezoresistors. Three shapes were studied: "single-line", "n-shape" and "m-shape". Figure 6.7 plots the measured output voltage in the pressure range 0–1 bar for $250 \times 250\ \mu m^2$ sensors with the three different longitudinal piezoresistor shapes mentioned. In all cases the transverse piezoresistors are placed at the membrane edge. In agreement with the simulations, no significant impact of longitudinal piezoresistor shape on the sensor response is observed. As seen in Chap. 3, this is due to the fact that for the three shapes considered, the average induced stress in the resistors as the membrane bends is practically the same.

So far only results corresponding to square-shape sensors have been reported. However, a rectangular sensor of dimensions $350 \times 175\ \mu m^2$ and piezoresistor arrangement corresponding to design D3_T was also fabricated. Figure 6.8 shows a microscope picture of the fabricated rectangular sensor, together with its pressure response.

According to the simulations, this rectangular sensor should offer a sensitivity ~36 % higher than an equivalent $200 \times 200\ \mu m^2$ sensor, while exhibiting the same maximum deflection. From Fig. 6.8, a sensitivity of $5.46 \pm 0.15$ mV/V/bar for the rectangular sensors can be extracted. The measured sensitivity for a $200 \times 200\ \mu m^2$ sensor with the same piezoresistor design (D3_T) was $3.7 \pm 0.3$ mV/V/bar, between 24 and 38 % smaller as compared to the sensitivity of the rectangular sensor. Therefore, there is a relatively good match between the simulated behaviour and the measured response for the rectangular sensor.

To finish this section, Table 6.2 summarizes the measured sensitivities (in mV/V/bar) for the different sensor designs illustrated in Fig. 6.3. For each sensor design, the measured sensitivity for the different membrane areas considered is listed.



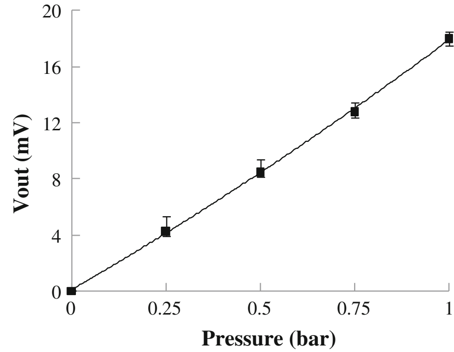



**Fig. 6.8** Microscope picture of a fabricated *rectangular* sensor, together with the measured output voltage vs. pressure (for $V_{bias} = 3.3$ V). The data point at vacuum is taken as reference for the data, to eliminate the bridge offset. The data points are fitted to a quadratic function

**Table 6.2** Measured sensor sensitivities (in mV/V/bar) for the different designs (see Fig. 6.3) and membrane areas considered. The sensors were tested in the pressure range 0–1 bar

| Sensor area ($\mu m^2$) | Sensor designs | | | | | |
|---|---|---|---|---|---|---|
| | D1 | D1_T | D2 | D2_T | D3 | D3_T |
| 200 × 200 | 1.78±0.05 | 4.25±0.3 | 1.73±0.15 | 4.17±0.4 | 1.58±0.1 | 3.7±0.3 |
| 250 × 250 | 2.5±0.1 | 6±0.2 | 2.58±0.2 | 5.91±0.5 | 2.45±0.15 | 5.6±0.4 |
| 300 × 300 | – | – | – | – | 3.45±0.06 | – |
| 350 × 175 | – | – | – | – | – | 5.46±0.15 |

## *6.2.2 Comparison to Simulations*

The measured sensitivities are in good qualitative agreement with the conclusions drawn from simulations in Chap. 3. As predicted by simulations:

- For the same piezoresistor design and membrane thickness, sensors with larger membranes exhibit higher sensitivities.
- By placing the transverse piezoresistors in the centre of the membrane instead of at the edge, the sensitivity is improved by a factor of ∼2.
- No significant impact on sensor sensitivity is observed by using an "n-shape" or
- "m-shape" longitudinal piezoresistor instead of the usual line-shaped resistor.
- For the same design, rectangular poly-SiGe sensors offer higher sensitivities than equivalent sensors (i.e. exhibiting the same deflection for equal external pressure) with square-shaped membrane.

However, the measured sensitivities are considerably smaller than the values predicted by simulations. For instance, for the rectangular sensor a sensitivity of 7.83 mV/V/bar was predicted by simulations (see Chap. 3, Sect. 3.2.6) while the

measured sensitivity was only ~5.5 mV/V/bar. The main reasons for this mismatch between the simulations and the experimental values are listed below.

1. The piezoresistive layer used for the fabrication of the sensor was deposited and annealed at temperatures below 460 °C, which results in smaller piezoresistive coefficients compared to the values assumed in the simulations (corresponding to a poly-SiGe layer deposited at 500 °C and annealed at 570 °C). The right piezoresistive coefficients are $\pi_l = 12.4 \cdot 10^{-11}$ and $\pi_t = 5 \cdot 10^{-11} Pa^{-1}$.
2. The residual stress in the membrane was not considered in the simulations. From Chap. 5 we know that a poly-SiGe membrane sealed with SACVD oxide exhibits a tensile stress in the MPa range. A tensile residual stress results in less deflection [4], and therefore, in a smaller sensor sensitivity.
3. The sensor model used in the simulations was extremely simplified: only the poly-SiGe membrane and piezoresistors were considered. However, the fabricated sensor contains different layers, as shown in Fig. 4.1 in Chap. 4. The most relevant extra layers for the sensor performance are the SiC isolation layer between piezoresistors and membrane and the oxide sealing layer, which increases the total membrane thickness, therefore reducing the pressure deflection and the sensitivity.

Moreover, due to problems with the Al filling of the piezoresistor contacts, the layout of the piezoresistors had to be adapted to allow for bigger contacts (see Chap. 4). As a result, the transverse piezoresistors are no longer "single-line" and the longitudinal piezoresistors had to be extended over the edge of the membrane to allocate the larger contacts. See appendix A for a clear view of the final layout of the sensors. Also the effect of the release holes (decreased Young's modulus) and the movable supports (although its impact was already predicted to be negligible in Sect. 3.2.6) were not taken into account in the simulations.

To better understand the behaviour of the fabricated sensors, new finite element simulations with a more realistic model (including residual stress and all the extra layers) were performed using COMSOL. Table 6.3 lists the different layers included in the model, along with the corresponding material properties and thicknesses. For accuracy, the exact thicknesses of the different layers that constitute the sensors were obtained from cross-section SEM pictures (Fig. 6.9). As can be seen from this Fig. 6.9, the real average thickness of the SiGe membrane is ~3.5 μm, thinner than the expected 4 μm. This is mainly due to three reasons: a mismatch between the targeted poly-SiGe thickness and the deposited one, the CMP step performed after the membrane deposition to smooth the surface, and also the overetch of the membrane during the poly-SiGe piezoresistor patterning (see Chap. 4). Also the SiC isolation layer is thinner than expected (~60 nm instead of the specified thickness of 100 nm).

The Young's modulus of the sealed membrane was obtained using expression (5.4), with $\lambda = 0.967$, $E_{SiGe} = 147$ GPa, $E_{SiO_2} = 60$ GPa, $t_{SiGe} = 3.25\,\mu$m and $t_{SiO_2} = 1.35\,\mu$m. The factor λ is included to account for the effect of the release holes (see Chap. 5). The residual stress in the sealed membrane was obtained

**Table 6.3** Thickness, Young's modulus and residual stress of the different layers that form the sensor

| Layer | Thickness | Young's modulus (GPa) | Residual stress (MPa) |
|---|---|---|---|
| Sealed membrane ($SiGe+SiO_2$) | ~4.6 μm (250 nm + 3.25 μm + 1.1 μm) | 118 | 11 |
| SiC isolation layer | ~60 nm | 150 | 0 |
| SiGe piezoresistor | ~200 nm | 103.5 | 0 |

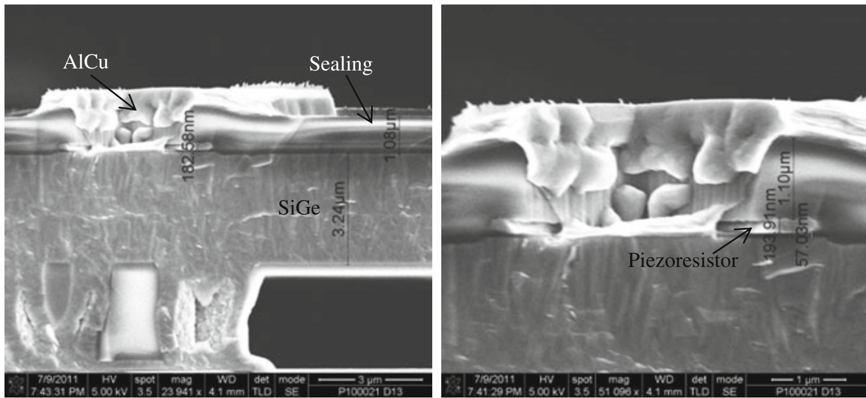



**Fig. 6.9** Cross-section SEM pictures of a fabricated device. The following layers, along with their corresponding thicknesses, are visible: the SiGe membrane, the SiC isolation layer, the SiGe piezoresistors and the oxide sealing layer

in Chap. 5 by applying the load-deflection technique. The residual stresses in the poly-SiGe piezoresistors and SiC isolation layer are unknown, and therefore, set to zero. In any case the residual stresses in the piezoresistor layers are not expected to have an impact on the sensor sensitivity, although they may contribute to the offset voltage.

Figure 6.10 shows the model of a rectangular sensor for the new simulations. The model consists of a 4.6 μm thick-membrane (SiGe + oxide sealing) surrounded by a 25 μm-thick support frame. The poly-SiGe piezoresistors are located on top of the membrane, with a thin layer (SiC) separating the membrane and the piezoresistors. Similar models were constructed for some of the other fabricated sensors. Figure 6.11 and Table 6.4 show a comparison between the simulated and the measured response of sensors with different dimensions and designs. A reasonable agreement (within 25 %) between the measured values and those calculated with the new simulations (including all the layers with the corresponding real thicknesses and residual stress) is obtained. When measuring the longitudinal piezoresistive coefficient ($\pi_l$) of the

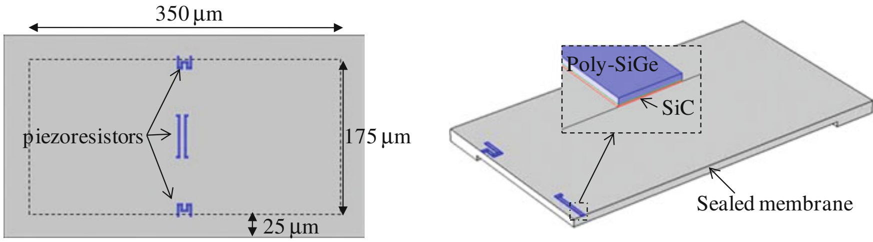
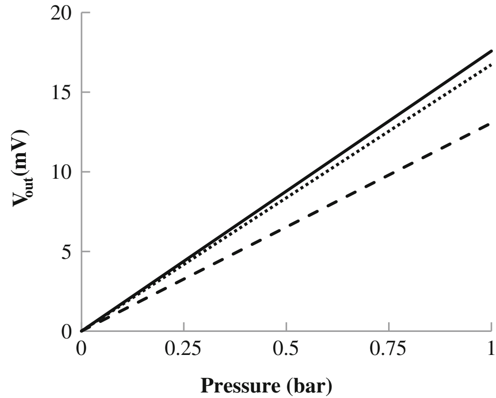



**Fig. 6.10** Model of a *rectangular* sensor including the supports and all the layers that form the membrane and the piezoresistors

**Fig. 6.11** Measured *(continuous line)* and simulated *(dashed line)* pressure response for a *rectangular* sensor. Two simulated responses are included: using $\pi_l = 12.4 \cdot 10^{-11}$ Pa$^{-1}$ *(dashed line)* and with $\pi_l = 16 \cdot 10^{-11}$ Pa$^{-1}$ *(dotted line)*




CMOS-compatible sensing layer (Chap. 2), the calculated mean value was, as mentioned above, $12.4 \cdot 10^{-11}$ Pa$^{-1}$ while the maximum measured value was $16 \cdot 10^{-11}$ Pa$^{-1}$. It is interesting to note that, if instead of the mean value we use $\pi_l = 16 \cdot 10^{-11}$ Pa$^{-1}$ (with $\pi_t = 5 \cdot 10^{-11}$ Pa$^{-1}$) for the simulations, a nearly perfect matching with the measurements can be obtained. This suggested improvement in piezoresistivity could be explained considering the results reported in Sect. 2.4, where a certain increase in gauge factor was observed after extending the annealing from 30 to 60 mins. During the pressure sensor fabrication, the annealing time of the piezoresitors is

**Table 6.4** Comparison between measured and simulated sensitivites for sensors with different areas and design. In all simulations a $\pi_t = 5 \cdot 10^{-11}$ Pa$^{-1}$ was used

| Sensitivity (mV/V/bar) | Rectangular D3_T | 250 × 250 µm$^2$ D2 | 200 × 200 µm$^2$ D2_T |
|---|---|---|---|
| Measured | 5.46 ± 0.15 | 2.58 ± 0.2 | 4.17 ± 0.4 |
| Simulated ($\pi_l = 12.4 \cdot 10^{-11}$ Pa$^{-1}$) | 4 | 1.9 | 3.2 |
| Simulated ($\pi_l = 16 \cdot 10^{-11}$ Pa$^{-1}$) | 5.1 | 2.6 | 4 |

30 min at 455 °C. However, after this annealing the piezoresistors must still undergo some extra processing steps at relatively high temperatures, like the SACVD oxide sealing deposition, performed at 420 °C. These subsequent high temperature steps could influence the piezoresistive coefficients, partially explaining the good match when using a larger $\pi_l$ value.

On the other hand, several other factors could play a role. The thicknesses of the layers were estimated from a cross-section picture. However, due to thickness variations across the wafer, it is possible that for some of the measured sensors the membrane or the SiC isolation layer are actually thinner, resulting in a higher sensitivity. Also variations in the assumed Young's modulus or residual stresses in the layers (Table 6.3) could play a role. With so many unknown variables it is difficult to conclude if the piezoresistivity of the poly-SiGe resistors really improved during the pressure sensor fabrication flow.

### 6.2.3 *Offset*

As explained in Chap. 3, the offset voltage represents the output of the pressure sensor without any pressure being applied. Ideally, it should be zero. During the sensor design, special care was taken to ensure an equal resistance value for the four piezoresistors in the Wheatstone bridge, in order to obtain a zero offset voltage. However, the fabricated sensors exhibited very high offsets. Also, a large offset spread is observed. For example, the offset measured for 7 rectangular sensors across the wafer was 1 ± 90 mV (for 3.3 V applied voltage). In general, offset values between −182 and 105 mV were measured, with no observable correlation between offset and sensor dimensions or design. Table 6.5 lists the measured offsets for the different designs.

The large offset spread can be attributed to an unbalance of the resistivity values of the Wheatstone bridge induced by variations in the fabrication process (piezoresistor ion implantation or non-uniformity in the poly-SiGe piezoresistor thickness across the wafer). These possible process variations would also explain the large variations in the resistivity of the piezoresistive layer, reported in Chap. 2. On the other hand, cross-section pictures in Chap. 4 showed that the Al filling of the piezoresistor contacts was also not perfect; differences in the contact resistances for different resistors can

**Table 6.5** Mean values of offset voltage (in mV) for pressure sensors with different dimensions and desings (see Fig. 6.3). The bias voltage is, in all cases, 3.3 V

| Sensor area ($\mu m^2$) | Sensor Designs | | | | | |
|---|---|---|---|---|---|---|
| | D1 | D1_T | D2 | D2_T | D3 | D3_T |
| 200 × 200 | − 15 ± 70 | −56 ± 100 | −35 ± 120 | −49 ± 130 | 18 ± 60 | −50 ± 70 |
| 250 × 250 | −62 ± 60 | 53 ± 50 | −13 ± 100 | −29 ± 35 | −26 ± 80 | −73 ± 40 |
| 300 × 300 | – | – | – | – | 6.5 | – |
| 350 × 175 | – | – | – | – | – | 1 ± 90 |

also lead to large offset values, with a big spread. Finally, the residual stresses in the sensor layers, together with the residual pressure inside the cavity, can also contribute to the sensors voltage offset, although to a lesser extent than process variations or bad contacts.

### 6.2.4 Nonlinearity

As can be seen from Figs. 6.4, 6.5, 6.6, 6.7, 6.8, most of the tested sensors exhibited a quite linear pressure response in the 0 to 1 bar pressure range. Only the pressure response of the rectangular and the 300 × 300 $\mu m^2$ sensors showed clearly some nonlinearity. The corresponding calculated nonlinearity values are $\sim -4\,\%$ and $\sim -2.86\,\%$ for the 300×300 $\mu m^2$ and the rectangular sensors, respectively. Although, due to the relative big error in the measurement data points, it is difficult to accurately calculate the nonlinearity of the fabricated sensors.

These measured nonlinearity (NL) values are much higher than those predicted by simulations. Taking as an example the rectangular sensor, the measured NL ($\sim -2.86\,\%$) is about 20 times higher than the value given by simulations in Sect. 3.2.5 (0.114 %). This large mismatch can be due to the fact that, in the simulations, only the structural nonlinearity was considered, while the bridge nonlinearity or the nonlinearity in the piezoresistive effect of the poly-SiGe resistors was neglected. Other possible reasons for the measurements/simulations disagreement can be inaccuracies in the measurements, the thinner membranes of the fabricated sensors as compared to the thickness considered in the simulations, effect of release holes, etc.

Despite this quantitative mismatch, the calculated nonlinearity values do show a good qualitative agreement with the trends predicted by simulations. In this sense, for the same design, larger sensors do indeed exhibit higher nonlinearity; for example, the NL for the 300 × 300 $\mu m^2$ sensor is $\sim -4\,\%$, as mentioned above, while a 200 × 200 $\mu m^2$ with the same design exhibits a NL of $\sim -1.5\,\%$, around three times smaller. On the other hand, no effect of the longitudinal piezoresistor shape on the NL is observed. For a membrane area of 200 × 200 $\mu m^2$, sensors with design D1 (linear longitudinal resistor) exhibited a NL $\sim -1.5\,\%$, while a sensor with design D2 ("n-shape" resistor) exhibited a NL $\sim -1.3\,\%$.

Finally, sensors with the transverse piezoresistors placed in the centre of the membrane showed similar NL than equivalent sensors with the transverse piezoresistors placed at the edge. For example, 200 × 200 $\mu m^2$ sensors with designs D1_T and D2_T showed NL of $\sim -2\,\%$ and $\sim 1.6\,\%$, respectively, very similar to the NL values for designs D1 and D2 ($\sim -1.5\,\%$ and $\sim -1.3\,\%$). However, according to simulations, the sensors with the transverse piezoresistors placed at the edge are expected to show higher NL, as the stress nonlinearity is expected to be larger at the membrane centre (see Sect. 3.2.2). This apparent disagreement is due to the fact that the fabricated pressure sensors could only be tested in the pressure range 0 to 1 bar, and not in their full-working pressure range. Considering Fig. 3.14 (for a 250 × 250 $\mu m^2$ sensor), the larger NL when the transverse piezoresistors are placed in the centre of the mem-

brane is only visible for pressures higher 2 bar, while in the tested pressure range (0 to 1 bar), both placements (central and edge) behave the same.

### 6.2.5 Thermal Behaviour

Temperature coefficients of sensitivity (TCS) and offset (TCO) have been obtained for a temperature range from 25 to 125 °C. The measurement pressure range was, again, 0–1 bar. The temperature was increased in steps of 25 °C, and was stabilized for at least 1.5 h after reaching each programmed value. During the stabilization time the chamber pressure was held at a low level (few mbars). Pressure response characteristics for each of the considered temperatures have been obtained by increasing the pressure up to 1 bar (in 0.5 bar steps) and measuring the output voltage of the sensor (applying an input voltage sweep from 0 to 3.3V).

The fabricated sensors are comprised of several materials, such as poly-SiGe, Si-oxide, SiC, and AlCu (for the metal interconnects). The mismatch between the thermal expansion coefficients (CTE) of the different materials will cause thermal-induced stresses as the temperature changes, and hence lead to variations in the sensor output voltage. On the other hand, the gauge factor of the poly-SiGe piezoresistors is also expected to be sensitive to temperature. In silicon, the gauge factor drops with increasing temperature due to decreasing strain sensitivity with increasing temperature, which is associated with inter-valley electron-transport phenomena [5]. The temperature coefficient of gauge factor for poly-Si has been found to be $\sim -0.1$ %/°C [6–8]. For poly-SiGe, it has not been determined. Finally, also the trapped gas effects [9] (variation in the cavity pressure with temperature) will cause a temperature drift in the sensor performance.

For the piezoresistive pressure sensors tested in this work, the sensitivity was found to decrease with temperature. The output voltage versus applied pressure for a rectangular sensor at room and elevated temperatures is shown in Fig. 6.12. The sensor sensitivity (also shown in Fig. 6.12) is reduced from ∼5.46 mV/V/bar at room temperature to ∼5.01 mV/V/bar at 125 °C, which translates into a TCS (relative to the sensitivity at room temperature) of $\sim -820$ ppm/°C. All the average TCS values measured for the sensors in this work remain within $-800$ and $-2{,}500$ ppm/°C. Table 6.6 lists the obtained TCS values for sensors with different dimensions and designs. No correlation between sensor design and TCS was observed.

Compared to the TCS, the TCO data showed more spread. TCO values between $-0.05$ and 0.06 mV/°C (for an input voltage of 3.3 V) were measured. This spread can be attributed to the same mechanisms that explained the large variations in offset voltage for different sensors. As an example, Fig. 6.13 shows the measured temperature drift of the voltage offset of a rectangular sensor.

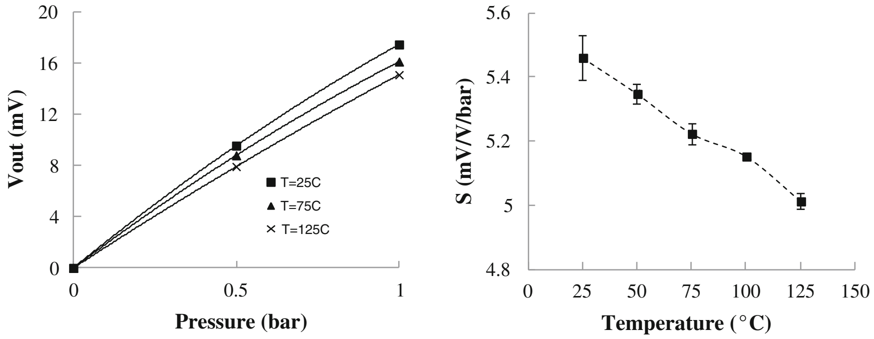



**Fig. 6.12** Ouput voltage vs. pressure for different temperatures (*left*) and temperature drift of the sensitivity (*right*) of *rectangular* sensors

**Table 6.6** Average TCS values ($\times 10^3$ ppm/°C) measured in the temperature range 25–125 °C for piezoresistive pressure sensors with different membrane areas and designs (from Fig. 6.3)

| Sensor area ($\mu m^2$) | Sensor Designs | | | | | |
|---|---|---|---|---|---|---|
| | D1 | D1_T | D2 | D2_T | D3 | D3_T |
| 200 × 200 | $-0.8 \pm 0.2$ | $-2 \pm 0.4$ | $-2 \pm 0.5$ | $-1.3 \pm 0.5$ | $-2.5 \pm 1$ | $-2 \pm 0.25$ |
| 250 × 250 | $-1.74$ | $-1.3$ | $-2 \pm 0.2$ | $-1.2 \pm 0.25$ | $-1.5 \pm 1$ | $-1.2 \pm 0.2$ |

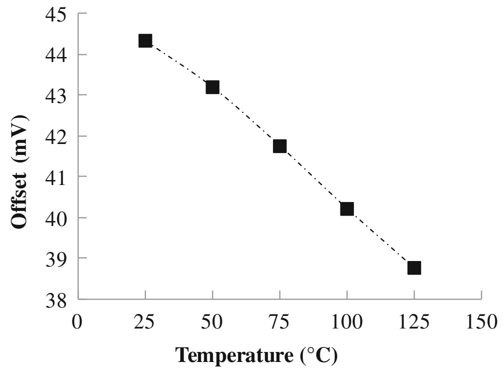



**Fig. 6.13** Measured temperature variation of the voltage offset (for an applied voltage of 3.3 V) of one *rectangular* sensor

## 6.3 Summary and Conclusions

The fabricated pressure sensors have been tested in the pressure range 0 to 1 bar. The impact of membrane area and piezoresistor design on performance parameters such as sensitivity, nonlinearity and offset voltage has been studied. Sensitivities between 1.5 and 5.5 mV/V/bar have been obtained, with nonlinearity errors below 4 %. The temperature dependence of the sensors was also characterized in the temperature range 25–125 °C.

In general, good qualitative agreement to simulations is observed:

- Larger sensors exhibited higher sensitivity but also higher nonlinearity errors.
- By placing the transverse piezoresistors in the centre, instead of at the edge, the sensitivity could be improved by a factor of ∼2. However, no impact of the longitudinal piezoresistor shape on sensor performance is observed.
- The use of rectangular instead of square-shaped membranes is beneficial for the sensor sensitivity.

However, the obtained sensitivities are substantially lower than the values predicted by the simulations in Chap. 3. One reason for this mismatch is the use of a piezoresistive layer processed at temperatures below 460 °C, which results in smaller piezoresistive coefficients compared to the values assumed in the simulations. Moreover, in the simulations performed in Chap. 3 the SiC isolation layer between piezoresistors and membrane was not considered. Also, the oxide sealing layer, which increases the total membrane thickness and reduces the pressure deflection and the sensitivity, was not taken into account. New simulations, including all these extra layers with the residual stresses, were proposed in this chapter; a good matching, within 25 %, with the measured values is observed.

Despite not being designed for any specific application, and not including circuit compensation, the performance of the fabricated pressure sensors is comparable to commercially available devices (Table 6.7). Only the offset voltage and the nonlinearity (NL) seem to be out of range. To reduce the offset of the sensors, we could try to improve the piezoresistor/metal contact (it will reduce contact resistance value and spread) and the uniformity of the piezoresistive layer (from Chap. 2 we know the electrical and piezoresistive properties of this layer exhibits great variability across the wafer). From Chap. 3 we know that one possibility to reduce the nonlinearity error of the pressure sensors is to decrease the area/thickness ratio of the membranes (i.e. use smaller and/or thicker membranes). However, this will come at a cost of deteriorated sensitivity. Several structures, based on a local stiffening of the membrane while the resistors are kept in a local concentration area, have been reported in order to improve the linearity minimizing the sensitivity loss. Mallon et al. [15] used a square diaphragm with a concentric boss, while the resistors were kept in the thinner rim surrounding the boss. An alternative mechanical structure is the double-island diaphragm proposed by Wilner [16].

On the other hand, by substituting the SACVD oxide by a sealing layer with a coefficient of thermal expansion (CTE) closer to the CTE of the poly-SiGe structural layer, the temperature dependence could also be reduced. One option might be to use SiGe (for example an undoped layer) also as sealing layer. It would also be beneficial to have vacuum-sealed cavities, as this will eliminate the trapped gas effects [9]. Finally, for certain applications, especially for biomedical and consumer electronics, larger sensitivities are required. However, the sensitivity of the sensors can easily be adjusted by external circuitry, for example by using a CMOS amplifier, as will be seen in next chapter.

**Table 6.7** Typical performance parameters of commercially available silicon piezoresistive pressure sensors

| Parameter | Ge NPP-301 [10] | IMIT [11] | Ge P562series [12] | Freescale[a] MPX2300DT1 [13] | Freescale MPX10series [14] | This work |
|---|---|---|---|---|---|---|
| Application | General purpose | General purpose | Medical | Medical | General purpose | General purpose |
| Vbias (V) | 3 | 5.6 | 1 | 6 | 3 | 3.3 |
| FS (bar) | 0–1, 0–2 or 0–7 | 0–1 | 0–0.13 | 0–0.4 | 0–0.1 | 0–1 |
| Sensitivity (mV/V/bar) | 20, 10 or 3 | ~10 | 33 | 3.75 | ~115 | 1.5–5.5 |
| FSS (mV) | $60 \pm 20$ | 50 | – | 9 | 35 | 5-20 |
| Voff (mV) | 30 | $\pm 70$ | $\pm 4$ | $\pm 0.75$ | 20 | $\sim \pm 150$ |
| NL (%) | $\pm 0.2$[b] | <1 | 1.5 | $\pm 1.5$ | $\pm 1$ | $\leq 4$ |
| TCO (mV/°C) | $\pm 2.4 \cdot 10^{-3}$ | 0.5 | 0.03 | $\pm 9 \cdot 10^{-3}$ | $\pm 15 \cdot 10^{-3}$ | $\pm 0.05$ |
| TCS (ppm/°C) | $-2000$ | 1000 | $-1100$ | $\pm 1000$ | $-2500$ | $\sim[-1000, -2000]$ |
| Membrane area (mm) | Package $5 \times 6$ mm$^2$ | $0.8 \times 0.8$ | $1 \times 1$ | – | – | $0.2 \times 0.2 - 0.3 \times 0.3$ |
| Membrane thickness (μm) | – | 15 | 400 | – | – | ~3.5 |

[a] This sensors include calibration and temperature compensation circuitry
[b] Linearity error calculated using best-fit straight line
The data obtained for the poly-SiGe fabricated in this work is included for comparison

## 6.4 Capacitive Pressure Sensors

Although the first pressure sensors introduced in the market relied on the piezoresistive sensing principle, in the last years capacitive pressure sensors have attracted increasing attention. Capacitive pressure sensors offer a series of advantages over its piezoresistive counterparts: higher sensitivity, lower power consumption, decreased temperature drift or superior long-term stability [19]. These features make them especially attractive in biomedical implant devices, or in other telemetry applications, where high sensitivity is needed and power is not randomly available. Despite these interesting features, capacitive pressure sensors still present a series of drawbacks with respect to piezoresistive sensors, like larger nonlinearity or a somewhat higher complexity of the interface circuit. Moreover, capacitive sensors do not benefit from the continued MEMS miniaturization. Since the value of the capacitor is directly related to its size, a smaller capacitor would mean higher noise susceptibility. On the other hand, the above-CMOS monolithic integration could be potentially more interesting for capacitive than for piezoresistive pressure sensors, as will be discussed at the end of this section.

Since the focus of this work was the study of poly-SiGe piezoresistive pressure sensors, no specific design or process flow was developed for capacitive pressure sensors. However, in order to highlight the versatility of poly-SiGe for MEMS sensor applications, in some of the fabricated piezoresistive pressure sensors, electrodes were included under the membranes in order to allow also for capacitive measurements. Figure 6.14 shows a microscope picture of one of these piezoresistive/capacitive sensors, together with a schematic cross-section. A 400 nm-thick SiGe electrode is included below the sensor membrane. As the membrane deflects under the action of an external pressure, the capacitance between the SiGe membrane, which acts as the top flexible electrode, and the bottom SiGe electrode will increase. The sensor membrane is connected to the corresponding bondpad via the SiGe electrode layer. On the other hand, an AlCu line runs below the sensor anchors to provide electrical connection to the SiGe electrode. Tungsten (W) filled vias are used to connect the AlCu line to the SiGe electrode. All the capacitive sensors mentioned in this section are also piezoresistive sensors, none only-capacitive sensors were fabricated. The only difference between this type of sensors and the only-piezoresistive sensors is, as mentioned above, the inclusion of the bottom SiGe electrode plus the two extra bondpads connected to the SiGe and the bottom electrode, respectively.

In this work, different areas for the sensor membrane ($200 \times 200$, $250 \times 250$ and $300 \times 300\ \mu m^2$) and for the SiGe electrodes ($50 \times 50$, $100 \times 100$, $150 \times 150$ and $200 \times 200\ \mu m^2$) were considered. Two different gap depths (distance between the movable membrane and the bottom electrode) were considered: 1 and 3 $\mu$m. The gap depth is defined by the thickness of the sacrificial oxide.

Similar as the piezoresistive sensors, the capacitive pressure sensors were tested in the range 0–1 bar in a Suss Microtech PMV-150 environmental chamber. To measure the capacitance change, the Agilent E4980A precision LCR (Inductance (L), Capacitance (C) and Resistance (R)) meter was used. The high measurement accuracy

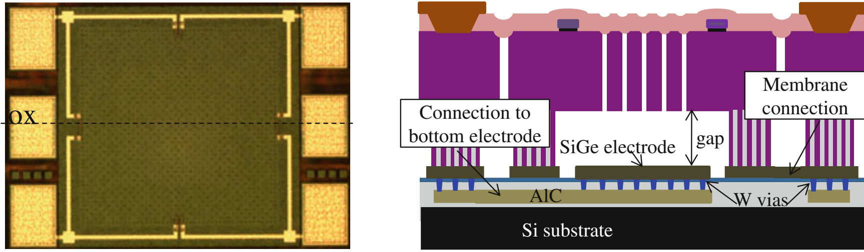



**Fig. 6.14** Microscope picture of a fabricated piezoresistive/capacitive pressure sensor. On the *right*, schematic cross-section of such a device; the AlCu connection *line*, the SiGe *bottom* electrode and the tungsten (W) vias are indicated

and stability ($\sigma < 1$ fF) of this LCR meter allows small capacitances to be measured with sub-femto farad resolution [17]. It also includes cable compensation features to minimize errors caused by the extension cables. Thanks to these characteristics, this LCR meter is suitable for accurate measurements of small capacitances, in the range of fF, as is the case in this work.

All measurements were performed at room temperature, at a frequency of 100 kHz and a voltage level of 1 V. Before each set of capacitance vs. pressure measurements, a calibration step (with the probes separated from the bondpads) is performed. In this way the contribution from the parasitic capacitance between the measurement probes can be eliminated. To minimize possible errors in capacitance reading due to the relative displacement of the measurement probes, the probes remain fixed while the pressure is varied from 0 to 1 bar. This means that, in each pressure sweep, only one capacitive sensor is measured. Figures 6.15, 6.16, 6.17 show the obtained measurement results for capacitive sensors with different membrane and electrode areas, and different gap depths.

Figure 6.15 plots the capacitance change with pressure as a function of electrode area, keeping the membrane area constant. As can be expected, both the reference capacitance value at 0 bar and the capacitance variation increase with electrode area. For a sensor with a bottom electrode of $50 \times 50\ \mu\text{m}^2$, the measured sensitivity is $8.7 \pm 0.3$ fF/bar. By increasing the electrode area up to $100 \times 100\ \mu\text{m}^2$, the sensitivity can be improved by a factor of $\sim$38 %; if an electrode of $150 \times 150\ \mu\text{m}^2$ is used instead, the total sensitivity increase would be $\sim$64 %. Figure 6.16 a illustrates the effect of membrane area on the capacitance variation with pressure with fixed electrode area. Increasing the membrane area from $250 \times 250\ \mu\text{m}^2$ to $300 \times 300\ \mu\text{m}^2$ while keeping the electrode area constant ($100 \times 100\ \mu\text{m}^2$) results in a moderate increase in sensor sensitivity, from $12 \pm 0.5$ fF/bar to $13.5 \pm 0.25$ fF/bar ($\sim$12 %). Therefore, increasing the sensor membrane only is not an efficient method to improve sensor sensitivity; the electrode area should also be scaled accordingly (Fig. 6.16 b).

On the other hand, a decrease in gap depth translates into a drastic increase in sensor sensitivity (Fig. 6.17). The measured sensitivity for a $200 \times 200\ \mu\text{m}^2$ sensor with a $100 \times 100\ \mu\text{m}^2$ electrode and a gap of 1 μm is $47.9 \pm 2.5$ fF/bar, almost 300 %

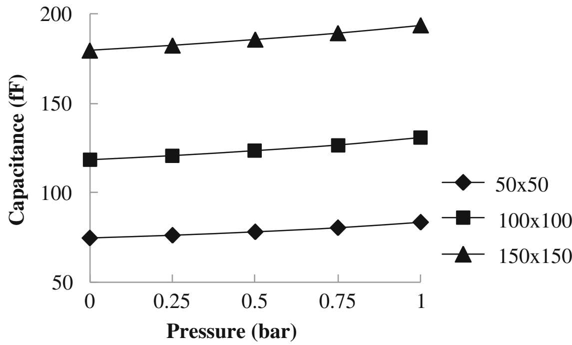



**Fig. 6.15** Capacitance vs. external pressure for $250 \times 250\ \mu m^2$ sensors with three different *bottom* electrode areas = $50 \times 50$, $100 \times 100$ and $150 \times 150\ \mu m^2$. The gap is, for all cases, 3 μm

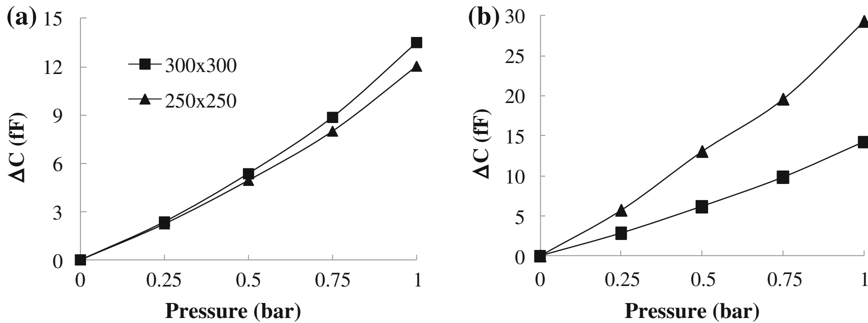



**Fig. 6.16** **a** Capacitance variation vs. pressure for sensors with different membrane areas (in $\mu m^2$). In all cases the *bottom* electrode area is $100 \times 100\ \mu m^2$ and the gap depth, 3 μm. **b** Effect of membrane and electrode area increase on the sensor sensitivity: the curve with triangle markers corresponds to a $300 \times 300\ \mu m^2$ sensor with a $200 \times 200\ \mu m^2$ electrode; the square markers represent a $250 \times 250\ \mu m^2$ sensor with a $150 \times 150\ \mu m^2$ electrode. Both in **a** and **b** the capacitance value at 0 bar is taken as reference

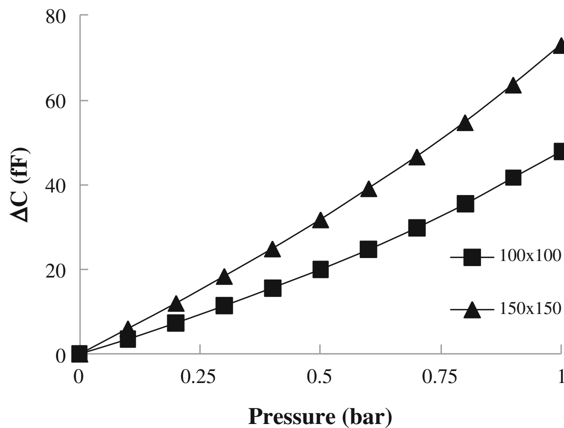



**Fig. 6.17** Capacitance variation vs. pressure for $200 \times 200\ \mu m^2$ sensors with two different bottom electrode areas: $100 \times 100$ and $150 \times 150\ \mu m^2$. The gap depth is 1 μm. The capacitance value at 0 bar is taken as reference

higher than for a $250 \times 250\ \mu m^2$ sensor with equal electrode and a gap of 3 μm, despite the lower membrane area. Sensors with smaller gap seem also more sensitive to variations in electrode area.

The highest measured sensitivity in this work is $73 \pm 3$ fF/bar, and corresponds to a $200 \times 200\ \mu m^2$sensor with a gap of 1 μm and an electrode with an area of $150 \times 150\ \mu m^2$. This sensor has a 0-pressure capacitance of $377.5 \pm 2$ fF and the nonlinearity (in the pressure range 0 to 1 bar) is 6.5 %. If higher sensitivities are required, an array of such sensors could be used. Thanks to the low processing temperature of the described sensor, relative large arrays can be integrated with the readout electronics without extra die consumption. Taking as an example the readout circuit described in [18], with a total area of 2 mm $\times$ 2 mm, an array of 8 $\times$ 8 sensors, with a total sensitivity $\sim$4.7 pF/bar, could be implemented without extra die consumption. That is, the total die area of the integrated sensor (MEMS + CMOS) would still be equal to the CMOS-only area (2 mm $\times$ 2 mm).

The possibility of post-processing on top of CMOS thanks to the use of poly-SiGe as structural layer can be more interesting for capacitive than for piezoresistive pressure sensors. On one hand, as explained above, the benefit of area saving is more pronounced in the case of capacitive applications where usually relatively large arrays of devices are employed (the total MEMS area is therefore larger than for piezoresistive sensors). On the other hand, the impact of parasitic reduction on device performance is also more obvious in capacitive sensors than in piezoresistive pressure sensors. The source capacitance of capacitive pressure sensors is relatively small, causing the sensitivity to parasitics and noise to be relatively high (higher than for piezoresistive sensors) [20]. Thanks to the above-CMOS integration, the parasitics introduced by interconnects will be reduced, translating into an improved sensor performance [21].

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# Chapter 7
# CMOS Integrated Poly-SiGe Piezoresistive Pressure Sensor

This chapter describes the fabrication and testing of an integrated poly-SiGe-based piezoresistive pressure sensor directly fabricated above 0.13 μm Cu-backend CMOS technology. This represents not only the first integrated poly-SiGe pressure sensor directly fabricated above its readout circuit, but also the first time that a poly-SiGe MEMS device is processed on top of Cu-backend CMOS. In the past, imec already proved the potential of poly-SiGe for MEMS-above-CMOS integration by presenting, for example, an integrated poly-SiGe micromirror array and an integrated gyroscope , both of them fabricated on top of Al-based CMOS. However, the aggressive interconnect scaling, essential to the continuation of Moore's law, has led to the replacement of the traditional aluminum metallization by copper metallization, due to its lower resistivity and improved reliability.

The described integrated sensor includes a surface-micromachined poly-SiGe based piezoresistive pressure sensor (fabricated following the process flow described in Chap. 4) and an instrumentation amplifier that acts as the sensor readout circuit. The amplifier has been fabricated using imec's 0.13 μm CMOS technology, with Cu- interconnects (two metal layers), oxide dielectric and Cu-filled metal-to-metal vias. The chapter begins with a description of the design, fabrication and testing of the instrumentation amplifier used as the sensor readout circuit. The processing of the integrated sensor is explained next, with special attention to the development of the CMOS (Cu) to MEMS (Al) interface. The effect of the MEMS processing on the underlying CMOS performance is also characterized. Finally, the performance of the fabricated integrate sensor is evaluated.

## 7.1 The Sensor Readout Circuit: An Instrumentation Amplifier

A typical signal conditioning circuit for a piezoresistive pressure sensor comprises the following blocks (Fig. 7.1) [1]: a biasing circuit, an amplifier, a temperature compensation stage, an offset compensation stage and, in case digital output is required,

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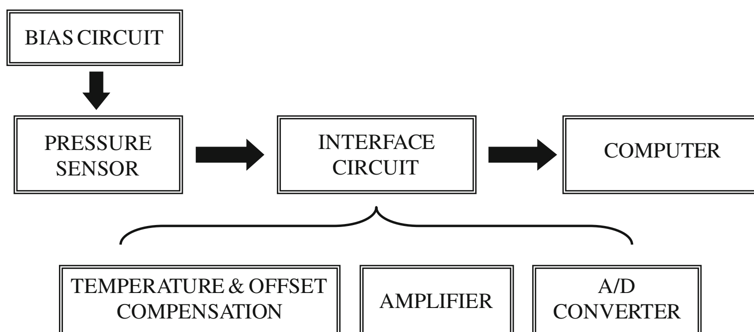


**Fig. 7.1** Basic block diagram of a typical signal conditioning circuit for piezoresistive pressure sensors

an analog-to-digital converter. The biasing circuit provides the electrical excitation to the sensor bridge. An amplifier is needed due to the typically weak electrical output signal of piezoresistive sensors. Since the bridge output is not only sensitive to pressure but also to temperature, compensation for the temperature drift is important, especially for high accuracy applications. Some read out circuits may also include a linearization stage to compensate for the nonlinearity in the sensor output.

The zero pressure offset and, in general, the errors caused by processing variations can effectively be handled by the double-bridge compensation technique [2]. It makes use of two piezoresistive Wheatstone bridges: one fabricated on top of the movable sensor membrane while an identical compensation bridge is located on a rigid, non-release part of the sensor chip. The output of the first bridge is, therefore, a function of pressure, temperature and process variations, whereas the compensation bridge response is dependent on temperature and process variations only. The difference of the two bridge outputs removes the voltage offset and any other effect of process variations. Another possibility for compensation of zero-pressure voltage offset and TCO is to connect, in parallel with each of the four bridge piezoresistors, an electrically adjustable resistor with independent adjustment of its total resistance and TCR [3]. By trimming one or more of these adjustable resistors, the offset and TCO can be compensated. Yet another option to cancel the offset could be to power each of the two arms of the sensor Wheatstone bridge by an independent current source; by adjusting the value of the input currents, a zero offset can be achieved.

One of the main reasons for the sensor sensitivity to temperature is the variation of the piezoresistive effect with temperature. A simple way of compensating the TCS is to power the sensor with current instead of voltage. In this way, the TCS will be a function of both the temperature coefficient of piezoresistivity and the TCR of the bridge resistors, which are opposite in sign (depending on the doping concentration). A better compensation, proposed in [4], is to power the sensor with a voltage controlled current source with a pre-defined thermal coefficient, which should have an absolute value close in magnitude but opposite in sign to the sensor TCS. Another scheme for temperature drift cancellation, proposed in [5], is to divide

the sensor Wheatstone bridge in two half bridges with a common reference arm. The output voltages of each half-bridge are amplified separately by a differential amplifier. The gains of the amplifiers are adjusted so that the temperature sensitivities of the half-bridge output voltages cancel each other.

Even though, as can be concluded from the results reported in Chap. 6, the fabricated poly-SiGe pressure sensors in this work exhibited large offsets and a pronounced temperature drift, due to time and resources limitations, the designed sensor readout includes only an amplification circuitry, with no temperature compensation. In any case, as the objective of this work is not to provide a complete integrated sensor suitable for commercial applications but just a demonstrator of the above-CMOS integration capabilities of poly-SiGe, a simple amplifier can be considered enough for this purpose.

The main requirements for an amplifier to be used at the output of a resistive bridge sensor are [6]: relatively high gain, high common mode rejection ratio (CMRR) and high input impedance, to avoid loading the resistive bridge, altering its functioning. One amplifier circuitry fulfilling these requirements, widely used in piezoresistive pressure sensors applications, is the instrumentation amplifier. An instrumentation amplifier (in-amp) [7, 8] is a differential operational amplifier (op-amp) circuit with two high impedance input terminals, which provides effective rejection of the dc common-mode voltage appearing at the two bridge outputs, while amplifying the weak bridge signal voltage. An in-amp employs an internal feedback resistor network that is isolated from its signal input terminals. The gain of the instrumentation amplifier is controlled by the values of these resistors and can be easily adjusted.

### *7.1.1 Design*

The designed amplifier is a classic three-op-amp instrumentation amplifier as shown in Fig. 7.2. The amplifier was designed using a modified version of the imec 0.13 μm technology, with thicker oxide to allow for a higher bias voltage (3.3 V instead of 1.2 V). A higher bias voltage was preferred as the sensor output is directly proportional to the input voltage (as was already seen in Chap. 3). The minimum allowed gate length is 0.35 μm. Spectre, from the Cadence Virtuoso platform [9], was used for the circuit simulations.

The three op-amps is the most straight forward implementation of an instrumentation amplifier. It consists of two non-inverting input buffer amplifiers, followed by a difference amplifier. The two amplifiers on the left, connected in a buffer configuration, provide the high input impedance to the amplifier, necessary to avoid loading the sensor. The third amplifier is used to subtract the two gained input signals, providing a single ended output. The gain of this circuit is determined by the internal feedback resistor network according to expression (7.1):

$$V_{out} = \left(V^{+} - V^{-}\right) \times \left(1 + \frac{2R_1}{R_{gain}}\right) \cdot \frac{R_3}{R_2} \tag{7.1}$$

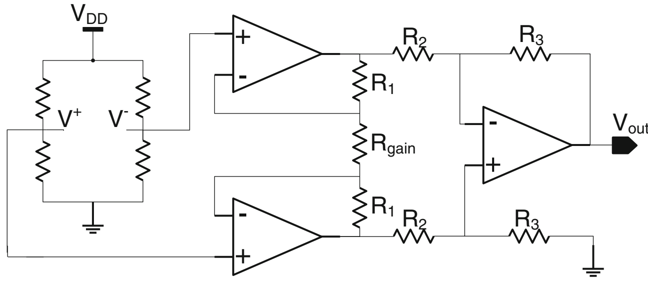


**Fig. 7.2** Schematic of the integrated sensor designed in this work: on the *left*, the resistive Wheatstone bridge representing the pressure sensor, and on the *right*, the instrumentation amplifier that acts as the sensor readout circuit

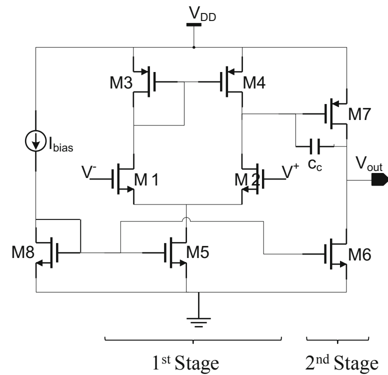


**Fig. 7.3** Schematic of a classic two-stage Miller compensated op-amp with an n-channel input differential pair and a p-channel common-source amplifier at the output

where $V^+ - V^-$ represents the differential output of the sensor bridge. Ideally, the common-mode gain of an instrumentation amplifier should be zero. However, mismatches in the values of the equally-numbered resistors and in common mode gains of the two input op-amps result in a non-zero common-mode gain.

All the three op-amps in the instrumentation amplifier are classic two-stage Miller differential-input, single-output op-amps [10, 11] as depicted in Fig. 7.3. This simple op-amp provides good CMRR, output swing and voltage gain. The first stage consists of an n-channel differential pair $M_1 - M_2$ with a p-channel current mirror load $M_3 - M_4$ and an n-channel tail current source $M_5$. The second stage consists of a p-channel common-source amplifier $M_7$ with an n-channel current-source load $M_6$. For biasing purposes, a single input current source is needed; transistor $M_8$ provides the mirror current for both $M_5$ and $M_6$. A compensation capacitor connects the output of the second stage back to the output of the first stage. This capacitor adds stability through the so-called pole splitting Miller compensation [11–13].

The main design specifications considered in this work for the op-amps were high gain and good phase margin ($\geq 60°$). The phase margin (PM in Fig. 7.4) is a measure of stability in a feedback system; it represents the difference between the phase (in degrees) of the amplifier output signal and $-180°$, measured at the unity-gain

**Table 7.1** Final transistor dimensions (W/L), compensation capacitor ($C_c$) and bias current ($I_{bias}$) for the two types of op-amps designed. The transistors gate width (W) and length (L) are expressed in μm

| Device | Input OP-AMPS | | Output OP-AMP | |
|---|---|---|---|---|
| | W | L | W | L |
| $M_{1,2}$ | 2 | 8 | 2 | 8 |
| $M_{3,4}$ | 2 | 8 | 2 | 8 |
| $M_5$ | 2 | 4 | 2 | 4 |
| $M_6$ | 20 | 4 | 40 | 4 |
| $M_7$ | 10 | 1 | 5 | 1 |
| $M_8$ | 2 | 4 | 2 | 4 |
| $C_c$ | 2 pF | | 2 pF | |
| $I_{bias}$ | 10 μA | | 2 μA | |

frequency. In most of the cases, 60° phase margin is considered an optimum one. A 60° phase margin will also allow for the fastest settling time when attempting following a voltage step input. For the two input op-amps (Fig. 7.2), apart from high gain and safe phase margin, also high output current is required in order to be able to drive the resistor network in the instrumentation amplifier.

The design parameters include transistor dimensions (W/L), bias current ($I_{bias}$) and compensation capacitor. The design of the op-amps was performed following the steps described in [11]. For the compensation capacitor, an increment in value improves the phase margin, but also an increase in die area consumed. Finally a value of 2 pF was chosen. The final transistor dimensions (Table 7.1) were obtained after several simulation iterations, until the desired requirements were met. Figure 7.4 shows the frequency response of one of the two op-amps that act as input buffer in the instrumentation amplifier. The designed operational amplifiers exhibit >70 dB of open-loop gain and ∼60° of phase margin (PM). The output current for each one of the two input op-amps is ∼80μA, whereas for the output op-amp is ∼10μA. Even though the minimum allowed gate length in the used technology was 0.35 μm, long gate lengths ($L > 1$ μm) were chosen for the design as transistors with longer gates are more robust against process variations.

Two types of instrumentation amplifiers were designed: with fixed and with variable gain. Both types are based on the schematic shown in Fig. 7.2, with the same three op-amps. The only difference is the design of the resistor network. According to expression (7.1), the gain of the instrumentation amplifier is determined by the value of the resistors. In order to obtain an amplifier with variable gain, it is necessary to replace the resistors in Fig. 7.2 by resistors whose value can be externally adjusted. In this work, these "variable resistors" were designed as depicted in Fig. 7.5: a group of resistor/switch pairs connected in parallel. Every switch is built-up by a combination of a CMOS inverter and a transmission gate. Every switch has an independent input signal to turn it off/on. In this way the gain of the amplifier can be tuned by activating the switch corresponding to the required resistance value. For example, by activating

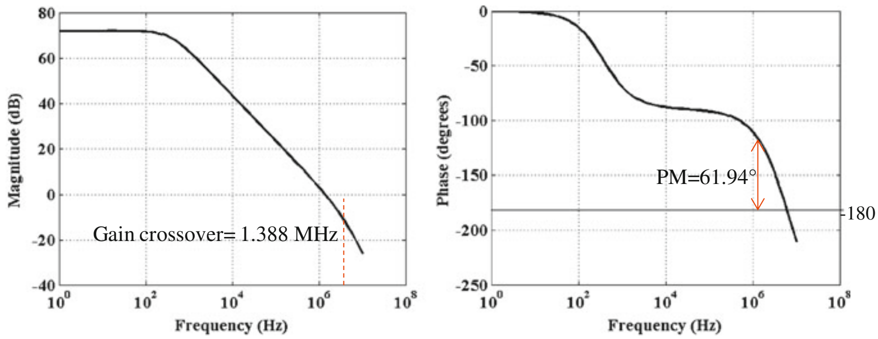


**Fig. 7.4** Magnitude and phase plot (from simulations) of the input op-amp of the instrumentation amplifier

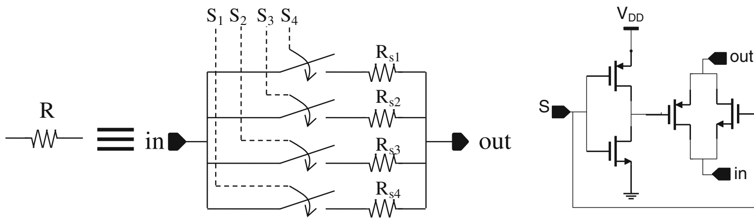


**Fig. 7.5** Schematic of the designed variable resistor. By activating the corresponding switch signal ($S_1 \ldots S_4$), the desired resistance is selected. On the right, schematic of one of the CMOS switches

**Table 7.2** Value of resistors (in kΩ) for the two types of instrumentation amplifiers designed: with fixed and with variable gain. The expected gain (obtained from simulations) in each case is also included

| | Fixed gain | Variable gain |
|---|---|---|
| $R_1$ | 1 | 1 |
| $R_2$ | 2 | 3, 5, 7, 10 |
| $R_3$ | 100 | 50, 100, 150, 200 |
| $R_{gain}$ | 5 | 5 |
| Gain | 65.2 | 3.3 194.4 |

$S_1$ ($S_1$=‘1’) while keeping the other signals off ($S_{2...4}$=‘0’), the value of R will be equal to $R_{S1}$. Note that it is also possible to activate several switch signals at the same time. In that case, the value of R will be equal to the parallel of the selected resistors.

Only two resistors ($R_2$ and $R_3$ in Fig. 7.2) were designed as variable resistors, while resistors $R_1$ and $R_{gain}$ exhibit fixed values. For the instrumentation amplifier with fixed gain, on the other hand, only standard resistors with fixed value were used. Table 7.2 lists the values of the different components of the resistor network for the two types of amplifiers. The expected gains, obtained in each case from the slope of

the corresponding simulated output voltage versus input voltage, are also listed. A gain of 65.2 is obtained for the instrumentation amplifier with fixed resistors. For the variable gain amplifiers, on the other hand, the gain can vary from 3 up to almost 200 depending on the selected resistor values. There is a slight mismatch between the amplifier gain obtained from simulations and the gain calculated using expression (7.1). From example, by substituting in expression (7.1) the resistor values listed in column 1 in Table 7.2, a gain of 70 is calculated for the amplifier with fixed gain, ∼7.4% higher than the gain obtained from simulations. This mismatch is mainly due to the fact that expression (7.1) is obtained by analyzing the circuit in Fig. 7.2 considering the op-amps as ideal: infinite gain, infinite input-impedance, zero input-current and zero output impedance. However, in the simulations, real models of the transistors that build up the op-amps are used, and therefore "non-idealities" such as finite gain or finite input impedance are included.

### *7.1.2 Layout*

The layout was performed using Layout XL from the Cadence Virtuoso platform [9]. The following techniques were used to verify layout: DRC (Design Rule Check) and LVS (Layout vs. Schematic). The designs were made for the HAWK maskset (2009), which includes both CMOS and MEMS masks for integrated fabrication. In this section, only specific details of the amplifiers layout are included. A more general description of the HAWK maskset, including also the MEMS part, can be found in appendix A.

Figure 7.6 shows the layout of an instrumentation amplifier with fixed gain. The compensation capacitors (three in total, one per op-amp) occupy most of the die area. The capacitors are realized using the poly and metal 1 layers as the bottom and top plates, respectively, assuming a nominal capacitance of $150 \cdot 10^{-6}$ pF/$\mu$m$^2$(total area needed for a 2 pF capacitor is $\sim 116 \times 116$ $\mu$m$^2$). The resistors are implemented as non-silicided (using an extra layer to block silicidation) polysilicon resistors on n-well, with a nominal sheet resistance of 230 Ω/□. Two types of resistor layouts are implemented (Fig. 7.7). For better matching, an interdigitized structure is used for a pair of resistors that need to be equal (like $R_1$, $R_2$ or $R_3$). For $R_{gain}$, a "serpentine" structure is used.

Figure 7.8 shows a close-up view of the layout of one of the two input op-amps of the instrumentation amplifier. The eight transistors (5 NMOS and 3 PMOS) are visible, together with part of the poly-metal compensation capacitor. The following layout techniques were used for better performance [11, 14–17]:

- Guard ring around PMOS transistors $M_3$, $M_4$ and $M_7$ to reduce substrate coupling noise.
- "Common-centroid" configuration in differential pair ($M_1$ and $M_2$) to cancel first-order gradient: each of the two transistors is decomposed in two halves that are placed opposite of each other and connected in parallel.

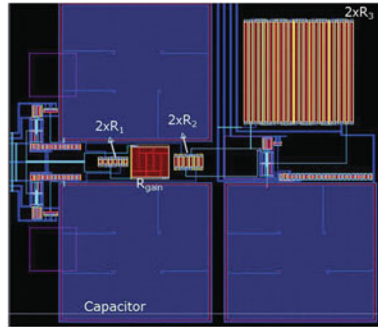


**Fig. 7.6** Layout of a 3 op-amps instrumentation amplifier with fixed gain. The three compensation poly-metal capacitors are visible, together with the poly resistors (of fixed value). Resistors pairs ($R_1$, $R_2$ or $R_3$ in Fig. 7.2) are interdigitated for better matching. For $R_{gain}$, a simple serpentine structure is used

- The source diffusion and the drain diffusion are filled with the maximum number of contacts to reduce the metal/diffusion contact resistance.
- To avoid circuit failure due to bad-processed vias or contacts, at least double contacts or double vias are used whenever possible.
- The gate oxide underneath the poly is incredibly thin. If the charge accumulated on the poly is sufficiently large, the accumulated charge can threaten to overstress and irreparably damage the thin gate oxides of the transistor, causing unreliable operation. This is known as process antenna effect. To protect the transistors gate, no contacts or vias are placed over the poly gate, and no routing is done over the gates.
- Fingering of wide transistors. The fingering technique allows reducing the drain and source area, reducing in turn the parasitic capacitance which results in an increased transistor speed. Folded transistors also have smaller gate resistance, and can therefore turn off and on faster. This fingering technique is only applied

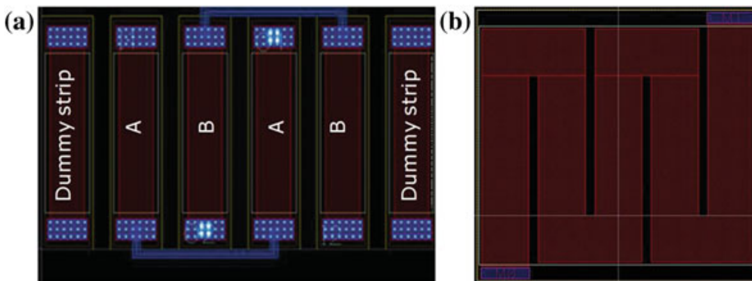


**Fig. 7.7** **a** Interdigitated structure of two resistors of 2 kΩ (A-A and B-B), corresponding to $R_2$ in the amplifier schematic (Fig. 7.2). Each poly line is 1 kΩ. Two "*dummy poly lines*" are included on the sides for better matching: to make sure the ending elements have the same boundary conditions than the inner elements. **b** Resistor of 5 kΩ (corresponding to $R_{gain}$) with "serpentine" structure

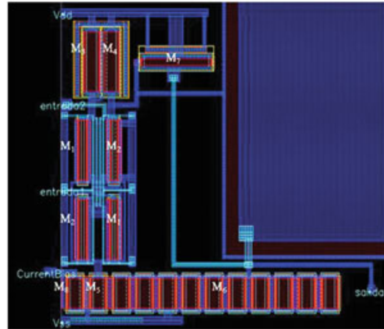


**Fig. 7.8** Layout of a two-stage Miller op-amp, corresponding to one of the two input op-amps of the instrumentation amplifier. Only part of the compensation capacitor is visible. Transistors are named according to Fig. 7.3

to transistor $M_6$, which forms a current mirror with transistor $M_8$ (W/L = 2/4). To improve matching, transistor $M_6$(W/L = 20/4 or 40/4 for input and output op-amp, respectively) is divided into 10 (or 20) transistors of 2/4 connected in parallel. Metal, instead of poly, was used to interconnect the gates, as poly exhibits a higher resistivity and a larger parasitic capacitance poly-substrate.

It is important to note that the amplifier layout was not optimized in terms of die area consumption. The layout of the fixed gain instrumentation amplifier (shown in Fig. 7.6) occupies a total area of $290 \times 280\ \mu m^2$. Robustness was the main layout design concern, and not area consumption. For example, very large transistors were used as they are more robust against process variations. From the interconnections point of view, wide lines (width at least double of the minimum allowed by technology) were used with enough spacing from one another (to avoid unwanted shorts during fabrication). A considerable amount of the circuit area is devoted to the poly resistors; especially large is resistor $R_3$ (100 kΩ). To save area, a (properly biased) transistor could have been used instead, as a transistor can provide a large resistance with significantly smaller area. However, the resulting resistor would be non-linear. For this reason, non-silicided polyresistors, although more area consuming, were used.

Figure 7.9 shows the layout of the two types of variable gain amplifiers designed. In the first amplifier (Fig. 7.9a) the resistors are designed as simple "serpentine" structures; the resistance values in each "resistive block" are: $R_2 = 3/5/7/10$ kΩ and $R_3 = 50/100/150/200$ kΩ. In the second amplifier (Fig. 7.9b) "interdigitated" resistors (see Fig. 7.7) are used for better matching; $R_2$ contains four resistors with values 2, 5, 7 and 10 kΩ while $R_3$ contains only two resistors with values 100 and 200 kΩ. The total circuit areas are $\sim 540 \times 270$ and $\sim 525 \times 285\ \mu m^2$, respectively. In both cases the op-amp layouts are exactly the same as for the fixed-gain amplifier (Fig. 7.8).

Figure 7.10 shows the final layout. Eight blocks can be identified, containing three fixed-gain amplifier and five variable gain amplifiers: two with "interdigitated" variable resistors (Fig. 7.9b) and three with "serpentine" resistors (Fig. 7.9a). In some cases, certain building blocks of the instrumentation amplifiers (like the op-amps or the variable resistors) are wired out independently for testing purposes. Each module

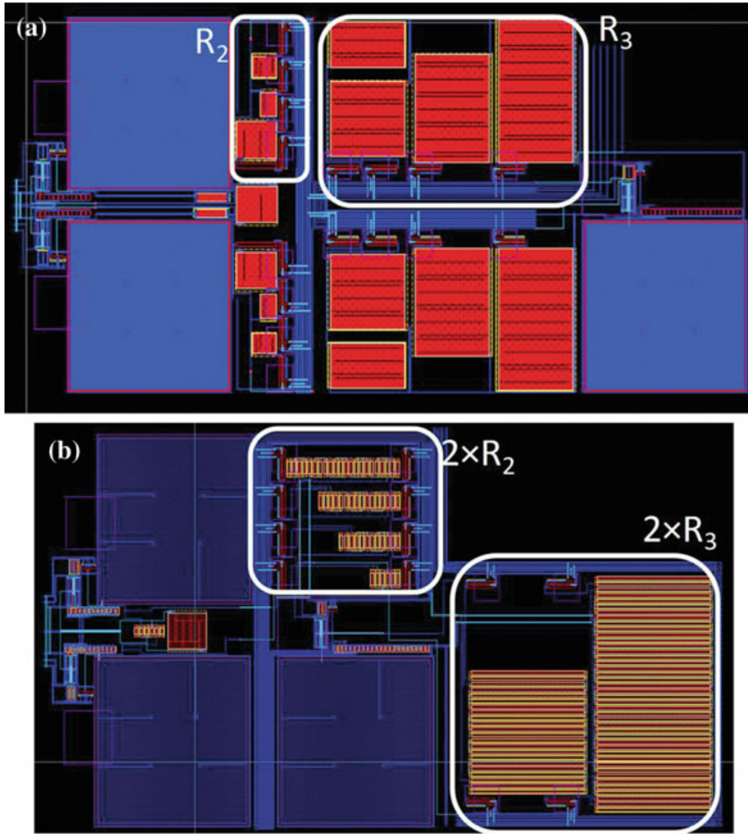


**Fig. 7.9** Layout of the two instrumentation amplifiers with variable gain designed in this work. In **a** "serpentine" resistors are used while in **b** interdigitated resistors for better matching are employed

contains a standard imec 24 pins probecard pad structure. It contains 24 bondpads of $80 \times 60\ \mu m^2$ with a vertical (horizontal) pitch of 40 μm (30 μm). This is not the optimum bondpads distribution from area consumption point of view; a smarter design could use bondpads placed surrounding the circuit. However, the use of a non-standard probecard layout is also more time consuming: not only the specific layout has to be designed, but the appropiate probecard for the electrical measurements must also be fabricated. Four of the modules include ESD protection [18, 19]. It consists of two wide parallel lines (metal 1 for GROUND and metal 2 for VDD) interconnected by one diode (in reverse) and 6 diodes (alternating). Each bondpad is connected by diodes to VDD (reversed) and GROUND.

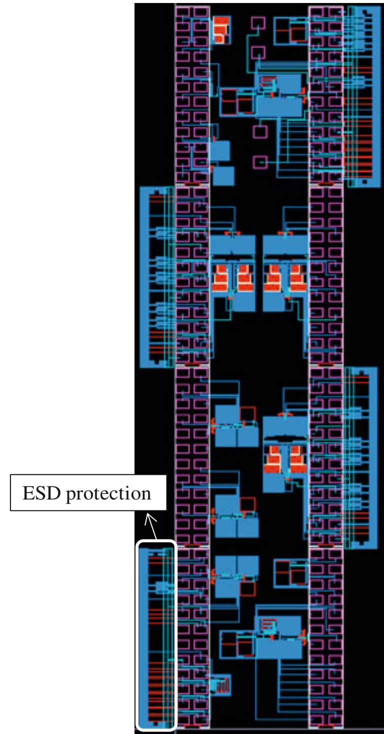


**Fig. 7.10** General overview of the complete CMOS layout designed for the HAWK maskset. It includes eight modules, each of them containing the layout for imec's 24 pins standard probecard. The use of the standard probecard will facilitate the electrical measurements later on. The top-right module contains four extra bondpads to study the "hybrid" integration (wirebonding) with the MEMS pressure sensor (see appendix A)

### *7.1.3 Fabrication*

The designed amplifiers were fabricated using a modified version of imec's 0.13 μm CMOS technology, with a thicker gate oxide (∼7 nm instead of ∼2 nm) to allow for higher voltages (3.3 V instead of 1.2 V). The polysilicon gate is 150 nm thick. The front end of line process includes shallow trench isolation, N-well and P-well implants, NMOS and PMOS source and drain formation (including pocket implants to reduce short channel effects) and nickel salicidation. The back end of line process includes two copper (Cu) interconnect layers with thicknesses of 360 nm (for Metal 1) and 600 nm (for Metal 2) with $0.2 \times 0.2\ \mu m^2$ Cu-filled vias connecting the two layers. Before each (Cu) metal layer deposition, a thin Ta (adhesion)/TaN (barrier) layer is deposited. The intermetal dielectric is formed by 50 nm SiC (Cu diffusion barrier layer and etch stop) and 600 nm PECVD (Plasma-enhanced Chemical Vapor Deposition) Si-oxide. The pre-metal dielectric (between poly and metal 1) is formed by 50 nm of Si-nitride, 500 nm of PSG (phophosilicate glass) and 10 nm PECVD $SiO_2$. Tungsten (W) filled $0.15 \times 0.15\ \mu m^2$ vias with Ti/TiN diffusion barrier are used to connect the poly and metal 1 layers. Figure 7.11 shows the schematic cross-section.

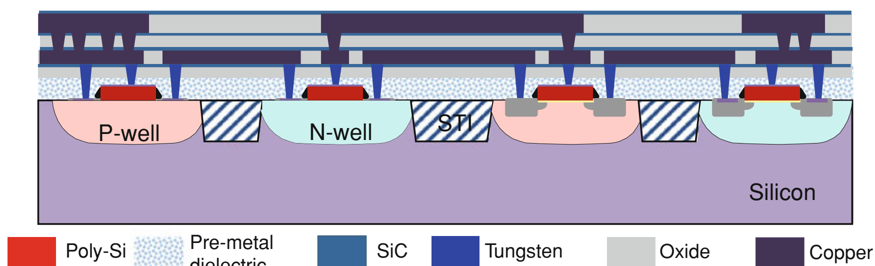


**Fig. 7.11** Schematic cross-section of the described 0.13 μm CMOS technology. Dimensions not to scale.

### *7.1.4 Measurements*

The fabricated circuit has been tested on a Suss PA300 probe station with measurement equipment from National Instruments and Keithley. Labview software was used to control the measurement setup. Figure 7.12 plots the output voltage vs. input differential voltage for an instrumentation amplifier with fixed gain. A very high yield (above 88 %) for this kind of amplifiers was obtained. Figure 7.12 also includes an histogram representing the distribution of the measured amplifier gain (obtained from the output voltage slope). The gain, with a mean value of 68.3, exhibits a great uniformity across the wafer (with a variation within 0.8 %). The measured gain is also very close to the gain predicted by simulations (65.2, see Table 7.2). As can be observed in Fig. 7.12, the output voltage of the amplifier for zero input voltage is different from zero. This output voltage for zero input is known as offset, and it is generally undesired. Most of the measured amplifier exhibited an offset of ∼43 mV, although some devices had offsets up to 300 mV. This offset might be explained considering imbalance of resistors values or mismatches between transistors. Finally, the amplifier output saturates at a voltage of ∼3.15 V, slightly lower than the power supply voltage (3.3 V).

Figure 7.13 shows the response of an instrumentation amplifier with variable gain for different combinations of the switch activation signals of the programmable resistors. Table 7.3 lists the corresponding resistance values for each switch combination, together with the measured and simulated gain. As can be observed, the gain of the amplifier can be varied according to the input switch combination. When integrated with a pressure sensor, this kind of amplifiers can be very useful as the gain can be tuned according to specifications or the sensitivity or offset of the sensor. For example, if the final sensitivity of the sensor is lower than expected, a higher gain can be selected. On the other hand, if the offset is too high, a lower gain can be chosen in order to avoid early saturation.

The results shown above correspond to a variable gain amplifier with “interdigitated” resistors (Fig. 7.9b). For the secon d type of variable gain amplifiers, with “serpentine” resistors (Fig. 7.9a), a similar behaviour is observed: the gain can be

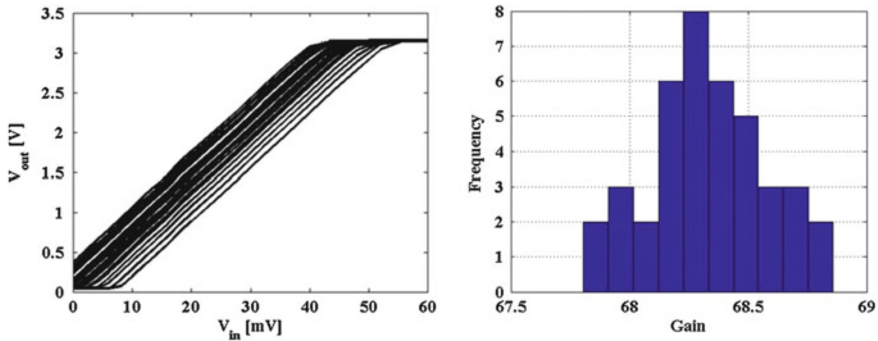


**Fig. 7.12** Measured output voltage versus input differential voltage for a fixed gain amplifier across full wafer. On the right, histogram representing the gain distribution across the wafer. A great uniformity in the measurements is observed

tuned according to the chosen switch signals, and the measured gains matched very closely those predicted by simulations.

## 7.2 Fabrication of a CMOS Integrated Pressure Sensor

After the fabrication of the CMOS readout circuit is completed, the processing of the poly-SiGe pressure sensor takes place. Two main measures were taken during the MEMS fabrication in order to avoid introducing any degradation in the underlying CMOS circuitry. First, the maximum processing temperature of the complete sensor, including the poly-SiGe piezoresistors, is kept $\leq$455 °C. And second, to protect the

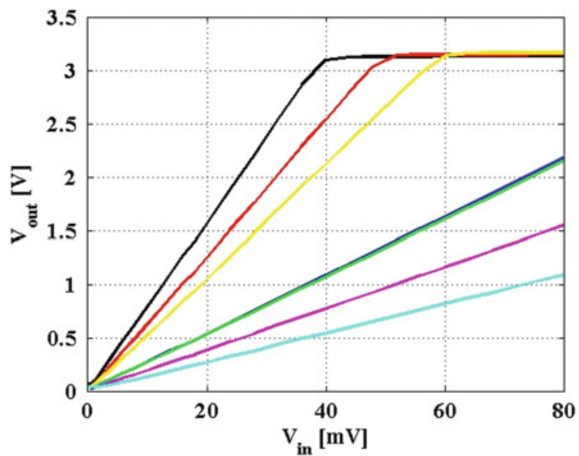


**Fig. 7.13** Measured output voltage of a variable gain amplifier with “interdigitated” resistors for different switch signals. A different response is obtained for each switch combination

**Table 7.3** Corresponding resistance values ($R_3$ and $R_2$) for each switch combination. A comparison between the measured and simulated gains is also included. In general, a good matching between the simulated and the measured gains is observed

| $R_3$ | | $R_2$ | | | | $R_3$ (kΩ) | $R_2$ (kΩ) | Gain measured | Gain simulations |
|---|---|---|---|---|---|---|---|---|---|
| $S_1$ | $S_2$ | $S_4$ | $S_3$ | $S_2$ | $S_1$ | | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 67 | 1 | 78.7 | 82.7 |
| 1 | 0 | 0 | 0 | 0 | 1 | 200 | 10 | 27.3 | 27.3 |
| 0 | 1 | 1 | 0 | 0 | 0 | 100 | 2 | 63.8 | 65.2 |
| 0 | 1 | 0 | 1 | 0 | 0 | 100 | 5 | 27 | 26.98 |
| 1 | 0 | 0 | 0 | 1 | 0 | 200 | 7 | 53.5 | 38.7 |
| 0 | 1 | 0 | 0 | 1 | 0 | 100 | 7 | 19.4 | 19.4 |
| 0 | 1 | 0 | 0 | 0 | 1 | 100 | 10 | 13.7 | 13.65 |

electronic circuit from the aggressive etch and deposition steps (specially the release process in vHF) which are needed to fabricate the MEMS devices, a SiC protection layer was used.

Figure 7.14 shows the layout and a top view microscope picture of two integrated sensors. The two shown sensors have an "n-shape" piezoresistor design (see Chaps. 3

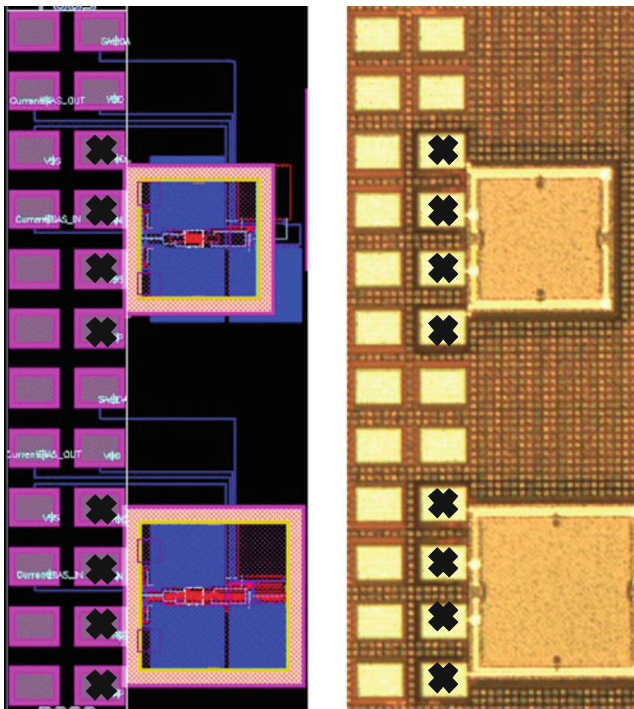

**Fig. 7.14** Layout and microscope picture of two integrated pressure sensors. The sensor bondpads appear marked with a cross

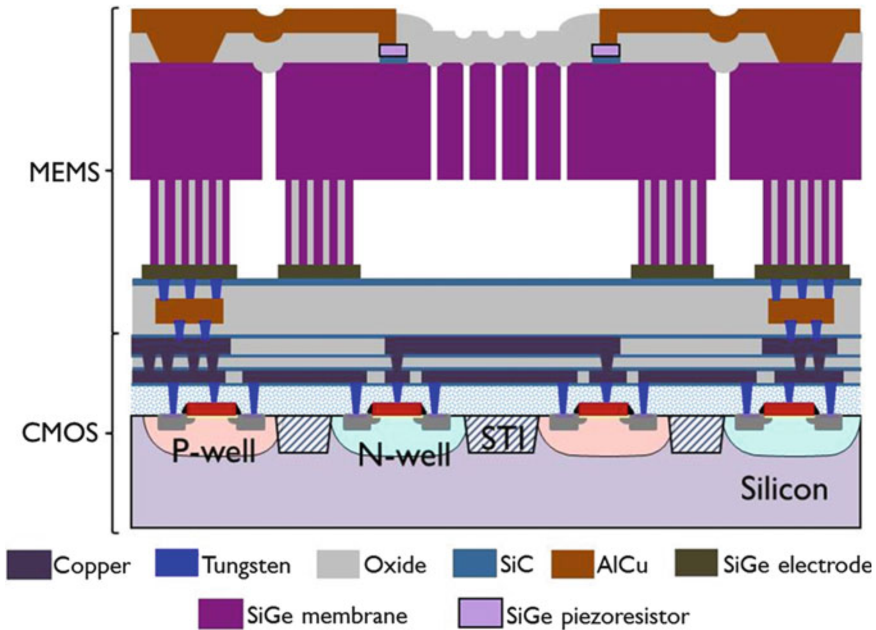


**Fig. 7.15** Cross-section of the integrated pressure sensor, with the most relevant layers highlighted

and 6) with the transverse piezoresistors placed at the membrane edge. Both of them are integrated with a fixed gain amplifier. In the layout snapshot, the CMOS circuit just below the pressure sensor is clearly visible. In the microscope picture only the sensors can be appreciated, as the CMOS is completely covered by MEMS layers (the SiC protection layer and the sacrificial oxide, among others). For the bottom integrated sensor ($250 \times 250\,\mu m^2$), the circuit (without including the bondpads) occupies approximately the same area as the poly-SiGe piezoresistive sensor. In this case, by fabricating the MEMS directly on top of the CMOS (only possible thanks to the use of poly-SiGe), the total die area occupied by the complete integrated sensor has been reduced by a factor of $\sim$2, as compared to the traditional integration methods (see Chap. 1). This is a clear example of one of the main advantages of using poly-SiGe as MEMS structural material: the reduction in area consumption.

Figure 7.15 shows a cross-section of the fabricated integrated sensor. The MEMS process starts with the formation of $0.5 \times 0.5\,\mu m^2$ tungsten-filled vias that provide electrical connection between the pressure sensor and the CMOS circuit. These vias connect the CMOS top-metal layer (Cu) and the MEMS metal layer (AlCu). They are located exclusively on the bondpads; in the rest of the die area, the MEMS are completely isolated from the CMOS. All the 24 bondpads (and not only the 8 corresponding to the sensor) shown in Fig. 7.14 include these vias, to be able to provide the necessary inputs to the circuit after the MEMS processing. The vias are

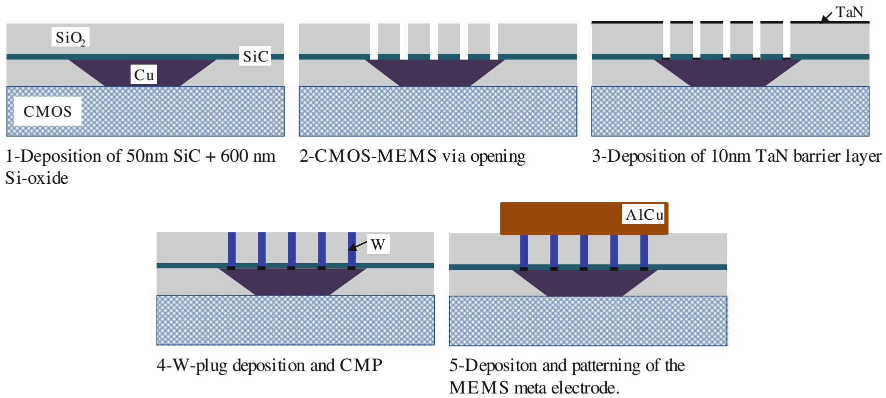


**Fig. 7.16** Schematic process flow for the fabrication of the W-filled CMOS-MEMS vias. Note that scales are distorted

distributed forming a perfect μm$^2$ square grid with a pitch of 4.5 μm. In total there are 165 CMOS-MEMS vias in each bondpad.

The fabrication of these CMOS-MEMS vias is schematically illustrated in Fig. 7.16. The isolation between the CMOS top-metal layer (Cu) and the MEMS metal layer (AlCu) is provided by a thin SiC layer (50 nm), which acts as a Cu diffusion barrier, and 600 nm of PECVD Si-oxide. A dry etch process is used to etch both the SiC and the Si-oxide to open the CMOS-MEMS vias. These $0.5 \times 0.5$ μm$^2$ vias are filled by a stack of 10nm TaN (Cu diffusion barrier), Ti/TiN (15/10 nm) liner/barrier layer and 350 nm of tungsten (W). After via filling, a CMP step is performed to remove the W everywhere except in the vias. This CMP also removes the TaN layer everywhere except inside the CMOS-MEMS vias. The 880 nm-thick AlCu MEMS bottom electrode is then deposited and patterned, following the process described in Chap. 4. Figure 7.17 shows a cross-section SEM picture of a W via connecting the Cu top metal layer and the Al MEMS bottom electrode. The measured contact resistance of one of these CMOS-MEMS vias is 0.8 Ω with a ±6 % maximum variation across the wafer.

After the formation of these CMOS-MEMS vias, the rest of the MEMS pressure sensor fabrication proceeds as explained in Chap. 4. The main steps in the pressure sensor fabrication process are (a more detailed description can be found in Chap. 4):

1. Deposition and patterning of a metal stack composed of 5 nm of Ti, 880 nm of AlCu (0.5 wt%) and 60 nm of TiN.
2. Deposition of the 400 nm-thick SiC CMOS protection layer. This passivation layer protects the electronic circuit from the aggressive etch and deposition steps which are needed to fabricate the MEMS devices.
3. Formation of 400 nm-thick boron doped ($B \sim 1 \times 10^{21}$ cm$^{-3}$) SiGe electrodes. The SiGe electrodes and MEMS metal layer are separated by the SiC protection layer plus 600 nm of oxide, and connected through $0.5 \times 0.5$ μm$^2$ W-filled vias.

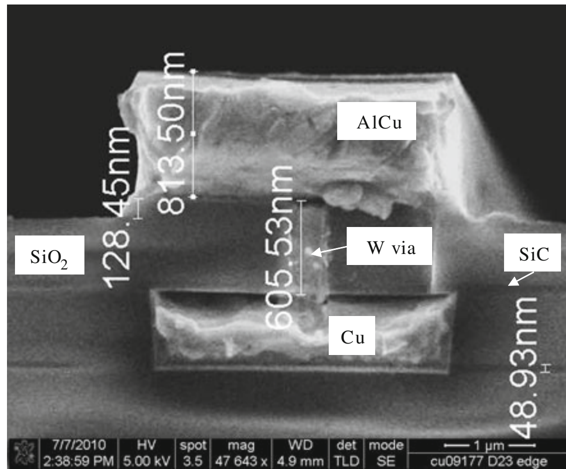


**Fig. 7.17** Cross-section of a W-filled CMOS-MEMS via. The bottom Cu and top Al layers, together with the SiC+$SiO_2$ dielectric, are visible

4. Deposition of 3 μm of sacrificial oxide, followed by the patterning of the membrane anchors.
5. Deposition of the poly-SiGe membrane and filling of the anchors by a combination of CVD and PECVD processes.
6. To define the piezoresistors, a 200 nm-thick poly-SiGe layer (∼77 % Ge) is deposited, boron doped through implantation ($B \sim 1 \times 10^{19}\,\text{cm}^{-3}$), and annealed at 455 °C for 30 min. The longitudinal and transverse gauge factors for such a poly-SiGe layer are, approximately, 12.9 and 5.2, respectively (see Chap. 2). A thin SiC layer (∼ 60 nm) is used as isolation layer between the SiGe membrane and the SiGe piezoresistors.
7. Opening of $1 \times 1\,\mu\text{m}^2$ etching channels in the membrane and removal of the sacrificial oxide by a combination of anhydrous vapor HF (AVHF) and ethanol vapor.
8. Sealing of the membrane with ∼1.2 μm of SACVD (Sub-atmospheric CVD) Si-oxide. The cavity pressure after sealing, determined from load-deflection measurements, is ∼7 kPa (Chap. 5).
9. Opening of contacts, followed by the deposition and patterning of 500 nm AlCu to connect the piezoresistors.
10. A final lithographic step, followed by the etching of the sealing and SiGe membrane layer, to separate the bondpads and cavities from one another.

Figure 7.18 shows a SEM picture of an integrated sensor with “n-shape” piezoresistors. At the bottom, the two Cu metal layers of the CMOS circuitry are visible. The poly-SiGe piezoresistive pressure sensor, fabricated directly on top of the CMOS, can also be observed. Figure 7.19 shows a closer view to the bottom layers: the two Cu metal lines, the AlCu MEMS bottom electrode, the SiC CMOS protection layer and the MEMS SiGe electrode are clearly visible. Even the CMOS transistors can be appreciated.

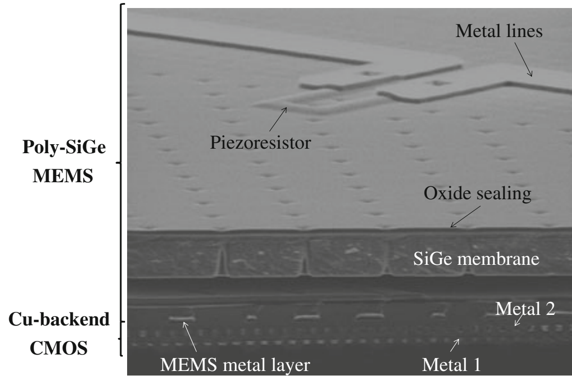


**Fig. 7.18** Cross-section SEM picture of the integrated sensor. At the bottom, the two Cu metal lines of the CMOS circuit can be observed. Above, the MEMS layers (the poly-SiGe membrane and piezoresistors, the oxide sealing layer and the metal interconnects) are visible

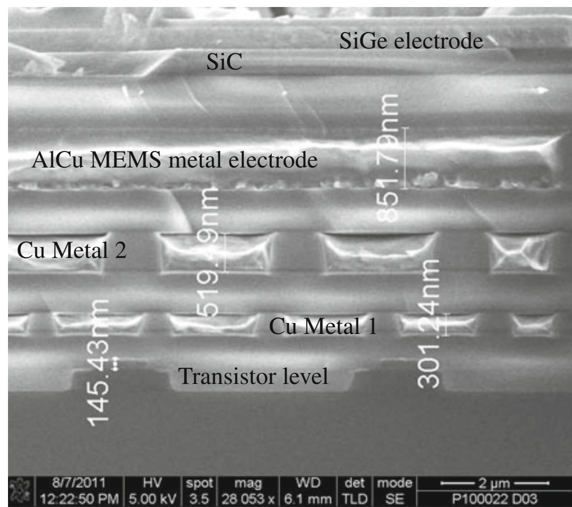


**Fig. 7.19** XSEM picture offering a closer view to the metal bottom layers (the two CMOS Cu lines and the AlCu MEMS electrode). Above, the SiC protection layer and the SiGe electrode can be appreciated. At the bottom, the CMOS transistor level is visible

The two biggest issues faced during the MEMS fabrication above Cu-based CMOS were:

1. Delamination. Although already observed during the stand-alone pressure sensors fabrication, delamination issues were worse during the integrated sensor fabrication. This might be due to the extra stress coming from the CMOS layers.
2. Contamination. Cu is considered level 3 in imec's cleanroom facility, while most of the MEMS processing tools are level 2. In order to ensure no copper contamination of the level 2 tools, Total reflection X-ray fluorescence (TXRF) analysis [20] had to be performed after each critical processing step (all the wet and dry etch/strip operations). However, no Cu was ever found after the processing of the integrated wafers, which indicate that both TaN and SiC are good Cu barrier layers.

**Table 7.4** Effect of MEMS post-processing on relevant CMOS parameters

| | Before MEMS | After MEMS[a] |
|---|---|---|
| Threshold voltage linear | 0.495 V ± 26 mV | 0.527 V ± 85mV |
| Threshold voltage saturation | 0.538 V ± 9.7mV | 0.56 V ± 11 mV |
| Leakage current | 12.8 ± 7.4 pA | 13.1 ± 7 pA |
| Drive current | 351 ± 5.45 μA | 343 ± 5.33 μA |
| $R_{sheet}$ Metal 2 (mΩ/sq) | 43.02 ± 1.33 | 41.79 ± 1.23 |
| M1/M2 contact | 3.12 ± 0.5 Ω | 7.93 ± 4.36 Ω |

[a] The measurements before and after MEMS were performed on different wafers (although with the same CMOS processing), so the observed variations may also be partially due to wafer to wafer variations

## 7.3 Effect of the MEMS Processing on CMOS

This section evaluates the impact of the MEMS post-processing on the underlying CMOS. During the MEMS pressure sensor fabrication, the CMOS wafers withstand a maximum process temperature of 455 °C (corresponding to the SiGe depositions and several annealing steps) for ∼ 8.5 h (see Chap. 4 for more details). Table 7.4 shows the effect of the MEMS processing on relevant transistor parameters, CMOS backend and overall amplifier gain. The measurements before and after MEMS correspond to different wafers (although with the same processing), so the observed variations may also be partially due to wafer to wafer variations.

The threshold voltage, in the linear and saturation region, has been measured at a drain to source voltage of 0.1 and 3.3 V, respectively. After the MEMS processing, a slight increase in both the linear and the saturation threshold voltage is observed. The change for the linear threshold voltage was 32 mV (∼ 6.4 %), while for the saturation threshold voltage the increase was around 22 mV (∼ 4.1 %). Also for positive channel MOS (PMOS) transistors an increase in threshold voltage was observed. Similar results were obtained in [21], where electron trapping during the annealing step was proposed as explanation. The transistor leakage current seems to increase after the MEMS processing, although the measured variation (0.3 pA) is well within the error margin and can be considered negligible. On the other hand, the transistor drive current is found to decrease (∼ 2.3 %) due to the MEMS processing, which is in agreement with the observed increase in threshold voltage.

For the CMOS backend, a decrease of ∼ 3.2 % in the sheet resistance of the Cu metal 2 line was observed, which might be attributed to a possible grain growth due to the thermal budget of the MEMS processing [22], although the change is too small to draw any conclusion. The metal-to-metal Cu-filled vias resulted to be the most temperature sensitive structure in the CMOS, with a pronounce increase in via resistance. One possible explanation for this increase in via resistance could be the formation of voids to relax the mechanical stress induced by the mismatch between the thermal expansion coefficient of copper and the surrounding oxide [23]. In [24], voids in Cu-filled Through Silicon Vias (TSV) were observed after Cu electroplating, and void-growth was observed at the void location after annealing. The authors

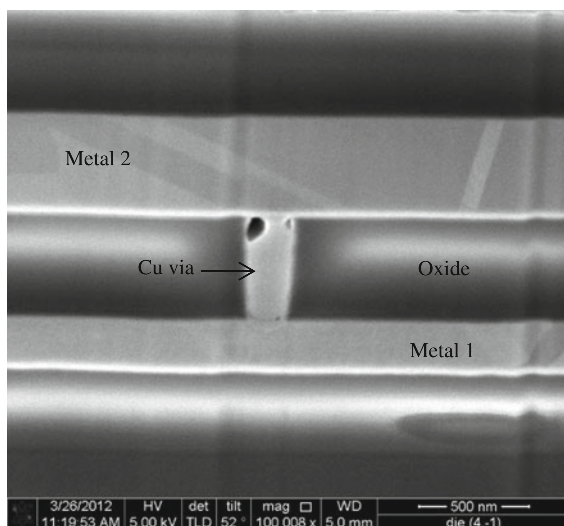


**Fig. 7.20** Cross-section picture of a $0.2 \times 0.2 \mu m^2$ CMOS Cu-filled via after MEMS processing. Voids in the via are clearly visible

suggested hydrostatic stress-assisted void growth as the responsible mechanism. Figure 7.20 shows a cross-section picture (obtained in a FIB-SEM system) of one of these $0.2 \times 0.2\ \mu m^2$ CMOS Cu-filled vias. A void is clearly visible at the via/metal 2 interface. There seem to be also small voids at the barrier sidewalls and bottom.

The found increase in via resistance is much more pronounced than predicted by previous annealing tests (see appendix D) on similar CMOS wafers ($<\ 10\,\%$ for 6 h annealing at 455 °C). One explanation for this could be the longer time that the wafers must withstand at high temperature (455 °C) during MEMS processing as compared to the times considered in the annealing tests. Moreover, all of the SiGe depositions and annealing steps during the MEMS flow are performed in a hydrogen-rich atmosphere. In [25], a much higher density of voids in samples annealed in atmosphere containing hydrogen was observed, as compared to samples annealed in an Ar atmosphere. A possible reaction of oxygen impurities contained in the Cu films to form water vapor when annealed at high temperatures in an hydrogen atmosphere was proposed as explanation. To prevent this Cu via degradation, work at imec is ongoing to further reduce the MEMS processing time (e.g by reducing the number and length of the annealing steps) and temperature (e.g. below 400 °C) and/or to reduce the amount of hydrogen used in the process flow. In any case, no significant impact on the amplifier gain was observed, although after the MEMS processing the values exhibited a larger spread (Fig. 7.21).

Regarding the CMOS-MEMS interface, the resistance of the tungsten-filled vias increased from $\sim$0.82 Ω to $\sim$1 Ω. The MEMS processing also resulted in an increase in the sheet resistance of the Al MEMS bottom electrode from 340 m/sq to 396 m/sq, which can be explained by Ti/Al reactions [26].

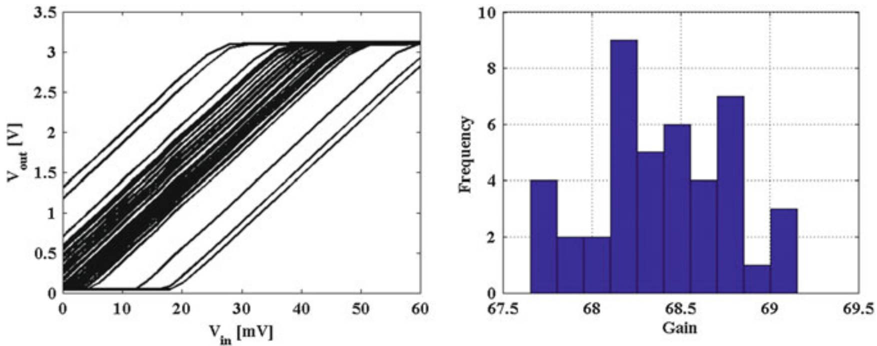


**Fig. 7.21** Output voltage for a fixed gain instrumentation amplifier measured after MEMS post-processing. On the *right*, histogram representing the gain distribution across the wafer

These resistance changes are however not detrimental to the overall performance of the CMOS circuit, as demonstrated by the functional integrated pressure sensor (see next section). A more complete study of the thermal budget limits for imec standard 0.13 μm CMOS technology is presented in appendix D.

## 7.4 Evaluation of the CMOS-Integrated Pressure Sensor

Similar as the stand alone pressure sensors (Chap. 6), the integrated sensors have been tested in the pressure range from 0 to 1 bar using an environmental chamber in combination with a HP4156A precision parameter analyzer. For these experiments the used environmental chamber was a Suss Microtech PAV-150 instead of the PMV-150 chamber used in the evaluation of the stand alone sensors. The difference between these two chambers is that the PAV is a semiautomatic vacuum prober while the PMV is a manual prober. The PAV was preferred for the measurements of the integrated sensors since up to eight probes can be added to the chamber, while in the PMV the maximum number of probes is only six. For the measurement of the integrated sensor, the minimum number of probes needed is seven (corresponding to a sensor integrated with a fixed gain amplifier).

It is important to note that, due to time limitations, only the pressure response of the integrated sensors could be characterized. A complete evaluation should include other important performance parameters, like temperature drift and signal-to-noise ratio (SNR). The SNR could be an important indicator to evaluate if the parasitic reduction thanks to the CMOS-monolithic integration really results in the promised improved performance with respect to the traditional hybrid integration.

Figure 7.22 shows a microscope picture of a 250 × 250 $\mu m^2$ poly-SiGe piezoresistive sensor integrated with a fixed gain amplifier. The necessary electrical stimuli are indicated on top of the corresponding bondpads. All the electrical signals

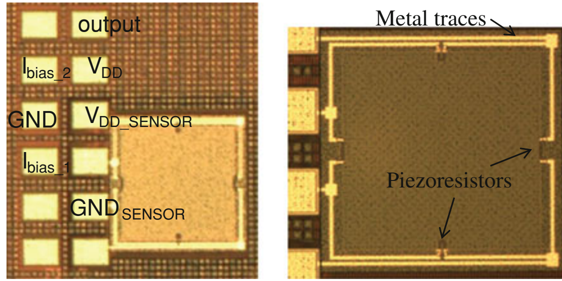


**Fig. 7.22** Microscope picture of a fabricated integrated sensor (with fixed gain amplifier). The necessary electrical stimuli for measurements are indicated. For the CMOS, two input currents ($I_{bias}_1 = 10\,\mu A$ and $I_{bias}_2 = 2\,\mu A$), one ground and one power supply are needed. For the sensor, only two electrical signals (ground and $V_{DD}$) are needed. The output of the integrated sensor (CMOS+MEMS) can be read through the bondpad mark as "output". On the right, close-up view of the sensor, with the piezoresistors and metal interconnects clearly visible, can be observed

are provided by the HP4156A parameter analyzer and its four input/output ports. Two ports are used to provide the two current bias necessary for the CMOS circuit ($I_{bias}_1 = 10\,\mu A$ and $I_{bias}_2 = 2\,\mu A$). One port is used to provide the bias voltage ($V_{DD} = 3.3$ V) both to the circuit and the sensor. And finally, one port is used to measure the output of the integrated sensor (CMOS+MEMS). Note that the input differential voltage for the amplifier comes directly from the differential output of the sensor. The ground connection of the parameter analyzer provides the ground for the circuit and the sensor.

Figure 7.23 plots the pressure response of a $250 \times 250\ \mu m^2$ pressure sensor with "n-shape" longitudinal piezoresistors and transverse piezoresistors placed at the edge of the membrane (design D2 according to Fig. 6.3). The left graph plots the voltage output versus pressure for the sensor alone, while the right graph plots the output of the integrated sensor (CMOS+MEMS). The sensitivity of the poly-SiGe piezoresistive sensor alone was around 2.48 mV/V/bar (similar to the stand-alone sensors with the same design, see Chap. 6). The integrated sensor (same sensor + Cu-based CMOS amplifier underneath) showed a sensitivity of $\sim 159.5 \pm 1$ mV/V/bar, $\sim$64 times higher than the stand-alone sensor. This gain is very close to the gain exhibitted by the CMOS amplifier alone ($\sim$68), which corroborates the conclusion from the previous section: the MEMS processing does not have a significant effect on the CMOS circuit.

One of the main problems exhibited by the stand alone pressure sensors in Chap. 6 was a very high offset. Since the amplifier does not include offset compensation, the offset of the pressure sensor is also amplified by a factor of $\sim$64. For the sensor described in Fig. 7.23, a zero-pressure output of $\sim$43 mV is obtained, which translates into an initial voltage output of $\sim$2.78 V for the integrated sensor. On the other hand, the maximum voltage at the output of the amplifier is $\sim$3.15. This means that, for the sensor above, the maximum output swing is $\sim$370 mV, which corresponds to the pressure range 0–0.7 bar. For higher pressures, the output saturates.

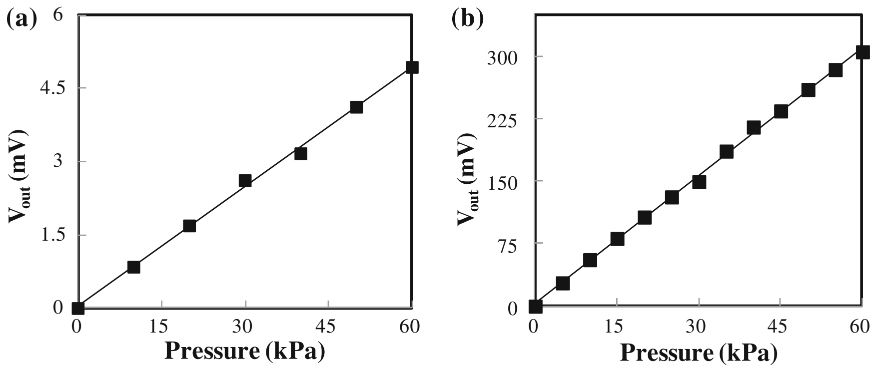


**Fig. 7.23** Measured output voltage versus applied pressure for (**a**) a stand-alone pressure sensor and (**b**) the same sensor + an instrumentation amplifier with fixed gain. The pressure sensor is 250 × 250 μm$^2$ with design D2 (see Fig. 6.3). The data point at vacuum is taken as reference for the data, to eliminate the offset. The data points are fitted to a linear function. In (**b**) the last three points had to be obtained by data extrapolation due to saturation of the output voltage

**Table 7.5** Measured output voltage for different switches configuration for a sensor integrated with a variable gain amplifier. The output of the sensor alone, together with the measured and calculated gains (from (7.1)) are also listed. The measurements were performed under 1 bar external pressure

| $R_3$ | | | | $R_2$ | | | | $R_3$ | $R_3$ | $V_{out}$ | $V_{out}$ | Gain[a] | Gain |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $S_4$ | $S_3$ | $S_2$ | $S_1$ | $S_4$ | $S_3$ | $S_2$ | $S_1$ | (KΩ) | (KΩ) | (S+A) (V) | (Sensor) (mV) | | calculated |
| 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 50 | 3 | 1 | 48.4 | 20.8 | 22.2 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 100 | 3 | 1.75 | 48.4 | 36.4 | 44.3 |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 50 | 5 | 0.63 | 48.4 | 13 | 13.5 |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 50 | 7 | 0.44 | 48.4 | 9.1 | 9.7 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 50 | 10 | 0.34 | 48.4 | 7.1 | 6.8 |

[a] Calculated as the ratio of the sensor output voltage measured before and after amplification

Another problem occurs for pressure sensors with negative offset, since the amplifier was designed to work only for positive inputs. Combining the condition of positive offset with the saturation problem, we can conclude that only sensors with an offset between 0 and 50 mV can, at least partially, be tested. Moreover, a problem with the ESD protection (Fig. 7.10) after the MEMS post-processing was observed: the diodes start conducting at voltages below 3.3 V, clipping the voltage and causing a short between the signal and power lines and the malfunctioning of the circuit. Due to this, modules with ESD protection, i.e. three modules out of seven per die, will not work .The stringent offset condition combined with the ESD problem, plus other MEMS processing issues (like broken membranes due to delamination), caused that only one integrated sensor with fixed-gain amplifier (in a whole wafer) could be properly tested.

Regarding the integrated sensors with variable gain amplifiers, the offset limitation is more flexible since the gain can be increased or decreased as needed. However,

as these type of sensors require nine or eleven probes to be tested, depending on the type of resistors used ("interdigitated" or "serpentine"), and the maximum number of probes in the PAV is eight, their pressure response could not be tested. A possible solution to this problem would be to add an "arm" with a 24-pin standard probecard to the pressure chamber. Due to time limitations, this option could not be further explored. For this reason, this type of integrated sensor could only be tested at 1 bar (atmospheric pressure) using the measurement setup employed to characterize the CMOS circuit, and described in Sects. 7.1–7.4. Table 7.5 lists the measurement results of one sensor integrated with "variable-gain" amplifier. As can be observed, the device worked as expected: different output voltages depending on the selected resistance values, and a measured gain (obtained dividing the output voltage of the sensor + amplifier by the output voltage of the sensor alone) close to the gain exhibited by the amplifier before the MEMS processing.

## 7.5 Conclusions

A prototype integrated poly-SiGe-based piezoresistive pressure sensor directly fabricated above its readout circuit has been presented. A classic three op-amp instrumentation amplifier acted as the readout circuit of the pressure sensor. The surface-micromachined piezoresistive pressure sensor consisted in a poly-SiGe membrane with four poly-SiGe piezoresistors placed on top in a Wheatstone bridge configuration, as described in previous chapters. Tungsten-filled vias were used to connect the CMOS Cu top metal layer and the Al MEMS bottom electrode.

In this chapter, the CMOS readout circuit design, layout generation, fabrication and electrical evaluation have been described in detail. A modified version of imec 0.13 μm Cu-backend CMOS technology, with thicker oxide (~7 nm instead of ~2 nm) in order to allow for a higher bias voltage, has been used. Two Cu metal layers were provided for interconnections, with Cu-filled metal-to-metal vias and oxide intermetal dielectric. Two types of instrumentation amplifiers have been considered: with fixed gain and with variable gain. In the variable-gain amplifiers, the standard resistors have been replaced by "resistive blocks", which include several resistors connected in parallel through switches. By activating the corresponding switch, the desired resistance value is selected. The fabricated circuits exhibited a behavior very close to that predicted by simulations.

The impact of the MEMS processing on the CMOS circuit and the CMOS-MEMS interface has also been studied. The CMOS circuit showed no significant deterioration after the MEMS processing, although a resistance increase for the Cu-filled metal-to-metal and the tungsten-filled CMOS-MEMS vias was observed.

Measurements of an integrated sensor with a $250 \times 250\ \mu m^2$ membrane and fixed gain amplifier showed a sensitivity of ~159.5 mV/V/bar, about 64 times higher than the stand-alone pressure sensor (~2.5 mV/V/bar). For pressure sensors integrated with a variable gain amplifier, different sensitivities were obtained depending on the switch selection.

The devices presented in this chapter represent the first integrated poly-SiGe pressure sensors directly fabricated above their readout circuit. It is also the first time that a poly-SiGe MEMS device is processed on top of Cu-backend CMOS. The results obtained in this work demonstrate that the poly-SiGe MEMS process flows can potentially be compatible with post-processing above Cu-based CMOS, broadening the applications of poly-SiGe to the integration of MEMS with the advanced CMOS technology nodes. However, to ensure the complete CMOS-compatibility of the presented poly-SiGe flow, extra work is needed to better understand, and prevent, the observed deterioration of the Cu-filled CMOS vias after MEMS post-processing.

The presented integrated sensor is not in any way complete: the readout circuit includes only the amplifier stage, ignoring some of the fundamental parts of any piezoresistive sensor interface circuitry: temperature and offset compensation. Moreover, from the MEMS side, the poly-SiGe piezoresistive pressure sensor was not designed to fulfill typical performance requirements (in terms of temperature dependence, offset, linearity, etc). For these reasons, the integrated pressure sensor fabricated in this work may not have an immediate commercial application. However, as a demonstrator, it has a high significance.

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# Chapter 8
# Conclusions and Future Work

The final goal of this thesis was the fabrication of a CMOS-integrated piezoresistive pressure sensor. SiGe MEMS was selected as the technology platform in which to reach this goal. This dissertation provides all the steps for the successful design and fabrication of MEMS pressure sensors directly on top of their readout circuitry, allowing for smaller chips. The monolithic integration of MEMS on top of CMOS is also expected to improve the signal/noise ratio as compared to the traditional hybrid approaches: by processing the pressure signal in close proximity to the transducer, the parasitics introduced by the IC-MEMS interconnects and the effect of external noise can be greatly reduced. In this chapter an overview of the key aspects and contributions of this dissertation is presented, together with a list of recommendations to further improve the technology and the performance of the fabricated devices.

## 8.1 Conclusions and Contribution of the Dissertation

The primary contribution of this work is the realization of an integrated poly-SiGe-based piezoresistive pressure sensor directly fabricated above 0.13 μm Cu-backend CMOS technology. This represents not only the first integrated poly-SiGe pressure sensor directly fabricated above its readout circuit, but also the first time that a poly-SiGe MEMS device is processed on top of Cu-backend CMOS.

As explained in Chap. 1, polycrystalline SiGe has emerged as a promising MEMS structural material since it provides the desired mechanical properties at lower temperatures compared to poly-Si, allowing the post-processing of MEMS on top of CMOS. Of the different existing approaches for CMOS-MEMS monolithic integration, the MEMS-last approach is the most interesting one as it leads to smaller die areas and enables integrating the MEMS without introducing any changes in standard foundry CMOS processes. Compared to alternative technologies, for example using the CMOS top interconnect layers to fabricate the MEMS device, poly-SiGe offers a more generic and flexible technology for above CMOS integration, thanks

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to the fact that the MEMS fabrication can be completely decoupled from the CMOS fabrication.

In the past, imec already proved the potential of poly-SiGe for MEMS-above-CMOS integration by presenting, for example, an integrated poly-SiGe micromirror array and an integrated gyroscope, both of them fabricated on top of Al-based CMOS (from an external foundry). However, the aggressive interconnect scaling, essential to the continuation of Moore's law, has led to the replacement of the traditional aluminum metallization by copper metallization, due to its lower resistivity and improved reliability. The results obtained in this work demonstrate that the poly-SiGe MEMS process flows are also compatible with post-processing above Cu-based CMOS, broadening the applications of poly-SiGe to the integration of MEMS with the advanced CMOS technology nodes.

The described integrated sensor (fully fabricated in imec) includes a surface-micromachined piezoresistive pressure sensor, with a poly-SiGe membrane and four poly-SiGe piezoresistors, and an instrumentation amplifier fabricated using imec's 0.13 $\mu$m CMOS technology, with Cu-interconnects (two metal layers) and Si-oxide dielectric. Several steps were completed to realize the integrated pressure sensor. These steps comprised: development of a poly-SiGe piezoresistive layer to be used as sensing element in the pressure sensor, modeling and design of the sensors using FEM (Finite Element Methods), process development, fabrication and testing of the designed MEMS sensors, design of a readout circuit for the sensors and finally, proving the CMOS compatibility of the developed MEMS technology by fabricating the MEMS sensors directly on top of the CMOS readout circuit.

Other contributions of this work include the study, for the first time, of the piezoresistive properties of poly-SiGe. Also, never befefore was poly-SiGe used both as structural and sensing layer for MEMS pressure sensor applications. Moreover, together with the piezoresistive pressure sensors, also functional capacitive pressure sensors were succesfully fabricated on the same wafer, proving the versatility of poly-SiGe for MEMS sensor applications.

All of these key developments were addressed in detail in the different chapters of this thesis.

1. *Study of the electrical and piezoresistive properties of poly-SiGe*. Chapter 2 presents a detailed investigation on the influence of deposition conditions, germanium content and doping concentration on the electrical and piezoresistive properties of boron-doped poly-SiGe. The studied electrical properties include resistivity and temperature coefficient of resistance. Four different poly-SiGe layers were characterized. First, a heavily doped CVD poly-$Si_{24}Ge_{76}$, deposited at 450 °C was considered. This layer is used as the standard electrode layer in the SiGe-MEMS platform in imec. The layer exibitted a resistivity lower than 1 m$\Omega$ cm, a TCR of only $2.7 \times 10^{-4}$ °C$^{-1}$ and a gauge factor of 2.8. This gauge factor, although comparable to the gauge factor found for a similarly doped poly-Si layer (G = 4.2), is low for typical piezoresistive applications. Next, the piezoresistive and electrical properties of poly-$Si_{51}Ge_{49}$ and poly-$Si_{36}Ge_{64}$ for different doping concentrations (from $5 \times 10^{17}$ to $1 \times 10^{20}$ cm$^{-3}$) were evaluated.

Similar as for poly-Si, the gauge factor of poly-SiGe is found to tail off for low and high boron concentrations, reaching a maximum for a boron concentration around $1 \times 10^{19}\text{cm}^{-3}$. This optimum boron concentration also corresponds to a very low TCR, which is ideal for piezoresistive sensors applications. However, the processing temperatures used during the deposition and annealing of these layers were too high (above 500 °C) to allow for the monolithic integration of MEMS above CMOS. For this reason, a new poly-SiGe layer (Ge$\sim$77 %), deposited at 450 °C and annealed at 455 °C was developed to be used as sensing layer in the pressure sensors. A maximum gauge factor of $\sim$15 was obtained, which is somewhat smaller than reported maximum values for poly-Si. However, the possibility to post-process on top of CMOS still makes poly-SiGe a very interesting material for MEMS piezoresistive sensors as monolithic integration leads to a higher signal/noise ratio which might offset the slightly smaller gauge factor.

2. *Design of poly-SiGe based piezoresistive pressure sensors* (Chap. 3). Finite element simulations are used together with the experimentally obtained piezoresistive coefficients for poly-SiGe (Chap. 2) to predict the impact of the design parameters on sensor sensitivity and linearity. The design parameters include membrane area and shape and piezoresistors location, shape and dimensions. Finally, two membrane shapes (square and rectangular), four membrane areas ($200 \times 200$, $250 \times 250$, $300 \times 300$ and $350 \times 175\,\mu\text{m}^2$) and six different piezoresistor designs were included in the layout (Appendix A).
3. *The pressure sensor fabrication process*. The considered pressure sensors consist in a deformable poly-SiGe membrane, supported by a 25 μm-wide anchor ring, and four poly-SiGe piezoresistors placed on top following a Wheatstone bridge configuration. To enable above-CMOS integration the maximum processing temperature of the complete sensor, including the poly-SiGe piezoresistors, is kept $\leq$ 455 °C. A thin SiC isolation layer is included between the SiGe membrane and the SiGe piezoresistors. Also, to protect the electronic circuit from the aggressive etch and deposition steps which are needed to fabricate the MEMS devices, a SiC passivation layer was included. SACVD Si-oxide was used to seal the released (in vHF) membranes. The whole process sequence requires nine lithographic masks and more than 100 operations. The maximum process temperature was 455 °C, and corresponds to the SiGe depositions and the different annealing steps (for example after piezoresistor implantation for dopant activation) included during the flow. In total, during the processing of the MEMS pressure sensors on top of the read-out circuit, the CMOS will withstand a maximum temperature of approximately 455 °C for $\sim$8.5 h.
4. *Sealing process development*. The sealing process is one of the most important steps in the fabrication of a pressure sensor. For this reason a whole chapter of this thesis (Chap. 5) is dedicated to it. The most important requirements a sealing layer must fulfil are: provide a hermetic sealing of the cavity with a stable, preferably low, sealed-in pressure. Two different sealing techniques involving thin-film deposition are investigated: direct sealing and sealing using an intermediate porous layer. The sealing materials studied include Si-oxide and

sputter-deposited AlCu. To verify the sealing process, optical measurements of membrane deflection were carried out both in air and in vacuum. Analytical modelling and Finite Element Methods (FEM) were used to study the load-deflection behaviour of the (poly-SiGe/sealing layer) composite membranes and derive the overall stress and the pressure inside the cavities. The experimental results prove that both Si-oxide and AlCu can provide short- and long-term air-tight sealing. The use of a porous cover, although preventing the deposition of sealing material inside the cavity, resulted, for the cavities studied in this work, in a higher sealed-in pressure. Although direct sealing with AlCu provides a near-vacuum sealed cavity, its use for piezoresistive pressure sensors is not immediate as an extra isolation layer and/or extra processing steps might need to be introduced to avoid a short-circuit between piezoresistors. Finally, SACVD Si-oxide was the selected sealing layer for the pressure sensors since it represents a simple technique for the direct sealing of the sensors, with a resulting cavity pressure below 10 kPa and a marginally tensile stress in the sealed membrane.

5. *Experimental characterization of the fabricated MEMS pressure sensors*. In Chap. 6, the realized stand-alone poly-SiGe pressure sensors (both piezoresistive and capacitive) were evaluated in the pressure range from 0 to 1 bar. Sensitivities between 1.5 and 5.5 mV/V/bar have been obtained for the piezoresistive sensors, with nonlinearity errors below 4 %. In general, good qualitative agreement with the simulations in Chap. 3 is observed. The temperature dependence of the sensors was also characterized in the temperature range of 25 to 125 °C, leading to a temperature coefficient of sensitivity (TCS) in the range of −1000 to −2000 ppm/°C. The fabricated sensors exhibited very high voltage offsets with a large spread: values between −182 and 105 mV (for an input voltage of 3.3 V) were measured.
   For the capacitive pressure sensors, the impact of sensor membrane area, bottom electrode area and electrode/membrane gap on the sensor sensitivity was characterized. The highest measured sensitivity in this work is 73±3 fF/bar, and corresponds to a $200 \times 200\,\mu m^2$ sensor with a gap of 1 μm and an electrode of $150 \times 150\,\mu m^2$. If higher sensitivities are required, an array of such sensors could be used. Thanks to the low processing temperature of the described sensor, relative large arrays can be integrated with the readout electronics without extra die consumption. Moreover, this type of sensors is expected to benefit more from the parasitic reduction thanks to the above-CMOS integration than the piezoresisitve counterparts.
6. *Fabrication and evaluation of CMOS-integrated pressure sensors*. An instrumentation amplifier was designed to be used as the readout circuit for the piezoresistive pressure sensors. Two versions of the amplifier were implemented: with fixed and variable gain. The circuit was fabricated using a modified version of imec's 0.13 μm technology, with thicker gate oxide to allow for higher operating voltages (3.3 V instead of 1.2 V). The CMOS included two copper-based interconnect layers, with Si-oxide dielectric and Cu-filled metal-to-metal vias. To connect the top Cu-based CMOS metal layer and the bottom Al-based MEMS electrode, tungsten-filled vias were employed. The CMOS circuit showed no

significant deterioration after the MEMS processing, although an increase of $\sim$22 % in the CMOS-MEMS via resistance was observed. Only one integrated sensor could be properly evaluated. The poly-SiGe piezoresistive sensor alone ($250 \times 250\ \mu m^2$ membrane) showed a sensitivity of around 2.5 mV/V/bar. The integrated sensor (same sensor + Cu-based CMOS amplifier underneath) showed a sensitivity $\sim 159.5 \pm 1$ mV/V/bar, $\sim$64 times higher than the stand-alone sensor.

## 8.2 Future Research Directions and Recommendations

Although the developed poly-SiGe technology was successfully used to fabricate stand-alone MEMS pressure sensors, and the compatibility of the presented MEMS fabrication flow with CMOS was demonstrated through a functional integrated piezoresistive pressure sensor directly fabricated on top of its readout circuit, there is still room for improvement.

A better understanding of the poly-SiGe piezoresistors is needed. Characteristics such as noise and temperature coefficient of the gauge factor were not studied in this work. These material characteristics are important for the performance of piezoresistive pressure sensors as they contribute to define the minimum detectable pressure and resolution of the sensor, and the temperature coefficient of sensitivity. Also the nonlinearity of the piezoresistive response should be evaluated. In addition, it could be useful to develop an analytical model for the poly-SiGe piezoresistivity, similar to the model developed for poly-Si. Further improvement of the layer gauge factor by tuning the deposition and/or annealing conditions might also still be possible.

Despite not being designed for any specific application, the performance of the fabricated pressure sensors is comparable to commercially available devices. Only the offset voltage and the nonlinearity (NL) seem to be out of range. The reason for the high offset voltages is not yet fully understood. One possible reason could be the bad aluminum filling of the piezoresistor contacts. A bad filling of the contacts can translate into high contact resistance, and also lead to a large spread in the contact resistance values which might explain the high offset voltages. Test structures to better characterize the piezoresistor contact resistance should be designed, and different materials and/or deposition conditions could be studied to improve the contact filling. Also the uniformity of the poly-SiGe piezoresistive layer should be improved to reduce the offset voltage. In this sense, work at imec is ongoing to transfer the CVD part of the SiGe deposition process from the current PECVD tool to a CVD tool; an improvement in the uniformity of the SiGe layers is expected as a result. Finally, different sensor designs, based on a local stiffening of the membrane while the resistors are kept in a local stress concentration area, could be implemented to improve the linearity while minimizing the sensitivity loss.

On the other hand, by substituting the SACVD oxide by a sealing layer with a coefficient of thermal expansion (CTE) closer to the CTE of the poly-SiGe structural layer (for example using SiGe also as sealing layer), the temperature coefficient of sensitivity of the sensors could also be reduced. It would also be beneficial to

have vacuum-sealed cavities, as this will eliminate the trapped gas effects. Finally, a barrier coating (for example SiC or SiN) should be deposited on top of the metal interconnects to avoid corrosion.

Moreover, reliability tests of the fabricated pressure sensors should be performed. Important parameters, such as maximum allowed pressure or the operating temperature range were not determined. Also the repeatability of the sensor performance was not evaluated. The environment the piezoresistive sensors may be exposed to, depending on the application, may include cyclic or steady-state temperature, static or dynamic pressure, harsh media, vibration, and/or electric fields. To be assured that the sensor can sustain the environment, reliability testing should include media compatibility (i.e. exposure to fuel, water or strong acids), pulsed pressure with a cyclic temperature and bias, high and low temperature storage, high humidity exposure, and temperature cycling.

On the other hand, due to the limited time, the performance of the integrated sensors was evaluated only in terms of pressure response. A complete evaluation should include other important performance parameters like temperature drift and signal-to-noise ratio (SNR). Especially the SNR could be an important indicator to evaluate if the parasitic reduction thanks to the CMOS-monolithic integration really results in the promised improved performance with respect to the traditional hybrid integration.

A detailed study of the advantages offered by the above-CMOS integration is also missing in this work. From the fabricated devices, only the area reduction advantage can be appreciated. The supposed parasitic reduction and improved signal-to-noise ratio should be proven. For that purpose, specific structures were included in the layout to compare the hybrid versus monolithic integration approach; however, due to time limitations, this study could not be realized. The focus of this study was piezoresistive pressure sensors, and therefore little attention was paid to capacitive sensors. However, the benefits of above-CMOS monolithic integration, like for example the parasitic reduction, could be more obviously tested with an integrated capacitive sensor. Therefore, for a future work focusing on the advantages of monolithic over hybrid integration, capacitive pressure sensors, or also an RF MEMS device, would be a more suitable demonstrator.

Finally, a more complete readout circuit for the sensors is necessary. The simple readout circuit proposed in this work (just an amplifier) might be enough for a first demonstrator, but for real commercial applications, the circuit should include temperature compensation, offset calibration, etc. Also, the CMOS used in this work employs Si-oxide as dielectric layer. In standard copper-based advanced CMOS technologies, the low-permittivity dielectrics utilized in the metallization stack are less tolerant of post-deposition annealing, which might further restrict the thermal budget for the MEMS processing ($\sim$400 °C or even lower). In this case, the deposition temperature of the poly-SiGe structural layer and the processing temperature of the piezoresistors (455 °C in this work) have to be lowered. New techniques, like for example laser annealing, might need to be developed to avoid degradation of the poly-SiGe piezoresistivity.

# Appendix A

To develop the pressure sensor technology, mask sets are needed to be able to define the sensors using lithography and etch steps. For this purpose, two mask sets were designed in the frame of this work. These mask sets were called Piezopack and HAWK. On the Piezopack mask set only stand-alone MEMS pressure sensors (both piezoresistive and capacitive) were included. However, due to a bad design of the piezoresistor contacts (see Chap. 4), very few working devices were obtained. The results obtained with Piezopack are reported in Appendix B. All of the results reported in Chaps. 6 and 7 were obtained from the maskset HAWK. In this maskset, both CMOS and MEMS masks are included, allowing for the fabrication of integrated sensors. The problem of the bad aluminum filling of the piezoresistor contacts was solved by making the contacts larger, as compared to Piezopack. In this Appendix, only maskset HAWK will be described. For this maskset, the cross-section of the process flow is shown in Fig. A.1.

Figure A.2 shows an overview of the pressure sensor part in the HAWK maskset. The die area is 4x5.5 $mm^2$. A section of $1\times5.5\,mm^2$ is reserved for integrated pressure sensors (CMOS+MEMS) while the remaining area ($3\times5.5\,mm^2$) is dedicated to MEMS alone (stand-alone pressure sensors). As can be seen from Fig. A.2a, the MEMS stand-alone section can be further divided in 6 subsections: sensors for wire-bonding, sensors of different areas ($200\times200$, $250\times250$ and $300\times300\,\mu m^2$ sensors), sensors to be measured using the Suss pressure probe (tool in the university of Leuven-la-Neuve), and finally a section named “other”. Each of these sections will be explained in detail next.

## A.1 CMOS+MEMS

This section contains the layout of the integrated pressure sensors (CMOS instrumentation amplifier + MEMS piezoresistive pressure sensor) described in Chap. 7. Since the layout of the CMOS circuit was already described in Chap. 7, the rest of

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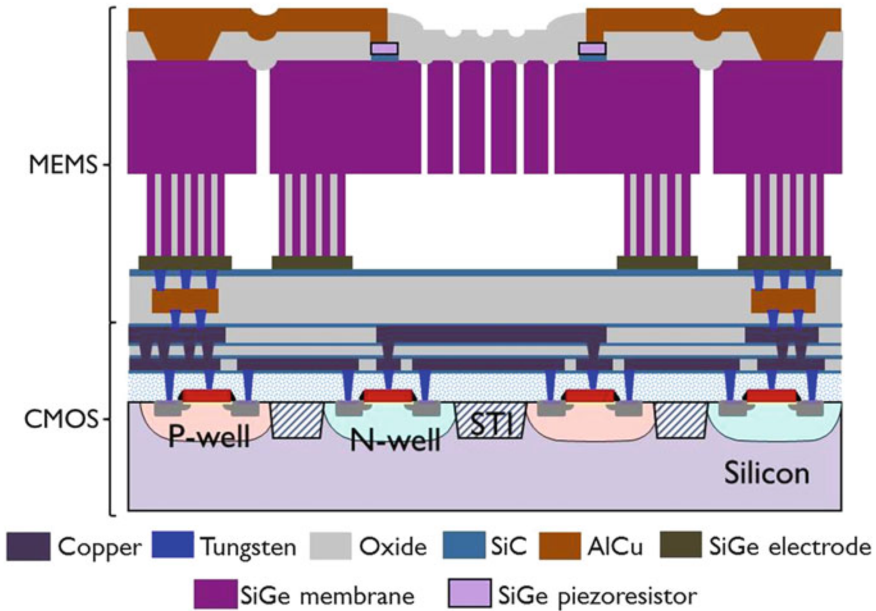


**Fig. A.1** Cross-section of the HAWK process flow with the most relevant layers highlighted (more information can be found in Chaps. 4 and 7). The MEMS stand-alone pressure sensors do not have connection to the underneath CMOS

this appendix will be devoted to the layout of the MEMS sensors. A close-up view of the layout of one of the integrated sensors can be observed in Fig. A.3. The layout of the pressure sensor is exactly the same as for the stand-alone case, except for the bondpad distribution: the stand-alone sensors have the four bondpads distributed around the membrane, while for the integrated sensors the four bondpads are all grouped on a side of the membrane, located directly on top of the CMOS bondpads to allow for the CMOS-MEMS interaction.
In total seven integrated piezoresistive pressure sensors were designed:

- Three sensors with a membrane area of $200 \times 200\ \mu m^2$ of which:
  - one sensor with piezoresistor design D2 integrated with an instrumentation amplifier with variable gain (see Fig. 7.9a).
  - one sensor with piezoresistor design D3 integrated with an instrumentation amplifier with variable gain (see Fig. 7.9b).
  - one sensor with piezoresistor design D2 integrated with an instrumentation amplifier with fixed gain (see Fig. 7.6).
- Four sensors with a membrane area of $250 \times 250\ \mu m^2$ of which:
  - two sensors with piezoresistor designs D1 and D2, respectivelty,each of them integrated with an instrumentation amplifier with fixed gain.

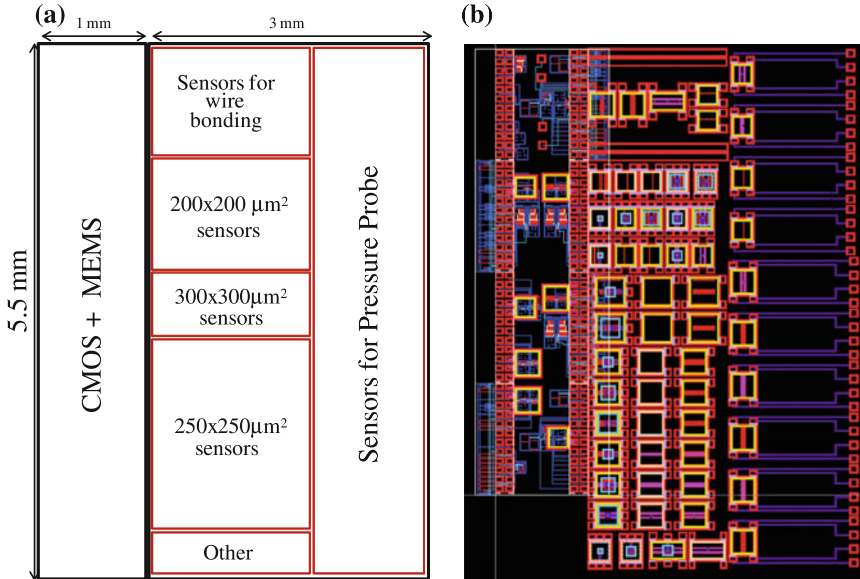


**Fig. A.2** Overview of the pressure sensor part in the HAWK maskset. **a** Floorplan. **b** Layout

– two sensors with piezoresistor designs D2 and D3, respectivelty, each of them integrated with an instrumentation amplifier with variable gain (see Fig. 7.9a).

In the above description, as in the rest of this appendix, designs D1, D2 and D3 refer to "line-shape", "n-shape" and "m-shape" longitudinal piezoresistors, respectively, with the transverse piezoresistors placed at the membrane edge. The sufix _T indicates that the transverse piezoresistors are placed at the centre of the membrane. More information on the different sensor designs can be found in Chap. 3 and Fig. 6.3.

## A.2 MEMS Alone

In the MEMS-only part we can find stand-alone pressure sensors with different areas ($200\times200$, $250\times250$ and $300\times300$ $\mu m^2$) and piezoresistor designs. Three rectangular sensors ($350\times175$ $\mu m^2$), all of them with the same piezoresistor design (design D3_T), are also included. Some of the sensors are unreleased (layout does not include release holes in the membrane, and therefore the sacrificial oxide remains under the membrane) and are intended to be used as reference in the measurements. Figure A.4 shows a close-view of a $250\times250$ $\mu m^2$ piezoresistive sensor with n-shape longitudinal piezoresistor and transverse piezoresistors placed at the centre of the membrane (design D2_T).

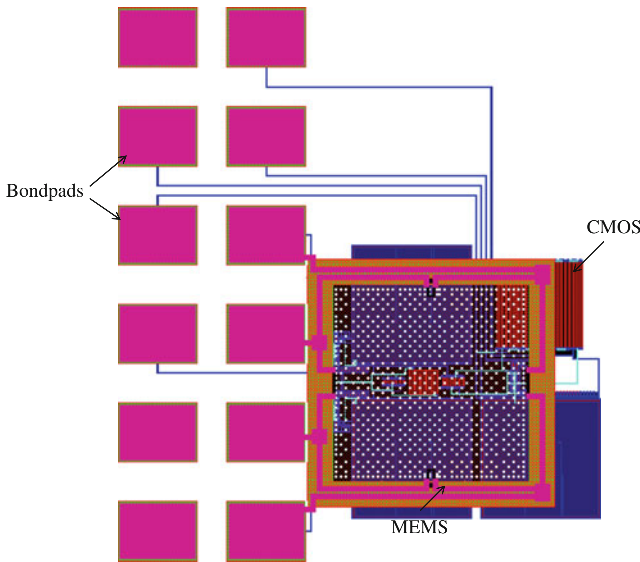


**Fig. A.3** Layout of an integrated pressure sensor: the CMOS circuit below (in *blue* metal 1 and in *red* the CMOS poly-Si layer) and the MEMS piezoresistive sensor on *top* are visible. The MEMS sensor bondpads are marked with a *circle*. The rest of the bondpads provide connection to the CMOS circuit bondpads below

Some of the piezoresistive pressure sensors include an electrode below the membrane to allow also for capacitive measurements. Figure A.5 shows a layout of such a sensor. These piezoresistive/capacitive pressure sensors include also two extra bondpads to connect to the membrane and the bottom electrode, respectively. Different bottom electrode areas were considered, from $50 \times 50$ up to $200 \times 200\,\mu m^2$. The combination of membrane areas and bottom electrode areas is as follows:

- For $200 \times 200\ \mu m^2$ sensors, the possible bottom electrodes areas are 50x50, $100 \times 100$ and $150 \times 150\,\mu m^2$.
- For $250 \times 250\,\mu m^2$ sensors, the possible bottom electrodes areas are $100 \times 100$, $150 \times 150$ and $200 \times 200\,\mu m^2$.
- For $300 \times 300\,\mu m^2$ sensors, the possible bottom electrodes areas are $100 \times 100$, and $200 \times 200\,\mu m^2$.

The MEMS stand-alone part can be further subdivided in the following sections:

**$200 \times 200\,\mu m^2$ sensors:**

This section includes 15 pressure sensors arranged in three rows with five sensors each, as can be seen in Fig. 1. Of these 15 sensors:

- Four sensors are piezoresistive-only pressure sensors with designs D1_T, D2, D3 and D3_T.

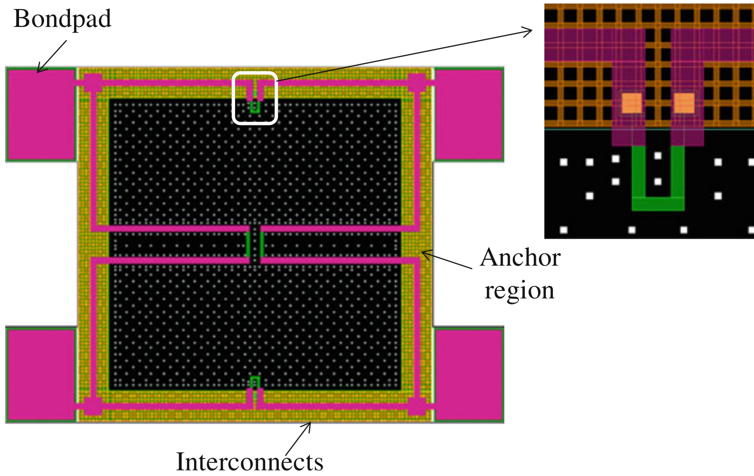


**Fig. A.4** Layout of a piezoresistive pressure sensor with design D2_T. A close-up view of the "n-shape" piezoresistor (*in green*), showing also the piezoresistor contact (*in yellow*) and the release holes (*in white*) is included. The bondpads are $60 \times 80\ \mu m^2$

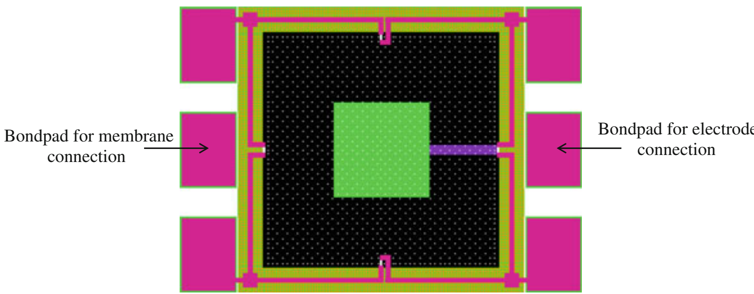


**Fig. A.5** Layout of a piezoresistive/capacitive pressure sensor, with piezoresistor design D1. The bottom electrode, realized using the SiGe electrode layer (see Chap. 4) is visible underneath the membrane. The two bondpads needed for capacitive measurements, connecting to the poly-SiGe membrane and bottom electrode, are indicated. The connection between the bondpad and the bottom SiGe electrode is realized using the MEMS AlCu bottom metal interconnect layer

- Five sensors are piezoresistive/capacitive sensors, with the following designs:
  - one sensor with piezoresistor design D3_T and bottom electrode of $150 \times 150\ \mu m^2$.
  - one sensor with piezoresistor design D3 and bottom electrode of $150 \times 150\ \mu m^2$.
  - one sensor with piezoresistor design D2 and bottom electrode of $100 \times 100\ \mu m^2$.
  - one sensor with piezoresistor design D1 and bottom electrode of $50 \times 50\ \mu m^2$.
  - one sensor with piezoresistor design D2_T and bottom electrode of $100 \times 100\ \mu m^2$.

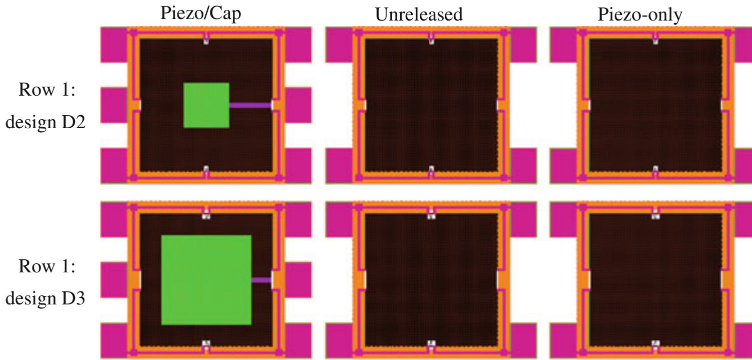


**Fig. A.6** Layout of the $300 \times 300\,\mu m^2$ sensor section

- Six reference sensors which are unreleased.

**$300 \times 300\,\mu m^2$ sensors:**

This section includes six pressure sensors arranged in two rows with 3 sensors each, as can be seen in Fig. A.6. These are the pressure sensors with the largest membrane area ($300 \times 300\,\mu m^2$). Three of the sensors (top row) have piezoresistor design D2 while the other three (bottom row) have design D3. The two central sensors are unreleased and are intended to be used as reference. Two of the sensors (on the left) are also capacitive sensors with electrode areas $100 \times 100\,\mu m^2$ (top) and $200 \times 200\,\mu m^2$ (bottom).

**$250 \times 250\,\mu m^2$ sensors:**

This section includes 18 pressure sensors arranged in three columns with 6 sensors each, as can be seen in Fig. 2b. Each column contains:

- Column 1: 6 piezoresistive/capacitive pressure sensors. The piezoresistor designs are, from top to bottom: D1, D2, D3, D1_T, D2_T and D3_T, respectively. The bottom electrode areas are, from top to bottom: $100 \times 100$, $150 \times 150$, $200 \times 200$, $100 \times 100$, $150 \times 150$ and $200 \times 200\,\mu m^2$, respectively.
- Column 2: 6 unreleased sensors with piezoresistors designs (from top to bottom) D1, D2, D3, D1_T, D2_T and D3_T, respectively.
- Column 3: 6 piezoresistive-only pressure sensors with piezoresistor designs (from top to bottom): D1, D2, D3, D1_T, D2_T and D3_T, respectively.

**Other:**

The section named "Other" in Fig. 1a contains four sensors. Two of them are $200 \times 200\,\mu m^2$unreleased piezoresistive/capacitive sensors to be used as reference. The other two sensors are rectangular sensors (membrane area $= 350 \times 175\,\mu m^2$) with piezoresistor design D3_T. One of the rectangular sensors include an electrode underneath the membrane (electrode area $= 100 \times 100\,\mu m^2$), to allow for capacitive measurements.

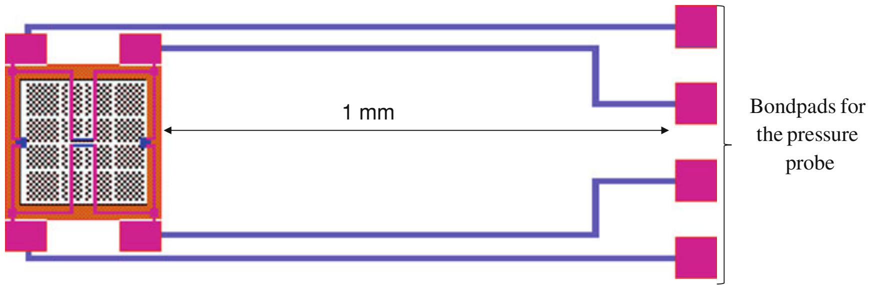


**Fig. A.7** Layout of a pressure sensor to be measured using the pressure probe setup in the university of Leuven-la-Neuve. The four bondpas where the probes of the tool will be placed are on the *right*, at a distance of 1 mm from the sensor. Four metal lines using the AlCu MEMS *bottom* interconnect layer connect these bondpads to the pressure sensor

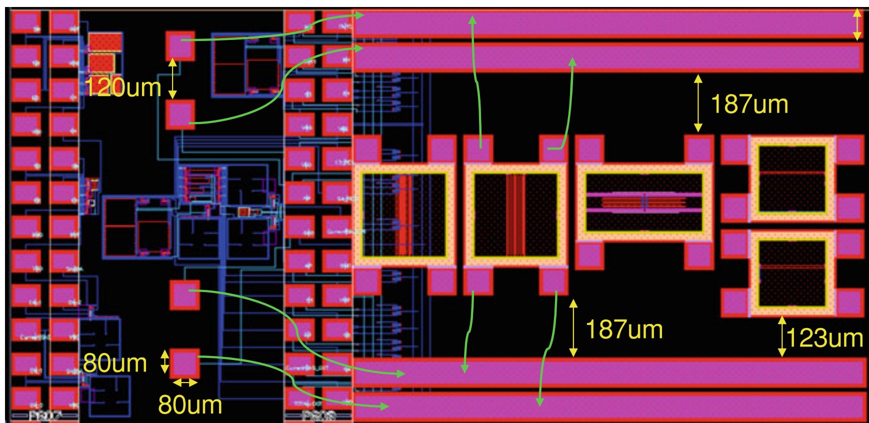


**Fig. A.8** Sensors for wirebonding, to study the MEMS-CMOS hybrid integration approach. On the *left*, the CMOS instrumentation amplifier is visible

### Sensors for pressure probe:

This section includes 10 piezoresistive-only sensors. Four of them are $200 \times 200\,\mu\text{m}^2$ with piezoresistor designs D3_T, D2_T, D3, D2, respectively. The other six sensors are $250 \times 250\,\mu\text{m}^2$ with piezoresistor designs D3_T, D3, D2_T, D2, D1_T and D1, respectively. These sensors are intended to be measured using SUSS pressure sensor measurement system (in the setup located in the University of Leuven-la-Neuve). This tool allows testing devices at wafer level under pressures up to seven bar. In order to be able to measure in this setup, the sensor layout has to fulfil certain specifications: The bondpads where the probes of the tool will be placed must be $80 \times 80\,\mu\text{m}^2$ in size with a pitch of $150\,\mu\text{m}$, placed at a distance of 1 mm from the sensor. Figure A.7 shows the layout of one of such sensors. Due to time limitations, these measurements could not be performed.

**Sensors for wirebonding:**

This section includes five piezoresistive only sensors: two $250 \times 250\,\mu m^2$ sensors with piezoresistor designs D2 and D3, respectively, one rectangular sensor with design D3_T and two $250 \times 250\,\mu m^2$ sensors with piezoresistor designs D2 and D3, respectively. These sensors are intended to be wirebonded to an instrumentation amplifier (Fig. A.8), in order to study the hybrid MEMS-CMOS integration approach, and allow for a comparison with the monolithic approach follow in this work. To allow for wirebonding, bigger bondpads (of $100 \times 100\,\mu m^2$) are used. Due to time limitations, these experiments could not be conducted.

# Appendix B

In Chap. 4, the fabrication process of the CMOS-compatible poly-SiGe based piezoresistive pressure sensors was presented. The performance of these sensors is explained in Chap. 6. However, in the frame of this work, poly-SiGe piezoresistive pressure sensors based on a simplified version of the process flow presented in Chap. 4 were also fabricated. This appendix deals with the fabrication and performance of such sensors. The results presented here were reported in [B1, B2].

The general fabrication process for the piezoresistive pressure sensors is schematically illustrated in Fig. B.1. These pressure sensors were fabricated starting at anchor level, and therefore do not include any of the bottom layers, such as metal and SiGe electrodes, SiC protection layer or MEMS vias. To avoid a short-circuit, since the conductive SiGe anchors are in contact with the also conductive Si substrate, the sealing layer on top of the bondpads is not opened. The electrical measurements are performed by probing on the AlCu layer that connects the piezoresistors, while the SiGe membrane and anchors remain isolated. Thanks to this, the final lithography/etch step of the sealing and SiGe membrane layers to separate the bondpads and cavities from one another, is not necessary. This process flow is therefore much shorter, and simple.
The main steps in the pressure sensor fabrication process illustrated in Fig. B.1 are (a more detailed description can be found in Chap. 4):

1. Deposition of 3 $\mu$m of sacrificial oxide, followed by the patterning of the membrane anchors (Fig. B.1a)
2. Deposition of the poly-SiGe membrane and filling of the anchors by a combination of CVD and PECVD processes (see Chap. 4). The total membrane thickness, estimated from cross-section pictures, is $\sim 3.1 \pm 0.1\,\mu$m.
3. To define the piezoresistors, a 200 nm-thick undoped poly-SiGe layer ($\sim$77 % Ge) is deposited, boron doped through implantation ($B \sim 1 \times 10^{19}\,cm^{-3}$), and annealed at 455°C for 2 h. A thin SiC layer ($\sim$60 nm) is used as isolation layer between the SiGe membrane and the SiGe piezoresistors. Note that the piezoresistors annealing used here is longer than the annealing time used in the final process flow described in Chap. 4 (30 min).

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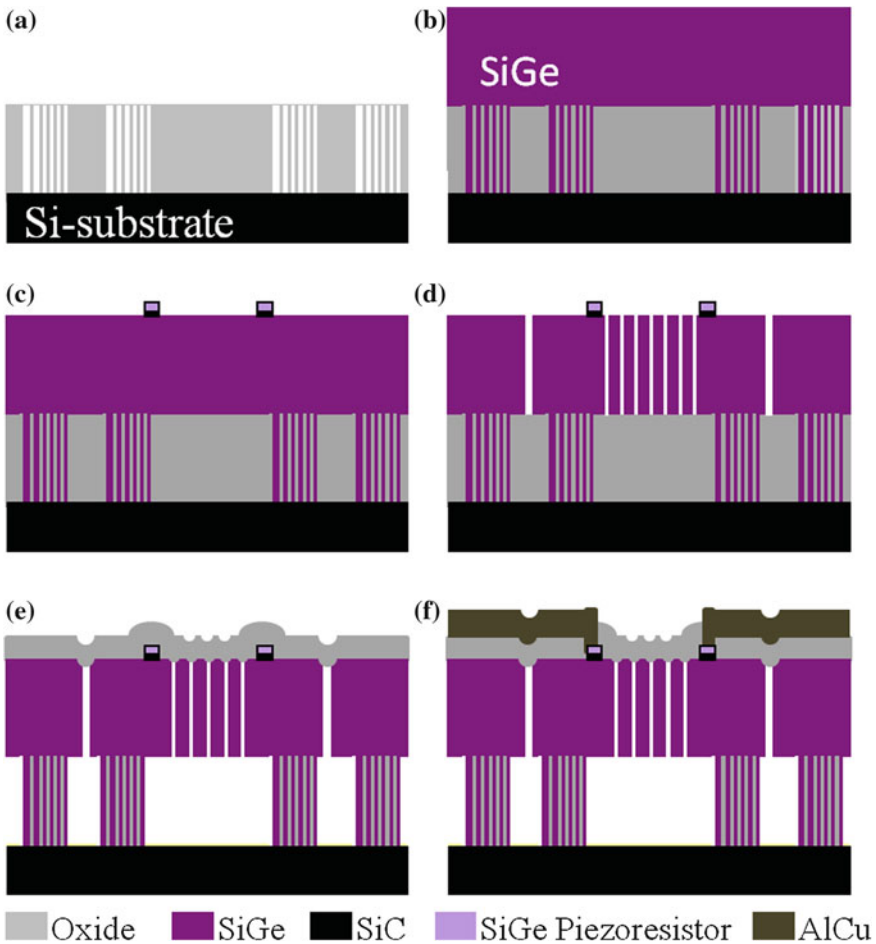


**Fig. B.1** Process flow. **a** Deposition of oxide and anchor patterning. **b** Deposition of poly-SiGe structural layer. **c** Piezoresistor patterning. **d** Opening of release holes. **e** Etching of the sacrificial oxide in vHF and sealing. **f** Deposition and patterning

4. Opening of $1 \times 1 \mu m^2$ etching channels in the membrane and removal of the sacrificial oxide by a combination of anhydrous vapor HF (AVHF) and ethanol vapor.
5. Sealing of the membrane with $\sim$1.2 µm of SACVD oxide. The cavity pressure after sealing, determined from load-deflection measurements, is $\sim$7 kPa (Chap. 5).
6. Opening of the piezoresistor contacts, followed by the deposition and patterning of a Ti (20 nm)/AlCu (880 nm)/TiN (60 nm) metal stack to connect the piezoresistors. This metal stack is different from the one used in the final runs (results reported in Chaps. 6 and 7). In those later runs the interconnect stack was 20 nm Ti/500 nm AlCu.

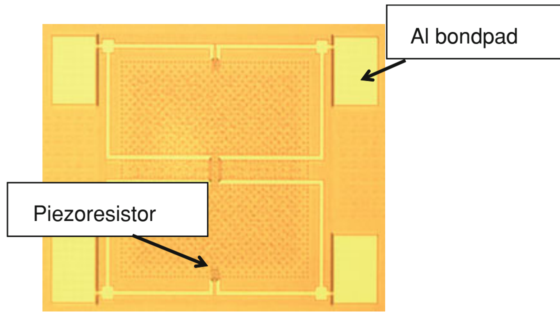


**Fig. B.2** Microscope picture of a fabricated device

**Table B.1** Measured sensor sensitivities (mV/V/bar) for the different designs

| Sensor Design | Sensitivity | Sensitivity from Chap. 6 |
|---|---|---|
| D1 | 2.15±0.1 | 1.78±0.05 |
| D1_T | 4.36±0.2 | 4.25±0.03 |
| D2 | 2.5±0.6 | 1.73±0.15 |
| D2_T | 4.6±0.5 | 4.17±0.4 |

The measured sensitivities for the same sensor designs in Chap. 6 are included for comparison

The maximum processing temperature used during the fabrication of these devices was again 455°C. Figure B.2 shows a microscope picture of one of the fabricated devices. The devices described here belong to an older run as compared to the devices reported in Chap. 6, and the original lithography masks were used. Therefore the width of the anchor trenches is 1 μm, instead of 0.8 μm, and the piezoresistor contacts are only $1 \times 1\,\mu m^2$, with the consequent bad Al filling (see Chap. 4 for more information). Considering this bad Al filling, the electrical contact to the piezoresistors is thought to be given by the highly conformal thin Ti bottom layer of the metal interconnect stack.

Due to severe delamination issues, together with the bad Al-filling of the piezoresistor contacts, only a few working devices were found in the wafer. Only pressure sensors with a membrane area of $200 \times 200\,\mu m^2$ and piezoresistor designs D1, D1_T, D2 and D2_T (see Fig. 6.3) could be measured. Designs D1 and D2 correspond to sensors with "line-shape" and "n-shape" longitudinal piezoresistors, respectively, with the transverse piezoresistors placed at the membrane edge. The sufix _T indicates that the transverse piezoresistors are placed at the centre of the membrane. The pressure sensors were tested in the pressure range from 0 to 1 bar with an input driving voltage of 3.3 V, using the same measurement setup as in Fig. 6.1. Figure B.3 shows the measured output voltage as a function of applied pressure for the four different sensor designs. All the measurements were performed at room temperature.
The corresponding measured sensitivities are listed in Table B.1. Similar as predicted in the simulations in Chap. 3, by placing the transverse piezoresistors in the centre of the membrane, the sensitivity could be improved by a factor of ∼2, while

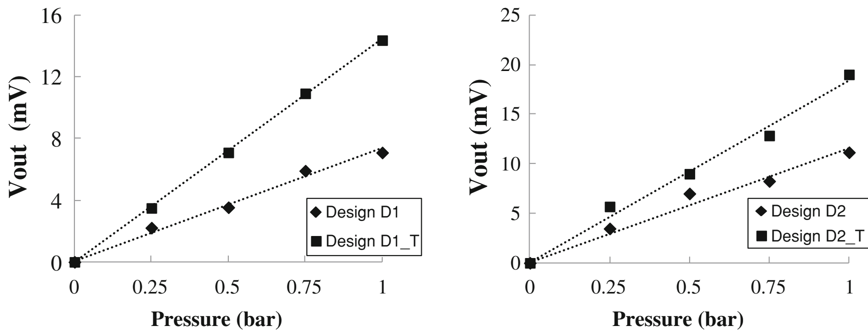


**Fig. B.3** Measured output voltage as a function of the applied pressure for the four different types of sensorssensors with longitudinal resistors. The data point at vacuum is taken as reference for the data, to eliminate the bridge offset. The number of samples considered are 2, 3, 5 and 4 for designs D1, D1_T, D2 and D2_T, respectively

no significant impact of longitudinal piezoresistor shape on the sensor sensitivity is observed. Comparing to the results obtained for the same sensor designs in Chap. 6, the same behaviour with respect to sensor design is observed, although the sensitivities reported here are slightly larger than those reported in Chap. 6. One possible explanation can be the slightly thinner SiGe membrane used here (3.1 μm instead of 3.25 μm). A larger spread in the sensitivity values with respect to Chap. 6 is also observed.

## References Appendix B

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# Appendix C

In Chap. 5, the sealing of poly-SiGe membranes released through a μc-SiGe porous cover was presented. The use of a porous cover has two main advantages: it prevents the deposition of sealing material inside the cavity and reduces the minimum required thickness of the sealing layer. In this appendix, the use of SiC as porous cover is investigated.

As already discussed in Chap. 5, it is preferred to use a material with a thermal expansion coefficient (CTE) close to that of the poly-SiGe membrane in order to limit the effect of this porous cover on the thermal behaviour of the sealed membrane. Moreover, since this porous cover could eventually be used as isolation between the poly-SiGe piezoresistors and the poly-SiGe membrane in the pressure sensor process flow, it must be a non-conductive layer. SiC is a good candidate since it is a good electrical insulator and has a CTE of 4.5 ppm/° C, very close to that of poly-SiGe (5 ppm/° C). However, due to the poor adhesion between SiC and the SiGe membrane, an intermediate "glue" layer has to be used to avoid delamination problems. In this work, titanium nitride (TiN), titanium (Ti) and a combination of titanium/titanium nitride (Ti/TiN) were considered as adhesive layer. Figure C.1 shows microscope pictures of poly-SiGe membranes released through a 100 nm-thick porous SiC layer for the different adhesive layers considered. The pictures on the bottom were taken after a tape test was performed to evaluate the efficiency of the release. All metal liner recipes include 2 nm pre-sputtering. In some cases an annealing step of 455° C for 1 h was applied before the SiC deposition. All the wafers were released using the standard vHF recipe (eight steps of 8 min).

In most of the cases "bubbles" were visible, probably due to delamination of the SiC porous layer. The 5 nm-thick Ti layer seems to give the best adhesion. However when a thicker (15 nm) Ti layer is used, delamination occurs probably due to the underetching of the Ti-SiC interface in vHF [C1] due to the small, but existing, etch rate of Ti in vHF. On the other hand, all the cavities are successfully released. In the case where TiN is used as adhesion layer (either alone or together with Ti), there are particles visible in the bottom of the cavity after tape test. These particles might be

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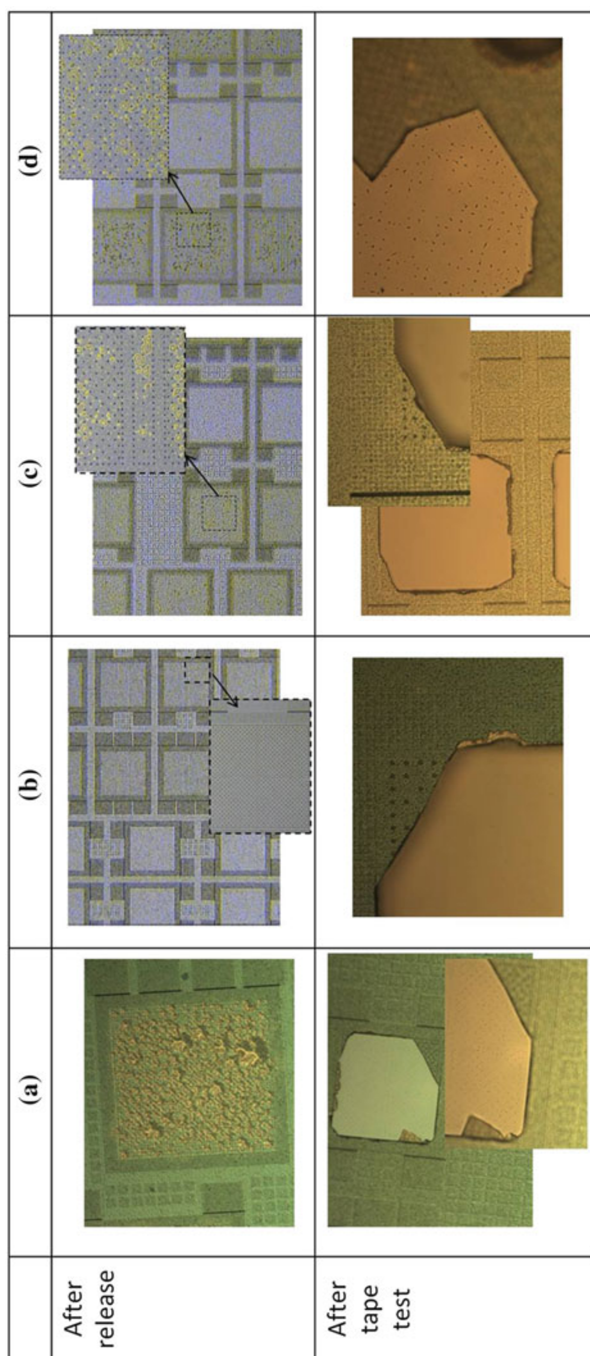


**Fig. C.1** Microscope pictures of poly-SiGe membranes after vHF release (*top row*) and after tape test (*bottom row*). Each column illustrates a different glue layer: **a** Ti/TiN 5/10 nm + 1 h annealing at 455 C + SiC 100 nm, **b** Ti 5 nm + SiC 100 nm, **c** Ti 15 nm + SiC 100 nm, **d** TiN 20 nm + 1 h annealing at 455 C + SiC 100 nm

due to a reaction of vHF with the N-containing TiN layer as also seen in other work and for other N-containing layers [C1, C2].

**References Appendix C**

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# Appendix D

To check the CMOS compatibility of the proposed process flows, annealing tests were performed on CMOS wafers fabricated with imec's 0.13 μm technology, with Cu-interconnects (two metal layers), oxide dielectric and Cu-filled metal-to-metal vias with a TaN/Ta liner. Similar tests, to determine the thermal budget limits for 0.35 μm and 0.25 μm CMOS wafers with aluminum based interconnects, have already been reported in [D1] and [D2], respectively. In this work, for the first time, such a study is performed on CMOS wafers with copper interconnects.

The CMOS test wafers were annealed in a traditional furnace. Three different annealing times were considered: 2, 4 and 6 h. The annealing temperature was set to 455° C, which corresponds to the maximum processing temperature used in this work for the fabrication of the poly-SiGe pressure sensors. Table D.1 demonstrates the effect of annealing time on relevant transistor parameters. The threshold voltage, in the linear and saturation region, has been measured at a drain to source voltage of 0.1 and 1.2 V, respectively. After annealing for 2 h at 455° C, the threshold voltage slightly increased. However, longer anneals of 4 or 6 h did not change the threshold voltage further. The change for the linear threshold voltage was ∼8 mV (= 3.2 %), while for the saturation threshold voltage the increase was ∼11.3 mV (= 3.4 %). Also for PMOS (Positive channel MOS) transistors an increase in threshold voltage was observed. Similar results were obtained in [D2], where electron trapping during the annealing step was proposed as explanation. The transistor leakage current decreases with increasing annealing time, which is positive for transistor performance. The maximum decrease in leakage current was ∼40 %, corresponding to the longest annealing time. On the other hand, the drive current seems to decrease with annealing time, although the change (<3 %) is within the measurement error margin.

From Fig. D.1a we can see that the sheet resistance of the Cu metal 2 line decreases slightly with annealing time. The maximum change, corresponding to the longest annealing time, is ∼1%. For metal 1 a similar result was found, with a maximum change of ∼0.5%. However these changes are within the error margin and can be considered negligible. Figure D.1b plots the via resistance change as a function of annealing time. These are copper filled vias connecting the two metal lines. The

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**Table D.1** Effect of the annealing time on the threshold voltage, leakage current and drive current for nMOS (Negative channel MOS) transistor. The annealing temperature is 455 °C.

| | **Annealing time** | | | |
|---|---|---|---|---|
| | **Standard** | **2h** | **4h** | **6h** |
| Threshold voltage (linear) | 0.249 V±10 mV | 0.257 V±5 mV | 0.256 V±4mV | 0.257 V±10 mV |
| Threshold voltage (saturation) | 0.334 V±15 mV | 0.343 V±5 mV | 0.348 V±4 mV | 0.344 V±10 mV |
| Leakage current (μA/μm) | $3.5\pm0.5\cdot10^{-10}$ | $2.98\pm1\cdot10^{-10}$ | $2.36\pm0.5\cdot10^{-10}$ | $2.1\pm0.5\cdot10^{-10}$ |
| Drive current (μA/μm) | 700±15 | 689±20 | 681±20 | 683±5 |

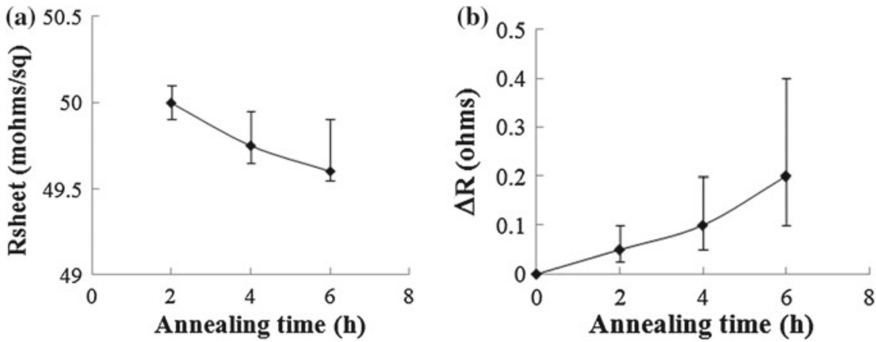


**Fig. D.1** **a** Effect of annealing time on the sheet resistance of Cu metal two line. **b** Variation with annealing time of the mean value of the contact resistance between the two metal lines. The initial contact resistance is 2.4 ohms

via resistance appears to increase nonlinearly with annealing time, with the rate of change increasing also with annealing time. The maximum resistance increase is ~8.3% and corresponds to an annealing time of 6 hours. This value, although not negligible, is still lower than the failure limit, defined as a 10% increase in the mean via resistance [D2].

Since the effect of the annealing time on the MOSFETS characteristics and sheet resistance of the metal interconnects can be considered insignificant, we can conclude that, for a maximum processing temperature of 455° C, the degradation in metal-to-metal via resistance is the factor limiting the MEMS thermal budget for post-processing on top of Cu-based CMOS wafers. For poly-SiGe flows with a total processing time at 455° C (maximum temperature) $\leq$ 6 h, the expected increase in via resistance is less than 10 % (failure limit). However, for longer processing times, the degradation in via resistance might be an issue for the successful integration on top of Cu-based CMOS. Therefore, limiting the processing temperature of the poly-SiGe MEMS to a maximum of 455° C may not always be enough to ensure CMOS-compatibility of the process flow.

## References Appendix D

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