Chapter 8
Quantization Error According to Bit Truncation Method in 4k-FFT Algorithm

Sangjung Ra, Dongjoon Choi, Namho Hur, Sangjin Ryoo and Cheolsung Kim

Abstract In this paper, we compare a quantization error performance of FFT algorithm according to bit truncation method. 4k-FFT algorithm of OFDM is proposed and implemented in field programmable gate arrays (FPGAs). We analyze the quantization error performance according to bit truncation method. Measured results show the maximum quantization error of 6.042152/6.067595 (real/imaginary value in 12 stage MSB truncation), 3.112953/2.627594 (real/imaginary value in 12 stage LSB truncation), 0.006065/0.005448 (real/imaginary value in 6 stage LSB/6 stage MSB truncation) in 1st method. And measured results show the maximum quantization error of 0.001464/0.00129 (real/imaginary value in truncation after FFT) in 2nd method.

Keywords Quantization error · Bit truncation · Hardware implementation · FFT · OFDM

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8.1 Introduction

In most of the wired/wireless system, OFDM is general structure for operation. In OFDM system, FFT algorithm is very crucial part and plays an important role in performance [1].

In this paper, we compare and analyze the quantization error performance of FFT algorithm according to bit truncation method. The first method is the way to handle the truncation within stage. Bit truncation is processed a Most Significant Bit (MSB) or Least Significant Bit (LSB) at all stage. Or previous 6 stage is truncated LSB and next 6 stage is truncated MSB. The second method is the way to handle the truncation after FFT. We implement a FFT algorithm of OFDM with FPGA for prototype. And, we measure the quantization error after bit truncation in 4k-FFT algorithm [2].

8.2 Structure of FFT Algorithm Including Truncation Block

8.2.1 Overall Structure of 4k-FFT Algorithm

Figure 8.1 shows an implemented structure of 4k-FFT algorithm including truncation block. 4k-FFT algorithm includes all 12 stage. Each stage has radix-2 butterfly structure. After passing through a stage, processing capacity is halved. For example, 1st stage's processing capacity is 4096 and 2nd stage's processing capacity is 2048, and so on [1, 3–5]. At every stage is 20 bits of the output of all stages because it involves the truncation block.

8.2.2 Stage Structure in 4k-FFT Algorithm

Figure 8.2 shows a detailed implementation structure of 1st to 11th stage in 4k-FFT algorithm. Even stage is different from odd stage. Even stage is multiplication of input data. But odd stage is multiply unique value named twiddle factor [1].

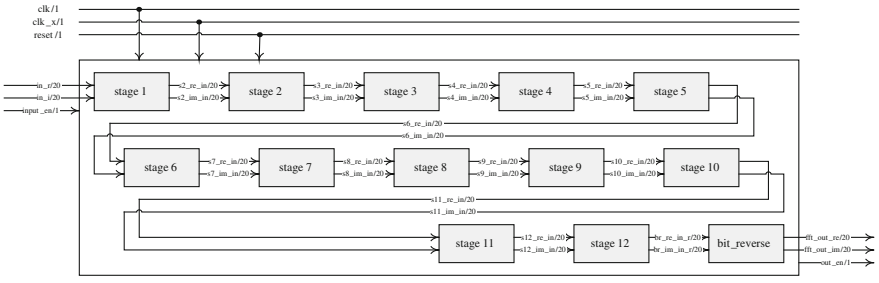

Fig. 8.1 Structure of 4k-FFT algorithm including truncation block

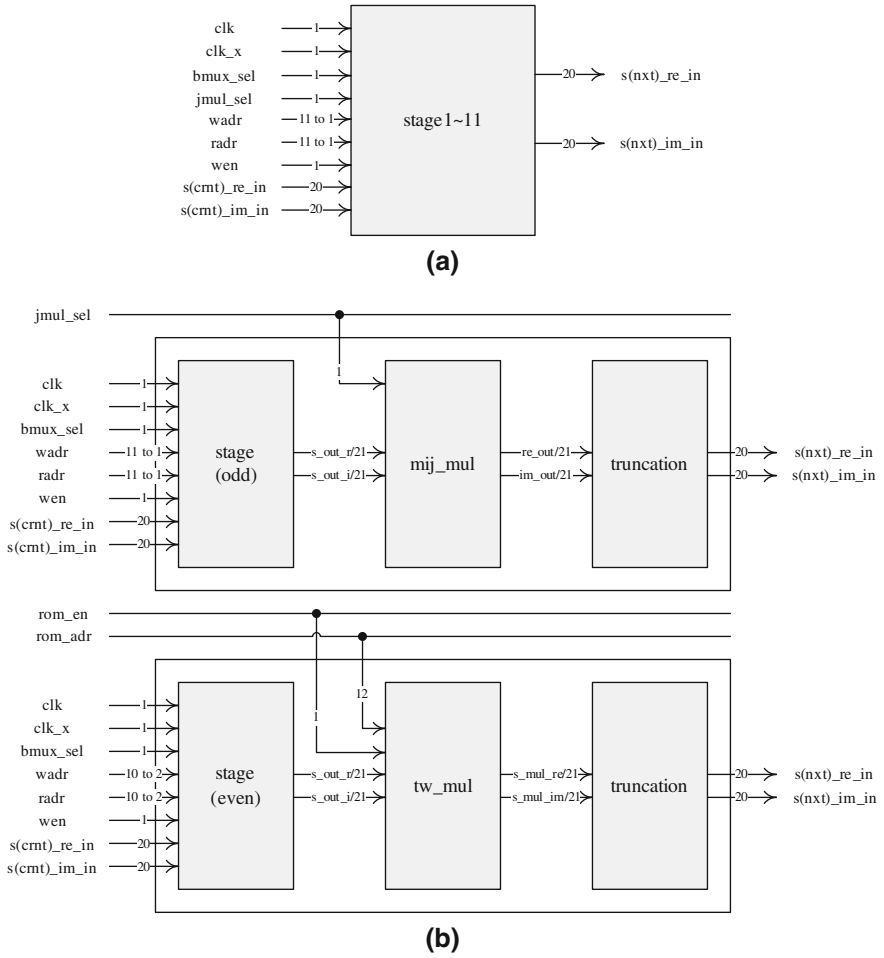

Fig. 8.2 Detailed 1st to 11th stage structure of 4k-FFT algorithm

Figure 8.3 shows a detailed structure of 12th stage in 4k-FFT algorithm. Twelfth stage is processed 1 data symbol, so multiplication block is removed.

8.2.3 Bit Truncation in 4k-FFT Algorithm

As noted earlier, every stage has truncation block. Truncation block is operated on control the number of processing bits in every stage. Processing bit can't be used indefinitely for hardware implementation. For hardware implementation, it is controlled the number of bits in truncation block. According to bit truncation method, performance of FFT algorithm has changed.

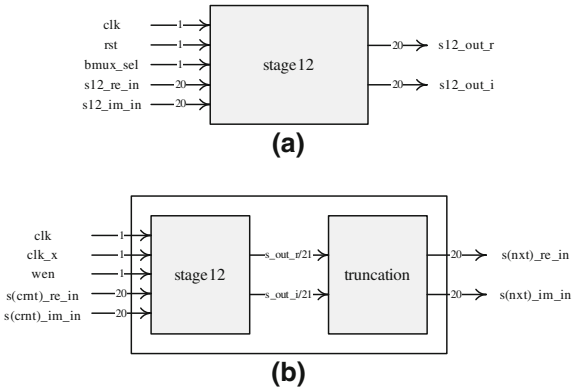

Fig. 8.3 Detailed 12th stage structure of 4k-FFT algorithm

In case of MSB truncation method, input bit is 21 bits and output bits is 20 bits because the MSB 1 bit will work to remove. In case of LSB truncation method, input bit is 21 bits and output bits is 20 bits because the LSB 1 bit will work to remove [1].

8.3 Structure of FFT Algorithm by Truncation After FFT

8.3.1 Overall Structure of 4k-FFT Algorithm

Figure 8.4 shows an implemented structure of 4k-FFT algorithm by truncation after FFT. Truncation is processed after 12 stage operation. Because of truncation method, every bit is incremented by one in every stage.

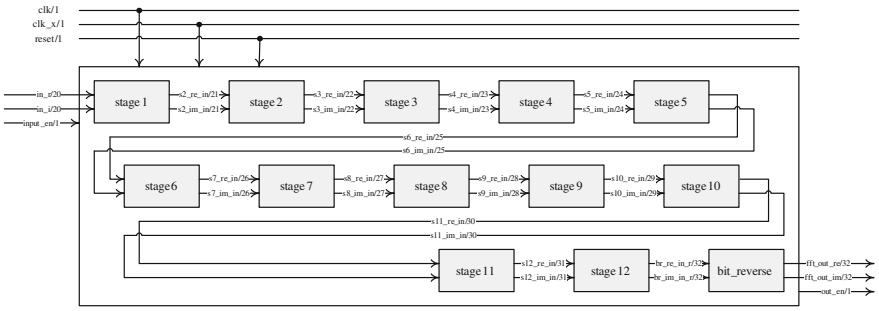

Fig. 8.4 Structure of 4k-FFT algorithm by truncation after FFT

8.3.2 Stage Structure in 4k-FFT Algorithm

Figure 8.5 shows a detailed implementation structure of 1st to 11th stage in 4k-FFT algorithm. Because truncation is processed after FFT operation, truncation block is removed in stage block.

Figure 8.6 shows a detailed structure of 12th stage in 4k-FFT algorithm. Twelfth stage is processed 1 data symbol, so multiplication block is removed. Also truncation is processed after FFT operation, truncation block is removed in stage block, too.

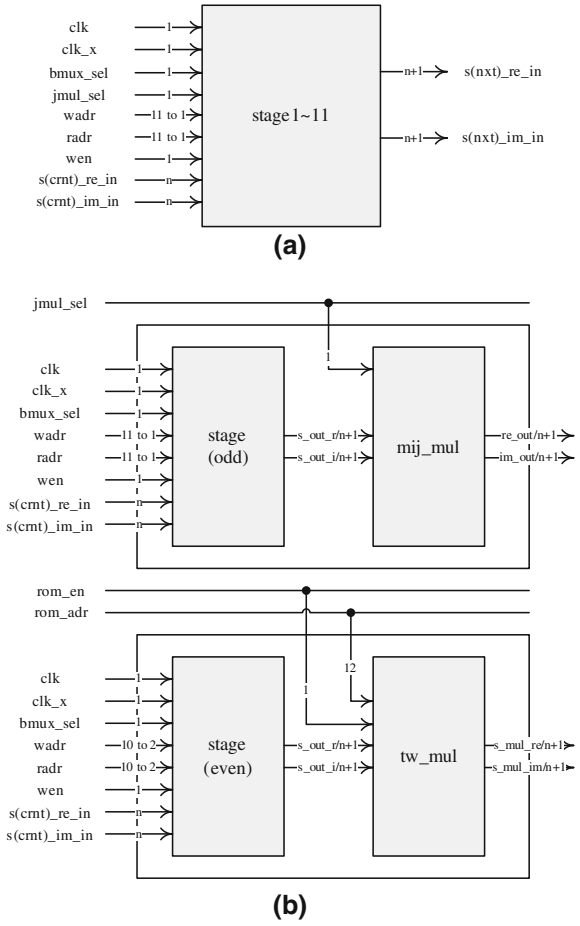

Fig. 8.5 Detailed 1st to 11th stage structure of 4k-FFT algorithm

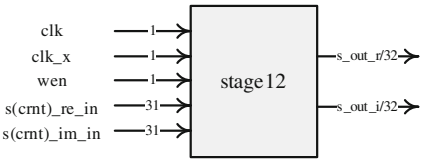

Fig. 8.6 Detailed 12th stage structure of 4k-FFT algorithm

8.3.3 Bit Truncation in 4k-FFT Algorithm

Likewise Sect. 8.2.3, bit truncation process is used to control the number of processing bits. In hardware implementation, processing bit can't be used indefinitely. Because of that, truncation process is controlled the number of bits after FFT operation.

In this approach, which operates by selecting only 20-bits of the full 32-bit valid.

8.4 Hardware Implementation

Figure 8.7 shows the developed and tested hardware implementation for 4k-FFT algorithm.

8.5 Test Results

Figures 8.8, 8.9 and 8.10 shows a quantization error of 4k-FFT output including truncation block in stage processing. Figure 8.8 is operated by 12 stage MSB truncation and Fig. 8.9 is operated by 12 stage LSB truncation. And Fig. 8.10 is operated by 6 stage LSB truncation and 6 stage MSB truncation. We measure the quantization error of 4k-FFT output. Measured results show the maximum quantization error of 6.042152/6.067596 (real/imaginary value in 12 stage MSB truncation), 3.112953/2.627594 (real/imaginary value in 12 stage LSB truncation), 0.006065/0.005448 (real/imaginary value in 6 stage LSB/6 stage MSB truncation).

And Fig. 8.11 shows a quantization error of 4k-FFT output by truncation after FFT. Measured results show the maximum quantization error of 0.001464/0.00129.

Table 8.1 shows the maximum/minimum quantization error value in 4k-FFT algorithm applied 12 stage MSB truncation. And Fig. 8.8 shows the real and imaginary quantization error after 12 stage MSB truncation.

Table 8.2 shows the maximum/minimum quantization error value in 4k-FFT algorithm applied 12 stage LSB truncation. And Fig. 8.9 shows the real and imaginary quantization error after 12 stage LSB truncation.

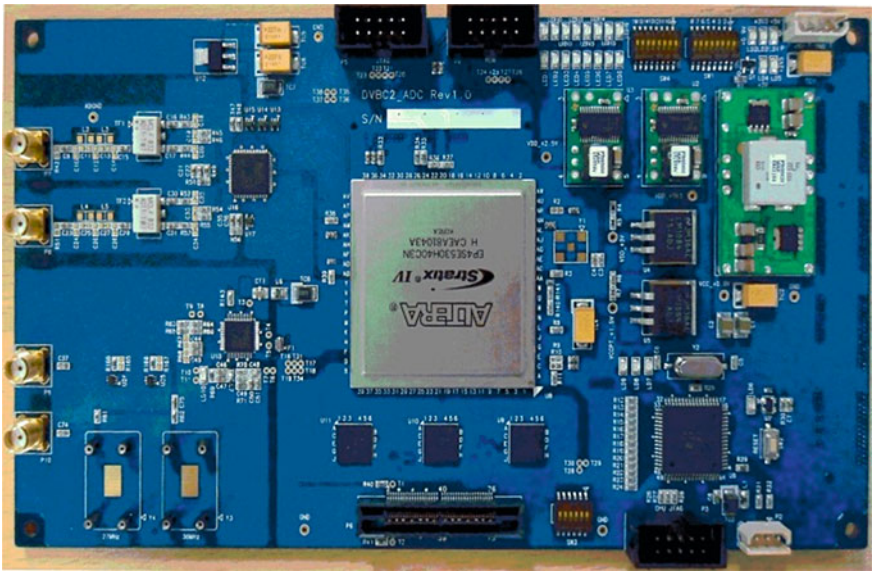

Fig. 8.7 Hardware implementation for 4k-FFT algorithm

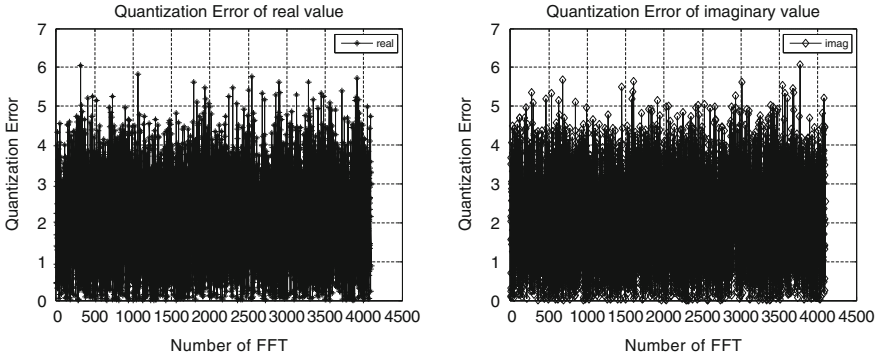

Fig. 8.8 Quantization error of 12 stage MSB truncation in 4k-FFT real/imaginary value

Table 8.3 shows the maximum/minimum quantization error value in 4k-FFT algorithm applied 6 stage LSB truncation and 6 stage MSB truncation. And Fig. 8.10 shows the real and imaginary quantization error after 6 stage LSB truncation and 6 stage MSB truncation.

Table 8.4 shows the maximum/minimum quantization error value in 4 k-FFT algorithm applied by truncation after FFT. And Fig. 8.11 shows the real and imaginary quantization error by truncation after FFT.

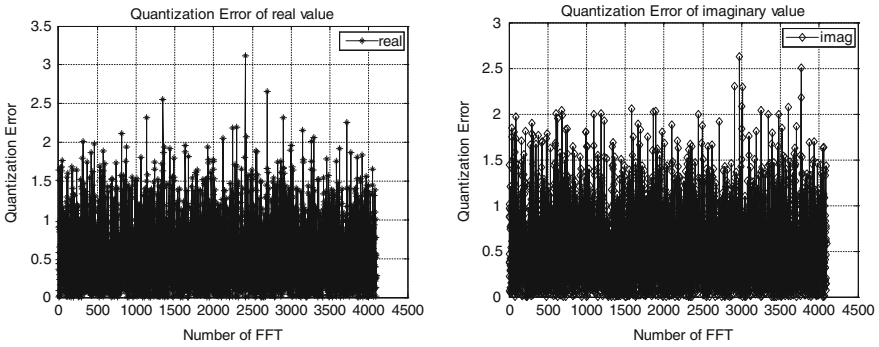

Fig. 8.9 Quantization error of 12 stage LSB truncation in 4k-FFT real/imaginary value

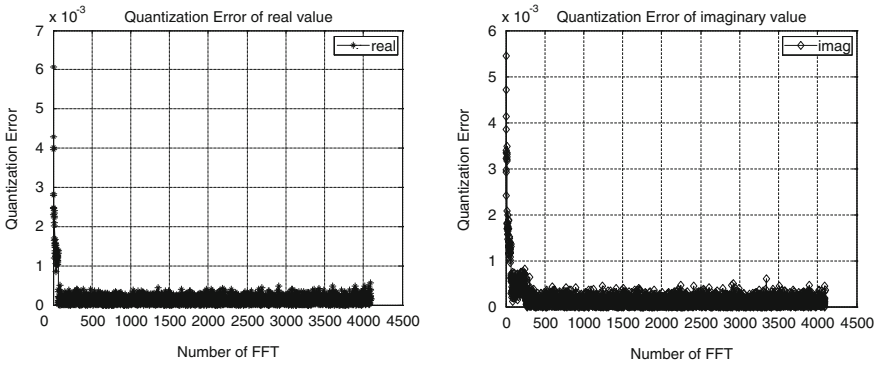

Fig. 8.10 Quantization error of 6 stage LSB/6 stage MSB truncation in 4k-FFT real/imaginary value

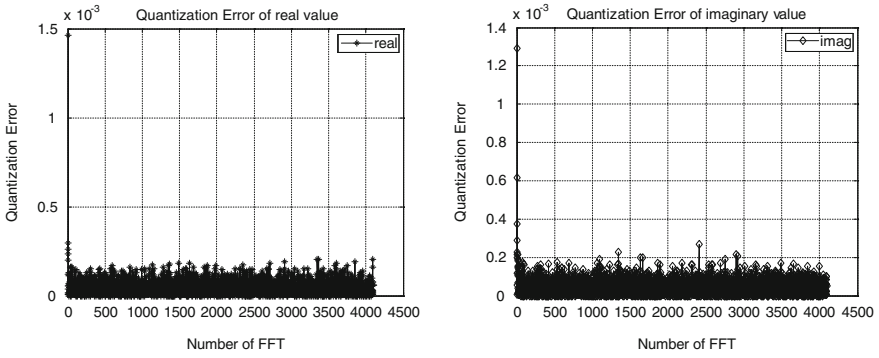

Fig. 8.11 Quantization error by truncation after FFT in 4k-FFT real/imaginary value

Table 8.1 Maximum/Minimum quantization error value in 4k-FFT 12 stage MSB truncation

Quantization error			
Real value		Imaginary value	
Maximum	Minimum	Maximum	Minimum
6.042152	0.000214	6.067596	0.000328

Table 8.2 Maximum/Minimum quantization error value in 4k-FFT 12 stage LSB truncation

Quantization error			
Real value		Imaginary value	
Maximum	Minimum	Maximum	Minimum
3.112953	0.000679	2.627594	0.000145

Table 8.3 Maximum/Minimum quantization error value in 4k-FFT 6 stage LSB/6 stage MSB truncation

Quantization error			
Real value		Imaginary value	
Maximum	Minimum	Maximum	Minimum
0.006065	0	0.005448	0

Table 8.4 Maximum/Minimum quantization error value in 4k-FFT bit truncation after FFT

Quantization error			
Real value		Imaginary value	
Maximum	Minimum	Maximum	Minimum
0.001464	0	0.00129	0

8.6 Conclusion

In this paper, we analyze a quantization error for design and implementation of 4k-FFT algorithm. Bit truncation method is adjusted to optimize hardware performance. Four kinds of simulation showed the best performance of truncation after FFT output. The developed 4k-FFT algorithm has been tested in laboratory environment.

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