Chapter 1
Device Stability and Photo-Excited Charge-Collection Spectroscopy

Abstract Important performance factors and basic device physics of organic or inorganic-channel thin-film transistors (TFTs) are addressed before introducing the photo-excited charge collection spectroscopy (PECCS), so that systematic and in-depth understanding on the device stability issues may be naturally drawn in focus. Device architecture, device physics, and general stability issues in TFT (or field-effect transistor) are thus introduced in the initial sections, and in the last section our photon-probing technique is explained along with its own device physics.

1.1 Thin-Film Transistor Architectures for Photon Probe Measurements

In general, there are four types of thin-film transistor (TFT) architectures: staggered, inverted staggered, coplanar, and inverted coplanar [1–4]. As shown below in Fig. 1.1, bottom gate TFTs with inverted staggered or inverted coplanar types are quite manageable for the photon probe measurements since they already have transparent windows above active semiconductor channels. In contrast, the top gate devices such as staggered or coplanar type need transparent gate electrodes for the photon measurements. In our experimentations of the following chapters, we usually take the inverted staggered type for bottom gate and the staggered type for top gate devices.

1.2 Device Physics and Equations for Thin-Film Transistors

1.2.1 Gradual Channel Approximation

As in the case of Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs), TFTs have two different operational regimes depending on the drain voltage: linear

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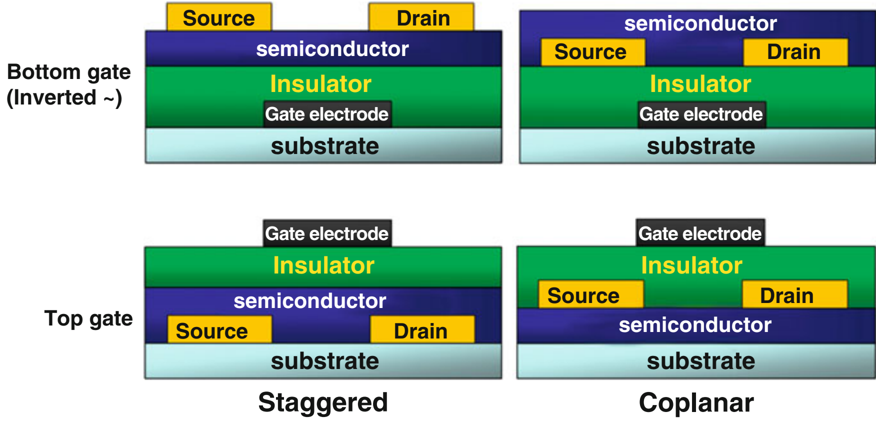

Fig. 1.1 The four types of TFT in device architectures: top gate and bottom gate (Inverted) types for staggered or coplanar TFTs

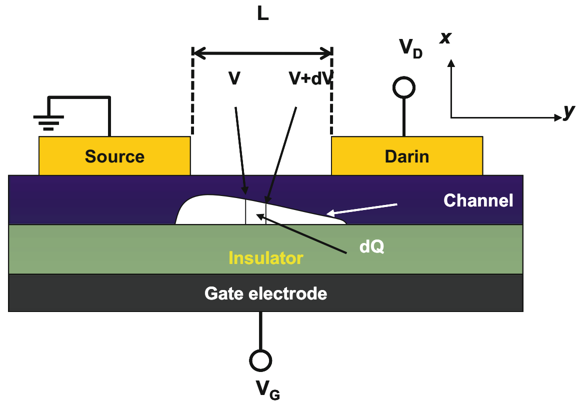

Fig. 1.2 Cross sectional view illustrating the gradual channel model

and saturation. A gradual channel approximation is assumed for the TFT channel, where y is the source-to-drain direction while z is the channel thickness direction perpendicular to the channel. The carrier density per unit area in the channel is the function of y-direction potential V_y caused by drain bias V_D. We illustrate the cross section of an inverted stagger type bottom gate TFT in Fig. 1.2 [5–7].

When the gate potential/voltage V_G overcomes the threshold voltage V_{th}, the accumulated mobile charge density Q_z is presented as the function of V_y and V_G in the following the formula

$$Q_z(y) = C_{ox}\left(V_G - V_{th} - V_y\right), \tag{1.1}$$

where C_{ox} is the capacitance per unit area of gate insulator (GI). Since the accumulated mobile charges are composed of majority carriers at/near the

channel/dielectric (or GI) interface, the drain current I_D comes out from the following equations,

$$J_n = I_D/(W \cdot Z) = nq\mu E_y = nQ_z\left(dV_y/dy\right)/Z, \quad (1.2)$$

where J_n is the current density, W is the channel width, Z is the channel thickness as a function of V_y and V_G, E_y is the electric-field (E-field) between source and drain, μ is the average carrier mobility (field-effect mobility), and n is the average carrier concentration in the channel as a function of V_G. Now, $Q_z(y)$ is presented to be nqZ as the function of V_y (at a certain y position) under a fixed value of V_G. Therefore, the drain current I_D is defined at a certain V_G as below.

$$I_D = W\mu Q_z\left(dV_y/dy\right), \quad (1.3)$$

$$I_D dy = W\mu Q_Z\left(dV_y\right) = W\mu Q_z\left(C_{ox}\left(V_G - V_{th} - V_y\right)\right)dV_y \quad (1.4)$$

Since V_{th} and V_G are constant values, we can extract the I_D from Eq. (1.4) by integrating the equation over the channel length range ($0 \sim L$) which is corresponding to the respective voltage range from 0 to V_D, the drain voltage. As results, we obtain the following well-known equation,

$$I_D = \mu \cdot C_{ox}(W/L)\left[(V_G - V_{th})V_D - (1/2)V_D^2\right] \quad (1.5)$$

In the linear regime, $V_D \ll V_G - V_{th}$ so that I_D can be expressed as below using μ_{Lin}, the linear mobility.

$$I_D = \mu_{Lin} \cdot C_{ox}(W/L)[(V_G - V_{th})V_D] \quad (1.6)$$

The gate field-induced carriers are quickly depleted to the drain electrode as the V_D increases, and eventually when V_D comes across the condition of $V_D = V_G - V_{th}$, the carrier channel becomes completely pinched-off at a ceratin V_D causing the I_D saturation. Then, for the condition of $V_D > V_G - V_{th}$, Eq. (1.5) is no longer valid. Instead, we generally use an empirical equation below,

$$I_D = \mu_{Sat} \cdot C_{ox}(W/2L)(V_G - V_{th})^2, \quad (1.7)$$

which uses the saturation mobility, μ_{Sat}. Besides such a deviation from simple gradual channel approximation in the saturation regime, contact resistance in the source/drain and V_G-dependent mobility can also influence the I_D behavior in TFTs.

1.2.2 V_{th} Equation and Related Physics

The threshold voltage (V_{th}; practical turn-on voltage) and μ_{Sat} are experimentally extracted from the I_D-V_G transfer curve characterizations following Eq. (1.7) and experimentations on TFTs. However, device physics of a TFT expects a theoretical equation, too, similar to the case of MOSFET [8–10].

$$V_{th} = \phi_{ms} - \frac{Q_{eff}}{C_{ox}} + \Psi_{s,\max} + \frac{Q_G}{C_{ox}} \tag{1.8}$$

With

$$Q_{eff} = q \int_{VBM}^{CBM} D_{it,e}(E)F(E)dE, \ for \quad n - channel,$$

$$q \int_{CBM}^{VBM} D_{it,h}(E)\{1 - F(E)\}dE, \ for \quad p - channel \tag{1.9}$$

where the effective trap charge (Q_{eff}) is mainly for the traps located at the channel/dielectric interface, ϕ_{ms} is the metal–semiconductor work function difference, C_{ox} is the dielectric capacitance per unit area (F·cm^{-2}), $\psi_{s,max}$ is the potential due to a band bending of the channel semiconductor, Q_G is the charge associated with a dielectric band bending as induced by gate bias, N_b is the density (cm^{-3}) of bulk traps in the gate dielectric, t_{ox} is the dielectric thickness (nm), $D_{it,\ e}$ is the DOS of electron traps at the n-channel/dielectric interface, $D_{it,\ h}$ is the DOS of hole traps at the p-channel/dielectric interface (cm^{-2}eV^{-1}), and *F(E)* is the Fermi–Dirac distribution function whose value must be 1 for n-channel and 0 for p-channel. The first and second terms on the left-hand side of Eq. (1.8) is the same as the flat band voltage (V_{FB}) of a transistor [11].

In view of the threshold voltage Eq. (1.8), the most important and changeable factor is probably Q_{eff} which is located at/or very near the interface between dielectric and semiconductor channel, since the effective charge could be large or small depending on the interface state which always consists of such a variety of hetero-systems as organic/inorganic, organic/organic, and sometimes inorganic/inorganic. Hence, minimizing or controlling Q_{eff} in an appropriate way has been quite an important issue in TFT history, which actually began with a crystalline CdS or CdSe channel in the 1960s, rather than with an amorphous Si channel. Even though the crystalline CdS TFTs demonstrated field effect mobilities of over 150 cm^2/V s, time- and temperature-dependent performance changes (mobility and V_{th}) made those devices ineffective, and the hope rolled over to amorphous-Si channel TFTs in the 1970–1980 with the advent of liquid crystal display (LCD) composed of TFT, storage capacitor, and LC pixel came [12, 13]. The schematic band diagram and I_D-V_G transfer curves in Fig. 1.3 illustrates the interfacial states which trap mobile charges to change V_{th} or the flat band voltage (V_{FB}) of device, while Fig. 1.4 shows a modern electrically stable active matrix TFT pixel composed with amorphous-Si TFT and dielectric storage capacitor (Cs), along with its circuitry [5, 14].

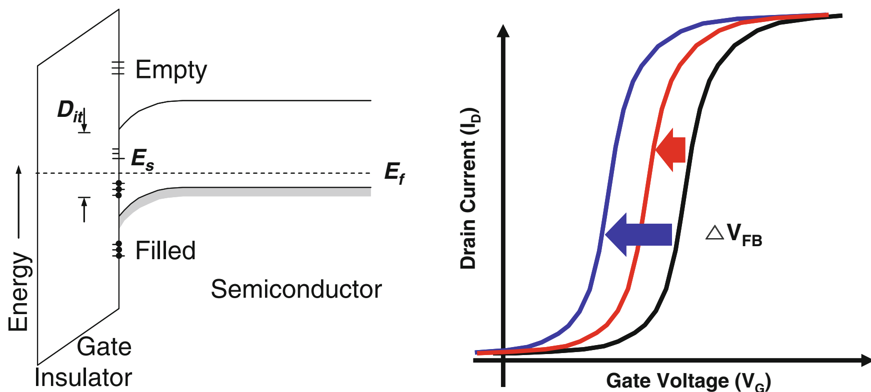

Fig. 1.3 Energy band diagram of the MOS cross section with interface traps, and trap-dependent transfer *curves*

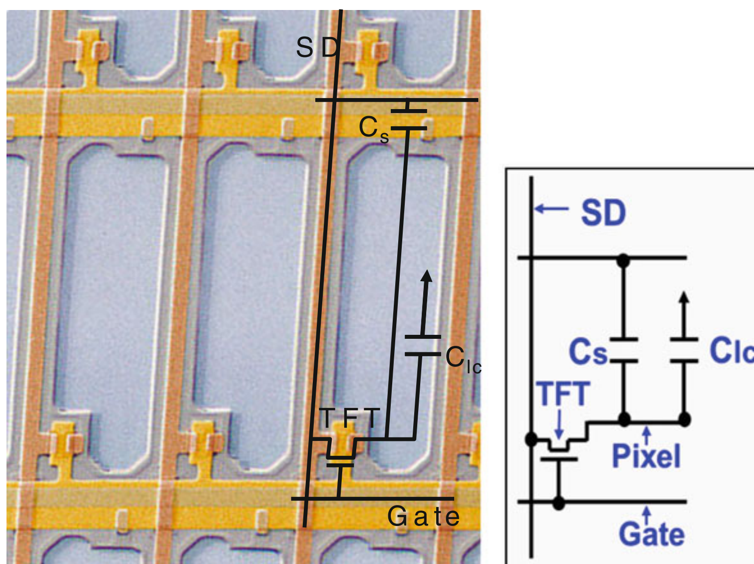

Fig. 1.4 Active matrix TFT pixel, circuit (*SD* source/drain, *Clc* LC capacitor), and backplane array scheme

1.2.3 Subthreshold Swing (SS) and Trap-Dependent I_D–V_G Transfer Curves

The transfer curve shape (the slope in the curves of Fig. 1.3) may depend upon the interface states (trap density at/near interface between gate insulator and channel) of a thin-film device, reflecting the density of the interfacial traps. It means, in fact, that the sub-threshold stage behavior in the curves may give a valuable insight, since the channel accumulation by mobile charge initially goes through the stage when the interfacial and near-interface traps are initially filled with the mobile charges under the V_G increase. According to the source-channel-drain band diagram of Fig. 1.5, with the (+) V_G increase the Fermi energy level at the channel/dielectric interface of n-channel TFT increases to fill the interfacial traps with electrons and eventually to overcome the conduction band minimum. (Note more bending in channel band.) When sufficient accumulation is obtained, those accumulated mobile electron charges are drifted/transported to the drain electrode through the channel (starting from the source). The sub-threshold behavior is well known as subthreshold swing (*SS*), of which the unit is Volt/dec, and the value must be small if the trap density is low and thus rapidly filled, leading to a steep curve shape. In contrast, if the trap density is large, SS is slow because more gate

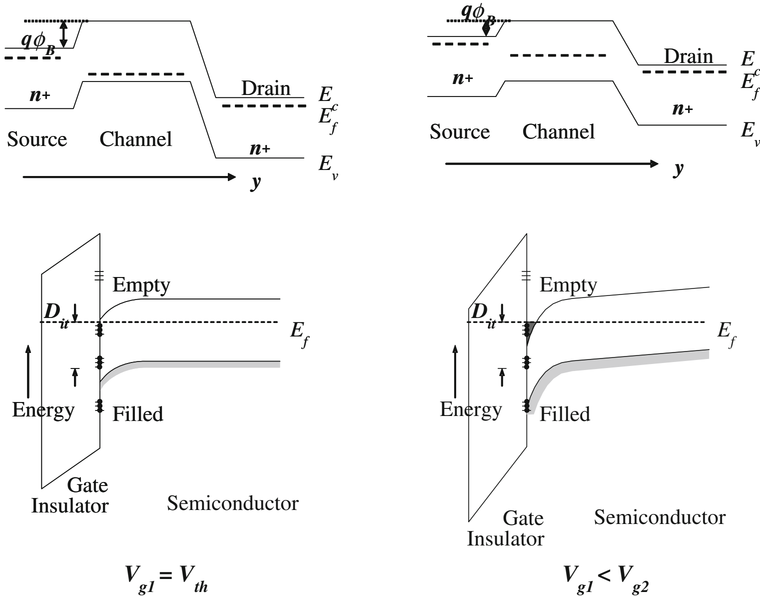

Fig. 1.5 Energy band diagram at the channel/dielectric interface illustrating the source-channel-drain sub-threshold ($V_{G1} = V_{th\text{-}sub}$) and accumulation ($V_{G2} > V_{th}$) stage schemes. With $+V_G$ increase, the barrier $q\phi_B$ between the source and channel decreases while the dielectric/channel interface traps are filled

voltage is needed to get sufficient accumulation for channel. The following equation presents the *SS* in more details [14, 15].[1]

$$SS = \log(kT/q) \cdot \left[1 + \left(\varepsilon_{ch}/L_D + q^2 \cdot D_{it}\right)/C_{ox}\right]$$
$$= \log(kT/q) \cdot \left[1 + q \cdot x_{ox}\left(\sqrt{(\varepsilon_{ch} \cdot N_{bt}/kT)} + q \cdot D_{it}\right)/\varepsilon_{ox}\right], \quad (1.10)$$

where $kT = 0.026$ eV at room temperature, ε_{ch} and C_{ox} are respectively the dielectric constants of channel semiconductor and the electric capacitance of dielectrics, N_{bt} and D_{it} are respectively the near-interface-bulk trap density and the interface trap density-of-states (DOS) at the channel/dielectric interface as energy-independent average values; their units are cm^{-3} and cm^{-2} eV^{-1}, respectively. Q_{eff} (of Eq. 1.9) is related to D_{it} and also probably to N_{bt} in Eq. 1.10 as the charge density near the interface. In Eq. 1.10 the second term within the large parenthesis only exists for FETs operating in accumulation mode, derivable to be from $(\varepsilon_{ch}/L_D)/C_{ox}$ and a Poisson's electrostatic equation to express the charging (filling) of near-interface traps; it thus includes the Debye length ($L_D \sim 2$ nm in general). This second term is usually ignored in Si-based MOSFETs operating in inversion mode. The third term with D_{it} presents the charging of only interface traps, considered important for both inversion and accumulation mode transistors. Still, there is more kept in mind; contact resistance and parasitic resistance in staggered type TFTs can influence I_D and thus apparent *SS* value as well. So, above Eq. (1.10) is essentially theoretical, only considering the events at/near the channel/dielectric interface area.

1.3 Stability Issues: Hysteresis by Gate Voltage Sweep

1.3.1 Shallow Level Traps versus Injection from Gate Electrode to Gate Insulator

If the dielectric/channel interface contains shallow traps, trapped mobile charges would be de-trapped or released to join the drain current under a gate bias which has the same polarity as that of trapped charges, while they would be trapped again under the other bias polarity opposite to the charges. If the interface already has negative traps filled with electrons, the channel of p-type TFT can easily be accumulated with holes under a smaller value of (–) V_G, but as the next step of V_G sweep, the trapped electrons would be ejected/de-trapped from the interface by a large value of (−) gate bias; then hole accumulation is not easy, requiring higher (−) V_G. Figure 1.6 displays such interface-trap-induced hysteresis as observed

[1] [14, 15] See J. Electrochem. Soc. 140, 3679–3683 (1993) and R. S. Muller, T. I. Kamins, M. Chan, *Device Electronics for Integrated Circuits*, 3rd edn. (Wiley, New York, 2003), pp. 443–444, 405–409, 397. for more details.

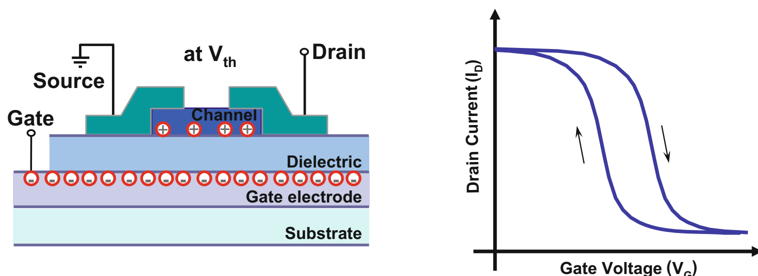

Fig. 1.6 Schematics on interface-trap-induced hysteresis in a p-channel pentacene TFT

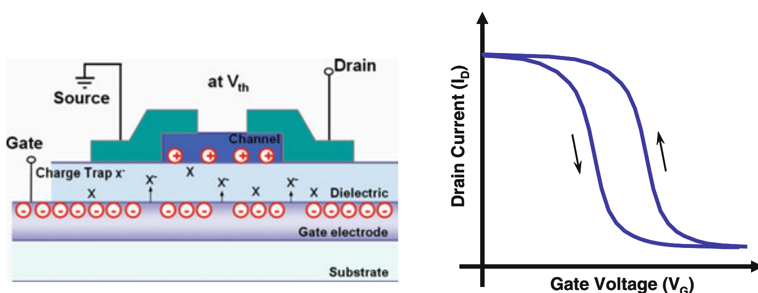

Fig. 1.7 Schematics on gate-injection-induced hysteresis in a p-channel pentacene TFT

from p-channel organic TFTs. Positive (+) V_G induces electrons to be trapped at the interface so that the threshold voltage gets small in the first V_G sweep, but in the second sweep coming from (−) V_G V_{th} became larger [16].

Similar but opposite-direction hysteresis could be found with V_G sweep, caused by charge injection from the gate electrode to the dielectric insulator. This is the case that the interface has a relatively small density of shallow traps while the dielectric of the TFT may be weak enough to allow charge injection from the gate electrode. The injected charges are electrons (for instance, p-channel transistor) under (−) V_G in general, then hole accumulation in the channel becomes easier than without the injection, leading to a smaller V_{th}. The injected electrons are actually embedded in the insulator, but normally ejected back to the gate electrode under a positive (+) bias, making the V_{th} move back to its original value. The hysteresis cycle is thus exactly opposite to the interface-trap-induced event. The hysteresis of Fig. 1.7 shows such gate-injection effects in p-channel pentacene TFT with organic dielectrics. It is worthy of note that the hysteresis direction is quite opposite to that of Fig. 1.6 [17].

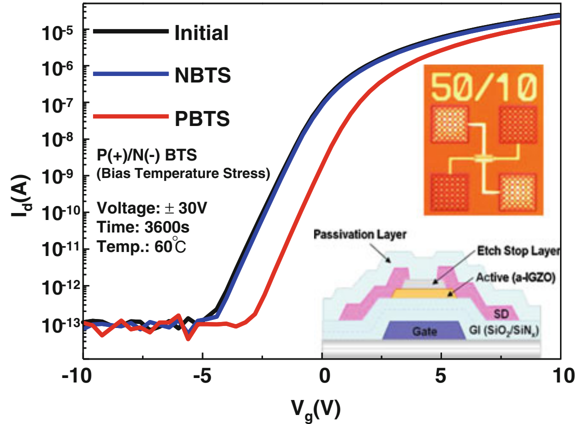

Fig. 1.8 Positive and negative BTS (PBTS and NBTS) results obtained from an InGaZnO TFT. Only the positive BTS shows a noticeable V_{th} shift

1.4 Stability Issues: Bias-Temperature-Stress

The V_{th} shift can also take place in a working TFT device during operation, since the device is either under a constant positive gate bias (for ON state) or under a negative gate bias (for OFF state) at a certain temperature above room temperature. If V_{th} moves with the gate bias, ON and OFF behavior could be unpredictable or irregular, and as a result, the devices become unusable. These were the main problems of previous CdS, CdTe, and CdSe-based TFTs in earlier days. The main reason for the V_{th} shift is probably that the deep- and shallow-level traps become active at the dielectric/channel interface where mobile charges are trapped during operation under constant gate voltage [18–21]. In order to assess the V_{th} shift behavior in a practical way, bias-temperature-stress (BTS) tests were developed in the industry. An elevated operational temperature of 60 ^{o} C has been used for the test along with an operation gate bias (± 10–20 V) for ON/OFF switching (in n-channel TFTs). The transfer curves of Fig. 1.8 shows the positive and negative BTS effects on an InGaZnO TFT as taken during various periods. Positive BTS leads to a small voltage shift while negative BTS hardly contributes to any shift in the dark, indicating that many of electron (negative) traps are present at/near the interface in the n-channel TFT [22].

1.5 Stability Issues: Photostability

The interface-trapped charges can be released by gate voltage stress but deep level traps may not release their charges. Those deep level-trapped charges are released or de-trapped only by high energy photons. If such deep charges are in high density at the interfaces or at the bulk near the interface, devices cannot be stable under visible photons. All LCDs using amorphous-Si TFT drivers adopt opaque metal gate electrode to block the back light [23, 24].

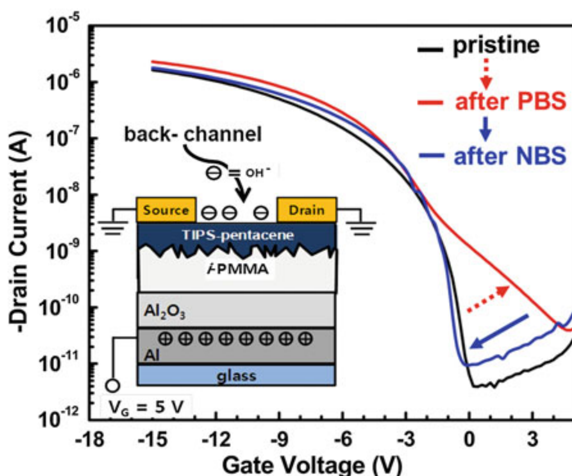

Fig. 1.9 Transfer *curves* after 5000 s-long positive bias-stress (PBS) on TIPS-pentacene p-channel TFT with a passivation layer. OFF-I_D increases along with a S.S. degradation under PBS which would attract water molecules and OH- hydroxyl groups on the device surface, providing back-channel hole current even in the off-state. Interestingly, such back-channel effects vanish with NBS, probably because negative gate bias would eject the negatively-charged molecules from the surface

1.6 Stability Issues: Back Channel Current

All staggered type TFTs (Fig. 1.1) tend to have a parasitic back channel path between source and drain, as well as the front channel. Under a negative BTS in n-channel or a positive BTS in p-channel devices, such back-channel effects may appear as an indicator of a degradation of S.S. and OFF-current increase. Figure 1.9 shows the transfer curves of a p-channel organic TFT right after stressed under long term positive BS. It suggests that any bottom gate TFTs need a passivation layer on the top of the devices, which will protect against or reduce ambient molecules-influenced current occurring at the device top surface, the source of the back channel [25].

1.7 Importance of Dielectric/Channel Interface Trap States

TFT devices have four parameters representing their performance in general: field-effect mobility, ON/OFF ratio, threshold voltage, and S.S., all of which are influenced by channel/dielectric interface traps. High-density trap states would reduce the mobility and ON/OFF ratio while they would lead to some fluctuation

Table 1.1 Controlling factors for TFT performance show the importance of channel/dielectric interface traps or traps near the interface

TFT performance	Control factor
Field-effect mobility	• Channel/dielectric interface trap states • Interface Morphology
Threshold voltage	• Channel/dielectric interface trap states • Gate metal vs. channel semiconductor work function difference
On & Off–current	• W/L ratio • Drift mobility • Interface trap states & roughness • Source/drain Ohmic contact
Sub-threshold swing (S.S.)	• Channel/dielectric interface trap state • Channel bulk trap states near the interface • Dielectric capacitance

in threshold voltage, degrading S.S. Hence, any quantitative analysis of the trap density-of-states (DOS) is very important for a working TFT device, even though the device already exhibits apparently high field-effect mobility (See Table 1.1).

1.8 Previous Interface Trap Measurements

DLTS: A representative previous method is deep level transient spectroscopy (DLTS), which is known to use thermal energy to release the trapped charges. However, this technique utilizes a Schottky or p-n diode and MOS-capacitor structures rather than a working TFT device. Moreover, thermal energy cannot release ultra deep-level charges, since increasing the temperature has a practical limit. So, its use has been limited to Si-based test devices, with quite a low energy resolution [26].

CMS: Charge modulated spectroscopy (CMS) is a recently introduced method that generally operates on a working organic TFT devices. CMS uses photons under long term gate bias (for accumulation mode). The advantage of CMS lies in the fact that it uses a working device and signal energy resolution is quite good, however disadvantages of CMS are several, since it takes a very long term under the gate bias to obtain a substantial signal from the interface-trapped and accumulated charges near the interface. More details are found elsewhere [27].

1.9 Photo-Excited Charge-Collection Spectroscopy (PECCS)

Photo-excited trap-charge-collection spectroscopy (PECCS) utilizes the photo-induced threshold voltage (V_{th}) response of a working TFT device as a direct probe of the interfacial traps. Interface charges trapped at a certain energy level are liberated by the energetic photons and then electrically collected at the source/drain (S/D) electrodes. During this photo-electric process V_{th} or the onset voltage of TFTs is shifted. The magnitude of the threshold voltage shift (ΔV_{th}) provides us with a direct measure of the density-of-charge traps while the energy levels of those traps are simply scanned over by the photon energy. As a consequence, we can sensitively probe the fine density-of-states (DOS) profiles for detailed mid-gap states in the channel/dielectric interface of a working TFT device whether it has inorganic, organic, or even nano structure channel. For the photo-electric measurement, we sequentially apply mono-energetic photons onto our TFT device from low to high energy, to release the trapped charges at the channel/dielectric interface in the order from shallow- to deep-levels. Fig. 1.10a and b display the

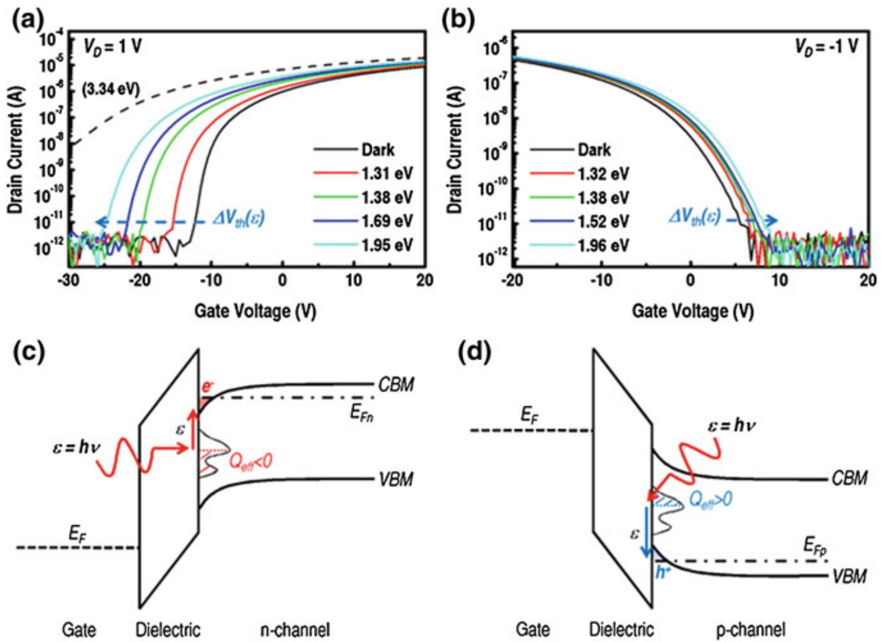

Fig. 1.10 Static photo-induced transfer curves obtained from (**a**) a transparent n-channel TFT and (**b**) a p-channel TFT under energetic photon beams. Energy band diagrams which elucidate the photo-excitation of (**c**) electron-trap charges in an n-channel TFT and that of (**d**) hole-trap charges in a p-channel TFT. Those excited charge carriers contribute to the abrupt shift of V_{th} in the TFT devices. The red and blue shades represent remaining electron and hole charges trapped at the respective interfaces

respective photo-induced transfer characteristics of n- and p-channel TFTs, to which a very low V_D of 1 V was applied, so that the photo-charge collection proceeds in a very linear regime, not in the saturation (to remove any probable measurement error by a large drain electric field which may excite some charges in bulk traps). Gate bias sweep started from the channel accumulation state because we should initially fill up all the interface trap states with charge carriers prior to the photo-excitation process. If the TFT has an n-channel, the trap states are to be initially filled with electrons (Fig. 1.10c), but if it is a p-channel TFT, the traps would be filled with holes and/or most of the electrons in the traps will be evacuated (Fig. 1.10d). When the photo-excitation initiates, the trapped charge carriers are released into the band edges as indicated by the arrows. As shown in Fig. 1.10a and b, ΔV_{th} as a function of photon energy was clearly observed in both the n- and p-channel TFTs while no significant changes in the sub-threshold slope (SS), field-effect mobility (μ_{FET}), and off-state drain current (I_{off}) values were observed. These photo-induced ΔV_{th} can be explained by electron transitions from electron-trap charge states (e.g. deep acceptor or deep donor in the accumulation state) to the conduction band minimum (CBM) in the case of n-channel TFT (Fig. 1.10c) and by hole transitions from its hole-trap charge states to the valence band maximum (VBM) in the other case of p-channel TFT (Fig. 1.10d). When photons with a specific energy, ε, illuminate through the thin channel to reach the channel/dielectric interface of a TFT, most of the trap charges (electrons) in the gap states between CBM–ε and CBM are excited to the CBM level in the n-channel TFT, since the number of incident photons (order of $\sim 10^{15}$ cm^{-2}) is large compared to that of trap states, which is far smaller (order of 10^{12}–10^{13} cm^{-2}). Likewise most of the trapped holes in the gap states between VBM and VBM + ε are excited to VBM level in the p-channel TFT. This means that the effective trap charge (Q_{eff}), which is mainly for the traps remaining at the channel/dielectric interface, can be varied with photon energy ε, and then the photo-shifted V_{th} can be represented by

$$V_{th}(\varepsilon) = \phi_{ms} - \frac{Q_{eff}(\varepsilon)}{C_{ox}} + \Psi_{s,\max} + \frac{Q_G}{C_{ox}}. \tag{1.11}$$

where

$$\begin{aligned} Q_{eff}(\varepsilon) &= q\int_{VBM}^{CBM-\varepsilon} D_{it,e}(E)F(E)dE + qN_b t_{ox} = q\int_{VBM}^{CBM-\varepsilon} D_{it,e}(E)dE + qN_b t_{ox} \quad for\ \ n-channel \\ & q\int_{CBM}^{VBM+\varepsilon} D_{it,h}(E)\{1-F(E)\}dE + qN_b t_{ox} = q\int_{CBM}^{VBM+\varepsilon} D_{it,h}(E)dE + qN_b t_{ox} \quad for\ \ p-channel \end{aligned} \tag{1.12}$$

and ϕ_{ms} is the metal–semiconductor work function difference, C_{ox} is the dielectric capacitance per unit area (F·cm^{-2}), $\psi_{s,max}$ is the potential due to band bending of the channel semiconductor, Q_G is the charge associated with dielectric band

bending induced by gate bias, N_b is the density (cm^{-3}) of bulk traps in the gate dielectric, t_{ox} is the dielectric thickness (nm), $D_{it,e}$ is the DOS of electron traps at the n-channel/dielectric interface, $D_{it,h}$ is the DOS of hole traps at the p-channel/dielectric interface ($cm^{-2}eV^{-1}$), and *F(E)* is the Fermi–Dirac distribution function whose value must be 1 for n-channel and 0 for p-channel (see the Fermi levels of n-channel (E_{fn}) and p-channel (E_{fp}) in Fig. 1.10c and d). (We assumed 0 Kelvin step function for considering *F(E)* in Eq. (1.12)). Since ϕ_{ms}, $\psi_{s,max}$, and Q_G in Eq. (1.11) are rarely changed by ε, and since N_b in Eq. (1.12) also hardly varies with ε, photo-induced ΔV_{th} can be analyzed by taking a derivative of Eq. (1.11) with ε, as shown below,

$$\frac{\partial V_{th}(\varepsilon)}{\partial\varepsilon} = -\frac{1}{C_{ox}}\frac{\partial Q_{eff}(\varepsilon)}{\partial\varepsilon} \tag{1.13}$$

and then by substituting Eq. (1.12) into Eq. (1.13), which now results in

$$\begin{aligned}\frac{\partial V_{th}(\varepsilon)}{\partial\varepsilon} &= \frac{q}{C_{ox}}\left\{D_{it,\,e}(CBM-\varepsilon)\right\} \quad with \quad for\;\; n-channel \\ &= -\frac{q}{C_{ox}}\left\{D_{it,\,h}(VBM+\varepsilon)\right\} \quad with \quad for\;\; p-channel\end{aligned} \tag{1.14}$$

If the bulk-trap densities in the both channel and dielectric oxide are negligible, $D_{it,\ e}$ (*CBM*−ε) and $D_{it,\ h}$ (*VBM* + ε) are determined, to be

$$\begin{aligned}D_{it,e}(CBM-\varepsilon) &= \frac{C_{ox}}{q}\frac{\partial V_{th}(\varepsilon)}{\partial\varepsilon} \quad for\;\; n-channel \\ D_{it,h}(VBM+\varepsilon) &= -\frac{C_{ox}}{q}\frac{\partial V_{th}(\varepsilon)}{\partial\varepsilon} \quad for\;\; p-channel,\end{aligned} \tag{1.15}$$

where $D_{it,\ e}$ (*CBM*-ε) and $D_{it,\ h}$ (*VBM* + ε) are the DOS ($cm^{-2}eV^{-1}$) with respect to CBM and VBM for n-channel and p-channel, respectively. Above equations from (1.13) to (1.15) shows how we can eventually extract the information on $\Delta Q_{eff}(\varepsilon)$ and DOS, which is not much difficult because ΔV_{th} (ε) with respect to ε is easily achievable from photo-induced transfer curves (experimental section shows more details). According to the Eq. (1.15) it is worth while to note that if $\partial V_{th}/\partial\varepsilon < 0$ for n-channel (negative V_{th} shift) and $\partial V_{th}/\partial\varepsilon > 0$ for p-channel (positive V_{th} shift) with electronic charge ($q < 0$), the DOS values are always positive regardless of the channel type. It should be again considered that this D_{it} measurement by photo-induced ΔV_{th} with $\Delta\varepsilon$ is only valid in the case without high bulk trap density but in fact with interface trap densities. If our oxide and organic devices respectively with 20- and 50 nm-thick channels show quite a density of bulk traps, their *SS*, μ_{FET}, and I_{off} values should also change because an effective channel layer thickness is at most 5 nm (Debye length) from the interface. However, little change in those experimental factors was observed and now this confirms that our interfacial DOS estimation is valid. If the I_{off} level of given TFT

somewhat increases under photons, the DOS for its interface traps would not be easily distinguished from that of bulk traps [28–30].

1.10 Chapter Summary

TFTs and field-effect transistors have four important performance parameters, which are always influenced by the insulator dielectric/semiconductor channel interface. The electronic, chemical, and physical states of the interface may control the field effect mobility and off-state current etc. due to deep and shallow level traps at/near the interface. Quantitative characterization of such interfacial trap states is not a trivial matter at all, since it should be done with a working TFT/FET. Hence, we suggest the use of PECCS, which accounts for both TFT device physics and interface trap DOS in more or less quantitative ways.

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