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Photo-Excited Charge Collection Spectroscopy

Probing the Traps in Field-Effect Transistors

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To the Lord Jesus and my wife Jihye

Seongil Im, 2013–01–10

Preface

Solid-state field-effect devices such as organic and inorganic-channel thin-film transistors (TFTs) have been expected to promote advances in display electronics based on low cost, high transparency, and flexibility. The operational stabilities of such TFTs are thus important, strongly depending on the nature and density of charge traps present at the channel/dielectric interface or in the thin-film channel itself. In particular, the illuminated display back panel is susceptible to the charge-trap-induced instability. As conventional tests for the device instabilities, gate-bias stress techniques are adopted in general, however, those appear limited in providing any satisfying information.

This book contains how to characterize these traps, starting from the device physics of field-effect transistor (FET). Unlike conventional analysis techniques which are away from well-resolving spectral results, newly introduced photo-excited charge-collection spectroscopy (PECCS) utilizes the photo-induced threshold voltage (V_{th}) response from any type of working transistor devices with organic-, inorganic-, and even nanochannels, directly probing on the traps. So, our technique PECCS has been discussed through more than ten refereed-journal papers in the fields of device electronics, applied physics, applied chemistry, nanodevices, and materials science, finally finding a need to be summarized with several chapters in a short book. In this book, Chap. 1 addresses the device physics of FET and the main principles of PECCS measurements, of which the detailed instrumentations are introduced in Chap. 2. From Chaps. 3 to 5 we address the applications of PECCS on organic, oxide, and nanostructure-based FETs while in the last Chap. 6 we discuss some weakness of PECCS and summarize the whole chapters as well. In the book, we distinguished the term TFT from FET, which may be a more extensive term including TFT, since we treated both thin-films and nanowires/or nanosheets for transistor fabrications and measurements.

Besides the coauthors, I acknowledge Dr. Kimoon Lee, presently at Tokyo Institute of Technology for his innovative initiations on PECCS, my graduate student Syed Raza Ali for the PECCS characterizations on ZnO nanowire-based field-effect transistors, Dr. Do Kyung Hwang, Dr. Ji Hoon Park, and Dr. Jiyoul Lee for the supports with their organic field-effect transistors, Dr. Jeong-Min Choi in Korean Intellectual Property Office for Patent examining.

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Chapter 1
Device Stability and Photo-Excited Charge-Collection Spectroscopy

Abstract Important performance factors and basic device physics of organic or inorganic-channel thin-film transistors (TFTs) are addressed before introducing the photo-excited charge collection spectroscopy (PECCS), so that systematic and in-depth understanding on the device stability issues may be naturally drawn in focus. Device architecture, device physics, and general stability issues in TFT (or field-effect transistor) are thus introduced in the initial sections, and in the last section our photon-probing technique is explained along with its own device physics.

1.1 Thin-Film Transistor Architectures for Photon Probe Measurements

In general, there are four types of thin-film transistor (TFT) architectures: staggered, inverted staggered, coplanar, and inverted coplanar [1–4]. As shown below in Fig. 1.1, bottom gate TFTs with inverted staggered or inverted coplanar types are quite manageable for the photon probe measurements since they already have transparent windows above active semiconductor channels. In contrast, the top gate devices such as staggered or coplanar type need transparent gate electrodes for the photon measurements. In our experimentations of the following chapters, we usually take the inverted staggered type for bottom gate and the staggered type for top gate devices.

1.2 Device Physics and Equations for Thin-Film Transistors

1.2.1 Gradual Channel Approximation

As in the case of Metal–Oxide–Semiconductor Field-Effect Transistors (MOSFETs), TFTs have two different operational regimes depending on the drain voltage: linear

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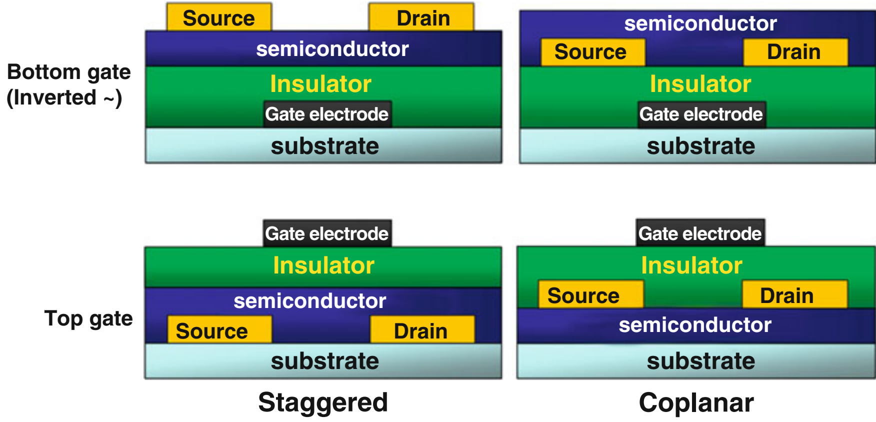

Fig. 1.1 The four types of TFT in device architectures: top gate and bottom gate (Inverted) types for staggered or coplanar TFTs

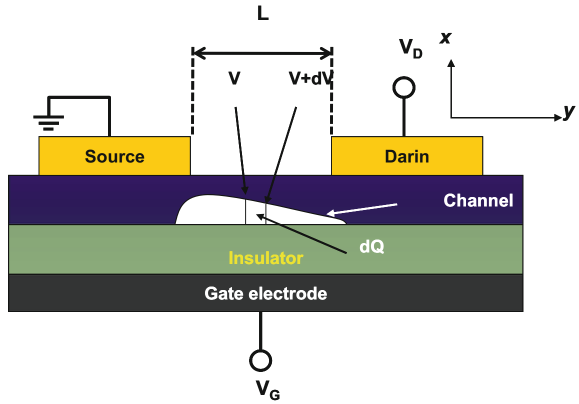

Fig. 1.2 Cross sectional view illustrating the gradual channel model

and saturation. A gradual channel approximation is assumed for the TFT channel, where y is the source-to-drain direction while z is the channel thickness direction perpendicular to the channel. The carrier density per unit area in the channel is the function of y-direction potential V_y caused by drain bias V_D. We illustrate the cross section of an inverted stagger type bottom gate TFT in Fig. 1.2 [5–7].

When the gate potential/voltage V_G overcomes the threshold voltage V_{th}, the accumulated mobile charge density Q_z is presented as the function of V_y and V_G in the following the formula

$$Q_z(y) = C_{ox}\left(V_G - V_{th} - V_y\right), \tag{1.1}$$

where C_{ox} is the capacitance per unit area of gate insulator (GI). Since the accumulated mobile charges are composed of majority carriers at/near the

channel/dielectric (or GI) interface, the drain current I_D comes out from the following equations,

$$J_n = I_D/(W \cdot Z) = nq\mu E_y = nQ_z(dV_y/dy)/Z, \tag{1.2}$$

where J_n is the current density, W is the channel width, Z is the channel thickness as a function of V_y and V_G, E_y is the electric-field (E-field) between source and drain, μ is the average carrier mobility (field-effect mobility), and n is the average carrier concentration in the channel as a function of V_G. Now, $Q_z(y)$ is presented to be nqZ as the function of V_y (at a certain y position) under a fixed value of V_G. Therefore, the drain current I_D is defined at a certain V_G as below.

$$I_D = W\mu Q_z(dV_y/dy), \tag{1.3}$$

$$I_D dy = W\mu Q_Z(dV_y) = W\mu Q_z(C_{ox}(V_G - V_{th} - V_y))dV_y \tag{1.4}$$

Since V_{th} and V_G are constant values, we can extract the I_D from Eq. (1.4) by integrating the equation over the channel length range ($0 \sim L$) which is corresponding to the respective voltage range from 0 to V_D, the drain voltage. As results, we obtain the following well-known equation,

$$I_D = \mu \cdot C_{ox}(W/L)\left[(V_G - V_{th})V_D - (1/2)V_D^2\right] \tag{1.5}$$

In the linear regime, $V_D \ll V_G - V_{th}$ so that I_D can be expressed as below using μ_{Lin}, the linear mobility.

$$I_D = \mu_{Lin} \cdot C_{ox}(W/L)[(V_G - V_{th})V_D] \tag{1.6}$$

The gate field-induced carriers are quickly depleted to the drain electrode as the V_D increases, and eventually when V_D comes across the condition of $V_D = V_G - V_{th}$, the carrier channel becomes completely pinched-off at a ceratin V_D causing the I_D saturation. Then, for the condition of $V_D > V_G - V_{th}$, Eq. (1.5) is no longer valid. Instead, we generally use an empirical equation below,

$$I_D = \mu_{Sat} \cdot C_{ox}(W/2L)(V_G - V_{th})^2, \tag{1.7}$$

which uses the saturation mobility, μ_{Sat}. Besides such a deviation from simple gradual channel approximation in the saturation regime, contact resistance in the source/drain and V_G-dependent mobility can also influence the I_D behavior in TFTs.

1.2.2 V_{th} Equation and Related Physics

The threshold voltage (V_{th}; practical turn-on voltage) and μ_{Sat} are experimentally extracted from the I_D-V_G transfer curve characterizations following Eq. (1.7) and experimentations on TFTs. However, device physics of a TFT expects a theoretical equation, too, similar to the case of MOSFET [8–10].

$$V_{th} = \phi_{ms} - \frac{Q_{eff}}{C_{ox}} + \Psi_{s,\max} + \frac{Q_G}{C_{ox}} \tag{1.8}$$

With

$$\begin{aligned} Q_{eff} = & q \int_{VBM}^{CBM} D_{it,e}(E)F(E)dE, \ for \quad n-channel, \\ & q \int_{CBM}^{VBM} D_{it,h}(E)\{1-F(E)\}dE, \ for \quad p-channel \end{aligned} \tag{1.9}$$

where the effective trap charge (Q_{eff}) is mainly for the traps located at the channel/dielectric interface, ϕ_{ms} is the metal–semiconductor work function difference, C_{ox} is the dielectric capacitance per unit area (F·cm^{-2}), $\psi_{s,max}$ is the potential due to a band bending of the channel semiconductor, Q_G is the charge associated with a dielectric band bending as induced by gate bias, N_b is the density (cm^{-3}) of bulk traps in the gate dielectric, t_{ox} is the dielectric thickness (nm), $D_{it,\ e}$ is the DOS of electron traps at the n-channel/dielectric interface, $D_{it,\ h}$ is the DOS of hole traps at the p-channel/dielectric interface (cm^{-2}eV^{-1}), and *F(E)* is the Fermi–Dirac distribution function whose value must be 1 for n-channel and 0 for p-channel. The first and second terms on the left-hand side of Eq. (1.8) is the same as the flat band voltage (V_{FB}) of a transistor [11].

In view of the threshold voltage Eq. (1.8), the most important and changeable factor is probably Q_{eff} which is located at/or very near the interface between dielectric and semiconductor channel, since the effective charge could be large or small depending on the interface state which always consists of such a variety of hetero-systems as organic/inorganic, organic/organic, and sometimes inorganic/inorganic. Hence, minimizing or controlling Q_{eff} in an appropriate way has been quite an important issue in TFT history, which actually began with a crystalline CdS or CdSe channel in the 1960s, rather than with an amorphous Si channel. Even though the crystalline CdS TFTs demonstrated field effect mobilities of over 150 cm^2/V s, time- and temperature-dependent performance changes (mobility and V_{th}) made those devices ineffective, and the hope rolled over to amorphous-Si channel TFTs in the 1970–1980 with the advent of liquid crystal display (LCD) composed of TFT, storage capacitor, and LC pixel came [12, 13]. The schematic band diagram and I_D-V_G transfer curves in Fig. 1.3 illustrates the interfacial states which trap mobile charges to change V_{th} or the flat band voltage (V_{FB}) of device, while Fig. 1.4 shows a modern electrically stable active matrix TFT pixel composed with amorphous-Si TFT and dielectric storage capacitor (Cs), along with its circuitry [5, 14].

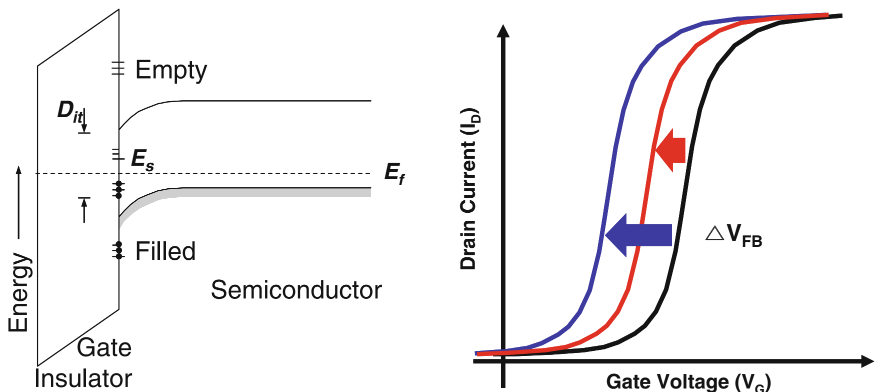

Fig. 1.3 Energy band diagram of the MOS cross section with interface traps, and trap-dependent transfer *curves*

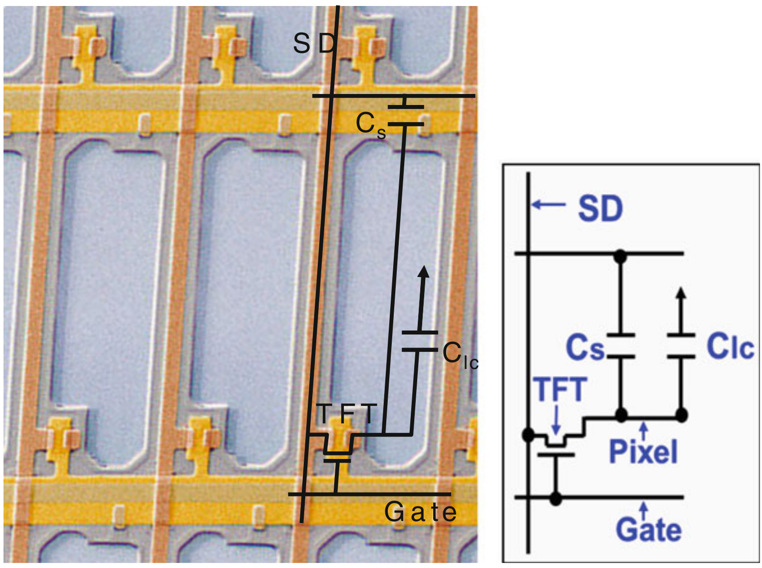

Fig. 1.4 Active matrix TFT pixel, circuit (*SD* source/drain, *Clc* LC capacitor), and backplane array scheme

1.2.3 Subthreshold Swing (SS) and Trap-Dependent I_D–V_G Transfer Curves

The transfer curve shape (the slope in the curves of Fig. 1.3) may depend upon the interface states (trap density at/near interface between gate insulator and channel) of a thin-film device, reflecting the density of the interfacial traps. It means, in fact, that the sub-threshold stage behavior in the curves may give a valuable insight, since the channel accumulation by mobile charge initially goes through the stage when the interfacial and near-interface traps are initially filled with the mobile charges under the V_G increase. According to the source-channel-drain band diagram of Fig. 1.5, with the (+) V_G increase the Fermi energy level at the channel/dielectric interface of n-channel TFT increases to fill the interfacial traps with electrons and eventually to overcome the conduction band minimum. (Note more bending in channel band.) When sufficient accumulation is obtained, those accumulated mobile electron charges are drifted/transported to the drain electrode through the channel (starting from the source). The sub-threshold behavior is well known as subthreshold swing (*SS*), of which the unit is Volt/dec, and the value must be small if the trap density is low and thus rapidly filled, leading to a steep curve shape. In contrast, if the trap density is large, SS is slow because more gate

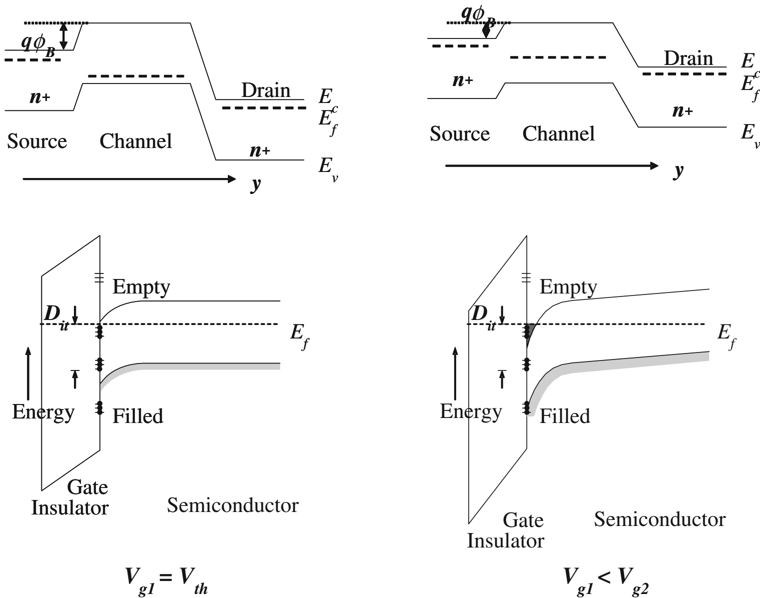

Fig. 1.5 Energy band diagram at the channel/dielectric interface illustrating the source-channel-drain sub-threshold ($V_{G1} = V_{th\text{-}sub}$) and accumulation ($V_{G2} > V_{th}$) stage schemes. With $+V_G$ increase, the barrier $q\phi_B$ between the source and channel decreases while the dielectric/channel interface traps are filled

voltage is needed to get sufficient accumulation for channel. The following equation presents the SS in more details [14, 15].[1]

$$\begin{aligned} SS &= \log(kT/q) \cdot \left[1 + \left(\varepsilon_{ch}/L_D + q^2 \cdot D_{it}\right)/C_{ox}\right] \\ &= \log(kT/q) \cdot \left[1 + q \cdot x_{ox}\left(\sqrt{(\varepsilon_{ch} \cdot N_{bt}/kT)} + q \cdot D_{it}\right)/\varepsilon_{ox}\right], \end{aligned} \tag{1.10}$$

where $kT = 0.026$ eV at room temperature, ε_{ch} and C_{ox} are respectively the dielectric constants of channel semiconductor and the electric capacitance of dielectrics, N_{bt} and D_{it} are respectively the near-interface-bulk trap density and the interface trap density-of-states (DOS) at the channel/dielectric interface as energy-independent average values; their units are cm^{-3} and cm^{-2} eV^{-1}, respectively. Q_{eff} (of Eq. 1.9) is related to D_{it} and also probably to N_{bt} in Eq. 1.10 as the charge density near the interface. In Eq. 1.10 the second term within the large parenthesis only exists for FETs operating in accumulation mode, derivable to be from $(\varepsilon_{ch}/L_D)/C_{ox}$ and a Poisson's electrostatic equation to express the charging (filling) of near-interface traps; it thus includes the Debye length ($L_D \sim 2$ nm in general). This second term is usually ignored in Si-based MOSFETs operating in inversion mode. The third term with D_{it} presents the charging of only interface traps, considered important for both inversion and accumulation mode transistors. Still, there is more kept in mind; contact resistance and parasitic resistance in staggered type TFTs can influence I_D and thus apparent SS value as well. So, above Eq. (1.10) is essentially theoretical, only considering the events at/near the channel/dielectric interface area.

1.3 Stability Issues: Hysteresis by Gate Voltage Sweep

1.3.1 Shallow Level Traps versus Injection from Gate Electrode to Gate Insulator

If the dielectric/channel interface contains shallow traps, trapped mobile charges would be de-trapped or released to join the drain current under a gate bias which has the same polarity as that of trapped charges, while they would be trapped again under the other bias polarity opposite to the charges. If the interface already has negative traps filled with electrons, the channel of p-type TFT can easily be accumulated with holes under a smaller value of (–) V_G, but as the next step of V_G sweep, the trapped electrons would be ejected/de-trapped from the interface by a large value of (−) gate bias; then hole accumulation is not easy, requiring higher (−) V_G. Figure 1.6 displays such interface-trap-induced hysteresis as observed

[1] [14, 15] See J. Electrochem. Soc. 140, 3679–3683 (1993) and R. S. Muller, T. I. Kamins, M. Chan, *Device Electronics for Integrated Circuits*, 3rd edn. (Wiley, New York, 2003), pp. 443–444, 405–409, 397. for more details.

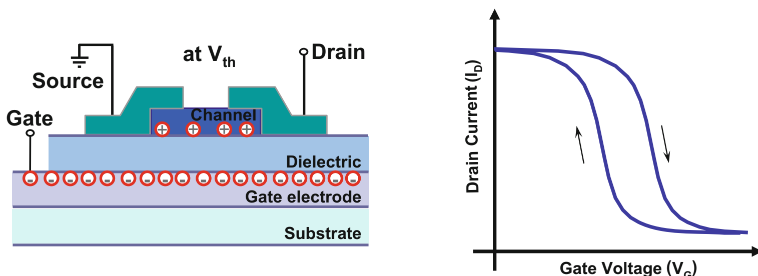

Fig. 1.6 Schematics on interface-trap-induced hysteresis in a p-channel pentacene TFT

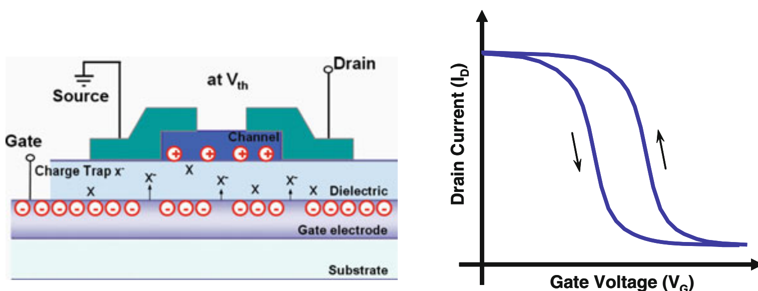

Fig. 1.7 Schematics on gate-injection-induced hysteresis in a p-channel pentacene TFT

from p-channel organic TFTs. Positive (+) V_G induces electrons to be trapped at the interface so that the threshold voltage gets small in the first V_G sweep, but in the second sweep coming from (−) V_G V_{th} became larger [16].

Similar but opposite-direction hysteresis could be found with V_G sweep, caused by charge injection from the gate electrode to the dielectric insulator. This is the case that the interface has a relatively small density of shallow traps while the dielectric of the TFT may be weak enough to allow charge injection from the gate electrode. The injected charges are electrons (for instance, p-channel transistor) under (−) V_G in general, then hole accumulation in the channel becomes easier than without the injection, leading to a smaller V_{th}. The injected electrons are actually embedded in the insulator, but normally ejected back to the gate electrode under a positive (+) bias, making the V_{th} move back to its original value. The hysteresis cycle is thus exactly opposite to the interface-trap-induced event. The hysteresis of Fig. 1.7 shows such gate-injection effects in p-channel pentacene TFT with organic dielectrics. It is worthy of note that the hysteresis direction is quite opposite to that of Fig. 1.6 [17].

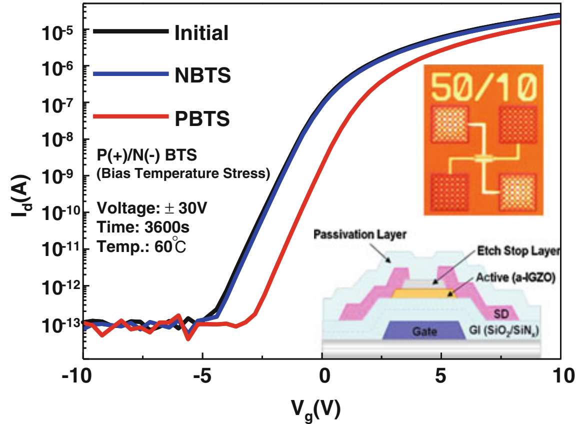

Fig. 1.8 Positive and negative BTS (PBTS and NBTS) results obtained from an InGaZnO TFT. Only the positive BTS shows a noticeable V_{th} shift

1.4 Stability Issues: Bias-Temperature-Stress

The V_{th} shift can also take place in a working TFT device during operation, since the device is either under a constant positive gate bias (for ON state) or under a negative gate bias (for OFF state) at a certain temperature above room temperature. If V_{th} moves with the gate bias, ON and OFF behavior could be unpredictable or irregular, and as a result, the devices become unusable. These were the main problems of previous CdS, CdTe, and CdSe-based TFTs in earlier days. The main reason for the V_{th} shift is probably that the deep- and shallow-level traps become active at the dielectric/channel interface where mobile charges are trapped during operation under constant gate voltage [18–21]. In order to assess the V_{th} shift behavior in a practical way, bias-temperature-stress (BTS) tests were developed in the industry. An elevated operational temperature of 60 ^{o} C has been used for the test along with an operation gate bias (± 10–20 V) for ON/OFF switching (in n-channel TFTs). The transfer curves of Fig. 1.8 shows the positive and negative BTS effects on an InGaZnO TFT as taken during various periods. Positive BTS leads to a small voltage shift while negative BTS hardly contributes to any shift in the dark, indicating that many of electron (negative) traps are present at/near the interface in the n-channel TFT [22].

1.5 Stability Issues: Photostability

The interface-trapped charges can be released by gate voltage stress but deep level traps may not release their charges. Those deep level-trapped charges are released or de-trapped only by high energy photons. If such deep charges are in high density at the interfaces or at the bulk near the interface, devices cannot be stable under visible photons. All LCDs using amorphous-Si TFT drivers adopt opaque metal gate electrode to block the back light [23, 24].

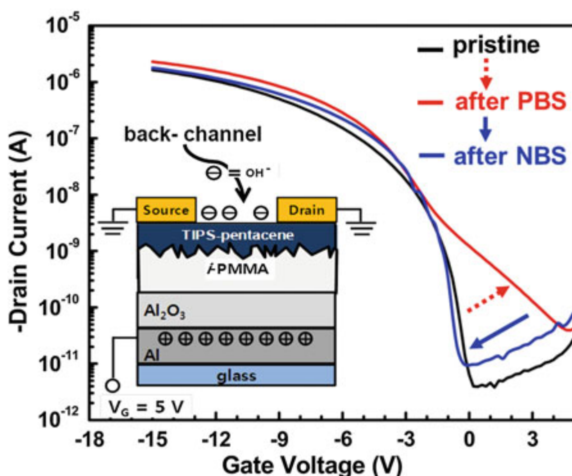

Fig. 1.9 Transfer *curves* after 5000 s-long positive bias-stress (PBS) on TIPS-pentacene p-channel TFT with a passivation layer. OFF-I_D increases along with a S.S. degradation under PBS which would attract water molecules and OH- hydroxyl groups on the device surface, providing back-channel hole current even in the off-state. Interestingly, such back-channel effects vanish with NBS, probably because negative gate bias would eject the negatively-charged molecules from the surface

1.6 Stability Issues: Back Channel Current

All staggered type TFTs (Fig. 1.1) tend to have a parasitic back channel path between source and drain, as well as the front channel. Under a negative BTS in n-channel or a positive BTS in p-channel devices, such back-channel effects may appear as an indicator of a degradation of S.S. and OFF-current increase. Figure 1.9 shows the transfer curves of a p-channel organic TFT right after stressed under long term positive BS. It suggests that any bottom gate TFTs need a passivation layer on the top of the devices, which will protect against or reduce ambient molecules-influenced current occurring at the device top surface, the source of the back channel [25].

1.7 Importance of Dielectric/Channel Interface Trap States

TFT devices have four parameters representing their performance in general: field-effect mobility, ON/OFF ratio, threshold voltage, and S.S., all of which are influenced by channel/dielectric interface traps. High-density trap states would reduce the mobility and ON/OFF ratio while they would lead to some fluctuation

Table 1.1 Controlling factors for TFT performance show the importance of channel/dielectric interface traps or traps near the interface

TFT performance	Control factor
Field-effect mobility	• Channel/dielectric interface trap states • Interface Morphology
Threshold voltage	• Channel/dielectric interface trap states • Gate metal vs. channel semiconductor work function difference
On & Off–current	• W/L ratio • Drift mobility • Interface trap states & roughness • Source/drain Ohmic contact
Sub-threshold swing (S.S.)	• Channel/dielectric interface trap state • Channel bulk trap states near the interface • Dielectric capacitance

in threshold voltage, degrading S.S. Hence, any quantitative analysis of the trap density-of-states (DOS) is very important for a working TFT device, even though the device already exhibits apparently high field-effect mobility (See Table 1.1).

1.8 Previous Interface Trap Measurements

DLTS: A representative previous method is deep level transient spectroscopy (DLTS), which is known to use thermal energy to release the trapped charges. However, this technique utilizes a Schottky or p-n diode and MOS-capacitor structures rather than a working TFT device. Moreover, thermal energy cannot release ultra deep-level charges, since increasing the temperature has a practical limit. So, its use has been limited to Si-based test devices, with quite a low energy resolution [26].

CMS: Charge modulated spectroscopy (CMS) is a recently introduced method that generally operates on a working organic TFT devices. CMS uses photons under long term gate bias (for accumulation mode). The advantage of CMS lies in the fact that it uses a working device and signal energy resolution is quite good, however disadvantages of CMS are several, since it takes a very long term under the gate bias to obtain a substantial signal from the interface-trapped and accumulated charges near the interface. More details are found elsewhere [27].

1.9 Photo-Excited Charge-Collection Spectroscopy (PECCS)

Photo-excited trap-charge-collection spectroscopy (PECCS) utilizes the photo-induced threshold voltage (V_{th}) response of a working TFT device as a direct probe of the interfacial traps. Interface charges trapped at a certain energy level are liberated by the energetic photons and then electrically collected at the source/drain (S/D) electrodes. During this photo-electric process V_{th} or the onset voltage of TFTs is shifted. The magnitude of the threshold voltage shift (ΔV_{th}) provides us with a direct measure of the density-of-charge traps while the energy levels of those traps are simply scanned over by the photon energy. As a consequence, we can sensitively probe the fine density-of-states (DOS) profiles for detailed mid-gap states in the channel/dielectric interface of a working TFT device whether it has inorganic, organic, or even nano structure channel. For the photo-electric measurement, we sequentially apply mono-energetic photons onto our TFT device from low to high energy, to release the trapped charges at the channel/dielectric interface in the order from shallow- to deep-levels. Fig. 1.10a and b display the

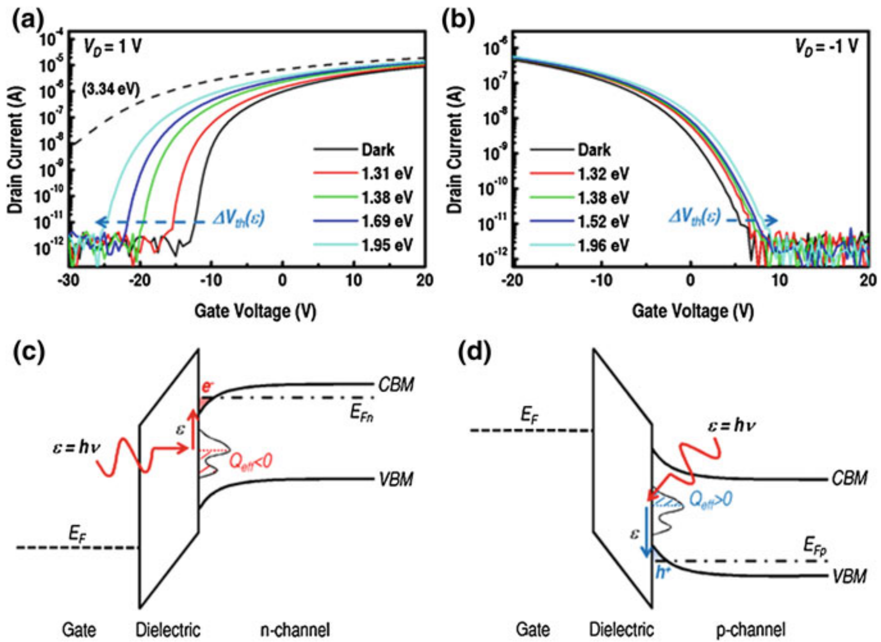

Fig. 1.10 Static photo-induced transfer curves obtained from (**a**) a transparent n-channel TFT and (**b**) a p-channel TFT under energetic photon beams. Energy band diagrams which elucidate the photo-excitation of (**c**) electron-trap charges in an n-channel TFT and that of (**d**) hole-trap charges in a p-channel TFT. Those excited charge carriers contribute to the abrupt shift of V_{th} in the TFT devices. The red and blue shades represent remaining electron and hole charges trapped at the respective interfaces

respective photo-induced transfer characteristics of n- and p-channel TFTs, to which a very low V_D of 1 V was applied, so that the photo-charge collection proceeds in a very linear regime, not in the saturation (to remove any probable measurement error by a large drain electric field which may excite some charges in bulk traps). Gate bias sweep started from the channel accumulation state because we should initially fill up all the interface trap states with charge carriers prior to the photo-excitation process. If the TFT has an n-channel, the trap states are to be initially filled with electrons (Fig. 1.10c), but if it is a p-channel TFT, the traps would be filled with holes and/or most of the electrons in the traps will be evacuated (Fig. 1.10d). When the photo-excitation initiates, the trapped charge carriers are released into the band edges as indicated by the arrows. As shown in Fig. 1.10a and b, ΔV_{th} as a function of photon energy was clearly observed in both the n- and p-channel TFTs while no significant changes in the sub-threshold slope (*SS*), field-effect mobility (μ_{FET}), and off-state drain current (I_{off}) values were observed. These photo-induced ΔV_{th} can be explained by electron transitions from electron-trap charge states (e.g. deep acceptor or deep donor in the accumulation state) to the conduction band minimum (CBM) in the case of n-channel TFT (Fig. 1.10c) and by hole transitions from its hole-trap charge states to the valence band maximum (VBM) in the other case of p-channel TFT (Fig. 1.10d). When photons with a specific energy, ε, illuminate through the thin channel to reach the channel/dielectric interface of a TFT, most of the trap charges (electrons) in the gap states between CBM–ε and CBM are excited to the CBM level in the n-channel TFT, since the number of incident photons (order of $\sim 10^{15}$ cm^{-2}) is large compared to that of trap states, which is far smaller (order of 10^{12}–10^{13} cm^{-2}). Likewise most of the trapped holes in the gap states between VBM and VBM + ε are excited to VBM level in the p-channel TFT. This means that the effective trap charge (Q_{eff}), which is mainly for the traps remaining at the channel/dielectric interface, can be varied with photon energy ε, and then the photo-shifted V_{th} can be represented by

$$V_{th}(\varepsilon) = \phi_{ms} - \frac{Q_{eff}(\varepsilon)}{C_{ox}} + \Psi_{s,\max} + \frac{Q_G}{C_{ox}}. \tag{1.11}$$

where

$$\begin{aligned} Q_{eff}(\varepsilon) &= q\int_{VBM}^{CBM-\varepsilon} D_{it,e}(E)F(E)dE + qN_b t_{ox} = q\int_{VBM}^{CBM-\varepsilon} D_{it,e}(E)dE + qN_b t_{ox} \quad for\ \ n-channel \\ & q\int_{CBM}^{VBM+\varepsilon} D_{it,h}(E)\{1-F(E)\}dE + qN_b t_{ox} = q\int_{CBM}^{VBM+\varepsilon} D_{it,h}(E)dE + qN_b t_{ox} \quad for\ \ p-channel \end{aligned} \tag{1.12}$$

and ϕ_{ms} is the metal–semiconductor work function difference, C_{ox} is the dielectric capacitance per unit area (F·cm^{-2}), $\psi_{s,max}$ is the potential due to band bending of the channel semiconductor, Q_G is the charge associated with dielectric band

bending induced by gate bias, N_b is the density (cm^{-3}) of bulk traps in the gate dielectric, t_{ox} is the dielectric thickness (nm), $D_{it,e}$ is the DOS of electron traps at the n-channel/dielectric interface, $D_{it,h}$ is the DOS of hole traps at the p-channel/dielectric interface (cm^{-2}eV^{-1}), and *F(E)* is the Fermi–Dirac distribution function whose value must be 1 for n-channel and 0 for p-channel (see the Fermi levels of n-channel (E_{fn}) and p-channel (E_{fp}) in Fig. 1.10c and d). (We assumed 0 Kelvin step function for considering *F(E)* in Eq. (1.12)). Since ϕ_{ms}, $\psi_{s,max}$, and Q_G in Eq. (1.11) are rarely changed by ε, and since N_b in Eq. (1.12) also hardly varies with ε, photo-induced ΔV_{th} can be analyzed by taking a derivative of Eq. (1.11) with ε, as shown below,

$$\frac{\partial V_{th}(\varepsilon)}{\partial \varepsilon} = -\frac{1}{C_{ox}} \frac{\partial Q_{eff}(\varepsilon)}{\partial \varepsilon} \tag{1.13}$$

and then by substituting Eq. (1.12) into Eq. (1.13), which now results in

$$\begin{aligned} \frac{\partial V_{th}(\varepsilon)}{\partial \varepsilon} &= \frac{q}{C_{ox}} \left\{ D_{it,\,e}(CBM - \varepsilon) \right\} \quad with \quad for \;\; n-channel \\ &= -\frac{q}{C_{ox}} \left\{ D_{it,\,h}(VBM + \varepsilon) \right\} \quad with \quad for \;\; p-channel \end{aligned} \tag{1.14}$$

If the bulk-trap densities in the both channel and dielectric oxide are negligible, $D_{it,\ e}$ $(CBM-\varepsilon)$ and $D_{it,\ h}$ $(VBM + \varepsilon)$ are determined, to be

$$\begin{aligned} D_{it,e}(CBM - \varepsilon) &= \frac{C_{ox}}{q} \frac{\partial V_{th}(\varepsilon)}{\partial \varepsilon} \quad for \;\; n-channel \\ D_{it,h}(VBM + \varepsilon) &= -\frac{C_{ox}}{q} \frac{\partial V_{th}(\varepsilon)}{\partial \varepsilon} \quad for \;\; p-channel, \end{aligned} \tag{1.15}$$

where $D_{it,\ e}$ $(CBM\text{-}\varepsilon)$ and $D_{it,\ h}$ $(VBM + \varepsilon)$ are the DOS (cm^{-2}eV^{-1}) with respect to CBM and VBM for n-channel and p-channel, respectively. Above equations from (1.13) to (1.15) shows how we can eventually extract the information on $\Delta Q_{eff}(\varepsilon)$ and DOS, which is not much difficult because ΔV_{th} (ε) with respect to ε is easily achievable from photo-induced transfer curves (experimental section shows more details). According to the Eq. (1.15) it is worth while to note that if $\partial V_{th}/\partial\varepsilon < 0$ for n-channel (negative V_{th} shift) and $\partial V_{th}/\partial\varepsilon > 0$ for p-channel (positive V_{th} shift) with electronic charge ($q < 0$), the DOS values are always positive regardless of the channel type. It should be again considered that this D_{it} measurement by photo-induced ΔV_{th} with $\Delta\varepsilon$ is only valid in the case without high bulk trap density but in fact with interface trap densities. If our oxide and organic devices respectively with 20- and 50 nm-thick channels show quite a density of bulk traps, their *SS*, μ_{FET}, and I_{off} values should also change because an effective channel layer thickness is at most 5 nm (Debye length) from the interface. However, little change in those experimental factors was observed and now this confirms that our interfacial DOS estimation is valid. If the I_{off} level of given TFT

somewhat increases under photons, the DOS for its interface traps would not be easily distinguished from that of bulk traps [28–30].

1.10 Chapter Summary

TFTs and field-effect transistors have four important performance parameters, which are always influenced by the insulator dielectric/semiconductor channel interface. The electronic, chemical, and physical states of the interface may control the field effect mobility and off-state current etc. due to deep and shallow level traps at/near the interface. Quantitative characterization of such interfacial trap states is not a trivial matter at all, since it should be done with a working TFT/FET. Hence, we suggest the use of PECCS, which accounts for both TFT device physics and interface trap DOS in more or less quantitative ways.

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Chapter 2
Instrumentations for PECCS

Abstract As mentioned in previous chapter, there have been great efforts to study the trap or midgap states in real devices and semiconducting thin-films so far. Photoluminescence (PL) is a direct method to observe deep-level defects in semiconductors but can not be used on a working device with interfaces [1, 2]. Deep-level transient spectroscopy (DLTS) and gate-bias stress techniques may be used with working TFT devices to characterize the interface trap states, utilizing thermal and electrical energies, respectively [2–7]. However, DLTS has its own limit due to poor resolution on unpractical devices while deep-level in DLTS is actually not too deep because of the limit of temperature elevation. Gate bias stress technique is only an industrial test which can not resolve the density-of-states in trap energy level. In this chapter we thus display the instrumentation of photo-excited charge-collection spectroscopy (PECCS) on a working TFT device. [8].

2.1 Introduction of PECCS Measurements System

Figure 2.1 shows the full system of PECCS: photon source, monochromator, and electrical measurement systems.

It is the most important to make monochromatic light to probe the devices if we investigate our working TFT devices and their interfaces by light illumination. This means that it is the key point to understand the grating system and select quite a real monochromatic light from a lamp. Therefore, to install the PECCS measurement system, we should firstly understand about optical light source and gratings monochromator system, and then should study how to measure the interfacial trap density using current-voltage (IV) and capacitance-voltage (CV) measurement under the monochromatic light illumination.

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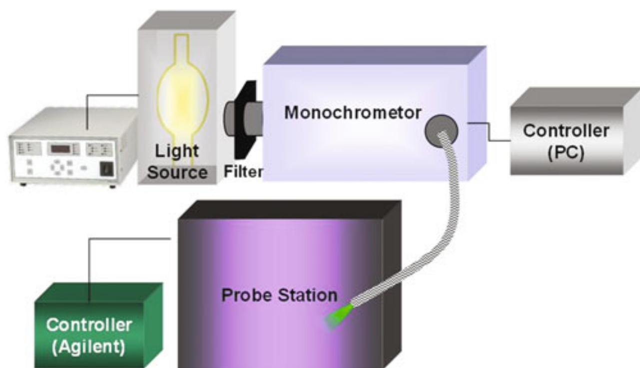

Fig. 2.1 The schematic of PECCS measurement system

2.2 Optical System for PECCS Measurement

2.2.1 Light Source

To get the monochromatic light, we use the 500 Watt Hg(Xe) lamp for light source (Oriel Co.). Figure 2.2 shows the Hg(Xe) lamp, lamp housing and power supply [9].

Arc lamps operate at very high pressures and temperatures, and emit ultraviolet radiation. So, they must be operated in a fully enclosed housing. All arc lamps must be handled properly to prevent contamination of the bulb and resultant thermal stress. Arc Lamp Housing is made up an aluminum enclosure for the lamp, igniter, condensing optics, rear reflector and lamp cooling fan. To get the maximum intensity of the lamp, it is necessary to optimize the position and to compensate for lamp to lamp variations, rear reflector and lamp adjusters. Because the

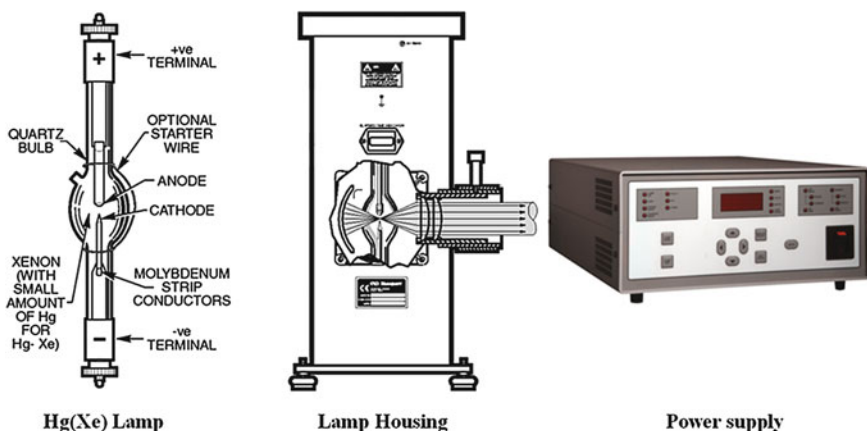

Fig. 2.2 Lamp, lamp housing, and power supply (courtesy from Newport Resource, Ref. [9])

Hg(Xe) Arc lamp emits very strong ultra violet (UV) light, we have to connect one end of the hose to our lamp housing fan and the other end to the Ozone Eater™ which is the catalytic filters that convert the ozone back into oxygen. And also it is better to use the UV protect goggle due to high intensity of deep UV from the lamp housing. Lamp has to be determined by application. One is what wavelength range we require, and the other is how much power we need. So we select the Hg(Xe) Arc lamp because we need wide range of the monochromatic light from infra red to ultra violet region continuously. Hg lamps radiate the strong UV and the Xe lines emit the radiation between 750 and 1000 nm IR range, so Hg(Xe) lamps are suitable for the application from IR to UV range scanning. Moreover Hg(Xe) doesn't have the large variations in output.

Combined with the wavelength, light intensity is important which depends on applied power. One of the matters that require attention to use arc lamp is the life time. Tungsten from the electrodes evaporates slowly with use, and deposits on the inside of the lamp envelope. The surface of lamp bulb is changed gray, then the intensity of the lamp is reduced comparing to that of beginning stage. Generally the life-time is the average period for the visible output to fall to 75 % of the initial value. The life-time of 500 W power Hg(Xe) lamp is about 500 h.

2.2.2 Beam Splitter and Grating Physics

It has to follow the grating equation based on optical physics that the monochromatic light is made from the mixed light source. The basic grating equations may be derived by section rules through the grating surface, normal to the ruling direction as a saw-tooth pattern, as shown in Fig. 2.3, [10].

Light rays A and B, of wavelength λ, incident on adjacent grooves at angle $\boldsymbol{I}$ to the grating normal are shown in Fig. 2.3. Consider light at angle $\boldsymbol{D}$ to the grating normal; this light originates from the A and B rays as they hit the grating. The path difference between the A' and B' rays can be seen to be:

$$a \cdot \sin I + a \cdot \sin D \tag{2.1}$$

Summing of the rays A' and B' results in constructive interference if the path difference is equal to any integer multiple of the wavelength λ:

$$a \cdot (\sin I + \sin D) = m\lambda \tag{2.2}$$

Where:

m = an integer, and is the order of diffraction

This is the basic grating equation.

Note that if $\boldsymbol{D}$ is on the opposite side of the grating normal from $\boldsymbol{I}$, it is of the opposite sign. We have considered only two grooves. Including all the other grooves does not change the basic equation but sharpens the peak in the plot of diffracted intensity against angle $\boldsymbol{D}$.

When a parallel beam of polychromatic light is incident on a grating then the light is dispersed so that each wavelength satisfies the grating equation.

In most monochromators, the input slit and collimating mirror fix the direction of the input beam which strikes the grating. The focusing mirror and exit slit fix the output direction. Only wavelengths which satisfy the grating equation pass through the exit slit. The remainder of the light is scattered and absorbed inside the monochromator. As the grating is rotated, the angles ***I*** and ***D*** change, although the difference between them remains constant and is fixed by the geometry of the monochromator.

A more convenient form of the grating equation for use with monochromators is

$$m\lambda = 2 \times a \times \cos\phi \times \sin\theta \tag{2.3}$$

where

□Φ = Half the included angle between the incident ray and the diffracted ray at the grating
□θ = Grating angle relative to the zero order position

when a special but common case is that in which the light is diffracted back toward the direction from which it came; this is called the*Littrow Configuration*.

These terms are related to the incident angle ***I*** and diffracted angle ***D*** by

$$I = \theta + \phi \quad and \quad D = \phi - \theta \tag{2.4}$$

It is important to note the sign of "m" is given by either form of the grating equation and can be positive or negative. In a monochromator, the angles ***I*** and ***D*** are determined by the rotational position of the grating. We use the sign

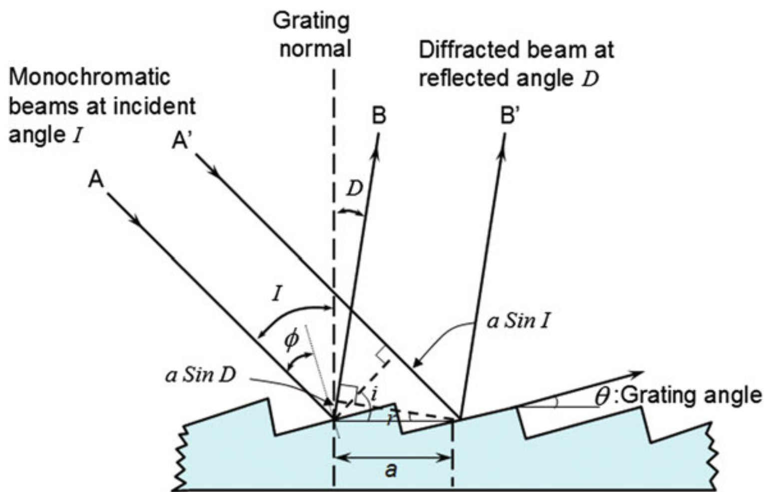

Fig. 2.3 The saw-tooth pattern of a grating section (courtesy from Palmer et al.: Diffraction Grating Handbook. 6th edition, Ref. [10])

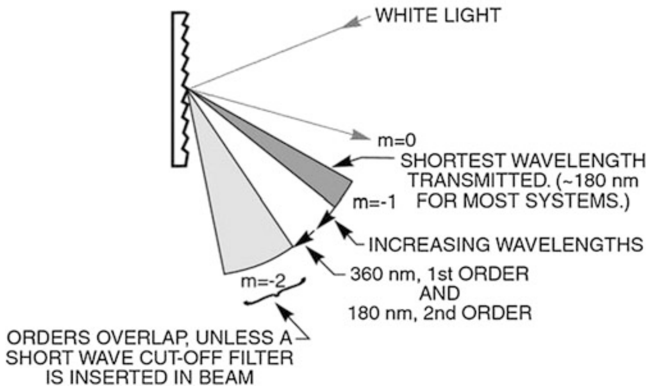

Fig. 2.4 Polychromatic light diffracted from a grating. Positive orders have been omitted for clarity (courtesy from Palmer et al.: Diffraction Grating Handbook. 6th edition, Ref. [10])

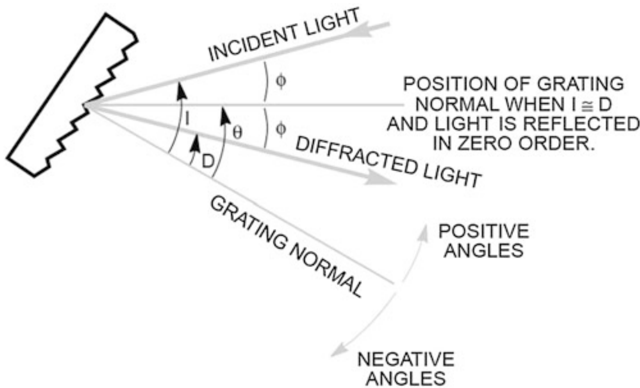

Fig. 2.5 The sign convention for the angle of incidence, angle of diffraction and grating angle (courtesy from Palmer et al.: Diffraction Grating Handbook. 6th edition, Ref. [10])

convention that all angles which are counter clockwise from the grating normal are positive, and all angles which are clockwise to the grating are negative (See Fig. 2.4). The incident light, diffracted light and grating rotation can be at positive or negative angles depending on which side of the grating normal they are. The half angle is always regarded as positive. If the angle $\boldsymbol{D}$ is equal to $\boldsymbol{I}$ and of opposite sign, then the grating angle and order are zero, and the light is simply being reflected. The grating equation is also satisfied for wavelengths in higher orders, when $|m|$ is > 1. Therefore $\lambda_2 = \lambda_1/2$ for $m = \pm 2$, $\lambda_3 = \lambda_1/3$ for $m = \pm 3$, etc. The wavelength λ_2 is in the second order and λ_3 is in the third order, etc. Again, this concept is illustrated in Fig. 2.5. Usually only the first order, positive or negative, is desired. The other wavelengths in higher orders may need

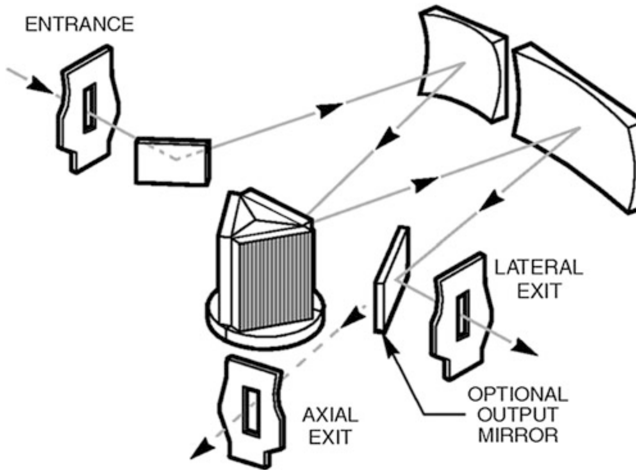

Fig. 2.6 The schematic of three stage grating system in the monochromator (courtesy from Newport Resource, Ref. [9])

to be blocked. The input spectrum and detector sensitivity determine whether order sorting or blocking filters are needed.

2.2.3 Resolving and Filtering Systems for Real Monochromatic Light

Figure 2.6 is the inner structure of the monochromator. It is necessary for the grating system to be used for scanning from NIR (2000 nm) to UV (200 nm) range. We use three stage grating system to get the monochromatic light considering the efficiency of intensity and resolution. We can enhance the resolution or reduce the peak width of our chosen monochromatic light selecting an appropriate grating with many saw-teeth.

It needs special care to extract the monochromatic light with this grating system from white light mixture, since it is rather possible to blend the high order diffraction lights through the monochromator. So, it is necessary to systematically use the band pass filters which may transmit the right light we want.

Figure 2.7 shows the spectrum of 1600 nm monochromatic light which does not pass through the band pass filter. There are 800 nm peak as a second order, and 533 nm peak as a third order, besides 1600 nm the first main peak, so we have to eliminate these higher order peak using the band pass filter. There are several filters for their own purpose: high pass, low pass and band pass filter. Each filter passes high and low wavelengths, while the band pass filter passes the lights between special wave lengths. In our experiments, we use three-four high pass

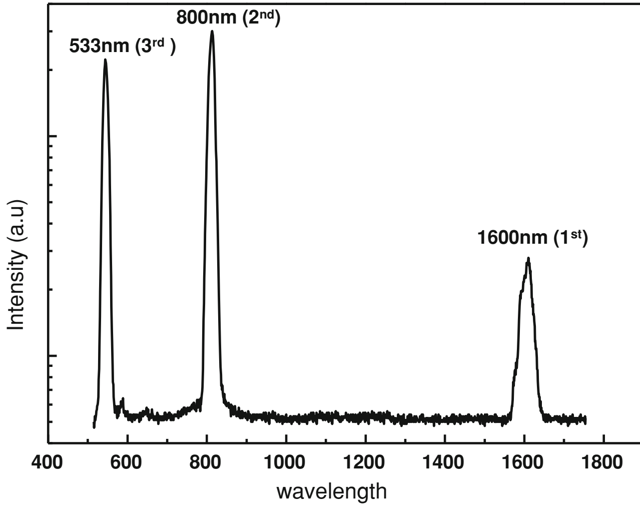

Fig. 2.7 The 1600 nm light made by monochromator without filter system. It includes higher order peaks besides the main 1600 nm light

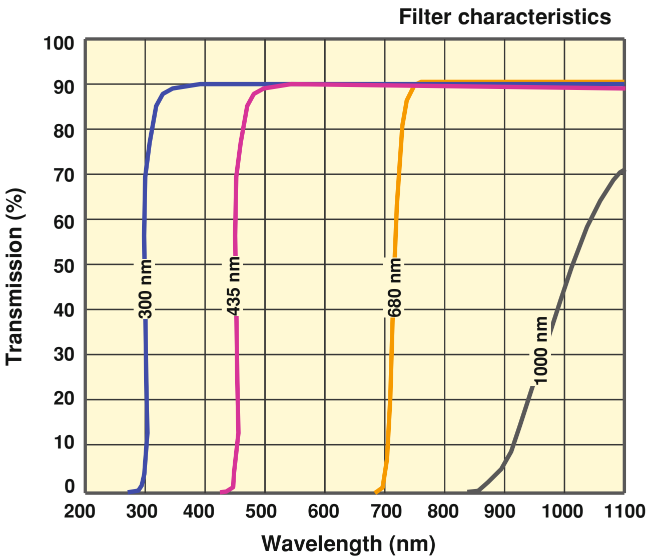

Fig. 2.8 The schematic of low pass filter spectra we used

filters with 300, 435, 680, and 1000 nm cut-off wavelengths as shown in the transmission cut-off spectra of Fig. 2.8, to make a real monochromatic light from the light that comes out of the monochromator. For example, for 1600 nm monochromatic light, we used the 1000 nm high pass filter, then the 680 nm, and 533 nm, so that any higher order light than 1600 nm might be cut-off. Otherwise,

such high-order monochromatic lights are irradiated onto our device, and might ruin any meaningful measurements for the interfacial trap investigation, which can be only possible by single-ordered monochromatic beams.

Figure 2.8 shows the transmission spectra of low pass filters we used. They have about 90 % transmittance except 1000 nm filter. The near IR range lights would thus have slightly lower intensities after going through the 1000 nm low pass filter.

2.2.4 Optical Power Density

A highly-resolved monochromatic light is now delivered from the optical system to a working through an optical fiber, which now becomes a photon probe. Although the efficiency of the optical fiber varies according to the wavelength of light, we can scan the light from near IR to UV energy region. Figure 2.9 shows the transmittance characteristics of the several types of optical fibers. Since we have to scan the ray from 2000 nm to 300 nm, we choose the optical fiber for VIS–NIR.

Figure 2.10 shows the optical system for monochromatic light extraction and probing, composed of lamp, lamp housing, filter, monochromator, and optical fiber set up on an optical table. (The system includes power supply and Ozone eater.) We finally measured the optical power and photon density using this system as shown in Fig. 2.11. An average optical power density of all the monochromatic photon beams (wave length range, 350–2000 nm) in PECCS was measured to be $\sim$0.1 mW/cm^2 (photon flux $\sim 10^{14}$ cm^{-2} eV^{-1} s^{-1}) as measured after delivered through an optical fiber. These number densities are enough for PECCS measurements since in general there are maximum 10^{13}/cm^2 eV^{-1} trap DOS at the dielectric/channel interface.

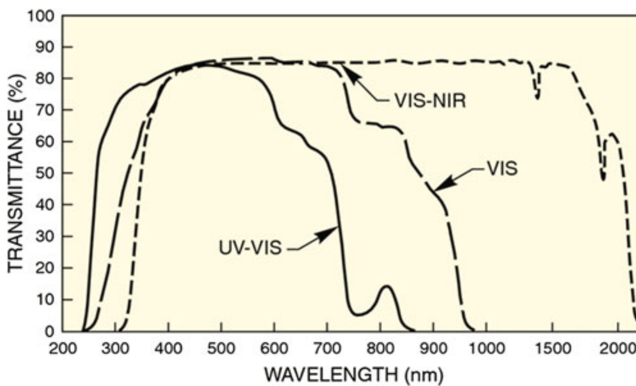

Fig. 2.9 The transmittance of different optical fibers (courtesy from Newport Resource, Ref. [9].)

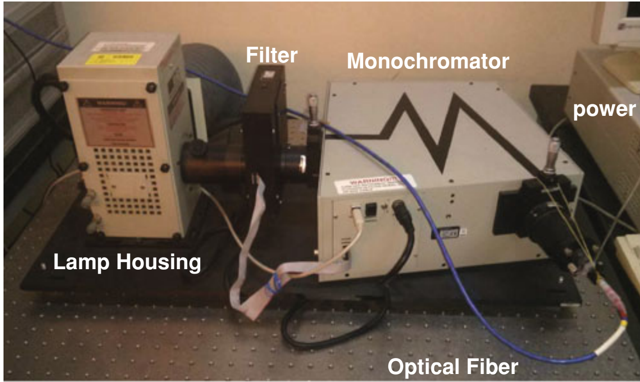

Fig. 2.10 Monochromatic light generation system

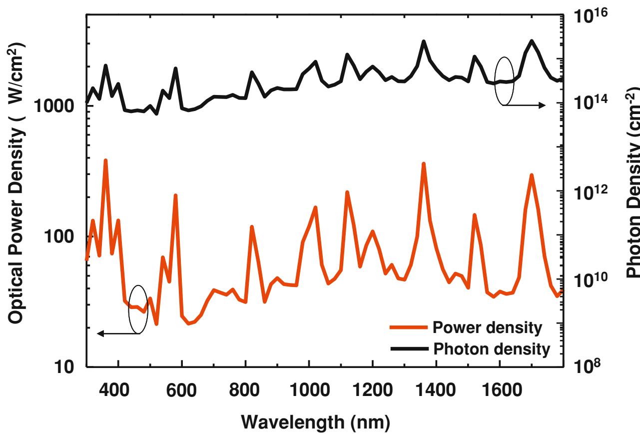

Fig. 2.11 The optical power and photon density of the system

2.3 Electrical Measurement

In this section, it is introduced that the electrical measurement system to measure the electrical properties of the device. Any I–V measurement of devices was carried out with a semiconductor parameter analyzer (Agilent 4155C) in a dark shielding box and in an air ambient at room temperature. C–V measurement was carried out with a precision LCR meter (Agilent 4284A LCR meter). Figure 2.12 shows the equipment, semiconductor parameter analyzer (Agilent 4155C) for I–V measurement and LCR meter (Agilent 4284A LCR meter) for C–V measurement (Fig. 2.13).

Figure 2.14a illustrates the system schematics of PECCS to measure the photo-induced charge density generated in our top-gate transparent ZnO-TFT and bottom-gate pentacene-TFT [8]. The system consist of a light source of 500 W

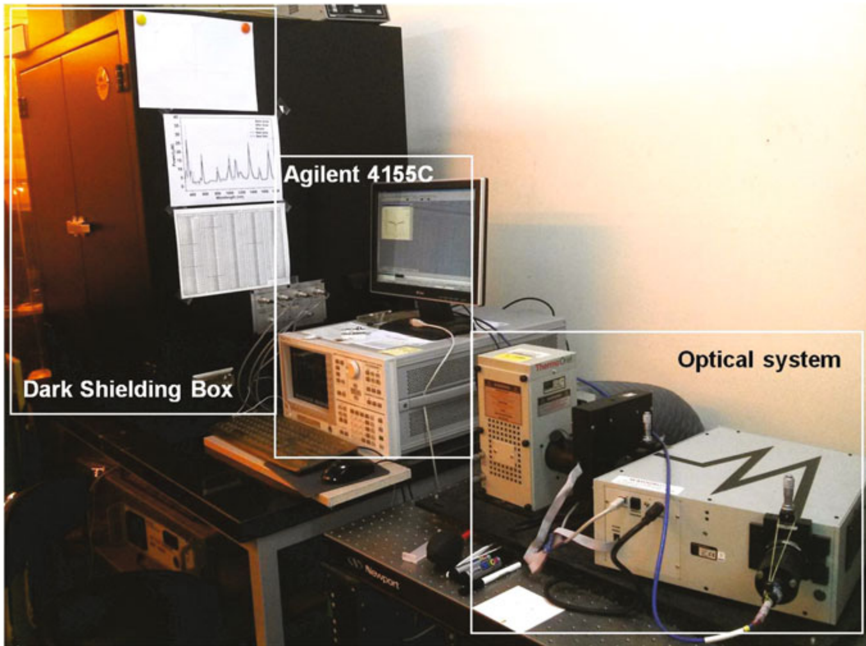

Fig. 2.12 Measurement system: dark shielding box for electrical measurement and the equipment for I–V measurement, Agilent 4155C, and optical system

Fig. 2.13 LCR meter (Agilent 4284A LCR meter) for C–V measurement

Hg(Xe) arc lamp, a grating monochromator covering the spectral range of 254–1000 nm, an optical fiber (core diameter of 200 μm) as an optical probe which guides photons onto the channel of our TFT device, and a semiconductor parameter analyzer (Model HP 4155C, Agilent Technologies). Under an intense monochromatic photon beam the transistor transfer curves were obtained from the TFTs engaged with electrical probes. Figure 2.14b displays the actual features of photo-excited charge-collection spectroscopy working for a top-gate transparent ZnO-TFT. We put our transparent TFT array with glass substrate on a black-color paper, to reveal the TFTs. As shown in Fig. 2.14b, we used three electrical probes of source, drain, and gate, and one optical probe delivering energetic photons. For the photo-electric measurement, we applied sequentially mono-energetic photons

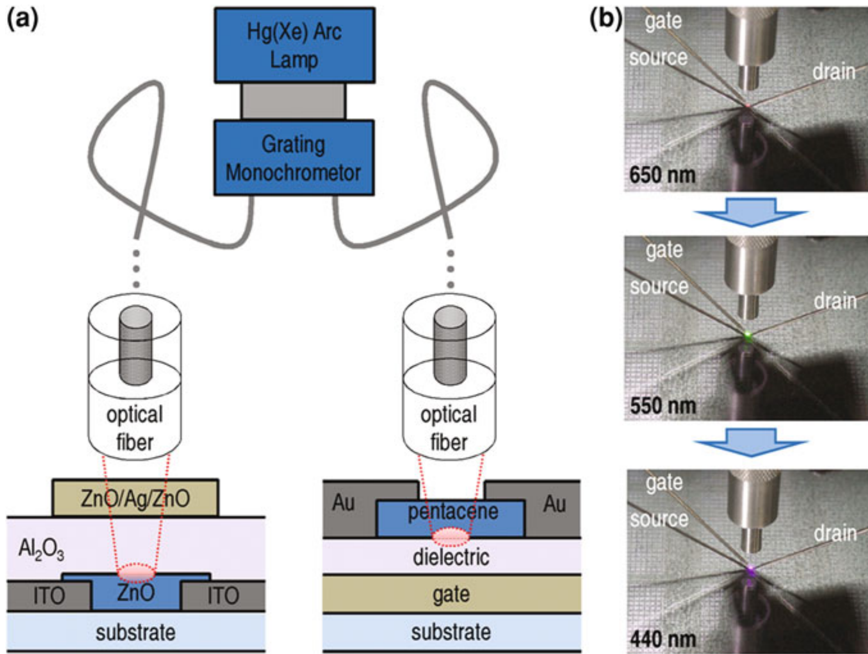

Fig. 2.14 **a** Measurement set-up: two kinds of working TFT devices (*top-gate* ZnO- and *bottom-gate* pentacene-TFT) and monochromatic illuminations to be delivered onto channel/dielectric interface by optical fiber probe. **b** Photographic views of photo-excited charge-collection spectroscopy using monochromatic beams, among which *red* (650 nm), *green* (550 nm), and *blue* (440 nm) lights are operating on fully transparent ZnO-TFTs. We put our transparent TFT array on a black-color paper to reveal the TFTs

onto our TFT device from low to high energy, to release the trapped charges at the channel/dielectric interface in the order from shallow to deep-level.

2.4 Data Processing and Analysis for DOS Profile

Details for the DOS and data process/analysis have already been introduced in previous chapter (Sect. 1.9) with ZnO- and pentacene-TFTs. For $\Delta Q_{eff}(\varepsilon)$ and the DOS, $D_{it}(\varepsilon)$ we had better chop the energy scale in more narrow way, to resolve the PECCS spectra, however, we should also consider that long measurement duration may cause unwanted gate bias stress effects on our TFT devices. So, we usually take a $\Delta\lambda$ of 5 nm wave length interval for each photo-transfer curve measurement step [$\varepsilon(\text{eV}) = 1240/\lambda$ (nm)]. After measuring and plotting the $\Delta Q_{eff}(\varepsilon)$ through more than 150 curves, the DOS, $D_{it}(\varepsilon)$ is plotted by differentiating the $\Delta Q_{eff}(\varepsilon)$ curve. Figure 2.15a and b thus show the interfacial trap DOS profiles for ZnO- and pentacene-TFTs as respective examples [8]. The inset of Fig. 2.15a

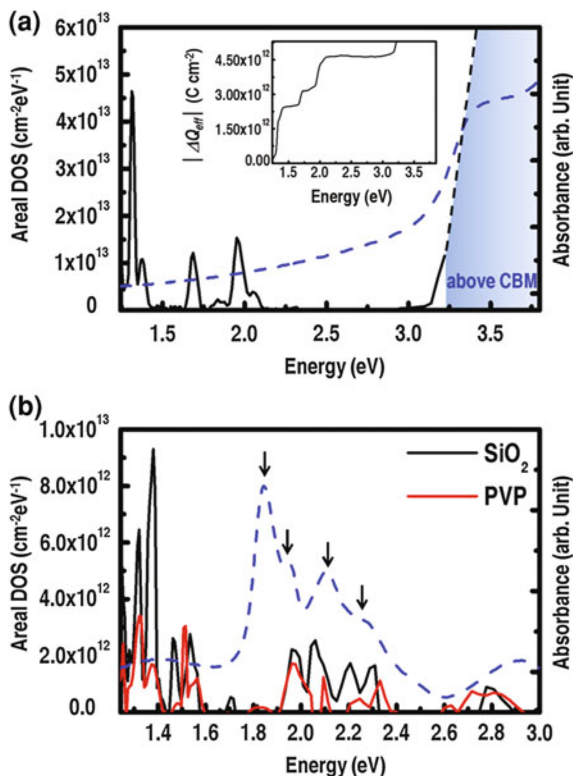

Fig. 2.15 **a** The DOS plot extracted from $|\Delta Q_{eff}(\varepsilon)|$ vs. ε plot (*inset*) of ZnO-TFT. The plot was overlapped with an optical absorbance spectrum of ZnO/Al_2O_3 on glass (*dashed blue*), which was prepared for comparison. The DOS profile above CBM is too high to be measured. (The*shaded region* means "above CBM".) **b** The obtained DOS plots for pentacene-TFTs with SiO_2 (*solid black*) and PVP (*solid red*) gate dielectric layer. The optical absorbance spectrum for pentacene/PVP on glass was measured (*dashed blue*), to be compared with the DOS profiles

shows the plot of $\Delta Q_{eff}(\varepsilon)$ vs. photon energy ε. The most interesting peaks are found at ~1.31 and 1.38 eV below CBM with a large DOS peak intensity of 4.6×10^{13} and 1.1×10^{13} $cm^{-2}eV^{-1}$, respectively. These peaks are apparently too deep to be considered as an oxygen vacancy (V_O) or a zinc interstitial state (Zn_i) in ZnO. When the photon energy approaches to the band gap of ZnO (~3.34 eV), the $\Delta Q_{eff}(\varepsilon)$ curve shoots up as shown in the inset of Fig. 2.15a. The dashed blue curve is an optical absorbance spectrum of ZnO/Al_2O_3 (on glass) which was fabricated under the same experimental conditions, to be compared with the DOS profile. Large absorption was observed at similar photon energy levels near the conduction band minimum (CBM) of ZnO. However, unlike the DOS profile, which was very sensitive to the interface traps, optical absorption could not resolve those trap levels located at the ZnO/Al_2O_3 interface. The DOS plots for two types of pentacene-TFTs with SiO_2 (solid black) and with poly-4-vinylphenol (PVP) gate dielectrics (solid red) are shown in Fig. 2.15b. Our PECCS again works equally well for organic pentacene-TFTs with pentacene/dielectric interface. Regardless of the type of dielectrics, the CBM state which is equivalent to the lowest unoccupied molecular orbital (LUMO) in organic semiconductors, was found at the same energy level, identified by a peak at ~1.96 eV, with similar DOS value of ~2×10^{12} $cm^{-2}eV^{-1}$ for both pentacene-TFTs. (Here the energy

level is with respect to valence band maximum (VBM) or the highest occupied molecular orbital (HOMO)). The peak value is in good agreement with the HOMO–LUMO gap of solid pentacene. Besides the HOMO–LUMO level, a few other molecular levels above the HOMO–LUMO were always observed at ~2.1, ~2.2, and ~2.3 eV in our DOS profiles. These features are the replica found from the (arrow-indicated) exciton peaks of optical absorbance spectra of a solid pentacene film (blue dashed line), but some energy deviation between optical gap and HOMO–LUMO gap is shown due to the high exciton binding energy over 0.1 eV in pentacene. However, the most important spectroscopic results from our photo-excitation method may be the DOS peaks observed at ~1.32 and ~1.38 eV. The DOS peaks are clearly observed for both pentacene-TFTs with PVP and SiO_2 dielectrics although the peaks are much smaller in the case of the device with PVP. Those two energy levels have not been reported but must be the states of deep hole traps although they are found above HOMO but quite near LUMO level. Those levels can not be resolved with optical absorption, which is not interface-sensitive. This again means that our photo-excited charge-collection spectroscopy is highly sensitive to interfacial traps.

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Chapter 3
PECCS Measurements in Organic FETs

Abstract Organic field-effect transistors (OFETs) have been extensively investigated for display and many other electronic applications, since they are expected to promote advances in plastic or glass electronics based on low cost and flexibility. Whether the type of organic semiconductor channels are small molecule-based or polymer-based, the performance and stability of OFETs strongly depends on the nature and density of charge traps present at the channel/dielectric interface and in the thin-film channel itself near the interface [1–3]. Therefore the characterization of these traps is critical. We here introduce PECCS-based DOS measurements on p-channel [4] and n-channel [5] small molecule (thermally evaporated pentacene)-based FETs with differently prepared channel/dielectric interface, so that we can display detailed mid-gap states in the various channel/dielectric interfaces of FET devices. In another section of, [6] we also included some detailed PECCS studies on polymer-based OFETs where their channels were composed of polymers such as P3HT etc., since the photo-induced current in polymer-based OFETs behave different from small-molecule OFETs.

3.1 PECCS on Small Molecule-Based p-Channel FETs

P-channel small molecule OFETs are the most well-known basic devices where pentacene crystal thin-film plays as an active semiconductor layer for the device in general even though other types of small molecules were reported. The issues of organic pentacene/organic or inorganic dielectric interface are extremely important because the surface states almost determine the crystalline quality of the channel layer and even the electric stability of devices along with the interfacial trap states. In this section, we thus studied the effects of dielectric surface states on the device performance and stability using our tool, PECCS.

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3.1.1 Experimental Procedures

3.1.1.1 Fabrication of Model Pentacene-Based FETs With Surface Functionalized Thin Al_2O_3 DIELECTRICS

The substrate of indium-tin-oxide (ITO)/glass was cleaned with acetone, methanol, and de-ionized (DI) water, in that order. The ITO was then patterned to be a bottom gate electrode by wet etching. For dielectric, we used atomic layer deposition (ALD)-grown 60 nm-thin Al_2O_3 as deposited it on patterned ITO glass at 200 °C [7, 8]. The surface of Al_2O_3 was functionalized with such a variety of self-assembled-monolayers (SAMs) as Hexamethyldisilazane (HMDS), 7-octenyltrichlorosilane (7-OTS), and Trichloro(1H, 1H, 2H, 2H-perfluorooctyl) Silane (FTS) by using the universal methods [9–13]; the substrates reacted with 7-OTS and FTS solution (0.1 wt%) using hexane as the solvent by immersion for 1 h at room temperature (RT). In HMDS coated sample case, it was coated on the substrates by spin casting at RT. After that, the SAM-modified samples were dried in the vacuum oven at 100 °C for 1 h. Pentacene (Aldrich Chem. Co., 99 % purity, no other distillation) active channel layers were patterned on the dielectric layers through a shadow mask by thermal evaporation at a substrate temperature of room temperature (RT). We fixed the deposition rate to 1 Å/s for the thermal evaporation in a vacuum chamber (base pressure of $\sim 2 \times 10^{-7}$ Torr). The final pentacene thickness was 50 nm, which are measured by ellipsometry. For S/D of the pentacene-FETs, Au was then evaporated onto the pentacene channels at RT. Nominal channel length (L) and width (W) of our pentacene-FETs were 90 and 500 μm, respectively. Figure 3.1a–d display schematic cross-sections of pentacene-FETs with pristine, HMDS-functionalized, 7-OTS-functionalized, and FTS-functionalized Al_2O_3 dielectrics, respectively.

3.1.1.2 PECCS

Figure 3.2a illustrates the measurement schematics of photo-excited charge-collection spectroscopy to measure the photo-induced charge carriers generated in our bottom-gate pentacene-FET. Our measurement setup consists of a light source of 500 W Hg(Xe) arc lamp, a grating monochromator covering the spectral range of 254–1000 nm, an optical fiber (core diameter of 200 mm) as an optical probe which guides photons onto the channel of our FET device, and a semiconductor parameter analyzer (Model HP 4155C, Agilent Technologies). Under an intense monochromatic photon beam (photon flux of at least 5×10^{15} cm^{-2} s^{-1} as estimated from the optical power density, ~ 2 mW cm^{-2}), the transistor transfer curves were obtained from the FETs engaged with electrical probes. The inset in Fig. 3.2a displays the actual feature of photo-excited charge-collection spectroscopy working for a pentacene-FET, on which three electrical probes of source, drain, and gate, and one optical probe delivering energetic photons are located.

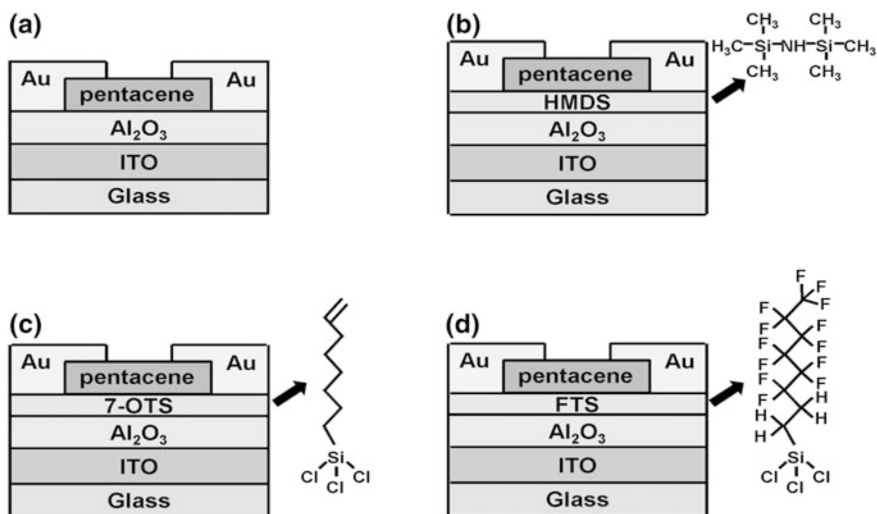


Fig. 3.1 Schematics of pentacene-FETs with **a** pristine, **b** HMDS-functionalized, **c** 7-OTS-functinalized, and **d** FTS-functionalized Al_2O_3 dielectric layers. Each chemical structure of SAMs is illustrated with its respective device

3.1.2 Analysis of Trap Density of States

For the photo-electric measurement, we applied sequentially mono-energetic photons onto our FET device from low to high energy (spectral/or wavelength interval $\Delta\lambda$: 5 nm), to release the trapped charges at the channel/dielectric interface in the order from shallow to deep-level. Gate-bias sweep started from the channel accumulation state because we should initially fill up all the interface trap states with charge carriers prior to the photo-excitation process. Since pentacene-FET has a p-channel, the traps would be filled with holes (see the band diagram in Fig. 3.2b). When the photo-excitation initiates, the trapped charge carriers are released into the band edges as indicated by the arrows. Then, threshold voltage shift, ΔV_{th}, as a function of photon energy would be clearly observed from pentacene-FETs (as those shifts are actually shown in the Fig. 3.3a–d). These photo-induced ΔV_{th} can be explained by hole transitions from its trap states to the highest occupied molecular orbital (HOMO) level. When photons with a specific energy, ε, illuminate through the thin channel to reach the channel/dielectric interface of a FET, most of the trapped holes in the gap states between HOMO and HOMO + ε are excited to HOMO level in the p-channel pentacene-FET, since the number of incident photons (order of $\sim 10^{14}$ cm^{-2}) is large compared to that of trap states, which is far smaller (less than order of $\sim 10^{13}$ cm^{-2}). This means that the effective trap charge (Q_{eff}), which is mainly for the traps at the channel/dielectric interface, can be varied with photon energy *e*, and then the photo-shifted V_{th} can be represented by

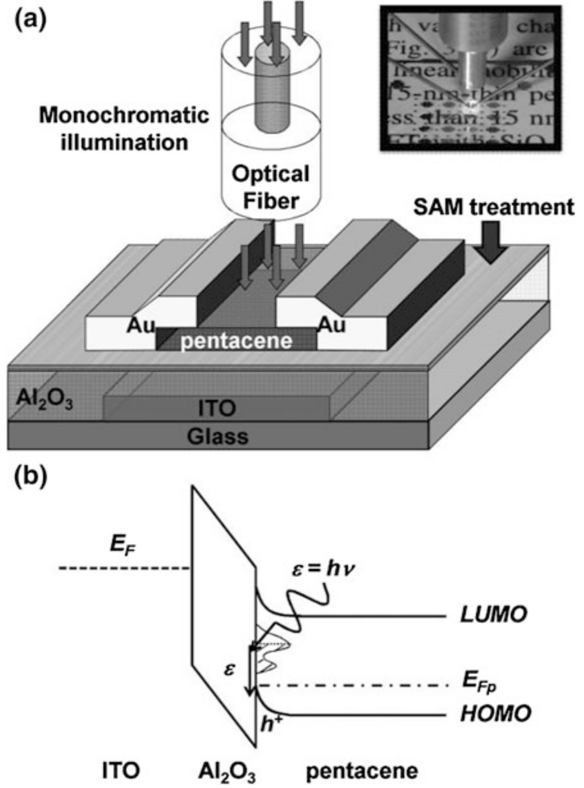


Fig. 3.2 **a** Schematic of photo-excited charge-collection spectroscopy with monochromatic illuminations. Inset shows the photographic view of real measurement with 550 nm-illumination. **b** Energy band diagram which elucidates the photo-excitation of interface trap charges in p-channel pentacene-FET

$$V_{th}(\varepsilon) = \phi_{ms} - \frac{Q_{eff}(\varepsilon)}{C_{ox}} + \Psi_{S,\max} + \frac{Q_G}{C_{ox}} \tag{3.1}$$

with

$$Q_{eff}(\varepsilon) = q \int_{LUMO}^{HOMO+\varepsilon} D_{it}(E)dE + qN_b t_{ox}, \tag{3.2}$$

where ϕ_{ms} is the metal–semiconductor work function difference, C_{ox} is the dielectric capacitance per unit area (F cm^{-2}, our 60 nm-thin Al_2O_3 showed $\sim$100 nF cm^{-2}), $\psi_{s,max}$ is the potential due to band bending of the channel semiconductor, Q_G is the charge associated with dielectric band bending as induced by gate bias, N_b is the average density (cm^{-3}) of bulk traps in the gate dielectric, t_{ox} is the dielectric thickness, and D_{it} is the DOS at channel/dielectric interface (cm^{-2} eV^{-1}). Since ϕ_{ms}, $\psi_{s,max}$, and Q_G in Eq. (3.1) are rarely changed by e, and N_b in Eq. (3.2) also hardly varies with ε, photo-induced ΔV_{th} can be analyzed by taking a derivative of Eq. (3.1) with ε, as shown below,

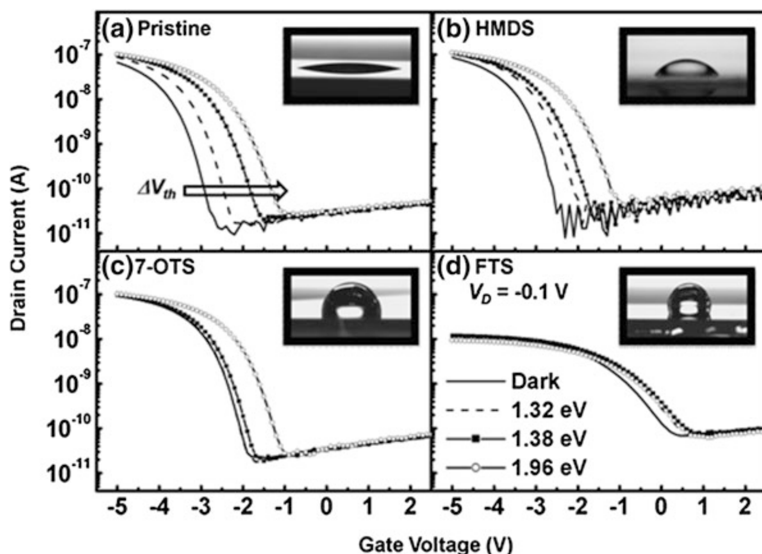


Fig. 3.3 Static photo-induced transfer characteristics obtained from **a** Pristine, **b** HMDS-functionalized, **c** 7-OTS-functionalized, and **d** FTS-functionalized pentacene-FETs. Inset shows DI water contact angle images for their respective SAMs

$$\frac{\partial V_{th}(\varepsilon)}{\partial \varepsilon} = -\frac{1}{C_{ox}}\frac{\partial Q_{eff}(\varepsilon)}{\partial \varepsilon} \tag{3.3}$$

and then by substituting Eqs. (3.2)–(3.3), which now results in

$$\frac{\partial V_{th}(\varepsilon)}{\partial \varepsilon} = -\frac{q}{C_{ox}} D_{it}(HOMO + \varepsilon) \tag{3.4}$$

If the second terms of Eq. (3.4) are negligible, (little change of experimental sub-threshold slope (S), field-effect mobility (μ_{FET}), and off-state drain current (I_{off}) values in Fig. 3.3a–d may confirm this [1, 14, 15]) $D_{it}(HOMO + \varepsilon)$ are determined, to be

$$D_{it}(HOMO + \varepsilon) = -\frac{C_{ox}}{q}\frac{\partial V_{th}(\varepsilon)}{\partial \varepsilon} \tag{3.5}$$

where and $D_{it}(HOMO + \varepsilon)$ are the DOS (cm^{-2} eV^{-1}) with respect to HOMO for p-channel. According to the Eq. (3.5) it is worthwhile to note that if $\partial V_{th}/\partial \varepsilon > 0$ for p-channel with electronic charge ($q < 0$), the DOS values are always positive regardless of the channel type.

3.1.3 Results and Discussion

3.1.3.1 Photo-Induced Transfer Curves of Pentacene-FETs with Various Dielectric Surfaces

The photo-induced transfer (drain current-gate voltage; $I_D - V_G$) characteristics for pentacene-FET with pristine Al_2O_3 are shown in Fig. 3.3a, along with its dark transfer curve. A very low drain voltage, V_D of -0.1 V was applied to the devices, so that the photo-charge collection proceeds in a very linear regime, not in saturation (to protect any probable measurement error by a large drain electric field). As shown in the Fig. 3.3a, the photo-induced ΔV_{th} was clearly observed under several exampled illuminations with the photon energies (1.32, 1.38, and 1.96 eV) while no significant changes in S, μ_{FET}, and I_{off} values were observed. According to the other Fig. 3.3b–d, the phenomena of photo-induced change become weak when the organic devices are prepared with an intermittent monolayer between pentacene channel and oxide dielectric. The inset photos in the figures shows the contact angles of DI water in the hydrophobicity order of the SAMs. In particular,

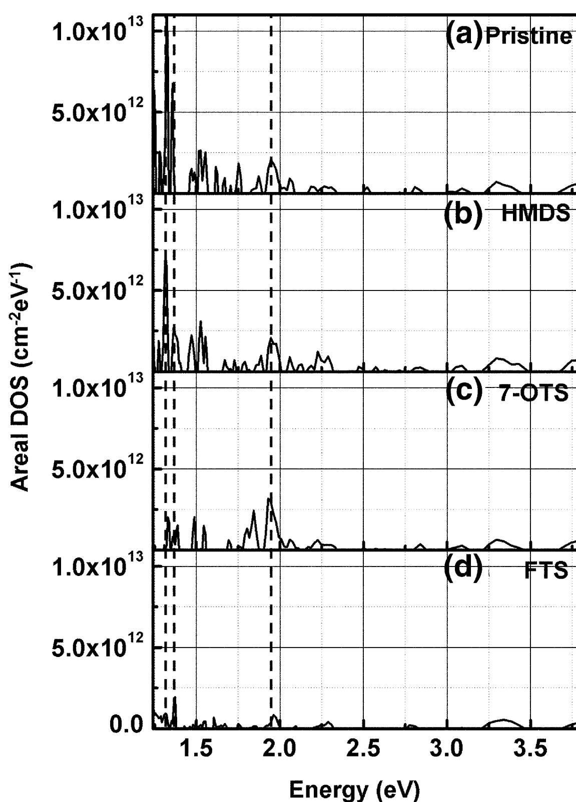


Fig. 3.4 DOS profiles obtained by photo-excited charge-collection spectroscopy from **a** pristine, **b** HMDS-functionalized, **c** 7-OTS-functionalized, and **d** FTS-functionalized pentacene-FETs. Positions of main DOS peaks of 1.32, 1.38, and 1.96 eV are marked with *dashed lines*. (Spectral interval $\Delta\lambda$: 5 nm for mono-energetic photons)

the FET with FTS-functionalized dielectric displayed a very small change of the transfer curves under the illuminations and also note that its I_D current level is an order of magnitude lower than those of other devices.

3.1.3.2 Measured DOS of Deep Traps in the Working Pentacene-FETs

The DOS plots for four types of pentacene-FETs with pristine and functionalized Al_2O_3 dielectrics ($C_{ox} \sim 100$ nF cm^{-2}) were obtained through the ΔV_{th} estimation from the photo-induced transfer curves, as shown in Fig. 3.4a–d. Regardless of the type of functional groups, the lowest unoccupied molecular orbital (LUMO) state in organic semiconductors, was found at the same energy level, identified by a peak at ~1.96 eV for all pentacene-FETs. (See the third dashed line. Here the energy level is with respect to HOMO). The peak value is in good agreement with the HOMO–LUMO gap of solid pentacene [16, 17]. Besides the HOMO–LUMO level, a few other molecular levels above the HOMO–LUMO were always observed near ~2.3, 3.3, and 3.8 eV in our DOS profiles. However, the most important spectroscopic results from our photo-excitation method may be the DOS peaks observed at ~1.32 and 1.38 eV. The DOS peaks are clearly observed for all the pentacene-FETs although the peaks are much smaller in the case of the device

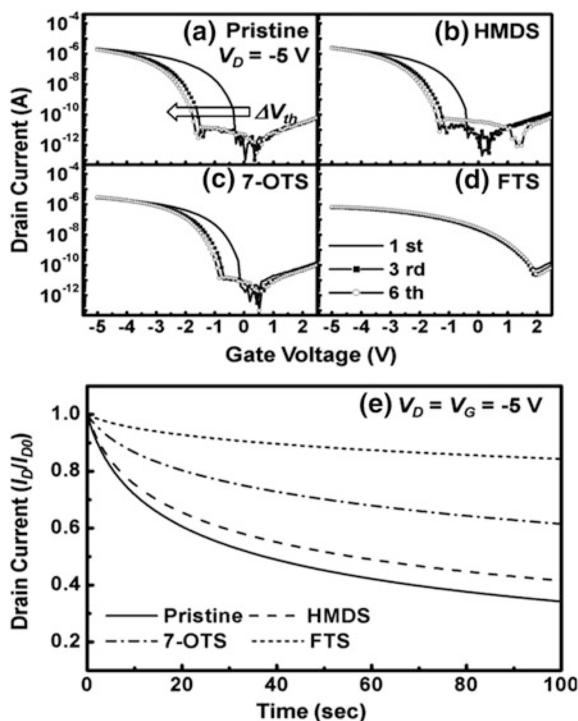


Fig. 3.5 Transfer curves obtained by repeated gate-bias sweep on **a** pristine, **b** HMDS-functionalized, **c** 7-OTS-functionalized, and **d** FTS-functionalized devices in saturation regime. ($V_D = -5$ V) **e** Time-dependent drain current behaviour of pentacene-FETs with different kinds of SAMs under a gate-bias stress condition. Such drain current is normalized by dividing its initial current (I_{D0})

with FTS-functionalized dielectric while the first device with pristine Al_2O_3 shows stronger DOS peak intensities than those of any other devices. Those two energy levels have not been reported but must be the states of deep hole traps. Those interface traps can not be sensed by optical absorption, which can only sense the bulk properties of thin films. This means that our photo-excited charge-collection spectroscopy is highly sensitive to interfacial traps, and according to the DOS profiles in Fig. 3.4a–d, more hydrophobic the dielectric surface is, lower densities of deep hole traps generate at the pentacene channel/dielectric interface.

Another feature which is worthwhile to note in Fig. 3.4a–b is the intensity difference of HOMO–LUMO peaks ($\sim$1.96 eV) which may represent the crystalline quality of the first few monolayer pentacene. According to our spectroscopy data, the HOMO–LUMO peak intensity of FTS-functionalized stable pentacene-FET is much smaller than those of other devices. This means that the crystalline quality of pentacene channel is quite inferior in the case of FTS-treated FET, and surprisingly the transfer curve of the FTS-treated device in Fig. 3.3d indirectly prove such fact, showing an order of magnitude lower I_D than those of pristine, HMDS-, and 7-OTS-functionalized devices. (Also see another sets of transfer curves of Fig. 3.5a–d. Our FTS-functionalized OFET displayed a low saturation mobility of $\sim$0.1 cm^2/Vs while that of pristine OFET did $\sim$0.7 cm^2/Vs.) Likewise, our photo-excited charge-collection spectroscopy again demonstrates its high detection sensitivity for the interfacial trap density and even provides an evaluation basis for the channel crystalline quality of working pentacene-FET as well.

3.1.3.3 Photo- vs. Dark-Electric Stabilities in Our Pentacene-FETs with Various Dielectric Surfaces

As a matter of fact, this photo-electric stability of channel/dielectric interface is deeply related to the dark electrical stability as well. For example, under long-term negative gate-bias stress or repeated gate-bias sweep in the dark, more holes are possibly trapped at the pentacene/dielectric interface, so that most of the devices with trap-containing pentacene/Al_2O_3 interface might show much unstable time-dependent behavior [18–20]. According to the dark transfer curves of Fig. 3.5a–d, the threshold voltage shift by repeated sweep (maximum 6 times) is clearly observed in the cases of pentacene-FETs with less hydrophobic SAMs while our FTS-treated device displayed very stable features. This is because during the negative bias sweep more of deep- or shallow-level holes become trapped at the interface where the trap sites exist, and this behavior thus shows the opposite directional shift of threshold voltage with respect to the photo-induced shift we observed from Fig. 3.3a–d [18–20]. More evidence comes from a gate stress measurement as shown in Fig. 3.5e. This time-dependent measurement again displayed that our FTS-treated FET contained the least number of deep or shallow trap sites at its pentacene/dielectric interface. For this reason, in the case of FTS-functionalized FET, the initial I_D (I_{D0}) only slowly decreases as time passes under a negative gate-bias while the I_{D0} rapidly drops in the other cases of devices.

As above, we have implemented PECCS to quantitatively measure the DOS of interfacial deep traps in working organic pentacene channel FETs. The photo-induced ΔV_{th} successfully quantified the profile of the DOS of deep-level defects located at or near the channel/dielectric interface. Inspired by the spectroscopy results, we have also fabricated a very photo-stable trap-minimized pentacene-FET with FTS-functionalized dielectrics. As a byproduct of PECCS measurement, we could observe the electronic structure of organic semiconductor as DOS of HOMO–LUMO, which indicates even the crystalline quality of semiconductor channel film.

3.2 PECCS on Small Molecule-Based n-Channel FETs

An important motivation of n-channel organic EFT research may be the fact that n-channel ORGANIC FET can use less expensive source/drain (S/D) electrode than that of p-channel device; in fact, Au has been used as a common hole-injection electrode material for p-channel ORGANIC FET while its price has been continuously increased for the last 10 years [21, 22, 28]. Since usual n-type organics are unstable in air, many groups studied to improve the stability and have reported somewhat air-stable n-channel performance. Researchers have introduced electron-withdrawing substituents to the host n-channel materials, lowering the lowest unoccupied molecular orbital (LUMO) level below an empirical onset region (~ 3.8–4.0 eV) of ambient oxidation [24–27]. Among many commercially-available n-type materials, for our experiments, we employed N,N′-ditridecyl-perylene-3,4:9,10-tetracarboxylic diimide–C13 (PTCDI-C13, see the inset of Fig. 3.6c for its molecular structure), which has been most widely studied as a

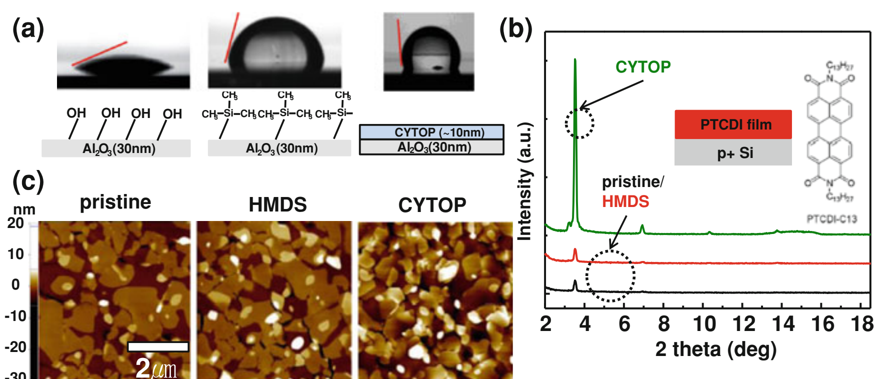


Fig. 3.6 **a** DI water contact angles measured on pristine, HMDS-modified, and 10 nm-thin CYTOP surfaces, **b** AFM images of PTCDI-C13 crystalline film grown on the three dielectric surfaces, **c** X-ray diffraction results from the PTCDI-C13 crystalline films grown on the three surfaces the inset molecular structure represent a molecule of PTCDI-C13

vacuum-deposited n-type small molecule in crystalline form with quite a high lowest unoccupied molecular orbital (LUMO) level of ~3.6 eV [29]. Due to its air-stability and tunability of LUMO level in perylene derivative, they were used in such general research areas as organic light-emitting transistor and complementary circuits [30, 31]. As the main focus of our n-channel ORGANIC FET study, we modified the surface states (or hydrophobicity) of dielectric expecting an improved device stability. This surface modification includes the introduction of hydrophobic self-assembled monolayers (SAMs) and formation of hydrophobic polymer film on a dielectric oxide layer [30, 32, 33]. Since a larger number of hydroxyl (–OH) sites on the surface of usual oxide dielectrics not only impede the device performances of ORGANIC FETs (carrier mobility etc.) but also induce unstable device behavior (gate hysteresis and threshold voltage shift, ΔV_{th}) during device operation, it is meaningful to make the dielectric/channel interface electrically stable by modifying the dielectric surface in regards of both p- and n-channel ORGANIC FETs [23, 30, 32, 33].

In order to improve the device stability further, we also introduced a small molecule passivation layer, which is composed of 6,13 pentacenequinone, oxidized pentacene form [34]. The passivation layer plays as a barrier against ambient oxygen and water molecule, retarding their penetration into active layer or channel interface. Finally, we quantitatively analyzed the trap density-of-states (DOS) at the active channel/dielectric interface by means of photo-excited charge carrier spectroscopy (PECCS) method, as a measure of interface stability [33, 35].

3.2.1 Experimental Procedures

For the substrate of ORGANIC FETs, the glass (Eagle 2000) was cleaned with acetone, ethanol, and de-ionized water in that order. After that, a bottom gate electrode of 100 nm-thick Al was thermally evaporated to be patterned on the cleaned glass through a shadow mask. A 30 nm-thin Al_2O_3 film was deposited by atomic layer deposition (ALD) at 100 °C and its surface was modified in two different ways; hexamethyldisilazane (HMDS) and dilute CYTOP solution were coated by spin-coating on the pristine Al_2O_3 film, to be respectively cured at 110 and 180 °C [36].

Then 40 nm-thin PTCDI-C13 channel layer was patterned by thermal evaporation (rate: 0.1 nm/s) on the three different Al_2O surfaces (pristine, HMDS-treated, and CYTOP-coated). Each sample was post-annealed in vacuum for 1 h oven at appropriate temperature between 80 and 140 °C, and Al source/drain electrode was patterned on the channel layer by thermal evaporation. For the passivation on the ORGANIC FETs, 100 nm-thick 6,13 pentacenequinone (PQ, Aldrich Chem. Co.) was thermally evaporated by organic molecule beam deposition system at the deposition rate of 0.1 nm/s. All of FETs have nominal channel length (L) and width (W) of 90 and 500 μm, respectively. Thin-film samples for the measurements of contact angle, atomic force microscope (AFM) and X-ray

diffraction (XRD), 100 nm thick PTCDI film was prepared on a p+ -silicon of which the surface was modified with the same manner as done for above ORGANIC FETs. All PTCDI films were post-annealed at 140 °C. All the electrical measurements such as drain current-gate voltage ($I_D - V_G$) transfer, gate-bias stress test, were performed with Agilent 4155C semiconductor parameter analyzer in the dark and in an ambient condition. Photo-excited charge collection spectroscopy (PECCS) was performed with a light source (500 W, Hg(Xe) arc lamp), a grating monochromator covering the spectral range of 254–1000 nm, and an optical fiber (core diameter of 200 μm) as an optical probe which guide photons onto the channel region of the working device. Photon flux of at least 2×10^{14} cm^{-2} s^{-1} (optical power density, 0.2 mW cm^{-2}) was measured after lights passed through the optical fiber.

3.2.2 Results and Discussion

3.2.2.1 PTCDI Crystalline Films and ORGANIC FETs With Surface-Modified Dielectric Layers

Figure 3.6a presents the de-ionized (DI) water contact angles as measured on differently-prepared substrates (see schematics under the results). The most hydrophobic state is observed from the thin-coated CYTOP on Al_2O_3 dielectric, while the raw surface without any treatment appears much hydrophilic with many OH groups. When 100 nm-thick PTCDI film was grown, AFM observation showed larger grains from the PTCDI film on un-modified dielectric surface than from the films on hydrophobic surfaces (Fig. 3.6b). It should be noted that all PTCDI film shown in Figs. 3.6, 3.7, 3.8, is post-annealed at 140 °C. The HMDS-modified dielectric surface resulted in smaller PTCDI grains than those on

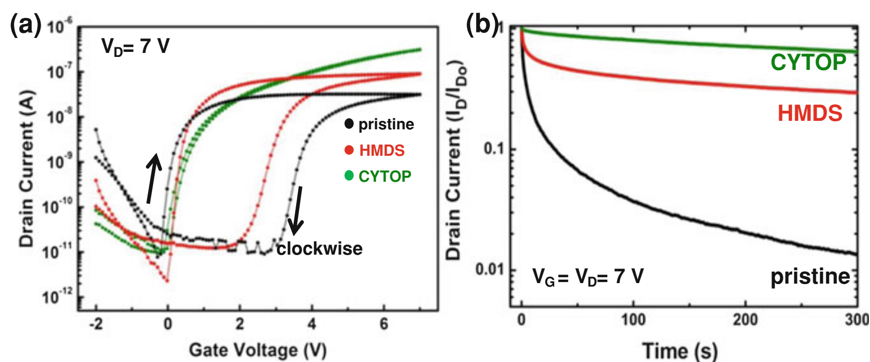


Fig. 3.7 **a** ID-VG transfer curves of the three ORGANIC FETs with pristine, HMDS-and CYTOP-modified Al2O3, **b** Time dependent ID plots for the ORGANIC FETs as normalized by initial ID current

unmodified surface, but showed relatively larger grains than those on CYTOP. The PTCDI film grown on CYTOP exhibits the most corrugated surface, since the CYTOP surface has more hydrophobic state than the others. However, regardless of its smallest size, the PTCDI film grown on CYTOP showed incomparably superior crystalline quality to those from other surface states in regards of XRD peak intensity, as shown in Fig. 3.6c. This means that the crystalline ordering in organic crystals is not significantly related to their grain size.

The ORGANIC FET devices show their transfer characteristics at 7 V drain voltage (VD) in Fig. 3.7a as fabricated according to the surface modifications of Fig. 3.6a; the curves qualitatively reflect their organic channel/dielectric interface states. All of three devices exhibit clock-wise hysteresis. In general, such a

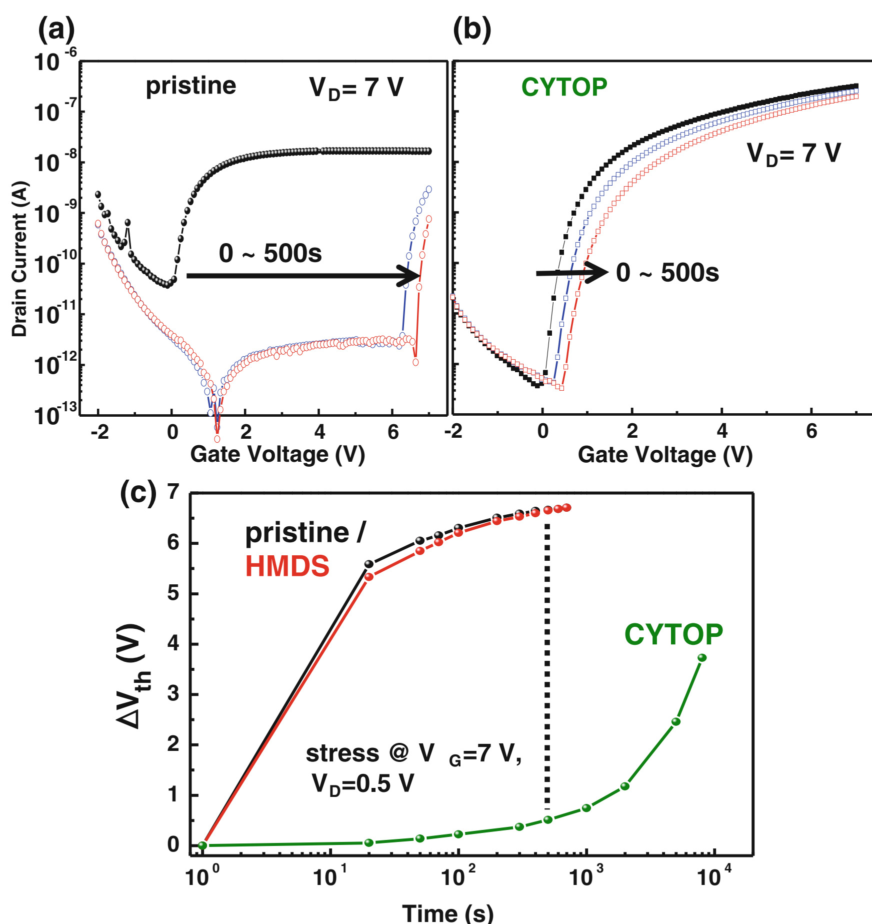


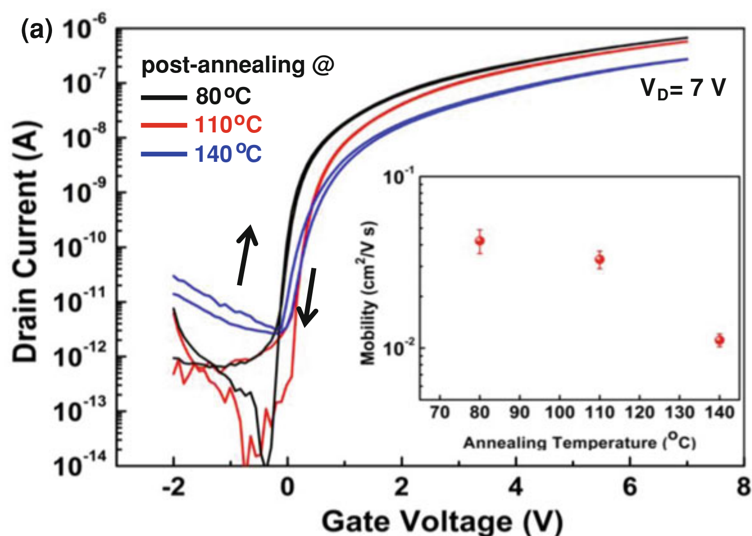
Fig. 3.8 Bias stress-induced transfer curves obtained from our ORGANIC FETs **a** with pristine Al_2O_3 dielectric and **b** with CYTOP-modified Al_2O_3 dielectric. **c** Those results are summarized as time domain ΔV_{th} plots where the device with CYTOP appears the most stable

clock-wise gate-hysteresis is due to the shallow-level trap charges which repetitively experience V_G-induced trapping and de-trapping processes at the semiconductor/dielectric interface, and we suspect that the charges are the OH group-trapped electrons [37–39]. As expected, the most hydrophobic surface appears to show little hysteresis in the figure while more hydrophilic dielectric surface introduces larger hysteresis window. It is noteworthy that along with the smaller hysteresis the on current I_D level increases. High density traps are electrically negative, probably deterring the accumulation of carrier electrons at the channel/dielectric interface and also playing as scattering centres to retard carrier transport.

Additional evidences for the electron charge trapping was observed from time-dependent I_D measurements which were performed under a fixed V_G (= V_D) of 7 V. As plotted in Fig. 3.7b for normalized I_D values (I_D/I_{Do}; I_{Do} is an initial drain current), the more hydrophobic surface induces less degree of time-dependent electron trapping, as a result, the ORGANIC FET with hydrophobic CYTOP-coated dielectric shows the least I_D decrease while other ORGANIC FETs with untreated and HMDS-treated dielectric do significant I_D drops due to charge trapping. Besides the time-dependent I_D decrease of Fig. 3.7b, time-dependent V_{th} shift (known as bias stress (BS) measurements) was also performed under the same gate-bias condition as taken in the time-dependent I_D tests, and the results are shown in Fig. 3.8a, b, [40]. Since the negative charges are trapped at the hydrophilic interface under the BS, the carrier electrons are hard to gather at the channel after the BS and the electron gathering requires higher positive V_{th}. In this regard, relatively fast and large V_{th} shift (ΔV_{th}–6 V) was observed from the ORGANIC FET with un-modified pristine dielectric at a $V_D = 0.5$ V after a BS stress of 7 V V_G for $\sim$500 s (Fig. 3.8a) while the other ORGANIC FET with CYTOP-modified dielectric shows only $\sim$0.5 V shift (Fig. 3.8b). According to the summary plot for BS in Fig. 3.8c, the ORGANIC FET with CYTOP-modified dielectric begins to show a significant V_{th} shift only after a few thousand seconds of BS stress. It is uncertain and can not be resolved by the BS measurements (Figs. 3.7b and 3.8a, b) whether the trap levels for the electron charges are shallow or deep. We regard that the trap levels are probably mixed.

3.2.2.2 ORGANIC FET Prepared at an Optimum Post-Annealing Temperature

Since relatively superior stability and performance were observed from the ORGANIC FET with CYTOP-modified dielectric, we chose the device as a prospective ORGANIC FET for more improvement. According to the previous reports, PTCDI-derivative thin-film needs to be post-annealed at 120–140 °C in general for gaining larger grain-size [39–42], while some other cases of n-channel ORGANIC FETs displayed proper mobilities even without post-annealing (instead, their deposition rate for PTCDI small molecules was as small as 0.01 nm/s [43–45] and in fact, our case of ORGANIC FET channel deposited at 0.1 nm/s without post-anneal did not show any proper on-current I_D due to its poor channel crystallinity).



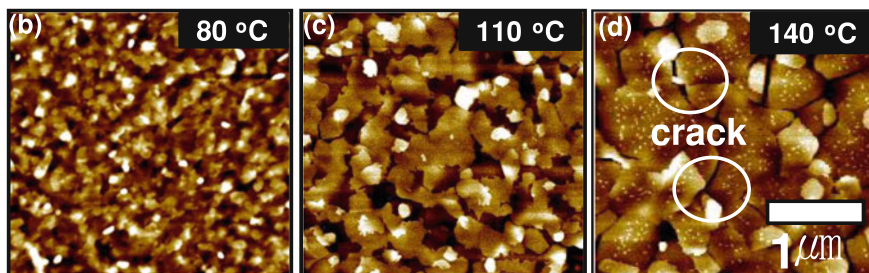


Fig. 3.9 **a** Post-annealing results for the device performance curves (temperature-dependent transfer characteristics and mobility plot (*inset*)) as obtained from our ORGANIC FETs with CYTOP-modified dielectric. **b–d** shows respective AFM images from the ORGANIC FETs annealed at 80, 110, and 140 °C

Our PTCDI n-channel interfaced with the CYTOP thin film which has quite a low glass transition temperature (T_g) near 110 °C. We thus attempted various annealing temperatures of 80, 110, and 140 °C, suspecting that there could be an optimal temperature below the general post-annealing temperature (120–140 °C). Figure 3.9a displays the transfer characteristics of ORGANIC FETs, whose PTCDI channels on CYTOP surface were annealed at the three different temperatures. Drain voltage (V_D) for the transfer curves was taken to be 7 V for the saturation mobility evaluation. According to the mobility evaluation (inset), the ORGANIC FET prepared by 140 °C annealing shows the lowest value of 0.01 cm^2/Vs even along with a little hysteresis. The highest mobility ($\sim$0.04 cm^2/Vs) and on-current without gate hysteresis was rather obtained from 80 °C annealing-prepared ORGANIC FET. The AFM images in Fig. 3.9b–d clearly show the increase of grain size with post-annealing temperature, but we can also observe that the PTCDI

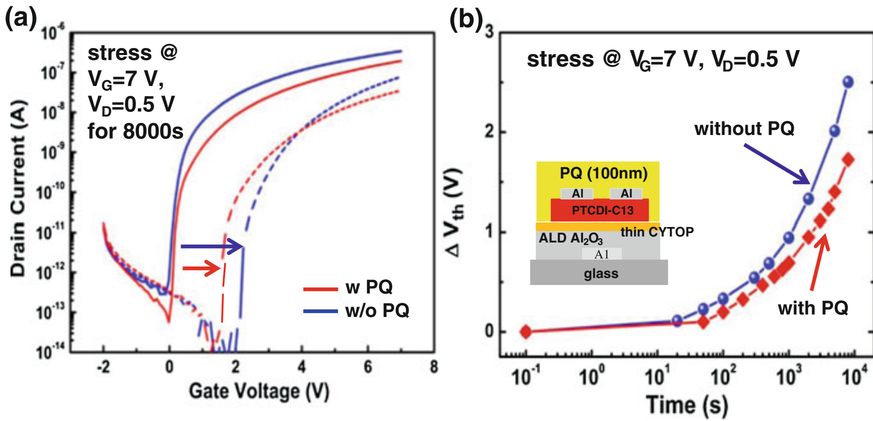


Fig. 3.10 **a** Long term BS-induced transfer curves and **b** time-dependent plots showing the positive V_{th} shift in PQ-passivated and un-passivated ORGANIC FETs with CYTOP-modified dielectric

surface processed at 140 °C contains intra-domain cracks which are certainly not grain boundaries. These intra-domain cracks might take place starting at the CYTOP/PTCDI interface since the T_g of the bulk CYTOP is around 110 °C and higher post-anneal temperature deforms the CYTOP/PTCDI interface [46]. We thus suspect those cracks the cause of low on-current, low mobility and a little hysteresis [38, 47]. In contrast, the PTCDI film annealed at lower temperature (80 °C) than T_g has smaller grain sizes but with more densely packed structure on CYTOP surface; it would be more desirable, having good interface without such cracks and resulting in a higher field-effect mobility.

In Fig. 3.10a, we display the BS stress results from our n-channel ORGANIC FETs prepared by 80 °C post-annealing when the BS condition of $V_G = 7$ V and $V_D = 0.5$ V was given for 8000 s. A relatively smaller V_{th} ($\sim$2.5 V) was observed than that ($\sim$3.8 V) from the previous ORGANIC FET with 140 °C post-anneal (see Fig. 3.8c). Anticipating any improved electrical stability, we applied 100 nm 6,13 pentacenequinone (PQ) layer as passivation layer on our ORGANIC FET device with the following reasons; 1) it can play as a blocking layer against ambient O_2 and H_2O molecules since it is an already-oxidized small molecule film, 2) the PQ layer also blocks ultraviolet (UV) since it absorbs UV to convert into green light, preventing UV-induced oxidation of PTCDI film. According to the results of Fig. 3.10a, b, the BS-induced V_{th} ($\sim$1.8 V) appears slightly lower in the ORGANIC FET with PQ-passivation than in the other without PQ. Therefore, it is likely that the already-oxidized PQ layer would be beneficial playing a role of a barrier against O_2 and H_2O diffusion into PTCDI channel [47–50]. The PQ layers were also applied to other devices with n-channels that were post-annealed at 110 and 140 °C, and again demonstrated the stability-improving effects for those devices (not shown here).

3.2.2.3 Trap DOS Measurements on Optimum-Processed ORGANIC FETs by PECCS

As our last experimentation, we implemented PECCS measurements on our 80 °C -annealed ORGANIC FETs with and without PQ passivation layer, to analyze and compare the trap DOS densities of the both ORGANIC FETs, which are located near the dielectric/n-channel interface. Fig. 3.11a, b shows the dark- and photo-transfer curves of the two ORGANIC FETs as obtained at a V_D of 0.5 V under monochromatic photons whose energy sequentially increases. When the photo-excitation initiates, the trapped charge carriers (electrons) are released/de-trapped into the LUMO edge and drained. Then, ΔV_{th} as negative shift with respect to initial curve is observed as a function of photon energy. Here, it is worthy of note that our PECCS-induced V_{th} shift is negative while the BS-induced ΔV_{th} is positive with respect to initial curve. According to the figures, the photo-induced V_{th} shifts observed from un-passivated ORGANIC FET is apparently larger than those from PQ-passivated one, indicating that un-passivated ORGANIC FET must have higher interfacial trap density. These results are more quantitatively summarized with the plot of effective trap charge density (ΔQ_{eff}) vs. photon energy

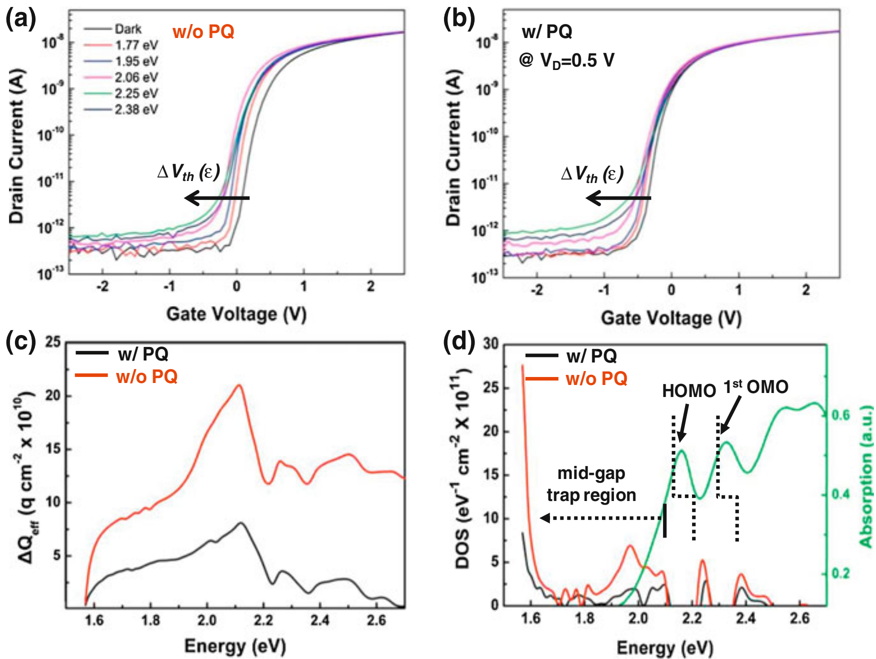


Fig. 3.11 Photo-induced transfer curves for **a** un-passivated and **b** PQ-passivated ORGANIC FETs prepared with CYTOP-modified dielectric and 80 °C post-annealing; note the negative V_{th} shift in both cases. Those V_{th} shifts are plotted as **c** Q_{eff} with respect to the photon energy and as **d** the trap DOS by differentiating the Q_{eff} with the photon energy. In DOS plots, HOMO–LUMO gap was determined to be 2.25 eV, below which the trap DOS peaks are observed

(Fig. 3.11c), where ΔQ_{eff} is $C_{ox} * \Delta V_{th}$ and C_{ox} is the dielectric capacitance. The estimated effective trap charge density of un-passivated ORGANIC FET is 2.2×10^{11} cm^{-2} which is 3 times larger than that of the PQ-passivated device. By differentiating the trap charge density plot with the photon energy, the trap DOS profiles are obtained as shown in Fig. 3.11d. In the figure for DOS, the green curve represents an optical absorption spectrum of thin PTCDI-C13 film deposited on glass. Whether the passivation layer was applied or not, highest occupied molecular orbital (HOMO) energy level was found at ~2.25 eV which is 0.1 eV larger than 2.15 eV observed in the optical absorption spectrum of PTCDI-C13 thin-film. This slight difference is attributed to exciton binding energy [51, 52], so we regard actual HOMO–LUMO gap of PTCDI-C13 film as 2.25 eV (as indicated by dashed lines). Worthwhile to note, in Fig. 3.11d, is that somewhat broad range of interfacial trap peaks are monitored below HOMO–LUMO gap (~2.25 eV). These interfacial trap DOS peaks are not shown by optical absorption spectra, since the electrically sensitive traps exist at the gate dielectric/channel interface of ORGANIC FET device. The trap DOS peaks of un-passivated ORGANIC FET appear higher in intensity as expected from Fig. 3.11c. We thus presume that the passivation layer on organic semiconductor layer plays its role of impeding the external O_2 or H_2O molecule diffusion to the interface. In Fig. 3.11d, the trap DOS peaks located at ~1.96, 2.06 eV and near 1.50 eV might be related to those molecules, although their exact charge-trapping mechanism at the interface is not clear yet. It also should be noted in the DOS plots that the peaks indicating the HOMO and 1st OMO levels (~2.25, 2.37 eV) exist for both ORGANIC FETs with and without PQ in similar manner.

As mentioned above, we have fabricated vacuum deposited PTCDI-C13-based n-channel ORGANIC FETs on 30 nm Al_2O_3 whose surface has been modified with HMDS and thin hydrophobic CYTOP. PQ passivation layer turn out to be helpful for keeping the interfacial trap DOS minimum, according to PECCS measurements.

3.3 PECCS on Polymer-Based FETs

Self-assembled regioregular thiophene based polymer semiconductors with supramolecular two-dimensional structures are of growing interest owing to their relatively high mobility coupled with solution processibility, allowing for printable low-cost large area electronic circuits [53–59]. It is well known that these semiconducting polymers modified for increased inter chain stacking can exhibit the carrier delocalization leading to the high field-effect mobility [58–63]. Therefore, self-ordering of the polymer chains in bulk polythiophene films has been extensively investigated for high-performance ORGANIC FET applications [53–63]. However, the research on the quantum states and their density of states (DOS) associated with the inter chain stacking in the polymer semiconductor bulk or at the polymer semiconductor/dielectric interface has rarely been carried out although this

quantum state information is significantly related to the device properties [57, 64, 65]. It is mainly attributed to a lack of in situ experimental techniques, which should sensitively measure the quantum states and DOS at the interface or in the bulk of working polymer FET channel. In this work, we use PECCS to investigate the two-dimentional polaronic structures in such a variety of thiophene-based crystalline-forming polymer semiconductors as poly(3-hexylthiophene) (**P3HT**), Poly(3,3‴-didodecylquaterthiophene) (**PQT-12**) [61, 62] and poly(didodecyl-quaterthiophene-*alt*-didodecylbithiazole) (**PQTBTz-C12**) [68], which is a newly synthesized polymer for an advanced channel material.

3.3.1 Experimental Procedures

Figure 3.12a shows the schematic experimental setup of PECCS. Our spectroscopic measurement system is equipped with a light source of 500 W Hg(Xe) arc

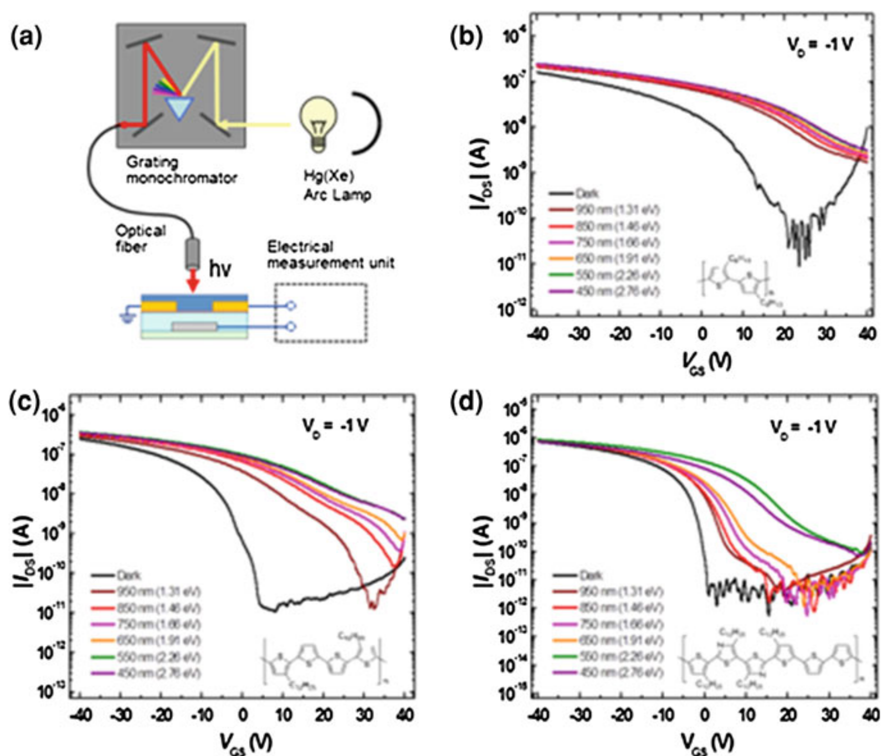


Fig. 3.12 **a** Schematic experimental setup of the PECCS measurement and the linear regime (VDS = −1 V) static photo-induced transfer curves obtained from **b** P3HT based FETs, **c** PQT-12 based FETs, and **d** PQTBTz-C12 based FETs under several energetic photon beams. The *inset* of the **b**–**c** shows molecule structure of the polymer semiconductor in the active channel layer

lamp, a grating monochromator covering the spectral range of 300–1000 nm, an optical fiber (core diameter of 200 μm) as an optical probe which guides photons onto the channel area of the testing device, and an electrical measurement unit (4155C Semiconductor Parameter Analyzer, Agilent Technologies). Under an intense monochromatic light (photon flux of at least 5×10^{14} cm^{-2} s^{-1} as estimated from the optical power density, 0.2 mW cm^{-2}), the transfer curves were obtained from the testing FETs connected to the electrical measurement unit. For the fabrication of the testing FETs, we used a 300 nm thick thermally grown silicon oxide gate dielectric (capacitance $C_i = 10$ nF cm^{-2}) on the heavily doped n^{++}-Si wafer (gate electrode). The surface of the wafer was treated with a 0.1 % solution of octadecyltrimethoxysilane, OTS (Gelest Inc.) in trichloroethylene (EMD Chemicals Inc.) to enhance the device performance [66]. Gold source-drain electrodes were evaporated through shadow masks. The final thickness of the electrodes was ~70 nm. The channel width (W) is 1000 μm, and the channel length (L) is typically 100 μm. The polymer semiconductor films were spun with 1 wt% solution of P3HT (purchased from Sigma-Aldrich Co.) or PQT-12 (purchased from American Dye Source) or PQTBTz-C12 (synthesized by Samsung Advanced Institute of Technology) in chlorobenzene onto OTS-treated SiO_2 substrates. Then, the channel polymer films were cured at an appropriate temperature (140 °C for P3HT, 130 °C for PQT-12, and 180 °C for PQTBTz-C12) for 1 h in N_2 ambient. The final thickness of all polymer films measured by a surface profiler was ~110 nm.

3.3.2 Results and Discussion

The linear regime photo-induced (and dark) transfer curves of the polymer semiconductor FETs based on P3HT, PQT-12, and PQTBTz-C12 are shown in Fig. 3.12b–d, where the respective polymer materials are also presented with their molecular schemes in insets. The field-effect mobility (m_{FE}) and threshold voltage (V_{Th}) were derived from the linear region of the $I_D - V_G$ characteristic and the inverse of the sub-threshold swing ($S = dV_G/dlog(I_D)$) from the linear region in the appropriate log plot. In the linear region of the $I_D(V_G)$ curve, the devices exhibited prototypical transistor behavior with reasonable ON–OFF ratios higher than 10^4 and with respective high m_{FE} values of 0.04, 0.07, and 0.20 cm^2/Vs for P3HT, PQT-12, and PQTBTz-C12, even though our newly developed ORGANIC FET with PQTBTz-C12 appeared the most superior to others in the regards of device performance and photo-stability. However, we can observe abrupt changes in V_{Th} and some alterations of other device parameters such as S and the off-state drain current (I_{off}) at a certain low photon energy (1.31 eV). More importantly, the dependence of the change in V_{Th} on the wavelength (or energy) of the incident photons is elucidated by charge transitions from certain energy states in the highest occupied molecular orbital (HOMO) to lowest unoccupied molecular orbital (LUMO), midgap levels between the HOMO and LUMO, and even higher levels

than LUMO. When photons of a specific energy, e incident on both the channel area (near the interface) and the channel/dielectric interface of FET, most charges in the compatible energy states are excited to LUMO since the number of incident photons (order of $\sim 10^{14}$ cm^{-2}) is large enough to excite most electronic charges in low energy states (lower than $\sim 10^{13}$ cm^{-2}). This means that the excited charge (Q_e) in the sub-gap states formed at both the channel and the channel/dielectric interface of ORGANIC FET can be varied with e, and then the photo-induced ΔV_{Th} ($\Delta V_{Th} = V_{Th} - V_{Th}^{Dark}$) can be represented by [35]

$$\Delta V_{Th}(e) = Q_e(e)/C_i, \tag{3.6}$$

where C_i is the dielectric capacitance per unit area (F/cm^2).

On the other hand, unlike the small molecule-based ORGANIC FETs we observe serious modifications of S and I_{off} in these polymer-based ORGANIC FETs. We thus regard in these cases that the photo-induced S changes are much associated with the change of density of deep bulk states in the organic semiconductor channel as well as the interface/or the bulk states near the organic semiconductor channel/dielectric interface of ORGANIC FET. It is similar to the case for amorphous silicon (a-Si) based device, so we now remind ourselves of the S equation [67, 68]

$$S = \frac{kT}{q\,\log(e)}\left[1 + \frac{qd_i}{\varepsilon_i}\left(\sqrt{\varepsilon_{OSC} N_{BS}} + qN_{SS}\right)\right] \tag{3.7}$$

where ε_i and ε_{osc} are the insulator and semiconductor dielectric constants, respectively, d_i is the insulator thickness, q is the absolute value of the electron charge, k is the Boltzmann constant, T is the temperature, N_{BS} is the density of bulk states near interface and N_{SS} is the density of interface states. It should be noted that an accurate and analytical relation between the S in a polymer-based ORGANIC FET and the density of states in the organic material has not been derived yet. Instead, we can infer that the photo-induced S change possibly came from the real bulk states which are away from the interface and should thus be counted as an extra quantity beside the ($N_{BS}(e) + N_{SS}(e)$).

Such ΔV_{Th} dependence on the energy of the incident photons as identified from many individual photo-induced transfer curves of P3HT, PQT-12, and PQTBTz-C12 is plotted as normalized form in Fig. 3.13b–d, respectively. Respective optical absorption spectra of spin-coated polymer semiconductor thin-films were also plotted as references. According to Fig. 3.13b–d, the PECCS spectra of the polymer semiconductors exhibit the highest occupied molecular orbital-lowest unoccupied molecular orbital (HOMO–LUMO) absorption peaks in the band of 2.05–2.45 eV, with subtle differences due to the exciton-dissociation energy [69] but generally well matching those in the UV–vis absorption spectra of the corresponding polymer films meaning that $N_{SS}(e)$ is relatively small compared to $N_{BS}(e)$ in the π–π^* absorption region. The important difference between PECCS spectra and the UV–vis absorption is that only the PECCS spectra show some additional absorption peaks below the HOMO–LUMO absorption edge.

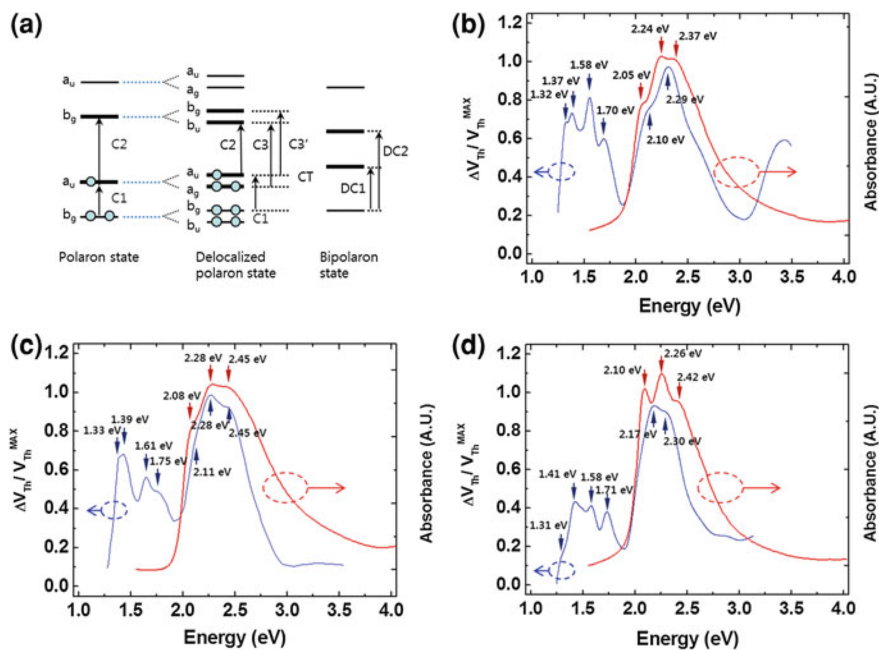


Fig. 3.13 **a** Schematic energy diagram of polarons on the isolated chains (*left*), interacting chains (*center*), and bipolaron states on the isolated chains (*right*). Adapted from Refs [4, 5]. **b** The dependence of normalized V_{Th} on the energy of the incident photons as achieved from many individual photo-induced transfer curves of **b** P3HT, **c** PQT-12, and **d** PQTBTz-C12

Table 3.1 Energy level of the optical transition in the polymer semiconductor TFTs

Molecule	C2 (eV)	C3 (eV)	C3′ (eV)	CT (eV)	DC2 (eV)
P3HT	1.37	1.70	1.32	0.33	1.58
PQT-12	1.39	1.75	1.33	0.36	1.61
PQTBTz-12	1.41	1.71	1.31	0.30	1.58

The position of these additional charge-induced absorption peaks are marked in the Fig. 3.13b–d. In order to interpret these spectral features, we employ a model that was originally developed for the charge modulation spectroscopy (CMS) result of P3HT by Sirringhuas group [54–57, 65, 70]. According to the model, only two optical transitions would be allowed (depicted C1 and C2 in the left scheme of Fig. 3.13a) for the polarons placed on an isolated single polymer chain. However, in the presence of strong interchain interaction for P3HT, PQT-12 and PQTBTz-C12, the polarons should no longer be confined to a single chain but would be delocalized over the two-dimensional lamellae structure of self-assembled polymer chains, resulting in a splitting of the polaronic levels into doublets. In this case, two new optical transitions (depicted CT, for charge transfer transition, and C3/C3’ in the middle scheme of Fig. 3.13a) appear, while the C2 transition

becomes symmetry-forbidden. For each polymer semiconductor, these additional charge-induced absorption peaks are summarized in Table 3.1.

The most distinguished difference between our PECCS and previously reported CMS results on thiophene based polymer semiconductors is the presence of the another peaks (positioned at around 1.60 eV), which might be related to the bi-polaron level presumably created during the bias stress [71–75]. In fact, for the highly ordered polymer semiconductors such as P3HT, PQT-12 and PQTBTz-C12 with crystalline domains, Coulombic repulsion hampers creation of bipolarons as the polymer chain increases in length [76]. However, the active polymer layers of the testing devices investigated with PECCS were exposed to air ambient during the operation and thus more easily oxidized, susceptible to the aforementioned changes of S and I_{off}, while the polymer semiconductor of the testing unit investigated by the CMS is covered with an electrode or an organic insulating material [56, 65]. Therefore, it is highly possible that the bipolarons are created by the self-trapping of polaron in the oxidized site of the polymer chain in the testing devices for PECCS. However, we also need to note that below the π–π^* absorption edge, $N_{BS}(e)$ is hardly distinguished with $N_{SS}(e)$ and thus the intensity or position of the featured peaks can be perturbed by the interface states. To clearly define the origin of these peaks—whether from the interface states or bulk states, the application of PECCS to the study of the bias stress effects will be presented for more details in the future [77].

In Fig. 3.14, we overlaid the density of state (DOS) profiles of P3HT, PQT-12 and PQTBTz-C12, as obtained by differentiating $Q_e(e)$ with the incident photon energy (e). Surprisingly, all the absorption peaks of respective polymers in the DOS profiles are nearly overlapped, implying that the intrinsic electronic properties of P3HT, PQT-12 and PQTBTz-C12 are very similar even though the intensities of the spectra are different. The DOS values near the band edge are 0.65×10^{12} cm^{-2} eV^{-1}, 1.66×10^{12} cm^{-2} eV^{-1} and 5.36×10^{12} cm^{-2} eV^{-1} for the P3HT, PQT-12 and PQTBTz-C12, respectively. It should also be noted that the total photo-induced bulk charge carrier densities by integrating the DOS profile over the energy range of 1.85–2.2 eV are 0.83×10^{12} cm^{-2}, 1.46×10^{12} cm^{-2}

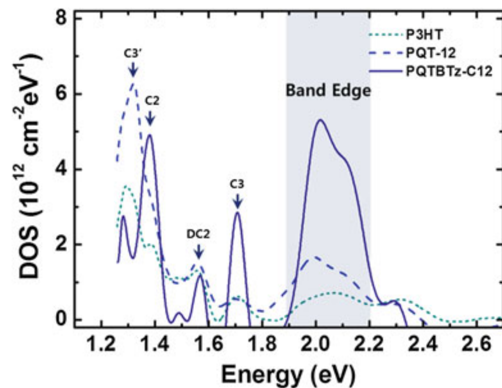


Fig. 3.14 The DOS profiles of P3HT, PQT-12 and PQTBTz-C12 extracted from the differential of $Q_e(e)$

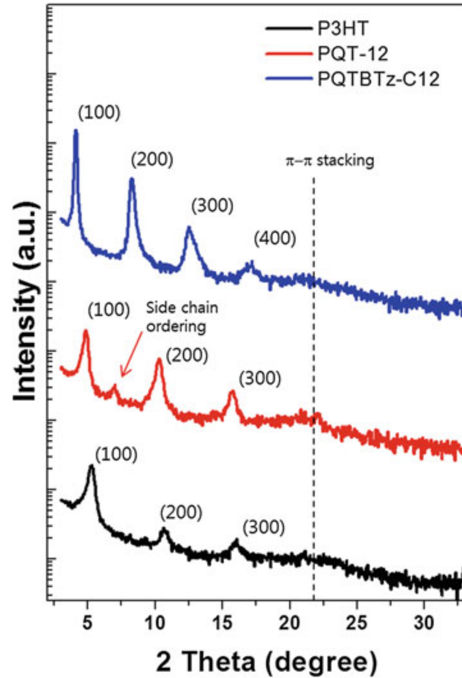


Fig. 3.15 XRD spectra of the 110 nm thick spin-coated P3HT, PQT-12 and PQTBTz-C12 polymer semiconductor films

and 2.00×10^{12} cm^{-2} for the P3HT, PQT-12 and PQTBTz-C12, respectively; the number values are quite similar to the previous reports on SiO_2–based P3HT polymer transistors [78, 79]. The numbers of integrating the DOS profile over π–π* band edge should depend on the crystalline quality because the dense packing brings more thiophene rings in the unit area.

The data from X-ray diffraction (XRD) using Cu Kα (λ = 1.5405 Å) shown in Fig. 3.15 confirm this. The PQTBTz-C12 film has high intensity with 4th peak in the (*h00*) direction, while P3HT film and PQT-12 film have only 3rd peak in the same direction. In addition, it is intriguing that the *d*-spacing difference between PQT-12 (17.0 Å) and P3HT (16.5 Å) is only 0.5 Å even though the alkyl-chain length of PQT-12 is two times longer than that of P3HT [1, 9, 10]. It means that the inter-digitation of the alkyl-side chain in the PQT-12 is more efficient than that in the P3HT and thus the PQT-12 film has more improved molecular ordering. On the one hand, the improved molecular ordering should enhance charge transport because the overlapping of p-orbital between the thiophene rings and the faced thiophene ring will increase. In fact, the mobilities of polymer semiconductors tend to increase with the numbers of integrating the DOS profile over π–π* band edge, which can also be explained with the mobility edge (ME) model [80, 81]. In the ME model, the effective mobility in the active channel is expressed as

$$\mu = \mu_0 \frac{N_{mob}}{N_{tot}}, \tag{3.8}$$

where m_0 is the mobility parameter, N_{mob} the number of mobile carriers in the $\pi-\pi^*$ band edge, which is related to the Fermi energy E_F via

$$N_{mob} = \int_{1.85}^{2.20} D(E)f(E_F, E)dE \tag{3.9}$$

with $D(E)$ the DOS at an energy E and f the Fermi–Dirac distribution function, and N_{tot} the total number of carriers in the channel given by the following equation:

$$N_{tot} = \frac{C_i|V_G - V_{Th}|}{t} = \int_{-\infty}^{\infty} D(E)f(E_F, E)dE \tag{3.10}$$

with $t \sim 1$ nm, the charge accumulation thickness. Since we assume that the intrinsic property such as m_0 is the same for the polymer semiconductors in question, in accordance with the ME model, the mobility value (0.04, 0.07, and 0.20 cm^2/Vs for the P3HT, PQT-12 and PQTBTz-C12, respectively) of our polymer transistors is proportional to the numbers of integrating the DOS profile over $\pi–\pi^*$ band edge for each polymers. Collectively, the denser inter-chain packing in the polymer semiconductor channel shows the larger number of density of states over the band edge, which resulted in the higher field-effect mobility.

3.4 Chapter Summary

As mentioned above, we conducted PECCS spectroscopy to investigate the two-dimentional polaronic structures in polymer thiophene-based crystalline-domain-forming polymer semiconductors, as well as to investigate the interfacial trap DOS in small molecule organic p- and n-channel TFTs. The PECCS spectroscopy reveals not only the $\pi–\pi^*$ absorption peaks between 2.05 and 2.45 eV but also the charge-induced absorption peaks appeared at around 1.32, 1.39, 1.58, and 1.71 eV below the p–p* absorption edge in polymer-based organic TFTs. Using PECCS, we also estimated the DOS of the polymer active channel in ORGANIC FETs and found that the denser interchain packing leads to a higher number DOS near the band edge, resulting in a higher field-effect mobility; in small molecule-based OTFTs, high intensity of DOS peaks indicates high crystalline quality of organic channels.

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Chapter 4
PECCS Measurements in Oxide FETs

Abstract Oxide FETs or thin-film transistors (TFTs) have been extensively investigated for display and many other electronic applications, since they are expected to promote advances over conventional a-Si TFTs in plastic or glass electronics maintaining low process cost. Among many other oxide channels, crystalline ZnO and amorphous oxides such as InGaZnO were adopted for mainstream devices, Since they have larger energy band gap over 3 eV, they easily contain some density of midgap states at the channel/inorganic dielectric interface. Here, we address PECCS measurements on ZnO-based TFTs in section [1] and on InGaZnO-based TFTs in the next sections of [2, 3]. In the aspects of display industry, InGaZnO TFTs become more important due to their photostability.However, the polycrystalline ZnO is the basic primitive channel material containing higher density traps at the interface with any inorganic dielectrics, being worthy of initial PECCS study.

4.1 PECCS on ZnO Based n-Channel FETs

ZnO based thin-film transistors (ZnO-TFTs) were expected to promote advances in display electronics, due to their features of low cost process and high transparency [4, 5]. The operational stabilities of such TFTs are thus important, strongly depending on the nature and density of charge traps present at the channel/dielectric interface or in the thin-film channel itself [6, 7]. In particular, the illuminated display back panel is susceptible to the charge-trap-induced instability. Therefore the characterization of these traps is critical. Despite such immediate demands, appropriate methodologies to directly analyze the interfacial properties are quite rare and conventional analysis such as photoluminescence (PL), deep-level transient spectroscopy (DLTS) and gate-bias stress techniques are rather unsatisfactory; PL is not adequate for any working thin film devices [8, 9] while DLTS and gate-bias stress techniques are limited to obtain the information on relatively shallow level traps placed a few hundred meV below the conduction

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band level (E_c) [9–11]. PECCS as a direct probe of the traps would thus be more useful than abovementioned previous techniques, since it can sensitively measure the fine density-of-states (DOS) profiles for detailed mid-gap states in the channel/dielectric interface of a working TFT device.

4.1.1 Experimental Procedures

The indium-tin-oxide (ITO)-deposited glass substrate was cleaned with acetone, methanol, and de-ionized water, in that order. The 50 nm-thin ITO S/D electrodes were patterned by using ITO etchant solution (LCE-12 K). Then 90 nm-thick ZnO films were deposited by r.f. sputtering at room-temperature (RT) through a shadow mask. For high dielectric capacitance (C_{ox}) and strength, polymer/oxide double dielectrics were employed [12] with different sequence to construct two kinds of structure as shown in Fig. 4.1a and c. To deposit the polymer dielectric layer, spin casting was performed with a 20 nm-thin poly-4-vinylphenol (PVP) [12]. Another dielectric layer of 20 nm-thin Al_2O_3 was deposited by atomic layer deposition (ALD) process at 150 °C. Total C_{ox} values for both types of double dielectric layers were identical, to be ~100 nF/cm^2 as confirmed by a capacitance–voltage (*C*–*V*) measurement. A 30 nm-thin ITO top-gate electrode (transmittance of ~80 %) was finally deposited through another shadow mask by e-beam evaporation at 150 °C under O_2 flow of 1.5 sccm. Our ZnO-TFT device thus appeared very transparent while we defined the device geometry to be 90 μm and ~6 for a nominal channel length (*L*) and a width/length (*W/L*) ratio, respectively. All electrical characterizations were carried out with a semiconductor parameter analyzer (Model HP 4155C, Agilent Technologies) in the dark and in an air ambient at RT. PECCS measurement setup includes a light source of 500 W Hg (Xe) arc lamp, a grating monochromator covering the spectral range of 254–1000 nm, and an optical fiber (core diameter of 200 μm) as an optical probe of Fig. 4.1a which guides the monochromatic photons onto the channel of our TFT device. Optical power density after the fiber was measured to be ~0.2 mW•cm^{-2}. Figure 4.1b displays a photographic view of PECCS measurement on our transparent device.

4.1.2 Results and Discussion

Figure 4.2a and b display the transfer curves of our transparent ZnO-TFTs with Al_2O_3/PVP (black curve; from Fig. 4.1c device) and PVP/Al_2O_3 (red; from Fig. 4.1a device) double layers as obtained under a drain bias (V_D) of 10 V. The device with Al_2O_3/PVP layer shows a measurable amount of hysteresis with counter clock-wise direction. Since this device has PVP layer contacting ITO gate, the injection of some positive charges from ITO gate into the PVP (or the

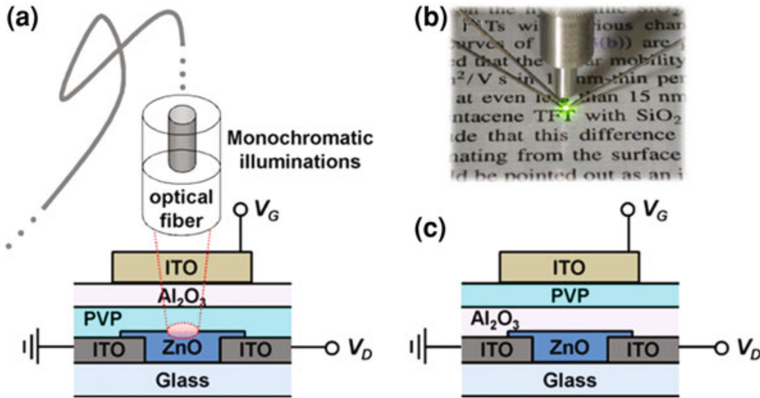

Fig. 4.1 **a** Scheme of the PECCS measurement with monochromatic illuminations on our electrically stable ZnO-TFT with PVP/Al_2O_3 dielectric layer. **b** Photographic view of the real PECCS measurement on our transparent ZnO-TFT with 550 nm illumination. **c** Schematic cross-sectional view of ZnO-TFTs with Al_2O_3/PVP double dielectric layer

extraction of electrons from PVP, equivalently) may take place and then more electron charges (resulting in higher drain current of I_D) can be drawn to the semiconductor channel that is very close to the ZnO/Al_2O_3 interface [13]. However, in the other case with PVP/Al_2O_3 double layer as dielectric, the inorganic ALD-Al_2O_3 layer is apparently more injection-resistant than the PVP polymer under the same gate bias (V_G) sweep condition. During the V_G sweep, no visible hysteresis has been observed from this case. (The saturation mobility (μ_{FET}) of the two TFTs was about the same, to be $\sim$0.15 cm^2/Vs). These stability differences between the two devices were again found from V_G stress tests. As shown in Fig. 4.2c, the initial drain current (I_{D0}) of the former device with Al_2O_3/PVP dielectric rapidly increases by two or three times within 30 s whether the device was 1 month-aged or not. (The aging was done inside a 1 Torr-vacuum desiccator.) In contrast but also as expected, the other device with PVP/Al_2O_3 double dielectric displayed only a little change of I_D during 100 s under the same bias and aging conditions, exhibiting relatively a very good bias-stability. Regardless of such a good electrical stability, it is also very necessary to investigate the photo-stability of the same device because its deep-level traps located near the channel/dielectric interface may not be activated under such an electrical stress, and also because the most probable applications of these ZnO-TFTs may be display-drivers which should meet with photon environment.

In order to evaluate the photo-stability of our electrically stable ZnO-TFT with PVP/Al_2O_3 dielectric, we performed the PECCS measurement on the device. For the photo-electric measurement, we sequentially applied mono-energetic photons onto our TFT device from low to high energy (spectral/or wavelength interval $\Delta\lambda$: 5 nm), to release the trapped charges at the channel/dielectric interface in the order from shallow- to deep-level. V_G sweep started from the channel accumulation state

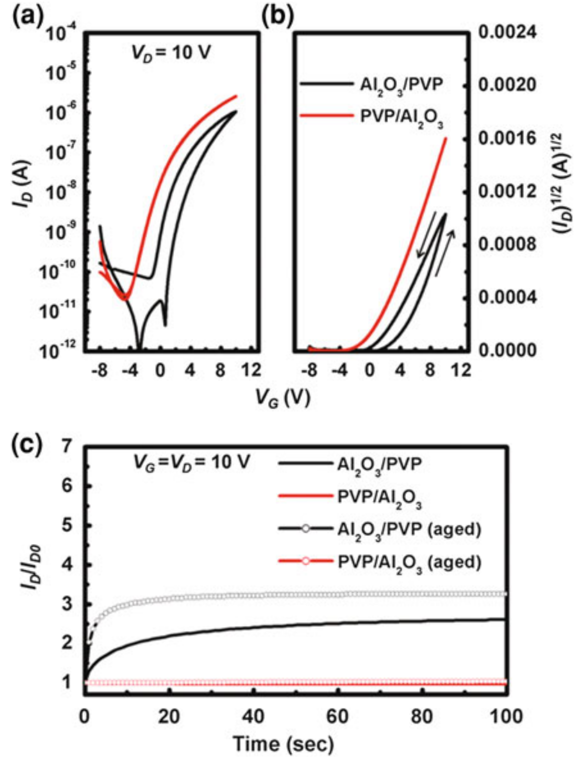

Fig. 4.2 Transfer characteristics as **a** $logI_D$ versus V_G and **b** $\sqrt{I_D}$ versus V_G plots, obtained from two different ZnO-TFTs with Al_2O_3/PVP (*solid black*) and PVP/Al_2O_3 (*solid red*) double dielectric layers. **c** Time-dependent I_D behaviors of those devices with Al_2O_3/PVP and PVP/Al_2O_3 dielectrics under $V_G = V_D = 10$ V before (*solid*) and after (*circled*) 1 month aging. Such I_D behaviors are normalized by dividing its initial current (I_{D0})

because we should initially fill up all the interfacial trap states with charge carriers prior to the photo-excitation process. Since a ZnO-TFT has n-channel, the traps would be filled with electrons (see the band diagram in Fig. 4.3b). When the photo-excitation is initiated, the trapped charge carriers are released into the E_c as indicated by the arrow. Then, ΔV_{th}, as a function of photon energy would be clearly observed from the ZnO-TFT (see the photo-induced transfer curves of Fig. 4.3a). When photons with a specific energy, ε, transmit through the gate materials to reach the channel/dielectric interface of a TFT, most of the trapped electrons in the gap states between $E_c - \varepsilon$ and E_c levels are excited to E_c in the n-channel ZnO-TFT, since the number of incident photons (order of $\sim 10^{14}$ cm^{-2} as calculated from the optical power density, $\sim$0.2 mW•cm^{-2}) is large enough compared to that of trap states, which is in the order of $\sim 10^{13}$ cm^{-2}. This means that the effective trap charge (Q_{eff}), which is mainly for the traps at the channel/dielectric interface, can be varied with photon energy, ε, and then the photo-shifted V_{th} can be represented by [6]

$$V_{th}(\varepsilon) = \phi_{ms} - \frac{Q_{eff}(\varepsilon)}{C_{ox}} + \psi_{s,\max} + \frac{Q_G}{C_{ox}} \tag{4.1}$$

with

$$Q_{eff}(\varepsilon) = q\int_{E_v}^{E_c-\varepsilon} D_{it}(E)F(E)dE + qN_b t_{ox} = q\int_{E_v}^{E_c-\varepsilon} D_{it}(E)dE + qN_b t_{ox} \tag{4.2}$$

where ϕ_{ms} is the metal-semiconductor work function difference, C_{ox} is the dielectric capacitance per unit area (F cm^{-2}, our PVP/Al_2O_3 showed ~100 nF cm^{-2}), $\psi_{s,max}$ is the potential due to band bending of the channel semiconductor, Q_G is the charge associated with dielectric band bending as induced by gate bias, N_b is the density (cm^{-3}) of bulk traps in the gate dielectric, t_{ox} is the dielectric thickness, D_{it} is the DOS at channel/dielectric interface (cm^{-2}eV^{-1}) and *F(E)* is the Fermi–Dirac distribution function whose value must be 1 for n-channel. (We assumed 0 Kelvin step function for considering *F(E)* in Eq. (4.2).) Since ϕ_{ms}, $\psi_{s,max}$, and Q_G in Eq. (4.1) are rarely changed by ε while N_b in Eq. (4.2) also hardly varies with ε, photo-induced ΔV_{th} can be analyzed by taking a derivative of Eq. (4.1) with ε, as shown below,

$$\frac{\partial V_{th}(\varepsilon)}{\partial\varepsilon} = -\frac{1}{C_{ox}}\frac{\partial Q_{eff}(\varepsilon)}{\partial\varepsilon} \tag{4.3}$$

and then by substituting Eq. (4.2) into (4.3), which now results in

$$\frac{\partial V_{th}(\varepsilon)}{\partial\varepsilon} = \frac{q}{C_{ox}} D_{it}(E_c - \varepsilon) \tag{4.4}$$

Because the bulk-trap densities in the both channel and dielectric oxide are negligible due to no significant changes in sub-threshold slope (*S*), μ_{FET} and off-state current (I_{off}) values during the photo-electric measurement, [6, 14, 15] D_{it} $(E_c\text{-}\varepsilon)$ and are determined, to be

$$D_{it}(E_c - \varepsilon) = \frac{C_{ox}}{q}\frac{\partial V_{th}(\varepsilon)}{\partial\varepsilon}, \tag{4.5}$$

where D_{it} *(Ec-ε)* is the DOS (cm^{-2}eV^{-1}) with respect to E_c.

Figure 4.4 shows the fianl DOS profile which was acquired by PECCS for the ZnO-TFT with PVP/Al_2O_3 dielectric. As shown in Fig. 4.4, we can observe a number of DOS (cm^{-2}eV^{-1}) peaks which represent individual trap energy states in our ZnO-TFT. Among the DOS peaks, several located at ~1.55, 1.68, 1.96 and 2.31 eV incredibly well matched with the theoretical deep electron trap levels calculated by Janotti et al. [16], respectively corresponding to Zn_O (+4/+3) (1.55 eV), O_{Zn} (-/2-) (1.66 eV), Zn_O (4 +/2+) (1.98 eV) and Zn_O (3 +/2+)

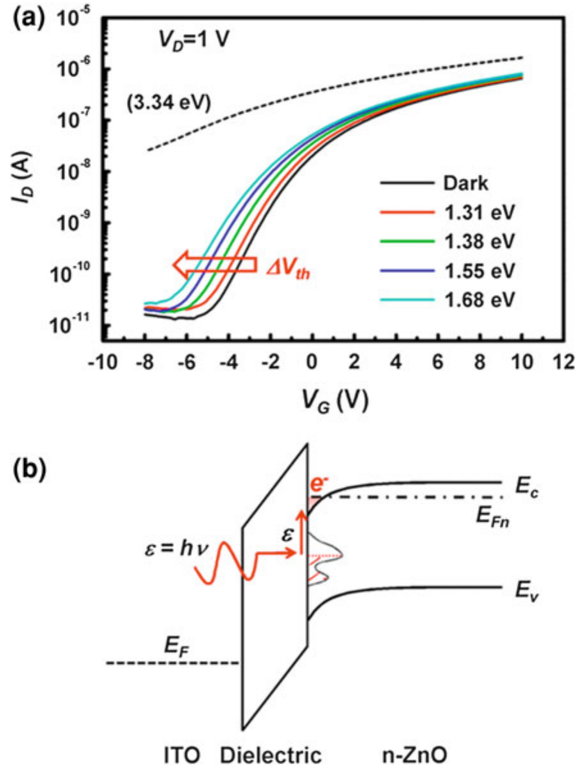

Fig. 4.3 **a** Photo-induced transfer characteristics obtained from the electrically stable ZnO-TFT with PVP/Al_2O_3 dielectric under mono-energetic photons with different energies. **b** Energy band diagram illustrates the photo-electric process details in n-channel ZnO-TFT, involving the behavior of interface trap charges under photons

(2.42 eV); they are located below the E_c of ZnO. (Here Zn_O: zinc antisite and O_{Zn}: oxygen antisite). Another peaks worthy of note are found at ~1.31 and 1.37 eV below E_c with a DOS peak intensity of 1.0×10^{13} and 5.1×10^{12} cm^{-2} eV^{-1}, respectively. These peaks are apparently too deep to be considered as an oxygen vacancy (V_O) or a zinc interstitial state (Zn_i) in ZnO because the reported values are quite shallow to be 0.1 (Zn_i) and less than at most ~1 eV (V_O) [16]. We thus regard those two peaks as the DOS of unknown interfacial traps which might be generated at ZnO/PVP interface, but there must be further computational studies.The total trap density is estimated by the integration of DOS profile, to be $\sim 10^{12}$ cm^{-2} which is a reasonable value comparable to that in the literature [17]. When the photon energy approaches to the band gap of ZnO (E_g ~3.34 eV), the DOS curve shoots up according to a dramatic ΔV_{th} increase as also shown from the dashed black curves of Fig. 4.3a. The inset of Fig. 4.4 displays an optical absorbance spectrum of ZnO/PVP/Al_2O_3 layers, which were fabricated on glass under the same experimental conditions, to be compared with the DOS profile of the real TFT device. Large absorption was observed near the E_c (or E_g) of ZnO and this result is matched to that of our PECCS experiment. However, unlike the DOS profile, the optical absorption spectra could not resolve those trap levels located at

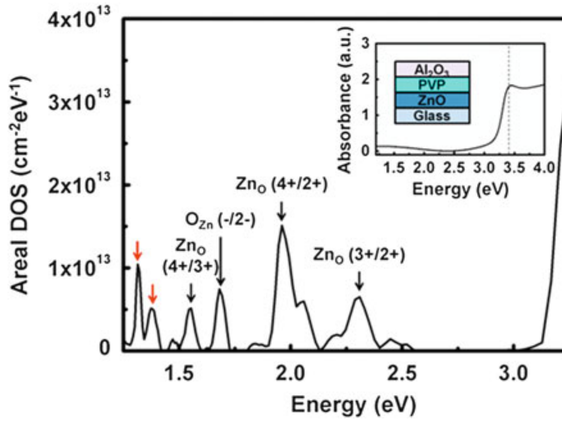

Fig. 4.4 The DOS profile for deep level interface traps in the ZnO-TFT with PVP/Al_2O_3 dielectric obtained by the PECCS measurement. (Spectral interval $\Delta\lambda$: 5 nm for mono-energetic photons) Positions of main DOS peaks are marked with *red* and *black* arrows for interfacial and native point defects, respectively. Inset shows the optical absorbance spectrum of ZnO/PVP/Al_2O_3 sample on glass substrate. (*Dashed line indicates* the E_g of ZnO, ~3.34 eV)

the ZnO/PVP interface. We thus regard that our PECCS measurements are very seneitive to the deep traps located near the dielectric/channel interface.

4.2 PECCS on Amorphous InGaZnO Based n-Channel FETs

Amorphous-InGaZnO thin-film transistors (a-IGZO-TFTs) have recently attracted a great deal of attention as driving device for large area display panels and transparent electronics, since developed [18]. For the industrialization of the a-IGZO-TFT the operational reliabilities of the device should now be secured while those mainly depend on the nature and density of charge traps present at the channel/dielectric interface or thin-film channel itself [19]. In particular, securing the photoelectric stabilities of the oxide TFTs is very critical since the oxide TFT devices have aimed at functioning as the pixel driver of display panel. Characterization methods such as capacitance-voltage measurement, optical and thermal effect analysis on the electrical property changes of devices have been introduced to find out the origin of the instabilities in a-IGZO-TFTs [20–22]. However, those measurements have always shown their limits, suggesting neither any quantitative information nor guide lines. We thus applied PECCS on our differently-processed a-IGZO TFTs, to characterize their stabilities and photo-stabilities quantifying their trap density of states (DOS), which are mainly present at the dielectric/IGZO channel interface.

4.2.1 Experimental Procedures

The structure of a-IGZO-TFTs are inverted stagger type and have an etch stopper layer on top of the semiconductor layer for protecting a-IGZO layer. Figure 4.5 shows the cross sectional and photographic plan views of the a-IGZO-TFTs that were fabricated with the width/length (W/L) ratio of 24/8 μm on the 370 × 470 mm glass substrates. Gate metal of Mo/AlNd bilayer was initially deposited on the glass substrate by DC magnetron sputtering, and then 200 nm-thick SiO_2 gate insulator was deposited by using plasma enhanced chemical vapor deposition (PECVD) processes. The 50 nm-thick a-IGZO (target composition, In:Ga:Zn = 1:1:1) layer was deposited to be an active channel by DC magnetron sputtering at room temperature. Two different DC sputtering power conditions of 1 and 3 kW for a-IGZO devices were deliberately chosen, to study the correlations between the DC power conditions and device stabilities. Etch stopper layer of SiO_2 was deposited by PECVD on the channel layer, and the source/drain (S/D) was then patterned with Mo. All the patterning processes were carried out by

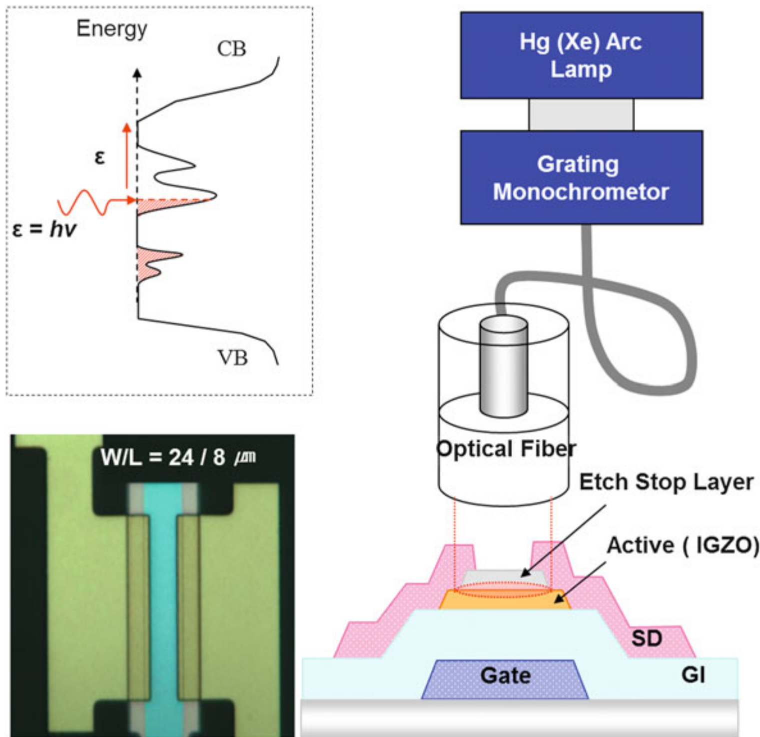

Fig. 4.5 Schematic cross-sectional and photographic plan views of our a-IGZO TFTs. Optical probing for PECCS measurements is also illustrated along with an expected scheme of photon energy-DOS diagram

photolithography that involved wet chemical etching and PECVD processes. The device annealing at 300 °C in an air ambient was performed as a final process. The drain current-gate bias (I_D–V_G) transfer characteristics and bias temperature stress (BTS) curves were measured with a semiconductor parameter analyzer (Model HP 4155C, Agilent Technologies) in the dark and in an air ambient at room temperature. Bias temperature stress ($V_{GS} = \pm$ 30 V) was applied for 3600 s at 60 °C to measure the electrical stability of our a-IGZO-TFTs. PECCS measurements were then carried out with the same electrical measurement setup, also incorporating an optical probe that uses the light source of 500 W Hg(Xe) arc lamp, a gratings monochromator covering the spectral range of 254–1000 nm, and an optical fiber (core diameter of 200 μm) as shown in Fig. 4.5. An average optical power density of all the monochromatic lights was ~0.2 mW/cm^2 as measured after the lights passed through the optical fiber. The inset of Fig. 4.1 shows a schematic energy-DOS diagram, to be obtained from PECCS measurements.

4.2.2 Results and Discussion

Figure 4.6a, b display the dark- and photo-transfer curves of a-IGZO TFTs which were prepared with DC sputtering power of 3 and 1 kW for IGZO deposition, respectively. In fact, either positive (+) or negative (−) BTS did not much change the initial behavior of high power-prepared TFT while the other device with low power-deposited IGZO showed −2 V and +7 V of V_{th} shifts in the dark transfer curve after the same (+) and (−) BTS tests, respectively. (Not shown here). However, even the device with low power-deposited IGZO did not show any V_{th} shift without the BTS. The field effect mobility (μ_{eff}) of the TFTs with high- and low-power-deposited IGZO are 7.25 cm^2/Vs and 2.81 cm^2/Vs, respectively. The mobility difference between two TFTs comes from the sputtering power as already known; a high power sputtering condition induces high indium ratio in a-IGZO channel resulting in both I_D and mobility increases [23]. In the present study, we were rather interested in the sources of the V_{th} shift observed from the low DC power-prepared TFT: deep traps near the a-IGZO/dielectric interface and their DOS. The nature of the deep traps is suspected as trapped electron that will reduce the I_D (or increase the V_{th}) when they are located near the channel interface (It is possible to consider that the deep traps are acceptor type.) [24]. In order to clarify the nature of these traps, we performed PECCS measurements with the two devices. Photo-transfer curves as initial step of PECCS were measured using many monochromatic photons (ranging from 1000–254 nm, wavelength λ interval: 5 nm), and for the transfer curves a small V_{DS} of 0.1 V (linear regime) was applied to possibly guide our trap-induced photo-I_D flow near the channel/dielectric interface [25].

According to Fig. 4.6a, the transfer curves of our high mobility device hardly change under several monochromatic photons and the change is barely observed by magnifying the curves (see the inset). This means that this device with the

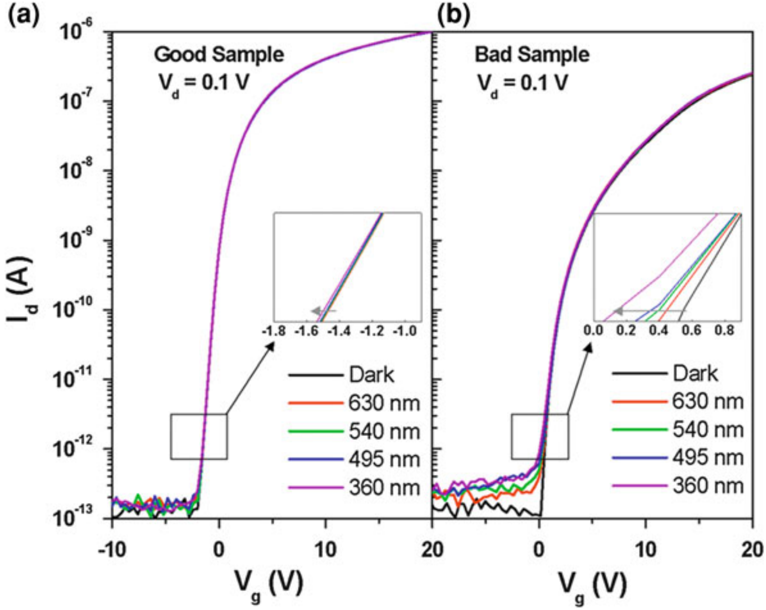

Fig. 4.6 Dark initial and photo-induced transfer curves for **a** high mobility device (Good Sample) and **b** low mobility one (Bad Sample). *Insets* show the zoom images of sub-threshold region

a-IGZO obtained by high-power DC sputtering must be quite trap-free. The photo-induced transfer curves from the low mobility device also showed only a little V_{th} shift in Fig. 4.6b but the change was quite visible toward negative bias direction if we again use the magnified observation on the curves (inset). According to the inset of Fig. 4.6b, it is likely that trapped electrons are more released by the energetic photons with their energy increases. Free charges trapped at a certain energy level are liberated by the correspondingly energetic photons and then electrically collected at the source/drain electrodes. Interestingly, this low mobility device also reveals a gradual increase of off-current with photon energy, pointing out that this TFT device contains a certain density of traps in the channel bulk region as well as at the channel/dielectric interface.

From the photo-induced transfer curve sets of the two devices, V_{th} shift with the photon energy increase was measured, and the trap DOS profiles were prepared as shown in Fig. 4.7. Equations (4.6)–(4.8) provide theoretical background of our DOS measurements,

$$V_{th}(\varepsilon) = \phi_{ms} - \frac{Q_{eff}(\varepsilon)}{C_{ox}} + \psi_{s,\max} + \frac{Q_G}{C_{ox}} \tag{4.6}$$

$$\frac{\partial V_{th}(\varepsilon)}{\partial \varepsilon} = -\frac{1}{C_{ox}} \frac{\partial Q_{eff}(\varepsilon)}{\partial \varepsilon}, \tag{4.7}$$

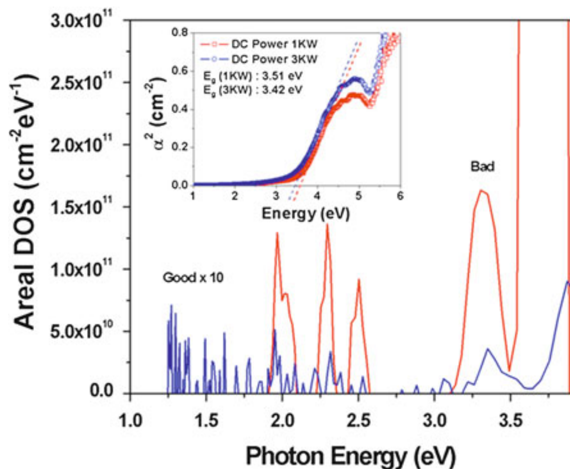

Fig. 4.7 DOS profile for deep level interface traps in the two a-IGZO TFTs obtained by PECCS measurements. Inset shows the optical absorption spectra (photon energy versus α^2) of the high and low mobility a-IGZO channel layer samples deposited on glass (50 nm)

where the photo-shifted V_{th} and effective trap charge Q_{eff}, which is mainly for the traps near the channel/dielectric interface, are the function of photon energy, ε, and Φ_{ms} is the metal–semiconductor work function difference, C_{ox} is the dielectric capacitance per unit area, $\psi_{s,max}$ is the potential due to band bending of the channel semiconductor, Q_G is the charge associated with dielectric band bending as induced by gate bias. Then, with a differential increase of photon energy, ε, we can have the Eqs. (4.7) and (4.8) that can provide the interfacial trap DOS ($cm^{-2}eV^{-1}$), $D_{it}(E_c{-}\varepsilon)$ at an energy, $E_c{-}\varepsilon$.

$$D_{it}(E_c - \varepsilon) = \frac{C_{ox}}{q}\frac{\partial V_{th}(\varepsilon)}{\partial \varepsilon}, \tag{4.8}$$

where E_c is the conduction band edge while q is an electronic charge. (More details are found elsewhere) [25]. As expected, the high mobility device did not show any significant DOS density with less than $\sim 10^{10}$ cm^{-2} eV^{-1} near the photon energies of 1.3, 2.0 and 2.3 eV. This stable device also displays small DOS peaks near 3.4 and 3.7 eV. We assign the peak at 3.4 eV as one indicating the band-to-band transition and thus assign 3.4 eV as the energy band gap (E_g), since the 3.4 eV in PECCS well matched with the E_g estimated by the optical absorption spectra of the same thin a-IGZO film as deposited on glass (see the inset where we also note that the E_g of less conductive a-IGZO is slightly higher than 3.4 eV possibly due to lower In content). As integrated with the energy in our measurement range (see Eq. (4.9) below), the total deep trap density (N_{it}) of our high mobility device was estimated to be only $\sim 6 \times 10^9$ cm^{-2}.

$$N_{it} = \int_{E_v}^{E_c-\varepsilon} D_{it}(E_c - \varepsilon)d\varepsilon, \tag{4.9}$$

where E_v is the valence band edge. Visible deep trap DOS peaks were clearly observed with the intensities of $\sim 10^{11}$ cm^{-2} eV^{-1} from the PECCS results of the low mobility device which displayed about the same E_g but with much increased DOS intensity at the energy. Three DOS peaks located at 2.0, 2.3, and 2.5 eV are similar to the peaks from ZnO-TFT samples where we assigned the DOS at 2.0 and 2.3 eV as ZnO (4+/2+) and ZnO (3+/2+) according to previous theoretical studies for defects in bulk ZnO [16, 25] (here, Zn_O: zinc anti-site and O_{Zn}: oxygen anti-site). The nature of the trap DOS at 2.5 eV was not reported yet, however, we can at least assume that the interfacial traps and their nature in a-IGZO TFT are not much different from those of crystalline ZnO-TFTs [6]. The N_{it} of this low mobility device was estimated to be $\sim 3 \times 10^{10}$ cm^{-2} which is at least 5 times higher than that of our high mobility device but is still quite low in industry standard. (Our N_{it} values were an order of magnitude lower than sub-threshold swing-estimated values, which presents maximally possible interface trap densities in TFTs) [26].

As above, we quantitatively measured the DOS profile of traps located near channel/dielectric interface in stably-working a-IGZO TFTs by PECCS. According to PECCS and BTS results, the main deep traps are regarded to have acceptor type states near the channel/dielectric interface and they are much similar to those in crystalline ZnO-TFTs. In our study, the high-power DC sputtering for a-IGZO turned out to be advantageous over the low-power sputtering in both trap density and electron mobility.

4.3 PECCS by Current–Voltage Versus Capacitance–Voltage Method on Amorphous Si and Amorphous InGaZnOTFTs

In the present study, as a similar probe for the traps, we showed another PECCS measurement technique, photon-probe capacitance–voltage (CV) measurement, which now utilizes the flat band voltage (V_{FB}) shift in CV curves of a working TFT device. While our previous PECCS measurement uses photo-induced current–voltage (IV) relation, the present method utilizes photo-induced CV curves. As interfacial charges trapped at gap state energy levels are liberated to the conduction band edge by the energetic photons (Fig. 4.8(a)), the gate voltage for channel accumulation must be lowered; the transient voltage in CV curve, V_{FB} shifts negatively and the magnitude of the shift provides us with a direct measure of the trap DOS, since the energy levels of those traps simply correspond to the photon energies.

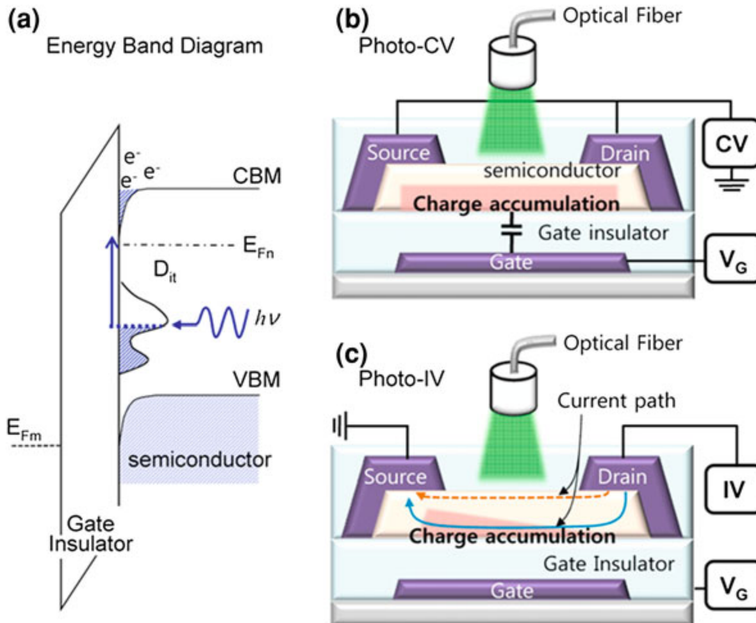

Fig. 4.8 **a** Energy band diagram to explain photo-excited charges. Measurement schemes of **b** photo-CV and **c** photo-IV methods using monochromatic illuminations on working TFTs. Unlike IV method where drain voltage is provided to collect charges, CV method uses S/D as ground

4.3.1 Experimental Procedures

The structure of a-Si TFTs was inverted stagger type using bottom gate. Figure 4.8b and c show the schematic cross sectional views of the a-Si TFT. A 400 nm-thick SiN_x gate insulator (GI) and a 170 nm-thick a-Si channel depositions were sequentially performed on the Cu/MoTi gate by plasma enhanced chemical vapor deposition (PECVD), followed by Cu/MoTi source/drain (S/D) and SiN_X passivation. As another amorphous TFT device, a-InGaZnO (IGZO) TFTs were prepared on Mo/AlNd gate, where 400 nm-thick SiO_2 was deposited as GI by PECVD and 60 nm-thin a-IGZO was subsequently patterned to be an active channel by DC magnetron sputtering. The formation of 75 nm-thick SiO_2 etch stopper and S/D layer was sequentially performed, followed by SiO_2 passivation. All I–V measurement was carried out with a semiconductor parameter analyzer (Agilent 4155C) and CV measurement was carried out with a precision LCR meter (Agilent 4284A LCR meter, 10 kHz). An average optical power density of all the monochromatic (mono-energetic) photon beams (wave length range, 350–2000 nm) in PECCS was $\sim$0.1 mW/cm^2 (photon flux $\sim 10^{14}$ cm^{-2} eV^{-1} s^{-1}) as measured after delivered through an optical fiber, as illustrated in Fig. 4.8b and c for the photo-CV and photo-IV measurements.

4.3.2 Results and Discussion

Figure 4.9a displays the photo-IV characteristics of a-Si TFT with a channel width/length (W/L) ratio of 1000/6 μm while Fig. 4.9b does the photo-CV results. The CV curves are well defined with high and low capacitance regions which respectively mean channel accumulation and depletion states. The V_{FB} of CV or V_{th} of IV curves shifted in general as the photon energy increases. However, the IV case showed a certain cross point among three photo-IV curves induced by 800, 900, 1000 nm wavelength photons, as indicated by inset of Fig. 4.9a. Likewise, it is interesting to note that the IV characteristics might be more sensitive in V_{th} shift than the CV characteristics, since the photo-IV results include large sub-threshold degradation that was caused by another source of photo current (additional drain current (I_D) induced by back channel- or channel film-trapped charges) [27]. In contrast, V_{FB} shifts in the photo-CV curves stably proceed with the photon energy increase because the photo-carriers simply generate at the channel/dielectric interface without any noise from back channel. The back channel surface is in an electrically floating state and S/D are in ground (Fig. 4.8b). Therefore, photo-excited charges near the back-channel surface are easily recombined with their original traps during CV measurements, hardly contributing to the CV

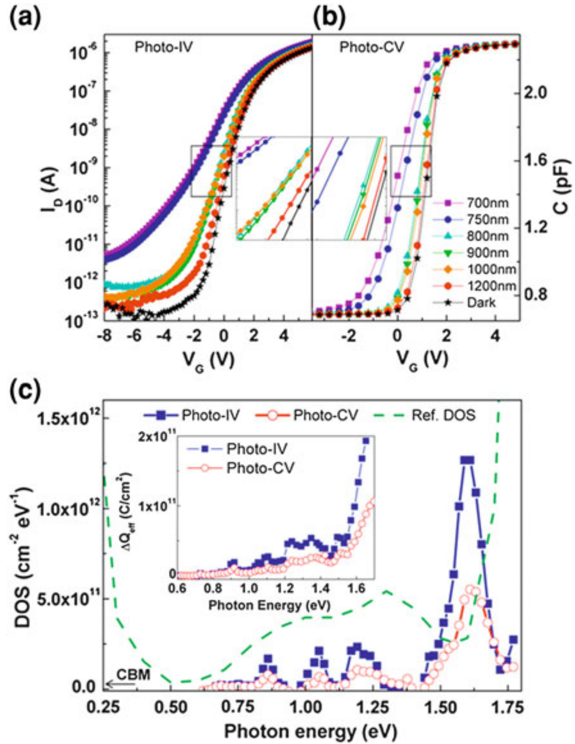

Fig. 4.9 **a** Photo-IV transfer [logI_D versus V_G] curves of our a-Si TFT with a W/L (1000/6 μm) and **b** photo-CV plots. (See the insets for magnified IV and CV features). **c** The trap DOS profiles of the a-Si TFT achieved from the IV and CV methods. The *dashed line* is a reference DOS profile, as obtained from a-Si MOS capacitor by DLTS method. The inset figure shows the ΔQ_{eff} plots as estimated by V_{th} and V_{FB} shifts.(1240/λ(nm) = ε (eV))

characteristics. Trap DOS profiles were extracted from the photo-IV (PECCS) and -CV methods, to be plotted for comparison as shown in Fig. 4.9c. For the photo-electric measurement, we sequentially applied mono-energetic photons onto our TFT device from low to high energy to release the trapped interface charges in the order from shallow- to deep-level. V_G sweep started from the channel accumulation state because we should initially fill up all the interfacial trap states with charge carriers prior to the photo-excitation process in both IV and CV methods. In the CV measurement, theoretical V_{FB} can be described as below [28].

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{x_{ox}} \frac{x}{x_{ox}} \rho(x) dx, \tag{4.10}$$

where Φ_{MS} is the metal-semiconductor work function difference, C_{ox} is the dielectric capacitance per unit area, Q_f is the fixed charge at the channel/dielectric interface, $\rho(x)$ is the density of bulk traps in the gate dielectric, x_{ox} is the dielectric thickness. Φ_{MS} and the third term for charge integration in bulk dielectric are rarely changed by photon energy. Only the second term regarding the interfacial charge effectively varies with photon energy ε, since the interfacial charges are excited by photons; the fixed charge Q_f thus changes to $Q_{eff}(\varepsilon)$ [non-excited gap states still filled with charges at the semiconductor-dielectric interface under illumination] and photo-induced V_{FB} (or V_{th}) shift can be expressed as below

$$\Delta V_{FB}(\varepsilon) = -\frac{|\Delta Q_{eff}(\varepsilon)|}{C_{ox}}; \text{ here } \Delta Q_{eff}(\varepsilon) = Q_f - Q_{eff}(\varepsilon) \tag{4.11}$$

$$Q_{eff}(\varepsilon) = q \int_{VBM}^{CBM-\varepsilon} D_{it}(\varepsilon) d\varepsilon, \tag{4.12}$$

where q is an electronic charge, CBM and VBM mean conduction band minimum and valence band maximum, respectively. Then, the density of state (DOS), D_{it}, has the relation with V_{FB}.

$$D_{it}(CBM - \varepsilon) = \frac{C_{ox}}{q} \frac{\partial V_{FB}(\varepsilon)}{\partial \varepsilon} \tag{4.13}$$

The inset figure in Fig. 4.9c shows $\Delta Q_{eff}(\varepsilon)$ plotted as the function of ε.

According to both DOS and $\Delta Q_{eff}(\varepsilon)$ plots, the photo-IV method (PECCS) show more sensitive profiles than those of photo-CV although the DOS profiles obtained from the two techniques are apparently similar. It is thus suspected that our photo-IV might involve photocurrent effects from back channel which may sensitively deliver some photo-excited trap charges to drain, adding more intensities to interfacial trap DOS profiles. The back channel photocurrent in the inverted stagger type TFTs is particularly important under thin-film depletion state because illuminated photons may find trapped carriers at the back channel interface where

gate/drain voltage-induced electric field exists. Therefore, it is somewhat understandable that the cross point among the three transfer curves under 800, 900, 1000 nm wavelength photon was observed under a depletion bias state (inset of Fig. 4.9a). Photo-CV measurement would hardly be influenced by such back channel effects in view of its intrinsic character. We also show a previously reported DOS profile as a reference, to be compared with our results [29]. According to the reference profile obtained from deep level transient spectroscopy (DLTS), the onset (or band tail) of a-Si energy band gap appears at 1.7 eV and broad band of trap DOS is shown from 0.75 to 1.5 eV while our results show the onset at 1.5 eV with discrete DOS peaks at 0.8, 1.05 and 1.2 eV. This difference may be attributed to the fact that the two a-Si films are basically different each other; our device was an a-Si TFT while the reference device was a metal-oxide-semiconductor (MOS) capacitor with a thin a-Si. Despite such difference, those results are regarded still comparable each other in respects of DOS energy level and DOS intensities.

Another DOS measurement was implemented for a-IGZO TFTs as shown in the Fig. 4.10a–c. In these oxide TFTs which appear very photo-stable, CV curve shift was not noticed until photon energies approach to band tail regime energy (~400 nm, 3.0 eV) while a maximum photo-induced voltage shift in IV curve

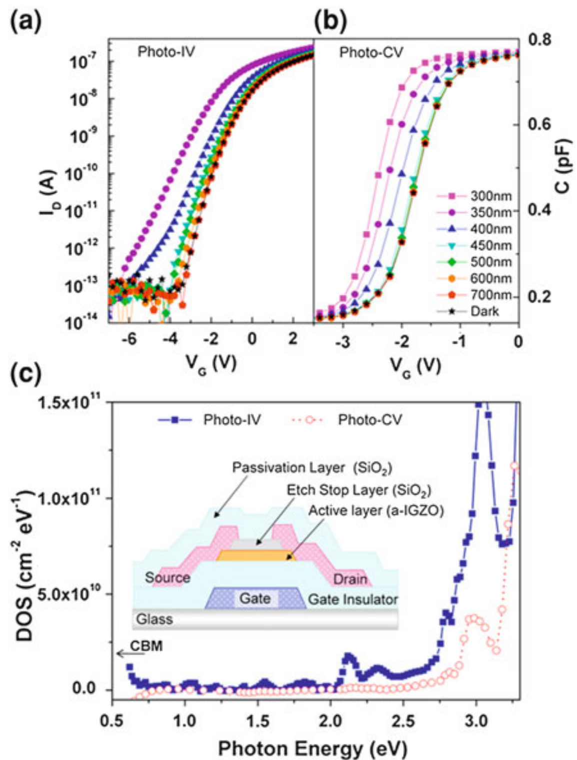

Fig. 4.10 **a** Photo-induced transfer characteristics [logI_D versus V_G] plots of an a-IGZO TFT with 50/6 μm W/L ratio and **b** photo-CV characteristics [C versus V_G] plots (from another a-IGZO TFT with 200/6 μm W/L ratio). **c** The trap DOS profiles of the a-IGZO TFTs achieved from IV to CV methods. The *inset* figure shows a schematic cross section of a-IGZO TFT

was as much as 0.6 V at 450 nm. So, it is again reflected that DOS analysis by photo-IV might be more sensitive than that by photo-CV which only senses the charge state of the channel/dielectric interface. Indeed, in the case of a-IGZO TFT, even the photo-IV measured the trap DOS of only $\sim 10^{10}$ cm^{-2} eV^{-1} (at 2.1, 2.3, and 2.8 eV), which is an order of magnitude lower than those of a-Si TFT (2×10^{11} cm^{-2} eV^{-1}). This also helps to understand why the photo-CV method could not clearly resolve the DOS peaks except the arrow-indicated small DOS shoulder at 2.8 eV.

As mentioned above, we quantitatively measured the interfacial trap DOS of typical amorphous TFTs by photo-CV measurement, comparing the profiles with those by photo-IV method. Our photo-CV results turned out to mainly present the trap DOS of channel/dielectric interface. Compared to the DLTS results where the trap DOS broadly ranges from 0.75–1.5 eV, our photo-CV results show discrete DOS peaks at 0.8, 1.05 and 1.2 eV. We conclude that our photo-CV method could be another valuable technique well compensating previously developed photo-IV method.

4.4 PECCS to Observe Interface- and Bulk-Originated Trap Densities in Amorphous InGaZnOTFTs

The previous PECCS study predominantly addresses the density-of-states (DOS) of channel/dielectric interface and near-interface traps, not the DOS from bulk-type traps which are away from the interface. We here report our observation on the respective DOS peaks of the interface- and bulk-origin traps by utilizing top-gate IGZO-TFTs with opaque and transparent source/drain (S/D) electrodes, in notion that the visible photons can penetrate the transparent S/D to reach and excite the trapped charges at the bulk IGZO region.

4.4.1 Experimental Procedures

For manufacturing an IGZO TFT, a substrate of corning glass (Eagle XG) was cleaned for 10 min in each acetone, methyl alcohol, and de-ionized water in an ultra-sonicator. For deposition and patterning of RF sputtered active IGZO channel, photo-lithography was carried out. First, we coated the Lift-Off-Layer solution (LOL: LOL 2000, Micro Chemical) and thermally cured the LOL coated substrate at 115 °C for 2 min. Then, we coated photo-resist (PR : SPR 3612, Micro Chemical) on LOL layer, and cure the PR layer at 95 °C for 2 min, too. Using a photo mask-aligner, we exposed the sample to ultraviolet (UV) light for 4 s. The samples were subsequently developed with metal-ion-free (MIF) developer solution. After that, a 60 nm-thick IGZO was deposited on the glass substrate by RF

magnetron sputtering under the following conditions: Ar/O ratio of 20 sccm: 1 sccm and 100 W sputtering power. A lift-off process was then followed. For the lift-off process, we used acetone and lift-off layer (LOL) remover solvents. Subsequently the IGZO pattern was thermally annealed in a furnace at 300 °C under ambient condition for 1 h. After annealing, employing the same photo lithographic processes (described above) we defined the source/drain (S/D) pattern, depositing Au/Al bi-layer as S/D electrode for one set of devices while depositing ITO S/D for the other set; we used DC sputtering system and then carried out the lift-off process as described earlier. After making S/D electrodes, 60 nm-thick Al_2O_3 was deposited as gate dielectric by atomic layer deposition (ALD) system. Finally, for making transparent top gate we again utilized the photolithography and 50 nm-thick ITO. For photo-excited charge-collection spectroscopy (PECCS) for trap DOS analysis, we applied mono-energetic photons onto our working TFTs from low to high energies, as shown in Fig. 4.11a, b. (More details can be found elsewhere [25]. The optical microscopy images of opaque and transparent S/D TFTs are shown in Fig. 4.11c, d, respectively. A fully transparent TFT array image is also demonstrated on our university emblem [Fig 4.11e]. As the first step for PECCS, transistor transfer curve (drain current-gate voltage: I_D–V_G) sweep was

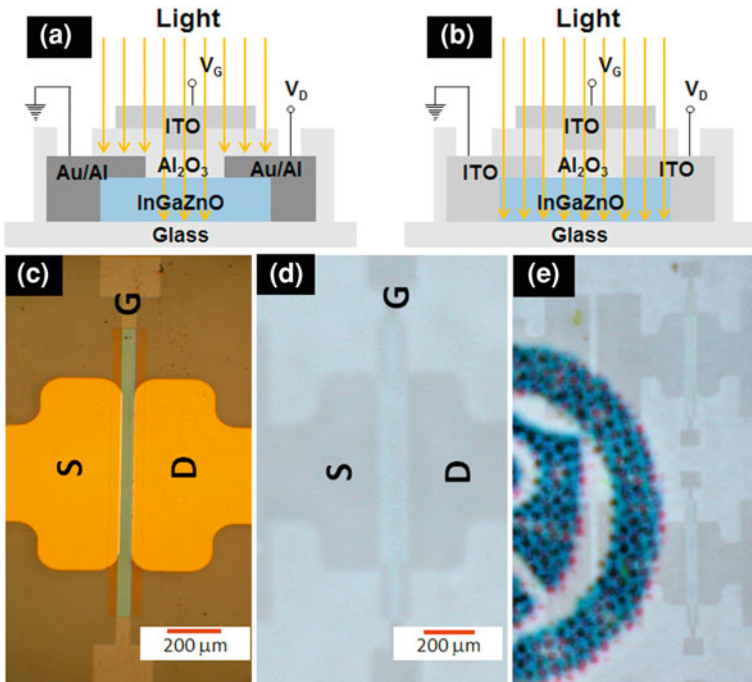

Fig. 4.11 Device cross section schematics illustrating the illuminated area of IGZO TFTs with **a** opaque and **b** transparent S/D. Optical microscope images of the **c** opaque and **d** transparent TFTs. **e** Image of transparent TFTs on university emblem

implemented under mono-energetic photons, starting with a V_G from channel accumulation to depletion state because we should initially fill up all the interfacial trap states with charge carriers prior to the photo-excitation.

4.4.2 Results and Discussion

Figure 4.12a, b show photo-induced transfer curves, indicating the threshold voltage (V_{th}) shift by photons that illuminate the TFT with opaque S/D and with transparent S/D, respectively. According to the curves of Fig. 4.12a for opaque S/D TFT, the V_{th} is shifted toward negative voltage with the photon energy increase, but little change of sub-threshold slope (SS) and off-current was noted until ~2.95 eV which may be the starting point of tail states near the band gap (~3.15 eV) of IGZO [15, 24]. In contrast, the SS and off-current of transparent device appear ready to increase at a low photon energy of 2.18 eV while its

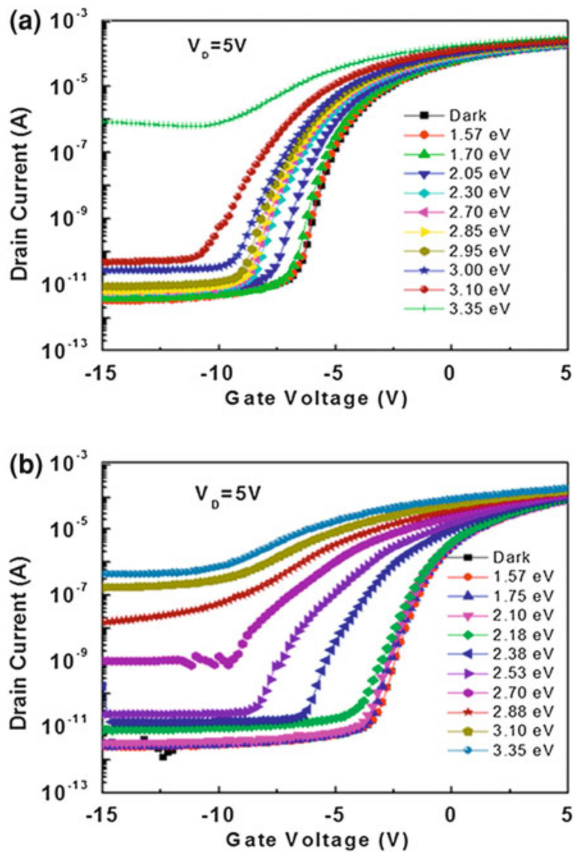

Fig. 4.12 Photo-transfer curves of the IGZO TFTs with **a** opaque and **b** transparent S/D electrode

photo-induced transfer characteristics was very stable before 2.18 eV. As the photon energy increases over 2.18 eV, the V_{th} is much shifted and the off-current of transparent device significantly jumps up at visible photon energy of 2.70 eV, which is much below the band gap. We attribute this off-current increase to a fact that the bulk region below the transparent ITO drain is strongly influenced by visible photons and electric field (by 5 V drain voltage). Understandably, the photo I_D–V_G behaviour of our opaque S/D TFT in Fig. 4.12a does evidence that the trapped charges at or near the IGZO channel/Al_2O_3 dielectric interface hardly contribute to the off-current increase under visible photons but only do to the V_{th} shift. It is thus obvious that bulk-trapped charges are excited and collected to the drain from the light-exposed active area under ITO S/D in transparent device, elevating the off-current level.

The trap DOS profiles were prepared as shown in Fig. 4.13a and b. Equations (4.14)–(4.16) provide theoretical back-ground of our DOS measurements [6],

$$V_{th}(\varepsilon) = \phi_{ms} - \frac{Q_{eff}(\varepsilon)}{C_{ox}} + \psi_{s,\max} + \frac{Q_G}{C_{ox}} \tag{4.14}$$

$$\frac{\partial V_{th}(\varepsilon)}{\partial \varepsilon} = -\frac{1}{C_{ox}} \frac{\partial Q_{eff}(\varepsilon)}{\partial \varepsilon}, \tag{4.15}$$

where the photo-shifted V_{th} and effective trap charge Q_{eff}, which is mainly for the traps near the channel/dielectric interface, are the function of photon energy, ε, and

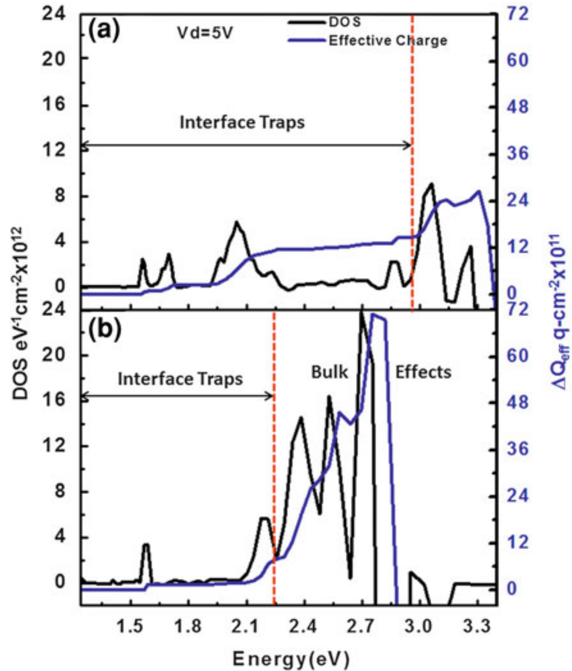

Fig. 4.13 Effective charge density (ΔQ_{eff}) and Density-of-states (DOS) profiles of IGZO-TFTs with **a** opaque and **b** transparent S/D

Φ_{ms} is the metal-semiconductor work function difference, C_{ox} is the dielectric capacitance per unit area, $\psi_{s,max}$ is the potential due to band bending of the channel semiconductor, Q_G is the charge associated with dielectric band bending as induced by gate bias. Then, with a differential increase of photon energy, ε, we can have the Eqs. (4.15) and (4.16) that can provide the interfacial trap DOS ($cm^{-2}eV^{-1}$), $D_{it}(E_c-\varepsilon)$ at an energy, $E_c-\varepsilon$.

$$D_{it}(E_c-\varepsilon)=\frac{C_{ox}}{q}\frac{\partial V_{FB}(\varepsilon)}{\partial\varepsilon}, \tag{4.16}$$

where E_c is the conduction band edge while q is an electronic charge. The DOS and ΔQ_{eff} profiles of opaque S/D TFT appear similar to those of previous reports on bottom-gate IGZO-TFTs, of which PECCS analysis showed interfacial trap DOS peaks at 1.7, 2.1, and 2.9 eV although their intensities were two orders of magnitude lower (since those were imported from industry) [2, 3]. The profiles of our transparent device are very different as expected from transfer curves. From low photon energy to ~2.18 eV, the DOS and ΔQ_{eff} profiles appear even superior to those of opaque device, indicating that this device may have small interfacial trap densities until 2.18 eV. However, over 2.18 eV the trap profiles show incomparably higher trap densities due to the bulk-origin traps below ITO S/D; although this high energy range profile may not be valid any more since Eqs. 4.1 and 4.2 cannot accept the bulk-origin traps in its genuine form, we used the equations to plot DOS curves, just to analyse the bulk trap energy levels. Unlike the opaque S/D TFT, the transparent device showed large extra DOS peaks at 2.4, 2.55, and 2.7 eV, which originate from various types of oxygen vacancies in bulk IGZO. The two DOS peaks at 2.4 and 2.7 eV are similar to Zn or O vacancy (V_{Zn}, V_O)-related traps in bulk ZnO [16, 24]. We thus regard that the bulk-trap effects can be distinguished from those of interface traps, using the transparent IGZO-TFTs under PECCS analysis. (Note the dashed vertical lines to separate interface- and bulk-origin trap levels in DOS plots in Fig. 4.12b).

4.5 Chapter Summary

We have fabricated two types of amorphous IGZO TFTs with transparent and opaque S/D on glass substrate, to measure their trap DOS profiles using PECCS. The DOS of the opaque S/D TFT mainly showed interfacial traps while the DOS of fully transparent TFT showed interface traps in a low photon energy regime but mainly bulk-origin traps in high energy over 2.18 eV, so that we might observe the both effects distinguished each other. We also quantitatively measured the interfacial trap DOS of typical amorphous TFTs by photo-CV measurement, comparing the profiles with those by photo-IV method. Our photo-CV results turned out to similarly present the trap DOS of channel/dielectric interface, which were shown

by photo-IV PECCS on polycrystalline ZnO- and amorphous IGZO-TFTs. We conclude that our photo-CV method could be another valuable technique well compensating the photo-IV PECCS method.

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Chapter 5
PECCS Measurements in Nanostructure FETs

Abstract Interfacial trap densities or DOS profiles in nano structure FETs with nano wire (NW) or nano sheet active layer have hardly been investigated due to such difficulties that the measurements would face: how to fabricate and probe the nano FETs. Fortunately, our PECCS using an optical fiber is an appropriate and probably the only method to probe for the nano materials and nano devices. So, in this special section we introduce our PECCS-adopting trap DOS results and band gap-determining study from top-gate ZnO NW FETs and MoS_2 nano sheet FETs [1], respectively.

5.1 PECCS on ZnO Nanowire-Based n-Channel FETs

Nanowire (NW)-based field-effect transistors (FETs) have been extensively studied [2–5] mostly in the form of bottom-gate FETs [6–8] on SiO_2/Si substrates, while some of NW-FETs have been fabricated with a top-gate [9–11] for more practical applications for future nano-electronics. In either bottom- or top-gate NW-FETs, the trap density-of-states (DOS) at the interface between NW and dielectric should be accurately determined as it indicates the photo- or electric-stability of NW devices. However, information on the trap DOS of NW-FETs is largely inaccessible, primarily because it is very difficult to quantitatively measure the interfacial trap DOS of NW-FETs with any existing methods. Here, we adopt an appropriate method, photo-excited charge-collection spectroscopy (PECCS) [12–14] which employs monochromatic photon probes on the gate of working transistors to measure the interfacial DOS of NW-FETs. Correspondingly, our NW-FETs were equipped with top-gate electrodes of indium-tin-oxide (ITO), transparent to monochromatic photons in the range from the visible to ultraviolet (UV), so that their electrical transfer curves can be modulated by different photon energies. As a model FET for the present photon-probe measurement, we have used ZnO NW-FETs, a potential candidate for electronics and optoelectronics [15–17] applications due to its wide band gap [18, 19] and easiness for ohmic

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contact [20]. Our ZnO NW-FET with a 100 nm-thin wire channel displayed highly sensitive threshold voltage (V_{th}) shifts under monochromatic visible photons while a reference FET with a thin-film channel showed much less sensitive reaction with the photo-induced V_{th} shift observed from respective photo-transfer curves, the interfacial trap DOS located below the conduction band minimum of ZnO was for the first time quantitatively measured; the energy levels of main trap DOS peaks appeared at 545 nm (2.3 eV), 460 nm (2.7 eV), and 430 nm (2.9 eV), with their intensities over 3×10^{12} eV^{-1} cm^{-2}. Based on this information, we can apply to highly efficient green and blue detection from our ZnO NW transistors with a transparent gate, which simultaneously exhibited sensitive UV detection as previously reported in literature [21–24].

5.1.1 Experimental Procedures

ZnO nanowires were synthesized by carbon-thermal reduction method with gold (Au) nanoparticle catalysts (which were already prepared on sapphire substrate in a tube furnace). To synthesize the ZnO nanowires with a certain diameter, average 80 nm diameter Au particles were used. The source (ZnO/C mixture) was loaded in an Al_2O_3 (alumina) boat, which was set at the center of the tube furnace. In order to achieve the ZnO nanowire growth, the chemical vapor deposition on the Au nano particles was performed at 1037 K for 30 min under flow of Ar (100 sccm) working as a carrier gas. The synthesized ZnO nano wires were transferred from the sapphire substrate to the glass substrate by using a drop-and-dry method. A combination of photolithography and lift-off processes were used to fabricate Ti/Au (50 nm/50 nm) source (S) and drain (D) electrodes while the electrodes were deposited by DC sputtering system. In order to form a top-gate FET, 30 nm-thick Al_2O_3 layer was deposited on by atomic layer deposition system (ALD). Finally, again utilizing photolithography a transparent indium tin oxide (ITO) (50 nm) gate electrode was deposited by DC sputtering system. The FET channel length was 5 μm. Our ZnO-based NW-FET with an Al_2O_3 dielectric and an ITO top-gate is shown in the schematic device cross section and top-view optical micrograph of Fig. 5.1a, c, respectively. Scanning electron microscopy (SEM) image was also taken from our fabricated device (Fig. 5.1b) to estimate the thickness or diameter of our ZnO NW, even though the image appears somewhat unclear due to charging effects from the 30 nm-thin Al_2O_3 over layer. The NW thickness estimated from SEM was around 150 nm but actually must be smaller ($\sim$100 nm) if subtracting the over layer thickness. For fabricating the reference ZnO thin-film transistor (TFT) a 20 nm-thin film of ZnO was deposited by atomic layer deposition system on glass substrate, the S/D of Al was deposited by thermal evaporator and a 30 nm Al_2O_3 layer was deposited using ALD system and finally 50 nm thin ITO gate was deposited using DC sputtering system. The channel length of the TFT is 50 μm and width 1000 μm (Fig. 5.1d, e for the images of reference ZnO TFT.

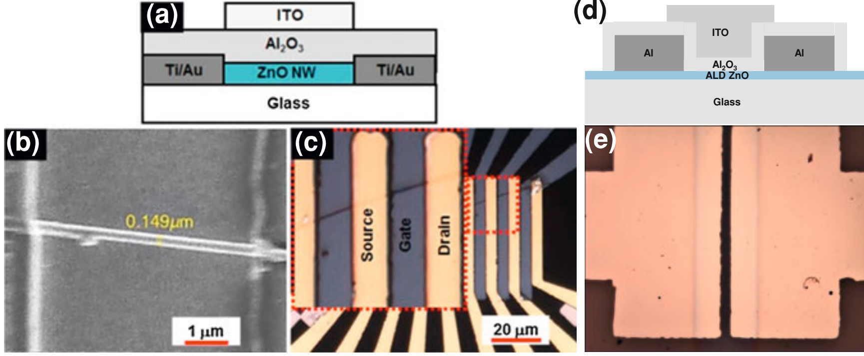

Fig. 5.1 **a** Schematic of transparent top-gate ZnO NW-FET on glass substrate **b** Scanning Electron Microscopy (SEM) image of ZnO nanowire FET showing the size of ZnO nanowire with 30 nm Al_2O_3 capping (NW size ~100 nm) **c** Optical microscope image of ZnO NW-FET **d** Schematic cross-section and **e** Optical microscopic plan view images of transparent top-gate ZnO (20 nm) TFT with 30 nm ALD Al_2O_3 gate insulator fabricated on glass substrate

PECCS measurements were implemented with the setup shown in Fig. 5.2a. For the photon-probed electric measurement, we sequentially applied mono-energetic photons onto our NW-FET from low to high energies, to release the trapped charges at the channel/dielectric interface in the order from shallow- to deep-levels (as shown in the schematic band diagram of Fig. 5.2b). The gate voltage (V_G) sweep started from the channel accumulation state because we should initially fill up all the interfacial trap states with charge carriers prior to the photo-excitation. Similar setup and implementations are found from our previous works on TFTs [12–14]. The main point of the PECCS measurements is a photo-induced shift of the flat band voltage (V_{FB}) [which would contribute to the same amount of threshold voltage (V_{th}) shift], as described below and Fig. 5.2c where

$$V_{FB} = \phi_{ms} - \frac{Q_f}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{x_{ox}} \frac{x}{x_{ox}} \rho(x) dx \tag{5.1}$$

Here Φ_{MS} is the metal-semiconductor work function difference, C_{ox} is the dielectric capacitance per unit area (F cm^{-2}), Q_f is the fixed charge per unit area at the channel/dielectric interface (Coul cm^{-2}), $\rho(x)$ is the density (# cm^{-3}) of bulk traps in the gate dielectric, and x_{ox} is the dielectric thickness. Since Φ_{MS} and dielectric-charge integration term are rather insensitive to incoming photons while only Q_f effectively changes with photon energies, the Eq. (5.1) can be rewritten as

$$V_{FB} = \phi_{ms} - \frac{Q_{eff}(\varepsilon)}{C_{ox}} - \frac{1}{C_{ox}} \int_0^{x_{ox}} \frac{x}{x_{ox}} \rho(x) dx, \tag{5.2}$$

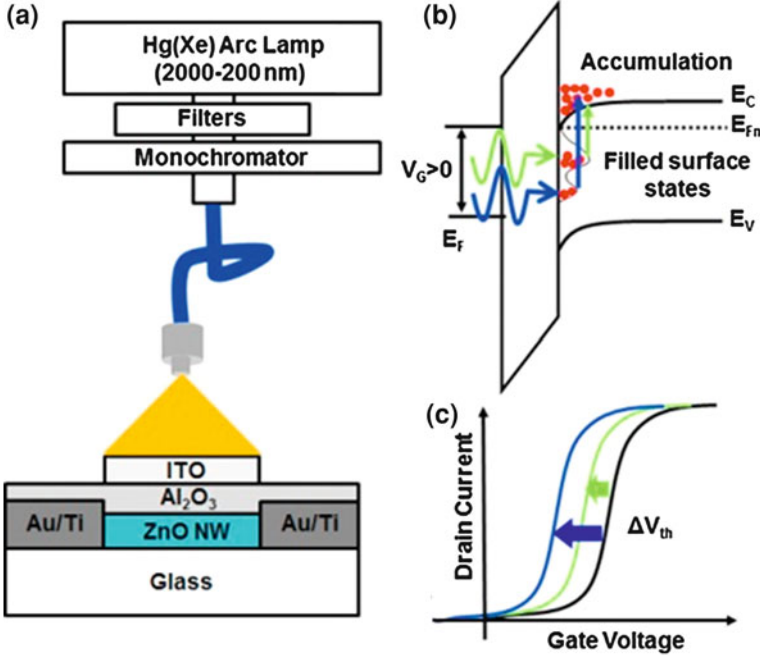

Fig. 5.2 **a** Photo-excited charge collection spectroscopy (PECCS) measurement setup with Hg(Xe) arc lamp (2000–200 nm), optical filters (NIR-VIS-UV), gratings monochromator and optical fiber (200 μm diameter) Optical power intensity was $\sim$0.1 mW/cm^2 in average for all the spectral photons. **b** Band diagram of ZnO nanowire under accumulation mode with surface states filled with electrons (filled *red circles* represent e$^-$) **c** Illustration of V_{th} shift under photons of different energies

where $\frac{Q_{eff}(\varepsilon)}{C_{ox}} = q\int_{VBM}^{CBM-\varepsilon} D_{it}(\varepsilon)d\varepsilon$ as a new form of Q_f (here, CBM and VBM indicate the conduction band minimum and valence band maximum, respectively). Then, the trap density of state (DOS), D_{it} is related to ΔV_{FB} (same as ΔV_{th}), as illustrated in Fig. 5.2b where

$$D_{it}(CBM-\varepsilon) = \frac{C_{ox}}{q}\frac{\partial V_{FB}(\varepsilon)}{\partial\varepsilon} \tag{5.3}$$

5.1.2 Results and Discussion

Based on the series of photo-induced transfer (drain current-gate voltage: I_D–V_G at a drain voltage of $V_D = 0.1$ V) characteristics of our NW-FET which are shown in Fig. 5.3a, we calculate $\Delta Q_{eff}(\varepsilon)$ as $C_{ox}.\Delta V_{th}(\varepsilon)$ and plot it to extract D_{it}, by

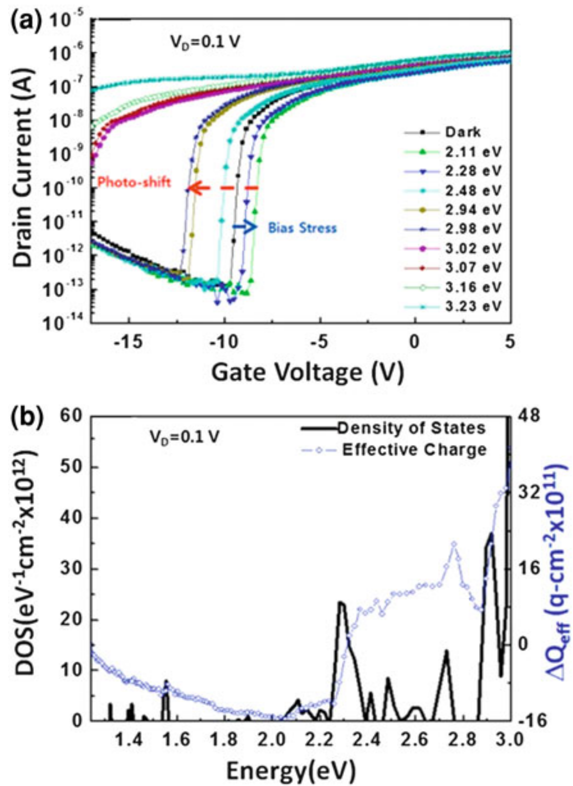

Fig. 5.3 **a** Photo-induced transfer curves showing the V_{th} shift of ZnO NW-FET ata drain voltage $V_D = 0.1$ V. **b** Density of states (DOS) (*black*) and effective interface charge modulation (*blue*) spectra obtained from ZnO NW-FET with 30 nm-thin top Al_2O_3 under photons of different energies

differentiating $\Delta Q_{eff}(\varepsilon)$ with photon energy ε (see Fig. 5.3b). According to Fig. 5.3a, our NW-FET has an excellent sub-threshold swing (SS) of less than $\sim$0.12 V/dec and a high on/off I_D ratio of $\sim 10^7$ in the dark (a maximum linear mobility of our device was 57 cm^2/Vs. But the V_{th} shifts to the negative side under light illumination as indicated by a long arrow because trapped charges are liberated by energetic photons (however, also see the short arrow indicating that under the low energy range photons the V_{th} initially moves to the positive side because of persistent bias-stress-induced trapping of electrons at the channel/ dielectric interface.

Due to the bias-stress-induced effects, the ΔQ_{eff} (ε) plot shows an initial negative shift up to 2.1 eV of photon energy in Fig. 5.3b, since the low energy photons cannot liberate the charges trapped at the deep levels). Our device nicely maintains its SS value and off-state I_D current even under the illumination up to a photon energy of 2.98 eV, and it is interesting to note that slightly higher energy (3.02 eV) photons cause sudden jump in I_D. Since the energy bandgap of crystalline ZnO is known to be 3.24–3.3 eV [25, 26], the energies of 3.02 or 3.06 eV cannot be the bandgap energy but could be an onset point of the band tail of NW ZnO channels. The trap DOS profile in Fig. 5.3b displays the main trap levels at 2.3, 2.7, and 2.9 eV along with their peak intensities of the order of 10^{13}/eV cm^2.

Those charge traps are believed to be mostly located near the ZnO NW/Al_2O_3 dielectric interface in view of the fact that SS and off-state I_D level were well maintained under visible illumination with almost the same values as those in the dark. On the other hand, the charge trap DOS above 3.02 eV must have included the bulk effects, in which the off-state I_D and SS significantly increase according to the band-to-band electron–hole generation in the bulk NW under a depletion state (off-state). Such discussion on the bulk and interfacial traps was previously admitted to report (in Chapter 1) and we again confirmed the change of off-I_D and SS due to the bulk trap charges from amorphous InGaZnO thin-film transistors. Almost the same plot of trap DOS was obtained at an increased V_D (= 1 V) as shown in Fig. 5.4a, b. The accumulated effective trap charge density, ΔQ_{eff}, was around 4.5×10^{12} q/cm^2 (q is the electronic charge), which was about the same as that of Fig. 5.3b, while the DOS values at 2.3, 2.7 and 2.9 eV range from 2.0 to 5.5×10^{13}/cm^2 eV (which are slightly higher than those observed in Fig. 5.3b). The two of the DOS peaks at 2.3 and 2.7 eV are assigned to Zn or O vacancy (V_{Zn}, V_O)-related traps [27–29] concentrated on the surface of ZnO NW [29–31] and, in particular, the 2.4–2.5 eV [28, 32] feature is known as the defect level causing green-emission photo luminescence in both bulk and NW single crystal ZnO. On one hand, our reference ZnO TFT with the same 30 nm-thin ALD dielectric and transparent top-gate (photos of Fig. 5.1d) displayed a similar V_{th} shift behaviour of photo-transfer curves but with little bias-stress effects as shown in Fig. 5.4c and d when V_D (= 5 V) was applied on the reference TFT to be compared with ZnO NW FETs. It also showed a sudden increase in off-state I_D with specific photon energy of 3.03 eV. However, its V_{th} shift is less notable than that of NW-FETs in general, and hence the total charge induced by photo-induced de-trapping appears three times smaller ($\sim 1.1 \times 10^{12}$ q/cm^2) while the DOS peak intensities become an order of magnitude smaller than those of NW devices as plotted in Fig. 5.4d. [We also applied lower V_D's of 0.1 and 1 V, since such conditions are more similar to those for ZnO NW FET, only confirming almost the same DOS profiles as the case of 5 V (see Fig. 5.4b)]. This means that our NW-FET must be much more photo-sensitive than ZnO TFTs whereas it may also be less stable under the gate bias stress. Since according to the literature ZnO NW intrinsically contains higher surface trap densities [29, 30] than thick wires or bulk films, our results are understandable.

5.2 PECCS Measurements for the Thickness-Modulated Bandgap of MoS_2 Nanosheets

Graphene exhibits a high carrier mobility (μ) over 100,000 cm^2/Vs, but it also reveals considerable limitations in regards to real device applications, due to an intrinsic difficulty caused by its small bandgap (E_g) [33–37]. In fact, the E_g of graphene turned out to be less than 200 meV [38, 39]; so, graphene could hardly

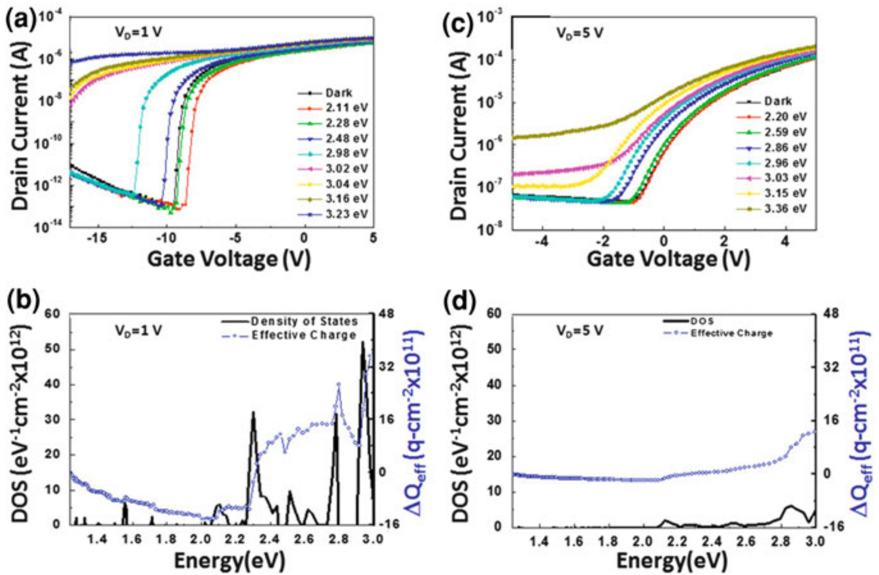

Fig. 5.4 **a** Transfer curves of ZnO NW-FET showing the photo-induced V_{th} shift at a drain voltage $V_D = 1$ V and **b** density of states (DOS) (*black*) and effective interface charge modulation (*blue*) spectra. **c** Photo-induced transfer curves of ALD-ZnO TFT with 30 nm-thin ALD Al_2O_3, as obtained at a drain voltage $V_D = 1$ V **d** Density of states (DOS) profile (*black*) and effective charge modulation (*blue*) results from ZnO TFT were displayed for comparison with (**b**)

be used for switching circuits or photo-detecting devices which need clearly defined on-and-off states. Molybdenum disulfide (MoS_2) layers very recently appeared as an alternative nano sheet material that may overcome the drawbacks of grapheme [40–43]. Bulk MoS_2 is known to have an indirect bandgap of ~1.2 eV, but the few angstrom-thin single-layered MoS_2 has recently been reported to exhibit a direct bandgap of 1.8 eV [43–48]. In fact, the E_g change of MoS_2 with thickness has previously been forecasted by theoretical estimations [49–51]. According to recent reports, a few-layered MoS_2 displayed light absorption and luminescence capabilities, enabling a photo-transistor operation [48, 52]. In this section, we fabricated a transparent top-gate photo-transistor with single-, double-, and triple-layer MoS_2 nanosheets, which was respectively analyzed by photo-electric probing as equipped with a patterned transparent gate electrode on a top of 50 nm-thin oxide dielectric [53]. According to our photo-electric probing results from the working nanosheet transistors, single-layer MoS_2 has a significant energy bandgap of 1.82 eV, while those with double- and triple-layer MoS_2 showed reduced values of 1.65 and 1.35 eV, respectively. We thus regard that our PECCS technique is quite promising to measure the bandgap of nano sheets which play an as active semiconductor layer of an FET.

5.2.1 Experimental Procedures

A surface-cleaned 285 nm-thick SiO_2/p^{++} -Si wafer was chosen as the substrate for our n-type MoS_2 nanosheet transistor with Au source/drain (S/D) electrodes, since 285 nm was reported as an optimal thickness to identify few-layer dichalcogenide [54]. Indeed, each exfoliated MoS_2 flake showed a distinctive optical contrast with thinner flakes exhibiting a lower optical density, which enabled fast screening of few-layered flakes under an optical microscope. Even though other exfoliated flakes exist around our single-layer MoS_2, as shown in the optical microscopy image of Fig. 5.5a for transistor top view, our nano-sheet-transistors operated well. Our MoS_2 nanosheet flakes were ~ 10 μm in one side, so that a long 5 μm channel was available for our device (W/L ratio was ~ 1). In Fig. 5.5b, Raman spectra obtained from three samples were respectively assigned to single-, double-, and triple-layered MoS_2 flakes spanning $\sim 5 \times 5$ μm^2. As shown by the previous report, the frequency difference between E^1_{2g} and A_{1g}, the two prominent Raman-active modes of 2H-MoS_2 crystals, decreases stepwise with the decreasing number of layers [55]. The inter-peak separation or frequency difference for the thinnest flake in Fig. 5.5b is 18.0 ± 1.0 cm^{-1},which is in excellent agreement with that for single-layer MoS_2 [55, 56]. (The thickness of monolayer MoS_2 was measured by previous researchers, to be ~ 0.65 nm [43].) Confirming the layer number of exfoliated flakes by Raman spectra, we respectively selected MoS_2 nanosheetsas the channel of our photo-transistors. Figure 5.5c illustrates the 3 dimensional (3D) scheme of our transparent top-gate photo-transistor with MoS_2 nanosheetand atomic-layer-deposited (ALD) 50 nm-thin Al_2O_3.

5.2.2 Results and Discussion

Figure 5.6a–c display the drain current-gate voltage (I_D–V_G) transfer characteristics of our top-gate nano sheet transistors. Their on/off current ratio was higher than 10^7 for the single- and double-layer MoS_2 nanosheet transistors, and was $\sim 10^6$ for the triple-layer transistor. The linear mobility μ_{lin} was respectively estimated to be 80, 27, and 10 cm^2/Vs as maximum values for single-, double, and triple-layer nano sheets, when it was plotted as a function of V_G (respective insets) based on the following equations: $g_m(V_G) = dI_D/dV_G$ (trans conductance) and $\mu_{lin} = (g_m/C_{ox}V_D) * (L/W)$, where C_{ox} and V_D are dielectric capacitance and drain voltage, respectively.

The sub-threshold swing (SS) of our single-layer MoS_2 transistor was ~ 300 mV/dec while it increases (degrades) with the total layer number. The μ_{lin} and SS values of our top-gate transistor with single-layer nano sheet trail the world record values of previously reported transistors [43], but are much superior to the values from double- and triple-layer MoS_2 transistors. According to the output (drain current-drain voltage; I_D–V_D) characteristics of our nanosheet

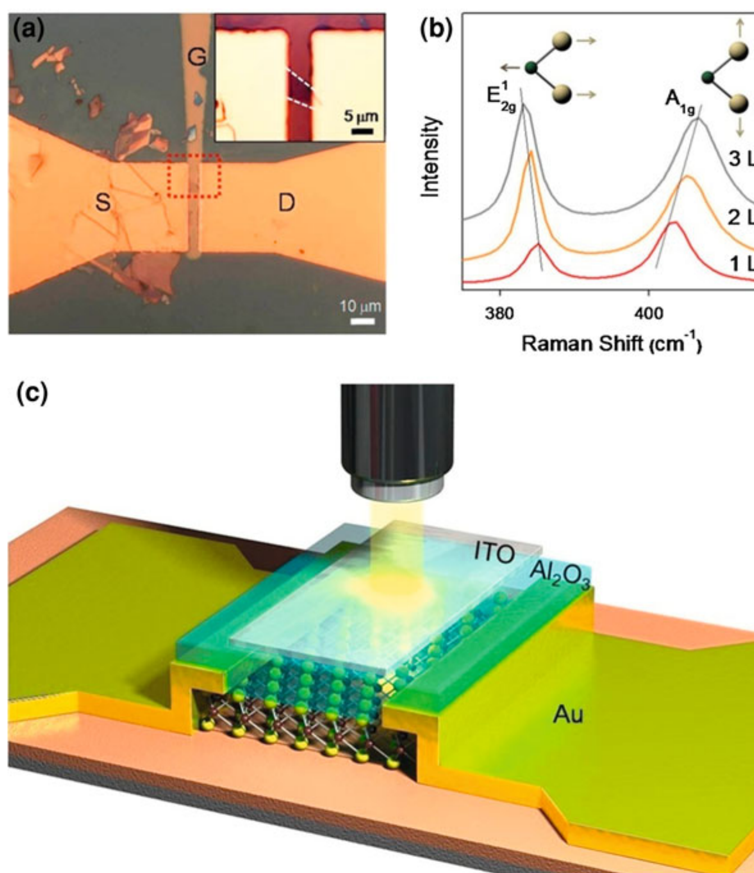

Fig. 5.5 **a** Optical image of the single-layer MoS_2-based top-gate transistor. The inset photograph shows a zoomed image of Au S/D electrodes, ITO top-gate, and exfoliated MoS_2. **b** Raman spectra of single-, double-, and triple-layer MoS_2. The inset image shows atomic displacements of the two Raman-active modes: E_{2g^1} and A_{1g}. **c** Schematic 3-D view of single-layer transistor with hexagonal structure MoS_2nanosheet, 50 nm-thick Al_2O_3 dielectric and ITO top-gate under monochromatic light

transistors (Fig. 5.6d–f), the source/drain contacts of our nanosheet transistors are almost ohmic with respect to Au regardless of their thickness (see the respective insets). However, the linear I_D behavior was only maintained with single- and double-layered MoS_2 transistors while the relatively thick triple-layer transistor showed slightly saturated I_D curves, probably due to the increase of thickness-direction scattering and some loss of dielectric screening, both of which cause the nanosheet to deviate from its low dimensional properties such as high mobility and linear I_D characteristics [57–59].

Figure 5.7a–c display the photo-induced transfer curves of our transparent top-gate nanosheet transistors, on which monochromatic red ($\lambda = 680$ nm; photon

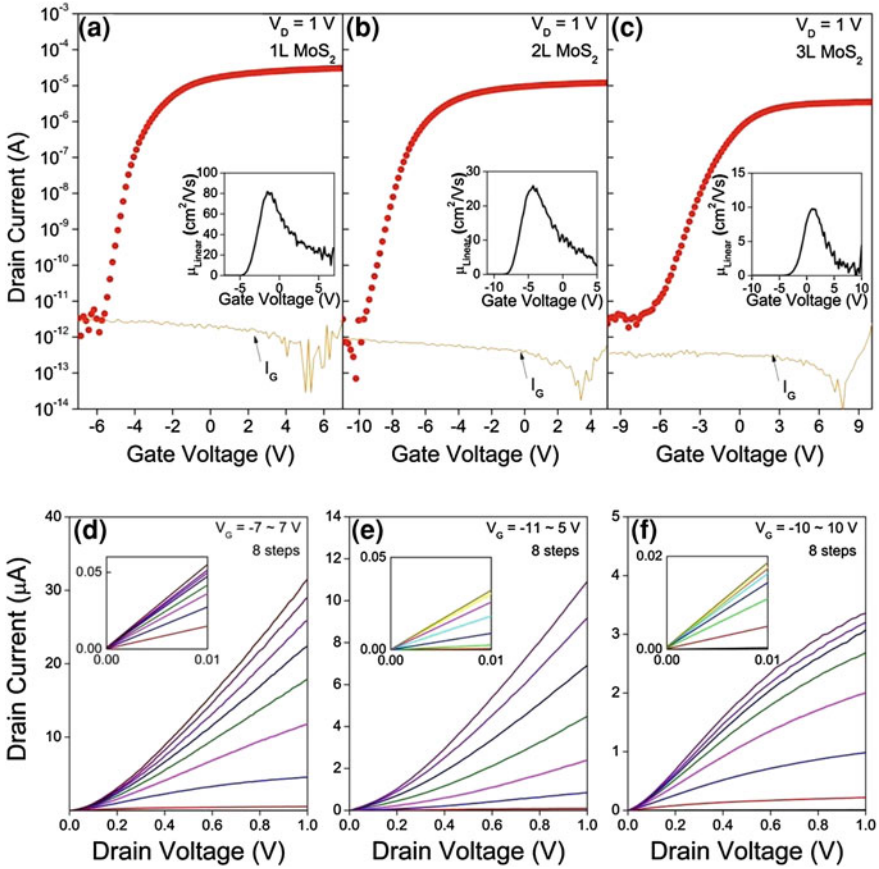

Fig. 5.6 The transfer curves of top-gate transistors with **a** single-, **b** double-, and **c** triple-layer MoS_2. Measurements were performed at $V_D = 1$ V and I_G means gate leakage current. Respective inset curves show V_G-dependent linear mobility plots. I_D-V_D output curves of **d** single-, **e** double-, and **f** triple-layer MoS_2-based transistors. Respective insets show an almost ohmic contact behavior between Au S/D and MoS_2nanosheet

energy $\varepsilon \sim 1.82$ eV), green ($\lambda = 550$ nm), and ultraviolet (UV; $\lambda = 365$ nm) lights were applied. The average illumination intensity was controlled to be $\sim$0.1 mW/cm^2 for all the wavelength photons probing on our devices. The single-layer MoS_2 transistor hardly responds to red light while the other two nanosheet transistors show quite good photo-responses to the red. Green and UV lights were well detected by all the nanosheet transistors regardless of their total layer number. Since the red light was not efficiently detected by the single-layer MoS_2 transistor, causing little threshold voltage (V_{th}) shift or photo current, we regard that the single-layer MoS_2 has an optical energy gap higher than or equivalent to 1.82 eV, and thus performed a photoelectric probing experiments on our nanosheet transistors using more than 50 serial monochromatic photon beams

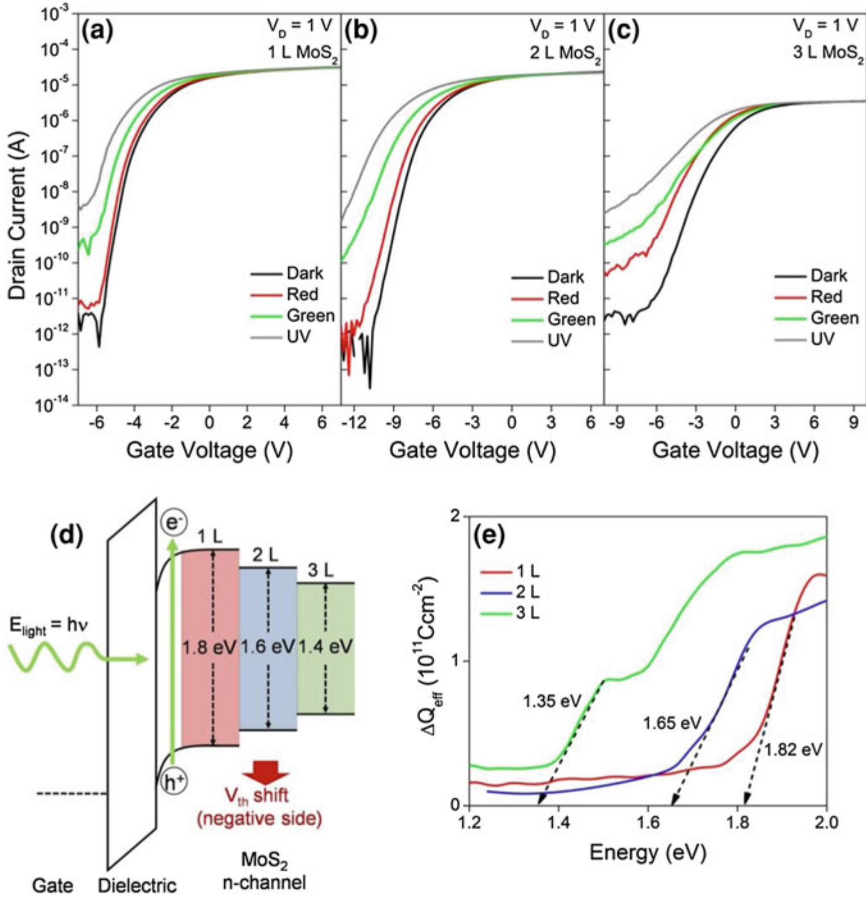

Fig. 5.7 The photo-induced transfer curves of respective top-gate transistors with **a** single-, **b** double-, and **c** triple-layer MoS_2 under monochromatic red, green, and UV lights. **d** The schematic band diagrams of ITO (gate)/Al_2O_3 (dielectric)/single (1L)-, double (2L)-, triple (3L)-layer MoS_2 (n-channel) under the light ($E_{light} = h\nu$) illustrate the photo-electric effects for band gap measurements. **e** Photon energy-dependent ΔQ_{eff} plots indicate the approximate optical energy gaps, to be 1.35, 1.65, and 1.82 eV for triple-, double-, and single-layer MoS_2nanosheets, respectively

ranging from low 1.2 to high 2.0 eV in energy, to measure their optical energy gap [53]. Based on the series of photo-induced transfer characteristics of our nanosheet transistors (acquired at a drain voltage of $V_D = 1$ V), we measured the series of photo-induced threshold voltage shift $\Delta V_{th}(\varepsilon)$ and plotted $\Delta Q_{eff}(\varepsilon)$ [$= C_{ox} \Delta V_{th}(\varepsilon)$] with respect to the photon energy, ε. Regarding any trap density small at the interface between MoS_2 and Al_2O_3 dielectric since our MoS_2 layer surface has few dangling bonds in fact [43], we can expect that a considerable ΔV_{th} is only observed with the photon energy higher than the optical energy gaps of respective

nanosheets as illustrated with their schematic band diagrams within a ITO/Al_2O_3/MoS_2 structure in Fig. 5.7d. According to the plots of Fig. 5.7e, the approximate optical energy gaps are found to be 1.35, 1.65, and 1.82 eV for triple-, double-, and single-layer MoS_2 nanosheets, respectively, while little ΔV_{th} is observed below 1.35 eV indicating small interface trap density. It means that the band gaps are thickness-modulated, and comparable results were also recently reported from the photoconductivity measurement of the single- and double-layer MoS_2 nanosheets [48]. We now understand why the red light detection was so marginal in our single-layer nanosheet transistor, where the largest slope in the plot of Fig. 5.7e is also noticed at the band-to-band transition onset (1.82 eV) as an indicator of direct gap character [48].

Such photo-response was again observed in a dynamic way over a 5 s interval for light-switching with the top-gate transistors. According to the time domain plot of Fig. 5.8a–c, the red light response increases with the total layer number; the triple-layer MoS_2nanosheet transistor appeared to show the largest dynamic photo-gain under the red light switching. These photocurrent dynamics were measured under respectively different off-state V_G conditions for the three MoS_2 transistors, based on the transfer curves in Fig. 5.7a–c.

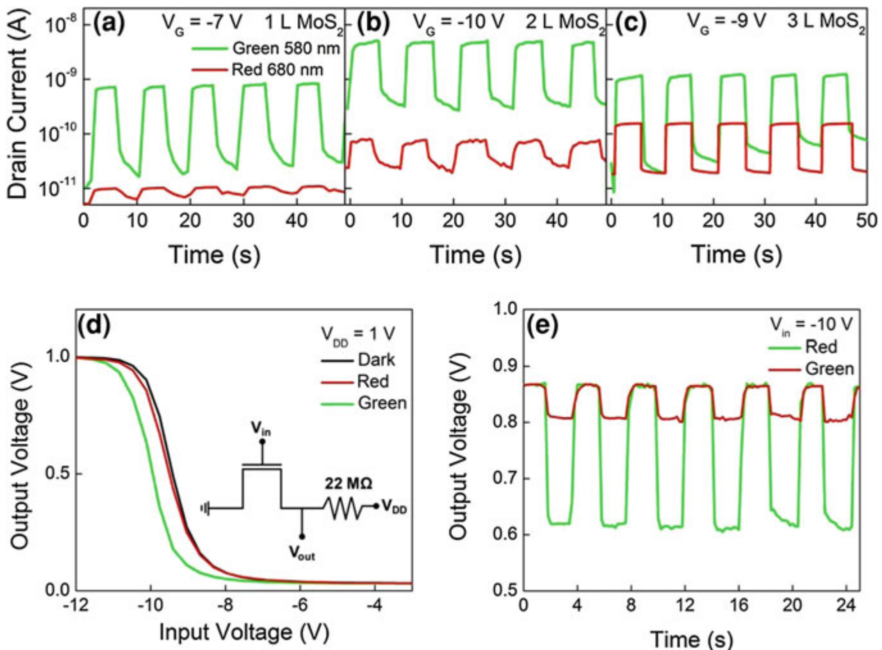

Fig. 5.8 Respective photocurrent dynamics of **a** single-, **b** double-, and **c** triple-layer MoS_2-based top-gate transistors under monochromatic red and green lights. **d** Dark and photo-induced VTC curves of our photo-inverter composed of serially connected 22 MΩ resistor and double-layer MoS_2 transistor (see the *inset for the circuit*). **e** Voltage dynamics of the resistive-type photo-inverter under monochromatic red and green lights

On the one hand, the green detection appears quite the same regardless of the layer number while the average response time (average of 80 % rise and fall) of single-, double-, and triple-layer MoS_2 phototransistors was respectively observed to be 1.5, 1, and ~0.3 s. In falling behavior, an approximate exponential decay was observed. As a representative for voltage dynamics, the double-layer MoS_2 nanosheet transistor among the three devices was selected, to form a photo-inverter with a serially connected 22 MΩ resistor (inset of Fig. 5.8d). According to the voltage transfer curves (VTCs) of Fig. 5.8d, the voltage shift by green light is as large as 0.7 V while the shift by red is minimal to be only less than 0.1 V. In Fig. 5.8e, the voltage dynamics of the photo-inverter was displayed; under the conditions of 1 V supply voltage (V_{DD}) and 2 s on-and-off light intervals, the photo-induced voltage gain of 0.26 V was achieved by green light while the red resulted in only 0.06 V. The signal voltage for the red light would increase with the triple-layer nanosheet transistor due to its reduced optical energy gap.

5.3 Chapter Summary

We have fabricated transparent top-gate ZnO NW-FET on glass substrates and quantitatively measured its trap DOS profile at the dielectric/ZnO NW interface. Our photo-excited charge collection spectroscopy (PECCS) does show much higher intensities of interfacial trap DOS in NW-FETs than in the reference ZnO-TFT, due to the high surface defect density in ZnO NW. With the DOS information that the low energy DOS peaks were mainly located near 2.3 eV below conduction band minimum, we may utilize the NW-FET as a highly sensitive photo-detector for green, blue, violet, and UV light. Besides nanowire FETs, we have also fabricated the top-gate photo-transistors based on single-, double- and triple-layer MoS_2 nanosheet. According to our photo-electric probing technique on working transistors with the nanosheets, single-layer MoS_2 has a significant energy bandgap of 1.82 eV, while those of double- and triple-layer MoS_2 showed 1.65 and 1.35 eV, respectively. For such nanostructure semiconductor channels, PECCS would be the only way to characterize their interface trap DOS and the bandgap information by PECCS would be an important useful byproduct.

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Chapter 6
Summary and Limiting Factors of PECCS

So far, through the previous 5 chapters, we have introduced the mechanisms and applications of our photo-electric probing methodology, PECCS to quantitatively measure the interfacial trap DOS of organic, oxide, and nanostructure channel FETs. In the case of p- and n-channel organic FETs, the PECCS plot demonstrates the interface trap DOS peaks and HOMO-LUMO peaks as well, while in the polycrystalline ZnO and amorphous InGaZnO TFTs electron trap DOS profiles were shown below their respective bandgaps ($\sim$3.2 eV). Nanowire ZnO FET displays quite unstable behavior during the initial gate bias sweeps for PECCS, showing a large amount of fifth shift from green illumination of 2.3 eV on due to high density traps at the single crystalline ZnO NW/oxide dielectric interface. Besides the interfacial trap DOS measurements, our PECCS method can measure a bandgap of nanosheet semiconductor such as MoS_2 layers. We thus conclude that the PECCS would be a strong tool to characterize the interface trap DOS of any working FETs and also to measure bandgap of semiconductor active layer of the FETs. However, along with abovementioned versatility, researchers may again take their heeds of the following several points that the PECCS owns;

1. Gate bias stress effects during measurements: PECCS involves a continuous gate bias sweep process for transfer curves under illumination. The gate bias sweep may cause the interface more unstable and may increase the trap DOS even during the measurements.
2. Photon intensity problems: If the photon power density is too large, it may cause photo-induced defects at the interface or in the bulk active semiconductor film. If the photon power is too small, it falls short and is not enough to excite all the trap DOS. However, our arc lamp showed enough photon power density in the useful measurement ranges from 300–2000 nm.
3. Photon energy limit: The PECCS method is generally useful for only large bandgap semiconductors in TFTs, since 2000 nm wavelength ($\sim$0.65 eV) is the longest in spectrally available range of our lamp. If the semiconductor active layer has a smaller energy gap than 0.65 eV, photon-probing is not feasible.

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4. Mainly interfacial traps are measured but a little portion of bulk traps may be included in our trap DOS estimation. Since almost the same SS and off-state current are maintained during our photo-probe measurements in general, the bulk trap involvement could be ignored. However, if the SS and off-level are noticeably changed during PECCS, the bulk trapped charges which are located away from the interface are included in the trap DOS estimation.
5. PECCS in organic FETs can not only assess the trap DOS but also the channel crystalline quality (the degree of ordered arrangement in polymer); since organic semiconductor channels have discontinuous quantized states below and above HOMO–LUMO gap, any LUMO level has a certain limited number states and charges at its own state. If the channel has good crystalline quality, the HOMO-LUMO peaks by PECCS gets large representing that it has a large number of states where charge carriers reside.

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