Chapter 10
Development of a Bottom-up Compact Model for Intel®'s High-K 45 nm MOSFET

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Abstract MOSFETs models have been critical components for evaluation of devices design and technology. These models face the challenge of being scalable to match the available semiconductor technologies. For the 45 nm MOSFET production, dielectric and metal gates were integrated. With new high dielectric materials and thinner oxide layers, new physics effects emerged that were not considered or integrated into the early models used in circuit simulators. Here an analytical model for 45 nm MOSFETs is presented. The model includes Short Channel Effects (Channel Length Modulation, the threshold voltage variation and carriers velocity saturation). The Drain-Source current and voltage equations derived from the model are implemented as a circuit device in SPICE 3F5. A comparison between the experimental data provided by the manufacturer and the simulation results obtained with the developed model integrating the technological and electrical parameters published by Intel®, demonstrates good agreement between both sets of data.

Keywords Compact · High-K · Model · MOSFET · Short channel effects · SPICE

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10.1 Introduction

The semiconductor industry has continuously increased the density of transistors on a chip, successfully reducing their physical dimensions. This trend, predicted by Moore's Law [1], has imposed challenges on device modeling, which is an essential tool to simulate the operation of Integrated Circuit (IC) prior to the fabrication process. One of the main challenges of device modeling is to describe the behavior of nanometer scaled Metal Oxide Semiconductor Field Effect Transistors (MOSFETs).

Table 10.1 summarizes the state of the art of compact models developed for SPICE:

The behaviour of a MOSFET in an electrical circuit has been studied using circuit simulators. The *Simulation Program with Integrated Circuits Emphasis* SPICE, is an example of them.

From the table it can be observed that:

- There is a high complexity involved on recently developed compact models
- Models have been strongly focused on Silicon dioxide

The complexity arises from the top-down approach focusing on the application rather than on the electrical transport properties on the device. The models above studied, do have a challenge to include others dielectric materials beyond SiO_2. An example of high dielectric materials is the hafnium dioxide HfO_2. This chapter describes a methodology proposed to build a compact model based on the transport properties at nanoscale, aiming to integrate the outputs of analytical equations into ABM blocks to simulate the output of a basic circuit topology (half-wave rectifier).

10.2 Field Effect Transistors State of the Art

Emergent novel structures of Field Effect Transistors (FET) were investigated prior developing the model, both in research (R) and production (P) stages. Table 10.1 summarize the structures reported by the ITRS in 2009. The Table 10.2 intends to review three key parameters: gate length and description and the structures power dissipation.

Intel®'s 45 nm High-k MOSFET is selected as the focused of the model given the barriers to keep the high number of transistors on a single chip: dissipated power and sacrificing device performance (thin SiO_2 layers affect the transistors leakage current and speed) [10]. The target model aims to integrate and understand the short channel effects and to keep the compatibility with one of the most widely used IC simulation language: SPICE.

It can also be observed that the devices in production involve new materials different form the conventional CMOS devices materials. Among the available High-κ dielectric materials (such as ZnO_2) Hafnium dioxide is considered to be a promise for replacing the silicon dioxide due to the high dielectric constant, good thermal stability in direct contact with silicon substrates and low leakage current [6].

Table 10.1 State of the art of compact models for MOSFETs. Information gathered from [2–5]

Model	Year of release	Modeled dielectric material	Gate length lower limit	Complexity level
Level-1	1972	SiO_2	50 μm	Low
Level-2	1975	SiO_2	10 μm	Low
Level-3	1978	SiO_2	2 μm	Medium
BSIM1	1985	SiO_2	1 μm	Low
BSIM2	1990	SiO_2	200 nm	Medium
BSIM3	1995	SiO_2	50 nm	High
BSIM4.4	2009	SiO_2, with EOT derived from Silicon dioxide	10 nm	High

Table 10.2 Novel FET structures and some of their main parameters

Device	FinFET	GAA-FET	High-K	VRG-FET	TriGate
Stage	R	R	P	R	P
L_G (nm)	20	30	45	50	60
Gate description	Si segment (*Fin*) divides the polysilicon gate	Metal gate that surrounds the cannel	High-κ metal gate	dielectric	HfO_2 gate dielectric grown by Atomic Layer
Deposition	Three effective gates, sources and drains				
Dissipated power (W)	44 n	30 n	61 n	39 μ	72 μ
References	[7]	[8]	[9, 10]	[11]	[12, 13]

GAA-FET Gate All Around FET, *VRG-FET* Vertical Replacement Gate FET, *TriGate* Triple Gate FET

10.3 Intel®'s High-k MOSFET Electrical and Physical Parameters

Table 10.3 describes in detail the geometrical and electrical properties of the device, as reported by the manufacturer [11, 14].

Where L_G is the Gate length, *Tox* is the oxide layer thickness I_{TH} is the average leakage current, x_{dD} and x_{ds} are the depth of the depletion region associated with the Drain and Source respectively, ρ is the electrical conductivity of the HfO_2 at 1100 °C, V_{GS} is the gate-source voltage, I_D is the Drain current, V_{TH} is the threshold voltage, ε_r is the relative permittivity of HfO_2 and V_{DS} is the Drain-Source voltage.

From the data at Table 10.2, it is possible to recognize that for the 45 nm gate length High-κ MOSFET, the oxide thickness T_{ox} has reach the size of a few atomic layers. This device also is considered to be a *short channel device*, because its gate

Table 10.3 Intel®'s 45 nm MOSFET electrical and physical parameters

Physical dimensions	Material parameters	Electrical parameters
L_G	ε_r	V_{gs}
45 nm	20	0–1.7 V
T_{ox}	K	I_D
1 nm	14–22	0–104 μA
x_{dD}, x_{ds}	P	V_{TH}
20–90 nm	4.5×10^3 @1100 °C	0.32 V @ Vds = 1 V
Gate pitch	Dielectric band gap	
160 nm	6 eV	

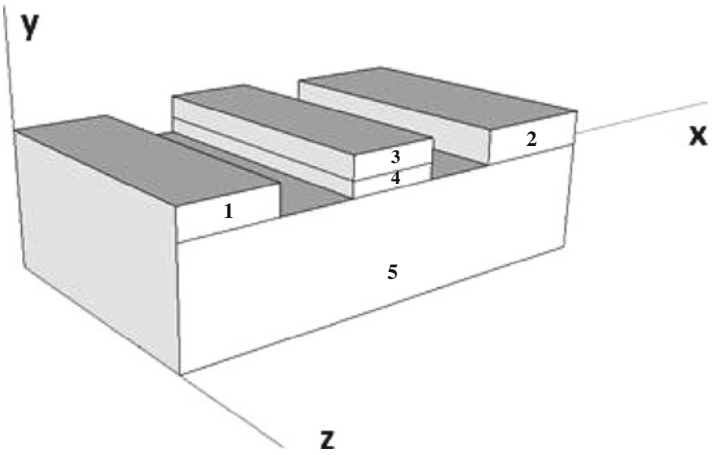

Fig. 10.1 Schematic view of a high-κ MOSFET. The main components are identified by number where *1* Source, *2* Drain, *3* Gate, *4* High-k dielectric layer, *5* Substrate

length (L_g) is in the same order of magnitude as x_{dD} and x_{ds}, which sets up a scenario where the electrical field along the y axis (see Fig. 10.1) is about 10^5 V/cm for N-channel High-κ MOSFET at $V_{DS} = 5V$ with $L_g = 100$nm [14], and where phenomena like carrier tunneling, Drain-Induced Barrier Lowering (DIBL), Channel Length Modulation (CLM), among others known as *Short Channel Effects* (SCE), are most likely to occur. SCE have not been fully implemented on modern MOSFET compact models mainly due to top-down approaches that make difficult to reach a particle-size level of detail in device analysis and authors considered the development of a model that accurately could describe the carrier transport in the presence of such phenomena.

10.4 A Model for Carrier Quantization

The model is based on the coupled Poisson-Schrodinger equations in order to describe the electron transport along the channel. The proposed procedure starts from Poisson equation describing 2-D potential distribution ϕ(x,y) along the channel.

$$\frac{\partial^2\phi(\mathrm{x,y})}{\partial \mathrm{x}^2} + \frac{\partial^2\phi(\mathrm{x,y})}{\partial \mathrm{y}^2} = \frac{\mathrm{q}}{\varepsilon_{\mathrm{HFO_2}}}(\mathrm{N_A(X)} + \mathrm{n(x,y)}) \tag{10.1}$$

Where q is the electron charge, ε_{HFO_2} is the electrical permittivity of Hafnium dioxide, $\mathrm{N_A}(x)$ is the density of acceptors along the channel and n(x, y) is the electron concentration along the channel.

In the scenario in which the charge is quantized, the continuous conduction band is now divided into two sub-bands. The wave function of each sub-band is given by the Schrödinger equation:

$$\frac{\hbar^2}{2m}\nabla^2\psi - q\phi(x,y)\psi_i(x,y) = E_i\psi_i(x,y) \tag{10.2}$$

Where $\hbar$ is the reduced Planck constant, $\psi_i(x,y)$ is the carrier wavefunction on the ith subband, m is the electron mass and the eigenvalue E_i is the energy level associated with wavefunction ψ_i [15]. Carrier's confinement is higher in the direction perpendicular to the Gate [16], so the one-dimensional Schrödinger equation can be used to assess the problem. Assuming a MOS structure with uniform potential distribution along the direction perpendicular to the Gate, the component in y axis can be removed from Poisson's equation, and the problem is reduced to coupled one-dimensional equations of Schrödinger-Poisson:

$$\frac{d^2\phi(x)}{dx^2} = \frac{qN_A(x)}{\varepsilon_{Hf}} - \sum_i \frac{Q_{inv,i}}{q\varepsilon_{Hfo_2}}|\psi_i(x)|^2 \tag{10.3}$$

$$-\frac{\hbar^2}{2m}\frac{d^2\psi(x)}{dx^2} - q\phi(x)\psi(x) = E\psi(x) \tag{10.4}$$

Where $Q_{inv,i}$ denotes the inversion charge on the ith subband. Reaching an analytical solution for this pair of equations is not an easy task; however, numerical simulations provide some insights into reaching this solution.

Figure 10.1 shows the results of simulating the carriers population per sub-band, using the parameters of Intel®'s High-κ MOSFET. $N_d = 1^{18}\mathrm{cm}^3$, $T_{ox} =$ 1 nm and $\kappa = 22$.

From Fig. 10.2, as we move on the voltage range between $0\mathrm{V}<\mathrm{V_{gs}}<3\mathrm{V}$, it is possible to see that between 45 and 85 % of the carriers are located in the lower sub-band $E_{1,1}$, so only the lowest level of energy can be considered to approach to the analytical solution. With that approximation, the pair of Eqs. (10.3) and (10.4)

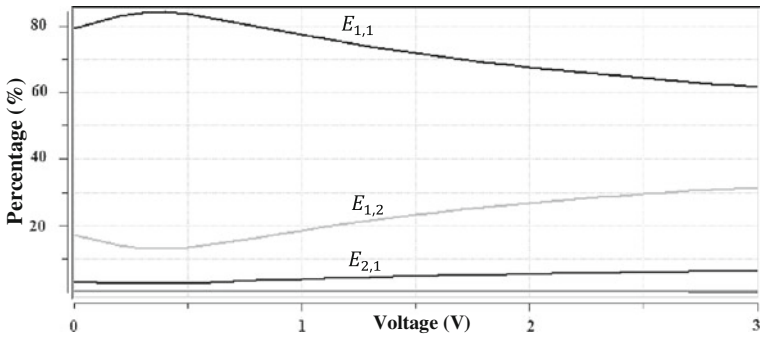

Fig. 10.2 Numeric simulation of carrier populations per sub-band, simulation conducted using SCHRED [18] with parameters $T_{ox} = 1$ nm, T = 300°K and $N_d = 10^{-18}\text{cm}^{-3}$

for each valley or group of sub-bands associated with the crystal structure of the interface *Si-Hfo*$_2$ are reduced to:

$$\frac{d^2\phi(x)}{dx^2} = \frac{qN_A(x)}{\varepsilon_{Hfo_2}} + \frac{Q_{inv,1}}{q\varepsilon_{Hfo_2}}\left|\psi_{1,1}(x)\right|^2 + \frac{Q_{inv,2}}{q\varepsilon_{Hfo_2}}\left|\psi_{1,2}(x)\right|^2 \tag{10.5}$$

$$-\frac{\hbar^2}{2m_i}\frac{d^2\psi_{1,1}(x)}{dx^2} - q\phi(x)\psi_{1,i}(x) = E_{i,1}\psi_{i,1}(x) \tag{10.6}$$

Where *i* denotes each one of the two valleys where the lowest energy level will be calculated.

Using calculus of variations, wave functions are assumed to have a shape similar to $\psi_{1,1}$ and $\psi_{1,2}$, thereby ensuring a good level of accuracy for the calculated energy levels [19]. The next step is to integrate the simplified Poisson equation from bulk to surface and also, in order to find the lowest expression of energy, expected value of the Hamiltonian of the wave function $\psi_{1,1}$ is calculated obtaining the following expression:

$$E_{1,1} = \int_0^\infty \psi_{1,1}(x)\frac{\hbar^2}{2m_1}\frac{d^2}{dx^2}\psi_{1,1}(x)dx + \int_0^\infty q\phi(x)\psi_{1,1}(x)^2 dx \tag{10.7}$$

A simulation of the sub-bands wave functions (shown in Fig. 10.3), provides elements to reach an analytical solution for Eq. (10.7)

Simulation of Fig. 10.2 shows that the peak of carrier density is a few nanometers (no more than 5 nm) below the channel surface, which leads to approximate:

$$d \gg \frac{1}{\alpha_1} \quad \text{and} \quad d \gg \frac{1}{\alpha_2}, \tag{10.8}$$

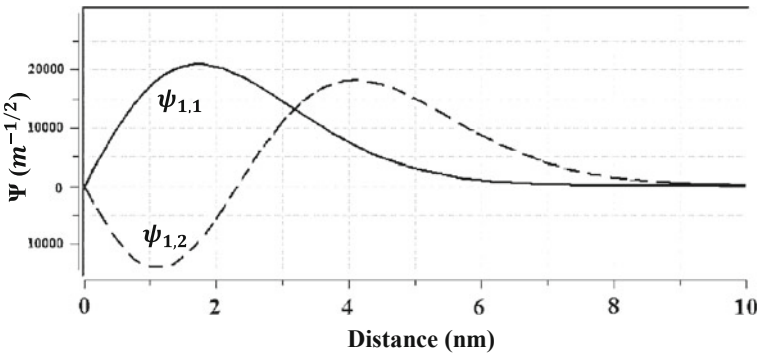

Fig. 10.3 Sub-bands wavefunctions, simulation conduced on SCHRED [20]

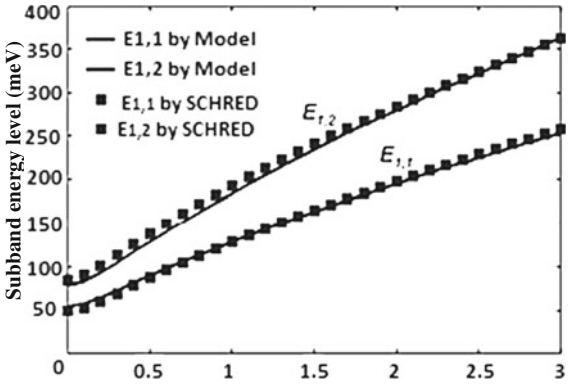

Fig. 10.4 Energy levels at each valley, by model expressions and by SCHRED simulation

Then, this approximation is applied and the result is factorized, based on the parameter of proportionality γ. According to the variations method, α_1 and α_2 should minimize the energy level, i.e:,

$$\frac{dE_{1,1}}{d\alpha_1} \quad \text{and} \quad \frac{dE_{1,1}}{d\alpha_1} = 0 \tag{10.9}$$

Calculating the derivatives, we obtain the expressions for α_1 and α_2 then the mean value of γ is obtained. Finally, replacing the values obtained and the approximations described above, leads to the expressions for $E_{1,1}$ and $E_{1,2}$:

$$E_{1,1} = \frac{3\hbar^2\alpha_1^2}{2m_1} \quad \text{and} \quad E_{1,2} = \frac{3\hbar^2\alpha_2^2}{2m_2} \approx 1,432E_{1,1} \tag{10.10}$$

Verification of model accuracy is performed by comparing its results with SCHRED simulation of energy levels for sub-bands $E_{1,1}$ and $E_{1,2}$ as shown in Fig. (10.4).

Accuracy of the quantization model obtained, allows us to approach to a short channel I-V model that takes into account the quantization of charge that occurs at this scale, and enables some approximations for that model.

10.5 I-V Short Channel Model

The fact that, in short channel devices, there is no complete control of the channel charge is an indicator that E_y is not negligible compared with E_x and the effects associated with this behavior should be incorporated in a compact model. In terms of I_d, the most significant effect to be included is velocity saturation, that may result in reduced effective drain saturation current. One of the empirical relations in use to model the dependence of carrier velocity V_d with respect to E_x was adopted for this step [19]:

$$|V_d| = \frac{|V_d| \max \frac{|E_x|}{|E_c|}}{1 + \frac{|E_x|}{|E_c|}} \tag{10.11}$$

Where E_c is defined as the intersection of the $v_d = \mu V_{GS} E_x$ line and an imaginary horizontal asymptote, as can be seen on Fig. 10.5 (Figs. 10.5, 10.6, 10.7).

The first step is to find an expression for I_d in non-saturation regime I_{dsn} E_x is expressed as the differentials of the potential between the polarization of the inversion layer and the end of the piece. The result of integrating these differences along the channel is presented in Eq. 10.12.

$$I_{DS} = \frac{W}{L_G} \mu c_{ox} \left[\frac{(V_{GS} - V_{TH}) V_{DS} - 0.5 \alpha v_{DS}^2}{1 + \frac{V_{DS}}{L_G . E_c}} \right] V_{DS} \leq V'_{DS} \tag{10.12}$$

Where W is the channel width and C_{ox} is the oxide capacitance. For the expression in the saturation region, it is necessary to include the effect of *Channel Length Modulation* (CLM) [18] finding the value of V_{ds} at which saturation occurs, so the expression of I_{ds} in presence of velocity saturation is given by:

$$\mathrm{I_{DS}} = \mathrm{W} \mu \mathrm{C_{ox}} \left[\frac{(\mathrm{V_{GS}} - \mathrm{V_{TH}}) \mathrm{V'_{DS}} - 0.5 \alpha \mathrm{v_{DS}^2}}{\mathrm{L_g} \left(1 - \frac{1_\mathrm{p}}{L_G} + \frac{\mathrm{V'_{DS}}}{L_G . E_c} \right)} \right] \tag{10.13}$$

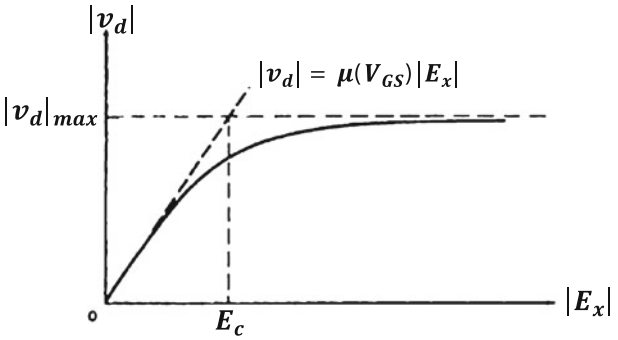

Fig. 10.5 Magnitude of carrier velocity in the inversion layer versus magnitude of the longitudinal component of the electric field [17]

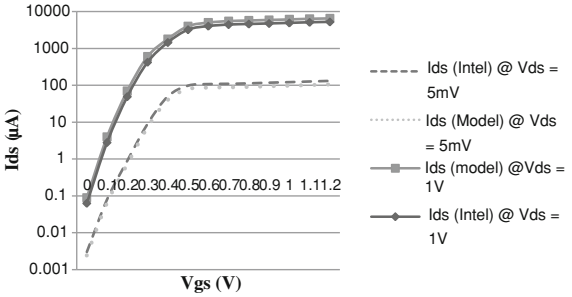

Fig. 10.6 Comparison of I-V characteristics provided by the manufacturer and calculated by the model equations

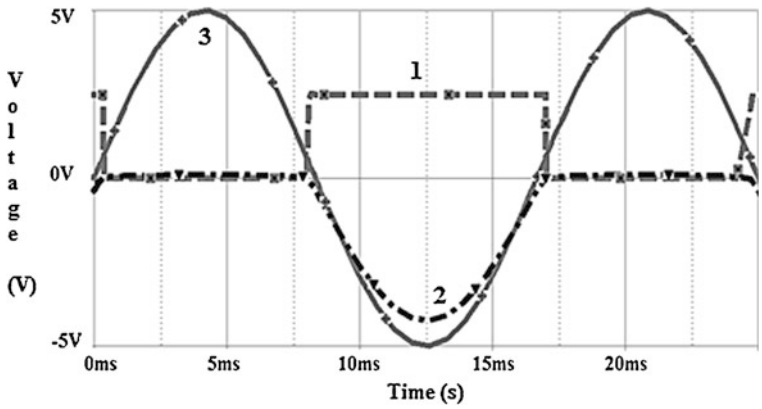

Fig. 10.7 Transient analysis using Orcad PSICE^{TM} 9.1 for three signals labeled. *1* Output voltage of native N-MOS MOSFET with High-k transistor physical and electrical parameters running under BSIM 4.4 model, *2* output of ABM blocks running model expressions obtained with this methodology, *3* input voltage signal with amplitude of 5 V and 60 Hz frequency. This results shows higher accuracy of simulations of a common circuit configuration compared with performance of state-of-the-art compact models, like BSIM 4.4

10.6 Compact I-V Short Channel Model

Finally, to obtain a unified expression of I_d in presence of velocity saturation, it becomes necessary to incorporate the smoothing equation of V_{ds}:

$$V_{deff} = V_{DSAT} - \frac{1}{2}\left[V_{DSAT} - V_{DS} - \delta_s + \sqrt{(V_{DSAT} - V_{DS} - \delta_s)^2 + 4\delta_s V_{DSAT}}\right] \tag{10.14}$$

Thus, V_{deff} is used to replace V_{ds} in the I_{ds} expression, as well as the early effective voltage V_{Aeff} to incorporate CLM in the unified expression, that is then obtained:

$$I_{ds} = \frac{I_{deff}}{1 + \frac{(R_{sd} I_{deff})}{V_{deff}}} \tag{10.15}$$

With

$I_{deff} = \left(1 + \frac{V_{DS} - V_{deff}}{V_{Aeff}}\right) I_{ds0}$ and $V_{Aeff} = \frac{E_{SAT} L_{eff} (E_{SAT} L_{eff} + V_{DS})}{\zeta v_{deff}}$

10.7 Comparison of Model Equations with Intel® Data

With the physical and electrical parameters given in Table 10.2 and those obtained by the *Arizona State University Predictive Technology Model* for 45 nm technology node [20], we compare the results using the IV model expressions obtained from the curve provided by the manufacturer (see Fig. (10.6)) [21].

The results show a correlation coefficient R^2 equal to 98 % and an average error of 0.33 %, indicating a relatively strong relationship between the data obtained by the model and those reported by the manufacturer. This level of accuracy, allows us to get to the next stage, which is the model equations testing in SPICE.

10.8 Testing the Model Expressions in a SPICE Circuit Simulation

To ensure the portability of the model for any SPICE-based simulator, obtained model expressions were represented by using Analog Behavioral Modeling blocks, included in Orcad© PSPICE 9.1. Those blocks have a maximum of three inputs and one output of voltage or current. They use mathematical relationships to model a circuit segment. When connected in cascade, and at netlist generation stage, the simulator concatenates the blocks to make the entire expression. Equations are entered in the model and tested in a configuration of half-wave rectifier-inverter,

compared with an N-channel MOSFET in the same configuration, whose electrical and physical parameters have been replaced by the ones of Intel's High-k MOSFET to verify the performance of BSIM4 model at sub-50 nm scale and the operation of the model obtained in a circuital implementation. Simulation (Fig. (10.7)) shows the degradation in the description of the MOSFET behavior in sub-threshold regime by BSIM4 model and a good performance of the equations obtained for the model.

10.9 Conclusions and Recommendations for Future Work

A compact model for High-κ 45 nm MOSFET was described including the short channel effects present at nanoscales. The methodology has consolidated in SCORM-compatible learning material (Sharable Content Object Reference Model), which is available at https://nanohub.org/resources/10024.

Future work could include additional effects such as temperature dependence and body effects. The model could be simplified to have as few parameters as possible, avoiding a great number of ABM blocks.

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