Chapter 11
A Low Power Limiting Amplifier Designed for the RSSI of a 5.8 GHz ETC Receiver

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Abstract A low power limiting amplifier designed for received signal strength indicator of a 5.8 GHz ETC receiver is presented in this chapter. Systematic analysis is carried out first to determine the optimal number of gain stages and the gain-bandwidth product of each stage. Then the detailed circuit design is discussed. The limiting amplifier consists of twelve AC-coupled gain stages, and is implemented using the standard CMOS 0.18 μm technology. The design is validated under Zeni design environment, and the simulation results show that the limiting amplifier achieves overall small signal gain of 98 dB, with 22 MHz bandwidth. Powered by a 1.8 V DC supply voltage, the total power consumption of the limiting amplifier is only 5.5 mW.

Keywords CMOS · Electronic tolling collection (ETC) · Limiting amplifier · Received signal strength indicator (RSSI)

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11.1 Introduction

In many major cities in china, traffic congestion is a prominent problem with the rapid increase of automobiles. Electronic tolling collection (ETC) is known to be an efficient method for congestion alleviation, for in an ETC system, the vehicle is allowed to be charged without slowing down, and therefore the traffic speed can be largely improved. The Standardization Administration of the People's Republic of China (SAC) has already released the Chinese standard of Dedicated Short Range Communications (DSRC), in which the ETC operating frequencies is defined to be from 5.8 to 5.9 GHz [1].

Currently, Shenzhen University is developing an ETC system. In the system, direct conversion architecture is adopted to implement the 5.8 GHz receiver due to its simple, robust structure and low power consumption. In order to prevent the undesired DC level presented at the base-band, which is primarily caused by the leakage from the local oscillator to the receiver front-end, from degrading the receiver performance, received signal is first down-converted to an intermediate frequency of 10 MHz.

In the envisioned application, when multiple vehicles are presented at the tolling gate, each should be assigned a distinct communication channel. To help select the vacant channel automatically, a received signal strength indicator (RSSI) is included in the ETC receiver design.

The RSSI monitors the received signal strength while the receiver scans all the communication channels, and bi-directional link between the vehicle and the tolling station can only be established once a vacant channel is found.

The RSSI is generally realized in logarithmic form because the wide dynamic variation of the received signal that can be represented within a limited indication range. The logarithmic characteristic can be realized through piecewise linear approximation by using a limiting amplifier with multiple cascaded gain stages [2]. As shown in Fig. 11.1, The output of each stage is rectified, summed together, and translated into electrical quantities, such as an output current or voltage, that are proportional to the input power level in terms of dBm.

This chapter focuses on the limiting amplifier design for RSSI in the ETC system. In Sect. 11.2, a systematic level optimization process is presented to help determine key parameters of the limiting amplifier. The detailed circuit implementation of the cascaded gain stages is shown in Sect. 11.3. The design is validated under the Zeni design environment, and the simulation results are discussed in Sect. 11.4. A concluding remark is given in Sect. 11.5.

11.2 Systematic Optimization

For a limiting amplifier design, the number of the cascading gain stages associated with their gain, bandwidth, and power determines the overall circuit performance. In order to achieve a large dynamic range, and at the same time minimize the

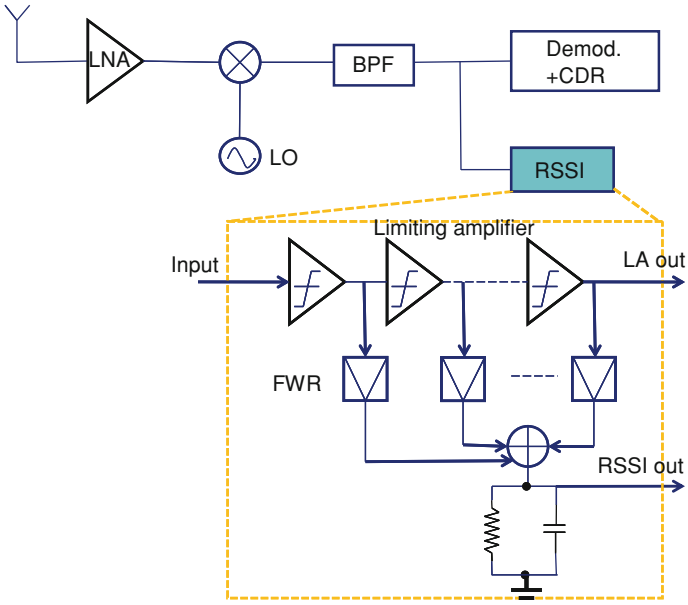

Fig. 11.1 Architecture of the ETC receiver and RSSI under developing in Shenzhen University

overall power consumption, optimal design parameters, such as the number of gain stages and the gain-bandwidth product (GBW) of each gain stage, have to be determined.

For design simplification, the cascading gain stages are kept identical. In its 1st order approximation, the identical gain stage is assumed to be linear, and the transfer function with voltage gain A can be written as:

$$\begin{aligned} V_{out} &= AV_{in} \quad for\ V_{in} < V_s \\ V_{out} &= V_{\mathrm{L}} \quad for\ V_{in} \geq V_s, \end{aligned} \tag{11.1}$$

in which V_s is the threshold voltage, above which a gain stage is saturated, and V_L is the corresponding output voltage.

If the input signal is small enough, all gain stages operate in the linear region, and the output voltage of the limiting amplifier is ANxVin, in which N is the number of gain stages. As the input signal strength increases, the gain stages are driven into saturation one by one starting from the last stage, resulting to an approximated logarithmic response.

Given the overall small signal gain and bandwidth of the limiting amplifier AV and fV, the required gain and bandwidth of the identical gain stage can be derived as [2]:

$$A_C = A_V^{(1/N)-1} \tag{11.2}$$

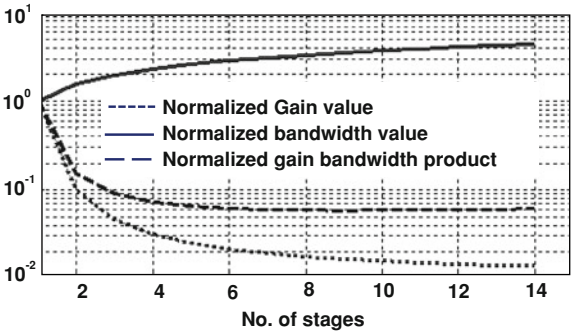

Fig. 11.2 Normalized gain, bandwidth and GBW of a identical gain stage for a limiting amplifier with 100 dB small signal gain

$$f_C = \frac{f_V}{\sqrt{2^{1/N} - 1}} \tag{11.3}$$

For a targeted 100 dB overall small signal gain, the normalized gain, bandwidth of the identical gain stage for specified number of stages are plots in Fig. 11.2. The voltage gain for each gain stage is obviously reduced if the cascading number of stages increases, but it requires each gain stage to have larger bandwidth to compensate the increased number of poles. Figure 11.2 also includes the normalized GBW of the identical gain stage.

Total power consumption of the limiting amplifier is another key design parameter. A large number of gain stages not only results to alleviated GBW requirement, it can also generate a logarithmic response with less error [2]. However, the overall power consumption might increase. To facilitate the optimal design, the relation between the overall power consumption of the limiting amplifier PV and GBW is derived.

PV is the product of the number of stage N and the power consumption of the identical gain stage, which can be expressed as [3]

$$\mathrm{P_V} = \mathrm{N} \times \mathrm{P_C} \propto \mathrm{N} \times (\mathrm{GBW})^2 \tag{11.4}$$

GBW in (11.4) is the ratio of the gain stage trans-conductance and the input capacitance of the following stage. It can be shown the GBW is also proportional to square root of the identical gain stage power consumption P_C, as in (11.5).

$$GBW = \frac{g_m}{C} = \frac{\sqrt{2\mu C_{ox}(W/L)I_d}}{kWL} \propto \sqrt{\frac{I_d}{WL^3}} = \sqrt{\frac{P_C}{V_{DD}WL^3}} \tag{11.5}$$

In (11.5), I_d is the bias current of the identical gain stage, W and L are the width and length of the MOS transistor that provides the trans-conductance.

The total power consumption of the limiting amplifier for 100 dB overall small signal gain is plotted in Fig. 11.3. Clearly, for the specified gain, the total power consumption decreases as the number of stages becomes larger. If the limiting amplifier consists of more than 4 stages, no obvious power increase can be

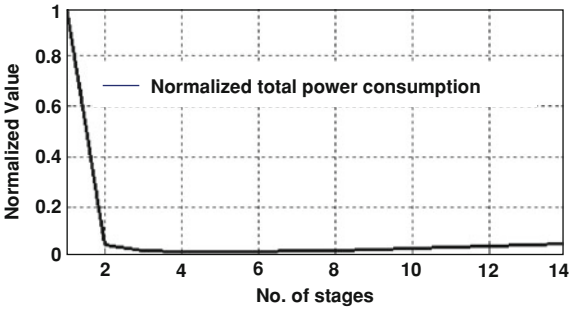

Fig. 11.3 Normalized total power consumption of a limiting amplifier with 100 dB small signal gain

observed. Therefore, more gain stages can be used to better approximate the required logarithmic response [4]. In this design, a total of twelve gain stages are used, with the gain of each set to 8.5 dB.

11.3 Circuit Implementation

The limiting amplifier consists of twelve cascading gain stages. Since the received signal is down-converted to 10 MHz intermediate frequency, the DC-offset cancellation scheme usually implemented in the RSSI designs is not required [5], and each stage can be AC-coupled to the following stage. Thus, the circuit design is greatly simplified.

Figure 11.4 shows the schematic of a single gain stage. A simple differential amplifier with NMOS input pair with load resistance R_D is utilized. To improve the amplifier linearity, a source degeneration resistor R_3 is added. The amplifier input pair is self-biased by the passive low pass network consisting of R_1, R_2, and therefore only one bias voltage V_b is required. Neglecting the gate-bulk capacitance of the input NMOS pair, the overall voltage gain of the identical gain stage can be written as:

$$A_V = \frac{G_m \times R_D \| C_L}{1 + sR_1C_1} = \frac{sG_mR_DR_1C_1}{(1 + sR_1C_1)(1 + sR_DC_L)} \tag{11.6}$$

The voltage transfer function of the gain stage has a bandpass characteristic, with its passing band determined by the two pole $1/R_1C_1$ and $1/R_DC_L$.

11.4 Design Validation

The limiting amplifier is implemented using CMOS 0.18 μm technology, and validated under the Zeni design environment.

In this design, C_1, C_L and R_D are selected as 950 fF, 400 fF and 3.76 KΩ, and the simulated frequency response of a single gain stage is shown in Fig. 11.5.

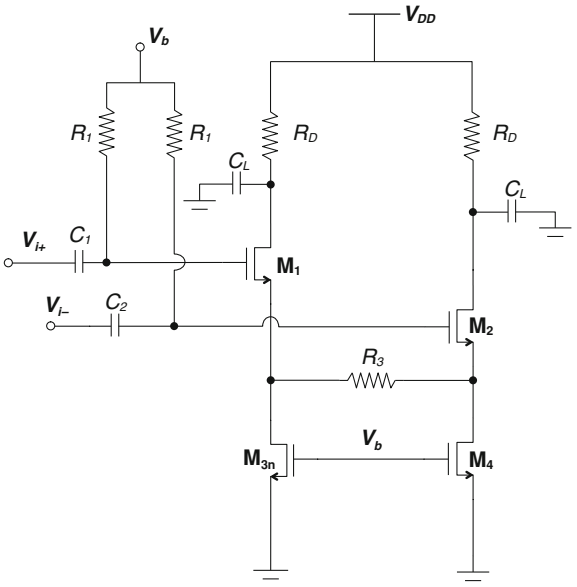

Fig. 11.4 Schematic of the identical gain stage

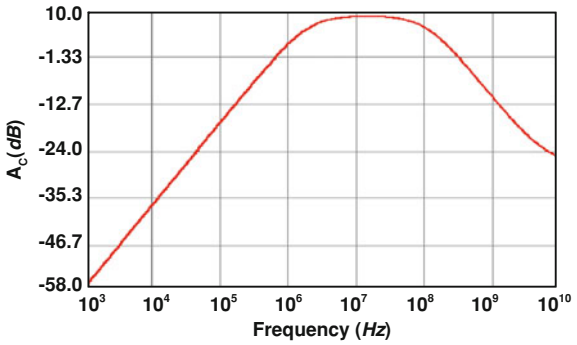

Fig. 11.5 Frequency response of the identical gain stage

A single gain stage has 8.5 dB small signal gain, and the 3 dB bandwidth is 2 ~ 110 MHz.

In total twelve identical gain stages are cascaded to form the limiting amplifier. The overall small signal gain of the completed limiting amplifier is simulated and shown in Fig. 11.6. The limiting amplifier achieves 98 dB overall small signal gain, and the 3 dB bandwidth is 5.6–22 MHz, approximately 1/5 of a single gain stage.

The −3 dB input sensitivity of the limiting amplifier is also simulated by varying the input signal strength from −100 to 0 dBm (Fig. 11.7). The limiting amplifier −3 dB input sensitivity can be defined as the input power that causes output power 3 dB lower than the saturated constant level, and is about −60 dBm for this design.

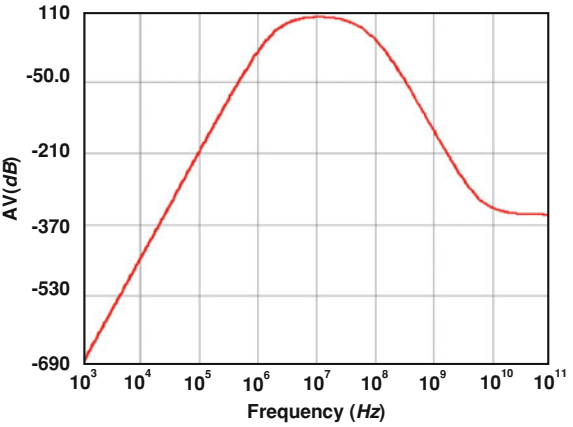

Fig. 11.6 Frequency response of the12-stage limiting amplifier

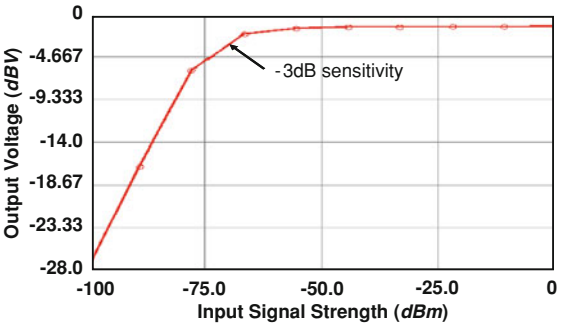

Fig. 11.7 The simulated −3 dB sensitivity of the limiting amplifier

With 1.8 V DC supply voltage, the power consumption of the completed limiting amplifier is 5.5 mW.

11.5 Conclusion

This chapter discusses a low power limiting amplifier designed for the RSSI of a 5.8 GHz ETC receiver. The number of stage and the gain bandwidth of a single gain stage are first determined through system level analysis, and then the detailed circuit implementation is presented. The limiting amplifier is designed and implemented using standard CMOS 0.18 μm technology. Formed by cascading twelve identical gain stages, the limiting amplifier achieves 100 dB overall small signal gain and 22 MHz bandwidth, while only consumes 5.5 mW of power from a 1.8 V voltage supply.

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