Chapter 40
A Low Noise 32-Channel CMOS Read-Out Circuit for X-ray Silicon Drift Chamber Detectors

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Abstract In this paper we present a 32-channel integrated front-end circuit for low-energy (0.5–100 keV) X-ray detection with a multi-anode silicon drift detector. The front-end circuit includes 32 read-out pixel cells (RPC), each consisting of a low noise preamplifier, a second-order RC-CR pulse shaper, a peak stretcher, an amplitude and a peak discriminator, as well as a reset and pile-up rejection circuit. Most of the parameters of the front-end circuit are programmable through a digital configuration register, supporting daisy-chain connection. At room temperature the equivalent noise charge of the RPC is 18.3 e$^-$ and its linearity error is lower than 5% over the complete input range. The front-end circuit has been designed in a 0.35-μm CMOS technology with main 3.3-V power supply. A single RPC occupies an area of 200×380 μm^2 and consumes 0.4 mW.

40.1 Introduction

Semiconductor devices for X-ray imaging and spectroscopy gained significant importance in the last decade and their exploitation is still growing, since they are the key elements in many medical and scientific applications [1, 2]. Pixel detectors
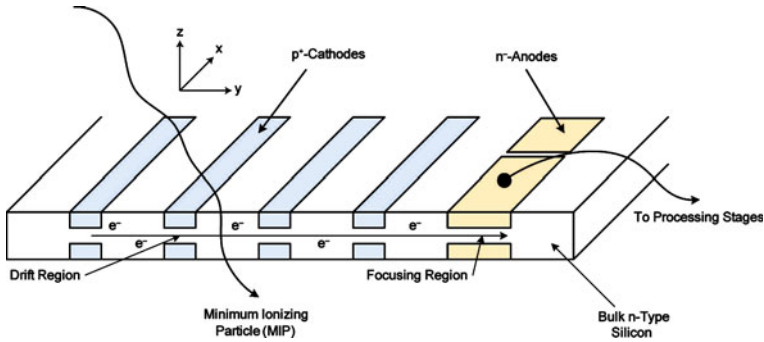
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**Fig. 40.1** Simplified structure of a typical silicon drift detector

and, in particular, silicon drift chambers play an important role in this field, because of their affordable manufacturing technology, high energy resolution, and nevertheless, low noise performance. The simplified structure of a silicon drift detector is shown in Fig. 40.1. This device consists of a pattern of cathodes (p^+ implants) on both sides of the silicon chip and a set of anodes (n^+ implants) at the edge of the chip, connected to the readout electronics [1].

Drift detectors have demonstrated excellent energy resolution because of their very small read-out anode geometry (hence capacitance), which allows the minimization of the contribution of the electronic noise of the preamplifier on the overall performance of the detection system. The charge carriers produced in the detector by the incident radiation, thanks to the transversal electric field, drift toward the anodes, where they are collected. The position of the anode collecting the charge provides the x coordinate of the incident radiation position, while from the drift time it is possible to determine the y coordinate. Therefore, with drift detectors it is possible to reconstruct the spatial position of the incident radiation on the plane (x and y coordinates), using a linear array of front-end circuits to read-out the information, instead of a matrix as in conventional pixel detectors. The output signal of a drift detector is a charge pulse, as in conventional pixel detectors, but with opposite polarity, which must be amplified and shaped, in order to extract the useful information.

40.2 Front-End Circuit Description

The block diagram of the proposed integrated front-end circuit is shown in Fig. 40.2. It consists of 32 RPCs, a digital logic block for system programmability and trigger management, two digital-to-analog converters (DACs) for generating programmable reference voltages (for calibration purpose), and an analog output buffer. The block diagram of the RPC is instead shown in Fig. 40.3. The circuit is based on the same architecture presented in [3], but, as mentioned, it has been

Fig. 40.2 Simplified block diagram of the proposed integrated front-end circuit
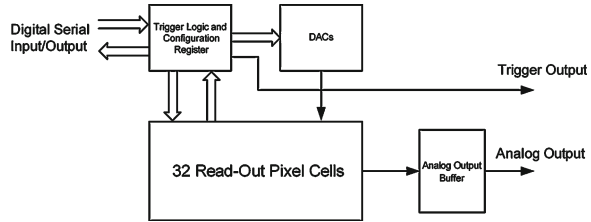
modified for handling electrons instead of holes as input signal and its functionality has been optimized for reading out silicon drift detectors with the required input signal range (0.5–100 keV, corresponding to 60–27,000 e^-). The RPC is divided into two main parts: an analog section, which includes a low-noise preamplifier, a pulse shaper, and peak stretcher, as well as a mixed-signal section, which includes an amplitude discriminator, a peak discriminator, and the digital logic required for reset and pile-up rejection [4]. The input low noise preamplifier is based on a folded cascode architecture with also an additional dedicated supply (2.0-V), to avoid interference from main 3.3-V rail. When disabled, the preamplifier sinks the detector current, thanks to the low input impedance by design, and ensures proper biasing of the anode of the detector, without providing any output signal. The output of the preamplifier is connected to the second order RC-CR pulse shaper. The shaping time can be digitally selected among eight different values, ranging from 0.7 to 5.5 μs, by means of two sets of switches controlled by a 3-bit digital word, stored in the configuration register. The two shaping stages are coupled by a gain compensation circuit, whose function is to maintain the gain constant for different shaping times. The output stage of the shaper also sets the desired baseline voltage (V_{bl}) by means of a feedback loop.

The peak stretcher is based on a differential input stage with an unidirectional current source, which charges the hold capacitor. When the pulse shaper output is below the threshold of the amplitude discriminator, the circuit behaves as a unity gain voltage buffer. When the amplitude discriminator is triggered by an input signal over threshold, the circuit follows instead the input signal up to its peak and then holds it, since the hold capacitor has no path for discharging. When the input signal reaches its peak, the peak stretcher also generates a trigger signal which connects its input node to a fixed voltage, lower than V_{bl}, in order to avoid variations of the held voltage due to noise peaks. The reset of the peak stretcher is performed by discharging the hold capacitor with a constant current source. An analog multiplexer, controlled by the digital bit Signal Selector, stored in the configuration register, allows the connection of either the pulse shaper output or the peak stretcher output to the analog output buffer, for testing purposes. The analog output buffer has been designed for low noise and low input capacitance, in order to avoid the degradation of the settling performance of the previous stage. The amplitude and peak discriminators generate two different digital trigger signals. In particular, the amplitude discriminator output signal rises when the pulse shaper output signal crosses a programmable threshold and it is used to arm
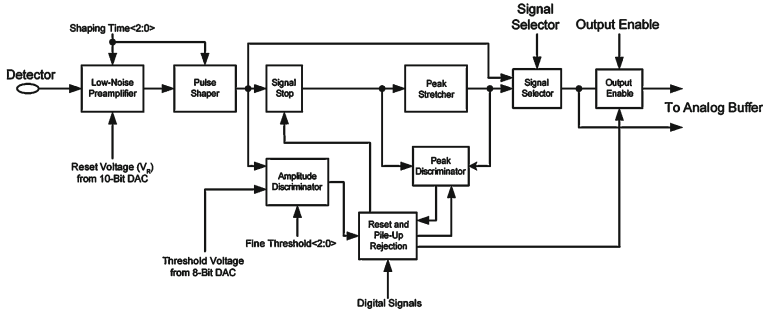
Fig. 40.3 Detailed architecture of a single RPC

the peak stretcher. The amplitude discriminator features global and local threshold level settings: the global threshold value is generated by an on-chip 8-bit resistive DAC controlled by a digital word stored in the configuration register and it is common for all the RPCs in the array, while the local or fine threshold value is set, separately for each RPC, by three bits stored in the configuration register. The global threshold tuning range is 60–1,400 e^- while the fine threshold tuning step is 50 e^-. The configuration register allows us to calibrate the front-end circuit parameters. It consists of a shift register, which receives as input a serial bitstream, and a configuration memory, which holds the configuration parameters of the circuit. Default values are provided after reset for typical operation.

40.3 Simulation Results

The proposed front-end circuit for low-energy X-rays detection has been designed in a 0.35-µm CMOS technology with 3.3- and 2.0-V power supply. The circuit has been simulated at transistor level, including post-layout capacitive and resistive parasitic extraction. Table 40.1 summarizes the achieved performance, while Fig. 40.4 represents the layout of the RPC. The power consumption per channel is 0.4 mW, while the input referred equivalent noise charge is 18.3 e^-_{rms}. The simulated distortion of the channel is lower than 5%.

40.4 Conclusions

In this paper we presented a 32-channel integrated front-end circuit for low-energy X-ray detection, designed for a multi-anode silicon drift detector. The chip has been designed in a 0.35-µm CMOS technology with a main 3.3-V power supply

Table 40.1 Simulated performance summary

Technology	CMOS 0.35 μm, 2-Poly, 4-Metal
Supply voltage	3.3 V, 2.0 V
Power consumption	0.4 mW per channel
Input signal range	500 eV–100 keV
	(60 e$^-$–27,000 e$^-$)
Equivalent noise charge	18.3 e$^-$ rms
Full scale linearity	5%
Shaping time	0.7–5.5 μs
Output voltage swing	1.1 V
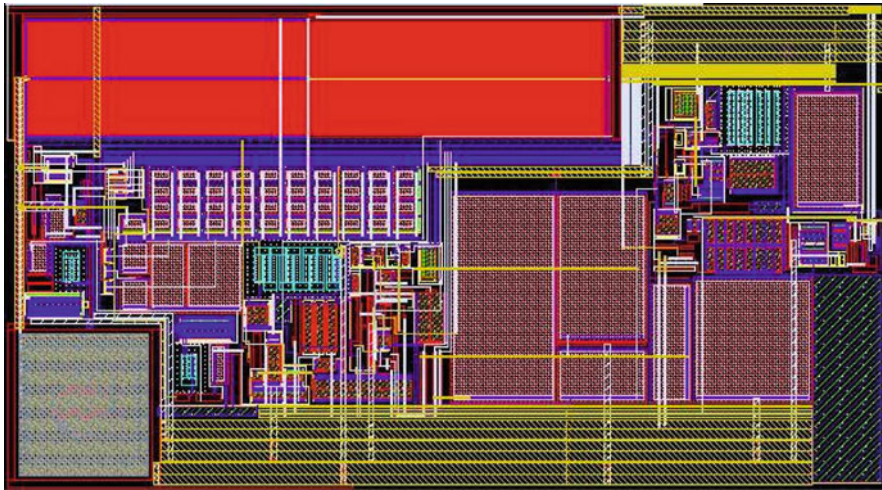
Fig. 40.4 Layout of the RPC

and consumes 0.4 mW per channel. The area of a single channel is
$200 \times 380 \ \mu m^2$. A dedicated memory is provided for calibration purpose.

References

1. Labanti C et al (1999) ICARUS ASIC: a 16 channel photodiode read-out system. IEEE Trans Nucl Sci 46(3):144–149
2. Debertin K, Helmer RG (1988) Gamma and X-ray spectrometry with semiconductor detectors. North-Holland, Amsterdam
3. Caccia S et al (2008) A mixed-signal spectroscopic-grade and highfunctionality CMOS readout cell for semiconductor X-gamma ray pixel detectors. IEEE Trans Nucl Sci 55(5):2721–2726
4. Bastia P et al (2006) An integrated reset/pulse pile-up rejection circuit for pixel readout ASICs. IEEE Trans Nucl Sci 53(1):414–417