Chapter 8
Network Reduction by Inductance Elimination

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Abstract A new approach to model order reduction of passive linear circuits is proposed. It is based on the successive elimination of small inductances. Simultaneously with the inductance removal additional capacitances are connected to neighboring branches to provide first order accuracy of the reduced transfer functions. The passivity of the reduced circuit is easily verified. The proposed approach can be applied jointly with the widely used node elimination algorithm TICER.

8.1 Introduction

Model-order reduction (MOR) of linear interconnects is the effective tool to decrease computational efforts in the simulation of integrated circuits (IC) [1].

Fast MOR of RC interconnect can be achieved by the TICER method [2]. The TICER performs the reduction by the successive elimination of circuit nodes. An analysis of the TICER in comparison with other approaches can be found in [3]. TICER usually does not provide the circuit reduction ratio that is achieved in the moment-matching or balanced truncation approaches [4]. Note that in such cases the method can be implemented as a preprocessing step [5] that allows to obtain the essential speedup of more complicated methods.

The TICER elimination algorithm cannot be applied to nodes with connected inductances. Usually the inductances in IC interconnects are neglected and this is considered to be insignificant for the interconnect reduction. But the growth of

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frequencies and/or power of IC increases the contributions of inductances into interconnect response which leads to a notable error caused by their neglect. Therefore it is desirable to extend the TICER approach to circuits with small inductances.

There are some proposals to take into account nodal inductances in the elimination algorithm. The special case of a node with two RL branches and a number of capacitances is considered in [6, 7]. In [8] high order admittances are obtained by the nodal elimination followed by optimization-based RLC synthesis procedure. Such an approach however seems to be too complicated and time-consuming. Paper [5] presents the rules for merging any two branches connected to the eliminating node. But the rules do not always save first order terms of Laplace admittances which results in an insufficient accuracy in the case of small inductances. One particular merging rule for LR-branch (at small L) and C-branch is equivalent to the inductance neglect.

The aim of this paper is the development of a first order elimination-based algorithm for circuits with small inductances. We propose an approach based on the simultaneous elimination of two circuit variables, i.e. nodal voltage and inductance current. The proposed approach generates a reduced circuit where the nodal inductance is deleted (shorted), and additional capacitances are connected to neighboring branches guaranteeing first order accuracy (Sect. 8.3). The circuit passivity can be verified by the criterion of the positive definiteness of the capacitance matrix. If the eliminated inductance is coupled with other circuit inductances (Sect. 8.4) then the reduced circuit contains couplings between inductances and capacitances (LC-couplings). It is shown that the couplings correspond to additional nonzero entries of the capacitance matrix of the Modified Nodal Analysis (MNA). This implies that the simulation of the reduced circuit with LC-couplings requires small corrections in the simulator code. The rules of inductance elimination in the presence of LC-couplings (Sect. 8.5) are also derived. The description of the algorithm (Sect. 8.6) and numerical experiments (Sect. 8.7) are presented.

8.2 Elimination of RC-Node by TICER

The elimination of an RC node (Fig. 8.1) is based on the expression for the star connection transform in the Laplace domain (we label branches by the same indexes as their outward nodes)

$$\tilde{y}_{ij} = \frac{y_i y_j}{Y_n} = \frac{(g_i + sc_i)(g_j + sc_j)}{G_n + sC_n}. \tag{8.1}$$

Here $y_i = g_i + sc_i$, $Y_n = \sum_{j \in S_n} y_j = G_n + sC_n$ are branch and nodal admittances respectively, S_n is the set of the indexes of outward nodes of RC-branches connected to the node n.

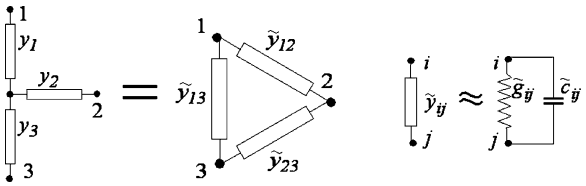

Fig. 8.1 Circuit transform under the elimination of an RC-node

If higher order terms of the Laplace variable s in the Taylor expansion of (8.1) are truncated then one obtains expressions for conductances and capacitances, which must be added to the circuit after node elimination:

$$\tilde{g}_{ij} = \frac{g_i g_j}{G_n}, \quad \tilde{c}_{ij} = \frac{g_i c_j + g_j c_i}{G_n} - \frac{g_i g_j}{{G_n}^2} C_n. \tag{8.2}$$

The method TICER [2] applies (8.2) without the last term in $\tilde{c}_{ij}$, and in this case all capacitances of the reduced circuit are positive. Thus the circuit passivity is provided. However, it has been proved in [9] that in spite of possible negative capacitances the application of (8.2) does not lead to the loss of circuit passivity. Hence, the exact first order expression (8.2) can be applied to the nodal elimination to achieve less error.

8.3 Inductance Elimination

Here we consider the case of a single inductance connected to an RC node (Fig. 8.2). To obtain the reduced circuit we perform simultaneous elimination of two circuit variables: nodal voltage and inductance current.

Let w_i be the current of the ith branch connected to node n

$$w_i = y_i(v_i - v_n), \quad i \in S_n. \tag{8.3}$$

The Kirchhoff Current Low (KCL) equation for node n allows us to obtain the inductance current as

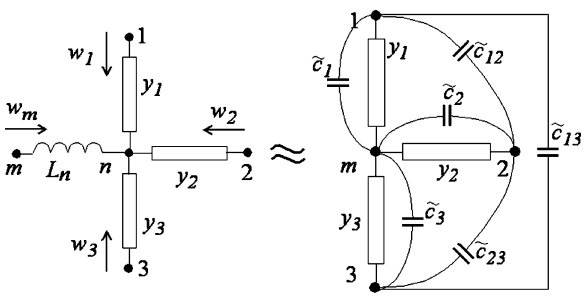

Fig. 8.2 Circuit transform under inductance elimination

$$w_m = -\sum_{j \in S_n} w_j = -\sum_{j \in S_n} y_j (v_j - v_n). \tag{8.4}$$

The inductance voltage is defined by the equation

$$v_n - v_m = sL_n w_m. \tag{8.5}$$

Substituting (8.4) into (8.5) we obtain

$$v_n(1 - sL_n Y_n) = v_m - sL_n \sum_{j \in S_n} y_j v_j. \tag{8.6}$$

The nodal variable derived from (8.6) by neglecting higher order terms is

$$v_n = v_m(1 + sL_n G_n) - sL_n \sum_{j \in S_n} g_j v_j. \tag{8.7}$$

After substitution of (8.7) into (8.3), neglecting higher order terms, and collecting terms in accordance to nodal voltages we obtain

$$w_i = y_i(v_i - v_m) + s\tilde{c}_i(v_i - v_m) + s \sum_{j \in S_n^i} \tilde{c}_{ij}(v_i - v_j), \tag{8.8}$$

where S_n^i is the set S_n without index i, and

$$\tilde{c}_i = -sL_n g_i G_n, \ \tilde{c}_{ij} = sL_n g_i g_j. \tag{8.9}$$

The expression for the ingoing current of the ith node (8.8) corresponds to the following reduced circuit (Fig. 8.2):

(a) node n is eliminated, and the inductance is shorted;
(b) old RC branches are saved in accordance with the first term of (8.8);
(c) new negative capacitances $\tilde{c}_i$ (8.9) are connected to each RC branch to define the current corresponding to the second term of (8.8);
(d) new capacitances $\tilde{c}_{ij}$ (8.9) are inserted between outward nodes of RC branches to define currents corresponding to the third term of (8.8).

Unlike the case of RC node elimination the passivity of the circuit after inductance elimination is not secured. So it is needed to test a passivity condition before the elimination is accepted. It is known that the circuit is passive if its conductance and capacitance matrices are nonnegative definite and the capacitance matrix is symmetric. In our case the conductance matrix is kept unchanged and the capacitance matrix is symmetric by the construction. Hence, the criterion for a symmetric matrix A to be nonnegative definite is applied to the capacitance matrix, i.e. $A_{ii} \geq 0$, $|A_{ij}| \leq \sqrt{A_{ii}A_{jj}}$. It is equivalent to the conditions on branch and nodal capacitances

$$C_i^{\mathrm{NEW}} \geq 0, \quad |c_{ij}^{\mathrm{NEW}}| \leq \sqrt{C_i^{\mathrm{NEW}} C_j^{\mathrm{NEW}}}, \tag{8.10}$$

where $c_{ij}^{\mathrm{NEW}} = c_{ij} + \tilde{c}_{ij}$.

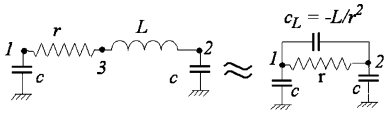

Fig. 8.3 RLC-section reducing

If (8.10) is not valid for the reduced circuit then the elimination must be rejected.

If the inductance L_n has a number of couplings with additional circuit iductances then each coupling must be processed in the same way.

A simple example of an inductance elimination is presented in Fig. 8.3. Conditions (8.10) for the reduced circuit yield $c \geq 2L/r^2$.

8.4 Elimination of Coupled Inductances

Here we consider the case that the inductance L_n is coupled with some other inductance L_k. This coupling is defined by the mutual inductance L_{nk} (Fig. 8.4).

In this case (8.3, 8.4) are valid, (8.5) is replaced by

$$v_n - v_m = sL_n w_m + sL_{nk} w_k \tag{8.11}$$

and the equation for the voltage of inductance L_k must be added:

$$u_k = sL_k w_k + sL_{nk} w_m. \tag{8.12}$$

Then the substitution of (8.4) into (8.11) leads to

$$v_n = v_m(1 + sL_n G_n) - sL_n \sum_{j \in S_n} g_j v_j + sL_{nk} w_k + O(s^2). \tag{8.13}$$

Substituting (8.13) into (8.3) we obtain a first order expression for the nodal current containing an additional term in comparison to (8.8)

$$w_i = \hat{w}_i + s\tilde{\theta}_{(i,m)k} w_k, \tag{8.14}$$

where $\hat{w}_i$ is the right hand side of (8.8),

$$\tilde{\theta}_{(i,m)k} = L_{nk} g_i. \tag{8.15}$$

The substitution of (8.4) into (8.12) leads to an expression for the inductance voltage containing a similar term:

$$u_k = sL_k w_k + s \sum_{j \in S_n} \tilde{\theta}_{(j,m)k}(v_j - v_m). \tag{8.16}$$

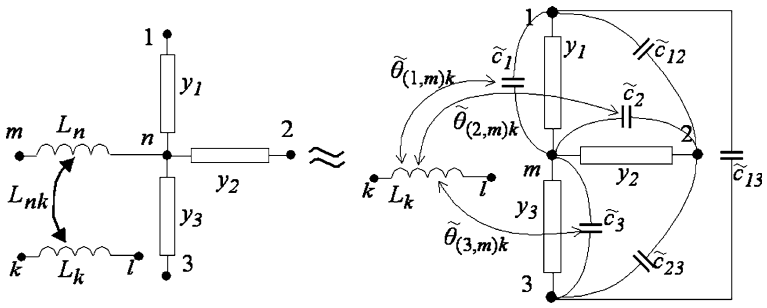

Fig. 8.4 Circuit transform by the elimination of the coupled inductance

The parameter $\tilde{\theta}_{(j,m)k}$ in (8.14, 8.16) corresponds to the coupling (Fig. 8.4) between RC- and L-branches (LC-coupling) that can be defined by the following time-domain expressions for the capacitance current (i_C) and the inductance voltage (u_L):

$$i_C = C\frac{du_C}{dt} + \theta\frac{di_L}{dt}, \quad u_L = L\frac{di_L}{dt} + \theta\frac{du_C}{dt}. \tag{8.17}$$

Our notation $\theta_{(i,m)k}$ refers to kth inductance coupled with the capacitance between nodes m, i. As far as we know there are no physical devices with such interaction. Formally it can be defined in the context of MNA approach as follows.

The MNA conductance and capacitance matrices of the RLCK circuit are

$$G^{\mathrm{MNA}} = \begin{bmatrix} G & I \\ -I^T & 0 \end{bmatrix}, \; C^{\mathrm{MNA}} = \begin{bmatrix} C & \Theta \\ \Theta^T & L \end{bmatrix}. \tag{8.18}$$

Here, submatrix I is the incidence matrix for the inductances. Submatrix Θ is the zero matrix for physically realizable RLCK circuits. With the Gaussian elimination the entries of Θ are replaced by nonzero values. Such nonzero values can be defined by LC-couplings

$$\Theta_{ik} = \sum_{j\in S_i} \theta_{(i,j)k}, \quad \theta_{(i,j)k} = -\theta_{(j,i)k}. \tag{8.19}$$

It can be seen from Fig. 8.4 and (8.14), (8.16) that the coupling of an eliminated inductance is replaced by LC-couplings with each RC-branch of the eliminated node. Due to the symmetry of C^{MNA} the passivity condition can be presented in the form

$$|\Theta_{ik}| \le \sqrt{L_k C_i}, \quad |\Theta_{jk}| \le \sqrt{L_k C_j}. \tag{8.20}$$

Standard SPICE-like simulators cannot process LC-couplings. Note that this capability can be easily implemented taking into account the corresponding time-domain expressions (8.17) and the MNA capacitance matrix (8.18).

8.5 Eliminations Under LC Couplings

The possible appearence of LC-couplings due to previous eliminations requires to analyze the case when the inductance to be eliminated has LC-coupling with any RC-branch (Fig. 8.5).

In this case, (8.5) must be replaced by

$$v_n - v_m = sL_n w_m + s\theta_{(k,l)n}(v_k - v_l). \tag{8.21}$$

After transformations similar to (8.6–8.8) we obtain

$$w_i = \hat{w}_i + sg_i\theta_{(k,l)n}(v_k - v_l) = \hat{w}_i + sg_i\theta_{(k,l)m}(v_k - v_i) + s(-g_i\theta_{(k,l)n})(v_l - v_i). \tag{8.22}$$

The current entering node m is defined as

$$w_m = -\sum_{j\in S_n} w_j = -\sum_{j\in S_n} \hat{w}_j + s(-G_n\theta_{(k,l)n})(v_k - v_m) + sG_n\theta_{(k,l)n}(v_l - v_m). \tag{8.23}$$

The last terms in (8.22, 8.23) represent the currents through the capacitances

$$\tilde{c}_{ki} = -\tilde{c}_{li} = g_i\theta_{(k,l)n}, \quad \tilde{c}_{lm} = -\tilde{c}_{km} = G_n\theta_{(k,l)n}. \tag{8.24}$$

Thus, after elimination of the inductance with LC-coupling the reduced circuit contains additional capacitances (8.24) as shown in Fig. 8.5. A special case of an elimination can be considered when the inductance is LC-coupled to one (kth) of its adjacent RC-branches. The resulting circuit contains capacitances

$$\tilde{c}_{ki} = -\tilde{c}_i = g_i\theta_{(k,n)n} \ (i \in S_n^k), \quad \tilde{c}_k = (g_k - G_n)\theta_{(k,n)n}. \tag{8.25}$$

These capacitances do not form additional entries of the capacitance matrix because shunt capacitances (8.9) are always created under inductance elimination.

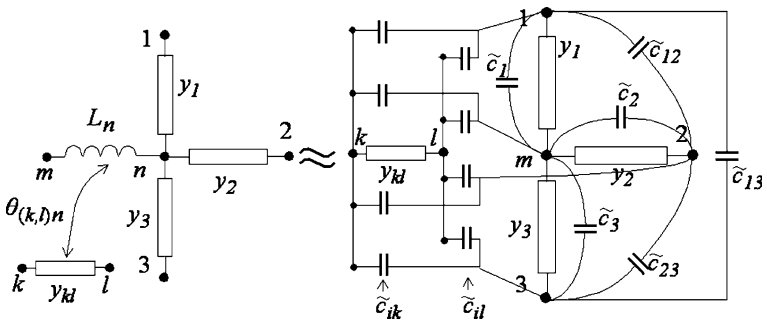

Fig. 8.5 Circuit transform by the elimination of the LC-coupled inductance

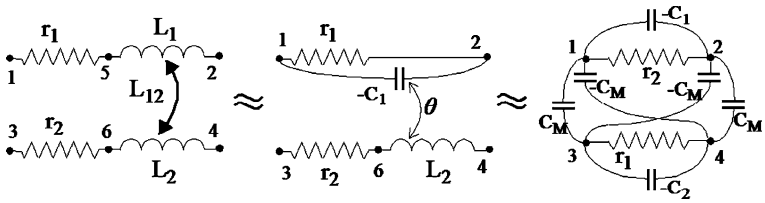

Fig. 8.6 Successive inductance eliminations transform inductively coupled branches into capacitively coupled branches. Here $\theta = L_{12}/r_1,\ c_1 = L_1/r_1^2,\ c_2 = L_2/r_2^2,\ c_M = L_{12}/r_1 r_2$

Note that if the circuit contains two coupled inductances then after their elimination the reduced circuit contains RC branches only. If all inductances of the circuit are eliminated then the reduced RLCK circuit is an RC circuit. An example of a reduction of two coupled LR branches by elimination of both inductances is presented in Fig. 8.6.

In the analysis presented above we ignored the nodes with multiple inductances. But this case does not require a special analysis because the presented algorithms are sufficient to provide the elimination of all small inductances. This can be explained in the following way. Since we do not consider DC undefined circuits containing inductance loops each connected graph of inductances is a tree that always has leaf nodes with only one inductance. Therefore if all inductances of that tree are sufficiently small the single-inductance algorithms will sequentially eliminate them.

LC-couplings must be taken into account in RC-node elimination (8.1, 8.2).

If the mth branch of node n which is to be eliminated is LC-coupled with the kth inductance (Fig. 8.7, $m = 1$), then the branch current is

$$w_m = y_m(v_m - v_n) + s\theta_{(m,n)k} w_k. \tag{8.26}$$

The currents of the other RC-branches are defined by (8.3), and the KCL for node n is

$$s\theta_{(m,n)k} w_k + \sum_{j \in S_n} y_j (v_j - v_n) = 0. \tag{8.27}$$

Substituting v_n derived from (8.27) into (8.2, 8.26), and neglecting higher order terms, we obtain

$$w_i = \sum_{j \in S_n^i} (\tilde{g}_{ij} + s\tilde{c}_{ij})(v_i - v_j) - s\theta_{(m,n)k} \frac{g_i}{G_n} w_k, \quad j \in S_n^m, \tag{8.28}$$

$$w_m = \sum_{j \in S_n^m} (\tilde{g}_{mj} + s\tilde{c}_{mj})(v_m - v_j) + s\theta_{(m,n)k} \frac{G_n - g_m}{G_n} w_k. \tag{8.29}$$

Here $\tilde{g}_{ij}$, $\tilde{c}_{ij}$ are defined by (8.2), and the second right hand terms (8.28, 8.29) correspond to LC-couplings in the reduced circuit (Fig. 8.7):

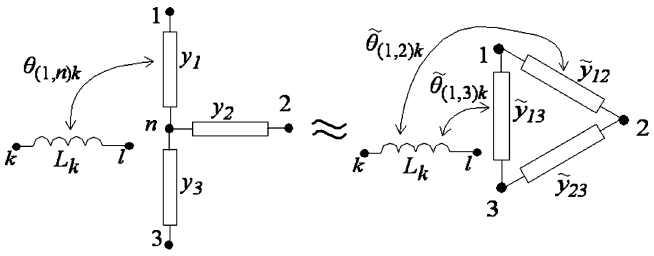

Fig. 8.7 Circuit transform by node elimination under LC-coupling

$$\tilde{\theta}_{(m,i)k} = \theta_{(m,n)k}\frac{g_i}{G_n}. \tag{8.30}$$

Thus after node elimination the branch coupling parameter is distributed among new branches adjacent to node m in proportion to their conductances.

8.6 Algorithmic Aspects

Presented above considerations allow us to extend the TICER reduction algorithm to include nodes with small inductances. The extention requires to adapt important details of the overall TICER algorithm for new types of eliminated nodes. First of all it is needed to provide an error control in the reduction algorithm.

The error due to the first order elimination is defined by the neglected higher order terms. For node elimination (8.2) one can evaluate the mth order term as $\delta_m^{(n)} = O(|s\tau_n|^m)$ [3], where $\tau_n = \tau_n^{RC} = C_n/G_n$ is the RC time-constant of the nth node. In TICER nodes to be eliminated are chosen by the condition $\tau_n < \tau_{\min}$ [3], where $\tau_{\min}$ is evaluated in accordance to the maximum operating frequency of interest $\tau_{\min} = a/f_{\max}$. Factor a is defined by the trade-off between the accuracy and the circuit reduction ratio.

To include the inductance elimination in the general algorithm it is necessary to define a nodal time-constant for the nodes with connected inductance. It can be shown that mth order terms neglected in the inductance elimination (8.7, 8.8) are evaluated as $\delta_m^{(n)} = O(|s\tau_n^{RC}|^k|s\tau_n^{RL}|^l)$, $(k + l = m)$, where τ_n^{RC} is defined earlier, and $\tau_n^{RL} = L_n G_n$ (RL time-constant). Thus, the nodal time-constant in this case can be evaluated as the worst-case value

$$\tau_n = \max(\tau_n^{RC}, \tau_n^{RL}). \tag{8.31}$$

This expression can be applied to each node if we assume $\tau_n^{RL} = 0$ for an RC node.

Another important aspect of TICER that can be extended for inductance eliminations is the restriction of the density of the reduced system. It is achieved

by introducing user-supplied maximal nodal degree. The nodal degree is defined as the number of incident resistors (N_R) that provides no more than $N^R_{\text{new}} = N_R(N_R - 1)$ new entries in the conductance matrix. Pure capacitance branches are not considered. We think that it is desirable to take into account the entries in the superposition of conductance and capacitance matrices because simulations both in time and frequency domains require linear combination of the matrices. In this case the maximal number of new entries is evaluated by $N^{RC}_{\text{new}} = N_{RC}(N_{RC} - 1)$, where N_{RC} is the number of incident RC-branches.

The inductance elimination generates new entries (Fig. 8.2) due to capacitances $\tilde{c}_{ij}$ (8.9). The entry is not produced for branches with zero conductances, hence the maximal number of new entries is $N_R(N_R - 1)$. Besides $2N_R$ new entries are produced by each inductance coupled with the eliminated one (Fig. 8.4) in accordance with (8.15). The factor 2 appears because LC-coupling $\theta_{(i,j)k}$ corresponds with two entries $\Theta_{i,k}$, $\Theta_{j,k}$ (8.19). Each LC-coupling (Fig. 8.5) produces $2(N_R + 1)$ new entries due to (8.24). Thus the number of new entries after inductance elimination can be evaluated as

$$N^L_{\text{new}} = N_R(N_{LL} + 1) + 2N_{LC}(N_{RC} + 1). \tag{8.32}$$

Here N_{LL} is the number of inductance couplings of eliminated inductance, N_{LC} is the number of the LC couplings not counting the couplings with incident branches.

In the general case incident branches of an RC node can posess LC couplings with circuit inductances (Fig. 8.7). All couplings with one inductance produce N_R new entries in the matrix Θ. Thus the total number of new entries after RC-node elimination is

$$N^{RC}_{\text{new}} = N_{RC}(N_{RC} - 1) + N_R N_{LC}, \tag{8.33}$$

where N_{LC} is the number of inductances coupled with any RC-branch of eliminated node.

The TICER algorithm [3] extended to include inductance eliminations contains the following operations. The sorted queue of internal nodes with no more than one connected inductance is supported after each elimination step. The fields of the sorting key are the number of new entries (8.32, 8.33) and nodal time constant (8.31). Maximal values of the keys are user-defined data.

The elimination is performed for the first node in the queue by applying either (8.2, 8.30) for an RC-node or (8.9, 8.15, 8.24, 8.25) for the node with inductance. If passivity conditions (8.10, 8.20) are not satisfied then the elimination is ignored and the next node in the queue is processed. The algorithm stops if the queue is empty or all nodes in the queue do not satisfy passivity conditions.

Experiments show that computational efforts of inductance elimination are typically 2–4 times greater than efforts of RC-node (TICER) elimination. This is resulted from more complicated analysis of the circuit structure and the need of passivity verification.

8.7 Numerical Examples

Two circuit examples are presented below to illustrate the proposed inductance elimination algorithms.

The first example is an RLC line containing ten identical sections presented in Fig. 8.3 with parameters $r = 1\,\Omega, L = 0.4\,\text{pH}, C = 1\,\text{pF}$. Note that inductance value is slightly smaller than the maximum value guaranteeing passivity ($L \leq 0.5\,\text{pH}$).

Two reduced circuits were obtained:

- RC line using the elimination of all inductances by the proposed method;
- RC line using the neglect of all inductances.

The frequency- and time-domain response of the original RLC line as well as two reduced circuits are computed. The time-domain simulation was performed under a unit step excitation with t_{rise} = 3 psec.

The reduction error for each method was evaluated as the difference between the responses of the original and reduced circuits (Fig. 8.8). One can see that the elimination error is about tenfold less than the neglect error both in frequency (Fig. 8.8a) and time-domain (Fig. 8.8b).

The second example presents inductively coupled branches shown on the left of Fig. 8.6 with parameters $r_1 = r_2 = 5\,\Omega$, $L_1 = L_2 = 1\,\text{pH}$, $L_{12} = 0.5\,\text{pH}$. Furthermore, load capacitances $1pF$ connected to nodes 2, 4 are added. Nodes 1 and 4 are assumed as input and output ports respectively. The reduced circuit is obtained in the form shown on the right of Fig. 8.6. Output frequency responses are shown in Fig. 8.9a. Time-domain crosstalk waveforms under an input pulse with unit magnitude and $t_{\text{pulse}} = 20\,\text{psec}, t_{\text{rise}} = 1\,\text{psec}, t_{\text{fall}} = 4\,\text{psec}$ are given in Fig. 8.9b. Note that in spite of large errors in the frequency response of the reduced circuit at $f > 100$ GHz the error in the time domain crosstalk waveform is sufficiently small because time-constants of eliminated nodes $L_1/r_1 = L_2/r_2 = 0.2\,\text{psec}$ are essentially less then t_{rise} and t_{fall}.

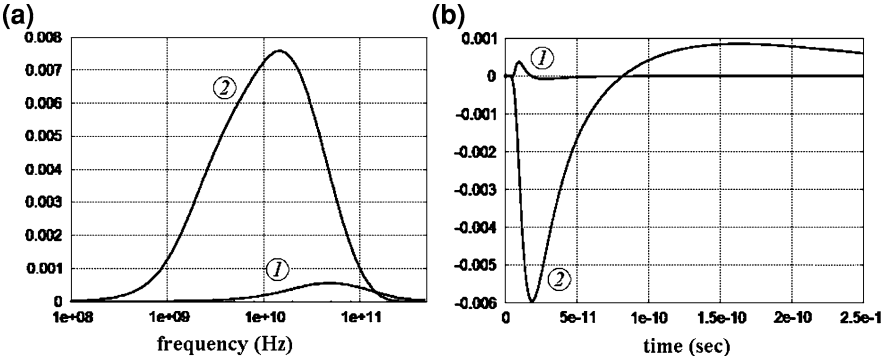

Fig. 8.8 RLC-line reduction errors due to the elimination (1) and the neglect (2)

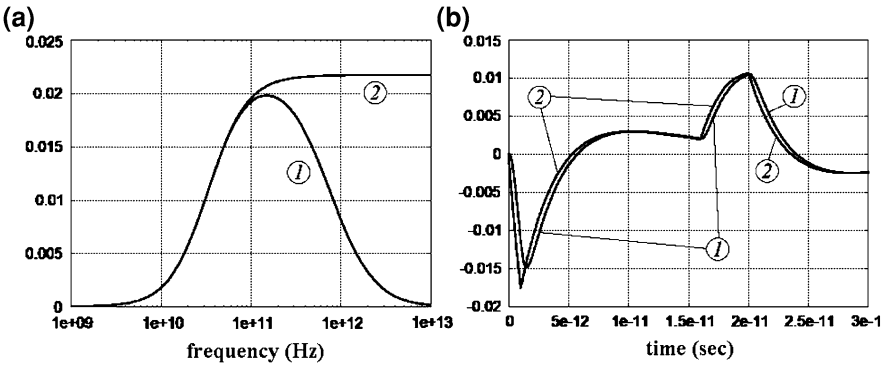

Fig. 8.9 Crosstalk frequency (a) and time-domain (b) responses in inductively coupled branches (1) and in the reduced circuit (2)

8.8 Conclusion

A new class of elimination algorithms for circuits with small inductances is presented in the paper. The proposed algorithms provide a reduction of an arbitrary RLCK circuit preserving first order accuracy of the circuit transfer functions. A passivity condition for the reduced circuit is given, which can be easily verified at each elimination step. Minor corrections in circuit simulators are required to perform the simulation of the reduced circuits. This work was supported by RFBR under grant 08-07-00171a.

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